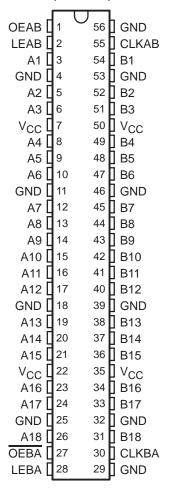
SCBS784 - NOVEMBER 2003

- **Controlled Baseline**
 - One Assembly/Test Site, One Fabrication
- **Enhanced Diminishing Manufacturing** Sources (DMS) Support
- **Enhanced Product-Change Notification**
- Qualification Pedigree[†]
- **Member of the Texas Instruments** Widebus™ Family
- **UBT** ™ Transceiver Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or **Clocked Mode**
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V **Operation and Low Static-Power** Dissipation
- **Supports Mixed-Mode Signal Operation** (5-V Input and Output Voltages With 3.3-V V_{CC})
- **Supports Unregulated Battery Operation** Down To 2.7 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3 \text{ V}, T_A = 25^{\circ}\text{C}$
- Ioff and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the **Need for External Pullup/Pulldown** Resistors
- Distributed V_{CC} and GND Pins Minimize **High-Speed Switching Noise**

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- **ESD Protection Exceeds JESD 22**
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

DGG PACKAGE (TOP VIEW)



description/ordering information

The SN74LVTH16501 is an 18-bit universal bus transceiver designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.



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SN74LVTH16501-EP 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCBS784 - NOVEMBER 2003

description/ordering information (continued)

ORDERING INFORMATION

TA	PACKAGE	:†	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	TSSOP - DGG	Tape and reel	CLVTH16501IDGGREP	LH16501EP

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B, but uses OEBA, LEBA, and CLKBA. The output enables are complementary (OEAB is active high and OEBA is active low).

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor and OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

This device is fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

FUNCTION TABLE†

	INPUTS								
OEAB	LEAB	CLKAB	Α	В					
L	Χ	Χ	Χ	Z					
Н	Н	Χ	L	L					
Н	Н	X	Н	Н					
Н	L	\uparrow	L	L					
Н	L	\uparrow	Н	Н					
Н	L	Н	Χ	B ₀ ‡					
Н	L	L	Χ	В ₀ §					

[†] A-to-B data flow is shown; B-to-A flow is similar, but uses OEBA, LEBA, and CLKBA.

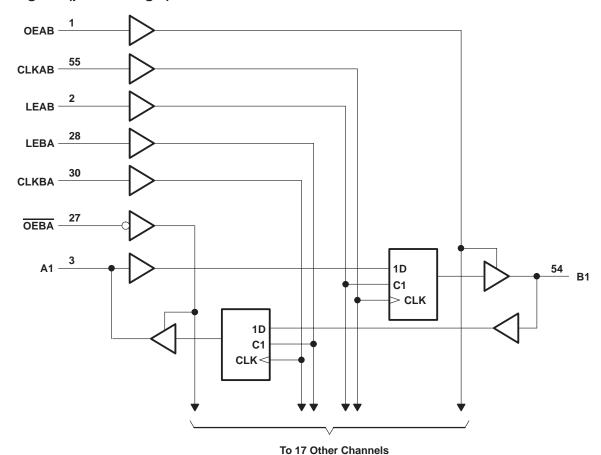


[‡]Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low

[§] Output level before the indicated steady-state input conditions were established

SCBS784 - NOVEMBER 2003

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} –0.5 V to	o 4.6 V
Input voltage range, V _I (see Note 1)	to 7 V
Voltage range applied to any output in the high-impedance	
or power-off state, V _O (see Note 1)	to 7 V
Voltage range applied to any output in the high state, V _O (see Note 1)0.5 V to V _{CC} -	+ 0.5 V
Current into any output in the low state, I _O	28 mA
Current into any output in the high state, I _O (see Note 2)	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	·50 mA
Output clamp current, I_{OK} ($V_O < 0$)	·50 mA
Package thermal impedance, θ _{JA} (see Note 3)	4°C/W
Storage temperature range, T _{stg} –65°C to	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
 - 3. The package thermal impedance is calculated in accordance with JESD 51-7.



SN74LVTH16501-EP 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCBS784 - NOVEMBER 2003

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	V
V _{IH}	High-level input voltage		2		V
V _{IL}	Low-level input voltage			0.8	V
VI	Input voltage			5.5	V
ЮН	High-level output current			-32	mA
loL	Low-level output current			64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10	ns/V
Δt/ΔV _{CC}	Power-up ramp rate		200		μs/V
TA	Operating free-air temperature	_	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAI	RAMETER	TEST CONDITIO	ONS	MIN	TYP [†]	MAX	UNIT	
VIK		V _{CC} = 2.7 V,	I _I = -18 mA			-1.2	V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V},$	I _{OH} = -100 μA	V _{CC} -0.2	2			
VOH		V _{CC} = 2.7 V,	$I_{OH} = -8 \text{ mA}$	2.4			V	
		V _{CC} = 3 V,	$I_{OH} = -32 \text{ mA}$	2				
		I _{OL} = 100 μA				0.2		
		V _{CC} = 2.7 V	$I_{OL} = 24 \text{ mA}$			0.5		
V_{OL}			I _{OL} = 16 mA			0.4	V	
		V _{CC} = 3 V	$I_{OL} = 32 \text{ mA}$			0.5		
			$I_{OL} = 64 \text{ mA}$			0.55		
		V _{CC} = 3.6 V,	$V_I = V_{CC}$ or GND			±1		
	Control inputs	V _{CC} = 0 or 3.6 V,	V _I = 5.5 V			10		
l _l			V _I = 5.5 V			20	μΑ	
	A or B ports‡	V _{CC} = 3.6 V	VI = VCC			1		
			V _I = 0			-5		
l _{off}		$V_{CC} = 0$,	V_I or $V_O = 0$ to 4.5 V			±100	μΑ	
		V 0V	V _I = 0.8 V	75				
I _{I(hold)}	A or B ports	VCC = 3 V	V _I = 2 V	-75			μΑ	
. ,		$V_{CC} = 3.6 \text{ V}$, $V_{I} = 0 \text{ to } 3.6 \text{ V}$				±500		
lozpu		$V_{CC} = 0$ to 1.5 V, $V_{O} = 0.5$ V to 3 V, $\overline{OE}/OE = 0.5$	= don't care			±100	μΑ	
lozpd		$V_{CC} = 1.5 \text{ V to } 0, V_{O} = 0.5 \text{ V to } 3 \text{ V}, \overline{\text{OE}/\text{OE}}$	= don't care			±100	μΑ	
02. 2			Outputs high			0.19	-	
ICC		$V_{CC} = 3.6 \text{ V}, I_{O} = 0, V_{I} = V_{CC} \text{ or GND}$	Outputs low			5	mA	
00			Outputs disabled			0.19	1	
ΔI _{CC} ¶ V _{CC}		$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$, One input at $V_{CC} - 0.6 \text{ V}$	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$, One input at $V_{CC} - 0.6 \text{ V}$, Other inputs at V_{CC} or GND			0.2	mA	
Ci		V _I = 3 V or 0			4		pF	
C _{io}		V _O = 3 V or 0			10		pF	

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ Unused pins at V_{CC} or GND

This is the increase in supply current for each input that is at the specified TTL voltage level, rather than VCC or GND.



[§] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

SN74LVTH16501-EP 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS SCBS784 - NOVEMBER 2003

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

				V _{CC} =		VCC =	2.7 V	UNIT
				MIN	MAX	MIN	MAX	
fclock	Clock frequency				150		150	MHz
	Poles donether	LE high		3.3		3.3		
t _W	Pulse duration	CLK high or low				3.3		ns
		A before CLKAB↑				2.4		
		B before CLKBA↑		2.1		2.4		
t _{su}	Setup time	. 5. (.5.	CLK high	2.4		1.6		ns
		A or B before LE↓	CLK low	1.4		0.5		
	Held Co.	A or B after CLK↑	1		0			
th	Hold time	A or B after LE↓		1.7		1.7		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

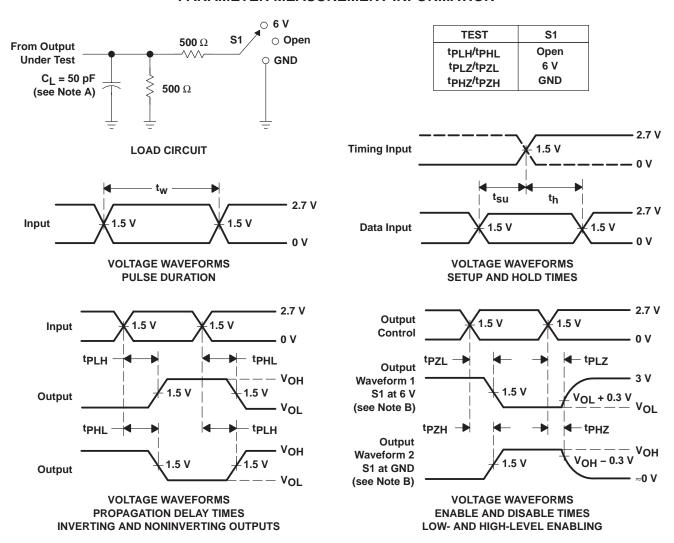
PARAMETER	FROM	TO		± 0.3 V	V	V _{CC} =	UNIT	
	(INPUT)	(OUTPUT)	MIN	TYP†	MAX	MIN	MAX	
f _{max}			150			150		MHz
^t PLH	B or A	A == D	1.3	2.7	3.7		4	
^t PHL	B OF A	A or B	1.3	2.4	3.7		4	ns
^t PLH	LEBA or LEAB	A == D	1.5	3.4	5.1		5.7	
^t PHL	LEBA OI LEAB	A or B	1.5	3.5	5.1		5.7	ns
^t PLH	CL KDA ar CL KAD	A == D	1.3	3.5	5.1		5.7	
^t PHL	CLKBA or CLKAB	A or B	1.3	3.4	5.1		5.7	ns
^t PZH	OEBA or OEAB	A an B	1.3	3.4	4.8		5.5	
tPZL	OEBA or OEAB	A or B	1.3	3.4	4.8		5.5	ns
^t PHZ	OEBA or OEAB	A or B	1.7	4.2	5.8		6.3	200
t _{PLZ}	OEDA UI OEAB	OEBA or OEAB A or B		3.8	5.8		6.3	ns

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.



SCBS784 - NOVEMBER 2003

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50~\Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms







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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins F	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CLVTH16501IDGGREP	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/04714-01XE	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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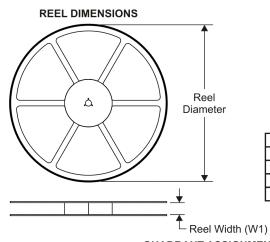
Catalog: SN74LVTH16501Military: SN54LVTH16501

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications



TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

	Device		Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CLVTH	H16501IDGGREP	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1





*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CLVTH16501IDGGREP	TSSOP	DGG	56	2000	346.0	346.0	41.0

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