

FFATURES

SCES122F-JULY 1997-REVISED OCTOBER 2004

FEATURES	DGG, DGV, OR DL PACKAGE
 Member of the Texas Instruments Widebus™ Family 	(TOP VIEW)
 EPIC[™] (Enhanced-Performance Implanted 	
CMOS) Submicron Process	Y1 2 55 A1
 Output Port Has Equivalent 26-Ω Series 	Y2 🛛 3 54 🛛 A2
Resistors, So No External Resistors Are	GND 4 53 2 GND
Required	Y3 5 52 A3
 Designed to Comply With JEDEC 168-Pin and 	Y4] 6 51] A4
200-Pin SDRAM Buffered DIMM Specification	V _{CC} [] 7 50 [] V _{CC}
ESD Protection Exceeds 2000 V Per	Y5 8 49 A5
MIL-STD-883, Method 3015; Exceeds 200 V	Y6 9 48 A6
Using Machine Model (C = 200 pF, R = 0)	Y7 0 10 47 A7
 Latch-Up Performance Exceeds 250 mA Per 	GND 11 46 GND
JESD 17	Y8 12 45 A8
	Y9 13 44 A9
Bus Hold on Data Inputs Eliminates the Need for External Bullum/Bulldown Resisters	Y10 14 43 A10
for External Pullup/Pulldown Resistors	Y11 15 42 A11
Package Options Include Plastic Shrink	Y12 16 41 A12
Small-Outline (DL), Thin Shrink Small-Outline	Y13 17 40 A13
(DGG), and Thin Very Small-Outline (DGV)	
Packages	Y14 19 38 A14
NOTE: For tape-and-reel order entry, the DGGR package is	Y15 20 37 A15
abbreviated to GR, and the DGVR package is abbreviated	Y16 21 36 A16
to VR.	V_{CC} 22 35 V_{CC}
DESCRIPTION	Y17 23 34 A17
DESCRIPTION	
This 20-bit universal bus driver is designed for 1.65-V	
to 3.6-V V _{CC} operation.	Y19 26 31 A19

NC – No internal connection

30 A20

29 LE

Y20 127

28

The output port includes equivalent 26- Ω series resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH162836 is characterized for operation from -40°C to 85°C.

Data flow from A to Y is controlled by the output-enable (\overline{OE}) input. The device operates in the

transparent mode when the latch-enable (LE) input is

low. When \overline{LE} is high, the A data is latched if the clock (CLK) input is held at a high or low logic level. If \overline{LE} is high, the A data is stored in the latch/flip-flop on the low-to-high transition of CLK. When \overline{OE} is high,

the outputs are in the high-impedance state.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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FUNCTION TABLE

	INPUTS								
ŌĒ	LE	CLK	CLK A						
Н	Х	Х	Х	Z					
L	L	Х	L	L					
L	L	Х	Н	н					
L	Н	\uparrow	L	L					
L	Н	\uparrow	Н	н					
L	Н	L or H	Х	Y ₀ ⁽¹⁾					

(1) Output level before the indicated steady-state input conditions were established

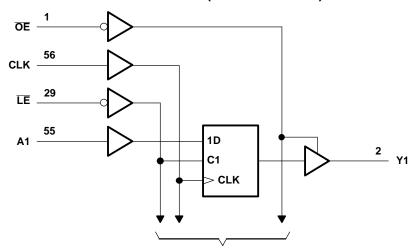
OE CLK LE	1 56 29	•	EN1 > 2C3 C3 G2				
Y1	2		רק קוריים	1	3D	55	A1
	3				30	54	
Y2 Y3	5					52	A2 A3
	6					51	
Y4	8		┣───			49	A4
Y5	9					48	A5
Y6	10	•				47	A6
Y7	12	•				45	A7
Y8	13	•	 			44	A8
Y9	14	•	 			43	A9
Y10	15	•	┣───			42	A10
Y11	16	•	 			41	A11
Y12	17	•	└───			40	A12
Y13	19	•	└───			38	A13
Y14	20	•	 			37	A14
Y15	21	•	 			36	A15
Y16	23	4	1			34	A16
Y17	24	•				33	A17
Y18	26	•	 			31	A18
Y19	27	4	 			30	A19
Y20		•					A20

LOGIC SYMBOL⁽¹⁾

(1) This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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LOGIC DIAGRAM (POSITIVE LOGIC)



To 19 Other Channels

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	4.6	V
VI	Input voltage range ⁽²⁾		-0.5	4.6	V
Vo	Output-voltage range ⁽²⁾⁽³⁾		-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V ₁ < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
I _O	Continuous output current			±50	mA
	Continuous current through each V_{CC} or	GND		±100	mA
		DGG package		81	
θ_{JA}	Package thermal impedance ⁽⁴⁾	DGV package		86	°C/W
		DL package		74	
T _{stg}	Storage temperature range		-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

(3) This value is limited to 4.6 V maximum.

(4) The package thermal impedance is calculated in accordance with JESD 51.

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RECOMMENDED OPERATING CONDITIONS⁽¹⁾

			MIN	MAX	UNIT
V_{CC}	Supply voltage		1.65	3.6	V
		V_{CC} = 1.65 V to 1.95 V	$0.65 imes V_{CC}$		
V _{IH}	High-level input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		
		V_{CC} = 1.65 V to 1.95 V		$0.35 \times V_{CC}$	
V _{IL}	Low-level input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	
VI	Input voltage		0	V _{CC}	V
Vo	Output voltage		0	V _{CC}	V
		$V_{CC} = 1.65 V$		-2	
	Llich lovel output ourrent	$V_{CC} = 2.3 V$		-6	
I _{OH}	High-level output current	$V_{CC} = 2.7 V$		-8	mA
		$V_{CC} = 3 V$		-12	
		V _{CC} = 1.65 V		2	
	Low level output ourrept	$V_{CC} = 2.3 V$		6	mA
I _{OL}	Low-level output current	$V_{CC} = 2.7 V$		8	ША
		$V_{CC} = 3 V$		12	
$\Delta t/\Delta v$	Input transition rise or fall rate	· · · · ·		10	ns/V
T _A	Operating free-air temperature		-40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETI	ER TEST CONDITIONS	V _{cc}	MIN	TYP ⁽¹⁾ MAX	UNIT
	I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} - 0.2		
	I _{OH} = -2 mA	1.65 V	1.2		
	I _{OH} = -4 mA	2.3 V	1.9		
V _{OH}	1 6 m 1	2.3 V	1.7		V
	I _{OH} = -6 mA	3 V	2.4		
	I _{OH} = -8 mA	2.7 V	2		
	I _{OH} = -12 mA	3 V	2		
	I _{OL} = 100 μA	1.65 V to 3.6 V		0.2	
	$I_{OL} = 2 \text{ mA}$	1.65 V		0.45	
	$I_{OL} = 4 \text{ mA}$	2.3 V		0.4	
V _{OL}		2.3 V		0.55	V
	$I_{OL} = 6 \text{ mA}$	3 V		0.55	
	I _{OL} = 8 mA	2.7 V		0.6	
	I _{OL} = 12 mA	3 V		0.8	
l _l	$V_{I} = V_{CC} \text{ or } GND$	3.6 V		±5	μΑ
	V _I = 0.58 V	1.65 V	25		
	V _I = 1.07 V	1.65 V	-25		
	V _I = 0.7 V	2.3 V	45		
I _{I(hold)}	V _I = 1.7 V	2.3 V	-45		μA
	V _I = 0.8 V	3 V	75		
	V _I = 2 V	3 V	-75		
	$V_{I} = 0$ to 3.6 V ⁽²⁾	3.6 V		±500	
I _{OZ}	$V_{O} = V_{CC}$ or GND	3.6 V		±10	μA
I _{CC}	$V_{I} = V_{CC} \text{ or } GND, \qquad I_{O} = 0$	3.6 V		40	μA
ΔI_{CC}	One input at V _{CC} - 0.6 V, Other inputs at	V _{CC} or GND 3 V to 3.6 V		750	μA
C Control in	puts	2.2.1/		5.5	~ F
C _i Data inpu	$V_1 = V_{CC} \text{ or GND}$	3.3 V		6	pF
C _o Outputs	$V_{O} = V_{CC}$ or GND	3.3 V		8	pF

(1) All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$. (2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

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TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 through Figure 3)

				V _{CC} =	1.8 V	V _{CC} = ± 0.	2.5 V 2 V	V _{CC} =	2.7 V	V _{CC} = 2 ± 0.3	3.3 V 3 V	UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock} Clock frequency				(1)		150		150		150	MHz	
	Dulas duration	LE low		(1)		3.3		3.3		3.3		~~~
t _w	Pulse duration	CLK high or low		(1)		3.3		3.3		3.3		ns
		Data before CLK↑		(1)		1.4		1.7		1.5		
t _{su}	Setup time	Data before LE↑	CLK high	(1)		1.2		1.6		1.3		ns
		Data before LE	CLK low	(1)		1.4		1.5		1.2		
		Data after CLK↑		(1)		0.9		0.9		0.9		
t _h	Hold time	Data after LE↑	CLK high or low	(1)		1.1		1.1		1.1		ns

(1) This information was not available at the time of publication.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 through Figure 3)

PARAMETER	FROM (INPUT)	TO	V _{CC} = 1	I.8 V	V _{CC} = 2 ± 0.2	2.5 V 2 V	V _{CC} = 2	2.7 V	V _{CC} = 3 ± 0.3	3.3 V 3 V	UNIT
	(INFOT)	(OUTPUT)	MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			(1)		150		150		150		MHz
	А			(1)	1	4.4		4.6	1.2	4	
t _{pd}	LE	Y		(1)	1.1	5.8		6.1	1.4	5.1	ns
	CLK			(1)	1	5.2		5.5	1.1	5	
t _{en}	OE	Y		(1)	1.1	6.4		6.5	1.2	5.5	ns
t _{dis}	ŌĒ	Y		(1)	1	4.7		5.2	1.7	5.1	ns

(1) This information was not available at the time of publication.

OPERATING CHARACTERISTICS

 $T_A = 25^{\circ}C$

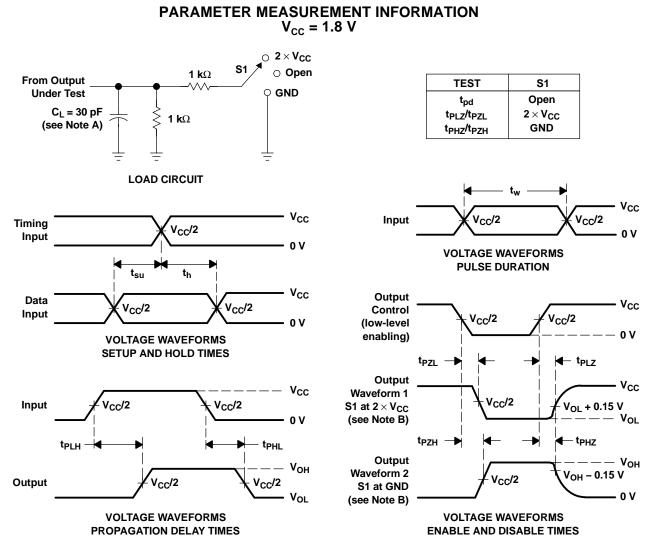
	PARAMETER		TEST	CONDITIONS	V _{CC} = 1.8 V TYP	V _{CC} = 2.5 V TYP	V _{CC} = 3.3 V TYP	UNIT
<u> </u>	Power dissipation	Outputs enabled	C 0	f 10 MU	(1)	31.5	36	۰L
C _{pd}	capacitance	Outputs disabled	$C_L = 0,$	f = 10 MHz	(1)	8	10.5	pF

(1) This information was not available at the time of publication.

TEXAS INSTRUMENTS www.ti.com

SN74ALVCH162836 20-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS

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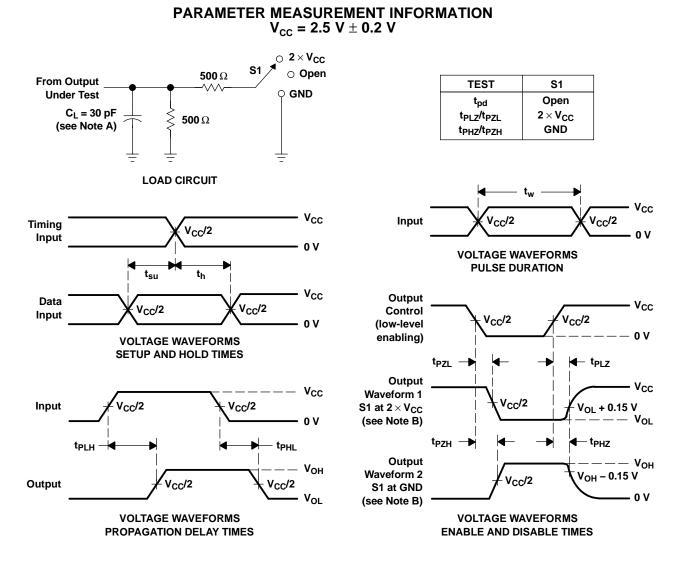
NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2 ns, t_f \leq 2 ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms



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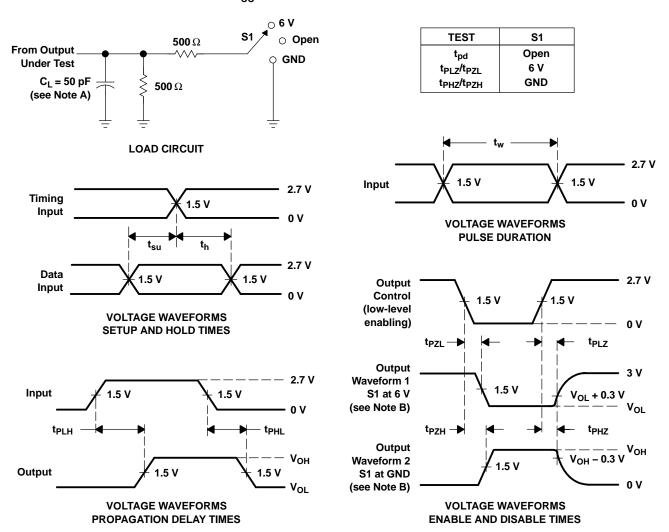
- NOTES: A. CL includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_r \leq 2 ns, t_f \leq 2 ns.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms



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PARAMETER MEASUREMENT INFORMATION V_{cc} = 2.7 V AND 3.3 V \pm 0.3 V



- NOTES: A. CL includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
 D. The outputs are measured one at a time, with one transition per measurement.
 - E. $t_{PLZ} \, \text{and} \, t_{PHZ} \, \text{are the same as} \, t_{dis}.$
 - F. t_{PZL} and t_{PZH} are the same as t_{en}.
 - G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 3. Load Circuit and Voltage Waveforms

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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74ALVCH162836DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVCH162836GRE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVCH162836GRG4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVCH162836VRE4	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVCH162836VRG4	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVCH162836DGGR	OBSOLETE	TSSOP	DGG	56		TBD	Call TI	Call TI
SN74ALVCH162836DGVR	OBSOLETE	TVSOP	DGV	56		TBD	Call TI	Call TI
SN74ALVCH162836DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVCH162836GR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVCH162836VR	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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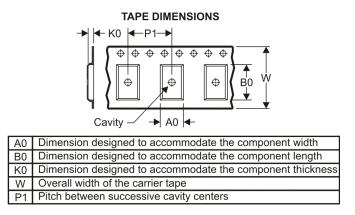
PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALVCH162836GR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
SN74ALVCH162836VR	TVSOP	DGV	56	2000	330.0	24.4	6.8	11.7	1.6	12.0	24.0	Q1

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PACKAGE MATERIALS INFORMATION

29-Jul-2009



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALVCH162836GR	TSSOP	DGG	56	2000	346.0	346.0	41.0
SN74ALVCH162836VR	TVSOP	DGV	56	2000	346.0	346.0	41.0

MECHANICAL DATA

MTSS003D - JANUARY 1995 - REVISED JANUARY 1998

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153



MECHANICAL DATA

MSSO001C - JANUARY 1995 - REVISED DECEMBER 2001

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

DL (R-PDSO-G**)



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MO-118



MECHANICAL DATA

PLASTIC SMALL-OUTLINE

MPDS006C - FEBRUARY 1996 - REVISED AUGUST 2000

DGV (R-PDSO-G**)

24 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
- D. Falls within JEDEC: 24/48 Pins MO-153

14/16/20/56 Pins – MO-194



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