



### **FEATURES**

- Member of the Texas Instruments Widebus™
  Family
- Operates From 1.65 V to 3.6 V
- Max t<sub>pd</sub> of 3.2 ns at 3.3 V
- ±24-mA Output Drive at 3.3 V
- Ideal for Use in PC100 Register DIMM
- Designed to Comply With JEDEC 168-Pin and 200-Pin SDRAM Buffered DIMM Specification
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

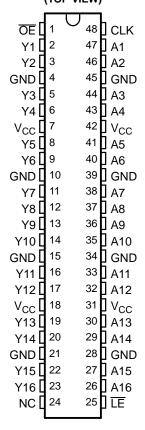
### **DESCRIPTION/ORDERING INFORMATION**

This 16-bit universal bus driver is designed for 1.65-V to 3.6-V  $V_{\rm CC}$  operation.

Data flow from A to Y is controlled by the output-enable  $(\overline{OE})$  input. The device operates in the transparent mode when the latch-enable  $(\overline{LE})$  input is low. When  $\overline{LE}$  is high, the A data is latched if the clock (CLK) input is held at a high or low logic level. If  $\overline{LE}$  is high, the A data is stored in the latch/flip-flop on the low-to-high transition of CLK. When  $\overline{OE}$  is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

# DGG, DGV, OR DL PACKAGE (TOP VIEW)



NC - No internal connection

#### ORDERING INFORMATION

T <sub>A</sub>	PACKA	GE <sup>(1)</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	SSOP - DL	Tube	SN74ALVC16334DL	ALVC16334
40°C to 95°C	330F - DL	Tape and reel	SN74ALVC16334DLR	ALVC10334
-40°C to 85°C	TSSOP - DGG	Tape and reel	SN74ALVC16334DGGR	ALVC16334
	TVSOP - DGV	Tape and reel	SN74ALVC16334DGVR	VC334

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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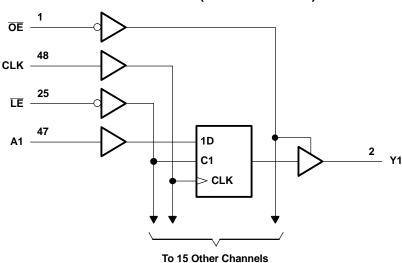


### **FUNCTION TABLE**

	IN	PUTS		OUTPUT
ŌĒ	LE	CLK	Α	Y
Н	Χ	Χ	Χ	Z
L	L	X	L	L
L	L	X	Н	Н
L	Н	$\uparrow$	L	L
L	Н	$\uparrow$	Н	Н
L	Н	L or H	Χ	Y <sub>0</sub> <sup>(1)</sup>

 Output level before the indicated steady-state input conditions were established

# LOGIC DIAGRAM (POSITIVE LOGIC)



# ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage range		-0.5	4.6	V
VI	Input voltage range <sup>(2)</sup>		-0.5	4.6	V
Vo	Output voltage range <sup>(2)(3)</sup>		-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		-50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		-50	mA
I <sub>O</sub>	Continuous output current			±50	mA
	Continuous current through each V <sub>CC</sub> or C	GND		±100	mA
		DGG package		58	
$\theta_{JA}$	Package thermal impedance (4)	DGV package		48	°C/W
		DL package		63	
T <sub>stg</sub>	Storage temperature range		-65	150	°C

<sup>(1)</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

<sup>(2)</sup> The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>(3)</sup> This value is limited to 4.6 V maximum.

<sup>(4)</sup> The package thermal impedance is calculated in accordance with JESD 51-7.



# **RECOMMENDED OPERATING CONDITIONS**(1)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		1.65	3.6	V
		V <sub>CC</sub> = 1.65 V to 1.95 V	$0.65 \times V_{CC}$		
$V_{IH}$	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		
		V <sub>CC</sub> = 1.65 V to 1.95 V		$0.35 \times V_{CC}$	
$V_{IL}$	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	
VI	Input voltage		0	3.6	V
Vo	Output voltage		0	$V_{CC}$	V
		V <sub>CC</sub> = 1.65 V		-4	
	Lligh lovel cutout current	V <sub>CC</sub> = 2.3 V		-12	A
I <sub>OH</sub>	High-level output current	$V_{CC} = 2.7 \text{ V}$		-12	mA
		V <sub>CC</sub> = 3 V		-24	
		V <sub>CC</sub> = 1.65 V		4	
	Low lovel output ourrent	V <sub>CC</sub> = 2.3 V		12	A
l <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2.7 V		12	mA
		V <sub>CC</sub> = 3 V		24	<u> </u>
Δt/Δν	Input transition rise or fall rate			10	ns/V
T <sub>A</sub>	Operating free-air temperature		-40	85	°C

<sup>(1)</sup> All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

# **ELECTRICAL CHARACTERISTICS**

over recommended operating free-air temperature range (unless otherwise noted)

P	ARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup> MAX	UNIT			
		I <sub>OH</sub> = -100 μA	1.65 V to 3.6 V	V <sub>CC</sub> - 0.2					
		I <sub>OH</sub> = -4 mA	1.65 V	1.2					
		I <sub>OH</sub> = -6 mA	2.3 V	2					
$V_{OH}$			2.3 V	1.7		V			
		I <sub>OH</sub> = -12 mA	2.7 V	2.2					
			3 V	2.4					
		I <sub>OH</sub> = -24 mA	3 V	2					
		I <sub>OL</sub> = 100 μA	1.65 V to 3.6 V		0.2				
		I <sub>OL</sub> = 4 mA	1.65 V		0.45				
/		I <sub>OL</sub> = 6 mA	2.3 V		0.4	V			
V <sub>OL</sub>		1 12 1	2.3 V		0.7	V			
		I <sub>OL</sub> = 12 mA	2.7 V		0.4				
		I <sub>OL</sub> = 24 mA	3 V		0.55				
I		V <sub>I</sub> = V <sub>CC</sub> or GND	3.6 V		±5	μΑ			
I <sub>OZ</sub>		V <sub>O</sub> = V <sub>CC</sub> or GND	3.6 V		±10	μΑ			
$I_{CC}$		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		40	μΑ			
$\Delta I_{CC}$		One input at V <sub>CC</sub> - 0.6 V, Other inputs	at V <sub>CC</sub> or GND 3 V to 3.6 V		750	μΑ			
_	Control inputs	V V ~ CND	2.2.7		5	pF			
Ci	Data inputs	$V_I = V_{CC}$ or GND	3.3 V		5.5				
Co	Outputs	V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V		7.5	pF			

<sup>(1)</sup> All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

# SN74ALVC16334 16-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS

SCES128E-FEBRUARY 1998-REVISED SEPTEMBER 2004



# **TIMING REQUIREMENTS**

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

				V <sub>CC</sub> =	V <sub>CC</sub> = 1.8 V		$V_{CC}$ = 2.5 V $\pm$ 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V	
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency				(1)		150		150		150	MHz
. 51		LE low		(1)		3.3		3.3		3.3		20
t <sub>w</sub>	Pulse duration	CLK high or low		(1)		3.3		3.3		3.3		ns
		Data before CLK	1	(1)		1.4		1.7		1.5		
t <sub>su</sub>	Setup time	Data before <del>LE</del> ↑	CLK high	(1)		1.2		1.6		1.3		ns
		Data before LET	CLK low	(1)		1.4		1.5		1.2		
	Hold time	Data after CLK↑		(1)		0.9		0.9		0.9		20
t <sub>h</sub>	Hold time	Data after <del>LE</del> ↑	CLK high or low	(1)		1.1		1.1		1.1		ns

<sup>(1)</sup> This information was not available at the time of publication.

# **SWITCHING CHARACTERISTICS**

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	TO (OUTPUT)	V <sub>CC</sub> =	V <sub>CC</sub> = 1.8 V		$V_{CC}$ = 2.5 V $\pm$ 0.2 V		V <sub>CC</sub> = 2.7 V		$V_{CC}$ = 3.3 V $\pm$ 0.3 V	
	(INPUT)	(OUTPUT)	MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			(1)		150		150		150		MHz
	Α			(1)	1	3.7		3.6	1.1	3.3	
t <sub>pd</sub>	ĪĒ	Y		(1)	1	4.8		5	1.3	4.4	ns
	CLK			(1)	1	4.4		4.5	1	4.1	
t <sub>en</sub>	ŌĒ	Y		(1)	1	5.4		5.4	1.1	4.6	ns
t <sub>dis</sub>	ŌĒ	Y		(1)	1	4.1		4.5	1.7	4.4	ns

<sup>(1)</sup> This information was not available at the time of publication.

# **SWITCHING CHARACTERISTICS**

from  $0^{\circ}$ C to  $65^{\circ}$ C,  $C_{L} = 50 \text{ pF}$ 

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 3 ± 0.1	3.3 V 5 V	UNIT
	(INFOT)	(001701)	MIN	MAX	
	Α	V	1.2	3.2	
τ <sub>pd</sub>	CLK	Y	1.1	4	ns

# **OPERATING CHARACTERISTICS**

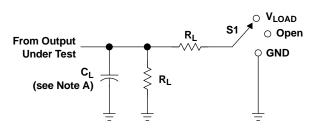
 $T_A = 25^{\circ}C$ 

	PARAMETER			CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	UNIT
				CHDITIONS	TYP	TYP	TYP	UNIT
_	Power dissipation capacitance	Outputs enabled	C - 0	f = 10 MHz	(1)	31	36	ρF
Cpo	rower dissipation capacitance	Outputs disabled	$C_L = 0,$	I = IU IVIMZ	(1)	7	11	pΓ

<sup>(1)</sup> This information was not available at the time of publication.



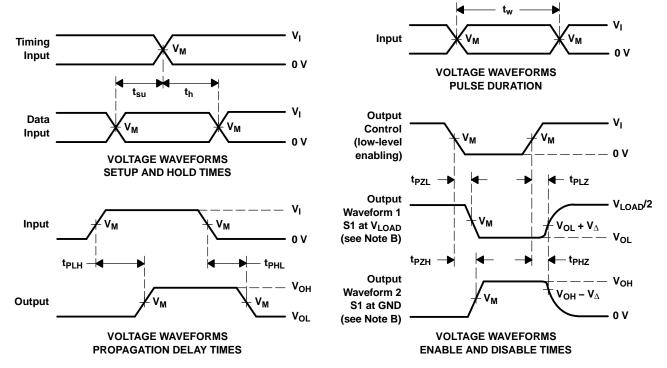
# PARAMETER MEASUREMENT INFORMATION



TEST	<b>S</b> 1
t <sub>pd</sub>	Open
t <sub>PLZ</sub> /t <sub>PZL</sub>	V <sub>LOAD</sub>
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND

**LOAD CIRCUIT** 

v	INPUT		V	v		6	v
V <sub>CC</sub>	VI	t <sub>r</sub> /t <sub>f</sub>	V <sub>M</sub>	V <sub>LOAD</sub>	CL	R <sub>L</sub>	$V_{\!\scriptscriptstyle \Delta}$
1.8 V	V <sub>CC</sub>	≤ <b>2</b> ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V $\pm$ 0.2 V	V <sub>CC</sub>	≤2 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3 V $\pm$ 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_{\Omega} = 50 \Omega$ .
- D. The outputs are measured one at a time, with one transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
- G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

### PACKAGE OPTION ADDENDUM

www.ti.com 11-Nov-2009

#### PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
74ALVC16334DGGRE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVC16334DGGRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVC16334DGVRE4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVC16334DGVRG4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVC16334DGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVC16334DGVR	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVC16334DL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVC16334DLG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

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**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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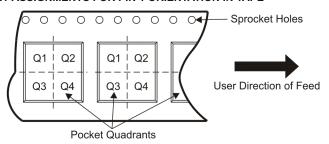
# TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALVC16334DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1
SN74ALVC16334DGVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1

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### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALVC16334DGGR	TSSOP	DGG	48	2000	346.0	346.0	41.0
SN74ALVC16334DGVR	TVSOP	DGV	48	2000	346.0	346.0	33.0

# DL (R-PDSO-G\*\*)

# **48 PINS SHOWN**

### PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MO-118

# DGG (R-PDSO-G\*\*)

# PLASTIC SMALL-OUTLINE PACKAGE

### **48 PINS SHOWN**



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

# DGV (R-PDSO-G\*\*)

# **24 PINS SHOWN**

# **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. Falls within JEDEC: 24/48 Pins – MO-153 14/16/20/56 Pins – MO-194

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