SCES357F - JULY 2001 - REVISED FEBRUARY 2010

8-BIT UNIVERSAL BUS TRANSCEIVER AND TWO 1-BIT BUS TRANSCEIVERS WITH SPLIT LVTTL PORT, FEEDBACK PATH, AND 3-STATE OUTPUTS

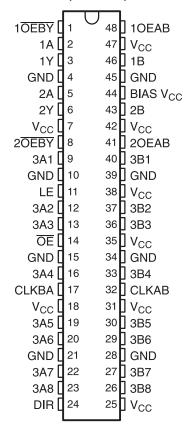
Check for Samples: SN74VMEH22501

FEATURES

- Member of the Texas Instruments Widebus™
 Family
- UBT[™] Transceiver Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Modes
- OEC[™] Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference (EMI)
- Compliant With VME64, 2eVME, and 2eSST Protocol
- Bus Transceiver Split LVTTL Port Provides a Feedback Path for Control and Diagnostics Monitoring
- I/O Interfaces Are 5-V Tolerant
- B-Port Outputs (–48 mA/64 mA)
- Y and A-Port Outputs (–12 mA/12 mA)
- I_{off}, Power-Up 3-State, and BIAS V_{CC} Support Live Insertion
- Bus Hold on 3A-Port Data Inputs
- 26-Ω Equivalent Series Resistor on 3A Ports and Y Outputs
- Flow-Through Architecture Facilitates Printed Circuit Board Layout
- Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DGG OR DGV PACKAGE (TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The SN74VMEH22501 8-bit universal bus transceiver has two integral 1-bit three-wire bus transceivers and is designed for 3.3-V V_{CC} operation with 5-V tolerant inputs. The UBT™ transceiver allows transparent, latched, and flip-flop modes of data transfer, and the separate LVTTL input and outputs on the bus transceivers provide a feedback path for control and diagnostics monitoring. This device provides a high-speed interface between cards operating at LVTTL logic levels and VME64, VME64x, or VME320⁽¹⁾ backplane topologies.

(1) VME320 is a patented backplane construction by Arizona Digital, Inc.



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DESCRIPTION/ORDERING INFORMATION (CONTINUED)

High-speed backplane operation is a direct result of the improved OECTM circuitry and high drive that has been designed and tested into the VME64x backplane model. The B-port I/Os are optimized for driving large capacitive loads and include pseudo-ETL input thresholds ($\frac{1}{2}$ V_{CC} ± 50 mV) for increased noise immunity. These specifications support the 2eVME protocols in VME64x (ANSI/VITA 1.1) and 2eSST protocols in VITA 1.5. With proper design of a 21-slot VME system, a designer can achieve 320-Mbyte transfer rates on linear backplanes and, possibly, 1-Gbyte transfer rates on the VME320 backplane.

All inputs and outputs are 5-V tolerant and are compatible with TTL and 5-V CMOS inputs.

Active bus-hold circuitry holds unused or undriven 3A-port inputs at a valid logic state. Bus-hold circuitry is not provided on 1A or 2A inputs, any B-port input, or any control input. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

This device is fully specified for live-insertion applications using I_{off} , power-up 3-state, and BIAS V_{CC} . The I_{off} circuitry prevents damaging current to backflow through the device when it is powered off/on. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict. The BIAS V_{CC} circuitry precharges and preconditions the B-port input/output connections, preventing disturbance of active data on the backplane during card insertion or removal, and permits true live-insertion capability.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, output-enable (\overline{OE} and \overline{OEBY}) inputs should be tied to V_{CC} through a pullup resistor and output-enable (\overline{OEAB}) inputs should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the drive capability of the device connected to this input.

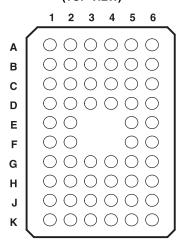
ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING		
	BGA MicroStar™ Junior – ZQL	Tape and reel	SN74VMEH22501ZQLR	VK501		
0°C to 85°C	TSSOP - DGG	Tape and reel	SN74VMEH22501DGGR	VMEH22501		
	TVSOP - DGV	Tape and reel	SN74VMEH22501DGVR	VK501		
	VFBGA – GQL	Tape and reel	SN74VMEH22501GQLR	VK501		

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/sc/packaging.



GQL OR ZQL PACKAGE (TOP VIEW)



TERMINAL ASSIGNMENTS(1)

	1	2	3	4	5	6
Α	1 OEBY	NC	NC	NC	NC	10EAB
В	1Y	1A	GND	GND	V _{CC}	1B
С	2Y	2A	V_{CC}	V _{CC}	BIAS V _{CC}	2B
D	3A1	2 OEBY	GND	GND	20EAB	3B1
E	3A2	LE			V _{CC}	3B2
F	3A3	ŌĒ			V_{CC}	3B3
G	3A4	CLKBA	GND	GND	CLKAB	3B4
Н	3A5	3A6	V_{CC}	V _{CC}	3B6	3B5
J	3A7	3A8	GND	GND	3B8	3B7
K	DIR	NC	NC	NC	NC	V_{CC}

(1) NC - No internal connection



FUNCTIONAL DESCRIPTION

The SN74VMEH22501 is a high-drive (–48/64 mA), 8-bit UBT transceiver containing D-type latches and D-type flip-flops for data-path operation in transparent, latched, or flip-flop modes. Data transmission is true logic. The device is uniquely partitioned as 8-bit UBT transceivers with two integrated 1-bit three-wire bus transceivers.

Functional Description for Two 1-Bit Bus Transceivers

The OEAB inputs control the activity of the 1B or 2B port. When OEAB is high, the B-port outputs are active. When OEAB is low, the B-port outputs are disabled.

Separate 1A and 2A inputs and 1Y and 2Y outputs provide a feedback path for control and diagnostics monitoring. The OEBY inputs control the 1Y or 2Y outputs. When OEBY is low, the Y outputs are active. When OEBY is high, the Y outputs are disabled.

The OEBY and OEAB inputs can be tied together to form a simple direction control where an input high yields A data to B bus and an input low yields B data to Y bus.

1-BIT BUS TRANSCEIVER FUNCTION TABLE

INP	UTS	OUTDUT	MODE			
OEAB	OEBY	OUTPUT	MODE			
L	Н	Z	Isolation			
Н	Н	A data to B bus	True driver			
L	L	B data to Y bus	True driver			
Н	L	A data to B bus, B data to Y bus	True driver with feedback path			

Functional Description for 8-Bit UBT Transceiver

The 3A and 3B data flow in each direction is controlled by the \overline{OE} and direction-control (DIR) inputs. When \overline{OE} is low, all 3A- or 3B-port outputs are active. When \overline{OE} is high, all 3A- or 3B-port outputs are in the high-impedance state.

FUNCTION TABLE

INP	UTS	OUTPUT		
OE	DIR	001701		
Н	Х	Z		
L	Н	3A data to 3B bus		
L	L	3B data to 3A bus		

The UBT transceiver functions are controlled by latch-enable (LE) and clock (CLKAB and CLKBA) inputs. For 3A-to-3B data flow, the UBT operates in the transparent mode when LE is high. When LE is low, the 3A data is latched if CLKAB is held at a high or low logic level. If LE is low, the 3A data is stored in the latch/flip-flop on the low-to-high transition of CLKAB.

The UBT transceiver data flow for 3B to 3A is similar to that of 3A to 3B, but uses CLKBA.



Table 1. UBT TRANSCEIVER FUNCTION TABLE(1)

	INPUTS			OUTPUT	MODE
ŌĒ	LE	CLKAB	3A	3B	MODE
Н	Χ	Χ	Χ	Z	Isolation
L	L	Н	Χ	B ₀ (2)	
L	L	L	X	B ₀ (3)	Latched storage of 3A data
L	Н	Χ	L	L	True transparent
L	Н	Χ	Н	Н	True transparent
L	L	1	L	L	Clasked storage of 2A data
L	L	↑	Н	Н	Clocked storage of 3A data

- (1) 3A-to-3B data flow is shown; 3B-to-3A data flow is similar, but uses CLKBA.
- (2) Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LE went low
- 3) Output level before the indicated steady-state input conditions were established

The UBT transceiver can replace any of the functions shown in Table 2.

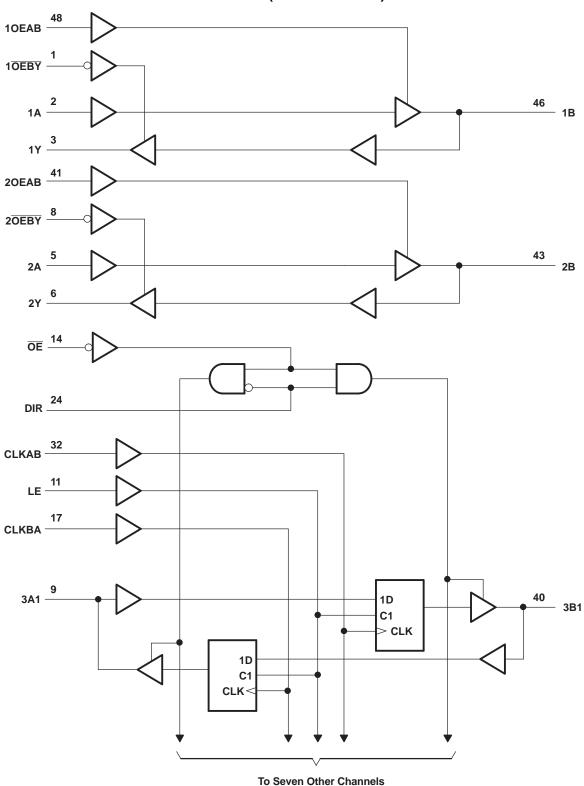
Table 2. SN74VMEH22501 UBT Transceiver Replacement Functions

•	
FUNCTION	8 BIT
Transceiver	'245, '623, '645
Buffer/driver	'241, '244, '541
Latched transceiver	'543
Latch	'373, '573
Registered transceiver	'646, '652
Flip-flop	'374, '574
SN74VMEH22501 UBT transceiver	replaces all above functions

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LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers shown are for the DGG and DGV packages.

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC} , BIAS V_{CC}	Supply voltage range		-0.5	4.6	V
V_{I}	Input voltage range ⁽²⁾		-0.5	7	V
Vo	Voltage range applied to any output in the high-impedar	nce or power-off state (2)	-0.5	7	V
V _o	Voltage range applied to any output in the high or low	3A port or Y output	-0.5	V _{CC} + 0.5	V
V _O	state ⁽²⁾	B port	-0.5 4.6 -0.5 7 -0.5 7	V	
1	Output augment in the law state	3A port or Y output		50	A
I _O	Output current in the low state	B port	50 100 –50	100	mA
		3A port or Y output		-50	
I _O	Output current in the high state	B port		4.6 7 7 7 V _{CC} + 0.5 4.6 50 100 -50 -100 -50 -50 70 58 42	mA
I _{IK}	Input clamp current	V _I < 0		-50	mA
I _{OK}	Output clamp current	$V_O < 0$ or $V_O > V_{CC}$, B port		-50	mA
		DGG package		70	
ок	Package thermal impedance (3)	DGV package		58	°C/W
		GQL/ZQL package		55 7 55 V _{CC} + 0.5 5 4.6 50 100 -50 -100 -50 -50 -50 -50 58 42	
T _{stg}	Storage temperature range		-65	150	°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

Recommended Operating Conditions (1) (2)

			MIN	NOM	MAX	UNIT
V_{CC} , BIAS V_{CC}	Supply voltage		3.15	3.3	3.45	V
V_{I}	Input voltage	Control inputs or A port		V_{CC}	5.5	V
νĮ	input voitage	B port		V_{CC}	5.5	V
V	High level input voltage	Control inputs or A port	2			V
V _{IH}	High-level input voltage	B port	0.5 V _{CC} + 50 mV			V
V_{IL}	Lave laval in a strategy	Control inputs or A port		0.8		V
	Low-level input voltage	B port			0.5 V _{CC} – 50 mV	V
I _{IK}	Input clamp current				-18	mA
	IP-de level endered encourt	3A port and Y output			-12	mA
Іон	High-level output current	B port		-48		
	Landard and and an extended	3A port and Y output			12	1
l _{OL}	Low-level output current	B port		64	mA	
Δt/Δν	Input transition rise or fall rate	Outputs enabled			10	ns/V
Δt/ΔV _{CC}	Power-up ramp rate	-	20			μs/V
T _A	Operating free-air temperature		0		85	°C

⁽¹⁾ All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

³⁾ The package thermal impedance is calculated in accordance with JESD 51-7.

⁽²⁾ Proper connection sequence for use of the B-port I/O precharge feature is GND and BIAS V_{CC} = 3.3 V first, I/O second, and V_{CC} = 3.3 V last, because the BIAS V_{CC} precharge circuitry is disabled when any V_{CC} pin is connected. The control inputs can be connected at any time, but normally are connected during the I/O stage. If B-port precharge is not required, any connection sequence is acceptable, but generally, GND is connected first.



Electrical Characteristics

over recommended operating free-air temperature range for A and B ports (unless otherwise noted)

	PARAMETER	TEST CONDI	ITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT	
V_{IK}		V _{CC} = 3.15 V,	$I_I = -18 \text{ mA}$			-1.2	V	
	3A port, any B ports, and Y outputs	$V_{CC} = 3.15 \text{ V to } 3.45 \text{ V},$	I _{OH} = -100 μA	V _{CC} - 0.2				
$V_{OH} = \begin{array}{c} V_{IK} & V_{CC} = 3.15 \ V, & I_{I} = -18 \ mA \\ \hline V_{OH} & 3A \ port, any \ B \ ports, and \ Y \ outputs & V_{CC} = 3.15 \ V \ to \ 3.45 \ V, & I_{OH} = -100 \ \mu A \\ \hline V_{OH} & 3A \ port \ and \ Y \ outputs & V_{CC} = 3.15 \ V & I_{OH} = -6 \ mA \\ \hline I_{OH} = -12 \ mA \\ \hline I_{OH} = -12 \ mA \\ \hline I_{OH} = -24 \ mA \\ \hline I_{OH} = -24 \ mA \\ \hline I_{OH} = -48 \ mA \\ \hline I_{OH} = -12 \ mA \\ \hline I_{OH} = -48 \ mA \\ \hline I_{OH} = -48 \ mA \\ \hline I_{OL} = 100 \ \mu A \\ \hline V_{CC} = 3.15 \ V & I_{OL} = 100 \ \mu A \\ \hline I_{OL} = 12 \ mA \\ \hline $	$I_{OH} = -6 \text{ mA}$	2.4			.,			
V _{OH}	on port and 1 outputs	VCC = 3.13 V	$I_{OH} = -12 \text{ mA}$	2	-1.2 2 4 2 4 2 0.2 0.55 0.8 0.4 0.55 0.6 ±1 5 -5 -20 ±10 5 5 0 0 ±10 30 30 30 76 19	V		
	Any B port	V 3 15 V	$I_{OH} = -24 \text{ mA}$	2.4				
	Any B port	VCC = 3.13 V	$I_{OH} = -48 \text{ mA}$	2	- 0.2 2.4 2 2.4 2 0.2 0.55 0.8 0.4 0.55 0.6 ±1 5 -5 -20 ±10 75 -75 500 -500 ±10 30 30 30 30			
		$V_{CC} = 3.15 \text{ V to } 3.45 \text{ V},$	I _{OL} = 100 μA			0.2		
	3A port and V outputs	V 3 15 V	I _{OL} = 6 mA			0.55		
Any B port Control inputs, 1A and 2A lozh (2) 3A port, any B pand Y outputs 3A port and Y o	3A port and 1 outputs	VCC = 3.13 V	I _{OL} = 12 mA			8.0	V	
	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$							
	Any B port	V _{CC} = 3.15 V	$I_{OL} = 48 \text{ mA}$	-1.2 V _{CC} - 0.2 2.4 2 2.4 2 0.2 0.55 0.8 0.4 0.55 0.6 ±1 5 -5 -20 ±10 75 -75 500 -500 ±10 4 30 30 76 19				
			I _{OL} = 64 mA		-1.2 0.2 0.55 0.8 0.4 0.55 0.6 ±1 5 -5 -20 ±10 ±10 30 30 30 76 19			
	Control inputs,	$V_{CC} = 3.45 \text{ V},$	$V_I = V_{CC}$ or GND		±1 5			
ΙΙ	1A and 2A	$V_{CC} = 0 \text{ or } 3.45 \text{ V},$	$V_1 = 5.5 \text{ V}$			5	μΑ	
I _{OZH} (2)		V _{CC} = 3.45 V,	$V_O = V_{CC}$ or 5.5 V			5	μΑ	
. (2)	3A port and Y outputs	V 2.45 V	V CND			– 5		
OZL (=)	Any B port	$V_{CC} = 3.45 \text{ V},$	$v_0 = GND$			-20	μΑ	
		$V_{CC} = 0$, BIAS $V_{CC} = 0$,	V_{I} or $V_{O} = 0$ to 5.5 V			±10	μΑ	
I _{BHL} (3)	3A port	V _{CC} = 3.15 V,	$V_1 = 0.8 \text{ V}$	75			μΑ	
I _{BHH} (4)	3A port	V _{CC} = 3.15 V,	$V_I = 2 V$	-75			μΑ	
	3A port	V _{CC} = 3.45 V,	$V_I = 0$ to V_{CC}	500			μΑ	
I _{BHHO} (6)	3A port	V _{CC} = 3.45 V,	$V_I = 0$ to V_{CC}	-500			μΑ	
I _{OZ(PU/PD)}	(7)	$V_{CC} \le 1.5 \text{ V}, V_O = 0.5 \text{ V to } V_{CC}, V_I = \text{GND or } V_{CC}, \overline{\text{OE}} = \text{don't care}$				±10	μΑ	
			Outputs high			30		
I_{CC}			Outputs low			30	mA	
		AL = ACC OL GIAD	Outputs disabled			30		
		$V_{CC} = 3.45 \text{ V}, I_{O} = 0,$	Outputs enabled		76		μ A /	
I _{CCD}	Any B port $V_{CC} = 3.15 \text{ V}$ Any B port $V_{CC} = 3.15 \text{ V}$ 3A port, any B ports, and Y outputs $V_{CC} = 3.15 \text{ V}$ 3A port and Y outputs $V_{CC} = 3.15 \text{ V}$ Any B port $V_{CC} = 3.15 \text{ V}$ Control inputs, 1A and 2A $V_{CC} = 3.45 \text{ V}$ Cat (2) 3A port, any B port, and Y outputs $V_{CC} = 3.45 \text{ V}$, $V_{CC} = 0 \text{ or } 3.45 \text{ V}$, $V_{CC} = 3.$	Outputs disabled		19		clock MHz/ input		
ΔI _{CC} ⁽⁸⁾		V_{CC} = 3.15 V to 3.45 V, One input a Other inputs at V_{CC} or GND	at V _{CC} – 0.6 V,			750	μА	

- (1) All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.
- 2) For I/O ports, the parameters I_{OZH} and I_{OZL} include the input leakage current.
- (3) The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND, then raising it to V_{IL} max.
- (4) The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC}, then lowering it to V_{IH} min.
- (5) An external driver must source at least I_{BHLO} to switch this node from low to high.
- 6) An external driver must sink at least I_{BHHO} to switch this node from high to low.
- (7) High-impedance state during power up or power down
- (8) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

Electrical Characteristics (continued)

over recommended operating free-air temperature range for A and B ports (unless otherwise noted)

	PARAMETER	TE	ST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
C	1A and 2A inputs	(– 2.15 \ / or 0			2.8		n.E
C _i	Control inputs	$V_1 = 3.15 \text{ V or } 0$		2.6		pF	
Co	1Y or 2Y outputs	V _O = 3.15 V or 0			5.6		pF
0	3A port	V 22V	V 22V = 0		7.9		
C _{io}	Any B port	$V_{CC} = 3.3 \text{ V},$	$V_0 = 3.3 \text{ V or } 0$		11	12.5	pF

Live-Insertion Specifications

over recommended operating free-air temperature range for B port

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
I _{CC} (BIAS V _{CC})	$V_{CC} = 0 \text{ to } 3.15 \text{ V},$	BIAS $V_{CC} = 3.15 \text{ V to } 3.45 \text{ V},$	$I_{O(DC)} = 0$			5	mA
ICC (DIA2 VCC)	$V_{CC} = 3.15 \text{ V to } 3.45 \text{ V}^{(2)},$	BIAS $V_{CC} = 3.15 \text{ V to } 3.45 \text{ V},$	$I_{O(DC)} = 0$			5 10 5 1.7 –100	μΑ
Vo	$V_{CC} = 0$,	BIAS $V_{CC} = 3.15 \text{ V to } 3.45 \text{ V}$		1.3	1.5	1.7	V
	V 0	$V_O = 0$,	BIAS V _{CC} = 3.15 V	-20		-100	^
IO	$V_{CC} = 0$	V _O = 3 V,	BIAS V _{CC} = 3.15 V	20		100	μΑ

⁽¹⁾ All typical values are at V_{CC} = 3.3 V, T_A = 25°C. (2) V_{CC} – 0.5 V < BIAS V_{CC}

Timing Requirements for UBT Transceiver

over recommended operating conditions (unless otherwise noted) (see Figure 1 and Figure 2)

	·			MIN	MAX	UNIT
f _{clock}	Clock frequency				120	MHz
	Pulco duration	LE high		2.5		ns
t _w	ruise duration	CLK high or low		3		115
	Research Clock frequency Pulse duration Setup time Hold time	3A before CLK↑	Data high	2.1		
		SA before CEN	Data low	2.2		
	Pulse duration Setup time	3A before LE↓	CLK high	2		
		SA before LE	CLK low	2		20
t _{su}	Setup time	3B before CLK↑	Data high	2.5 3 2.1 2.2 2	ns	
		36 before CLK	Data low	2.7		
		2D hefere LEI	CLK high	2		
		3B before LE↓	CLK low	2	2.5 3 2.1 2.2 2 2 2.5 2 2 2.5 2 0 0 0 1 1 0 0 1	
	Pulse duration Setup time	3A after CLK↑	Data high	0		
		SA allei CEN	Data low	0		
		24 ofter 5	CLK high	1		
	Hald time	3A after LE↓	CLK low	120 2.5 3 3 3 3 3 3 3 3 3		
t _h	Hold time	2D affair CLIVA	Data high		ns	
		3B after CLK↑	Data low	0		
		2D offer LE	CLK high	1		
		3B after LE↓	CLK low	2.5 3 2.1 2.2 2 2 2.5 2.7 2 2 0 0 1 1 0 0 1		

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Switching Characteristics for Bus Transceiver Function

over recommended operating conditions (unless otherwise noted) (see Figure 1 and Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
t _{PLH}	1A or 2A	1B or 2B	5.1		8.9	ns
t _{PHL}	TA OF ZA	ID UI ZD	4.5		7.8	115
t _{PLH}	10 or 20	1Y or 2Y	7.2		14.5	no
t _{PHL}	1A or 2A	11 01 21	6.1		13	ns
t _{PZH}	OEAB	1B or 2B	4.6		8.1 7.4	ne
t _{PZL}	OLAB	16 01 26	3.7			115
t _{PHZ}	OEAB	1B or 2B	3.3		9.7	no
t _{PLZ}	OEAB	ID 01 2D	1.8		4.8	ns
t _r	Transition time, E	3 port (10%–90%)		4.3		ns
t _f	Transition time, E	3 port (90%–10%)		4.3		ns
t _{PLH}	1B or 2B	1Y or 2Y	1.6		5.6	ns
t _{PHL}	18 01 28	11 01 21	1.6		5.6	115
t _{PZH}	 OEBY	1Y or 2Y	1.2		5.6	no
t _{PZL}	OEDT	11 01 21	1.8		4.9	ns
t _{PHZ}	 OEBY	1Y or 2Y	1.4		5.4	ne
t _{PLZ}	OLBT	11 01 21	1.7		4.5	ns

Switching Characteristics for UBT Transceiver

over recommended operating conditions (unless otherwise noted) (see Figure 1 and Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
f _{max}			120			MHz
t _{PLH}	24	an.	5.5		9.3	
t _{PHL}	3A	3B	4.7		8.3	ns
t _{PLH}	LE	3B	6		10.6	20
t _{PHL}	LE	3D	4.9		8.7	ns
t _{PLH}	CLKAB	3B	5.8		10.1	20
t _{PHL}	CLNAB	3D	4.6		8.4	ns
t _{PZH}	ŌĒ	2D	4.6		9.3	20
t _{PZL}	OE .	3B	3.5		8.5	ns
t _{PHZ}	ŌĒ	3B	4.8		9.3	20
t _{PLZ}	GE.	36	2.4		5.7	ns
t _r	Transition time, E	3 port (10%–90%)		4.3		ns
t _f	Transition time, E	3 port (90%–10%)		4.3		ns
t _{PLH}	3B	0.4	1.7		5.9	20
t _{PHL}	35	3A	1.7		5.9	ns
t _{PLH}	LE	3A	1.7		5.9	20
t _{PHL}	LL	JA.	1.7		5.9	ns
t _{PLH}	CLKBA	3A	1.4		5.5	20
t _{PHL}	CLNDA	3A	1.4		5.5	ns
t _{PZH}	ŌĒ	3A	1.5		6.2	ns
t _{PZL}	GL .	JA.	2.1		5.5	115
t _{PHZ}	ŌĒ	3A	1.8		6.2	ne
t _{PLZ}	OE .	SA SA	2.3		5.6	ns



Skew Characteristics for Bus Transceiver

for specific worst-case V_{CC} and temperature within the recommended ranges of supply voltage and operating free-air temperature (see Figure 1 and Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN MAX	UNIT
t _{sk(LH)}	14 07 24	1B or 2B	0.8	20
t _{sk(HL)}	1A or 2A	IB OI 2B	0.7	ns
t _{sk(LH)}	t _{sk(LH)} 1B or 2B 1Y or 2Y	1Y or 2Y	0.7	20
t _{sk(HL)}	16 01 26	11 01 21	0.6	ns
. (1)	1A or 2A	1B or 2B	1.7	
$t_{sk(t)}$ ⁽¹⁾	1B or 2B	1Y or 2Y	1.2	ns
	1A or 2A	1B or 2B	2.8	
t _{sk(pp)}	1B or 2B	1Y or 2Y	1.4	ns

⁽¹⁾ t_{sk(t)} – Output-to-output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs of the same packaged device. The specifications are given for specific worst-case V_{CC} and temperature and apply to any outputs switching in opposite directions, both low to high (LH) and high to low (HL) [t_{sk(t)}].

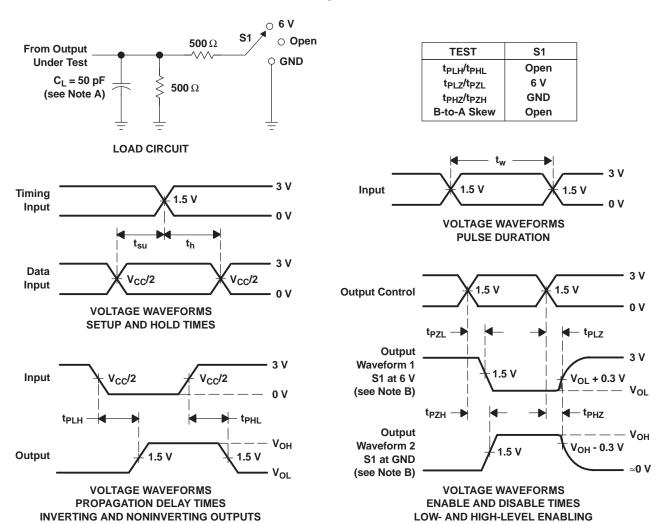
Skew Characteristics for UBT

for specific worst-case V_{CC} and temperature within the recommended ranges of supply voltage and operating free-air temperature (see Figure 1 and Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN MAX	UNIT
t _{sk(LH)}	3A	3B	1.3	ns
t _{sk(HL)}	SA	36	1.1	110
t _{sk(LH)}	CLKAB	3B	0.8	ns
t _{sk(HL)}		36	0.8	115
t _{sk(LH)}	3P	3A	0.7	ne
t _{sk(HL)}	3B	3A	0.6	ns
t _{sk(LH)}	CLKBA	3A	0.7	no
t _{sk(HL)}	CLNDA	SA .	0.6	ns
	3A	3B	1.9	
t _{sk(t)} (1)	CLKAB	3B	2.1	20
^L sk(t) ` ′	3B	3A	1.2	ns
	CLKBA	3A	1	
	3A	3B	2.8	
	CLKAB	3B	2.7	no
t _{sk(pp)}	3B	3A	1.3	ns
	CLKBA	3A	1.2	

⁽¹⁾ t_{sk(t)} – Output-to-output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs of the same packaged device. The specifications are given for specific worst-case V_{CC} and temperature and apply to any outputs switching in opposite directions, both low to high (LH) and high to low (HL) [t_{sk(t)}].

PARAMETER MEASUREMENT INFORMATION A PORT



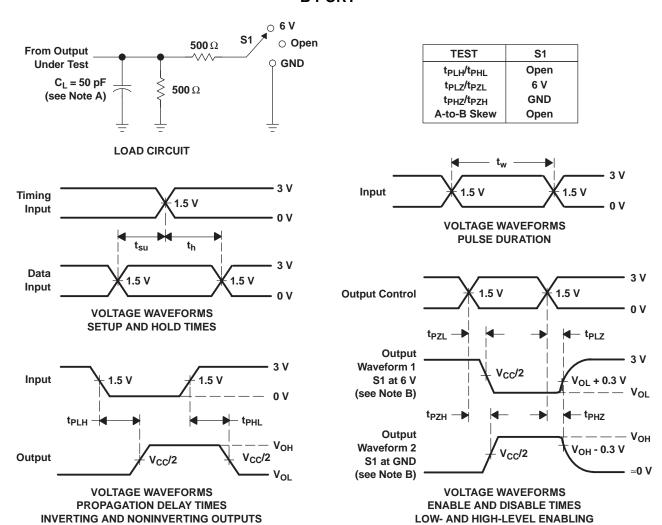
NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \approx 10 MHz, $Z_O = 50~\Omega$, $t_r \approx 2~ns$, $t_f \approx 2~ns$.
- D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION B PORT



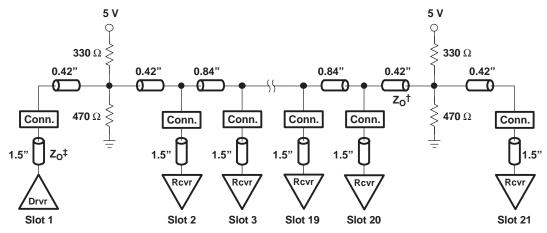
NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \approx 10 MHz, $Z_O = 50~\Omega$, $t_r \approx 2~ns$, $t_f \approx 2~ns$.
- D. The outputs are measured one at a time, with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

Distributed-Load Backplane Switching Characteristics

The preceding switching characteristics tables show the switching characteristics of the device into the lumped load shown in the parameter measurement information (PMI) (see Figure 1 and Figure 2). All logic devices currently are tested into this type of load. However, the designer's backplane application probably is a distributed load. For this reason, this device has been designed for optimum performance in the VME64x backplane as shown in Figure 3.



[†] Unloaded backplane trace natural impedence (Z_0) is 45 Ω . 45 Ω to 60 Ω is allowed, with 50 Ω being ideal.

Figure 3. VME64x Backplane

The following switching characteristics tables derived from TI-SPICE models show the switching characteristics of the device into the backplane under full and minimum loading conditions, to help the designer better understand the performance of the VME device in this typical backplane. See www.ti.com/sc/etl for more information.

Driver in Slot 11, With Receiver Cards in All Other Slots (Full Load)

Switching Characteristics for Bus Transceiver Function

over recommended operating conditions (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP ⁽¹⁾	MAX	UNIT
t _{PLH}	1A or 2A	1B or 2B	5.9		8.5	20
t _{PHL}	1A or 2A	1B 01 2B	5.5		8.7	ns
t _r ⁽²⁾	Transition time, B port (10%–90%)		9	8.6	11.4	ns
t _f (2)	Transition time, E	3 port (90%–10%)	8.9	9	10.8	ns

⁽¹⁾ All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$. All values are derived from TI-SPICE models.

(2) All t_r and t_f times are taken at the first receiver.

[‡] Card stub natural impedence (Z_O) is 60 Ω .



Switching Characteristics for UBT

over recommended operating conditions (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP ⁽¹⁾	MAX	UNIT
t _{PLH}	3A	3B	6.2		8.9	20
t _{PHL}	SA SA	36	5.6		9	ns
t _{PLH}	LE	3В	6.1		9.1	20
t _{PHL}	LE		5.6		9	ns
t _{PLH}	CLKAB	3B	6.2		9.1	20
t _{PHL}	CLNAB	36	5.7		9	ns
t _r (2)	Transition time, B port (10%–90%)		9	8.6	11.4	ns
t _f (2)	Transition time, E	3 port (90%–10%)	8.9	9	10.8	ns

All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.

Skew Characteristics for Bus Transceiver

for specific worst-case V_{CC} and temperature within the recommended ranges of supply voltage and operating free-air temperature (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN TYP(1) MAX	UNIT
t _{sk(LH)}	1A or 2A	1B or 2B	2.5	
t _{sk(HL)}	TA OF ZA	16 01 26	3	ns
t _{sk(t)} (2)	1A or 2A	1B or 2B	1	ns
t _{sk(pp)}	1A or 2A	1B or 2B	0.5 3.4	ns

Skew Characteristics for UBT

for specific worst-case V_{CC} and temperature within the recommended ranges of supply voltage and operating free-air temperature (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN TYP(1) MAX	UNIT
t _{sk(LH)}	3A	3B	2.4	20
t _{sk(HL)}	SA	ЭБ	3.4	ns
t _{sk(LH)}	CLKAB	3B	2.7	ne
t _{sk(HL)}	CERAB	36	3.4	ns
t _{sk(t)} (2)	3A	3B	1	20
^L sk(t)	CLKAB	3B	1	ns
4	3A	3B	0.5 3.4	20
t _{sk(pp)}	CLKAB	3B	0.6 3.5	ns

All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.

Driver in Slot 1, With One Receiver in Slot 21 (Minimum Load)

Switching Characteristics for Bus Transceiver Function

over recommended operating conditions (unless otherwise noted) (see Figure 3)

All t_r and t_f times are taken at the first receiver.

All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$. All values are derived from TI-SPICE models. $t_{sk(t)}$ – Output-to-output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs of the same packaged device. The specifications are given for specific worst-case V_{CC} and temperature and apply to any outputs switching in opposite directions, both low to high (LH) and high to low (HL) [t_{sk(t)}].

 $t_{sk(t)}$ – Output-to-output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs of the same packaged device. The specifications are given for specific worst-case V_{CC} and temperature and apply to any outputs switching in opposite directions, both low to high (LH) and high to low (HL) [t_{sk(t)}].

Switching Characteristics for Bus Transceiver Function (continued)

over recommended operating conditions (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP ⁽¹⁾	MAX	UNIT
t _{PLH}	1A or 2A	1B or 2B	5.5		7.4	
t _{PHL}	IA OI ZA	IB OI 2B	5.3		7.4	ns
t _r ⁽²⁾	Transition time, E	Transition time, B port (10%–90%)		3.4	4.4	ns
t _f ⁽²⁾	Transition time, E	3 port (90%–10%)	3.7	3.4	4.8	ns

- All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$. All values are derived from TI-SPICE models.
- All t_r and t_f times are taken at the first receiver.

Switching Characteristics for UBT

over recommended operating conditions (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP ⁽¹⁾	MAX	UNIT
t _{PLH}	3A	3B	5.8		7.9	20
t _{PHL}	3A	35	5.5		7.7	ns
t _{PLH}	LE	3B	5.9		8	no
t _{PHL}	LE 	36	5.5		7.8	ns
t _{PLH}	CLKAR	0.0	5.9		8.1	20
t _{PHL}	CLKAB	3B	5.5		7.7	ns
t _r ⁽²⁾	Transition time, B port (10%–90%)		3.9	3.4	4.4	ns
t _f (2)	Transition time, E	3 port (90%–10%)	3.7	3.4	4.8	ns

- (1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.
- All t_r and t_f times are taken at the first receiver.

Skew Characteristics for Bus Transceiver

for specific worst-case V_{CC} and temperature within the recommended ranges of supply voltage and operating free-air temperature (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN TYP ⁽¹⁾ MAX	UNIT
t _{sk(LH)}	1A or 2A	1B or 2B	1.7	no
t _{sk(HL)}	1A 01 2A	1B 01 2B	2.1	ns
$t_{sk(t)}$ (2)	1A or 2A	1B or 2B	1	ns
t _{sk(pp)}	1A or 2A	1B or 2B	0.2 2.1	ns

All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$. All values are derived from TI-SPICE models. $t_{sk(t)}$ – Output-to-output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs of the same packaged device. The specifications are given for specific worst-case V_{CC} and temperature and apply to any outputs switching in opposite directions, both low to high (LH) and high to low (HL) [$t_{sk(t)}$].



Skew Characteristics for UBT

for specific worst-case V_{CC} and temperature within the recommended ranges of supply voltage and operating free-air temperature (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN TYP ⁽¹⁾ MAX	UNIT
t _{sk(LH)}	3A	3B	2	
t _{sk(HL)}	3A	36	2.3	ns
t _{sk(LH)}	sk(LH)	3B	2.1	
t _{sk(HL)}	CLKAB	36	2.4	ns
4 (2)	3A	3B	1	20
t _{sk(t)} (2)	CLKAB	3B	1	ns
t _{sk(pp)}	3A	3B	0.2 2.5	
	CLKAB	3B	0.2 2.9	ns

- (1) All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$. All values are derived from TI-SPICE models.
- (2) t_{sk(t)} Output-to-output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs of the same packaged device. The specifications are given for specific worst-case V_{CC} and temperature and apply to any outputs switching in opposite directions, both low to high (LH) and high to low (HL) [t_{sk(t)}].

By simulating the performance of the device using the VME64x backplane (see Figure 3), the maximum peak current in or out of the B-port output, as the devices switch from one logic state to another, was found to be equivalent to driving the lumped load shown in Figure 4.

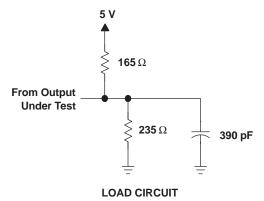


Figure 4. Equivalent AC Peak Output-Current Lumped Load

In general, the rise- and fall-time distribution is shown in Figure 5. Since VME devices were designed for use into distributed loads like the VME64x backplane (B/P), there are significant differences between low-to-high (LH) and high-to-low (HL) values in the lumped load shown in the PMI (see Figure 1 and Figure 2).



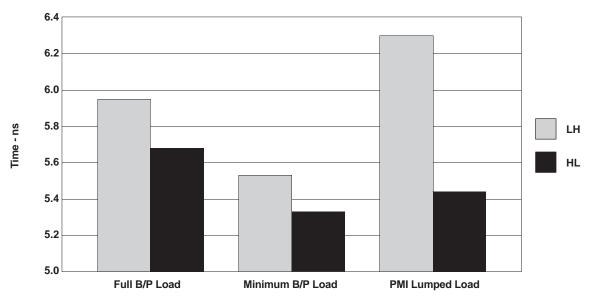
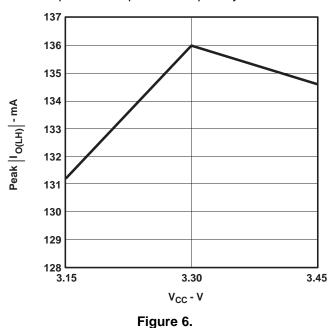


Figure 5.

Characterization-laboratory data in Figure 6 and Figure 7 show the absolute ac peak output current, with different supply voltages, as the devices change output logic state. A typical nominal process is shown to demonstrate the devices' peak ac output drive capability.



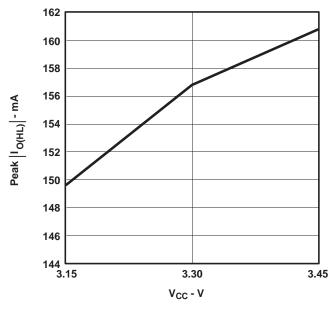
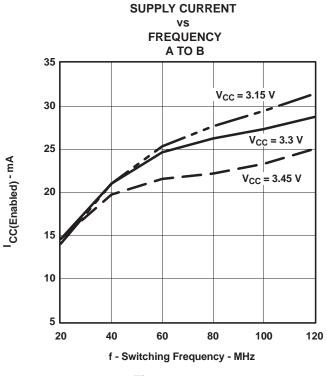
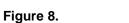


Figure 7.



TYPICAL CHARACTERISTICS





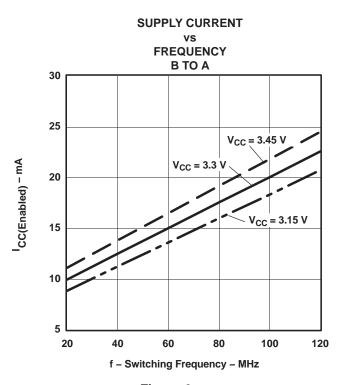


Figure 9.



TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE **HIGH-LEVEL OUTPUT CURRENT** 300 $V_{CC} = 3.15 \text{ V}$ 250 V_{OH} - High-Level Output Voltage - V $V_{CC} = 3.3 V$ 200 $V_{CC} = 3.45 \text{ V}$ 150 100 50 10 0 20 40 50 60 70 80 90 100

Figure 10. V_{OL} vs I_{OL}

I_{OH} - High-Level Output Current - mA

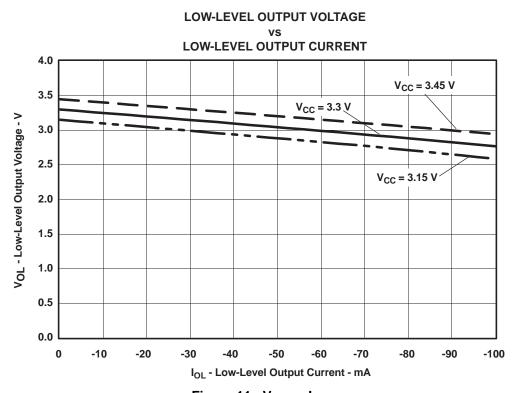


Figure 11. V_{OH} vs I_{OH}



VMEbus Summary

In 1981, the VMEbus was introduced as a backplane bus architecture for industrial and commercial applications. The data-transfer protocols used to define the VMEbus came from the Motorola™ VERSA bus architecture that owed its heritage to the then recently introduced Motorola 68000 microprocessor. The VMEbus, when introduced, defined two basic data-transfer operations: single-cycle transfers consisting of an address and a data transfer, and a block transfer (BLT) consisting of an address and a sequence of data transfers. These transfers were asynchronous, using a master-slave handshake. The master puts address and data on the bus and waits for an acknowledgment. The selected slave either reads or writes data to or from the bus, then provides a data-acknowledge (DTACK*) signal. The VMEbus system data throughput was 40 Mbyte/s. Previous to the VMEbus, it was not uncommon for the backplane buses to require elaborate calculations to determine loading and drive current for interface design. This approach made designs difficult and caused compatibility problems among manufacturers. To make interface design easier and to ensure compatibility, the developers of the VMEbus architecture defined specific delays based on a 21-slot terminated backplane and mandated the use of certain high-current TTL drivers, receivers, and transceivers.

In 1989, multiplexing block transfer (MBLT) effectively increased the number of bits from 32 to 64, thereby doubling the transfer rate. In 1995, the number of handshake edges was reduced from four to two in the double-edge transfer (2eVME) protocol, doubling the data rate again. In 1997, the VMEbus International Trade Association (VITA) established a task group to specify a synchronous protocol to increase data-transfer rates to 320 Mbyte/s, or more. The unreleased specification, VITA 1.5 [double-edge source synchronous transfer (2eSST)], is based on the asynchronous 2eVME protocol. It does not wait for acknowledgement of the data by the receiver and requires incident-wave switching. Sustained data rates of 1 Gbyte/s, more than ten times faster than traditional VME64 backplanes, are possible by taking advantage of 2eSST and the 21-slot VME320 star-configuration backplane. The VME320 backplane approximates a lumped load, allowing substantially higher-frequency operation over the VME64x distributed-load backplane. Traditional VME64 backplanes with no changes theoretically can sustain 320 Mbyte/s.

From BLT to 2eSST – A Look at the Evolution of VMEbus Protocols by John Rynearson, Technical Director, VITA, provides additional information on VMEbus and can be obtained at www.vita.com.

Maximum Data Transfer Rates

DATE	TOPOLOGY	PROTOCOL	DATA BITS PER CYCLE	DATA TRANSFERS	PER SYSTEM	FREQUENCY (MHz)			
				PER CLOCK CYCLE	(Mbyte/s)	BACKPLANE	CLOCK		
1981	VMEbus IEEE-1014	BLT	32	1	40	10	10		
1989	VME64	MBLT	64	1	80	10	10		
1995	VME64x	2eVME	64	2	160	10	20		
1997	VME64x	2eSST	64	2-No Ack	160–320	10–20	20–40		
1999	VME320	2eSST	64	2-No Ack	320-1000	20-62.5	40-125		

Applicability

Target applications for VME backplanes include industrial controls, telecommunications, simulation, high-energy physics, office automation, and instrumentation systems.





4-May-2012

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
74VMEH22501DGGRE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74VMEH22501DGGRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74VMEH22501DGVRE4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74VMEH22501DGVRG4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74VMEH22501DGG	ACTIVE	TSSOP	DGG	48	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74VMEH22501DGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74VMEH22501DGVR	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74VMEH22501GQLR	LIFEBUY	BGA MICROSTAR JUNIOR	GQL	56	1000	TBD	SNPB	Level-1-240C-UNLIM	
SN74VMEH22501ZQLR	ACTIVE	BGA MICROSTAR JUNIOR	ZQL	56	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.



PACKAGE OPTION ADDENDUM

4-May-2012

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

All differisions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74VMEH22501DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1
SN74VMEH22501DGVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1
SN74VMEH22501GQLR	BGA MI CROSTA R JUNI OR	GQL	56	1000	330.0	16.4	4.8	7.3	1.45	8.0	16.0	Q1
SN74VMEH22501ZQLR	BGA MI CROSTA R JUNI OR	ZQL	56	1000	330.0	16.4	4.8	7.3	1.45	8.0	16.0	Q1

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*All dimensions are nominal

All differsions are nominal								
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
SN74VMEH22501DGGR	TSSOP	DGG	48	2000	346.0	346.0	41.0	
SN74VMEH22501DGVR	TVSOP	DGV	48	2000	346.0	346.0	33.0	
SN74VMEH22501GQLR	BGA MICROSTAR JUNIOR	GQL	56	1000	333.2	345.9	28.6	
SN74VMEH22501ZQLR	BGA MICROSTAR JUNIOR	ZQL	56	1000	333.2	345.9	28.6	

ZQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-285 variation BA-2.
- D. This package is Pb-free. Refer to the 56 GQL package (drawing 4200583) for tin-lead (SnPb).

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DGV (R-PDSO-G**)

24 PINS SHOWN

PLASTIC SMALL-OUTLINE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. Falls within JEDEC: 24/48 Pins – MO-153 14/16/20/56 Pins – MO-194

GQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-285 variation BA-2.
- D. This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.



DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

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