

FEATURES

- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- DOC™ (Dynamic Output Control) Circuit Dynamically Changes Output Impedance, Resulting in Noise Reduction Without Speed Degradation
- Dynamic Drive Capability Is Equivalent to Standard Outputs With I_{OH} and I_{OL} of ± 24 mA at 2.5-V V_{CC}
- Overvoltage-Tolerant Inputs/Outputs Allow Mixed-Voltage-Mode Data Communications
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- Package Options Include Plastic Thin Shrink Small-Outline (DGG) and Thin Very Small-Outline (DGV) Packages

DESCRIPTION

A Dynamic Output Control (DOC™) circuit is implemented, which, during the transition, initially lowers the output impedance to effectively drive the load and, subsequently, raises the impedance to reduce noise. Figure 1 shows typical V_{OL} vs I_{OL} and V_{OH} vs I_{OH} curves to illustrate the output impedance and drive capability of the circuit. At the beginning of the signal transition, the DOC circuit provides a maximum dynamic drive that is equivalent to a high-drive standard-output device. For more information, refer to the TI application reports, *AVC Logic Family Technology and Applications*, literature number SCEA006, and *Dynamic Output Control (DOC™) Circuitry Technology and Applications*, literature number SCEA009.

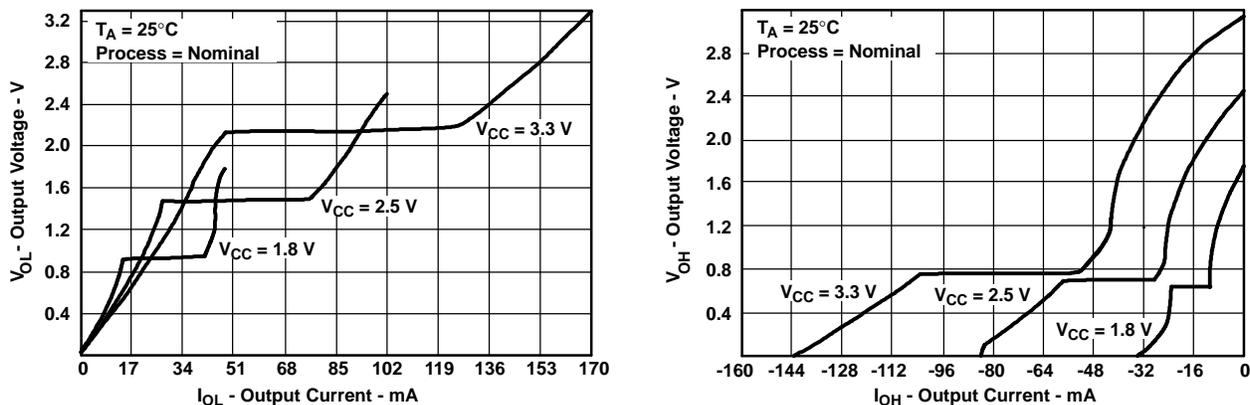


Figure 1. Output Voltage vs Output Current

This 12-bit to 24-bit registered bus exchanger is operational at 1.2-V to 3.6-V V_{CC} , but is designed specifically for 1.65-V to 3.6-V V_{CC} operation.

The SN74AVC16269 is used in applications in which two separate ports must be multiplexed onto, or demultiplexed from, a single port. The device is particularly suitable as an interface between synchronous DRAMs and high-speed microprocessors.

Data is stored in the internal B-port registers on the low-to-high transition of the clock (CLK) input when the appropriate clock-enable ($\overline{\text{CLKENA}}$) inputs are low. Proper control of these inputs allows two sequential 12-bit words to be presented as a 24-bit word on the B port. For data transfer in the B-to-A direction, a single storage register is provided. The select ($\overline{\text{SEL}}$) line selects 1B or 2B data for the A outputs. The register on the A output permits the fastest possible data transfer, thus extending the period during which the data is valid on the bus.



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SN74AVC16269
12-BIT TO 24-BIT REGISTERED BUS EXCHANGER
WITH 3-STATE OUTPUTS

SCES152G–DECEMBER 1998–REVISED MAY 2005

DESCRIPTION (CONTINUED)

The control terminals are registered so that all transactions are synchronous with CLK. Data flow is controlled by the active-low output enables (\overline{OEA} , $\overline{OEB1}$, $\overline{OEB2}$).

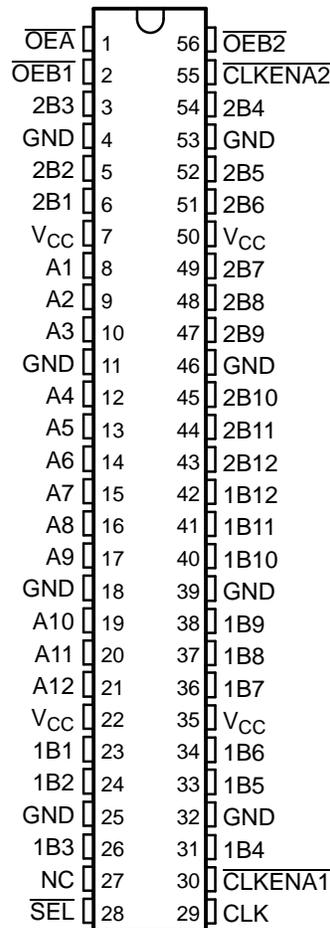
To ensure the high-impedance state during power up or power down, a clock pulse should be applied as soon as possible, and \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. Due to \overline{OE} being routed through a register, the active state of the outputs cannot be determined prior to the arrival of the first clock pulse.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The SN74AVC16269 is characterized for operation from -40°C to 85°C .

TERMINAL ASSIGNMENTS

DGG OR DGV PACKAGE
(TOP VIEW)



NC - No internal connection

FUNCTION TABLES

OUTPUT ENABLE

| INPUTS | | | OUTPUTS | |
|--------|------------------------|------------------------|---------|--------|
| CLK | $\overline{OE\bar{A}}$ | $\overline{OE\bar{B}}$ | A | 1B, 2B |
| ↑ | H | H | Z | Z |
| ↑ | H | L | Z | Active |
| ↑ | L | H | Active | Z |
| ↑ | L | L | Active | Active |

A-TO-B STORAGE ($\overline{OE\bar{B}} = L$)

| INPUTS | | | | OUTPUTS | |
|----------------------|----------------------|-----|---|--------------------------------|--------------------------------|
| $\overline{CLKENA1}$ | $\overline{CLKENA2}$ | CLK | A | 1B | 2B |
| H | H | X | X | 1B ₀ ⁽¹⁾ | 2B ₀ ⁽¹⁾ |
| L | X | ↑ | L | L | X |
| L | X | ↑ | H | H | X |
| X | L | ↑ | L | X | L |
| X | L | ↑ | H | X | H |

(1) Output level before the indicated steady-state input conditions were established

B-TO-A STORAGE ($\overline{OE\bar{A}} = L$)

| INPUTS | | | | OUTPUT |
|--------|------------------|----|----|-------------------------------|
| CLK | \overline{SEL} | 1B | 2B | A |
| X | H | X | X | A ₀ ⁽¹⁾ |
| X | L | X | X | A ₀ ⁽¹⁾ |
| ↑ | H | L | X | L |
| ↑ | H | H | X | H |
| ↑ | L | X | L | L |
| ↑ | L | X | H | H |

(1) Output level before the indicated steady-state input conditions were established

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---------------|--|-------------|----------------|-------------|
| V_{CC} | Supply voltage range | -0.5 | 4.6 | V |
| V_I | Input voltage range ⁽²⁾ | -0.5 | 4.6 | V |
| V_O | Voltage range applied to any input/output when the output is in the high-impedance or power-off state ⁽²⁾ | -0.5 | 4.6 | V |
| V_O | Voltage range applied to any input/output when the output is in the high or low state ⁽²⁾⁽³⁾ | -0.5 | $V_{CC} + 0.5$ | V |
| I_{IK} | Input clamp current | $V_I < 0$ | -50 | mA |
| I_{OK} | Output clamp current | $V_O < 0$ | -50 | mA |
| I_O | Continuous output current | | ±50 | mA |
| | Continuous current through each V_{CC} or GND | | ±100 | mA |
| θ_{JA} | Package thermal impedance ⁽⁴⁾ | DGG package | 64 | °C/W |
| | | DGV package | 48 | |
| T_{stg} | Storage temperature range | -65 | 150 | °C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.
- (4) The package thermal impedance is calculated in accordance with JESD 51.

SN74AVC16269
12-BIT TO 24-BIT REGISTERED BUS EXCHANGER
WITH 3-STATE OUTPUTS

SCES152G–DECEMBER 1998–REVISED MAY 2005

Recommended Operating Conditions⁽¹⁾

| | | MIN | MAX | UNIT | |
|------------------|---|------------------------------------|------------------------|-----------------|------|
| V _{CC} | Supply voltage | Operating | 1.4 | 3.6 | V |
| | | Data retention only | 1.2 | | |
| V _{IH} | High-level input voltage | V _{CC} = 1.2 V | V _{CC} | | V |
| | | V _{CC} = 1.4 V to 1.6 V | 0.65 × V _{CC} | | |
| | | V _{CC} = 1.65 V to 1.95 V | 0.65 × V _{CC} | | |
| | | V _{CC} = 2.3 V to 2.7 V | 1.7 | | |
| | | V _{CC} = 3 V to 3.6 V | 2 | | |
| V _{IL} | Low-level input voltage | V _{CC} = 1.2 V | GND | | V |
| | | V _{CC} = 1.4 V to 1.6 V | 0.35 × V _{CC} | | |
| | | V _{CC} = 1.65 V to 1.95 V | 0.35 × V _{CC} | | |
| | | V _{CC} = 2.3 V to 2.7 V | 0.7 | | |
| | | V _{CC} = 3 V to 3.6 V | 0.8 | | |
| V _I | Input voltage | 0 | 3.6 | V | |
| V _O | Output voltage | Active state | 0 | V _{CC} | V |
| | | 3-state | 0 | 3.6 | |
| I _{OHS} | Static high-level output current ⁽²⁾ | V _{CC} = 1.4 V to 1.6 V | –2 | | mA |
| | | V _{CC} = 1.65 V to 1.95 V | –4 | | |
| | | V _{CC} = 2.3 V to 2.7 V | –8 | | |
| | | V _{CC} = 3 V to 3.6 V | –12 | | |
| I _{OLS} | Static low-level output current ⁽²⁾ | V _{CC} = 1.4 V to 1.6 V | 2 | | mA |
| | | V _{CC} = 1.65 V to 1.95 V | 4 | | |
| | | V _{CC} = 2.3 V to 2.7 V | 8 | | |
| | | V _{CC} = 3 V to 3.6 V | 12 | | |
| Δt/Δv | Input transition rise or fall rate | V _{CC} = 1.4 V to 3.6 V | | 5 | ns/V |
| T _A | Operating free-air temperature | –40 | 85 | °C | |

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

(2) Dynamic drive capability is equivalent to standard outputs with I_{OH} and I_{OL} of ±24 mA at 3.3-V V_{CC}. See Figure 1 for V_{OL} vs I_{OL} and V_{OH} vs I_{OH} characteristics. Refer to the TI application reports, *AVC Logic Family Technology and Applications*, literature number SCEA006, and *Dynamic Output Control (DOC™) Circuitry Technology and Applications*, literature number SCEA009.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|--------------------------------|----------------|---|-----------------|-----------------------|--------------------|-------|------|
| V _{OH} | | I _{OHS} = -100 μA | 1.4 V to 3.6 V | V _{CC} - 0.2 | | | V |
| | | I _{OHS} = -2 mA, V _{IH} = 0.91 V | 1.4 V | 1.05 | | | |
| | | I _{OHS} = -4 mA, V _{IH} = 1.07 V | 1.65 V | 1.2 | | | |
| | | I _{OHS} = -8 mA, V _{IH} = 1.7 V | 2.3 V | 1.75 | | | |
| | | I _{OHS} = -12 mA, V _{IH} = 2 V | 3 V | 2.3 | | | |
| V _{OL} | | I _{OLS} = 100 μA | 1.4 V to 3.6 V | | | 0.2 | V |
| | | I _{OLS} = 2 mA, V _{IL} = 0.49 V | 1.4 V | | | 0.4 | |
| | | I _{OLS} = 4 mA, V _{IL} = 0.57 V | 1.65 V | | | 0.45 | |
| | | I _{OLS} = 8 mA, V _{IL} = 0.7 V | 2.3 V | | | 0.55 | |
| | | I _{OLS} = 12 mA, V _{IL} = 0.8 V | 3 V | | | 0.7 | |
| I _I | Control inputs | V _I = V _{CC} or GND | 3.6 V | | | ±2.5 | μA |
| I _{off} | | V _I or V _O = 3.6 V | 0 | | | ±10 | μA |
| I _{OZ} ⁽²⁾ | | V _O = V _{CC} or GND | 3.6 V | | | ±12.5 | μA |
| I _{CC} | | V _I = V _{CC} or GND, I _O = 0 | 3.6 V | | | 40 | μA |
| C _i | Control inputs | V _I = V _{CC} or GND | 2.5 V | | | 3.5 | pF |
| | | | 3.3 V | | | 3.5 | |
| C _{io} | A or B ports | V _O = V _{CC} or GND | 2.5 V | | | 8.5 | pF |
| | | | 3.3 V | | | 8.5 | |

 (1) Typical values are measured at T_A = 25°C.

 (2) For I/O ports, the parameter I_{OZ} includes the input leakage current.

Timing Requirements

 over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 2](#) through [Figure 5](#))

| | | V _{CC} = 1.2 V | V _{CC} = 1.5 V ± 0.1 V | | V _{CC} = 1.8 V ± 0.15 V | | V _{CC} = 2.5 V ± 0.2 V | | V _{CC} = 3.3 V ± 0.3 V | | UNIT |
|--------------------|---------------------------------|--|------------------------------------|-----|-------------------------------------|-----|------------------------------------|-----|------------------------------------|-----|------|
| | | TYP | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| f _{clock} | Clock frequency | | | | 75 | | 125 | | 175 | | MHz |
| t _w | Pulse duration, CLK high or low | | | | 5.8 | | 5 | | 3.5 | | ns |
| t _{su} | Setup time | A data before CLK↑ | 4.7 | 3.9 | 2.6 | 2.1 | 1.9 | | | ns | |
| | | B data before CLK↑ | 6.2 | 4.3 | 3 | 2.1 | 1.9 | | | | |
| | | $\overline{\text{SEL}}$ before CLK↑ | 4.5 | 3.4 | 2.2 | 1.6 | 1.3 | | | | |
| | | $\overline{\text{CLKENA1}}$ or $\overline{\text{CLKENA2}}$ before CLK↑ | 0.9 | 0.9 | 1 | 1.1 | 1.1 | | | | |
| | | $\overline{\text{OE}}$ before CLK↑ | 5.4 | 5.3 | 2 | 1.6 | 1.1 | | | | |
| t _h | Hold time | A data after CLK↑ | 1.9 | 2 | 1.2 | 1.1 | 1 | | | ns | |
| | | B data after CLK↑ | 0.4 | 1.3 | 0.5 | 0.6 | 0.7 | | | | |
| | | $\overline{\text{SEL}}$ after CLK↑ | 1 | 1 | 0.4 | 0.3 | 0.4 | | | | |
| | | $\overline{\text{CLKENA1}}$ or $\overline{\text{CLKENA2}}$ after CLK↑ | 2.6 | 2.2 | 1.4 | 1.1 | 1 | | | | |
| | | $\overline{\text{OE}}$ after CLK↑ | 0.4 | 0.4 | 0.4 | 0.5 | 0.3 | | | | |

SN74AVC16269
12-BIT TO 24-BIT REGISTERED BUS EXCHANGER
WITH 3-STATE OUTPUTS



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Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 2](#) through [Figure 5](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 1.2\text{ V}$ | | $V_{CC} = 1.5\text{ V} \pm 0.1\text{ V}$ | | $V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$ | | $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ | | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | | UNIT |
|-----------|--------------|-------------|-------------------------|-----|--|-----|---|-----|--|-----|--|-----|------|
| | | | TYP | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| f_{max} | | | | | | | 75 | | 125 | | 175 | | MHz |
| t_{pd} | CLK | B | 13.5 | 3 | 9.5 | 2.5 | 6.7 | 1.6 | 4 | 1.1 | 3 | | ns |
| | | A | 11.6 | 2.6 | 7.4 | 2.2 | 5.8 | 1.5 | 3.5 | 1 | 2.7 | | |
| t_{en} | CLK | B | 16 | 3.5 | 12 | 2.4 | 8.5 | 2.1 | 4.8 | 1.5 | 3.8 | | ns |
| | | A | 14.2 | 3.2 | 9.3 | 2 | 6.7 | 2 | 4.4 | 1.4 | 3.4 | | |
| t_{dis} | CLK | B | 16 | 4.9 | 12.3 | 3.3 | 8.5 | 1.9 | 4.8 | 1.3 | 3.7 | | ns |
| | | A | 11.9 | 3 | 8.7 | 2.1 | 6.7 | 1.8 | 3.6 | 1.7 | 3.4 | | |

Switching Characteristics⁽¹⁾

$T_A = 0^\circ\text{C}$ to 85°C , $C_L = 0\text{ pF}$

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 3.3\text{ V} \pm 0.15\text{ V}$ | | UNIT |
|-----------|--------------|-------------|---|-----|------|
| | | | MIN | MAX | |
| t_{pd} | CLK | B | 1.4 | 2.4 | ns |
| | | A | 1.2 | 2.1 | |

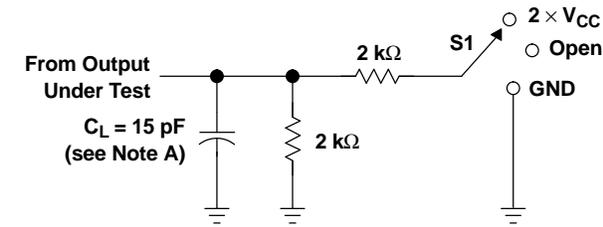
(1) Texas Instruments SPICE simulation data

Operating Characteristics

$T_A = 25^\circ\text{C}$

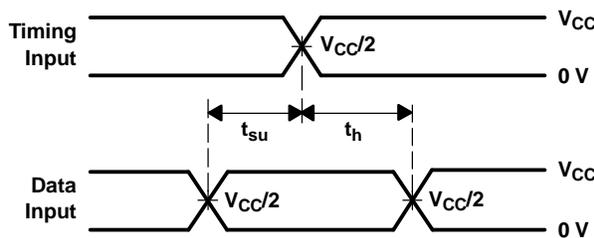
| PARAMETER | | TEST CONDITIONS | $V_{CC} = 1.8\text{ V}$ | $V_{CC} = 2.5\text{ V}$ | $V_{CC} = 3.3\text{ V}$ | UNIT | |
|-----------|-------------------------------|------------------|------------------------------------|-------------------------|-------------------------|------|----|
| | | | TYP | TYP | TYP | | |
| C_{pd} | Power dissipation capacitance | Outputs enabled | $C_L = 0, \quad f = 10\text{ MHz}$ | 133 | 145 | 168 | pF |
| | | Outputs disabled | | 102 | 109 | 124 | |

PARAMETER MEASUREMENT INFORMATION
 $V_{CC} = 1.2\text{ V AND }1.5\text{ V} \pm 0.1\text{ V}$

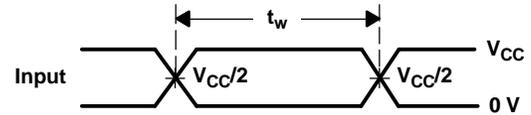


LOAD CIRCUIT

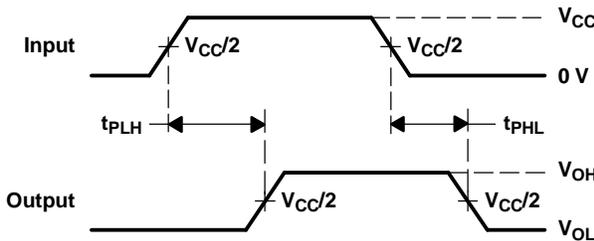
| TEST | S1 |
|-------------------|---------------------|
| t_{pd} | Open |
| t_{PLZ}/t_{PZL} | 2 \times V_{CC} |
| t_{PHZ}/t_{PZH} | GND |



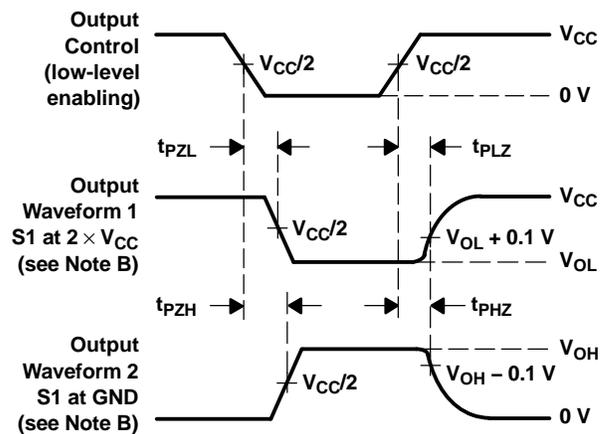
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



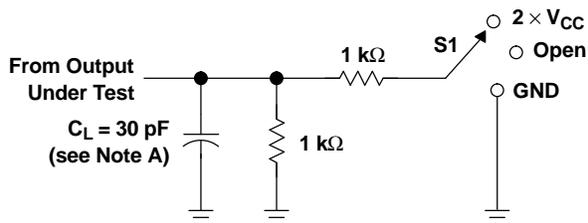
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: PRR $\leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

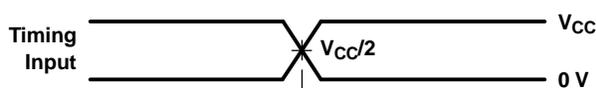
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$

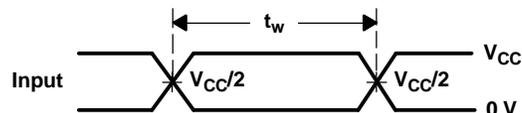


LOAD CIRCUIT

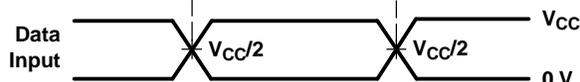
| TEST | S1 |
|-------------------|---------------------|
| t_{pd} | Open |
| t_{PLZ}/t_{PZL} | 2 \times V_{CC} |
| t_{PHZ}/t_{PZH} | GND |



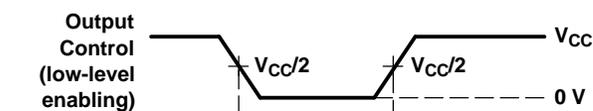
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



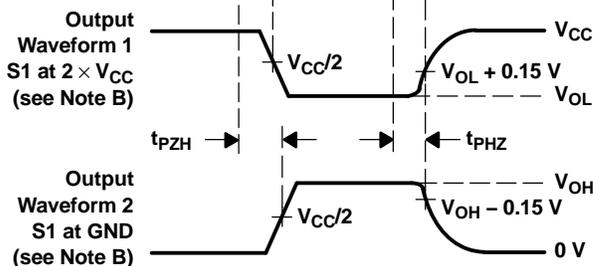
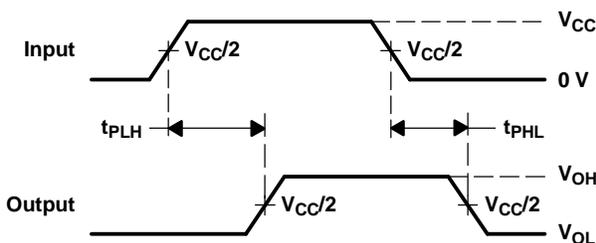
VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



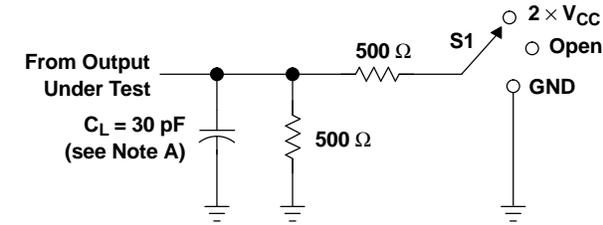
VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES



- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
F. t_{PZL} and t_{PZH} are the same as t_{en} .
G. t_{PLH} and t_{PHL} are the same as t_{pd} .

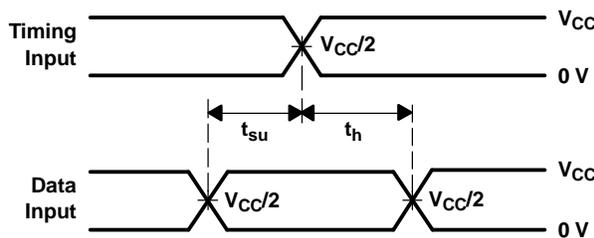
Figure 3. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
 $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$

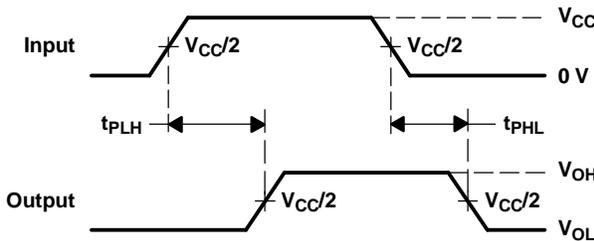


LOAD CIRCUIT

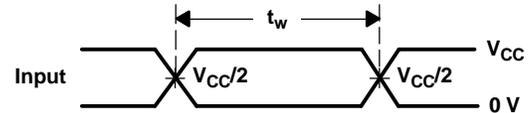
| TEST | S1 |
|-------------------|-------------------|
| t_{pd} | Open |
| t_{PLZ}/t_{PZL} | 2 $\times V_{CC}$ |
| t_{PHZ}/t_{PZH} | GND |



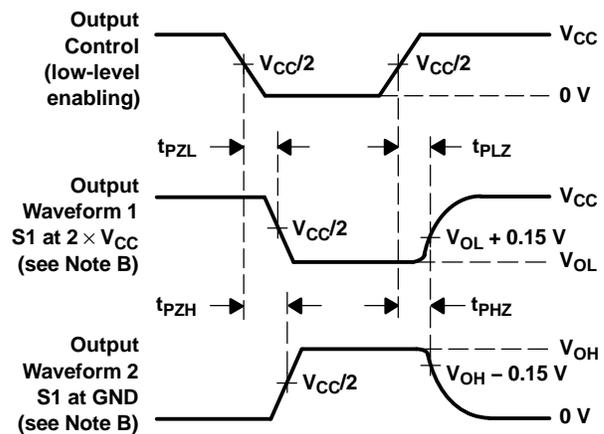
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION

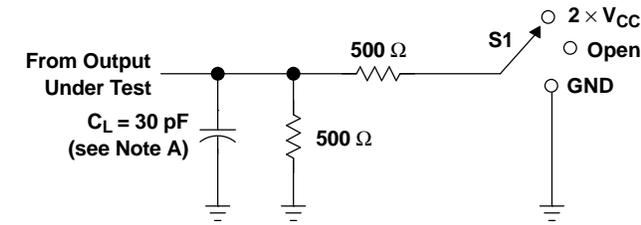


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
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G. t_{PLH} and t_{PHL} are the same as t_{pd} .

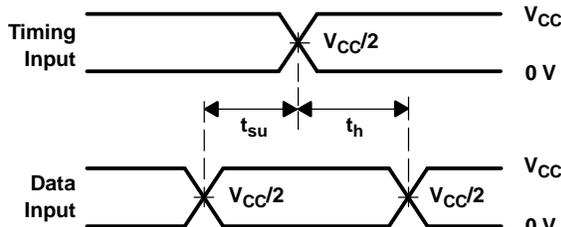
Figure 4. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

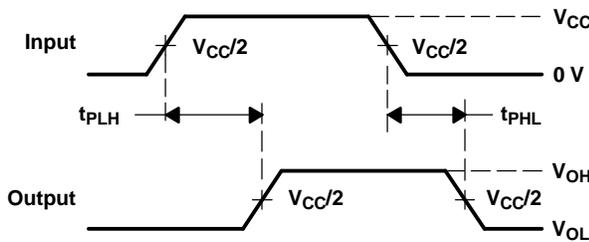


| TEST | S1 |
|-------------------|-------------------|
| t_{pd} | Open |
| t_{PLZ}/t_{PZL} | $2 \times V_{CC}$ |
| t_{PHZ}/t_{PZH} | GND |

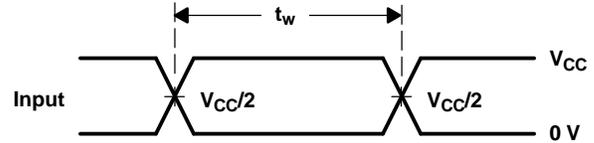
LOAD CIRCUIT



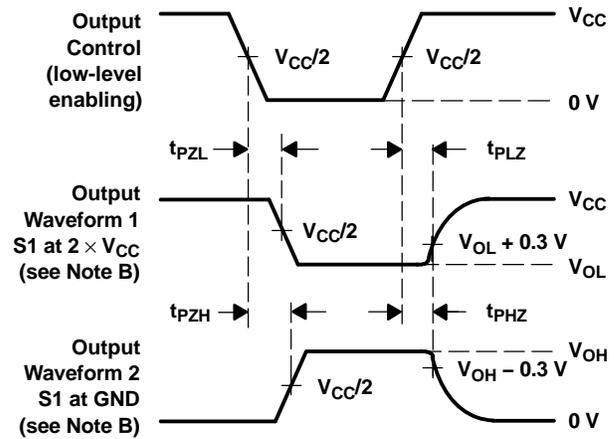
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
F. t_{PZL} and t_{PZH} are the same as t_{en} .
G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 5. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/ Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|----------------------------|----------------------|------------------------------|-----------------------------|
| 74AVC16269DGGRE4 | ACTIVE | TSSOP | DGG | 56 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| 74AVC16269DGGRG4 | ACTIVE | TSSOP | DGG | 56 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74AVC16269DGGR | ACTIVE | TSSOP | DGG | 56 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

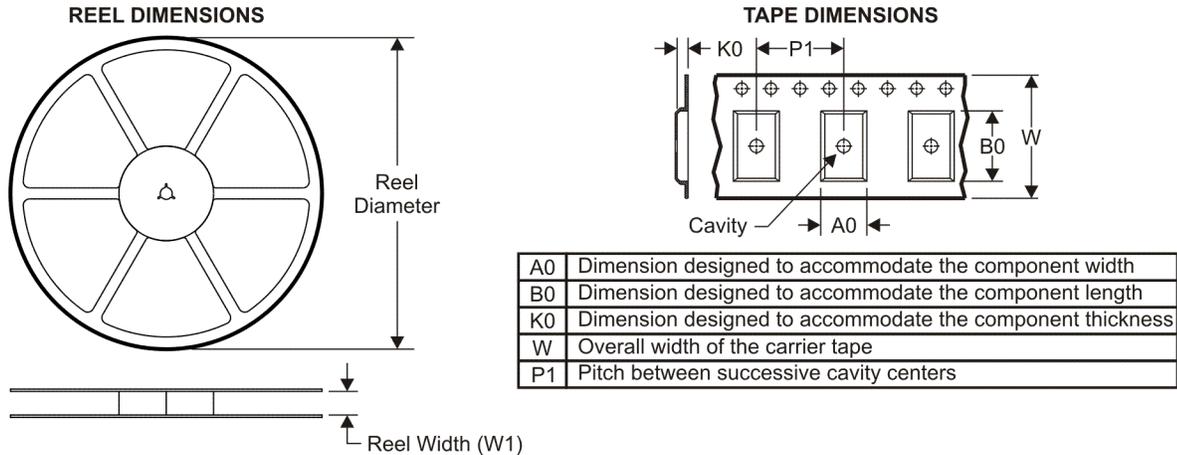
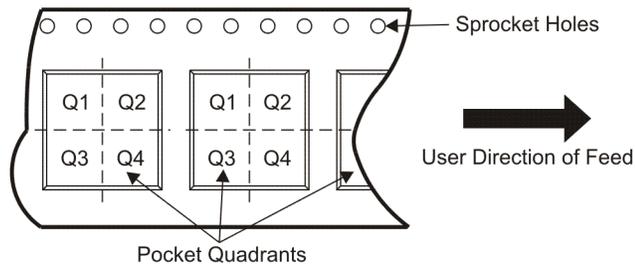
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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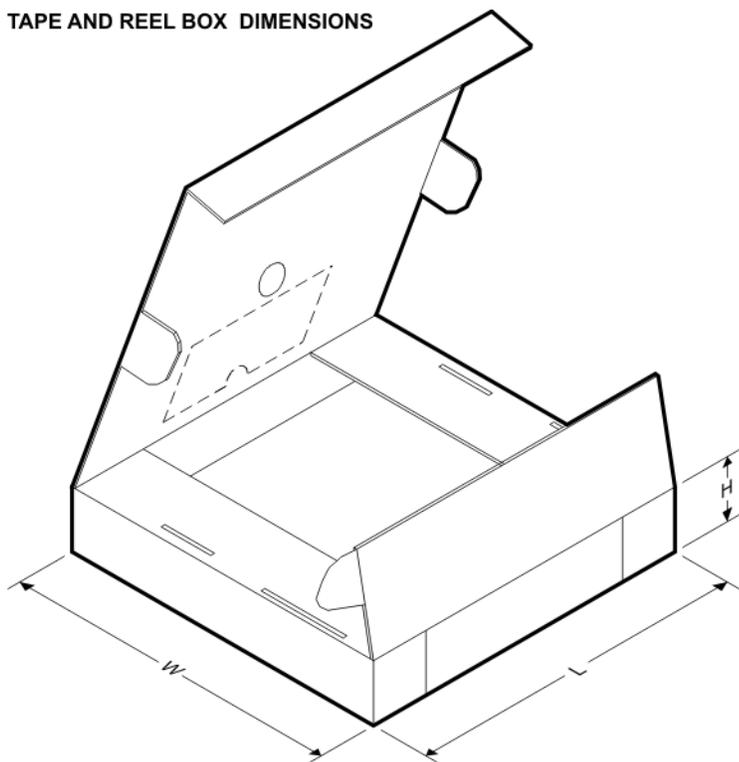
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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74AVC16269DGGR | TSSOP | DGG | 56 | 2000 | 330.0 | 24.4 | 8.6 | 15.6 | 1.8 | 12.0 | 24.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



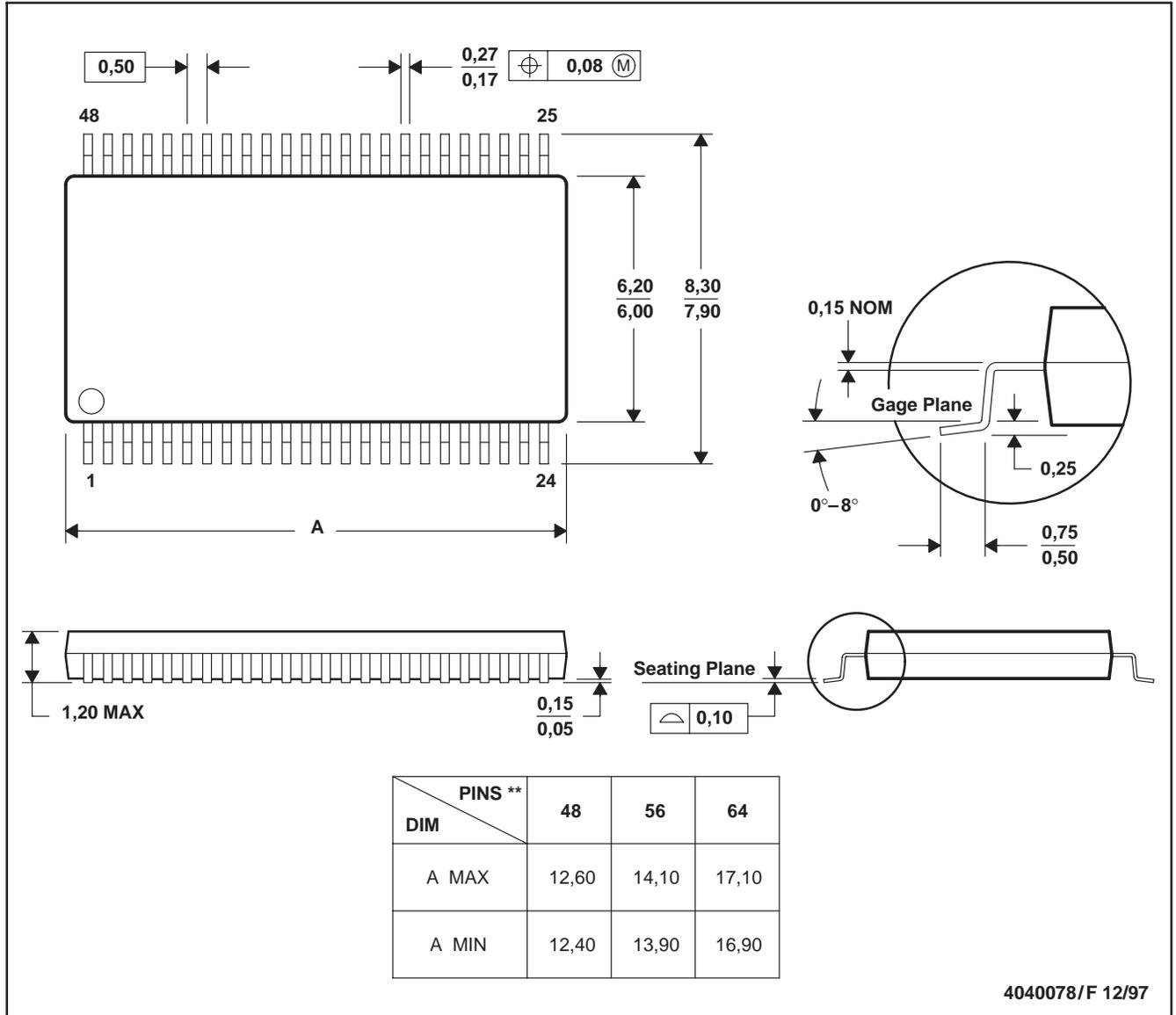
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74AVC16269DGGR | TSSOP | DGG | 56 | 2000 | 346.0 | 346.0 | 41.0 |

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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