SCBS247G - AUGUST 1992 - REVISED JULY 1998

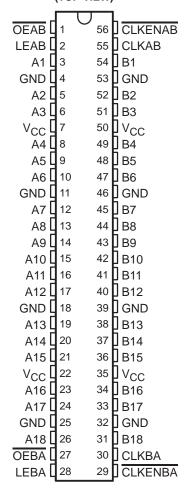
- **Members of the Texas Instruments** Widebus™ Family
- B-Port Outputs Have Equivalent 25- $\Omega$ Series Resistors, So No External Resistors Are Required
- State-of-the-Art *EPIC-IIB™* BiCMOS Design Significantly Reduces Power Dissipation
- **UBT** ™ (Universal Bus Transceiver) **Combines D-Type Latches and D-Type** Flip-Flops for Operation in Transparent, Latched, Clocked, or Clock-Enabled Mode
- Latch-Up Performance Exceeds 500 mA Per **JESD 17**
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 0.8 V at  $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$
- **High-Impedance State During Power Up** and Power Down
- Flow-Through Architecture Optimizes PCB Layout
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package **Using 25-mil Center-to-Center Spacings**

#### description

These 18-bit universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the clock-enable (CLKENAB and CLKENBA) inputs.

SN54ABT162601...WD PACKAGE SN74ABT162601...DGG OR DL PACKAGE (TOP VIEW)



For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. Output-enable OEAB is active-low. When OEAB is low, the outputs are active. When OEAB is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that of A to B but uses  $\overline{OEBA}$ , LEBA, CLKBA, and  $\overline{CLKENBA}$ .

The B-port outputs, which are designed to source or sink up to 12 mA, include equivalent  $25-\Omega$  series resistors to reduce overshoot and undershoot.

When  $V_{CC}$  is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.



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# SN54ABT162601, SN74ABT162601 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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# description (continued)

The SN54ABT162601 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to  $125^{\circ}$ C. The SN74ABT162601 is characterized for operation from  $-40^{\circ}$ C to  $85^{\circ}$ C.

#### **FUNCTION TABLE**<sup>†</sup>

	OUTPUT				
CLKENAB	OEAB	LEAB	CLKAB	Α	В
Х	Н	Х	Х	Χ	Z
Х	L	Н	X	L	L
Х	L	Н	X	Н	н
Н	L	L	X	Χ	в <sub>0</sub> ‡
Н	L	L	X	Χ	В <sub>0</sub> ‡ В <sub>0</sub> ‡
L	L	L	$\uparrow$	L	L
L	L	L	$\uparrow$	Н	н
L	L	L	L	Χ	B <sub>0</sub> ‡
L	L	L	Н	Χ	В <sub>0</sub> §

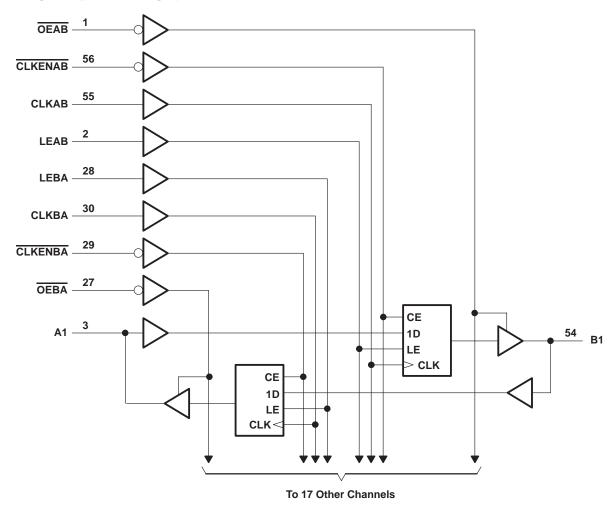
<sup>†</sup> A-to-B data flow is shown: B-to-A flow is similar but uses  $\overline{\text{OEBA}}$ , LEBA, CLKBA, and  $\overline{\text{CLKENBA}}$ .



<sup>‡</sup> Output level before the indicated steady-state input conditions were established

<sup>§</sup> Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low

## logic diagram (positive logic)



# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)	
Voltage range applied to any output in the high or power-off state, VO	0.5 V to 5.5 V
Current into any output in the low state, IO: SN54ABT162601 (A port)	96 mA
SN74ABT162601 (A port)	128 mA
B port	30 mA
Input clamp current, $I_{ K }(V_{ I } < 0)$	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 2): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, T <sub>Stq</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.



# SN54ABT162601, SN74ABT162601 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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# recommended operating conditions (see Note 3)

			SN54ABT	162601	SN74ABT	162601	UNIT	
		MIN	MAX	MIN	MAX	UNIT		
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V	
VIH	High-level input voltage		2		2		V	
V <sub>IL</sub>	Low-level input voltage		0.8		8.0	V		
VI	Input voltage		0	Vcc	0	VCC	V	
la	High level output ourrent	A port		-24		-32	mA	
ЮН	High-level output current	B port		-12		-12	IIIA	
1	Low lovel output ourrent	A port				64	A	
lOL	Low-level output current	B port		12		12	mA	
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V	
Δt/ΔVCC	Power-up ramp rate	-	200		200		μs/V	
T <sub>A</sub>	Operating free-air temperature	-55	125	-40	85	°C		

NOTE 3: All unused inputs of the devices must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application note, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DAI	RAMETER	TEST CON	Т	A = 25°C	;	SN54ABT	162601	SN74ABT162601		UNIT	
FAI	KAWETEK	TEST CON	IDITIONS	MIN	TYP <sup>†</sup>	MAX	MIN	MAX	MIN	MAX	UNIT
٧ıK		$V_{CC} = 4.5 \text{ V},$	I <sub>I</sub> = -18 mA			-1.2		-1.2		-1.2	V
		$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -3 \text{ mA}$	2.5			2.5		2.5		
	A port	$V_{CC} = 5 V$ ,	$I_{OH} = -3 \text{ mA}$	3			3		3		
	A port	V 45V	I <sub>OH</sub> = -24 mA	2			2				
V		V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = -32 mA	2*					2		V
VOH		V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -1 mA	3.35			3.3		3.35		V
	D nort	V <sub>CC</sub> = 5 V,	$I_{OH} = -1 \text{ mA}$	3.85			3.8		3.85		
	B port	V <sub>CC</sub> = 4.5 V	$I_{OH} = -3 \text{ mA}$	3.1			3		3.1		
		VCC = 4.5 V	I <sub>OH</sub> = -12 mA	2.6					2.6		
	A port	V00 - 4 5 V	I <sub>OL</sub> = 48 mA			0.55		0.55			
VOL	A port	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 64 mA			0.55*				0.55	V
	B port	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 12 mA			0.8		0.8		0.8	
V <sub>hys</sub>					100						mV
	Control inputs	V <sub>CC</sub> = 0 to 5.5 V, V <sub>I</sub>			±1		±1		±1		
ΙΙ	A or B ports	$V_{CC} = 2.1 \text{ V to } 5.5 \text{ V}$ $V_I = V_{CC} \text{ or GND}$			±20		±20		±20	μΑ	
lozpu	J	$V_{CC} = 0 \text{ to } 2.1 \text{ V},$ $V_{O} = 0.5 \text{ V to } 2.7 \text{ V},$			±50		±50**		±50	μΑ	
IOZPE	)	V <sub>CC</sub> = 2.1 V to 0, V <sub>O</sub> = 0.5 V to 2.7 V,			±50		±50**		±50	μА	
loz <sub>H</sub> ‡	:	$V_{CC} = 2.1 \text{ V to } 5.5 \text{ V}$ $V_{O} = 2.7 \text{ V}, \text{ OE } \ge 2 \text{ V}$				10		10		10	μΑ
l <sub>OZL</sub> ‡		$V_{CC} = 2.1 \text{ V to } 5.5 \text{ V}$ $V_{O} = 0.5 \text{ V}, \overline{OE} \ge 2 \text{ V}$	/, /			-10		-10		-10	μΑ
l <sub>off</sub>		$V_{CC} = 0$ ,	V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V			±100*				±100	μА
ICEX		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μΑ
	A port	V 55V		-50	-100	-180	-50	-180	-50	-180	Δ
ΙΟ§	B port	V <sub>CC</sub> = 5.5 V,	$V_0 = 2.5 \text{ V}$	-25	-55	-100	-25	-100	-25	-100	mA
		V <sub>CC</sub> = 5.5 V,	Outputs high			3		3		3	
Icc	A or B ports	$I_{O} = 0$ ,	Outputs low			36		36		36	mA
		$V_I = V_{CC}$ or GND	Outputs disabled			3		3		3	
ΔICC¶			V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND			50		50		50	μА
Ci	Control inputs	V <sub>I</sub> = 2.5 V or 0.5 V			3						pF
C <sub>io</sub>	A or B ports	V <sub>O</sub> = 2.5 V or 0.5 V			9						pF
.5	<u>' '</u>										

<sup>\*</sup> On products compliant to MIL-PRF-38535, this parameter does not apply.



<sup>\*\*</sup> On products compliant to MIL-PRF-38535, this parameter is not production tested.

 $<sup>\</sup>dagger$  All typical values are at  $V_{CC} = 5 \text{ V}$ .

<sup>&</sup>lt;sup>‡</sup> The parameters IOZH and IOZL include the input leakage current.

<sup>§</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>¶</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

# SN54ABT162601, SN74ABT162601 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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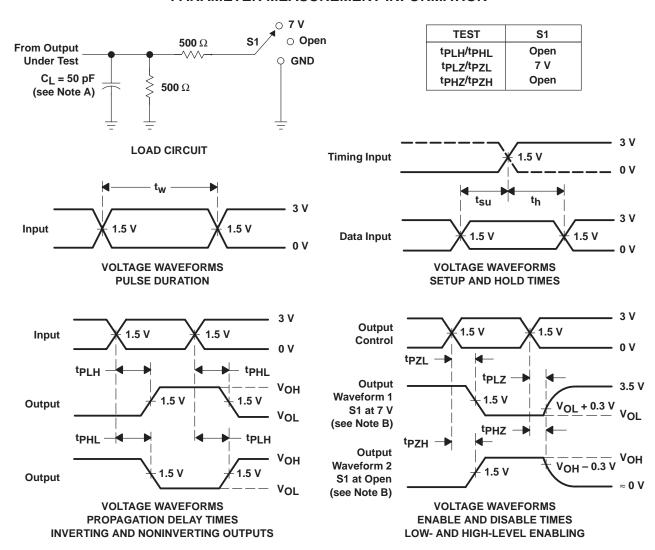
# timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(see Figure 1)

				SN54ABT	162601	SN74ABT	162601	UNIT
				MIN	MAX	MIN	MAX	UNIT
fclock	Clock frequency			0	150	0	150	MHz
t <sub>W</sub> Pulse duration	LEAB or LEBA high		2.5		2.5			
	Puise duration	CLKAB or CLKBA high or low	3.3		3		ns	
		A before CLKAB↑ or B before CLKBA↑	4.8		4.3			
	Catum time	A. ( 1500 D. ( 1500 D.	CLK high	2.5		2.5		ns
t <sub>su</sub>	Setup time	A before LEAB↓ or B before LEBA↓	CLK low	1.2		1		
		CLKEN before CLK↑	CLKEN before CLK↑			2.7		
		A after CLKAB↑ or B after CLKBA↑	0.5		0			
th	Hold time	A after LEAB↓ or B after LEBA↓	2		0.5		ns	
		CLKEN after CLK↑		0.5		0		.

# switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>(</sub>	CC = 5 V A = 25°C	', ;	SN54ABT	162601	SN74ABT162601		UNIT	
	(INFOT)	(001F01)	MIN	TYP	MAX	MIN	MAX	MIN	MAX		
f <sub>max</sub>			150			150		150		MHz	
<sup>t</sup> PLH	А	В	1.5	2.8	4	1.5	5.1	1.5	4.8	ns	
t <sub>PHL</sub>	A	<u> </u>	2	3.7	5.2	2	6.1	2	5.7	115	
t <sub>PLH</sub>	В	А	1	2.5	3.6	1	4.5	1	4	ns	
t <sub>PHL</sub>	Ь	A	2	3.3	4.5	2	5.1	2	4.9	115	
<sup>t</sup> PLH	LEBA	А	2	3.3	4.5	2	5.6	2	5	ns	
t <sub>PHL</sub>	LEDA	^	2	3.6	4.7	2	5.4	2	5	115	
<sup>t</sup> PLH	LEAB	В	2	3.4	4.8	2	6.1	2	5.6	ns	
<sup>t</sup> PHL	LLAD	Ь	2	3.8	5.2	2	6.4	2	5.9	113	
<sup>t</sup> PLH	CLKBA	А	1.5	3.1	4.7	1.5	5.4	1.5	5.3	ns	
<sup>t</sup> PHL	CLNDA	A	1.5	3.1	4.3	1.5	5.2	1.5	5	113	
<sup>t</sup> PLH	CLKAB	В	1.5	3.3	4.7	1.5	6	1.5	5.5	ns	
<sup>t</sup> PHL	CLNAD	В	1.5	3.5	4.8	1.5	5.8	1.5	5.3	118	
<sup>t</sup> PZH	<del>OEBA</del>	А	2	3.5	4.6	2	5.5	2	5.1	nc	
t <sub>PZL</sub>	OEBA	^	2	3.7	4.7	2	5.8	2	5.4	ns	
<sup>t</sup> PZH	OEAB	В	2	3.8	5.3	1.5	6.6	2	6.1	ns	
<sup>t</sup> PZL	OEAB		2	3.6	5.1	2	6.2	2	5.7	115	
<sup>t</sup> PHZ	<del>OEBA</del>	А	2	3.6	5.4	1.4	6.6	2	6.2	ns	
t <sub>PLZ</sub>	OEBA		1.5	3.2	4.7	1.5	5.8	1.5	5.4	118	
<sup>t</sup> PHZ	<del></del> OEAB	В	2	3.4	4.8	1.4	5.6	2	5.4	ns	
<sup>t</sup> PLZ	OLAB		1.5	3.2	4.5	1.5	5.7	1.5	5.2	119	

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \ \Omega$ ,  $t_f \leq 2.5 \ ns$ ,  $t_f \leq 2.5 \ ns$ .
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms





5-Sep-2011

#### **PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
5962-9859301QXA	ACTIVE	CFP	WD	56	1	TBD	Call TI	Call TI	
74ABT162601DGGRE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74ABT162601DGGRG4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74ABT162601DLRG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ABT162601DGGR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ABT162601DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ABT162601DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ABT162601DLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SNJ54ABT162601WD	ACTIVE	CFP	WD	56	1	TBD	A42	N / A for Pkg Type	

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.





5-Sep-2011

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#### OTHER QUALIFIED VERSIONS OF SN54ABT162601, SN74ABT162601:

Catalog: SN74ABT162601

Military: SN54ABT162601

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications



## TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



### \*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT162601DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
SN74ABT162601DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1





\*All dimensions are nominal

Device	Package Type Package Drawing		vice Package Type Package D		Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT162601DGGR	TSSOP	DGG	56	2000	346.0	346.0	41.0		
SN74ABT162601DLR	SSOP	DL	56	1000	346.0	346.0	49.0		

## WD (R-GDFP-F\*\*)

#### **CERAMIC DUAL FLATPACK**

### **48 LEADS SHOWN**



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only
- E. Falls within MIL STD 1835: GDFP1-F48 and JEDEC MO-146AA

GDFP1-F56 and JEDEC MO-146AB

## DL (R-PDSO-G\*\*)

### **48 PINS SHOWN**

#### PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MO-118

# DGG (R-PDSO-G\*\*)

# PLASTIC SMALL-OUTLINE PACKAGE

#### **48 PINS SHOWN**



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

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