

DGG OR DL PACKAGE

SCES017G-JULY 1995-REVISED SEPTEMBER 2004

### **FEATURES**

- Member of the Texas Instruments Widebus™ Family
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22 - 2000-V Human-Body Model (A114-A)

  - 200-V Machine Model (A115-A)

### DESCRIPTION/ORDERING INFORMATION

This 12-bit to 24-bit bus exchanger is designed for 1.65-V to 3.6-V V<sub>CC</sub> operation.

The SN74ALVCH16271 is intended for applications in which two separate data paths must be multiplexed onto, or demultiplexed from, a single data path. This device is particularly suitable as an interface between conventional DRAMs and high-speed microprocessors.

A data is stored in the internal A-to-B registers on the low-to-high transition of the clock (CLK) input, provided that the clock-enable (CLKENA) inputs are low. Proper control of these inputs allows two sequential 12-bit words to be presented as a 24-bit word on the B port.

Transparent latches in the B-to-A path allow asynchronous operation to maximize memory access throughput. These latches transfer data when the latch-enable (LE) inputs are low. The select (SEL) line selects 1B or 2B data for the A outputs. Data flow is controlled by the active-low output enables (OEA, OEB).

	(TOP VI	EW)	)
OEA [ LE1B [ 2B3 [	1 2 3	56 55 54	F
GND [	4	53	] GND
2B2 [	5	52	] 2B5
2B1 [	6	51	] 2B6
V <sub>CC</sub> [	7	50	] V <sub>CC</sub>
A1 [	8	49	<b>F</b>
A2 [	9	48	] 2B8
A3 [		47	<b>]</b> 2B9
GND [	11	46	
A4 [	12		] 2B10
A5 [	13	44	] 2B11
A6 [	14	43	] 2B12
A7 [	15	42	] 1B12
A8 [	16	41	] 1B11
A9 [	17		] 1B10
GND [	18	39	] GND
A10 [	19	38	] 1B9
A11 [	20	37	] 1B8
A12 [	21	36	] 1B7
V <sub>CC</sub> [	22	35	]V <sub>cc</sub>
1B1 [	23	34	] 1B6
1B2 [	24	33	] 1B5
GND [	25	32	] GND
1B3 [	26	31	] 1B4
LE2B	27	30	CLKENA1
SEL [	28	29	] CLK

To ensure the high-impedance state during power up or power down, the output enables should be tied to  $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

#### **ORDERING INFORMATION**

T <sub>A</sub>	PACK	AGE <sup>(1)</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING	
	SSOP - DL	Tube	SN74ALVCH16271DL	ALVCH16271	
-40°C to 85°C	330F - DL	Tape and reel	SN74ALVCH16271DLR	ALVCH16271	
	TSSOP - DGG	Tape and reel	SN74ALVCH16271DGGR	ALVCH16271	

(1) Package drawings, standard packing guantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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#### **FUNCTION TABLES**

#### **OUTPUT ENABLE**

INP	UTS	OUTPUTS		
OEA	OEB	Α	1B, 2B	
Н	Н	Z	Z	
н	L	Z	Active	
L	н	Active	Z	
L	L	Active	Active	

### A-TO-B STORAGE ( $\overline{OEB} = L$ )

	INPU	OUTPUTS			
CLKENA1	CLKENA2	CLK	Α	1B	2B
Н	Н	Х	Х	1B <sub>0</sub> <sup>(1)</sup>	2B <sub>0</sub> <sup>(1)</sup>
L	Х	$\uparrow$	L	L	Х
L	Х	$\uparrow$	н	Н	Х
Х	L	$\uparrow$	L	Х	L
Х	L	$\uparrow$	Н	A <sub>0</sub>	н

(1) Output level before the indicated steady-state input conditions were established

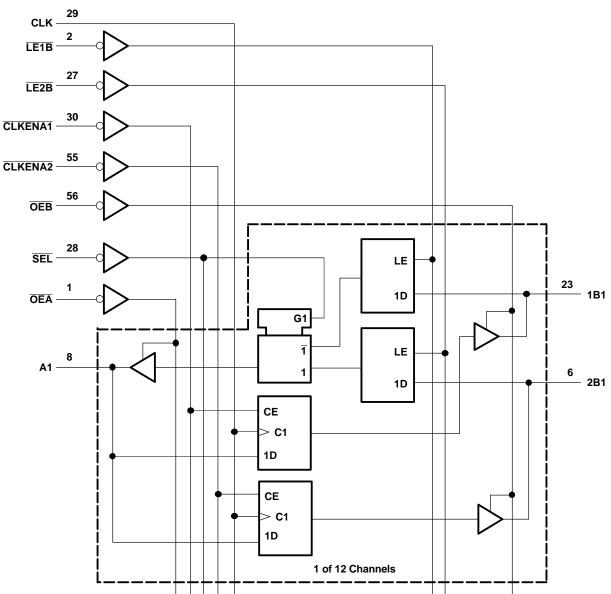
#### B-TO-A STORAGE ( $\overline{OEA} = L$ )

	INPUTS							
LE	SEL	1B	2B	Α				
Н	Х	Х	Х	A <sub>0</sub> <sup>(1)</sup>				
н	х	Х	Х	A <sub>0</sub> <sup>(1)</sup> A <sub>0</sub> <sup>(1)</sup>				
L	н	L	Х	L				
L	н	Н	Х	н				
L	L	Х	L	L				
L	L	Х	Н	Н				

(1) Output level before the indicated steady-state input conditions were established



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LOGIC DIAGRAM (POSITIVE LOGIC)

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### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range		-0.5	4.6	V
V		Except I/O ports <sup>(2)</sup>	-0.5	4.6	
VI	Input voltage range	I/O ports <sup>(2)(3)</sup>	-0.5	V <sub>CC</sub> + 0.5	V
Vo	Output voltage range <sup>(2)(3)</sup>	I	-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>1</sub> < 0		-50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		-50	mA
I <sub>O</sub>	Continuous output current			±50	mA
	Continuous current through each V <sub>CC</sub> or GN	ND		±100	mA
0	Declares the surrel impredence $(4)$	DGG package		64	°C/W
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>	DL package		56	
T <sub>stg</sub>	Storage temperature range		-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

(3) This value is limited to 4.6 V maximum.

(4) The package thermal impedance is calculated in accordance with JESD 51-7.

### **RECOMMENDED OPERATING CONDITIONS**<sup>(1)</sup>

			MIN	MAX	UNIT	
V <sub>CC</sub>	Supply voltage		1.65	3.6	V	
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$				
VIH	High-level input voltage	$V_{CC}$ = 2.3 V to 2.7 V	1.7		V	
		$V_{CC}$ = 2.7 V to 3.6 V	2			
		V <sub>CC</sub> = 1.65 V to 1.95 V		$0.35  imes V_{CC}$		
VIL	Low-level input voltage	$V_{CC}$ = 2.3 V to 2.7 V		0.7	V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8		
VI	Input voltage		0	V <sub>CC</sub>	V	
Vo	Output voltage		0	V <sub>CC</sub>	V	
		V <sub>CC</sub> = 1.65 V		-4	mA	
		V <sub>CC</sub> = 2.3 V		-12		
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2.7 V		-12		
		$V_{CC} = 3 V$		-24		
		V <sub>CC</sub> = 1.65 V		4		
		V <sub>CC</sub> = 2.3 V		12 12		
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2.7 V				
		$V_{CC} = 3 V$	24			
$\Delta t/\Delta v$	Input transition rise or fall rate			10	ns/V	
T <sub>A</sub>	Operating free-air temperature		-40	85	°C	

(1) All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



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### **ELECTRICAL CHARACTERISTICS**

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>cc</sub>	MIN	TYP <sup>(1)</sup> MAX	UNIT
	I <sub>OH</sub> = -100 μA	1.65 V to 3.6 V	V <sub>CC</sub> - 0.2		
	I <sub>OH</sub> = -4 mA	1.65 V	1.2		
	I <sub>OH</sub> = -6 mA	2.3 V	2		
V <sub>OH</sub>		2.3 V	1.7		V
	I <sub>OH</sub> = -12 mA	2.7 V	2.2		
		3 V	2.4		
	I <sub>OH</sub> = -24 mA	1.65 V 1.2   2.3 V 2   2.3 V 1.7   2.7 V 2.2			
	I <sub>OL</sub> = 100 μA	1.65 V to 3.6 V		0.2	
	I <sub>OL</sub> = 4 mA	1.65 V		0.45	
V <sub>OL</sub>	I <sub>OL</sub> = 6 mA	2.3 V		0.4	V
	1 12	2.3 V		0.7	v
	$I_{OL} = 12 \text{ mA}$	2.7 V		0.4	
	I <sub>OL</sub> = 24 mA	3 V 0.5	0.55		
1	$V_{I} = V_{CC} \text{ or } GND$	3.6 V		±5	μA
	V <sub>I</sub> = 0.58 V	1.65 V	25		
	V <sub>I</sub> = 1.07 V	1.65 V	-25		
	V <sub>I</sub> = 0.7 V	2.3 V	45		
l(hold)	V <sub>I</sub> = 1.7 V	2.3 V	-45		μA
	V <sub>I</sub> = 0.8 V	3 V	75		
	V <sub>1</sub> = 2 V	3 V	-75		
	$V_{I} = 0$ to 3.6 V <sup>(2)</sup>	3.6 V		±500	
OZ <sup>(3)</sup>	$V_{O} = V_{CC} \text{ or } GND$	3.6 V		±10	μA
cc	$V_{I} = V_{CC} \text{ or } GND, \qquad I_{O} = 0$	3.6 V		40	μA
۵l <sub>CC</sub>	One input at $V_{CC}$ - 0.6 V, Other inputs at $V_{CC}$ or GND	3 V to 3.6 V		750	μA
C <sub>i</sub> Control inputs	$V_{I} = V_{CC}$ or GND	3.3 V		3.5	pF
C <sub>io</sub> A or B ports	$V_{O} = V_{CC}$ or GND	3.3 V		9	pF

(1) All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ . (2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

(3) For I/O ports, the parameter  $I_{\mbox{\scriptsize OZ}}$  includes the input leakage current.

### TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 through Figure 3)

			V <sub>CC</sub> = 2 ± 0.2		V <sub>CC</sub> =	2.7 V	V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT	
			MIN	MAX	MIN	MAX	MIN	MAX		
f <sub>clock</sub>	Clock frequency			130		130		130	MHz	
t <sub>w</sub>	Pulse duration, CLK high or lo	W	3.3		3.3		3.3		ns	
		A before CLK1	2.6		2.1		1.7			
t <sub>su</sub>	Setup time	B before LE	1.7		1.5		1.3		ns	
		CLKEN before CLK <sup>↑</sup>	1.6		1.3		1			
		A after CLK↑	0.6		0.6		0.7			
t <sub>h</sub>	Hold time	B after LE	0.9		0.9		1.1		ns	
		CLKEN after CLK <sup>↑</sup>	1		0.9		0.9			

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### SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 through Figure 3)

PARAMETER	FROM			$V_{CC}$ = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT	
	(INPUT)	(001201)	TYP	MIN	MAX	MIN	MAX	MIN	MAX		
f <sub>max</sub>				130		130		130		MHz	
	CLK	В	8	1	6.2		5	1	4.3		
	В		7	1	5.3		4.7	1.4	4	20	
t <sub>pd</sub>	LE	А	7	1	6		5.9	1.4	4.8	ns	
	SEL		7	1.1	6.4		6.2	1.3	5.2		
t <sub>en</sub>	OEB or OEA	B or A	8	1	6		6.1	1	5.1	ns	
t <sub>dis</sub>	OEB or OEA	B or A	7	1.4	5.4		4.6	1.7	4.2	ns	

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### **OPERATING CHARACTERISTICS**

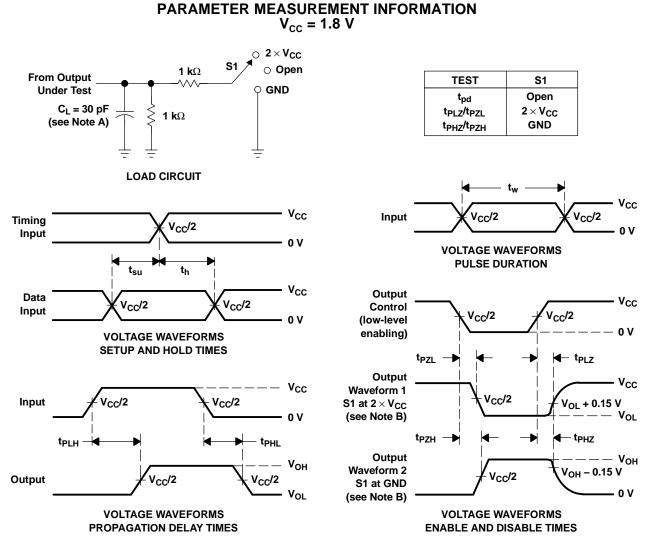
 $T_A = 25^{\circ}C$ 

	~								
		PARAMETER	TESTO	ONDITIONS	$V_{CC}$ = 2.5 V	$V_{CC}$ = 3.3 V	UNIT		
					1231 0	ONDITIONS	TYP	TYP	UNIT
		A to B	Outputs enabled			92	105		
	~	Dower dissinction conseitones	AIUB	Outputs disabled	0 0	( 10 MU-	61	76	~ <b>F</b>
	C <sub>pd</sub> Power dissipation capacitance	D to A	Outputs enabled	$C_L = 0,$	f = 10  MHz	39	43	pF	
			B to A	Outputs disabled			11	13	

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## SN74ALVCH16271 12-BIT TO 24-BIT MULTIPLEXED BUS EXCHANGER WITH 3-STATE OUTPUTS

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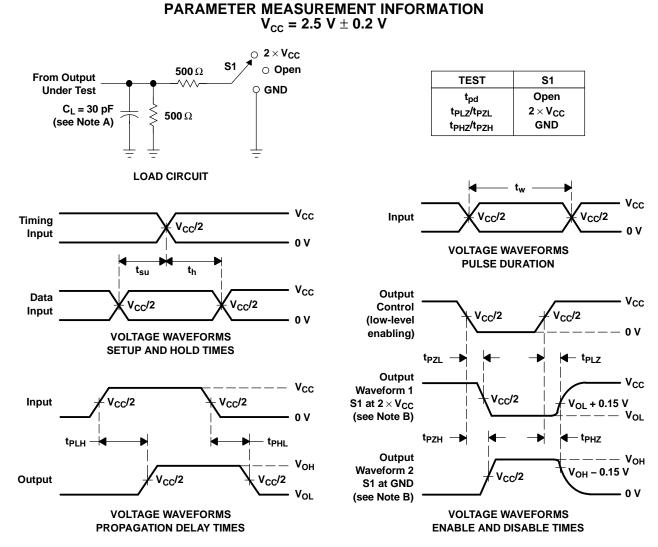
#### NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ , t<sub>r</sub>  $\leq$  2 ns, t<sub>f</sub>  $\leq$  2 ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.
- F. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
- G. t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>pd</sub>.

#### Figure 1. Load Circuit and Voltage Waveforms



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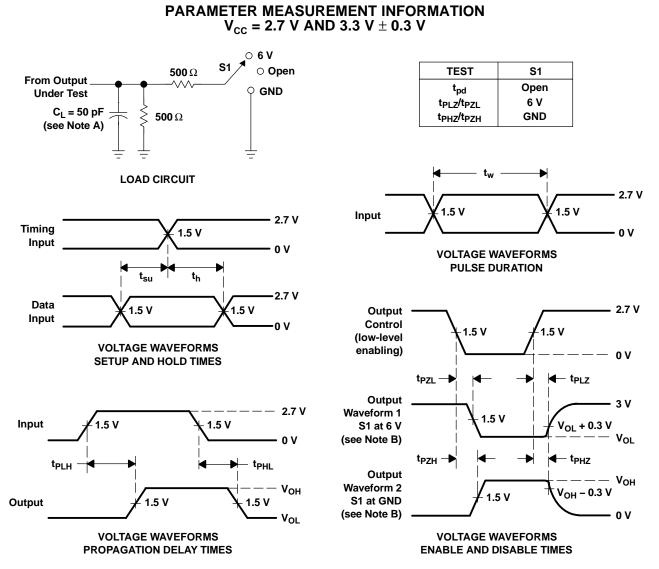


- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ , t<sub>f</sub>  $\leq$  2 ns, t<sub>f</sub>  $\leq$  2 ns.
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E. t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.
  - F. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
  - G. t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>pd</sub>.

#### Figure 2. Load Circuit and Voltage Waveforms



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NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ , t<sub>r</sub>  $\leq$  2.5 ns, t<sub>f</sub>  $\leq$  2.5 ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E.  $t_{\text{PLZ}} \, \text{and} \, t_{\text{PHZ}} \, \text{are the same as} \, t_{\text{dis}}.$

F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .

G.  $t_{\mathsf{PLH}}$  and  $t_{\mathsf{PHL}}$  are the same as  $t_{\mathsf{pd}}.$ 

#### Figure 3. Load Circuit and Voltage Waveforms



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### PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
74ALVCH16271DGGRE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74ALVCH16271DGGRG4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALVCH16271DGGR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between

the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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# PACKAGE MATERIALS INFORMATION

Pin1

Quadrant

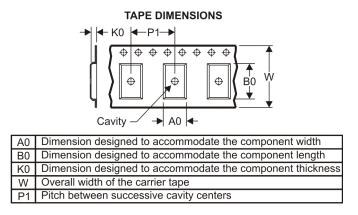
Q1

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### **TAPE AND REEL INFORMATION**





### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal											
Device		Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)
SN74ALVCH16271DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0

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# PACKAGE MATERIALS INFORMATION

29-Jul-2009



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALVCH16271DGGR	TSSOP	DGG	56	2000	346.0	346.0	41.0

# **MECHANICAL DATA**

MTSS003D - JANUARY 1995 - REVISED JANUARY 1998

#### DGG (R-PDSO-G\*\*)

### PLASTIC SMALL-OUTLINE PACKAGE

**48 PINS SHOWN** 



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153



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