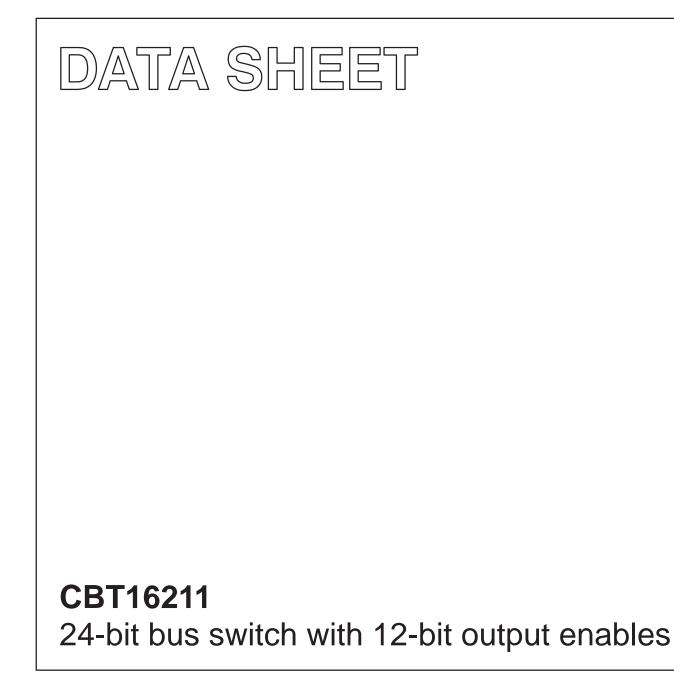
INTEGRATED CIRCUITS



Product data

2001 Jun 13



CBT16211

FEATURES

- 5 Ω switch connection between two ports
- TTL compatible control input levels
- Package options include plastic shrink small outline (SSOP), thin shrink small outline (TSSOP)
- ESD protection exceeds 1000 V CDM per JESD22-C101
- Latch-up testing is done to JESDEC Standard JESD78 which exceeds 100 mA

DESCRIPTION

The CBT16211 provides 24 bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as a dual 12-bit bus switch with separate output-enable (\overline{OE}) inputs. It can be used as two 12-bit bus switches or as one 24-bit bus switch. When \overline{OE} is low, the associated 12-bit bus switch is on, and port A is connected to port B. When \overline{OE} is high, the switch is open, and a high-impedance state exists between the ports.

The CBT16211 is characterized for operation from -40 to 85 °C.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T _{amb} = 25 °C; GND = 0 V	TYPICAL	UNIT
t _{PLH} t _{PHL}	Propagation delay An to Yn	C _L = 50 pF; V _{CC} = 5 V	0.25	ns
C _{IN}	Input capacitance	$V_I = 0 V \text{ or } V_{CC}$	4.3	pF
C _{OUT}	Output capacitance	Outputs disabled; $V_O = 0 V \text{ or } V_{CC}$	6.9	pF
I _{CC}	Total supply current	Outputs disabled; $V_{CC} = 5.5 V$	3.0	μA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DWG NUMBER
56-Pin Plastic SSOP Type III	–40 to 85 °C	CBT16211DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40 to 85 °C	CBT16211DGG	SOT364-1

FUNCTION TABLE

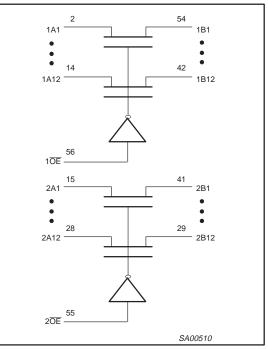
INP	UTS	OUTPUTS		
1 0E	2 <mark>0E</mark>	1A, 1B	2A, 2B	
L	L	1A = 1B	2A = 2B	
L	н	1A = 1B	Z	
н	L	Z	2A = 2B	
н	н	z	Z	

H = High voltage level

L = Low voltage level

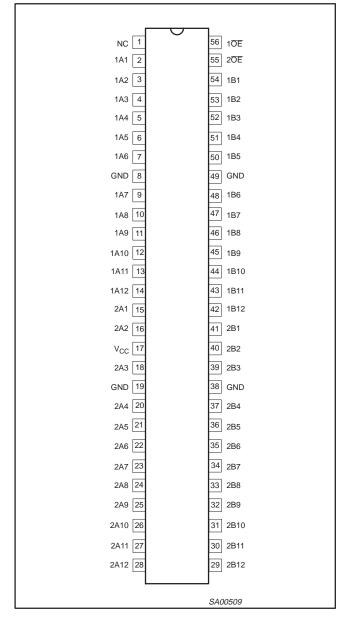
Z = High impedance "off" state

LOGIC SYMBOL



CBT16211

PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	NC	No internal connection
56, 55	1 <u>0E,</u> 2 <u>0E</u>	Output Enables
2, 3, 4, 5, 6, 7, 9, 10, 11, 12, 13, 14	1A1-1A12	Inputs
54, 53, 52, 51, 50, 48, 47, 46, 45, 44, 43, 42	1B1-1B12	Outputs
15, 16, 18, 20, 21, 22, 23, 24, 25, 26, 27, 28	2A1-2A12	Inputs
41, 40, 39, 37, 36, 35, 34, 33, 32, 31, 30, 29	2B1-2B12	Outputs
8, 19, 38, 49	GND	Ground (0 V)
17	V _{CC}	Positive supply voltage

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Product data

ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		-0.5 to +7.0	V
I _{IK}	DC input diode current	V ₁ < 0	-50	mA
VI	DC input voltage ³		-0.5 to +7.0	V
V _{OUT}	DC output voltage ³	output in Off or High state	–0.5 to +5.5	V
I _{OUT}	DC output current	output in Low state	128	mA
T _{stg}	Storage temperature range		-65 to 150	°C

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction 2. temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C. The input and output voltage ratings may be exceeded if the input and output current ratings are observed. 3.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIM	UNIT	
STMBOL	PARAMETER	Min	Max	UNIT
V _{CC}	DC supply voltage	4.5	5.5	V
V _{IH}	High-level input voltage	2.0	—	V
VIL	Low-level Input voltage	—	0.8	V
T _{amb}	Operating free-air temperature range	-40	+85	°C

LIMITS SYMBOL **TEST CONDITIONS** T_{amb} = -40 to +85 °C UNIT PARAMETER Min Typ¹ Max Input clamp voltage $V_{CC} = 4.5 \text{ V}; I_{I} = -18 \text{ mA}$ -1.2 V Vik $V_{IN} = V_{CC} = 5.0 \text{ V}; I_{OUT} = -100 \text{ }\mu\text{A}$ V VP Output high pass voltage 3.4 3.9 3.6 $V_{CC} = 0 V; V_{I} = 5.5 V$ _ ____ 10 Input leakage current μΑ Ιį. V_{CC} = 5.5 V; V_I = GND or 5.5 V ±1 ICC Quiescent supply current $V_{CC} = 5.5 \text{ V}; I_O = 0, V_I = V_{CC} \text{ or GND}$ ____ _ 3 μA V_{CC} = 5.5 V, one input at 3.4 V, Additional supply current per 2.5 mΑ ΔI_{CC} input pin² other inputs at V_{CC} or GND CI Control pins $V_{I} = 3 V \text{ or } 0$ 4.5 ____ pF _ Port OFF capacitance $V_{O} = 3 V \text{ or } 0, \overline{OE} = V_{CC}$ 6.9 pF CI(OFF) $V_{CC} = 4.0 \text{ V}; \text{ V}_1 = 2.4 \text{ V}; \text{ I}_1 = 15 \text{ mA}$ 14 20 ____ $V_{CC} = 4.5 \text{ V}; V_1 = 0 \text{ V}; I_1 = 64 \text{ mA}$ 5 7 r_{on}3 Ω V_{CC} = 4.5 V; V₁ = 0 V; I_I = 30 mA 5 7 _ V_{CC} = 4.5 V; V₁ = 2.4 V; I_I = -15 mA 8 12

DC ELECTRICAL CHARACTERISTICS

NOTES:

1. All typical values are at V_{CC} = 5 V, T_{amb} = 25 °C.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND. 2.

Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. 3.

On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

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AC CHARACTERISTICS

GND = 0 V; t_{R;} C_L = 50 pF

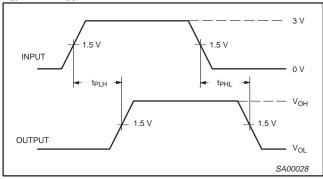
SYMBOL	DADAMETED	FROM (INPUT)	то	V_{CC} = 5.0 V ± 0.5 V		
	PARAMETER		(INPUT) (OUTPUT)	Min	Мах	UNIT
t _{pd}	Propagation delay ¹	A or B	B or A	—	0.25	ns
t _{en}	Output enable time to High and Low level	ŌĒ	A or B	1.5	6.0	ns
t _{dis}	Output disable time from High and Low level	ŌE	A or B	1.5	6.0	ns

NOTE:

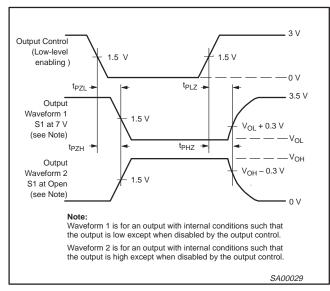
1. This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).

AC WAVEFORMS

 V_{M} = 1.5 V, V_{IN} = GND to 3.0 V.

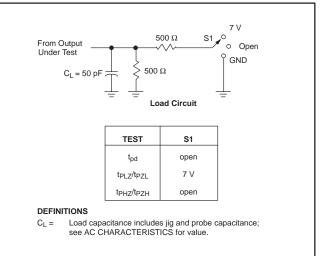




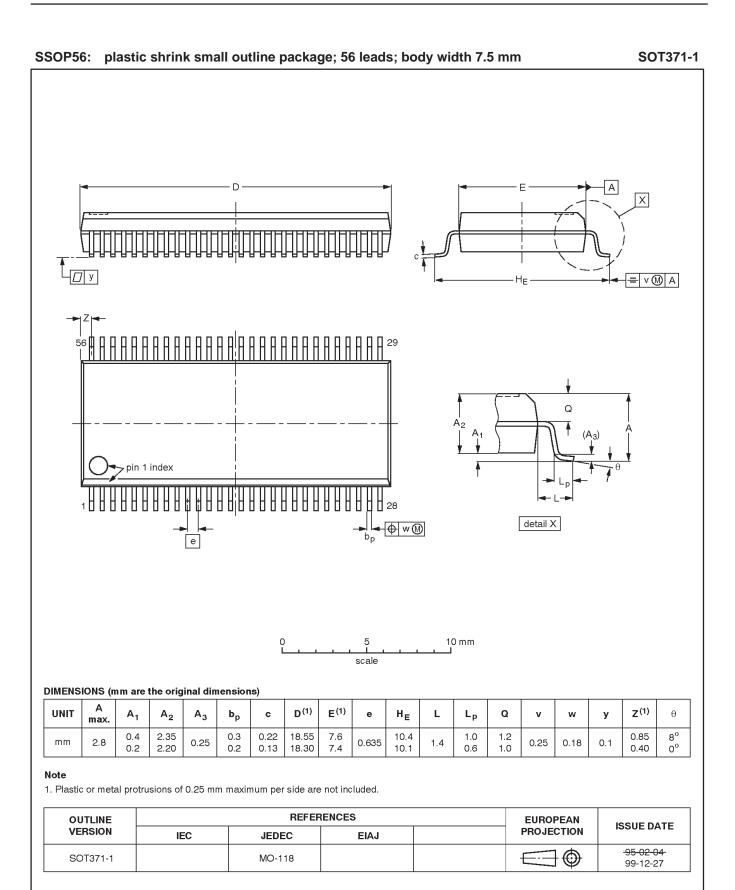


Waveform 2. 3-State Output Enable and Disable Times

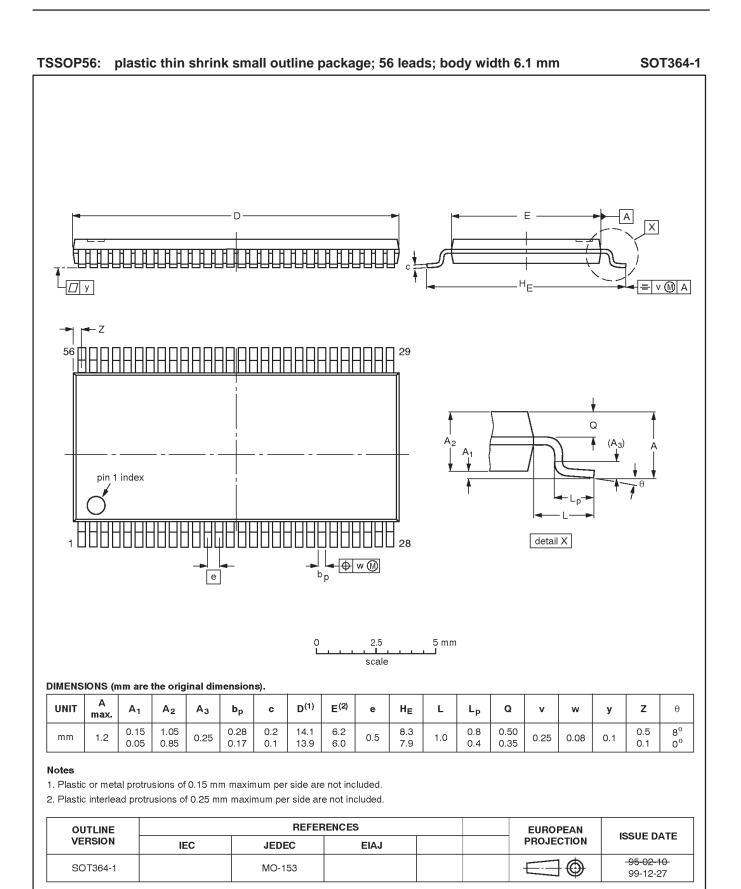
TEST CIRCUIT AND WAVEFORMS



SA00012



CBT16211



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Data sheet status

Data sheet status ^[1]	Product status ^[2]	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

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Date of release: 06-01

Document order number:

9397 750 08481

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