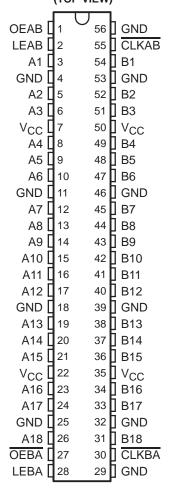
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- Members of the Texas Instruments
 Widebus™ Family
- UBT [™] Transceivers Combine D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce)
 <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- I_{off} and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

description/ordering information

The 'LVTH16500 devices are 18-bit universal bus transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

SN54LVTH16500 . . . WD PACKAGE SN74LVTH16500 . . . DGG OR DL PACKAGE (TOP VIEW)



ORDERING INFORMATION

T _A PACKAGE		t	ORDERABLE PART NUMBER	TOP-SIDE MARKING
SSOP - DL		Tube	SN74LVTH16500DL	1)/TU40500
	550P - DL	Tape and reel	SN74LVTH16500DLR	LVTH16500
-40°C to 85°C	TSSOP - DGG	Tape and reel	SN74LVTH16500DGGR	LVTH16500
	VFBGA – GQL	Town and made	SN74LVTH16500GQLR	11500
	VFBGA – ZQL (Pb-free)	Tape and reel	SN74LVTH16500ZQLR	LL500
-55°C to 125°C CFP – WD		Tube	SNJ54LVTH16500WD	SNJ54LVTH16500WD

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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SCBS701F - JULY 1997 - REVISED SEPTEMBER 2003

description/ordering information (continued)

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the devices operate in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A data is stored in the latch/flip-flop on the high-to-low transition of CLKAB. OEAB is active high. When OEAB is high, the B-port outputs are active. When OEAB is low, the B-port outputs are in the high-impedance state.

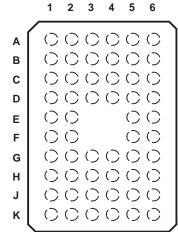
Data flow for B to A is similar to that of A to B, but uses OEBA, LEBA, and CLKBA. The output enables are complementary (OEAB is active high and OEBA is active low).

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When V_{CC} is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor and OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

GQL OR ZQL PACKAGE (TOP VIEW)



terminal assignments

	1	2	3	4	5	6
Α	A1	LEAB	OEAB	GND	CLKAB	B1
В	А3	A2	GND	GND	B2	В3
С	A5	A4	Vcc	Vcc	B4	B5
D	A7	A6	GND	GND	B6	В7
Е	A9	A8			B8	B9
F	A10	A11			B11	B10
G	A12	A13	GND	GND	B13	B12
Н	A14	A15	Vcc	Vcc	B15	B14
J	A16	A17	GND	GND	B17	B16
K	A18	OEBA	LEBA	GND	CLKBA	B18

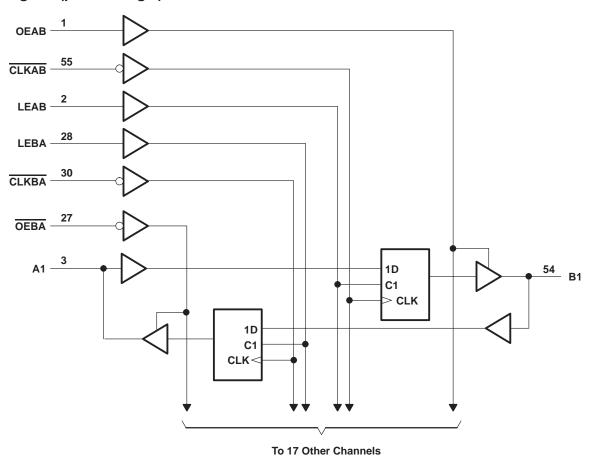
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FUNCTION TABLE†

	INPUTS								
OEAB	LEAB	CLKAB	Α	В					
L	Χ	Χ	Χ	Z					
Н	Н	Χ	L	L					
Н	Н	Χ	Н	Н					
Н	L	\downarrow	L	L					
Н	L	\downarrow	Н	Н					
Н	L	Н	Χ	B ₀ ‡					
Н	L	L	Χ	В ₀ §					

[†] A-to-B data flow is shown: B-to-A flow is similar, but uses OEBA, LEBA, and CLKBA.

logic diagram (positive logic)



Pin numbers shown are for the DGG, DL, and WD packages.



[‡] Output level before the indicated steady-state input conditions were established

[§] Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low

SCBS701F - JULY 1997 - REVISED SEPTEMBER 2003

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	\dots -0.5 V to 7 V
Voltage range applied to any output in the high-impedance	
or power-off state, V _O (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state, V _O (see Note 1)0.5	
Current into any output in the low state, IO: SN54LVTH16500	96 mA
SN74LVTH16500	128 mA
Current into any output in the high state, I _O (see Note 2): SN54LVTH16500	
SN74LVTH16500	64 mA
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I _{OK} (V _O < 0)	
Package thermal impedance, θ _{JA} (see Note 3): DGG package	
DL package	56°C/W
GQL/ZQL package	
Storage temperature range, T _{stg}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
- 3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

			SN54LVT	H16500	SN74LVT	H16500	
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	2.7	3.6	V
VIH	High-level input voltage		2	Ź.	2		V
V _{IL}	Low-level input voltage			0.8		8.0	V
VI	Input voltage		4	5.5		5.5	V
Іон	High-level output current		7	-24		-32	mA
loL	Low-level output current		3	48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	0	10		10	ns/V
Δt/ΔVCC	Power-up ramp rate		200		200	·	μs/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

SCBS701F - JULY 1997 - REVISED SEPTEMBER 2003

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

				SN5	4LVTH1	6500	SN7	4LVTH16	500	
PAF	RAMETER	TEST CO	ONDITIONS	MIN	TYP	MAX	MIN	TYP [†]	MAX	UNIT
VIK		$V_{CC} = 2.7 \text{ V},$	$I_{\parallel} = -18 \text{ mA}$			-1.2			-1.2	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V},$	$I_{OH} = -100 \mu A$	V _{CC} -0	.2		V _{CC} -0	.2		
.,		$V_{CC} = 2.7 \text{ V},$	$I_{OH} = -8 \text{ mA}$	2.4			2.4			.,,
VOH		V 2V	I _{OH} = -24 mA	2						V
		V _{CC} = 3 V	$I_{OH} = -32 \text{ mA}$				2			
		V 07V	I _{OL} = 100 μA			0.2			0.2	
		V _{CC} = 2.7 V	I _{OL} = 24 mA			0.5			0.5	
V			I _{OL} = 16 mA			0.4			0.4	
VOL			I _{OL} = 32 mA			0.5			0.5	V
		VCC = 3 V	I _{OL} = 48 mA			0.55				
			I _{OL} = 64 mA						0.55	
	O and the Library to	V _{CC} = 3.6 V,	$V_I = V_{CC}$ or GND			±1			±1	
	Control inputs	$V_{CC} = 0 \text{ or } 3.6 \text{ V},$	V _I = 5.5 V			10			10	
Ц			V _I = 5.5 V		20			20		
	A or B ports ‡ $V_{CC} = 3.6 \text{ V}$		$V_I = V_{CC}$		2	1			1	
			V _I = 0		20,	-5			-5	
l _{off}		$V_{CC} = 0$,	V_I or $V_O = 0$ to 4.5 V		9				±100	μΑ
			V _I = 0.8 V	75	7		75			
l _l (hold)	A or B ports	VCC = 3 V	V _I = 2 V	-75			-75			μΑ
, ,		V _{CC} = 3.6 V§,	$V_{I} = 0 \text{ to } 3.6 \text{ V}$						±500	
IOZPU		$\frac{V_{CC}}{OE/OE} = 0$ to 1.5 V, $V_{O} = 0$	0.5 V to 3 V,			±100*			±100	μΑ
lozpd		$\frac{\text{V}_{\text{C}}\text{C}}{\text{OE}/\text{OE}} = 1.5 \text{ V to 0, V}_{\text{O}} = \frac{\text{OE}/\text{OE}}{\text{OE}} = \frac{\text{OE}/\text{OE}}{$	0.5 V to 3 V,			±100*			±100	μΑ
		V _{CC} = 3.6 V,	Outputs high			0.19			0.19	
Icc		$I_{O} = 0$,	Outputs low			5			5	mA
		$V_I = V_{CC}$ or GND	Outputs disabled			0.19			0.19	
ΔI _{CC} ¶		$V_{CC} = 3 \text{ V to } 3.6 \text{ V, One}$ Other inputs at V_{CC} or 0				0.2			0.2	mA
Ci		V _I = 3 V or 0			4			4		pF
C _{io}		$V_O = 3 V \text{ or } 0$			10			10		pF
		-		-			-			

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.



[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ Unused pins at V_{CC} or GND

[§] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

[¶] This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

SCBS701F - JULY 1997 - REVISED SEPTEMBER 2003

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

					SN54LV	ГН16500		8	N74LV	ГН16500		
					$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V} $ $V_{CC} = 2.7 \text{ V}$		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT	
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency				150		150		150		150	MHz
	Dulas dunation	LE high		3.3		3.3		3.3		3.3		
t _W	Pulse duration	CLK high or low		3.3		3.3		3.3		3.3		ns
		A before CLKAB↓		3.1		3.1		2.9		2.9		
		B before CLKBA↓		3.1	1	3.1		2.9		2.9		
tsu	Setup time	A D b - (1 E l	CLK high	1.5	2	0.6		1.4		0.5		ns
		A or B before LE↓	CLK low	3.1	000	2.5		2.9		2.3		
	Hald Care	A or B after CLK↓		0.4	Q	0.4		0.4		0.4		
th	Hold time	A or B after LE↓		1.7		1.7		1.6		1.6		ns

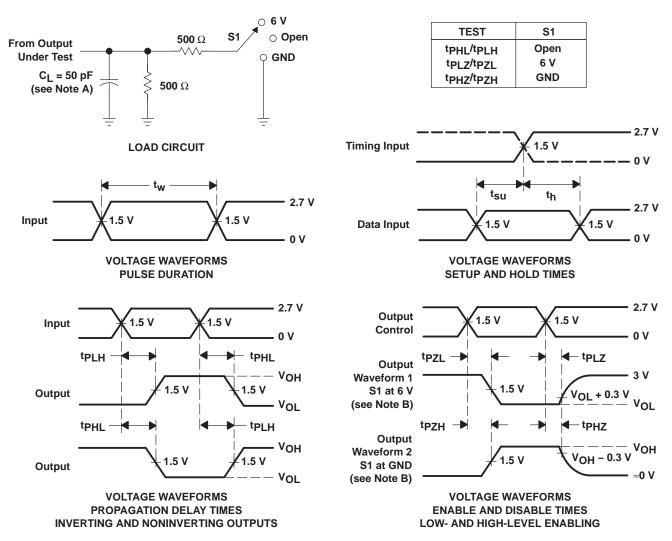
switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

				SN54LV	TH16500			SN74	LVTH16	5500		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	MIN	TYP [†]	MAX	MIN	MAX	
f _{max}			150		150		150			150		MHz
t _{PLH}	B or A	A == D	1.2	3.9		4.1	1.3	2.8	3.7		4	
t _{PHL}	BOLA	A or B	1.2	3.9	2	4.1	1.3	2.6	3.7		4	ns
^t PLH	LEBA or LEAB	A D	1.4	5.5	N.	5.9	1.5	3.8	5.1		5.7	
^t PHL	LEDA OI LEAD	A or B	1.4	5.5	34	5.9	1.5	3.8	5.1		5.7	ns
^t PLH	CLKBA or	۸ ۵	1.2	5.3		6.1	1.3	3.6	5		5.9	
^t PHL	CLKAB	A or B	1.2	5.3		6.1	1.3	3.5	5		5.9	ns
^t PZH	OFDA OFAD	A or D	1.2	5.1		5.8	1.3	3.6	4.8		5.5	50
tPZL	OEBA or OEAB	A or B	1.2	5.1		5.8	1.3	3.6	4.8		5.5	ns
^t PHZ	OEBA or OEAB	A or B	1.6	6.1		6.6	1.7	4.5	5.8		6.3	ns
tPLZ	OLDA UI OLAB	AUB	1.6	6.1		6.6	1.7	4.1	5.8		6.3	115

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

SCBS701F - JULY 1997 - REVISED SEPTEMBER 2003

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \,\Omega$, $t_f \leq 2.5 \,\text{ns}$.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms





4-May-2012

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
74LVTH16500DGGRE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74LVTH16500DGGRG4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVTH16500DGGR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVTH16500DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVTH16500DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVTH16500GQLR	LIFEBUY	BGA MICROSTAR JUNIOR	GQL	56	1000	TBD	SNPB	Level-1-240C-UNLIM	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE OPTION ADDENDUM

4-May-2012

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OTHER QUALIFIED VERSIONS OF SN74LVTH16500:

● Enhanced Product: SN74LVTH16500-EP

NOTE: Qualified Version Definitions:

www.ti.com

• Enhanced Product - Supports Defense, Aerospace and Medical Applications

PACKAGE MATERIALS INFORMATION

www.ti.com 23-Jul-2011

TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVTH16500DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
SN74LVTH16500GQLR	BGA MI CROSTA R JUNI OR	GQL	56	1000	330.0	16.4	4.8	7.3	1.45	8.0	16.0	Q1

PACKAGE MATERIALS INFORMATION

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVTH16500DGGR	TSSOP	DGG	56	2000	346.0	346.0	41.0
SN74LVTH16500GQLR	BGA MICROSTAR JUNIOR	GQL	56	1000	333.2	345.9	28.6

GQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-285 variation BA-2.
- D. This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.



DL (R-PDSO-G**)

48 PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MO-118

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

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