WM9090

Ultra Low Power Audio Subsystem

DESCRIPTION

The WM9090[1] is a high performance low power audio subsystem with integrated headphone driver and Class D speaker driver. The speaker driver supports 750mW output power at 3.7V, 1%THD.

The unique dual mode charge pump architecture provides ground referenced headphone outputs, removing the requirement for external coupling capacitors. Class G technology is integrated to increase the efficiency and extend playback time by optimizing the headphone driver supply voltages according to the volume control.

The flexible input configuration allows single ended or differential stereo inputs. Mixers allow highly flexible routing to the outputs.

Separate mixer and volume controls are provided for each headphone and speaker driver. Automatic Gain Control limits the speaker output signal in order to prevent clipping. DC offset correction to less than 1mV guarantees a pop/click-free headphone start up.

WM9090 is controlled using a two-wire I2C interface. An integrated oscillator generates all internal clocks, removing the need to provide any external clock.

WM9090 is available in a 2.53mm x 2.07mm 20-bump CSP package.

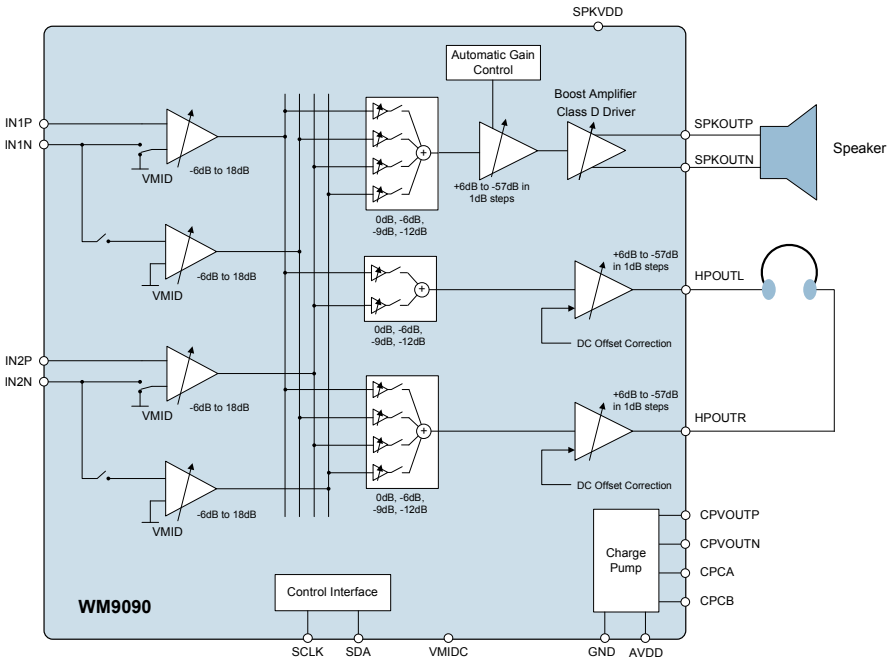
FEATURES

- Mono Class D speaker driver
  - 750mW at 3.7V SPKVDD @ 1% THD+N
  - 950mW at 4.2V SPKVDD @ 1% THD+N
  - 90dB SNR
- Ground referenced stereo headphone driver
  - 35mW into 16Ω load @ 1% THD+N
  - 95dB SNR
  - 80dB THD+N
- Differential and single ended analogue input configurations
- Integrated oscillator for clocking requirements
- I^2C 2-wire software control interface
- Automatic gain control (AGC) for speaker output
- SilentSwitch™ Pop and click suppression
  - < 1mV DC offset
- <50ms start up time
- Excellent RF and TDMA noise immunity
- Ultra low power consumption
  - 4mW quiescent for headphone driver
  - 5mW quiescent for speaker driver
- Shutdown current < 2uA
- Supply voltage
  - SPKVDD = 2.7V to 5.5V
  - AVDD = 1.8V
- 1.8V to 2.7V control interface compatibility
- 20-bump CSP package

APPLICATIONS

- Mobile handsets

BLOCK DIAGRAM



[1] This product is protected by US Patents 7,622,984 and 7,626,445

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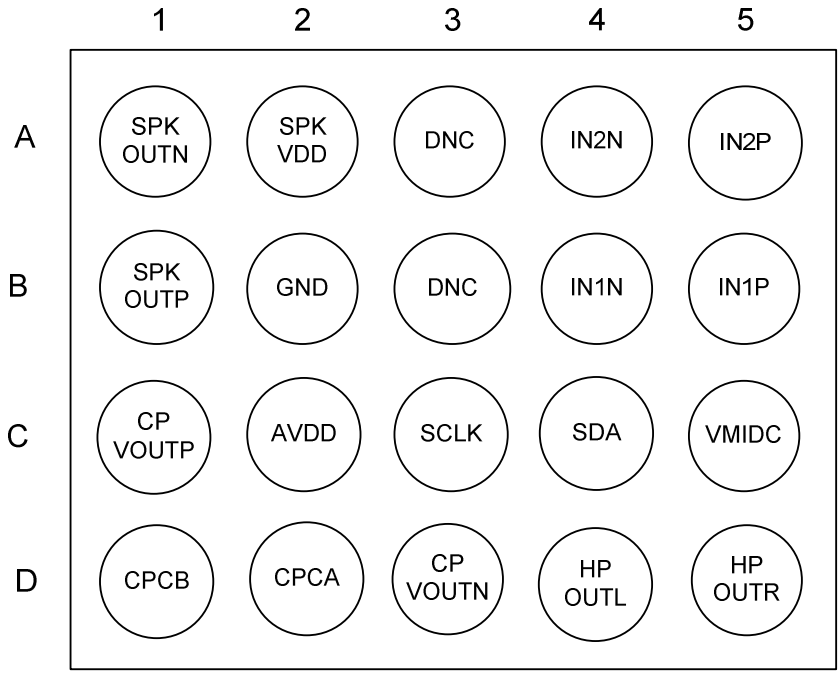
PIN CONFIGURATION

20-bump CSP package; Top View



ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM9090ECS/R	-40°C to +85°C	20-ball W-CSP (Pb-free, Tape and reel)	MSL1	260°C

Note:

Reel quantity = 3500

PIN DESCRIPTION

PIN NO	NAME	TYPE	DESCRIPTION
A1	SPKOUTN	Analogue Output	Speaker negative output
A2	SPKVDD	Supply	Speaker supply
A3	DNC	n/a	Do Not Connect
A4	IN2P	Analogue Input	IN2 positive analogue input
A5	IN2N	Analogue Input	IN2 negative analogue input
B1	SPKOUTP	Analogue Output	Speaker positive output
B2	GND	Supply	Ground for speaker and charge pump
B3	DNC	n/a	Do Not Connect
B4	IN1N	Analogue Input	IN1 negative analogue input
B5	IN1P	Analogue Input	IN1 positive analogue input
C1	CPVOUTP	Analogue Output	Charge pump positive rail decoupling pin
C2	AVDD	Supply	Analogue supply
C3	SCLK	Digital Input	Control interface clock
C4	SDA	Digital Input / Output	Control interface data
C5	VMIDC	Analogue Output	Mid-rail voltage decoupling pin
D1	CPCB	Analogue Output	Charge pump flyback capacitor pin
D2	CPCA	Analogue Output	Charge pump flyback capacitor pin
D3	CPVOUTN	Analogue Output	Charge pump negative rail decoupling pin
D4	HPOUTL	Analogue Output	Left headphone output
D5	HPOUTR	Analogue Output	Right headphone output

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Supply voltages (AVDD)	-0.3V	+2.5V
Supply voltages (SPKVDD)	-0.3V	+7.0V
Voltage range digital inputs (SCLK, SDA)	GND -0.3V	+3.3V
Voltage range analogue inputs	GND -0.3V	+3.3V
Operating temperature range, T_A	-40ºC	+85ºC
Junction temperature, T_{JMAX}	-40ºC	+150ºC
Storage temperature after soldering	-65ºC	+150ºC

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Charge Pump supply range	AVDD	1.71	1.8	2.0	V
Speaker supply range	SPKVDD	2.7	3.6	5.5	V
Ground	GND		0		V

THERMAL PERFORMANCE

Thermal analysis should be performed in the intended application to prevent the WM9090 from exceeding maximum junction temperature. Several contributing factors affect thermal performance most notably the physical properties of the mechanical enclosure, location of the device on the PCB in relation to surrounding components and the number of PCB layers. Connecting the GND balls through thermal vias and into a large ground plane will aid heat extraction.

Three main heat transfer paths exist to surrounding air as illustrated below in Figure 1:

- Package top to air (radiation).
- Package bottom to PCB (radiation).
- Package balls to PCB (conduction).

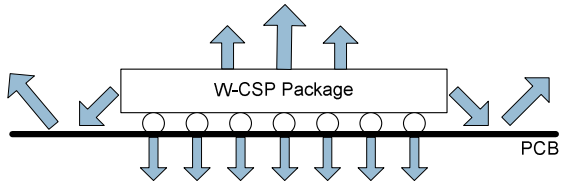


Figure 1 Heat Transfer Paths

The temperature rise T_R is given by $T_R = P_D * \Theta_{JA}$

- P_D is the power dissipated in the device.
- Θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature and is therefore a measure of heat transfer from the die to surrounding air. Θ_{JA} is determined with reference to JEDEC standard JESD51-9.

The junction temperature T_J is given by $T_J = T_A + T_R$, where T_A is the ambient temperature.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Operating temperature range	T_A	-40		85	°C
Operating junction temperature	T_J	-40		125	°C
Thermal Resistance	Θ_{JA}		TBD		°C/W

Note:

1. Junction temperature is a function of ambient temperature and of the device operating conditions. The ambient temperature limits and junction temperature limits must both be observed.

ELECTRICAL CHARACTERISTICS

Test Conditions

SPKVDD = 3.6V, AVDD=1.8V, GND=0V, T_A = +25°C, 1kHz signal, PGA gain = 0dB unless otherwise stated

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Input Pins					
Maximum Full-Scale input signal level - IN1P/N and IN2P/N	Single-ended input			1.0	Vrms
	Differential input			1.0	
Input Resistance	Differential or Single- Ended Mode		8.5		kΩ
Input Capacitance	All analogue input pins		TBD		pF
Input Programmable Gain Amplifiers (PGAs) IN1A, IN1B, IN2A and IN2B					
Minimum Programmable Gain			-6		dB
Maximum Programmable Gain			+18		dB
Mute Attenuation			TBD		dB
Common Mode Rejection Ratio	Differential Mode (217Hz input)		TBD		dB
Output Programmable Gain Amplifiers (PGAs) SPKVOL, HPOUT1LVOL and HPOUT1RVOL					
Minimum Programmable Gain			-57		dB
Maximum Programmable Gain			+6		dB
Programmable Gain Step Size			1		dB
Mute Attenuation			TBD		dB
Speaker Output Programmable Gain SPKOUTLBOOST					
Programmable Gain	SPKOUTLBOOST=111		12		dB
	SPKOUTLBOOST=110		9		
	SPKOUTLBOOST=101		7.5		
	SPKOUTLBOOST=100		6		
	SPKOUTLBOOST=011		4.5		
	SPKOUTLBOOST=010		3		
	SPKOUTLBOOST=001		1.5		
	SPKOUTLBOOST=000		0		
Headphone Driver Audio Performance (R_L = 16Ω)					
SNR (A-weighted)	Path from IN1P/N or IN2P/N		95		dB
THD (P_O=20mW)			-82		dB
THD+N (P_O=20mW)			-80		dB
THD (P_O=5mW)			-83		dB
THD+N (P_O=5mW)			-81		dB
Crosstalk (L/R)			TBD		dB
PSRR	AVDD with 100mVpk-pk at 217Hz, differential input		80		dB
	SPKVDD with 100mVpk-pk at 217Hz, differential input		70		
DC Offset	After DC Servo calibration		+/-1		mV
Output Power	0.1% THD+N		33		mW
	1% THD+N		35		
Minimum Headphone Resistance	Normal operation	15			Ω
	Device survival with load indefinitely applied	1			Ω
Headphone Capacitance				2	nF
Quiescent Current			4		mA

Test Conditions

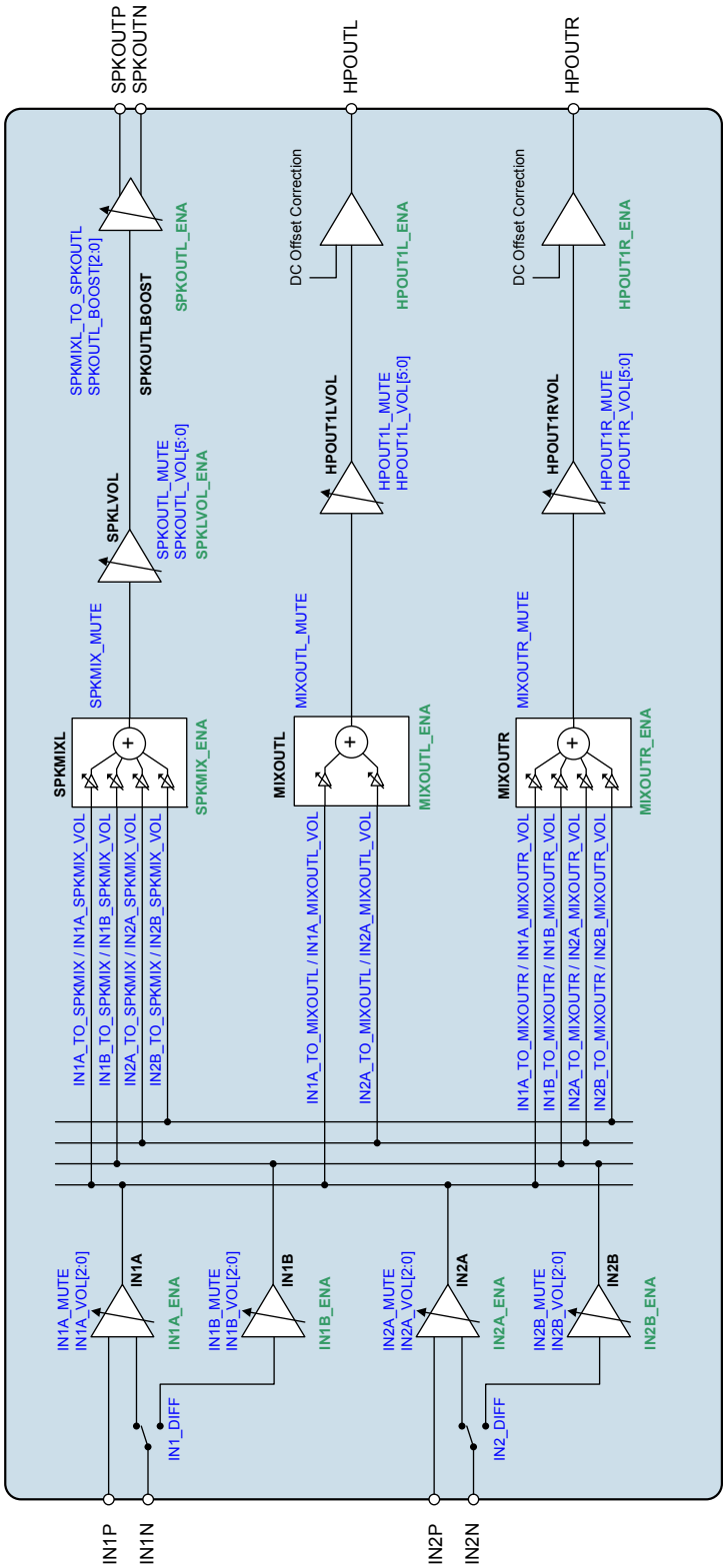
SPKVDD = 3.6V, AVDD=1.8V, GND=0V, T_A = +25°C, 1kHz signal, PGA gain = 0dB unless otherwise stated

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Speaker Driver Class D Audio Performance (R_L=8Ω + 10µH BTL)					
SNR (A-weighted)	Speaker Boost = 12dB, Differential input from IN1P/N or IN2P/N		92		dB
	Stereo input from IN1P/N or IN2P/N		90		
THD (P_O=500mW)	Speaker Boost = 12dB		-72		dB
THD+N (P_O=500mW)	Speaker Boost = 12dB		-70		dB
PSRR	AVDD with 100mVpk-pk at 217Hz, differential input		80		dB
	SPKVDD with 100mVpk-pk at 217Hz, differential input		70		
DC Offset at Load			TBD		mV
Efficiency	Speaker Boost = 12dB, 0dBFS input		85		%
Output Power	SPKVDD=5.0V, THD+N ≤ 1%, Speaker Boost = 12dB		1000		mW
	SPKVDD=4.2V, THD+N ≤ 1%, Speaker Boost = 12dB		950		
	SPKVDD=3.7V, THD+N ≤ 1%, Speaker Boost = 12dB		750		
SPKVDD Leakage Current			1		µA
Quiescent Current			5		mA
Analogue Reference Level					
VMID Midrail Reference Voltage		-3%	AVDD/2	+3%	V
Charge Pump					
Start-up Time				500	µs
Supply Voltage		1.71		2.0	V
CPVOUTP	Normal mode		AVDD		V
	Low power mode		AVDD/2		
CPVOUTN	Normal mode		-AVDD		V
	Low power mode		-AVDD/2		
Output Impedance			TBD		kΩ
Flyback Capacitor (between CPCA and CPCB)	at 2V	1	2.2		µF
CPVOUTP Capacitor	at 2V	2	2.2		µF
CPVOUTN Capacitor	at 2V	2	2.2		µF
Digital Input / Output					
Input HIGH Level		0.7 × AVDD			V
Input LOW Level				0.3 × AVDD	V
Output HIGH Level	I_{OL} = 1mA	0.7 × AVDD			V
Output LOW Level	I_{OH} = -1mA			0.3 × AVDD	V
Input capacitance			10		pF
Input leakage		-0.9		0.9	uA
Start-Up Time					
Start up time	Speaker and Headphone		50		ms

TERMINOLOGY

1. Signal-to-Noise Ratio (dB) – SNR is a measure of the difference in level between the maximum full scale output signal and the output with no input signal applied.
2. Total Harmonic Distortion (dB) – THD is the level of the rms value of the sum of harmonic distortion products relative to the amplitude of the measured output signal.
3. Total Harmonic Distortion plus Noise (dB) – THD+N is the level of the rms value of the sum of harmonic distortion products plus noise in the specified bandwidth relative to the amplitude of the measured output signal.
4. Crosstalk (L/R) (dB) – left-to-right and right-to-left channel crosstalk is the measured signal level in the idle channel at the test signal frequency relative to the signal level at the output of the active channel. The active channel is configured and supplied with an appropriate input signal to drive a full scale output, with signal measured at the output of the associated idle channel.
5. Mute Attenuation – This is a measure of the difference in level between the full scale output signal and the output with mute applied.
6. All performance measurements carried out with 20kHz low pass filter, and where noted an A-weighted filter. Failure to use such a filter will result in higher THD and lower SNR readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.

AUDIO SIGNAL PATHS DIAGRAM



CONTROL INTERFACE TIMING

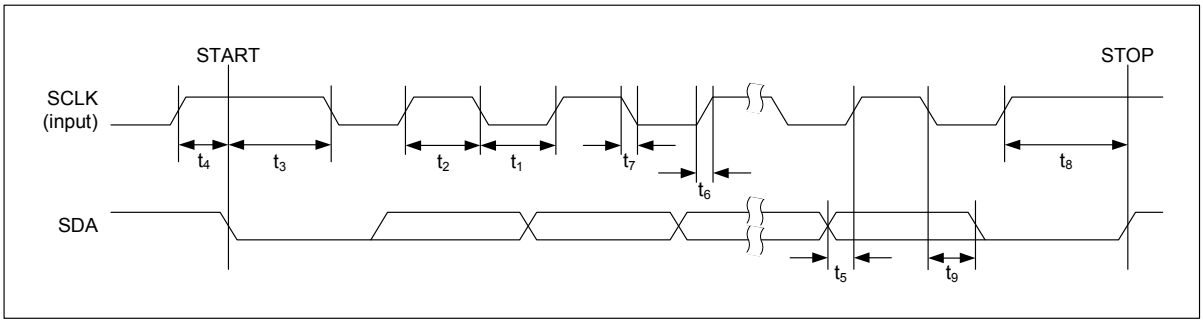


Figure 2 Control Interface Timing

Test Conditions

SPKVDD = 3.6V, AVDD=1.8V, GND=0V, T_A = +25°C, 1kHz signal, PGA gain = 0dB unless otherwise stated

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
SCLK Frequency				400	kHz
SCLK Low Pulse-Width	t_1	1300			ns
SCLK High Pulse-Width	t_2	600			ns
Hold Time (Start Condition)	t_3	600			ns
Setup Time (Start Condition)	t_4	600			ns
Data Setup Time	t_5	100			ns
SDA, SCLK Rise Time	t_6			300	ns
SDA, SCLK Fall Time	t_7			300	ns
Setup Time (Stop Condition)	t_8	600			ns
Data Hold Time	t_9			900	ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns

DEVICE DESCRIPTION

INTRODUCTION

The WM9090 is an ultra-low power, high quality audio subsystem, including a headphone and speaker driver. Its flexible architecture is designed to interface with a wide range of analogue components. The small 2.0 x 2.5mm footprint makes it ideal for portable applications such as mobile handsets.

Four flexible analogue input pins allow interfacing to up to four single-ended sources (eg. two stereo signal pairs). A differential input can also be accommodated if required. Connection to an external voice CODEC, FM radio, melody IC or generic line input are all fully supported. Signal routing to the output mixers provides maximum flexibility to support a wide variety of usage modes.

Three analogue output drivers are integrated, including a high quality Class D speaker driver supporting 750mW output power at 3.7V. A configurable automatic gain control (AGC) is provided on the speaker output path, to prevent clipping or power overload at the loudspeaker.

Ground-referenced stereo headphone outputs are also provided; these are powered from an integrated Charge Pump, enabling high quality, power efficient headphone playback. The ground-referenced design reduces power consumption, improves bass response, and enables direct headphone connection without any DC blocking capacitors. A DC Servo circuit is provided for DC offset measurement and correction, thereby suppressing pops and reducing power consumption.

Internal differential signal routing and amplifier configurations have been optimised to provide the lowest possible power consumption for a wide range of usage scenarios, including voice calls and music playback. The speaker drivers offer low leakage and high PSRR; this enables direct connection to a Lithium battery. The speaker driver provides eight levels of boost gain to allow output signal levels to be maximised for many commonly-used SPKVDD/AVDD combinations.

An integrated oscillator is provided to support all the WM9090 clocking requirements, including the Class D switching clock, Headphone Charge Pump and DC Servo control.

The WM9090 is controlled via a standard 2-wire I2C interface, providing full software control of all features, together with device register readback. The interface provides support for I/O voltages up to 2.7V. An integrated Control Write Sequencer enables automatic scheduling of control sequences; commonly-used signal configurations may be selected using ready-programmed sequences, including time-optimised control of the WM9090 pop suppression features. Unused circuitry can be disabled under software control, in order to save power; low leakage currents enable extended standby/off time in portable battery-powered applications.

INPUT SIGNAL PATH

The WM9090 supports two differential analogue input channels, configurable in a number of combinations:

- Up to two differential line inputs to analogue mixers
- Up to four single-ended line inputs to analogue mixers

The inputs may be mixed together or independently routed to different combinations of output drivers. The WM9090 input signal paths and control registers are illustrated in Figure 3.

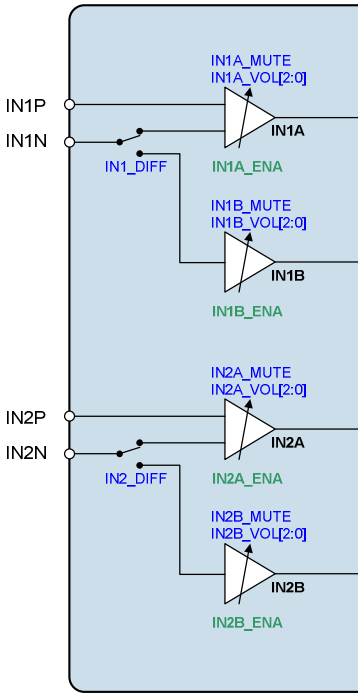


Figure 3 Control Registers for Input Signal Path

LINE INPUTS

All of the analogue input pins are designed as line inputs. These pins can be configured as single-ended or differential inputs, with flexible routing options and gain controls suitable for many different usage cases. These inputs provide a high gain path for low input signal levels.

The line input pins IN1P and IN1N provide a differential input path to PGA IN1A. If required, these input pins can be configured as two separate single-ended inputs to PGAs IN1A and IN1B respectively. Single ended configuration is selected by writing a 0 to the IN1_DIFF register bit.

The line input pins IN2P and IN2N provide a differential input path to PGA IN2A. If required, these input pins can be configured as two separate single-ended inputs to PGAs IN2A and IN2B respectively. Single ended configuration is selected by writing a 0 to the IN2_DIFF register bit.

Signal path configuration to the input PGAs is detailed later in this section. Signal path configuration to the output mixers and speaker mixers is described in “Output Signal Path”.

Note that, by default, the analogue input pins are clamped to VMID in order to prevent audible pops caused by enabling the input paths. When one or more analogue input path is in use, the respective input clamp(s) must be disabled using the register bits described under “Power Sequences and Pop Suppression Control”.

INPUT PGA ENABLE

The Input PGAs are enabled using register bits IN1A_ENA, IN1B_ENA, IN2A_ENA and IN2B_ENA, as described in Table 1. The Input PGAs must be enabled for line input on the respective input pins.

Note that, for differential input on IN1P and IN1N, it is not necessary to enable PGA IN1B.

Note that, for differential input on IN2P and IN2N, it is not necessary to enable PGA IN2B.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 (02h) Power Management (2)	7	IN1A_ENA	0	IN1A Input PGA Enable 0 = Disabled 1 = Enabled
	6	IN1B_ENA	0	IN1B Input PGA Enable 0 = Disabled 1 = Enabled (Note this is only required for single-ended input on the IN1N pin)
	5	IN2A_ENA	0	IN2A Input PGA Enable 0 = Disabled 1 = Enabled
	4	IN2B_ENA	0	IN2B Input PGA Enable 0 = Disabled 1 = Enabled (Note this is only required for single-ended input on the IN2N pin)

Table 1 Input PGA Enable

For normal operation of the input PGAs, the reference voltage VMID and the bias current must also be enabled. See “Reference Voltages and Master Bias” for details of the associated controls VMID_RES and BIAS_ENA.

INPUT PGA CONFIGURATION

The input PGAs can be configured in single-ended mode or differential mode, using the IN1_DIFF and IN2_DIFF register bits described in Table 2.

In single-ended mode, an input pin is routed to each individual PGA. In differential mode, a pair of input pins is routed to PGA IN1A or IN2A.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R22 (16h) IN1 Line Control	1	IN1_DIFF	1	PGA IN1A and IN1B configuration 0 = Single-ended mode 1 = Differential mode
R23 (17h) IN2 Line Control	1	IN2_DIFF	1	PGA IN2A and IN2B configuration 0 = Single-ended mode 1 = Differential mode

Table 2 Input PGA Configuration

INPUT PGA VOLUME CONTROL

Each of the four input PGAs has an independently controlled gain range of -6dB to +18dB. The gains on the inverting and non-inverting inputs to the PGAs are always equal. Each Input PGA can be independently muted using the PGA mute bits as described in Table 3.

Note that, when input pins IN1P and IN1N are configured in differential mode, then PGA IN1B is not used, and the volume control is provided on PGA IN1A only.

Note that, when input pins IN2P and IN2N are configured in differential mode, then PGA IN2B is not used, and the volume control is provided on PGA IN2A only.

The gain level of PGA IN1A and IN2A differs between single-ended and differential mode. For example, a 0dB volume setting provides 0dB gain in differential mode, but in single-ended mode it will apply +6dB gain. In single-ended mode, the IN1A/IN2A input PGAs have a controlled gain range of 0dB to +24dB. In differential mode, these PGAs have a controlled gain range of -6dB to +18dB.

To prevent "zipper noise", a zero-cross function is provided on the input PGAs. When this feature is enabled, volume updates will not take place until a zero-crossing is detected. In the case of a long period without zero-crossings, a timeout function is provided. When the zero-cross function is enabled, the volume will update after the timeout period if no earlier zero-cross has occurred. The timeout clock is enabled using TOCLK_ENA, the timeout period is set by TOCLK_RATE. See “Clocking Control” for more information on these fields.

The IN1_VU and IN2_VU bits control the loading of the input PGA volume data. When IN1_VU and IN2_VU are set to 0, the PGA volume data will be loaded into the respective control register, but will not actually change the gain setting. The IN1A and IN1B volume settings are both updated when a 1 is written to IN1_VU; the IN2A and IN2B volume settings are both updated when a 1 is written to IN2_VU. This makes it possible to update the gain of two single-ended input paths simultaneously.

Note that, in differential input modes, the Volume Update control bits IN1_VU and/or IN2_VU should always be set to 1.

The Input PGA Volume Control register fields are described in Table 3.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R24 (18h) IN1 Line Input A Volume	8	IN1_VU	N/A	IN1 Volume Update Writing a 1 to this bit will cause IN1A and IN1B input PGA volumes to be updated simultaneously
	7	IN1A_MUTE	1	IN1A PGA Mute 0 = Un-Mute 1 = Mute
	6	IN1A_ZC	0	IN1A PGA Zero Cross Control 0 = Change gain immediately 1 = Change gain on zero cross only

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	2:0	IN1A_VOL [2:0]	011	IN1A Volume (differential mode) 000 = -6dB 001 = -3.5dB 010 = 0dB 011 = +3.5dB 100 = +6dB 101 = +12dB 110 = +18dB 111 = +18dB IN1A Volume (single-ended mode) 000 = 0dB 001 = +2.5dB 010 = +6dB 011 = +9.5dB 100 = +12dB 101 = +18dB 110 = +24dB 111 = +24dB
R25 (19h) IN1 Line Input B Volume	8	IN1_VU	N/A	IN1 Volume Update Writing a 1 to this bit will cause IN1A and IN1B input PGA volumes to be updated simultaneously
	7	IN1B_MUTE	1	IN1B PGA Mute 0 = Un-Mute 1 = Mute
	6	IN1B_ZC	0	IN1B PGA Zero Cross Control 0 = Change gain immediately 1 = Change gain on zero cross only
	2:0	IN1B_VOL [2:0]	011	IN1B Volume (differential mode) 000 = -6dB 001 = -3.5dB 010 = 0dB 011 = +3.5dB 100 = +6dB 101 = +12dB 110 = +18dB 111 = +18dB IN1B Volume (single-ended mode) 000 = 0dB 001 = +2.5dB 010 = +6dB 011 = +9.5dB 100 = +12dB 101 = +18dB 110 = +24dB 111 = +24dB
R26 (1Ah) IN2 Line Input A Volume	8	IN2_VU	N/A	Input PGA Volume Update Writing a 1 to this bit will cause IN2A and IN2B input PGA volumes to be updated simultaneously
	7	IN2A_MUTE	1	IN2A PGA Mute 0 = Un-Mute 1 = Mute

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	6	IN2A_ZC	0	IN2A PGA Zero Cross Control 0 = Change gain immediately 1 = Change gain on zero cross only
	2:0	IN2A_VOL [2:0]	011	IN2A Volume (differential mode) 000 = -6dB 001 = -3.5dB 010 = 0dB 011 = +3.5dB 100 = +6dB 101 = +12dB 110 = +18dB 111 = +18dB IN2A Volume (single-ended mode) 000 = 0dB 001 = +2.5dB 010 = +6dB 011 = +9.5dB 100 = +12dB 101 = +18dB 110 = +24dB 111 = +24dB
R27 (1Bh) IN2 Line Input B Volume	8	IN2_VU	N/A	Input PGA Volume Update Writing a 1 to this bit will cause IN2A and IN2B input PGA volumes to be updated simultaneously
	7	IN2B_MUTE	1	IN2B PGA Mute 0 = Un-Mute 1 = Mute
	6	IN2B_ZC	0	IN2B PGA Zero Cross Control 0 = Change gain immediately 1 = Change gain on zero cross only
	2:0	IN2B_VOL [2:0]	011	IN2B Volume (differential mode) 000 = -6dB 001 = -3.5dB 010 = 0dB 011 = +3.5dB 100 = +6dB 101 = +12dB 110 = +18dB 111 = +18dB IN2B Volume (single-ended mode) 000 = 0dB 001 = +2.5dB 010 = +6dB 011 = +9.5dB 100 = +12dB 101 = +18dB 110 = +24dB 111 = +24dB

Table 3 Input PGA Volume Control

OUTPUT SIGNAL PATH

The WM9090 output mixers provide a high degree of flexibility, allowing configurable operation of multiple signal paths through the device to a variety of analogue outputs. The outputs comprise a ground referenced headphone driver and Class D loudspeaker driver. See “Analogue Outputs” for further details of these outputs.

The WM9090 output signal paths and control registers are illustrated in Figure 4.

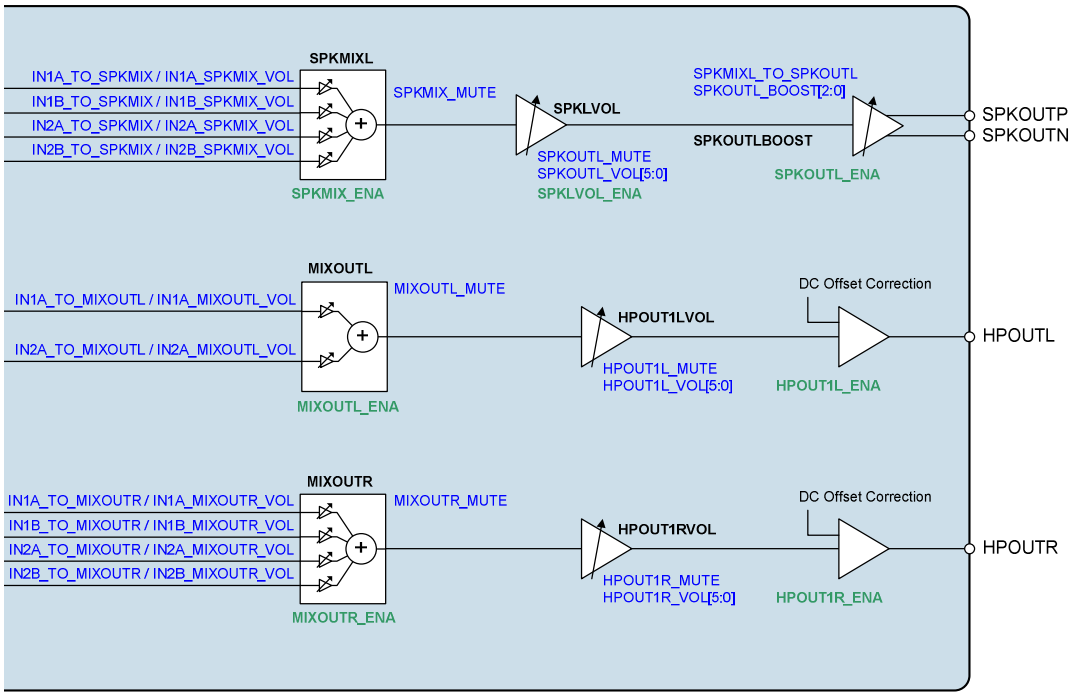


Figure 4 Control Registers for Output Signal Path

OUTPUT SIGNAL PATHS ENABLE

The output mixers and drivers can be independently enabled and disabled as described in Table 4.

See “Power Sequences and Pop Suppression Control” for details of additional control bits relating to the Headphone Output configuration.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1 (01h) Power Management (1)	12	SPKOUTL_ENA	0	Speaker Output Enable 0 = Disabled 1 = Enabled
	9	HPOUT1L_ENA	0	Headphone Output (HPOUTL) input stage enable 0 = Disabled 1 = Enabled
	8	HPOUT1R_ENA	0	Headphone Output (HPOUTR) input stage enable 0 = Disabled 1 = Enabled
R3 (03h) Power Management	8	SPKLVOL_ENA	0	Speaker PGA Enable 0 = Disabled 1 = Enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
(3)	5	MIXOUTL_ENA	0	MIXOUTL Headphone Mixer Enable 0 = Disabled 1 = Enabled
	4	MIXOUTR_ENA	0	MIXOUTR Headphone Mixer Enable 0 = Disabled 1 = Enabled
	3	SPKMIX_ENA	0	SPKMIX Speaker Mixer Enable 0 = Disabled 1 = Enabled

Table 4 Output Signal Paths Enable

SPEAKER MIXER CONTROL

The signal path configuration registers for the Speaker Mixer are described in Table 5. Each of the input PGAs IN1A, IN1B, IN2A and IN2B is independently selectable as an input to the Speaker Mixer.

Care should be taken when enabling more than one path to a Speaker Mixer in order to avoid clipping. The gain of each input path is adjustable using a selectable volume control in each path to facilitate this.

The Speaker Mixer output can be muted or enabled using the SPKMIX_MUTE register bit. The Speaker Mixer volume is also controlled by the Speaker Output PGA, as defined in Table 6.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R54 (36h) Speaker Mixer	6	IN1A_TO_SPKMIX	0	IN1A to SPKMIX enable 0 = Disabled 1 = Enabled
	4	IN1B_TO_SPKMIX	0	IN1B to SPKMIX enable 0 = Disabled 1 = Enabled
	2	IN2A_TO_SPKMIX	0	IN2A to SPKMIX enable 0 = Disabled 1 = Enabled
	0	IN2B_TO_SPKMIX	0	IN2B to SPKMIX enable 0 = Disabled 1 = Enabled
R34 (22h) SPKMIXL Attenuation	8	SPKMIX_MUTE	1	SPKMIX Output mute 0 = Un-Mute 1 = Mute
	7:6	IN1A_SPKMIX_VOL	00	IN1A to SPKMIX volume control 00 = 0dB 01 = -6dB 10 = -9dB 11 = -12dB
	5:4	IN1B_SPKMIX_VOL	00	IN1B to SPKMIX volume control 00 = 0dB 01 = -6dB 10 = -9dB 11 = -12dB
	3:2	IN2A_SPKMIX_VOL	00	IN2A to SPKMIX volume control 00 = 0dB 01 = -6dB 10 = -9dB 11 = -12dB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	1:0	IN2B_SPKMIX_VOL [1:0]	00	IN2B to SPKMIX volume control 00 = 0dB 01 = -6dB 10 = -9dB 11 = -12dB

Table 5 Speaker Mixer (SPKMIX) Control

SPEAKER OUTPUT VOLUME CONTROL

The speaker output PGA controls are shown in Table 6.

A zero-cross function is provided on the speaker output PGA. Note that the timeout clock TOCLK must be enabled when using the zero-cross function. See "Clocking Control" for more information on the TOCLK control fields.

The SPKOUT_VU bit controls the loading of the speaker PGA volume data. This bit should be set to 1 whenever the SPKOUTL_VOL register is updated.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R38 (26h) Speaker Volume Left	8	SPKOUT_VU	N/A	Speaker Output PGA Volume Update Writing a 1 to this bit will update the SPKOUTL volume.
	7	SPKOUTL_ZC	0	Speaker Output PGA Zero Cross Control 0 = Change gain immediately 1 = Change gain on zero cross only
	6	SPKOUTL_MUTE	0	Speaker Output PGA Mute 0 = Un-mute 1 = Mute
	5:0	SPKOUTL_VOL [5:0]	39h (0dB)	Speaker Output PGA Volume -57dB to +6dB in 1dB steps (See Table 11 for output PGA volume control range)

Table 6 Speaker Output PGA Control

SPEAKER BOOST MIXER CONTROL

The Class D speaker driver also incorporates its own boost mixer.

The boost mixer provides an additional AC gain (boost) function to shift signal levels between the AVDD and SPKVDD voltage domains for maximum output power. The AC gain (boost) function is described in the "Analogue Outputs" section.

The SPKMIXL_TO_SPKOUTL register bit must be enabled when using the speaker output signal path, as described in Table 7. Note that this is the default condition.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R36 (24h) SPKOUT Mixers	4	SPKMIXL_TO_SPKOUTL	1	SPKMIX to Speaker Output enable 0 = Disabled 1 = Enabled

Table 7 Speaker Boost Mixer Control

HEADPHONE MIXER CONTROL

The Headphone Mixer configuration registers are described in Table 8 for the Left Channel (MIXOUTL) and Table 9 for the Right Channel (MIXOUTR). A subset of the available input PGAs IN1A, IN1B, IN2A and IN2B is selectable as an input to each of the Headphone Mixers, as illustrated in Figure 4.

Care should be taken when enabling more than one path to a Headphone Mixer in order to avoid clipping. The gain of each input path is adjustable using a selectable volume control in each path to facilitate this.

The Headphone Mixer outputs can be muted or enabled using the MIXOUTL_MUTE and MIXOUTR_MUTE register bits. The Headphone Mixer volume is also controlled by the Headphone Output PGAs, as defined in Table 10.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R45 (2Dh) Output Mixer1	6	IN1A_TO_MIXOUTL	0	IN1A to MIXOUTL enable 0 = Disabled 1 = Enabled
	2	IN2A_TO_MIXOUTL	0	IN2A to MIXOUTL enable 0 = Disabled 1 = Enabled
R47 (2Fh) Output Mixer3	8	MIXOUTL_MUTE	1	MIXOUTL Output mute 0 = Un-Mute 1 = Mute
	7:6	IN1A_MIXOUTL_VOL [1:0]	00	IN1A to MIXOUTL volume control 00 = 0dB 01 = -6dB 10 = -9dB 11 = -12dB
	3:2	IN2A_MIXOUTL_VOL [1:0]	00	IN2A to MIXOUTL volume control 00 = 0dB 01 = -6dB 10 = -9dB 11 = -12dB

Table 8 Left Output Mixer (MIXOUTL) Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R46 (2Eh) Output Mixer2	6	IN1A_TO_MIXOUTR	0	IN1A to MIXOUTR enable 0 = Disabled 1 = Enabled
	4	IN1B_TO_MIXOUTR	0	IN1B to MIXOUTR enable 0 = Disabled 1 = Enabled
	2	IN2A_TO_MIXOUTR	0	IN2A to MIXOUTR enable 0 = Disabled 1 = Enabled
	0	IN2B_TO_MIXOUTR	0	IN2B to MIXOUTR enable 0 = Disabled 1 = Enabled
R48 (30h) Output Mixer4	8	MIXOUTR_MUTE	1	MIXOUTR Output mute 0 = Un-Mute 1 = Mute

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	7:6	IN1A_MIXOUTR_VOL [1:0]	00	IN1A to MIXOUTR volume control 00 = 0dB 01 = -6dB 10 = -9dB 11 = -12dB
	5:4	IN1B_MIXOUTR_VOL [1:0]	00	IN1B to MIXOUTR volume control 00 = 0dB 01 = -6dB 10 = -9dB 11 = -12dB
	3:2	IN2A_MIXOUTR_VOL [1:0]	00	IN2A to MIXOUTR volume control 00 = 0dB 01 = -6dB 10 = -9dB 11 = -12dB
	1:0	IN2B_MIXOUTR_VOL [1:0]	00	IN2B to MIXOUTR volume control 00 = 0dB 01 = -6dB 10 = -9dB 11 = -12dB

Table 9 Right Output Mixer (MIXOUTR) Control

HEADPHONE OUTPUT VOLUME CONTROL

The headphone output PGA controls are shown in Table 10.

A zero-cross function is provided on the headphone output PGAs. Note that the timeout clock TOCLK must be enabled when using the zero-cross function. See “Clocking Control” for more information on the TOCLK control fields.

The HPOUT1_VU bits control the loading of the headphone PGA volume data. When HPOUT1_VU is set to 0, the volume control data will be loaded into the respective control register, but will not actually change the gain setting. The headphone PGA volume settings are both updated when a 1 is written to either HPOUT1_VU bit. This makes it possible to update the gain of the left and right output paths simultaneously.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R28 (1Ch) Left Output Volume	8	HPOUT1_VU	N/A	Headphone Output PGA Volume Update Writing a 1 to this bit will update HPOUT1LVOL and HPOUT1RVOL volumes simultaneously.
	7	HPOUT1L_ZC	0	Left Headphone Output PGA Zero Cross Control 0 = Change gain immediately 1 = Change gain on zero cross only
	6	HPOUT1L_MUTE	0	Left Headphone Output PGA Mute 0 = Un-mute 1 = Mute
	5:0	HPOUT1L_VOL [5:0]	2Dh (-12dB)	Left Headphone Output PGA Volume -57dB to +6dB in 1dB steps (See Table 11 for output PGA volume control range)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R29 (1Dh) Right Output Volume	8	HPOUT1_VU	N/A	Headphone Output PGA Volume Update Writing a 1 to this bit will update HPOUT1LVOL and HPOUT1RVOL volumes simultaneously.
	7	HPOUT1R_ZC	0	Right Headphone Output PGA Zero Cross Control 0 = Change gain immediately 1 = Change gain on zero cross only
	6	HPOUT1R_MUTE	0	Right Headphone Output PGA Mute 0 = Un-mute 1 = Mute
	5:0	HPOUT1R_VOL [5:0]	2Dh (-12dB)	Right Headphone Output PGA Volume -57dB to +6dB in 1dB steps (See Table 11 for output PGA volume control range)

Table 10 Headphone Output PGA Control

PGA GAIN SETTING	VOLUME (dB)	PGA GAIN SETTING	VOLUME (dB)
0h	-57	20h	-25
1h	-56	21h	-24
2h	-55	22h	-23
3h	-54	23h	-22
4h	-53	24h	-21
5h	-52	25h	-20
6h	-51	26h	-19
7h	-50	27h	-18
8h	-49	28h	-17
9h	-48	29h	-16
Ah	-47	2Ah	-15
Bh	-46	2Bh	-14
Ch	-45	2Ch	-13
Dh	-44	2Dh	-12
Eh	-43	2Eh	-11
Fh	-42	2Fh	-10
10h	-41	30h	-9
11h	-40	31h	-8
12h	-39	32h	-7
13h	-38	33h	-6
14h	-37	34h	-5
15h	-36	35h	-4
16h	-35	36h	-3
17h	-34	37h	-2
18h	-33	38h	-1
19h	-32	39h	0
1Ah	-31	3Ah	+1
1Bh	-30	3Bh	+2
1Ch	-29	3Ch	+3
1Dh	-28	3Dh	+4
1Eh	-27	3Eh	+5
1Fh	-26	3Fh	+6

Table 11 Output PGA Volume Range

AUTOMATIC GAIN CONTROL (AGC)

The Speaker Output PGA incorporates an Automatic Gain Control (AGC) circuit. This feature provides an automatic reduction in the speaker path gain in order to prevent clipping or power overload at the loudspeaker. The AGC circuit provides two separate detection mechanisms to identify clipping or power overload respectively. Each of these two mechanisms can be independently configured to suit the loudspeaker characteristics and the desired audio response. The two control mechanisms operate together to provide a flexible and effective automatic gain control feature.

AGC CONTROL

AGC is enabled by setting the AGC_ENA register bit, as defined in Table 12.

The AGC can provide attenuation in the speaker output path - note that it can never apply additional gain to boost the signal level. The maximum extent of the AGC attenuation can be controlled by setting the AGC_MINGAIN register. This field sets the lowest gain level that can be selected by the AGC under signal clipping or power limiting conditions.

When the signal conditions trigger the AGC to apply attenuation, the Speaker PGA gain is controlled automatically by the AGC. In order to prevent 'zipper noise' from the gain adjustment, the PGA gain is only changed when a signal zero-cross is detected. When AGC_RAMP = 1, then the gain adjustment is restricted to a single gain step on each zero-cross. When AGC_RAMP = 0, then multiple gain steps may be applied, if necessary, on each zero-cross.

Selecting single gain steps only will result in a more gradual gain adjustment, but the AGC may also be slower to remove signal clipping under this selection. Note that the AGC attenuation has a step size of 0.5dB, providing a high resolution of signal level control.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3 (03h) Power Management (3)	14	AGC_ENA	0	AGC Enable 0 = Disabled 1 = Enabled
R100 (64h) AGC Control 2	8	AGC_RAMP	0	AGC Ramp Control Selects how the AGC gain adjustment is applied 0 = Multiple gains steps per zero-cross 1 = Single gain step per zero-cross
	5:0	AGC_MINGAIN [5:0]	00000	AGC Minimum Gain -57dB to +6dB in 1dB steps (See Table 11 for AGC Minimum Gain range)

Table 12 AGC Control

AGC ANTI-CLIP

The AGC incorporates two mechanisms for monitoring the signal conditions. One of these is the anti-clip threshold detection. The anti-clip function measures the speaker supply voltage, SPKVDD, and compares this with the output signal level. The difference between these voltages is referred to as the headroom; to avoid clipping, the signal level must always be less than the supply voltage. If the headroom is small (ie. the signal level is very close to the supply voltage), then clipping and distortion will occur.

The anti-clip function can be disabled using the AGC_CLIP_ENA bit. It is enabled by default.

The headroom threshold at which the AGC will apply attenuation is set using the AGC_CLIP_THR register. Values in the range -200mV to 800mV can be selected. When the signal headroom is 300mV, the distortion (THD) is approximately 1%. Therefore, if the anti-clip threshold is set to 300mV, then the AGC would aim to limit the distortion to be no worse than 1% under maximum signal conditions. Selecting a larger headroom threshold will avoid clipping across a wider range of operating conditions.

When the AGC applies signal attenuation triggered by the anti-clip threshold, the signal gain is reduced at a rate that is set by the AGC_CLIP_ATK register. When the anti-clip threshold is no longer met (due to the signal level reduction), then the AGC increases the signal gain at a rate set by the AGC_CLIP_DCY register.

Note that, when the anti-clip and power limiting thresholds are both triggered concurrently, then the signal gain is reduced at the rate set by the AGC_CLIP_ATK register and is increased at the rate set by AGC_PWR_DCY. These fields are defined in Table 13 and Table 14 respectively.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R98 (62h) AGC Control 0	15	AGC_CLIP_ENA	1	Enable AGC Anti-Clip Mode 0 = Disabled 1 = Enabled
	11:8	AGC_CLIP_THR [3:0]	0110	AGC Anti-Clip Threshold Sets the headroom between SPKPGA output and SPKVDD at which Anti-Clip limiting will be applied 0000 = -200mV 0001 = -150mV 0010 = -100mV 0011 = -50mV 0100 = 0mV 0101 = 50mV 0110 = 100mV 0111 = 150mV 1000 = 200mV 1001 = 250mV 1010 = 300mV 1011 = 400mV 1100 = 500mV 1101 = 600mV 1110 = 700mV 1111 = 800mV
	6:4	AGC_CLIP_ATK [2:0]	100	AGC Anti-Clip Attack Rate Sets the rate of AGC gain reduction when clipping is detected 000 = 0.6ms/6dB 001 = 5.4ms/6dB 010 = 10.2ms/6dB 011 = 15.0ms/6dB 100 = 19.8ms/6dB 101 = 24.6ms/6dB 110 = 29.4ms/6dB 111 = 34.1ms/6dB
	2:0	AGC_CLIP_DCY [2:0]	000	AGC Anti-Clip Decay Rate Sets the rate of AGC gain increments after a period of clipping 000 = 120ms/6dB 001 = 480ms/6dB 010 = 820ms/6dB 011 = 1170ms/6dB 100 = 1640ms/6dB 101 = 2050ms/6dB 110 = 2730ms/6dB 111 = 4100ms/6dB

Table 13 AGC Anti-Clip Control

AGC POWER LIMITING

The second mechanism used by the AGC to monitor signal conditions is the power limit function. The speaker output voltage is measured, and the corresponding power output is determined. The power limiting function can be disabled using the AGC_PWR_ENA bit. It is enabled by default.

The power output threshold at which the AGC will apply attenuation is set using the AGC_PWR_THR register. Power levels in the range 300mW and 1050mW can be selected. Note that these are RMS power levels, assuming an 8Ω speaker.

The power output threshold is also controlled by the AGC_PWR_AVG register. When AGC_PWR_AVG = 1, then the AGC responds to the RMS power level as quoted above. When AGC_PWR_AVG = 0, then the AGC responds to the instantaneous voltage at the speaker output. Selecting the RMS power level is recommended, as this represents the average signal level.

When the AGC applies signal attenuation triggered by the power limit threshold, the signal gain is reduced at a rate that is set by the AGC_PWR_ATK register. When the power limit threshold is no longer met (due to the signal level reduction), then the AGC increases the signal gain at a rate set by the AGC_PWR_DCY register.

Note that, when the anti-clip and power limiting thresholds are both triggered concurrently, then the signal gain is reduced at the rate set by the AGC_CLIP_ATK register and is increased at the rate set by AGC_PWR_DCY. These fields are defined in Table 13 and Table 14 respectively.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R99 (63h) AGC Control 1	15	AGC_PWR_ENA	1	Enable AGC Power Limit Mode 0 = Disabled 1 = Enabled
	12	AGC_PWR_AVG	0	AGC Power Measurement mode 0 = Peak power 1 = RMS power
	11:8	AGC_PWR_THR [2:0]	0000	AGC Power Limit Threshold Sets the output level at which Power limiting will be applied. Assumes RMS power mode and 8ohm speaker. 0000 = 300mW 0001 = 350mW 0010 = 400mW 0011 = 450mW 0100 = 500mW 0101 = 550mW 0110 = 600mW 0111 = 650mW 1000 = 700mW 1001 = 750mW 1010 = 800mW 1011 = 850mW 1100 = 900mW 1101 = 950mW 1110 = 1000mW 1111 = 1050mW
	6:4	AGC_PWR_ATK [2:0]	000	AGC Power Limiting Attack Rate Sets the rate of AGC gain reduction when power limiting is applied 000 = 120ms/6dB 001 = 480ms/6dB 010 = 840ms/6dB 011 = 1200ms/6dB 100 = 1680ms/6dB 101 = 2040ms/6dB 110 = 2760ms/6dB 111 = 4080ms/6dB
	2:0	AGC_PWR_DCY [2:0]	000	AGC Power Limiting Decay Rate Sets the rate of AGC gain increments after a period of power limiting 000 = 1080ms/6dB 001 = 1200ms/6dB 010 = 1320ms/6dB 011 = 1680ms/6dB 100 = 2040ms/6dB 101 = 2760ms/6dB 110 = 4080ms/6dB 111 = 8160ms/6dB

Table 14 AGC Power Limit Control

ANALOGUE OUTPUTS

The speaker, headphone and earpiece outputs are highly configurable and may be used in many different ways.

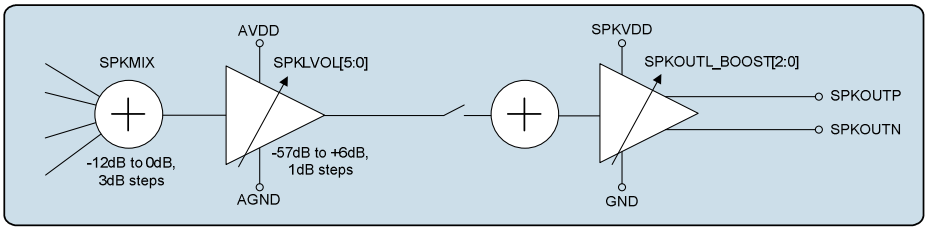
SPEAKER OUTPUT CONFIGURATIONS

The Class D speaker output is driven by the speaker mixer, SPKMIX. The speaker output operates in a BTL configuration. Fine volume control is available using the Speaker Output PGA; a boost function is also available. See the "Output Signal Path" section for more information on the speaker mixing options.

Eight levels of signal boost are provided in order to deliver maximum output power for many commonly-used SPKVDD/AVDD combinations. The boost level from 0dB to +12dB is selected using the SPKOUTL_BOOST register field. To prevent pop noise, the SPKOUTL_BOOST register should not be modified while the speaker output is enabled. Figure 5 illustrates the speaker output and the mixing and gain/boost options available.

Ultra-low leakage and high PSRR allow the speaker supply SPKVDD to be directly connected to a lithium battery. Note that an appropriate SPKVDD supply voltage must be provided to prevent waveform clipping when speaker boost is used.

DC gain is applied automatically to adjust the signal from VMID to SPKVDD/2. This provides optimum signal swing for maximum output power.



SPKOUTL_BOOST
000 = 1.00x (+0dB)
001 = 1.19x (+1.5dB)
010 = 1.41x (+3.0dB)
011 = 1.68x (+4.5dB)
100 = 2.00x (+6.0dB)
101 = 2.37x (+7.5dB)
110 = 2.81x (+9.0dB)
111 = 3.98x (+12.0dB)

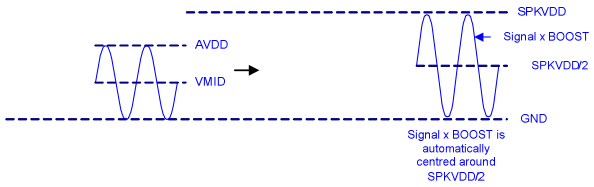


Figure 5 Speaker Output Configuration and Boost Operation

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R37 (25h) ClassD3	5:3	SPKOUTL_BOOST [2:0]	000 (1.0x)	Speaker Output Gain Boost 000 = 1.00x boost (+0dB) 001 = 1.19x boost (+1.5dB) 010 = 1.41x boost (+3.0dB) 011 = 1.68x boost (+4.5dB) 100 = 2.00x boost (+6.0dB) 101 = 2.37x boost (+7.5dB) 110 = 2.81x boost (+9.0dB) 111 = 3.98x boost (+12.0dB)

Table 15 Speaker Boost Control

HEADPHONE OUTPUT CONFIGURATIONS

The headphone output pins HPOUTL and HPOUTR are driven by the headphone output PGAs. Each PGA has its own dedicated volume control, as described in the “Output Signal Path” section. The inputs to these PGAs come from the respective output mixers MIXOUTL or MIXOUTR.

The headphone output driver is capable of driving up to 35mW into a 16Ω load such as a stereo headset or headphones. The outputs are ground-referenced, eliminating any requirement for AC coupling capacitors. This is achieved by having separate positive and negative supply rails powered by an on-chip charge pump. A DC Servo circuit removes any DC offset from the headphone outputs, suppressing ‘pop’ noise and minimising power consumption. The Charge Pump and DC Servo are described separately (see “Charge Pump” and “DC Servo” respectively).

The zobel network components should be connected to the headphone output pins HPOUTL and HPOUTR for best audio performance in all applications. The components of the zobel network have the effect of dampening high frequency oscillations and instabilities that can arise outside the audio band under certain conditions. Possible sources of these instabilities include the inductive load of a headphone coil or an active load in the form of an external line amplifier. The capacitance of lengthy cables or PCB tracks can also lead to amplifier instability. The zobel network should comprise of a 20Ω resistor and 100nF capacitor in series with each other, as illustrated in Figure 6.

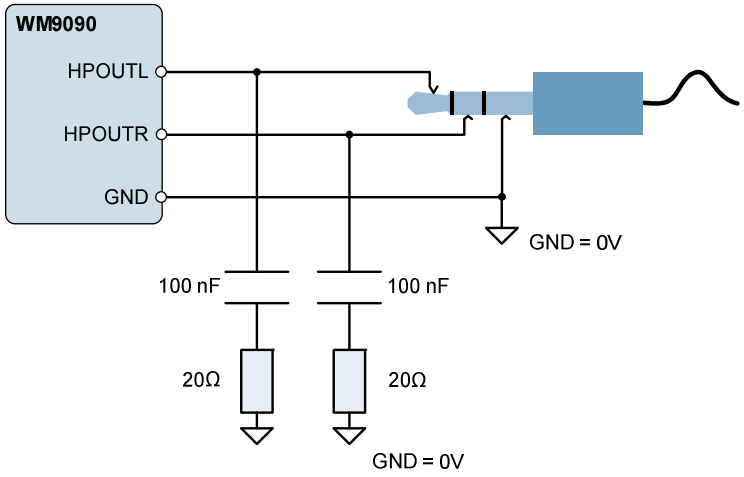


Figure 6 Zobel Network Components for HPOUTL and HPOUTR

CLOCKING CONTROL

The internal clocks for the WM9090 are derived from a common internal clock source, CLK_SYS. This clock is the reference for the Control Write Sequencer, Class D switching amplifier, DC servo control and other internal functions.

CLK_SYS is derived from an internal oscillator; this is controlled by the OSC_ENA register. The frequency of CLK_SYS is nominally 6MHz; internal dividers generate the other required clocks from this reference.

A slow clock, TOCLK, is used to set the timeout period for volume updates when zero-cross detect is used. This clock is derived from CLK_SYS and is enabled by TOCLK_ENA. The slow clock frequency is selected using the programmable dividers TOCLK_RATE, TOCLK_RATE_X4 and TOCLK_RATE_DIV16. See Table 17 for a list of possible TOCLK rates.

The clocking configuration is illustrated in Figure 7. The control registers associated with WM9090 Clocking are defined in Table 16.

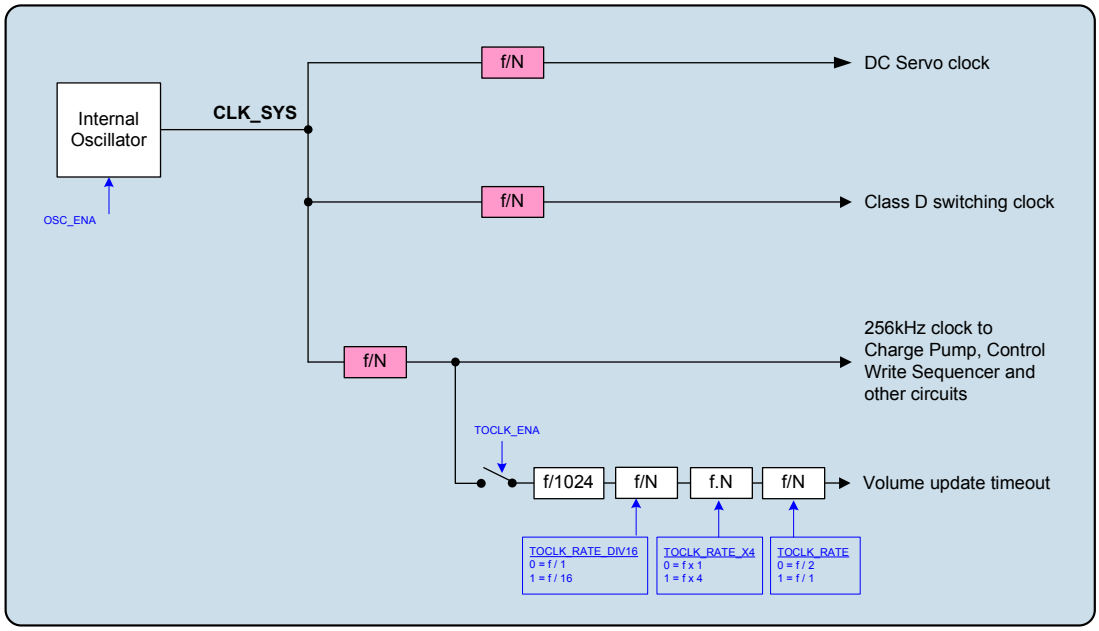


Figure 7 Clocking Scheme

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1 (01h) Power Management (1)	3	OSC_ENA	0	CLK_SYS Oscillator Enable 0 = Disabled 1 = Enabled
R6 (06h) Clocking 1	15	TOCLK_RATE	0	TOCLK Rate Divider (/2) 0 = f / 2 1 = f / 1
	14	TOCLK_ENA	0	TOCLK Enable 0 = Disabled 1 = Enabled
R66 (42h) Clocking 4	8	TOCLK_RATE_DIV16	0	TOCLK Rate Divider (/16) 0 = f / 1 1 = f / 16
	7	TOCLK_RATE_X4	0	TOCLK Rate Multiplier 0 = f x 1 1 = f x 4

Table 16 Clocking Control

TOCLK_RATE	TOCLK_RATE_X4	TOCLK_RATE_DIV16	TOCLK	
			FREQ (Hz)	PERIOD (ms)
1	1	0	1000	1
0	1	0	500	2
1	0	0	250	4
0	0	0	125	8
1	1	1	62.5	16
0	1	1	31.25	32
1	0	1	15.625	64
0	0	1	7.8125	128

Table 17 TOCLK Rates

CONTROL INTERFACE

The WM9090 is controlled by writing to registers through a 2-wire serial control interface. Readback is available for all registers, including Chip ID and power management status.

The WM9090 is a slave device on the control interface; SCLK is a clock input, while SDA is a bi-directional data pin. To allow arbitration of multiple slaves (and/or multiple masters) on the same interface, the WM9090 transmits logic 1 by tri-stating the SDA pin, rather than pulling it high. An external pull-up resistor is required to pull the SDA line high so that the logic 1 can be recognised by the master. Note that the control interface can support I/O levels up to 2.7V.

In order to allow many devices to share a single 2-wire control bus, every device on the bus has a unique 8-bit device ID (this is not the same as the 8-bit address of each register in the WM9090). The WM9090 device ID is 1101_1100 (DCh). The LSB of the device ID is the Read/Write bit; this bit is set to logic 1 for “Read” and logic 0 for “Write”.

The WM9090 operates as a slave device only. The controller indicates the start of data transfer with a high to low transition on SDA while SCLK remains high. This indicates that a device ID, register address and data will follow. The WM9090 responds to the start condition and shifts in the next eight bits on SDA (8-bit device ID including Read/Write bit, MSB first). If the device ID received matches the device ID of the WM9090, then the WM9090 responds by pulling SDA low on the next clock pulse (ACK). If the device ID is not recognised or the R/W bit is ‘1’ when operating in write only mode, the WM9090 returns to the idle condition and waits for a new start condition and valid address.

If the device ID matches the device ID of the WM9090, the data transfer continues as described below. The controller indicates the end of data transfer with a low to high transition on SDA while SCLK remains high. After receiving a complete address and data sequence the WM9090 returns to the idle state and waits for another start condition. If a start or stop condition is detected out of sequence at any point during data transfer (i.e. SDA changes while SCLK is high), the device returns to the idle condition.

The WM9090 supports the following read and write operations:

- Single write
- Single read
- Multiple write using auto-increment
- Multiple read using auto-increment

The sequence of signals associated with a single register write operation is illustrated in Figure 8.

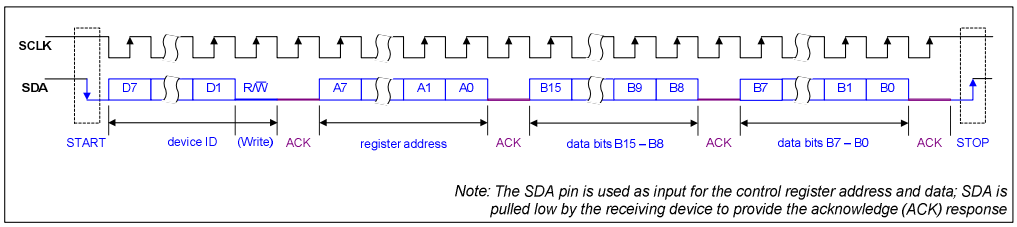


Figure 8 Control Interface Register Write

The sequence of signals associated with a single register read operation is illustrated in Figure 9.

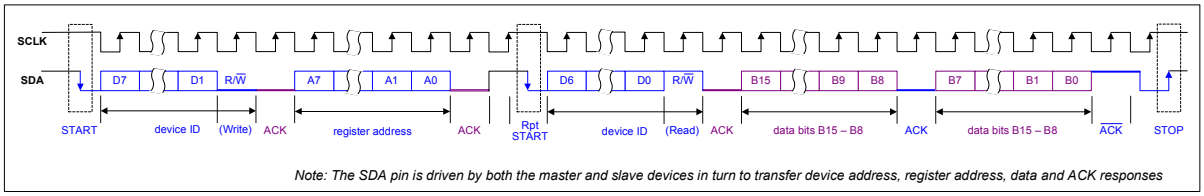


Figure 9 Control Interface Register Read

The Control Interface also supports other register operations, as listed above. The interface protocol for these operations is summarised below. The terminology used in the following figures is detailed in Table 18.

Note that multiple write and multiple read operations are supported using the auto-increment mode. This feature enables the host processor to access sequential blocks of the data in the WM9090 register map faster than is possible with single register operations.

TERMINOLOGY	DESCRIPTION	
S	Start Condition	
Sr	Repeated start	
A	Acknowledge (SDA Low)	
$\overline{A}$	Not Acknowledge (SDA High)	
P	Stop Condition	
R/$\overline{W}$	ReadNotWrite	0 = Write 1 = Read
[White field]	Data flow from bus master to WM9090	
[Grey field]	Data flow from WM9090 to bus master	

Table 18 Control Interface Terminology

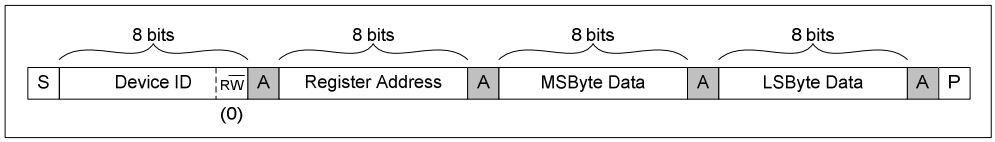


Figure 10 Single Register Write to Specified Address

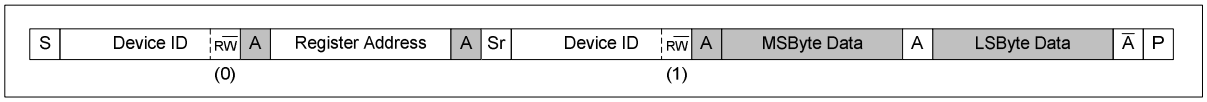


Figure 11 Single Register Read from Specified Address

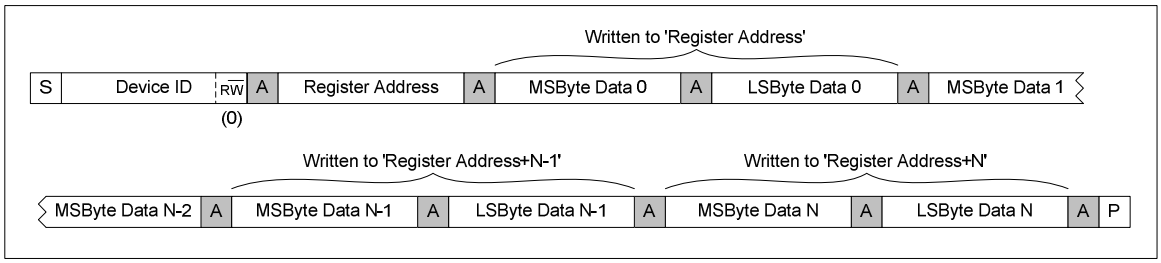


Figure 12 Multiple Register Write to Specified Address using Auto-increment

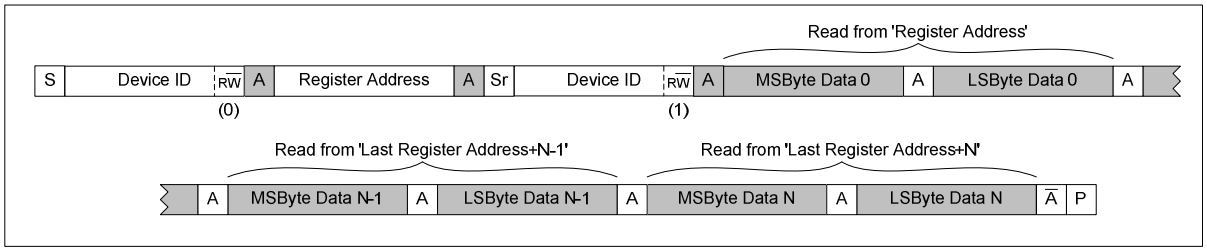


Figure 13 Multiple Register Read from Specified Address using Auto-increment

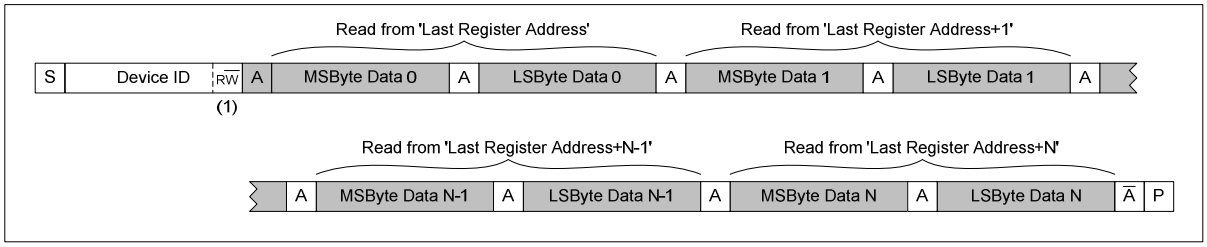


Figure 14 Multiple Register Read from Last Address using Auto-increment

CONTROL WRITE SEQUENCER

The Control Write Sequencer is a programmable unit that forms part of the WM9090 control interface logic. It provides the ability to perform a sequence of register write operations with the minimum of demands on the host processor - the sequence may be initiated by a single operation from the host processor and then left to execute independently.

Default sequences for Start-Up of each output driver and Shut-Down are provided (see “Default Sequences” section). It is recommended that these default sequences are used unless changes become necessary.

When a sequence is initiated, the sequencer performs a series of pre-defined register writes. The host processor informs the sequencer of the start index of the required sequence within the sequencer’s memory. At each step of the sequence, the contents of the selected register fields are read from the sequencer’s memory and copied into the WM9090 control registers. This continues sequentially through the sequencer’s memory until an “End of Sequence” bit is encountered; at this point, the sequencer stops and an Interrupt status flag is asserted. For cases where the timing of the write sequence is important, a programmable delay can be set for specific steps within the sequence.

Note that the Control Write Sequencer’s internal clock is derived from the internal clock CLK_SYS which must be enabled by setting OSC_ENA (see “Clocking Control”). The clock division from CLK_SYS is handled transparently by the WM9090 without user intervention.

INITIATING A SEQUENCE

The Register fields associated with running the Control Write Sequencer are described in Table 19. Note that the operation of the Control Write Sequencer also requires the internal clock CLK_SYS to be enabled via the OSC_ENA control bit (see “Clocking Control”).

The Write Sequencer is enabled by setting the WSEQ_ENA bit. The start index of the required sequence must be written to the WSEQ_START_INDEX field. Setting the WSEQ_START bit initiates the sequencer at the given start index.

The Write Sequencer can be interrupted by writing a logic 1 to the WSEQ_ABORT bit.

The current status of the Write Sequencer can be read using two further register fields - when the WSEQ_BUSY bit is asserted, this indicates that the Write Sequencer is busy. Note that, whilst the Control Write Sequencer is running a sequence (indicated by the WSEQ_BUSY bit), normal read/write operations to the Control Registers cannot be supported. The index of the current step in the Write Sequencer can be read from the WSEQ_CURRENT_INDEX field; this is an indicator of the sequencer’s progress. On completion of a sequence, this field holds the index of the last step within the last commanded sequence.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R70 (46h) Write Sequencer 0	8	WSEQ_ENA	0	Write Sequencer Enable 0 = Disabled 1 = Enabled
R73 (49h) Write Sequencer 3	9	WSEQ_ABORT	0	Writing a 1 to this bit aborts the current sequence and returns control of the device back to the serial control interface.
	8	WSEQ_START	0	Writing a 1 to this bit starts the write sequencer at the memory location indicated by the WSEQ_START_INDEX field. The sequence continues until it reaches an "End of sequence" flag. At the end of the sequence, this bit will be reset by the Write Sequencer.
	5:0	WSEQ_START_ INDEX [5:0]	00_0000	Sequence Start Index. This is the memory location of the first command in the selected sequence. 0 to 15 = RAM addresses 16 to 58 = ROM addresses 59 to 63 = Reserved
R74 (4Ah) Write Sequencer 4	0	WSEQ_BUSY (read only)	0	Sequencer Busy flag (Read Only). 0 = Sequencer idle 1 = Sequencer busy Note: it is not possible to write to control registers via the control interface while the Sequencer is Busy.
R75 (4Bh) Write Sequencer 5	5:0	WSEQ_CURRENT_INDEX [5:0] (read only)	00_0000	Sequence Current Index. This is the location of the most recently accessed command in the write sequencer memory.

Table 19 Write Sequencer Control - Initiating a Sequence

PROGRAMMING A SEQUENCE

A sequence consists of write operations to data bits (or groups of bits) within the control registers. The Register fields associated with programming the Control Write Sequencer are described in Table 20.

For each step of the sequence being programmed, the Sequencer Index must be written to the WSEQ_WRITE_INDEX field. The values 0 to 15 correspond to all the available RAM addresses within the Write Sequencer memory. (Note that memory addresses 16 to 58 also exist, but these are ROM addresses, which are not programmable.)

Having set the Index as described above, Register R71 must be written to (containing the Control Register Address, the Start Bit Position and the Field Width applicable to this step of the sequence). Also, Register R72 must be written to (containing the Register Data, the End of Sequence flag and the Delay time required after this step is executed). After writing to these two registers, the next step in the sequence may be programmed by updating WSEQ_WRITE_INDEX and repeating the procedure.

WSEQ_ADDR is an 8-bit field containing the Control Register Address in which the data should be written.

WSEQ_DATA_START is a 4-bit field which identifies the LSB position within the selected Control Register to which the data should be written. For example, setting WSEQ_DATA_START = 0100 will select bit 4 as the LSB position; in this case, 4-bit data would be written to bits 7:4 and so on.

WSEQ_DATA_WIDTH is a 3-bit field which identifies the width of the data block to be written. This enables selected portions of a Control Register to be updated without any concern for other bits within the same register, eliminating the need for read-modify-write procedures. Values of 0 to 7 correspond to data widths of 1 to 8 respectively. For example, setting WSEQ_DATA_WIDTH = 010 will cause a 3-bit data block to be written. Note that the maximum value of this field corresponds to an 8-bit data block; writing to register fields greater than 8 bits wide must be performed using two separate operations of the Control Write Sequencer.

WSEQ_DATA is an 8-bit field which contains the data to be written to the selected Control Register. The WSEQ_DATA_WIDTH field determines how many of these bits are written to the selected register; the most significant bits (above the number indicated by WSEQ_DATA_WIDTH) are ignored.

WSEQ_DELAY is a 4-bit field which controls the waiting time between the current step and the next step in the sequence i.e. the delay occurs after the write in which it was called. The total delay time per step (including execution) is given by:

$$T = k \times (2^{WSEQ\_DELAY} + 8)$$

where k = 62.5µs (under recommended operating conditions)

This gives a useful range of execution/delay times from 562µs up to 2.048s per step.

WSEQ_EOS is a 1-bit field which indicates the End of Sequence. If this bit is set, then the Control Write Sequencer will automatically stop after this step has been executed.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R70 (46h) Write Sequencer 0	3:0	WSEQ_WRITE_INDEX [3:0]	0000	Sequence Write Index. This is the memory location to which any updates to R71 and R72 will be copied. 0 to 15 = RAM addresses
R71 (47h) Write Sequencer 1	14:12	WSEQ_DATA_WIDTH [2:0]	000	Width of the data block written in this sequence step. 000 = 1 bit 001 = 2 bits 010 = 3 bits 011 = 4 bits 100 = 5 bits 101 = 6 bits 110 = 7 bits 111 = 8 bits
	11:8	WSEQ_DATA_START [3:0]	0000	Bit position of the LSB of the data block written in this sequence step. 0000 = Bit 0 … 1111 = Bit 15
	7:0	WSEQ_ADDR [7:0]	0000_0000	Control Register Address to be written to in this sequence step.
R72 (48h) Write Sequencer 2	14	WSEQ_EOS	0	End of Sequence flag. This bit indicates whether the Control Write Sequencer should stop after executing this step. 0 = Not end of sequence 1 = End of sequence (Stop the sequencer after this step).
	11:8	WSEQ_DELAY [3:0]	0000	Time delay after executing this step. Total time per step (including execution) = 62.5µs × (2^{WSEQ_DELAY} + 8)
	7:0	WSEQ_DATA [7:0]	0000_0000	Data to be written in this sequence step. When the data width is less than 8 bits, then one or more of the MSBs of WSEQ_DATA are ignored. It is recommended that unused bits be set to 0.

Table 20 Write Sequencer Control - Programming a Sequence

Note that a 'Dummy' write can be inserted into a control sequence by commanding the sequencer to write a value of 0 to bit 0 of Register R255 (FFh). This is effectively a write to a non-existent register location. This can be used in order to create placeholders ready for easy adaptation of the sequence. For example, a sequence could be defined to power-up a mono signal path from IN1P and IN1N to headphone, with a 'dummy' write included to leave space for easy modification to a stereo signal path configuration. Dummy writes can also be used in order to implement additional time delays between register writes. Dummy writes are included in the Headphone Start-Up sequence - see Table 21.

In summary, the Control Register to be written is set by the WSEQ_ADDR field. The data bits that are written are determined by a combination of WSEQ_DATA_START, WSEQ_DATA_WIDTH and WSEQ_DATA. This is illustrated below for an example case of writing to the VMID_RES field within Register R1 (01h).

In this example, the Start Position is bit 01 (WSEQ_DATA_START = 0001b) and the Data width is 2 bits (WSEQ_DATA_WIDTH = 0001b). With these settings, the Control Write Sequencer would update the Control Register R1 [2:1] with the contents of WSEQ_DATA [1:0].

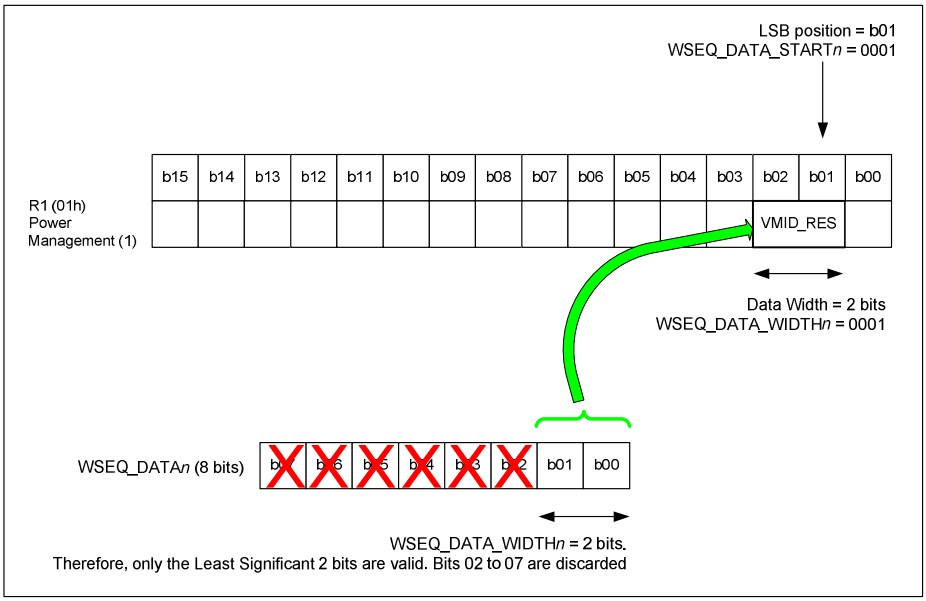


Figure 15 Control Write Sequencer Example

DEFAULT SEQUENCES

When the WM9090 is powered up, a number of Control Write Sequences are available through default settings in both RAM and ROM memory locations. The pre-programmed default settings comprise a Headphone Start-Up and a Generic Shut-Down sequence.

Note that the start-up sequence does not include audio signal path or gain setting configuration; this must be implemented prior to scheduling the sequence. Also, the start-up sequence does not include configuration of the master bias. The user must enable the clock and the master bias by setting OSC_ENA and VMID_ENA prior to executing the start-up control sequence. These registers may be reset to 0 after executing the shut-down sequence.

Index addresses 0 to 15 may be programmed to users' own settings at any time, as described in "Programming a Sequence". Users' own settings remain in memory regardless of WSEQ_ENA, and are not affected by software resets (i.e. writing to Register R0). However, any non-default sequences are lost when the device is powered down.

The following default control sequences are provided:

1. Headphone Start-Up - This sequence powers up the headphone driver and charge pump. It commands the DC Servo to perform offset correction. This sequence is intended for enabling the headphone output after initial power-on, when DC offset correction has not previously been run.

2. Generic Shut-Down - This sequence shuts down all of the WM9090 output drivers, DC Servo and charge pump circuits.

Specific details of these sequences are provided below. Note that the timings noted are typical values only.

Headphone Start-Up

The Headphone Start-Up sequence is initiated by writing 0100h to Register 73 (49h). This single operation starts the Control Write Sequencer at Index Address 0 (00h) and executes the sequence defined in Table 21.

This sequence takes approximately 40ms to run.

WSEQ INDEX	REGISTER ADDRESS	WIDTH	START	DATA	DELAY	EOS	DESCRIPTION
0 (00h)	R76 (4Ch)	1 bit	Bit 15	01h	6h	0b	CP_ENA = 1 (delay = 4.5ms)
1 (01h)	R1 (01h)	3 bits	Bit 7	07h	0h	0b	HPOUT1R_ENA = 1 HPOUT1L_ENA = 1 (delay = 0.5ms)
2 (02h)	R96 (60h)	5 bits	Bit 1	11h	0h	0b	HPOUT1R_DLY = 1 HPOUT1L_DLY = 1 (delay = 0.5ms)
3 (03h)	R84 (54h)	7 bits	Bit 0	33h	9h	0b	DCS_ENA_CHAN_0 = 1 DCS_ENA_CHAN_1 = 1 DCS_TRIG_STARTUP_0 = 1 DCS_TRIG_STARTUP_1 = 1 (delay = 32.5ms)
4 (04h)	R255 (FFh)	1 bit	Bit 0	00h	5h	0b	Dummy Write for additional delay (delay = 2.5ms)
5 (05h)	R255 (FFh)	1 bit	Bit 0	00h	0h	0b	Dummy Write for expansion (delay = 0.5ms)
6 (06h)	R255 (FFh)	1 bits	Bit 0	00h	0h	0b	Dummy Write for expansion (delay = 0.5ms)
7 (07h)	R96 (60h)	6 bits	Bit 2	3Bh	0h	1b	HPOUT1L_RMV_SHORT = 1 HPOUT1L_OUTP = 1 HPOUT1R_RMV_SHORT =1 HPOUT1R_OUTP = 1 (delay = 0.5ms)

Table 21 Headphone Start-Up Default Sequence

Generic Shut-Down

The Generic Shut-Down sequence can be initiated by writing 0110h to Register 73 (49h). This single operation starts the Control Write Sequencer at Index Address 16 (10h) and executes the sequence defined in Table 22.

This sequence takes approximately 2.8ms to run.

WSEQ INDEX	REGISTER ADDRESS	WIDTH	START	DATA	DELAY	EOS	DESCRIPTION
16 (10h)	R96 (60h)	7 bits	Bit 1	00h	0h	0b	HPOUT1R_DLY = 0 HPOUT1R_OUTP = 0 HPOUT1R_RMV_SHORT = 0 HPOUT1L_DLY = 0 HPOUT1L_OUTP = 0 HPOUT1L_RMV_SHORT = 0 (delay = 0.5ms)
17 (11h)	R84 (54h)	2 bits	Bit 0	00h	0h	0b	DCS_ENA_CHAN_0 = 0 DCS_ENA_CHAN_1 = 0 (delay = 0.5ms)
18 (12h)	R1 (01h)	2 bits	Bit 8	00h	0h	0b	HPOUT1R_ENA = 0 HPOUT1L_ENA = 0 (delay = 0.5ms)
19 (13h)	R76 (4Ch)	1 bit	Bit 15	00h	0h	0b	CP_ENA = 0 (delay = 0.5ms)
20 (14h)	R1 (01h)	2 bits	Bit 12	00h	0h	1b	SPKOUTL_ENA = 0 (delay = 0.5ms)

Table 22 Generic Shut-Down Default Sequence

POWER SEQUENCES AND POP SUPPRESSION CONTROL

The WM9090 incorporates a number of features, including Wolfson's SilentSwitch™ technology, designed to suppress pops normally associated with Start-Up, Shut-Down or signal path control. To achieve maximum benefit from these features, careful attention is required to the sequence and timing of these controls. Note that, under the recommended usage conditions of the WM9090, these features will be configured by running the default Start-Up and Shut-Down sequences as described in the "Control Write Sequencer" section. In these cases, the user does not need to set these register fields directly. Additional bias controls, also pre-programmed into Control Write Sequencer, are described in the "Reference Voltages and Master Bias" section.

INPUT VMID CLAMPS

The analogue inputs are biased to VMID in normal operation. In order to avoid audible pops caused by enabling the inputs, the WM9090 can clamp the input pins to VMID when the relevant input stage is disabled. This allows pre-charging of the input AC coupling capacitors during power-up.

The Input VMID Clamps connect the input pins to a buffered VMID reference. The buffered VMID reference is enabled by setting VMID_BUF_ENA. The VMID Clamp is enabled on each pair of input pins independently using the register bits defined in Table 23.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R22 (16h) IN1 Line Control	0	IN1_CLAMP	1	IN1P and IN1N input pad VMID clamp 0 = Clamp de-activated 1 = Clamp activated
R23 (17h) IN2 Line Control	0	IN2_CLAMP	1	IN2P and IN2N input pad VMID clamp 0 = Clamp de-activated 1 = Clamp activated
R57 (39h) AntiPOP2	3	VMID_BUF_ENA	0	VMID Buffer Enable 0 = Disabled 1 = Enabled

Table 23 Input VMID Clamps

HEADPHONE ENABLE/DISABLE

The ground-referenced headphone outputs implement Wolfson's SilentSwitch™ technology to minimise pop noise associated with enabling and disabling. The output pins HPOUTL and HPOUTR are shorted to GND by default while the individual driver stages are enabled. As a final step the short circuit is then removed on each of these paths by setting the applicable fields HPOUT1L_RMV_SHORT and HPOUT1R_RMV_SHORT.

The ground-referenced Headphone output drivers are designed to suppress pops and clicks when enabled or disabled. However, it is necessary to control the drivers in accordance with a defined sequence in start-up and shut-down to achieve the pop suppression. It is also necessary to schedule the DC Servo offset correction at the appropriate point in the sequence (see "DC Servo"). Table 24 and Table 25 describe the recommended sequences for enabling and disabling these output drivers.

SEQUENCE	HEADPHONE ENABLE
Step 1	HPOUT1L_ENA = 1 HPOUT1R_ENA = 1
Step 2	HPOUT1L_DLY = 1 HPOUT1R_DLY = 1
Step 3	DC offset correction
Step 4	HPOUT1L_OUTP = 1 HPOUT1L_RMV_SHORT = 1 HPOUT1R_OUTP = 1 HPOUT1R_RMV_SHORT = 1

Table 24 Headphone Output Enable Sequence

SEQUENCE	HEADPHONE DISABLE
Step 1	HPOUT1L_RMV_SHORT = 0 HPOUT1L_DLY = 0 HPOUT1L_OUTP = 0 HPOUT1R_RMV_SHORT = 0 HPOUT1R_DLY = 0 HPOUT1R_OUTP = 0
Step 2	HPOUT1L_ENA = 0 HPOUT1R_ENA = 0

Table 25 Headphone Output Disable Sequence

The register bits relating to pop suppression control are defined in Table 26.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1 (01h) Power Management (1)	9	HPOUT1L_ENA	0	Headphone Output (HPOUTL) input stage enable 0 = Disabled 1 = Enabled For pop-free operation, this bit should be set as the first stage of the HPOUTL Enable sequence.
	8	HPOUT1R_ENA	0	Headphone Output (HPOUTR) input stage enable 0 = Disabled 1 = Enabled For pop-free operation, this bit should be set as the first stage of the HPOUTR Enable sequence.
R96 (60h) Analogue HP 0	7	HPOUT1L_RMV_SHORT	0	Removes HPOUT1L short 0 = HPOUT1L short enabled 1 = HPOUT1L short removed For pop-free operation, this bit should be set to 1 as the final step in the HPOUTL Enable sequence.
	6	HPOUT1L_OUTP	0	Enables HPOUT1L output stage 0 = Disabled 1 = Enabled For pop-free operation, this bit should be set to 1 after the DC offset cancellation has been performed.
	5	HPOUT1L_DLY	0	Enables HPOUT1L intermediate stage 0 = Disabled 1 = Enabled For pop-free operation, this bit should be set to 1 after the output signal path has been configured, and before the DC Offset cancellation is scheduled This bit should be set with at least 20us delay after HPOUT1L_ENA.
	3	HPOUT1R_RMV_SHORT	0	Removes HPOUT1R short 0 = HPOUT1R short enabled 1 = HPOUT1R short removed For pop-free operation, this bit should be set to 1 as the final step in the HPOUTR Enable sequence.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	2	HPOUT1R_OUTP	0	Enables HPOUT1R output stage 0 = Disabled 1 = Enabled For pop-free operation, this bit should be set to 1 after the DC offset cancellation has been performed.
	1	HPOUT1R_DLY	0	Enables HPOUT1R intermediate stage 0 = Disabled 1 = Enabled For pop-free operation, this bit should be set to 1 after the output signal path has been configured, and before the DC Offset cancellation is scheduled This bit should be set with at least 20us delay after HPOUT1L_ENA.

Table 26 Pop Suppression Control

CHARGE PUMP

The WM9090 incorporates a dual-mode Charge Pump which generates the supply rails for the headphone output drivers, HPOUT1L and HPOUT1R. The Charge Pump has a single supply input, AVDD, and generates split rails CPVOUTP and CPVOUTN according to the selected mode of operation. The Charge Pump connections are illustrated in Figure 16 (see "Electrical Characteristics" for external component values). An input decoupling capacitor may also be required at AVDD, depending upon the system configuration.

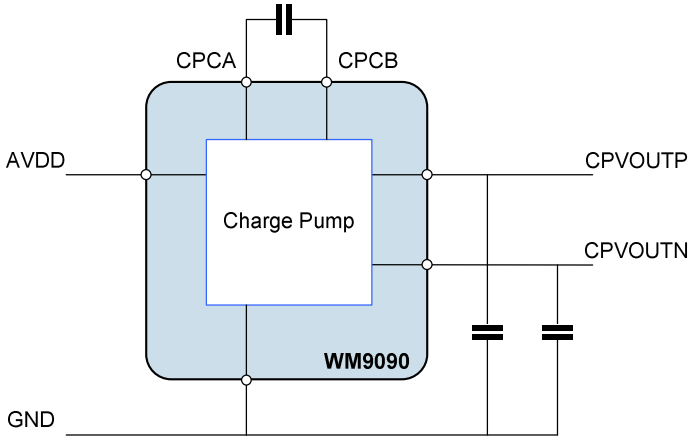


Figure 16 Charge Pump External Connections

The Charge Pump is enabled by setting the CP_ENA bit. When enabled, the charge pump adjusts the output voltages (CPVOUTP and CPVOUTN) as well as the switching frequency in order to optimise the power consumption according to the operating conditions.

The Charge Pump mode of operation is selected automatically according to the HPOUT1L_VOL and HPOUT1R_VOL register settings.

Under the recommended usage conditions of the WM9090, the Charge Pump will be enabled by running the default headphone Start-Up sequence as described in the "Control Write Sequencer" section. (Similarly, it will be disabled by running the Shut-Down sequence.) In these cases, the user does not need to write to the CP_ENA bit.

Note that the charge pump clock is derived from internal clock CLK_SYS which must be enabled by setting OSC_ENA (see "Clocking Control"). The clock division from CLK_SYS is handled transparently by the WM9090 without user intervention.

The CP_ENA register bit is defined in Table 27.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R76 (4Ch) Charge Pump 1	15	CP_ENA	0	Charge Pump Control 0 = Disabled 1 = Enabled

Table 27 Charge Pump Control

DC SERVO

The WM9090 provides a DC servo circuit on the headphone outputs HPOUTL and HPOUTR in order to remove DC offset from these ground-referenced outputs. When enabled, the DC servo ensures that the DC level of these outputs remains within 1mV of ground. Removal of the DC offset is important because any deviation from GND at the output pin will cause current to flow through the load under quiescent conditions, resulting in increased power consumption. Additionally, the presence of DC offsets can result in audible pops and clicks at power up and power down.

The recommended usage of the DC Servo is initialised by running the default Start-Up sequence as described in the "Control Write Sequencer" section. The default Start-Up sequence executes a series of DC offset corrections, after which the measured offset correction is maintained on the headphone output channels. If a different usage is required, eg. if a periodic DC offset correction is required, then the default Start-Up sequence may be modified according to specific requirements. The relevant control fields are described in the following paragraphs and are defined in Table 28.

DC SERVO ENABLE AND START-UP

The DC Servo circuit is enabled on HPOUTL and HPOUTR by setting DCS_ENA_CHAN_1 and DCS_ENA_CHAN_0 respectively. When the DC Servo is enabled, the DC offset correction can be commanded in a number of different ways, including single-shot and periodically recurring events.

Writing a logic 1 to DCS_TRIG_STARTUP_*n* initiates a series of DC offset measurements and applies the necessary correction to the associated output; ('n' = 1 for Left channel, 0 for Right channel). On completion, the headphone output will be within 1mV of GND. This is the DC Servo mode selected by the default Start-Up sequence. Completion of the DC offset correction triggered in this way is indicated by the DCS_STARTUP_COMPLETE field, as described in Table 28. Typically, this operation takes 25ms per channel.

Writing a logic 1 to DCS_TRIG_DAC_WR_*n* causes the DC offset correction to be set to the value contained in the DCS_DAC_WR_VAL_*n* fields in Register R87. This mode is useful if the required offset correction has already been determined and stored; it is faster than the DCS_TRIG_STARTUP_*n* mode, but relies on the accuracy of the stored settings. Completion of the DC offset correction triggered in this way is indicated by the DCS_DAC_WR_COMPLETE field, as described in Table 28. Typically, this operation takes 2ms per channel.

When using either of the DC Servo options above, the status of the DC offset correction process is indicated by the DCS_CAL_COMPLETE field; this is the logical OR of the DCS_STARTUP_COMPLETE and DCS_DAC_WR_COMPLETE fields.

The DC Servo control fields associated with start-up operation are described in Table 28. It is important to note that, to minimise audible pops/clicks, the Start-Up and DAC Write modes of DC Servo operation should be commanded as part of a control sequence which includes muting and shorting of the headphone outputs; a suitable sequence is defined in the default Start-Up sequence.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R84 (54h) DC Servo 0	5	DCS_TRIG_START UP_1	0	Writing 1 to this bit selects Start-Up DC Servo mode for HPOUT1L. In readback, a value of 1 indicates that the DC Servo Start-Up correction is in progress.
	4	DCS_TRIG_START UP_0	0	Writing 1 to this bit selects Start-Up DC Servo mode for HPOUT1R. In readback, a value of 1 indicates that the DC Servo Start-Up correction is in progress.
	3	DCS_TRIG_DAC_W R_1	0	Writing 1 to this bit selects DAC Write DC Servo mode for HPOUT1L. In readback, a value of 1 indicates that the DC Servo DAC Write correction is in progress.
	2	DCS_TRIG_DAC_W R_0	0	Writing 1 to this bit selects DAC Write DC Servo mode for HPOUT1R. In readback, a value of 1 indicates that the DC Servo DAC Write correction is in progress.
	1	DCS_ENA_CHAN_1	0	DC Servo enable for HPOUT1L 0 = Disabled 1 = Enabled
	0	DCS_ENA_CHAN_0	0	DC Servo enable for HPOUT1R 0 = Disabled 1 = Enabled
R87 (57h) DC Servo 3	15:8	DCS_DAC_WR_VA L1 [7:0]	0000 0000	DC Offset value for HPOUT1L in DAC Write DC Servo mode. Two's complement format. LSB is 0.25mV. Range is +/-32mV
	7:0	DCS_DAC_WR_VA L0 [7:0]	0000 0000	DC Offset value for HPOUT1R in DAC Write DC Servo mode. Two's complement format. LSB is 0.25mV. Range is +/-32mV
R88 (58h) DC Servo Readback 0	9:8	DCS_CAL_COMPL ETE [1:0]	00	DC Servo Complete status 00 = DAC Write or Start-Up DC Servo mode not completed. 01 = DAC Write or Start-Up DC Servo mode complete on HPOUT1R only. 10 = DAC Write or Start-Up DC Servo mode complete on HPOUT1L only. 11 = DAC Write or Start-Up DC Servo mode complete on HPOUT1L and HPOUT1R.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	5:4	DCS_DAC_WR_COMPLETE [1:0]	00	DC Servo DAC Write status 00 = DAC Write DC Servo mode not completed. 01 = DAC Write DC Servo mode complete on HPOUT1R only. 10 = DAC Write DC Servo mode complete on HPOUT1L only. 11 = DAC Write DC Servo mode complete on HPOUT1L and HPOUT1R.
	1:0	DCS_STARTUP_COMPLETE [1:0]	00	DC Servo Start-Up status 00 = Start-Up DC Servo mode not completed. 01 = Start-Up DC Servo mode complete on HPOUT1R only. 10 = Start-Up DC Servo mode complete on HPOUT1L only. 11 = Start-Up DC Servo mode complete on HPOUT1L and HPOUT1R.

Table 28 DC Servo Enable and Start-Up Modes

DC SERVO ACTIVE MODES

The DC Servo modes described above are suitable for initialising the DC offset correction circuit on the Headphone outputs as part of a controlled start-up sequence which is executed before the signal path is fully enabled. Additional modes are available for use whilst the signal path is active; these modes may be of benefit following a large change in signal gain, which can lead to a change in DC offset level. Periodic updates may also be desirable to remove slow drifts in DC offset caused by changes in parameters such as device temperature.

The DC Servo circuit is enabled on HPOUT1L and HPOUT1R by setting DCS_ENA_CHAN_1 and DCS_ENA_CHAN_0 respectively, as described earlier in Table 28.

Writing a logic 1 to DCS_TRIG_SINGLE_*n* initiates a single DC offset measurement and adjustment to the associated output; ('n' = 1 for Left channel, 0 for Right channel). This will adjust the DC offset correction on the selected channel by no more than 1LSB (0.25mV).

Setting DCS_TIMER_PERIOD_01 to a non-zero value will cause a single DC offset measurement and adjustment to be scheduled on a periodic basis. Periodic rates ranging from every 0.52s to in excess of 2hours can be selected.

Writing a logic 1 to DCS_TRIG_SERIES_*n* initiates a series of DC offset measurements and applies the necessary correction to the associated output. The number of DC Servo operations performed is determined by DCS_SERIES_NO_01. A maximum of 128 operations may be selected, though a much lower value will be sufficient in most applications.

The DC Servo control fields associated with active modes (suitable for use on a signal path that is in active use) are described in Table 29.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R84 (54h) DC Servo 0	13	DCS_TRIG_SINGLE_1	0	Writing 1 to this bit selects a single DC offset correction for HPOUT1L. In readback, a value of 1 indicates that the DC Servo single correction is in progress.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	12	DCS_TRIG_SINGLE_0	0	Writing 1 to this bit selects a single DC offset correction for HPOUT1R. In readback, a value of 1 indicates that the DC Servo single correction is in progress.
	9	DCS_TRIG_SERIES_1	0	Writing 1 to this bit selects a series of DC offset corrections for HPOUT1L. In readback, a value of 1 indicates that the DC Servo DAC Write correction is in progress.
	8	DCS_TRIG_SERIES_0	0	Writing 1 to this bit selects a series of DC offset corrections for HPOUT1R. In readback, a value of 1 indicates that the DC Servo DAC Write correction is in progress.
R85 (55h) DC Servo 1	11:5	DCS_SERIES_NO_01 [6:0]	010 1010	Number of DC Servo updates to perform in a series event. 0 = 1 updates 1 = 2 updates ... 127 = 128 updates
	3:0	DCS_TIMER_PERIOD_01 [3:0]	1010	Time between periodic updates. Time is calculated as 0.256s x (2^PERIOD) 0000 = Off 0001 = 0.52s 1010 = 266s (4min 26s) 1111 = 8519s (2hr 22s)

Table 29 DC Servo Active Modes

DC SERVO READBACK

The current DC offset value for each Headphone output channel can be read from Registers R89 and R90, as described in Table 30. Note that these values may form the basis of settings that are subsequently used by the DC Servo in DAC Write mode.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R89 (59h) DC Servo Readback 1	7:0	DCS_DAC_WR_VAL_1_RD	0000 0000	Readback value for HPOUT1L. Two's complement format. LSB is 0.25mV. Range is +/-32mV
R90 (5Ah) DC Servo Readback 2	7:0	DCS_DAC_WR_VAL_0_RD	0000 0000	Readback value for HPOUT1R. Two's complement format. LSB is 0.25mV. Range is +/-32mV

Table 30 DC Servo Readback

REFERENCE VOLTAGES AND MASTER BIAS

This section describes the analogue reference voltage and bias current controls. It also describes the VMID soft-start circuit for pop suppressed start-up and shut-down.

The analogue circuits in the WM9090 require a mid-rail analogue reference voltage, VMID. This reference is generated from AVDD via a programmable resistor chain. Together with the external decoupling capacitor (connected to the VMIDC pin), the programmable resistor chain results in a slow, normal or fast charging characteristic on VMID.

VMID is enabled by setting the VMID_ENA register bit. The programmable resistor chain is configured by VMID_RES [1:0], and can be used to optimise the reference for normal operation, low power standby or for fast start-up as described in Table 31.

When VMID is enabled using VMID_ENA, the WM9090 automatically controls VMID using a pop-suppression circuit to avoid a step change in VMID; this suppresses pop/click noise which could otherwise occur.

By default, the 2 x 5kΩ VMID divider is selected in order to allow fast start-up. For normal operation and lower power consumption, the VMID_RES register should be updated after start-up to select another resistor value.

The analogue circuits in the WM9090 require a bias current. The normal bias current is enabled by setting BIAS_ENA. Note that the normal bias current source requires VMID to be enabled also.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1 (01h) Power Management (1)	2:1	VMID_RES [1:0]	11	VMID Divider Enable and Select 00 = VMID disabled (for OFF mode) 01 = 2 x 50kΩ divider (for normal operation) 10 = 2 x 250kΩ divider (for low power standby) 11 = 2 x 5kΩ divider (for fast start-up)
	0	BIAS_ENA	0	Enables the Normal bias current generator (for all analogue functions) 0 = Disabled 1 = Enabled
R57 (39h) AntiPOP2	0	VMID_ENA	0	Enable VMID master bias current source 0 = Disabled 1 = Enabled

Table 31 Reference Voltages and Master Bias Enable

POWER MANAGEMENT

The WM9090 provides control registers that allow users to select which functions are active. For minimum power consumption, unused functions should be disabled. To minimise pop or click noise, it is important to enable or disable functions in the correct order. See “Power Sequences and Pop Suppression Control” for further details of recommended control sequences.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1 (1h) Power Management (1)	12	SPKOUTL_ENA	0	Speaker Output Enable 0 = Disabled 1 = Enabled
	9	HPOUT1L_ENA	0	Headphone Output (HPOUTL) input stage enable 0 = Disabled 1 = Enabled For pop-free operation, this bit should be set as the first stage of the HPOUTL Enable sequence.
	8	HPOUT1R_ENA	0	Headphone Output (HPOUTR) input stage enable 0 = Disabled 1 = Enabled For pop-free operation, this bit should be set as the first stage of the HPOUTR Enable sequence.
	2:1	VMID_RES [1:0]	00	VMID Divider Enable and Select 00 = VMID disabled (for OFF mode) 01 = 2 x 50k divider (for normal operation) 10 = 2 x 250k divider (for low power standby) 11 = 2 x 5k divider (for fast start-up)
	0	BIAS_ENA	0	Enables the Normal bias current generator (for all analogue functions) 0 = Disabled 1 = Enabled
R2 (02h) Power Management (2)	14	TSHUT_ENA	0	Thermal Sensor Enable 0 = Disabled 1 = Enabled
	13	TSHUT_OPDIS	1	Thermal Shutdown Control (Causes audio outputs to be disabled if an over-temperature occurs. The thermal sensor must also be enabled.) 0 = Disabled 1 = Enabled
	7	IN1A_ENA	0	IN1A Input PGA Enable 0 = Disabled 1 = Enabled
	6	IN1B_ENA	0	IN1B Input PGA Enable 0 = Disabled 1 = Enabled (Note this is only required for single-ended input on the IN1N pin)
	5	IN2A_ENA	0	IN2A Input PGA Enable 0 = Disabled 1 = Enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	4	IN2B_ENA	0	IN2B Input PGA Enable 0 = Disabled 1 = Enabled (Note this is only required for single-ended input on the IN2N pin)
R3 (03h) Power Management (3)	8	SPKLVOL_ENA	0	Speaker PGA Enable 0 = Disabled 1 = Enabled
	5	MIXOUTL_ENA	0	MIXOUTL Headphone Mixer Enable 0 = Disabled 1 = Enabled
	4	MIXOUTR_ENA	0	MIXOUTR Headphone Mixer Enable 0 = Disabled 1 = Enabled
	3	SPKMIX_ENA	0	SPKMIX Speaker Mixer Enable 0 = Disabled 1 = Enabled
R57 (39h) AntiPOP2	2	STARTUP_BIAS_ENA	0	Enables the Start-Up bias current generator 0 = Disabled 1 = Enabled
R70 (46h) Write Sequencer 0	8	WSEQ_ENA	0	Write Sequencer Enable 0 = Disabled 1 = Enabled
R76 (4Ch) Charge Pump 1	15	CP_ENA	0	Charge Pump Control 0 = Disabled 1 = Enabled
R84 (54h) DC Servo 0	1	DCS_ENA_CHAN_1	0	DC Servo enable for HPOUT1L 0 = Disabled 1 = Enabled
	0	DCS_ENA_CHAN_0	0	DC Servo enable for HPOUT1R 0 = Disabled 1 = Enabled

Table 32 Power Management

THERMAL SHUTDOWN

The WM9090 incorporates a temperature sensor which detects when the device temperature is within normal limits or if the device is approaching a hazardous temperature condition.

The temperature status can be polled at any time by reading the TSHUT register bit. The temperature sensor can be configured to automatically disable the audio outputs of the WM9090 in response to an over-temperature condition (approximately 150ºC).

The temperature sensor is enabled by setting the TSHUT_ENA register bit. When the TSHUT_OPDIS is also set, then a device over-temperature condition will cause the speaker output (SPKOUTP and SPKOUTN) to be disabled; this response is likely to prevent any damage to the device attributable to the large currents of the speaker output driver.

When the temperature sensor is enabled, the temperature status can be read from the TSHUT register bit.

Note that, to prevent pops and clicks, TSHUT_ENA and TSHUT_OPDIS should only be updated whilst the speaker and headphone outputs are disabled.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 (02h) Power Management (2)	15	TSHUT (read only)	0	Thermal shutdown status 0 = Normal temperature 1 = Over temperature
	14	TSHUT_ENA	1	Thermal sensor enable 0 = Disabled 1 = Enabled
	13	TSHUT_OPDIS	1	Thermal shutdown control (Causes audio outputs to be disabled if an overtemperature occurs. The thermal sensor must also be enabled.) 0 = Disabled 1 = Enabled

Table 33 Thermal Shutdown

SOFTWARE RESET AND CHIP ID

A Software Reset can be commanded by writing to Register R0. This is a read-only register field and the contents will not be affected by writing to this Register.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R0 (00h) Software Reset	15:0	SW_RESET [15:0]		Writing to this register causes a Software Reset.

Table 34 Chip Reset and ID

REGISTER MAP

Dec Addr	Hex Addr	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Bin Default
0	00	Software Reset	SW_RESET[15:0]																1001_0000_1001_0011
1	01	Power Management (1)	0	0	0	SPKOUTL_ENA	0	0	HPOUT1L_ENA	HPOUT1R_ENA	0	0	0	0	OSC_ENA	VMID_RES[1:0]		BIAS_ENA	0000_0000_P000_0110
2	02	Power Management (2)	TSHUT	TSHUT_ENA	TSHUT_OPDIS	0	0	0	0	0	IN1A_ENA	IN1B_ENA	IN2A_ENA	IN2B_ENA	0	0	0	0	0110_0000_0000_0000
3	03	Power Management (3)	0	AGC_ENA	0	0	0	0	0	SPKLVOL_ENA	0	0	MIXOUTL_ENA	MIXOUTR_ENA	SPKMIX_ENA	0	0	0	0000_0000_0000_0000
6	06	Clocking 1	TOCLK_RATE	TOCLK_ENA	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0000_0001_1100_0000
22	16	IN1 Line Control	0	0	0	0	0	0	0	0	0	0	0	0	0	0	IN1_DIFF	IN1_CLAMP	0000_0000_0000_0011
23	17	IN2 Line Control	0	0	0	0	0	0	0	0	0	0	0	0	0	0	IN2_DIFF	IN2_CLAMP	0000_0000_0000_0011
24	18	IN1 Line Input A Volume	0	0	0	0	0	0	0	IN1_VU	IN1A_MUTE	IN1A_ZC	0	0	0	IN1A_VOL[2:0]			0000_000P_1000_0011
25	19	IN1 Line Input B Volume	0	0	0	0	0	0	0	IN1_VU	IN1B_MUTE	IN1B_ZC	0	0	0	IN1B_VOL[2:0]			0000_000P_1000_0011
26	1A	IN2 Line Input A Volume	0	0	0	0	0	0	0	IN2_VU	IN2A_MUTE	IN2A_ZC	0	0	0	IN2A_VOL[2:0]			0000_000P_1000_0011
27	1B	IN2 Line Input B Volume	0	0	0	0	0	0	0	IN2_VU	IN2B_MUTE	IN2B_ZC	0	0	0	IN2B_VOL[2:0]			0000_000P_1000_0011
28	1C	Left Output Volume	0	0	0	0	0	0	0	HPOUT1_VU	HPOUT1L_ZC	HPOUT1L_MUTE	HPOUT1L_VOL[5:0]						0000_000P_0010_1101
29	1D	Right Output Volume	0	0	0	0	0	0	0	HPOUT1_VU	HPOUT1R_ZC	HPOUT1R_MUTE	HPOUT1R_VOL[5:0]						0000_000P_0010_1101
34	22	SPKMIXL Attenuation	0	0	0	0	0	0	0	SPKMIX_MUTE	IN1A_SPKMIX_VOL[1:0]		IN1B_SPKMIX_VOL[1:0]		IN2A_SPKMIX_VOL[1:0]		IN2B_SPKMIX_VOL[1:0]		0000_0001_0000_0000
36	24	SPKOUT Mixers	0	0	0	0	0	0	0	0	0	0	0	SPKMIXL_TO_SPKOUTL	0	0	0	0	0000_0000_0001_0000
37	25	ClassD3	0	0	0	0	0	0	0	1	0	1	SPKOUTL_BOOST[2:0]		0	0	0	0	0000_0001_0100_0000
38	26	Speaker Volume Left	0	0	0	0	0	0	0	SPKOUT_VU	SPKOUTL_ZC	SPKOUTL_MUTE	SPKOUTL_VOL[5:0]						0000_000P_0011_1001
45	2D	Output Mixer1	0	0	0	0	0	0	0	0	0	IN1A_TO_MIXOUTL	0	0	0	IN2A_TO_MIXOUTL	0	0	0000_0000_0000_0000
46	2E	Output Mixer2	0	0	0	0	0	0	0	0	0	IN1A_TO_MIXOUTR	0	IN1B_TO_MIXOUTR	0	IN2A_TO_MIXOUTR	0	IN2B_TO_MIXOUTR	0000_0000_0000_0000
47	2F	Output Mixer3	0	0	0	0	0	0	0	MIXOUTL_MUTE	IN1A_MIXOUTL_VOL[1:0]		0	0	IN2A_MIXOUTL_VOL[1:0]		0	0	0000_0001_0000_0000
48	30	Output Mixer4	0	0	0	0	0	0	0	MIXOUTR_MUTE	IN1A_MIXOUTR_VOL[1:0]		IN1B_MIXOUTR_VOL[1:0]		IN2A_MIXOUTR_VOL[1:0]		IN2B_MIXOUTR_VOL[1:0]		0000_0001_0000_0000
54	36	Speaker Mixer	0	0	0	0	0	0	0	0	0	IN1A_TO_SPKMIX	0	IN1B_TO_SPKMIX	0	IN2A_TO_SPKMIX	0	IN2B_TO_SPKMIX	0000_0000_0000_0000
57	39	AntiPOP2	0	0	0	0	0	0	0	0	0	0	0	0	VMID_BUF_ENA	1	0	VMID_ENA	0000_0000_0000_1101
66	42	Clocking 4	0	0	0	0	0	0	0	TOCLK_RATE_DIV16	TOCLK_RATE_X4	1	0	1	1	1	1	0	0000_0000_0101_1110

Dec Addr	Hex Addr	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Bin Default
70	46	Write Sequencer 0	0	0	0	0	0	0	0	WSEQ_ENA	0	0	0	0	WSEQ_WRITE_INDEX[3:0]				0000_0000_0000_0000
71	47	Write Sequencer 1	0	WSEQ_DATA_WIDTH[2:0]			WSEQ_DATA_START[3:0]				WSEQ_ADDR[7:0]								0000_0000_0000_0000
72	48	Write Sequencer 2	0	WSEQ_EOS	0	0	WSEQ_DELAY[3:0]				WSEQ_DATA[7:0]								0000_0000_0000_0000
73	49	Write Sequencer 3	0	0	0	0	0	0	WSEQ_ABORT	WSEQ_START	0	0	WSEQ_START_INDEX[5:0]						0000_0000_0000_0000
74	4A	Write Sequencer 4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	WSEQ_BUSY	0000_0000_0000_0000
75	4B	Write Sequencer 5	0	0	0	0	0	0	0	0	0	0	WSEQ_CURRENT_INDEX[5:0]						0000_0000_0000_0000
76	4C	Charge Pump 1	CP_ENA	0	0	1	1	1	1	1	0	0	1	0	0	1	0	1	0001_1111_0010_0101
84	54	DC Servo 0	0	0	DCS_TRIG_SINGLE_1	DCS_TRIG_SINGLE_0	0	0	DCS_TRIG_SERIES_1	DCS_TRIG_SERIES_0	0	0	DCS_TRIG_STARTUP_1	DCS_TRIG_STARTUP_0	DCS_TRIG_DAC_WR_1	DCS_TRIG_DAC_WR_0	DCS_ENA_CHAN_1	DCS_ENA_CHAN_0	00PP_00PP_00PP_PP00
85	55	DC Servo 1	0	0	0	0	DCS_SERIES_NO_01[6:0]						0	DCS_TIMER_PERIOD_01[3:0]					0000_0101_0100_1010
86	56	DC Servo 2	0	0	0	0	1	0	0	0	0	0	0	0	0	1	1	1	0000_1000_0000_0111
87	57	DC Servo 3	DCS_DAC_WR_VAL_1[7:0]										DCS_DAC_WR_VAL_0[7:0]						0000_0000_0000_0000
88	58	DC Servo Readback 0	0	0	0	0	0	0	DCS_CAL_COMPLETE[1:0]		0	0	DCS_DAC_WR_COMPLETE[1:0]		0	0	DCS_STARTUP_COMPLETE[1:0]		0000_0000_0000_0000
89	59	DC Servo Readback 1	0	0	0	0	0	0	0	0	DCS_DAC_WR_VAL_1_RD[7:0]								0000_0000_0000_0000
90	5A	DC Servo Readback 2	0	0	0	0	0	0	0	0	DCS_DAC_WR_VAL_0_RD[7:0]								0000_0000_0000_0000
96	60	Analogue HP 0	0	0	0	0	0	0	0	1	HPOUT1L_RMV_SHORT	HPOUT1L_OUTP	HPOUT1L_DLY	0	HPOUT1R_RMV_SHORT	HPOUT1R_OUTP	HPOUT1R_DLY	0	0000_0001_0000_0000
98	62	AGC Control 0	AGC_CLIP_ENA	0	0	0	AGC_CLIP_THR[3:0]				0	AGC_CLIP_ATK[2:0]			0	AGC_CLIP_DCY[2:0]			1000_0000_0100_0000
99	63	AGC Control 1	AGC_PWR_ENA	1	0	AGC_PWR_AVG	AGC_PWR_THR[3:0]				0	AGC_PWR_ATK[2:0]			0	AGC_PWR_DCY[2:0]			1100_0000_0000_0000
100	64	AGC Control 2	0	0	0	0	0	0	1	AGC_RAMP	0	0	AGC_MINGAIN[5:0]						0000_0010_0000_0000

REGISTER BITS BY ADDRESS

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R0 (00h) Software Reset	15:0	SW_RESET [15:0]		Writing to this register causes a Software Reset.	

Register 00h Software Reset

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1 (01h) Power Management (1)	12	SPKOUTL_ENA	0	Speaker Output Enable 0 = Disabled 1 = Enabled	
	9	HPOUT1L_ENA	0	Headphone Output (HPOUTL) input stage enable 0 = Disabled 1 = Enabled For pop-free operation, this bit should be set as the first stage of the HPOUTL Enable sequence.	
	8	HPOUT1R_ENA	0	Headphone Output (HPOUTR) input stage enable 0 = Disabled 1 = Enabled For pop-free operation, this bit should be set as the first stage of the HPOUTR Enable sequence.	
	3	OSC_ENA	0	CLK_SYS Oscillator Enable 0 = Disabled 1 = Enabled	
	2:1	VMID_RES [1:0]	11	VMID Divider Enable and Select 00 = VMID disabled (for OFF mode) 01 = 2 x 50k divider (for normal operation) 10 = 2 x 250k divider (for low power standby) 11 = 2 x 5k divider (for fast start-up)	
	0	BIAS_ENA	0	Enables the Normal bias current generator (for all analogue functions) 0 = Disabled 1 = Enabled	

Register 01h Power Management (1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R2 (02h) Power Management (2)	15	TSHUT	0	Thermal shutdown status 0 = Normal temperature 1 = Over temperature	
	14	TSHUT_ENA	1	Thermal sensor enable 0 = Disabled 1 = Enabled	
	13	TSHUT_OPDIS	1	Thermal shutdown control (Causes audio outputs to be disabled if an overtemperature occurs. The thermal sensor must also be enabled.) 0 = Disabled 1 = Enabled	
	7	IN1A_ENA	0	IN1A Input PGA Enable 0 = Disabled 1 = Enabled	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	6	IN1B_ENA	0	IN1B Input PGA Enable 0 = Disabled 1 = Enabled (Note this is only required for single-ended input on the IN1N pin)	
	5	IN2A_ENA	0	IN2A Input PGA Enable 0 = Disabled 1 = Enabled	
	4	IN2B_ENA	0	IN2B Input PGA Enable 0 = Disabled 1 = Enabled (Note this is only required for single-ended input on the IN2N pin)	

Register 02h Power Management (2)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R3 (03h) Power Management (3)	14	AGC_ENA	0	AGC Enable 0 = Disabled 1 = Enabled	
	8	SPKLVOL_ENA	0	Speaker PGA Enable 0 = Disabled 1 = Enabled Note that SPKMIXL and SPKLVOL are also enabled when SPKOUTL_ENA is set.	
	5	MIXOUTL_ENA	0	MIXOUTL Headphone Mixer Enable 0 = Disabled 1 = Enabled	
	4	MIXOUTR_ENA	0	MIXOUTR Headphone Mixer Enable 0 = Disabled 1 = Enabled	
	3	SPKMIX_ENA	0	SPKMIX Speaker Mixer Enable 0 = Disabled 1 = Enabled	

Register 03h Power Management (3)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R6 (06h) Clocking 1	15	TOCLK_RATE	0	TOCLK Rate Divider (/2) 0 = f / 2 1 = f / 1	
	14	TOCLK_ENA	0	TOCLK Enable 0 = Disabled 1 = Enabled	

Register 06h Clocking 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R22 (16h) IN1 Line Control	1	IN1_DIFF	1	PGA IN1A and IN1B configuration 0 = Single-ended mode 1 = Differential mode	
	0	IN1_CLAMP	1	IN1P and IN1N input pad VMID clamp 0 = Clamp de-activated 1 = Clamp activated	

Register 16h IN1 Line Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R23 (17h) IN2 Line Control	1	IN2_DIFF	1	PGA IN2A and IN2B configuration 0 = Single-ended mode 1 = Differential mode	
	0	IN2_CLAMP	1	IN2P and IN2N input pad VMID clamp 0 = Clamp de-activated 1 = Clamp activated	

Register 17h IN2 Line Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R24 (18h) IN1 Line Input A Volume	8	IN1_VU	0	IN1 Volume Update Writing a 1 to this bit will cause IN1A and IN1B input PGA volumes to be updated simultaneously	
	7	IN1A_MUTE	1	IN1A PGA Mute 0 = Un-Mute 1 = Mute	
	6	IN1A_ZC	0	IN1A PGA Zero Cross Control 0 = Change gain immediately 1 = Change gain on zero cross only	
	2:0	IN1A_VOL [2:0]	011	IN1A Volume (differential mode) 000 = -6dB 001 = -3.5dB 010 = 0dB 011 = +3.5dB 100 = +6dB 101 = +12dB 110 = +18dB 111 = +18dB IN1A Volume (single-ended mode) 000 = 0dB 001 = +2.5dB 010 = +6dB 011 = +9.5dB 100 = +12dB 101 = +18dB 110 = +24dB 111 = +24dB	

Register 18h IN1 Line Input A Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R25 (19h) IN1 Line Input B Volume	8	IN1_VU	0	IN1 Volume Update Writing a 1 to this bit will cause IN1A and IN1B input PGA volumes to be updated simultaneously	
	7	IN1B_MUTE	1	IN1B PGA Mute 0 = Un-Mute 1 = Mute	
	6	IN1B_ZC	0	IN1B PGA Zero Cross Control 0 = Change gain immediately 1 = Change gain on zero cross only	
	2:0	IN1B_VOL [2:0]	011	IN1B Volume (differential mode) 000 = -6dB 001 = -3.5dB 010 = 0dB 011 = +3.5dB 100 = +6dB 101 = +12dB 110 = +18dB 111 = +18dB IN1B Volume (single-ended mode) 000 = 0dB 001 = +2.5dB 010 = +6dB 011 = +9.5dB 100 = +12dB 101 = +18dB 110 = +24dB 111 = +24dB	

Register 19h IN1 Line Input B Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R26 (1Ah) IN2 Line Input A Volume	8	IN2_VU	0	Input PGA Volume Update Writing a 1 to this bit will cause IN2A and IN2B input PGA volumes to be updated simultaneously	
	7	IN2A_MUTE	1	IN2A PGA Mute 0 = Un-Mute 1 = Mute	
	6	IN2A_ZC	0	IN2A PGA Zero Cross Control 0 = Change gain immediately 1 = Change gain on zero cross only	
	2:0	IN2A_VOL [2:0]	011	IN2A Volume (differential mode) 000 = -6dB 001 = -3.5dB 010 = 0dB 011 = +3.5dB 100 = +6dB 101 = +12dB 110 = +18dB 111 = +18dB IN2A Volume (single-ended mode)	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				000 = 0dB 001 = +2.5dB 010 = +6dB 011 = +9.5dB 100 = +12dB 101 = +18dB 110 = +24dB 111 = +24dB	

Register 1Ah IN2 Line Input A Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R27 (1Bh) IN2 Line Input B Volume	8	IN2_VU	0	Input PGA Volume Update Writing a 1 to this bit will cause IN2A and IN2B input PGA volumes to be updated simultaneously	
	7	IN2B_MUTE	1	IN2B PGA Mute 0 = Un-Mute 1 = Mute	
	6	IN2B_ZC	0	IN2B PGA Zero Cross Control 0 = Change gain immediately 1 = Change gain on zero cross only	
	2:0	IN2B_VOL [2:0]	011	IN2B Volume (differential mode) 000 = -6dB 001 = -3.5dB 010 = 0dB 011 = +3.5dB 100 = +6dB 101 = +12dB 110 = +18dB 111 = +18dB IN2B Volume (single-ended mode) 000 = 0dB 001 = +2.5dB 010 = +6dB 011 = +9.5dB 100 = +12dB 101 = +18dB 110 = +24dB 111 = +24dB	

Register 1Bh IN2 Line Input B Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R28 (1Ch) Left Output Volume	8	HPOUT1_VU	0	Headphone Output PGA Volume Update Writing a 1 to this bit will update HPOUT1LVOL and HPOUT1RVOL volumes simultaneously.	
	7	HPOUT1L_ZC	0	Left Headphone Output PGA Zero Cross Control 0 = Change gain immediately 1 = Change gain on zero cross only	
	6	HPOUT1L_MUTE	0	Left Headphone Output PGA Mute 0 = Un-mute	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				1 = Mute	
	5:0	HPOUT1L_VOL [5:0]	10_1101	Left Headphone Output PGA Volume -57dB to +6dB in 1dB steps	

Register 1Ch Left Output Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R29 (1Dh) Right Output Volume	8	HPOUT1_VU	0	Headphone Output PGA Volume Update Writing a 1 to this bit will update HPOUT1LVOL and HPOUT1RVOL volumes simultaneously.	
	7	HPOUT1R_ZC	0	Right Headphone Output PGA Zero Cross Control 0 = Change gain immediately 1 = Change gain on zero cross only	
	6	HPOUT1R_MUTE	0	Right Headphone Output PGA Mute 0 = Un-mute 1 = Mute	
	5:0	HPOUT1R_VOL [5:0]	10_1101	Right Headphone Output PGA Volume -57dB to +6dB in 1dB steps	

Register 1Dh Right Output Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R34 (22h) SPKMIXL Attenuation	8	SPKMIX_MUTE	1	SPKMIX Output mute 0 = Un-Mute 1 = Mute	
	7:6	IN1A_SPKMIX_VOL [1:0]	00	IN1A to SPKMIX volume control 00 = 0dB 01 = -6dB 10 = -9dB 11 = -12dB	
	5:4	IN1B_SPKMIX_VOL [1:0]	00	IN1B to SPKMIX volume control 00 = 0dB 01 = -6dB 10 = -9dB 11 = -12dB	
	3:2	IN2A_SPKMIX_VOL [1:0]	00	IN2A to SPKMIX volume control 00 = 0dB 01 = -6dB 10 = -9dB 11 = -12dB	
	1:0	IN2B_SPKMIX_VOL [1:0]	00	IN2B to SPKMIX volume control 00 = 0dB 01 = -6dB 10 = -9dB 11 = -12dB	

Register 22h SPKMIXL Attenuation

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R36 (24h) SPKOUT Mixers	4	SPKMIXL_TO_SPKOUTL	1	SPKMIX to Speaker Output enable 0 = Disabled 1 = Enabled	

Register 24h SPKOUT Mixers

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R37 (25h) ClassD3	5:3	SPKOUTL_BOOST [2:0]	000	Speaker Output Gain Boost 000 = 1.00x boost (+0dB) 001 = 1.19x boost (+1.5dB) 010 = 1.41x boost (+3.0dB) 011 = 1.68x boost (+4.5dB) 100 = 2.00x boost (+6.0dB) 101 = 2.37x boost (+7.5dB) 110 = 2.81x boost (+9.0dB) 111 = 3.98x boost (+12.0dB)	

Register 25h ClassD3

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R38 (26h) Speaker Volume Left	8	SPKOUT_VU	0	Speaker Output PGA Volume Update Writing a 1 to this bit will update the SPKOUTL volume.	
	7	SPKOUTL_ZC	0	Speaker Output PGA Zero Cross Control 0 = Change gain immediately 1 = Change gain on zero cross only	
	6	SPKOUTL_MUTE	0	Speaker Output PGA Mute 0 = Un-mute 1 = Mute	
	5:0	SPKOUTL_VOL [5:0]	11_1001	Speaker Output PGA Volume -57dB to +6dB in 1dB steps	

Register 26h Speaker Volume Left

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R45 (2Dh) Output Mixer1	6	IN1A_TO_MIXOUTL	0	IN1A to MIXOUTL enable 0 = Disabled 1 = Enabled	
	2	IN2A_TO_MIXOUTL	0	IN2A to MIXOUTL enable 0 = Disabled 1 = Enabled	

Register 2Dh Output Mixer1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R46 (2Eh) Output Mixer2	6	IN1A_TO_MIXOUTR	0	IN1A to MIXOUTR enable 0 = Disabled 1 = Enabled	
	4	IN1B_TO_MIXOUTR	0	IN1B to MIXOUTR enable 0 = Disabled 1 = Enabled	
	2	IN2A_TO_MIXOUTR	0	IN2A to MIXOUTR enable 0 = Disabled 1 = Enabled	
	0	IN2B_TO_MIXOUTR	0	IN2B to MIXOUTR enable 0 = Disabled 1 = Enabled	

Register 2Eh Output Mixer2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R47 (2Fh) Output Mixer3	8	MIXOUTL_MUTE	1	MIXOUTL Output mute 0 = Un-Mute 1 = Mute	
	7:6	IN1A_MIXOUTL_VOL [1:0]	00	IN1A to MIXOUTL volume control 00 = 0dB 01 = -6dB 10 = -9dB 11 = -12dB	
	3:2	IN2A_MIXOUTL_VOL [1:0]	00	IN2A to MIXOUTL volume control 00 = 0dB 01 = -6dB 10 = -9dB 11 = -12dB	

Register 2Fh Output Mixer3

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R48 (30h) Output Mixer4	8	MIXOUTR_MUTE	1	MIXOUTR Output mute 0 = Un-Mute 1 = Mute	
	7:6	IN1A_MIXOUTR_VOL [1:0]	00	IN1A to MIXOUTR volume control 00 = 0dB 01 = -6dB 10 = -9dB 11 = -12dB	
	5:4	IN1B_MIXOUTR_VOL [1:0]	00	IN1B to MIXOUTR volume control 00 = 0dB 01 = -6dB 10 = -9dB 11 = -12dB	
	3:2	IN2A_MIXOUTR_VOL [1:0]	00	IN2A to MIXOUTR volume control 00 = 0dB 01 = -6dB 10 = -9dB 11 = -12dB	
	1:0	IN2B_MIXOUT	00	IN2B to MIXOUTR volume control	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
		R_VOL [1:0]		00 = 0dB 01 = -6dB 10 = -9dB 11 = -12dB	

Register 30h Output Mixer4

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R54 (36h) Speaker Mixer	6	IN1A_TO_SPKMIX	0	IN1A to SPKMIX enable 0 = Disabled 1 = Enabled	
	4	IN1B_TO_SPKMIX	0	IN1B to SPKMIX enable 0 = Disabled 1 = Enabled	
	2	IN2A_TO_SPKMIX	0	IN2A to SPKMIX enable 0 = Disabled 1 = Enabled	
	0	IN2B_TO_SPKMIX	0	IN2B to SPKMIX enable 0 = Disabled 1 = Enabled	

Register 36h Speaker Mixer

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R57 (39h) AntiPOP2	3	VMID_BUF_ENA	1	VMID Buffer Enable 0 = Disabled 1 = Enabled	
	0	VMID_ENA	1	Enable VMID master bias current source 0 = Disabled 1 = Enabled	

Register 39h AntiPOP2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R70 (46h) Write Sequencer 0	8	WSEQ_ENA	0	Write Sequencer Enable. 0 = Disabled 1 = Enabled	
	3:0	WSEQ_WRITE_INDEX [3:0]	0000	Sequence Write Index. This is the memory location to which any updates to R71 and R72 will be copied. 0 to 15 = RAM addresses	

Register 46h Write Sequencer 0

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R71 (47h) Write Sequencer 1	14:12	WSEQ_DATA_ WIDTH [2:0]	000	Width of the data block written in this sequence step. 000 = 1 bit 001 = 2 bits 010 = 3 bits 011 = 4 bits 100 = 5 bits 101 = 6 bits 110 = 7 bits 111 = 8 bits	
	11:8	WSEQ_DATA_ START [3:0]	0000	Bit position of the LSB of the data block written in this sequence step. 0000 = Bit 0 … 1111 = Bit 15	
	7:0	WSEQ_ADDR [7:0]	0000_0000	Control Register Address to be written to in this sequence step.	

Register 47h Write Sequencer 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R72 (48h) Write Sequencer 2	14	WSEQ_EOS	0	End of Sequence flag. This bit indicates whether the Control Write Sequencer should stop after executing this step. 0 = Not end of sequence 1 = End of sequence (Stop the sequencer after this step).	
	11:8	WSEQ_DELAY [3:0]	0000	Time delay after executing this step. Total time per step (including execution) = 62.5us × (2^WSEQ_DELAY + 8)	
	7:0	WSEQ_DATA [7:0]	0000_0000	Data to be written in this sequence step. When the data width is less than 8 bits, then one or more of the MSBs of WSEQ_DATA are ignored. It is recommended that unused bits be set to 0.	

Register 48h Write Sequencer 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R73 (49h) Write Sequencer 3	9	WSEQ_ABOR T	0	Writing a 1 to this bit aborts the current sequence and returns control of the device back to the serial control interface.	
	8	WSEQ_START	0	Writing a 1 to this bit starts the write sequencer at the memory location indicated by the WSEQ_START_INDEX field. The sequence continues until it reaches an “End of sequence” flag. At the end of the sequence, this bit will be reset by the Write Sequencer.	
	5:0	WSEQ_START _INDEX [5:0]	00_0000	Sequence Start Index. This is the memory location of the first command in the selected sequence. 0 to 15 = RAM addresses 16 to 58 = ROM addresses 59 to 63 = Reserved	

Register 49h Write Sequencer 3

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R74 (4Ah) Write Sequencer 4	0	WSEQ_BUSY	0	Sequencer Busy flag (Read Only). 0 = Sequencer idle 1 = Sequencer busy Note: it is not possible to write to control registers via the control interface while the Sequencer is Busy.	

Register 4Ah Write Sequencer 4

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R75 (4Bh) Write Sequencer 5	5:0	WSEQ_CURRENT_INDEX [5:0]	00_0000	Sequence Current Index. This is the location of the most recently accessed command in the write sequencer memory.	

Register 4Bh Write Sequencer 5

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R76 (4Ch) Charge Pump 1	15	CP_ENA	0	Charge Pump Control 0 = Disabled 1 = Enabled	

Register 4Ch Charge Pump 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R84 (54h) DC Servo 0	13	DCS_TRIG_SINGLE_1	0	Writing 1 to this bit selects a single DC offset correction for HPOUT1L. In readback, a value of 1 indicates that the DC Servo single correction is in progress.	
	12	DCS_TRIG_SINGLE_0	0	Writing 1 to this bit selects a single DC offset correction for HPOUT1R. In readback, a value of 1 indicates that the DC Servo single correction is in progress.	
	9	DCS_TRIG_SERIES_1	0	Writing 1 to this bit selects a series of DC offset corrections for HPOUT1L. In readback, a value of 1 indicates that the DC Servo DAC Write correction is in progress.	
	8	DCS_TRIG_SERIES_0	0	Writing 1 to this bit selects a series of DC offset corrections for HPOUT1R. In readback, a value of 1 indicates that the DC Servo DAC Write correction is in progress.	
	5	DCS_TRIG_STARTUP_1	0	Writing 1 to this bit selects Start-Up DC Servo mode for HPOUT1L. In readback, a value of 1 indicates that the DC Servo Start-Up correction is in progress.	
	4	DCS_TRIG_STARTUP_0	0	Writing 1 to this bit selects Start-Up DC Servo mode for HPOUT1R. In readback, a value of 1 indicates that the DC Servo Start-Up correction is in progress.	
	3	DCS_TRIG_DAC_WR_1	0	Writing 1 to this bit selects DAC Write DC Servo mode for HPOUT1L. In readback, a value of 1 indicates that the DC Servo DAC Write correction is in progress.	
	2	DCS_TRIG_DAC_WR_0	0	Writing 1 to this bit selects DAC Write DC Servo mode for HPOUT1R.	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				In readback, a value of 1 indicates that the DC Servo DAC Write correction is in progress.	
	1	DCS_ENA_CHAN_1	0	DC Servo enable for HPOUT1L 0 = Disabled 1 = Enabled	
	0	DCS_ENA_CHAN_0	0	DC Servo enable for HPOUT1R 0 = Disabled 1 = Enabled	

Register 54h DC Servo 0

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R85 (55h) DC Servo 1	11:5	DCS_SERIES_NO_01 [6:0]	010_1010	Number of DC Servo updates to perform in a series event. 0 = 1 updates 1 = 2 updates ... 127 = 128 updates	
	3:0	DCS_TIMER_PERIOD_01 [3:0]	1010	Time between periodic updates. Time is calculated as 0.256s x (2^PERIOD) 0000 = Off 0001 = 0.52s 1010 = 266s (4min 26s) 1111 = 8519s (2hr 22s)	

Register 55h DC Servo 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R87 (57h) DC Servo 3	15:8	DCS_DAC_WR_VAL_1 [7:0]	0000_0000	DC Offset value for HPOUT1L in DAC Write DC Servo mode. Two's complement format. LSB is 0.25mV. Range is +/-32mV	
	7:0	DCS_DAC_WR_VAL_0 [7:0]	0000_0000	DC Offset value for HPOUT1R in DAC Write DC Servo mode. Two's complement format. LSB is 0.25mV. Range is +/-32mV	

Register 57h DC Servo 3

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R88 (58h) DC Servo Readback 0	9:8	DCS_CAL_COMPLETE [1:0]	00	DC Servo Complete status 00 = DAC Write or Start-Up DC Servo mode not completed. 01 = DAC Write or Start-Up DC Servo mode complete on HPOUT1R only. 10 = DAC Write or Start-Up DC Servo mode complete on HPOUT1L only. 11 = DAC Write or Start-Up DC Servo mode complete on HPOUT1L and HPOUT1R.	
	5:4	DCS_DAC_W	00	DC Servo DAC Write status	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
		R_COMPLETE [1:0]		00 = DAC Write DC Servo mode not completed. 01 = DAC Write DC Servo mode complete on HPOUT1R only. 10 = DAC Write DC Servo mode complete on HPOUT1L only. 11 = DAC Write DC Servo mode complete on HPOUT1L and HPOUT1R.	
	1:0	DCS_STARTUP_COMPLETE [1:0]	00	DC Servo Start-Up status 00 = Start-Up DC Servo mode not completed. 01 = Start-Up DC Servo mode complete on HPOUT1R only. 10 = Start-Up DC Servo mode complete on HPOUT1L only. 11 = Start-Up DC Servo mode complete on HPOUT1L and HPOUT1R.	

Register 58h DC Servo Readback 0

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R89 (59h) DC Servo Readback 1	7:0	DCS_DAC_WR_VAL_1_RD [7:0]	0000_0000	Readback value for HPOUT1L. Two's complement format. LSB is 0.25mV. Range is +/-32mV	

Register 59h DC Servo Readback 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R90 (5Ah) DC Servo Readback 2	7:0	DCS_DAC_WR_VAL_0_RD [7:0]	0000_0000	Readback value for HPOUT1R. Two's complement format. LSB is 0.25mV. Range is +/-32mV	

Register 5Ah DC Servo Readback 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R96 (60h) Analogue HP 0	7	HPOUT1L_RMV_SHORT	0	Removes HPOUT1L short 0 = HPOUT1L short enabled 1 = HPOUT1L short removed For pop-free operation, this bit should be set to 1 as the final step in the HPOUTL Enable sequence.	
	6	HPOUT1L_OUTP	0	Enables HPOUT1L output stage 0 = Disabled 1 = Enabled For pop-free operation, this bit should be set to 1 after the DC offset cancellation has been performed.	
	5	HPOUT1L_DLY	0	Enables HPOUT1L intermediate stage 0 = Disabled 1 = Enabled For pop-free operation, this bit should be set to 1 after the output signal path has been configured, and before the DC Offset cancellation is scheduled This bit should be set with at least 20us delay after HPOUT1L_ENA.	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	3	HPOUT1R_RMV_SHORT	0	Removes HPOUT1R short 0 = HPOUT1R short enabled 1 = HPOUT1R short removed For pop-free operation, this bit should be set to 1 as the final step in the HPOUTR Enable sequence.	
	2	HPOUT1R_OUTP	0	Enables HPOUT1R output stage 0 = Disabled 1 = Enabled For pop-free operation, this bit should be set to 1 after the DC offset cancellation has been performed.	
	1	HPOUT1R_DLY	0	Enables HPOUT1R intermediate stage 0 = Disabled 1 = Enabled For pop-free operation, this bit should be set to 1 after the output signal path has been configured, and before the DC Offset cancellation is scheduled This bit should be set with at least 20us delay after HPOUT1L_ENA.	

Register 60h Analogue HP 0

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R98 (62h) AGC Control 0	15	AGC_CLIP_ENA	1	Enable AGC Anti-Clip Mode 0 = Disabled 1 = Enabled	
	11:8	AGC_CLIP_THR [3:0]	0110	AGC Anti-Clip Threshold Sets the headroom between SPKPGA output and SPKVDD at which Anti-Clip limiting will be applied 0000 = -200mV 0001 = -150mV 0010 = -100mV 0011 = -50mV 0100 = 0mV 0101 = 50mV 0110 = 100mV 0111 = 150mV 1000 = 200mV 1001 = 250mV 1010 = 300mV 1011 = 400mV 1100 = 500mV 1101 = 600mV 1110 = 700mV 1111 = 800mV	
	6:4	AGC_CLIP_ATK [2:0]	100	AGC Anti-Clip Attack Rate Sets the rate of AGC gain reduction when clipping is detected 000 = 0.6ms/6dB 001 = 5.4ms/6dB 010 = 10.2ms/6dB 011 = 15.0ms/6dB 100 = 19.8ms/6dB 101 = 24.6ms/6dB 110 = 29.4ms/6dB 111 = 34.1ms/6dB	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	2:0	AGC_CLIP_DCY [2:0]	000	AGC Anti-Clip Decay Rate Sets the rate of AGC gain increments after a period of clipping 000 = 120ms/6dB 001 = 480ms/6dB 010 = 820ms/6dB 011 = 1170ms/6dB 100 = 1640ms/6dB 101 = 2050ms/6dB 110 = 2730ms/6dB 111 = 4100ms/6dB	

Register 62h AGC Control 0

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R99 (63h) AGC Control 1	15	AGC_PWR_ENA	1	Enable AGC Power Limit Mode 0 = Disabled 1 = Enabled	
	12	AGC_PWR_AVG	0	AGC Power Measurement mode 0 = Peak power 1 = RMS power	
	11:8	AGC_PWR_THR [2:0]	0000	AGC Power Limit Threshold Sets the output level at which Power limiting will be applied. Assumes RMS power mode and 8ohm speaker. 0000 = 300mW 0001 = 350mW 0010 = 400mW 0011 = 450mW 0100 = 500mW 0101 = 550mW 0110 = 600mW 0111 = 650mW 1000 = 700mW 1001 = 750mW 1010 = 800mW 1011 = 850mW 1100 = 900mW 1101 = 950mW 1110 = 1000mW 1111 = 1050mW	
	6:4	AGC_PWR_ATK [2:0]	000	AGC Power Limiting Attack Rate Sets the rate of AGC gain reduction when power limiting is applied 000 = 120ms/6dB 001 = 480ms/6dB 010 = 840ms/6dB 011 = 1200ms/6dB 100 = 1680ms/6dB 101 = 2040ms/6dB 110 = 2760ms/6dB 111 = 4080ms/6dB	
	2:0	AGC_PWR_DCY [2:0]	000	AGC Power Limiting Decay Rate Sets the rate of AGC gain increments after a period of	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				power limiting 000 = 1080ms/6dB 001 = 1200ms/6dB 010 = 1320ms/6dB 011 = 1680ms/6dB 100 = 2040ms/6dB 101 = 2760ms/6dB 110 = 4080ms/6dB 111 = 8160ms/6dB	

Register 63h AGC Control 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R100 (64h) AGC Control 2	8	AGC_RAMP	0	AGC Ramp Control Selects how the AGC gain adjustment is applied 0 = Multiple gains steps per zero-cross 1 = Single gain step per zero-cross	
	5:0	AGC_MINGAIN [5:0]	00_0000	AGC Minimum Gain -57dB to +6dB in 1dB steps	

Register 64h AGC Control 2

APPLICATIONS INFORMATION

RECOMMENDED EXTERNAL COMPONENTS

Figure 17 below provides a summary of recommended external components for WM9090. Note that the diagram does not include any components that are specific to the end application e.g. they do not include filtering on the speaker outputs (assume filterless class D operation), RF decoupling, or RF filtering for pins which connect to the external world i.e. headphone or speaker outputs.

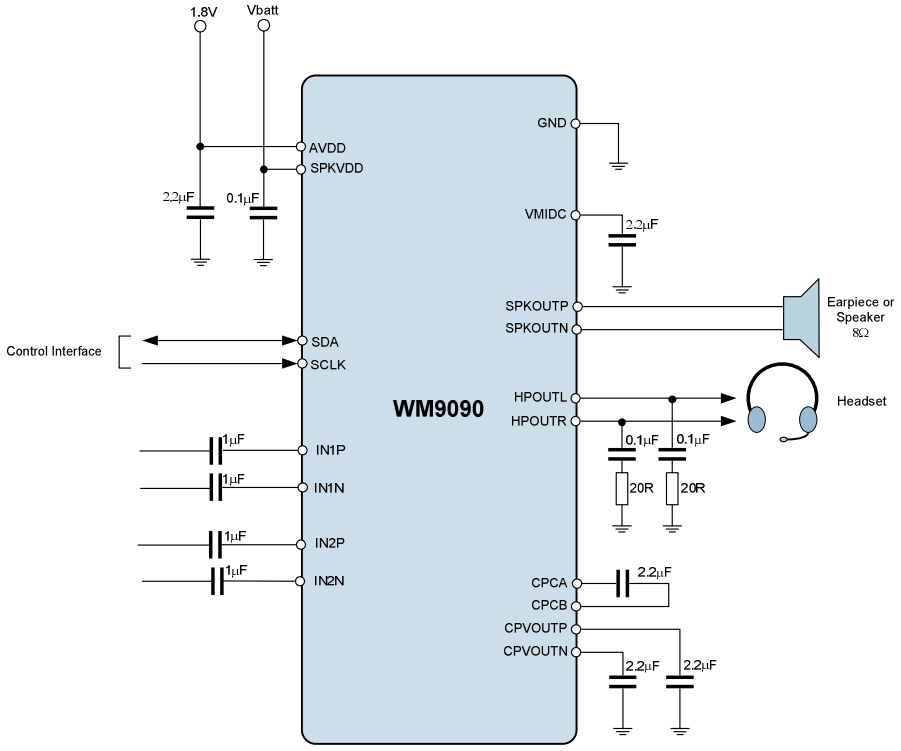
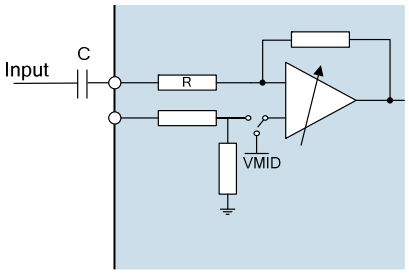


Figure 17 Recommended External Components

AUDIO INPUT PATHS

The WM9090 provides 4 analogue audio inputs. Each of these inputs is referenced to the internal DC reference, VMID. A DC blocking capacitor is required for each input pin used in the target application. The choice of capacitor is determined by the filter that is formed between that capacitor and the input impedance of the input pin. The circuit is illustrated in Figure 18.



$$Fc = \frac{1}{2\pi RC}$$

Fc = high pass 3dB cut-off frequency

Figure 18 Audio Input Path DC Blocking Capacitor

If the input impedance is known, and the cut-off frequency is known, then the minimum capacitor value may be derived easily. However, it can be seen from the representation in Figure 18 that the input impedance is not fixed in all applications but can vary with gain and boost amplifier settings. The choice of capacitor for a 20Hz cut-off frequency is shown in Table 35 for different input impedance conditions. The applicable input impedance can be found in the "Electrical Characteristics" section of this datasheet.

INPUT IMPEDANCE	MINIMUM CAPACITANCE FOR 20HZ PASS BAND
2kΩ	4 µF
15kΩ	0.5 µF
30kΩ	0.27 µF
60kΩ	0.13 µF

Table 35 Audio Input DC Blocking Capacitors

Using the figures in Table 35, it follows that a 1µF capacitance for all input connections will give good results in most cases. Tantalum electrolytic capacitors are particularly suitable as they offer high stability in a small package size.

Ceramic equivalents are a cost effective alternative to the superior tantalum packages, but care must be taken to ensure the desired capacitance is maintained at the AVDD operating voltage. Also, ceramic capacitors may show microphonic effects, where vibrations and mechanical conditions give rise to electrical signals. This is particularly problematic for microphone input paths where a large signal gain is required.

A single capacitor is required for a line input or single-ended microphone connection. In the case of a differential connection, a DC blocking capacitor is required on both input pins.

POWER SUPPLY DECOUPLING

Electrical coupling exists particularly in digital logic systems where switching in one sub-system causes fluctuations on the power supply. This effect occurs because the inductance of the power supply acts in opposition to the changes in current flow that are caused by the logic switching. The resultant variations (or 'spikes') in the power supply voltage can cause malfunctions and unintentional behavior in other components. A decoupling (or 'bypass') capacitor can be used as an energy storage component which will provide power to the decoupled circuit for the duration of these power supply variations, protecting it from malfunctions that could otherwise arise.

Coupling also occurs in a lower frequency form when ripple is present on the power supply rail caused by changes in the load current or by limitations of the power supply regulation method. In audio components such as the WM9090, these variations can alter the performance of the signal path, leading to degradation in signal quality. A decoupling (or 'bypass') capacitor can be used to filter these effects, by presenting the ripple voltage with a low impedance path that does not affect the circuit to be decoupled.

These coupling effects are addressed by placing a capacitor between the supply rail and the corresponding ground reference. In the case of systems comprising multiple power supply rails, decoupling should be provided on each rail.

The recommended power supply decoupling capacitors for WM9090 are listed below in Table 36.

POWER SUPPLY	DECOUPLING CAPACITOR
AVDD	2.2µF ceramic
SPKVDD	0.1µF ceramic (see note)
VMIDC	2.2µF ceramic (see text below)

Table 36 Power Supply Decoupling Capacitors

Note: 0.1µF is required with 2.2µF a guide to the total required power rail capacitance.

All decoupling capacitors should be placed as close as possible to the WM9090 device. The connection between GND, the AVDD decoupling capacitor and the main system ground should be made at a single point as close as possible to the GND ball of the WM9090.

The VMID capacitor is not, technically, a decoupling capacitor. However, it does serve a similar purpose in filtering noise on the VMID reference. The connection between GND, the VMID decoupling capacitor and the main system ground should be made at a single point as close as possible to the GND ball of the WM9090.

Due to the wide tolerance of many types of ceramic capacitors, care must be taken to ensure that the selected components provide the required capacitance across the required temperature and voltage ranges in the intended application. For most application the use of ceramic capacitors with capacitor dielectric X5R is recommended.

HEADPHONE OUTPUT PATH

The headphone output on WM9090 is ground referenced and therefore does not require the large, expensive capacitors necessary for VMID-referenced solutions. For best audio performance, it is recommended to connect a zobel network to the audio output pins. This network should comprise of a 100nF capacitor and 20ohm resistor in series with each other (see "Analogue Outputs" section). These components have the effect of dampening high frequency oscillations or instabilities that can arise outside the audio band under certain conditions. Possible sources of these instabilities include the inductive load of a headphone coil or an active load in the form of an external line amplifier.

CLASS D SPEAKER CONNECTIONS

The WM9090 incorporates a Class D speaker driver. As the Class D output is a pulse width modulated (PWM) signal, the choice of speakers and tracking of signals is critical for ensuring good performance and reducing EMI in this mode.

The efficiency of the speaker drivers is affected by the series resistance between the WM9090 and the speaker (e.g. PCB track loss and inductor ESR) as shown in Figure 19. This resistance should be as low as possible to maximise efficiency.

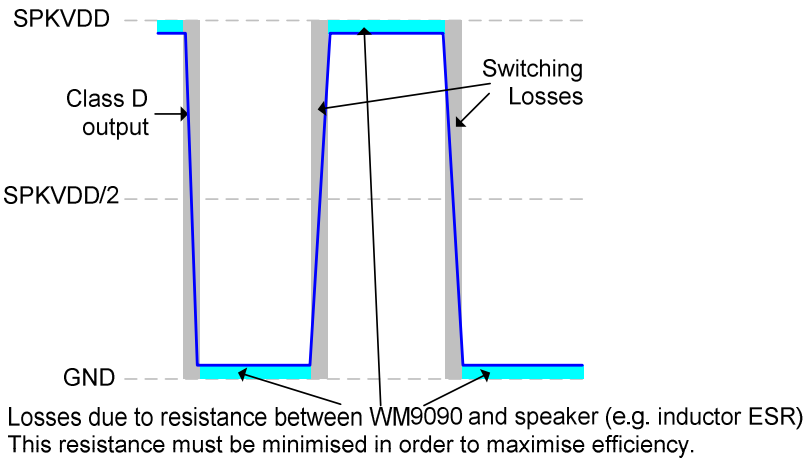


Figure 19 Speaker Connection Losses

The Class D output requires external filtering in order to recreate the audio signal. This may be implemented using a 2nd order LC or 1st order RC filter, or else may be achieved by using a loudspeaker whose internal inductance provides the required filter response. An LC or RC filter should be used if the loudspeaker characteristics are unknown or unsuitable, or if the length of the loudspeaker connection is likely to lead to EMI problems.

In applications where it is necessary to provide Class D filter components, a 2nd order LC filter is the recommended solution as it provides more attenuation at higher frequencies and minimises power dissipated in the filter when compared to a first order RC filter (lower ESR). This maximises both rejection of unwanted switching frequencies and overall speaker efficiency. A suitable implementation is illustrated in Figure 20.

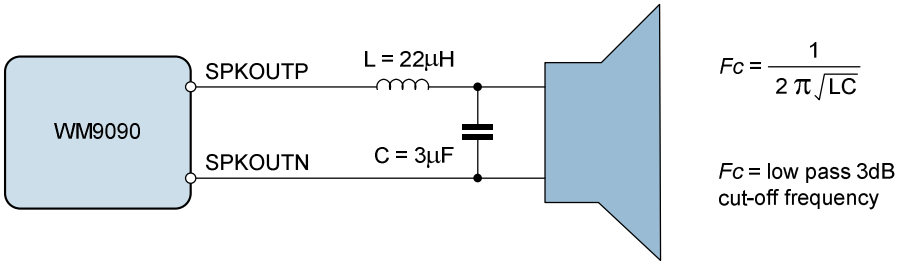
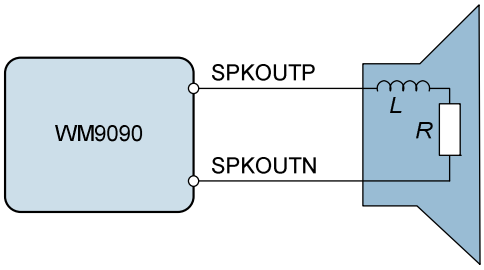


Figure 20 Class D Output Filter Components

A simple equivalent circuit of a loudspeaker consists of a serially connected resistor and inductor, as shown in Figure 21. This circuit provides a low pass filter for the speaker output. If the loudspeaker characteristics are suitable, then the loudspeaker itself can be used in place of the filter components described earlier. This is known as 'filterless' operation.



$$Fc = \frac{R}{2\pi L}$$

Fc = low pass 3dB cut-off frequency

Figure 21 Speaker Equivalent Circuit for Filterless Operation

For filterless Class D operation, it is important to ensure that a speaker with suitable inductance is chosen. For example, if we know the speaker impedance is 8Ω and the desired cut-off frequency is 20kHz, then the optimum speaker inductance may be calculated as:

$$L = \frac{R}{2\pi Fc} = \frac{8\Omega}{2\pi * 20kHz} = 64\mu H$$

8Ω loudspeakers typically have an inductance in the range 20μH to 100μH, however, it should be noted that a loudspeaker inductance will not be constant across the relevant frequencies for Class D operation (up to and beyond the Class D switching frequency). Care should be taken to ensure that the cut-off frequency of the loudspeaker's filtering is low enough to suppress the high frequency energy of the Class D switching and, in so doing, to prevent speaker damage. The Class D outputs of the WM9090 operate at much higher frequencies than is recommended for most speakers and it must be ensured that the cut-off frequency is low enough to protect the speaker.

PCB LAYOUT CONSIDERATIONS

Poor PCB layout will degrade the performance and be a contributory factor in EMI, ground bounce and resistive voltage losses. All external components should be placed as close to the WM9090 device as possible, with current loop areas kept as small as possible. Specific factors relating to Class D loudspeaker connection are detailed below.

CLASS D LOUDSPEAKER CONNECTION

Long, exposed PCB tracks or connection wires will emit EMI. The distance between the WM9090 and the loudspeaker should therefore be kept as short as possible. Where speakers are connected to the PCB via a cable form, it is recommended that a shielded twisted pair cable is used. The shield should be connected to the main system, with care taken to ensure ground loops are avoided.

Further reduction in EMI can be achieved using PCB ground (or VDD) planes and also by using passive LC components to filter the Class D switching waveform. When passive filtering is used, low ESR components should be chosen in order to minimise the series resistance between the WM9090 and the speaker, maximising the power efficiency.

LC passive filtering will usually be effective at reducing EMI at frequencies up to around 30MHz. To reduce emissions at higher frequencies, ferrite beads can also be used. These should be positioned as close to the device as possible.

These techniques for EMI reduction are illustrated in Figure 22.

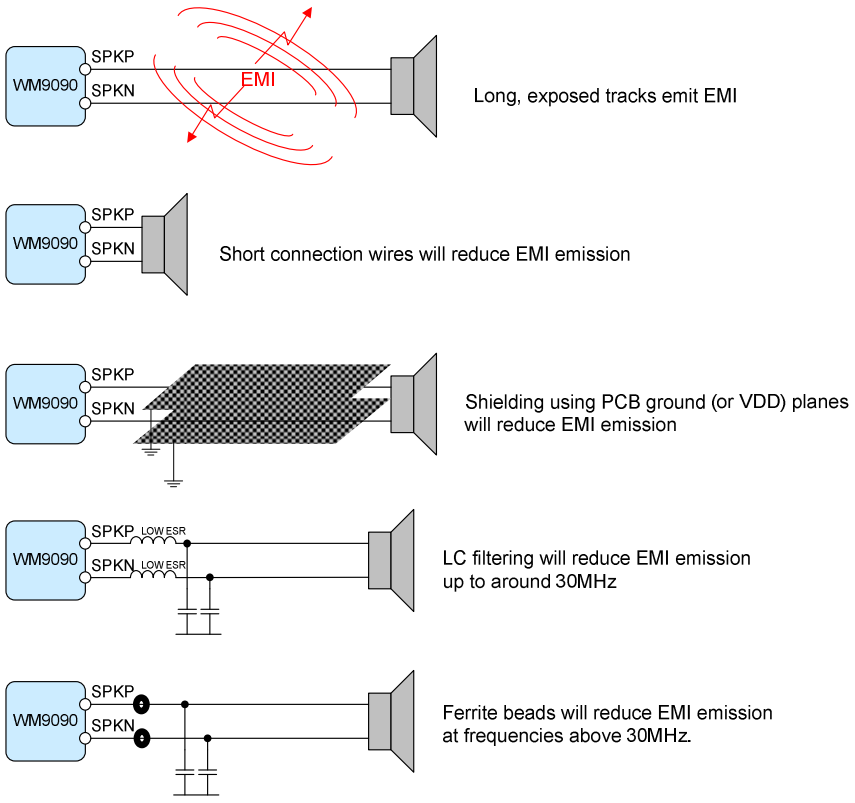
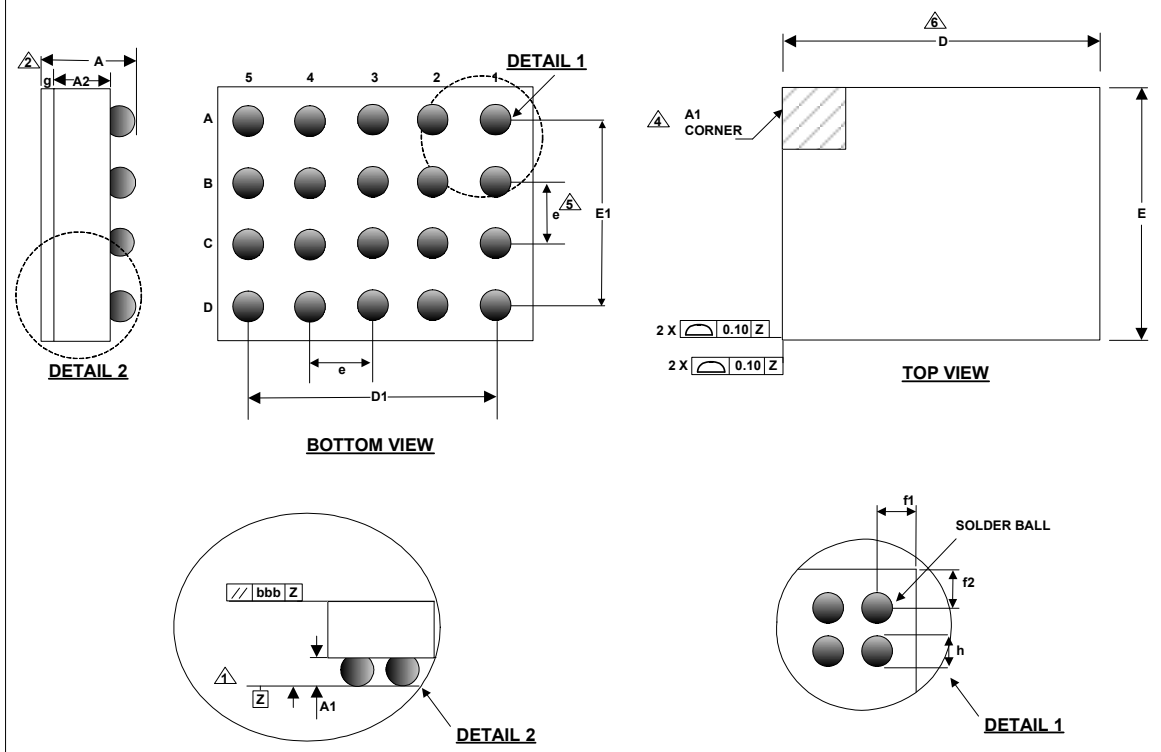


Figure 22 EMI Reduction Techniques

PACKAGE DIMENSIONS

B: 20 BALL W-CSP PACKAGE 2.530 x 2.070 x 0.7mm BODY, 0.50 mm BALL PITCH **DM073.A**



Symbols	Dimensions (mm)			
	MIN	NOM	MAX	NOTE
A	0.615	0.700	0.785	
A1	0.219	0.244	0.269	
A2	0.361	0.386	0.411	
D	2.500	2.530	2.560	
D1		2.000 BSC		
E	2.040	2.070	2.100	
E1		1.500 BSC		
e		0.500 BSC		5
f1	0.250			
f2	0.270			
g	0.035	0.070	0.105	
h		0.314 BSC		

NOTES:
1. PRIMARY DATUM -Z- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
2. THIS DIMENSION INCLUDES STAND-OFF HEIGHT 'A1' AND BACKSIDE COATING.
3. A1 CORNER IS IDENTIFIED BY INK/LASER MARK ON TOP PACKAGE.
4. BILATERAL TOLERANCE ZONE IS APPLIED TO EACH SIDE OF THE PACKAGE BODY.
5. 'e' REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
6. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
7. FOLLOWS JEDEC DESIGN GUIDE MO-211-C.

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ADDRESS:

Wolfson Microelectronics plc

26 Westfield Road

Edinburgh

EH11 2QB

United Kingdom

Tel :: +44 (0)131 272 7000

Fax :: +44 (0)131 272 7001

Email :: sales@wolfsonmicro.com