

24-bit, 192kHz 6-Channel CODEC with Volume Control

DESCRIPTION

The WM8772 is a multi-channel audio CODEC ideal for DVD and surround sound processing applications for home hi-fi, automotive and other audio visual equipment.

A stereo 24-bit multi-bit sigma delta ADC is used. Digital audio output word lengths from 16-32 bits and sampling rates from 32kHz to 96kHz are supported.

Three stereo 24-bit multi-bit sigma delta DACs are used with oversampling digital interpolation filters. Digital audio input word lengths from 16-32 bits and sampling rates from 8kHz to 192kHz are supported. Each DAC channel has independent digital volume and mute control.

The audio data interface supports I²S, left justified, right justified and DSP digital audio formats.

The device is controlled via a 3 wire serial interface. The interface provides access to all features including channel selection, volume controls, mutes, de-emphasis and power management facilities.

The device is available in a 28 lead SSOP.

The device is available over a functional temperature range of -40°C to +85°C

FEATURES

- Audio Performance
 - 100dB SNR ('A' weighted @ 48kHz) DAC
 - 98dB SNR ('A' weighted @ 48kHz) ADC
- DAC Sampling Frequency: 8kHz 192kHz
- ADC Sampling Frequency: 32kHz 96kHz
- 3-Wire SPI Serial or Hardware Control Interface
- Programmable Audio Data Interface Modes
 - I²S, Left, Right Justified or DSP
 - 16/20/24/32 bit Word Lengths
- Three Independent stereo DAC outputs with independent digital volume controls
- Master or Slave Audio Data Interface
- 3.0V to 5.5V Analogue, 3.0V to 3.6V Digital supply Operation
- 28 lead SSOP Package

APPLICATIONS

- DVD Players
- Surround Sound AV Processors and Hi-Fi systems
- Automotive Audio

BLOCK DIAGRAM

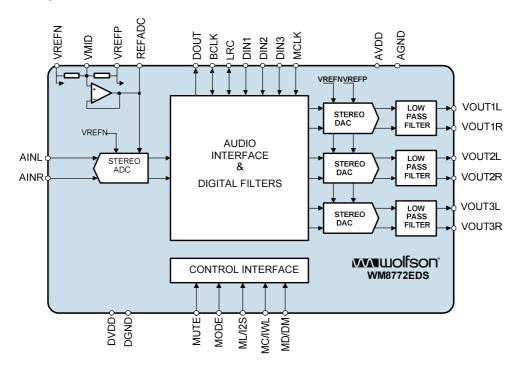
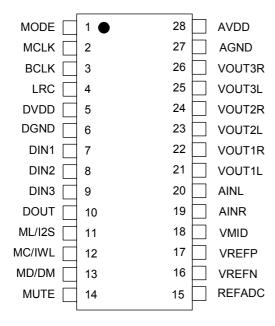


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PIN CONFIGURATION



ORDERING INFORMATION

| DEVICE | TEMPERATURE RANGE | PACKAGE | MOISTURE SENSITIVITY LEVEL | PEAK SOLDERING TEMPERATURE |
|---------------|----------------------|---|-------------------------------|-------------------------------|
| WM8772SEDS/V | -40 to +85°C | 28-lead SSOP (Pb free) | MSL3 | 260°C |
| WM8772SEDS/RV | -40 to +85°C | 28-lead SSOP (Pb free, tape and reel) | MSL3 | 260°C |

Note:

1. Reel quantity = 2,000

PIN DESCRIPTION

| PIN | NAME | TYPE | DESCRIPTION |
|-----|--------|----------------------|--|
| 1 | MODE | Digital input | Control format selection |
| | | | 0 = Software control |
| | | | 1 = Hardware control |
| 2 | MCLK | Digital input | Master clock; 256, 384, 512 or 768fs (fs = word clock frequency) |
| | | | (combined ADCMCLK and DACMCLK) |
| 3 | BCLK | Digital input/output | Audio interface bit clock (combined ADCBCLK and DACBCLK) |
| 4 | LRC | Digital input/output | Audio left/right word clock (combined ADCLRC and DACLRC) |
| 5 | DVDD | Supply | Digital positive supply |
| 6 | DGND | Supply | Digital negative supply |
| 7 | DIN1 | Digital input | DAC channel 1 data input |
| 8 | DIN2 | Digital input | DAC channel 2 data input |
| 9 | DIN3 | Digital input | DAC channel 3 data input |
| 10 | DOUT | Digital output | ADC data output |
| 11 | ML/I2S | Digital input | Software Mode: Serial interface Latch signal |
| | | | Hardware Mode: Input Audio Data Format |
| 12 | MC/IWL | Digital input | Software Mode: Serial control interface clock |
| | | | Hardware Mode: Audio data input word length |
| 13 | MD/DM | Digital input | Software Mode: Serial interface data |
| | | | Hardware Mode: De-emphasis selection |
| 14 | MUTE | Digital input/output | DAC Zero Flag output or DAC mute input |
| 15 | REFADC | Analogue output | ADC reference buffer decoupling pin; 10uF external decoupling |
| 16 | VREFN | Supply | ADC and DAC negative supply |
| 17 | VREFP | Supply | DAC positive reference supply |
| 18 | VMID | Analogue output | Midrail divider decoupling pin; 10uF external decoupling |
| 19 | AINR | Analogue input | ADC right input |
| 20 | AINL | Analogue input | ADC left input |
| 21 | VOUT1L | Analogue output | DAC channel 1 left output |
| 22 | VOUT1R | Analogue output | DAC channel 1 right output |
| 23 | VOUT2L | Analogue output | DAC channel 2 left output |
| 24 | VOUT2R | Analogue output | DAC channel 2 right output |
| 25 | VOUT3L | Analogue output | DAC channel 3 left output |
| 26 | VOUT3R | Analogue output | DAC channel 3 right output |
| 27 | AGND | Supply | Analogue negative supply and substrate connection |
| 28 | AVDD | Supply | Analogue positive supply |

Note: Digital input pins have Schmitt trigger input buffers.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.



ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.

MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

| CONDITION | MIN | MAX |
|---|------------|--------------------------------------|
| Digital supply voltage | -0.3V | +5V |
| Analogue supply voltage | -0.3V | +7V |
| Voltage range digital inputs ¹ | DGND -0.3V | DVDD +0.3V |
| Voltage range analogue inputs ¹ | AGND -0.3V | AVDD +0.3V |
| Master Clock Frequency | | 37MHz |
| Operating temperature range, - T _A | -40°C | +85°C |
| Storage temperature after soldering | -65°C | +150°C |
| Package body temperature (soldering 10 seconds) | | Refer to Ordering Information, p3 |
| Package body temperature (soldering 2 minutes) | | +183°C |

Notes:

1. Analogue and digital grounds must always be within 0.3V of each other.



RECOMMENDED OPERATING CONDITIONS

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------|-------------------|-----------------|------|-----|------|------|
| Digital supply range | DVDD | | 3.0 | | 3.6 | V |
| Analogue supply range | AVDD, VREFP | | 3.0 | | 5.5 | V |
| Ground | AGND, VREFN, DGND | | | 0 | | V |
| Difference DGND to AGND | | | -0.3 | 0 | +0.3 | V |

Note: Digital supply DVDD must never be more than 0.3V greater than AVDD.

ELECTRICAL CHARACTERISTICS

Test Conditions

AVDD, VREFP = 5V, DVDD = 3.3V, AGND, VREFN = 0V, DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs, ADC/DAC in Slave Mode unless otherwise stated.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------------|--------|---|-----|---------|-----|------------------|
| DAC Output (Load = 10kΩ, 50pF) | | | | | | • |
| 0dBFs Full scale output voltage | | | | 1.0 x | | V _{rms} |
| | | | | VREFP/5 | | |
| DAC Performance (+25°C) | | | | | | • |
| SNR (Note 1,2,4) | | A-weighted, | 95 | 100 | | dB |
| | | @ fs = 48kHz | | | | |
| SNR (Note 1,2,4) | | A-weighted | | 99 | | dB |
| | | @ fs = 96kHz | | | | |
| SNR (Note 1,2,4) | | A-weighted | | 98 | | dB |
| | | @ fs = 192kHz | | | | |
| SNR (Note 1,2,4) | | A-weighted | | 96 | | dB |
| | | @ fs = 48kHz, AVDD = | | | | |
| | | 3.3V | | | | |
| SNR (Note 1,2,4) | | A-weighted | | 96 | | dB |
| | | @ fs = 96kHz, AVDD = | | | | |
| | | 3.3V | | | | |
| Dynamic Range (Note 2,4) | DNR | A-weighted, -60dB full scale input | 90 | 100 | | dB |
| Total Harmonic Distortion (THD) | | 1kHz, 0dB.Fs | | -90 | -80 | dB |
| Mute Attenuation | | 1kHz Input, 0dB gain | | 100 | -00 | dB |
| | | TKT IZ ITIPUL, OUB GAIT | | 100 | | dВ |
| DAC channel separation | PSRR | 1k∐z 100m\/ | | 50 | | dВ |
| Power Supply Rejection Ratio | FORK | 1kHz 100mV _{p-p} 20Hz to 20kHz | | - | | |
| | | | | 45 | | dB |
| | | 100mV _{p-p} | | | | |



Test Conditions

AVDD, VREFP = 5V, DVDD = 3.3V, AGND, VREFN = 0V, DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs, ADC/DAC in Slave Mode unless otherwise stated.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------------------|-------------------|---------------------------------|-------------------|----------|-------------------|------------------|
| ADC Performance (+25°C) | | | | | | |
| Input Signal Level (0dB) | | | | 2.0 x | | V_{rms} |
| | | | | REFADC/5 | | |
| Input resistance | | | | 20 | | kΩ |
| Input capacitance | | | | 10 | | pF |
| SNR (Note 1,2,4) | | A-weighted, 0dB gain | 80 | 98 | | dB |
| | | @ fs = 48kHz | | | | |
| SNR (Note 1,2,4) | | A-weighted, 0dB gain | | 98 | | dB |
| | | @ fs = 96kHz | | | | |
| | | 64 x OSR | | | | |
| SNR (Note 1,2,4) | | A-weighted, 0dB gain | | 93 | | dB |
| | | @ fs = 48kHz, AVDD = | | | | |
| | | 3.3V | | | 1 | |
| SNR (Note 1,2,4) | | A-weighted, 0dB gain | | 93 | 1 | dB |
| | | @ fs = 96kHz, AVDD | | | 1 | |
| | | = 3.3V | | | | |
| | | 64 x OSR | | | + | |
| Total Harmonic Distortion (THD) | | 1kHz, -1dBFs | | -81 | | dB |
| | | | | | | |
| Dynamic Range | DNR | -60dBFS | | -98 | | dB |
| ADC Channel Separation | | 1kHz Input | | 90 | + | dB |
| Mute Attenuation | _ | 1kHz Input, 0dB gain | | 90 | | dB |
| Power Supply Rejection Ratio | PSRR | 1kHz 100mVpp | | 50 | | dB |
| | | 20Hz to 20kHz | | 45 | | dB |
| District Lawis Lawels (CMCC Law | -1-) | 100mVpp | | | | |
| Digital Logic Levels (CMOS Level | | 1 | | | 0.0 DV/DD | |
| Input LOW level | V _{IL} | | 0.7 | | 0.3 x DVDD | V |
| Input HIGH level | V _{IH} | | 0.7 x DVDD | .00 | 1 | V |
| Input leakage current | | | | ±0.2 | ±1 | μA |
| Input capacitance | | | | 5 | 1 | pF |
| Output LOW | V _{OL} | I _{OL} =1mA | | | 0.1 x DVDD | V |
| Output HIGH | V_{OH} | I _{OH} = -1mA | 0.9 x DVDD | | | V |
| Analogue Reference Levels | Г | | | Γ | <u> </u> | |
| Reference voltage | V _{VMID} | | VREFP/2 – 50mV | VREFP/2 | VREFP/2 + 50mV | V |
| Potential divider resistance | R_{VMID} | VREFP to VMID and VMID to VREFN | | 70 | | kΩ |
| Supply Current | | | | | | |
| Analogue supply current | | AVDD, VREFP = 5V | | 37 | | mA |
| Digital supply current | | DVDD = 3.3V | | 14 | | mA |

Notes:

- Ratio of output level with 1kHz full scale input, to the output level with all zeros into the digital input, measured 'A' weighted.
- All performance measurements done with 20kHz low pass filter, and where noted an A-weight filter. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.
- 3. VMID decoupled with 10uF and 0.1uF capacitors (smaller values may result in reduced performance).

TERMINOLOGY

1. Signal-to-noise ratio (dB) - SNR is a measure of the difference in level between the full scale output and the output with no signal applied. (No Auto-zero or Automute function is employed in achieving these results).

- 2. Dynamic range (dB) DNR is a measure of the difference between the highest and lowest portions of a signal. Normally a THD+N measurement at 60dB below full scale. The measured signal is then corrected by adding the 60dB to it. (e.g. THD+N @ -60dB= -32dB, DR= 92dB).
- 3. THD+N (dB) THD+N is a ratio, of the rms values, of (Noise + Distortion)/Signal.
- 4. Stop band attenuation (dB) Is the degree to which the frequency spectrum is attenuated (outside audio band).
- 5. Channel Separation (dB) Also known as Cross-Talk. This is a measure of the amount one channel is isolated from the other. Normally measured by sending a full scale signal down one channel and measuring the other.
- 6. Pass-Band Ripple Any variation of the frequency response in the pass-band region.

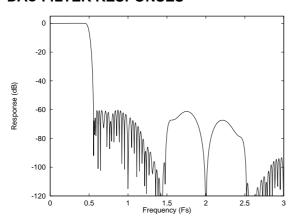


DIGITAL FILTER CHARACTERISTICS

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------|-----------------|----------|---------|----------|------|
| | ADC Fi | lter | | | |
| Passband | ±0.01 dB | 0 | | 0.4535fs | |
| | -6dB | | 0.5fs | | |
| Passband ripple | | | | ±0.01 | dB |
| Stopband | | 0.5465fs | | | |
| Stopband Attenuation | f > 0.5465fs | -65 | | | dB |
| | DAC Fi | lter | | | |
| Passband | ±0.05 dB | | | 0.444fs | |
| | -3dB | | 0.487fs | | |
| Passband ripple | | | | ±0.05 | dB |
| Stopband | | 0.555fs | | | |
| Stopband Attenuation | f > 0.555fs | -60 | | | dB |

Table 1 Digital Filter Characteristics

DAC FILTER RESPONSES



0.2 0.15 0.1 0.05 0.

Figure 1 DAC Digital Filter Frequency Response
- 44.1, 48 and 96KHz

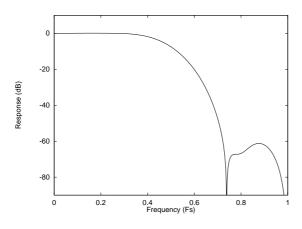


Figure 2 DAC Digital Filter Ripple -44.1, 48 and 96kHz

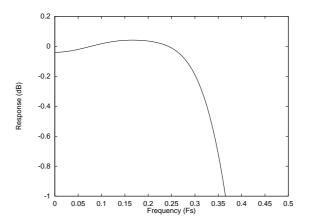
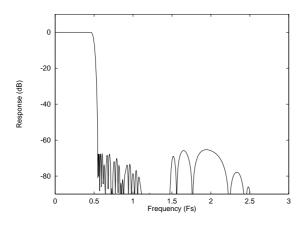


Figure 3 DAC Digital Filter Frequency Response
- 192KHz

Figure 4 DAC Digital Filter Ripple – 192kHz



ADC FILTER RESPONSES



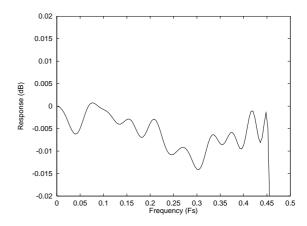


Figure 5 ADC Digital Filter Frequency Response

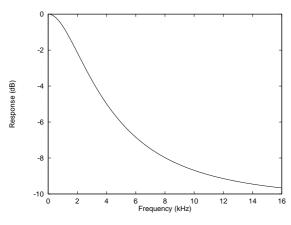
Figure 6 ADC Digital Filter Ripple

ADC HIGH PASS FILTER

The WM8772 has a selectable digital high pass filter to remove DC offsets. The filter response is characterised by the following polynomial.

$$H(z) = \frac{1 - z^{-1}}{1 - 0.9995z^{-1}}$$

DIGITAL DE-EMPHASIS CHARACTERISTICS



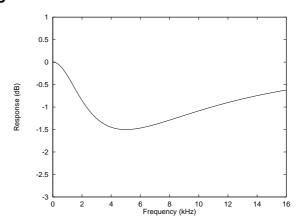
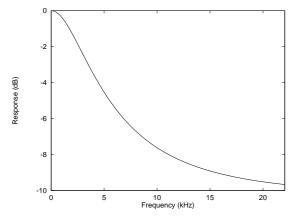


Figure 7 De-Emphasis Frequency Response (32kHz)

Figure 8 De-Emphasis Error (32KHz)



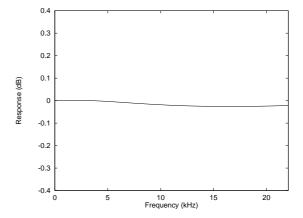
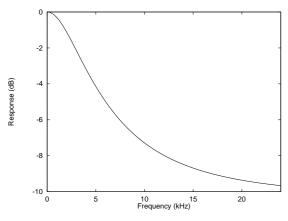


Figure 9 De-Emphasis Frequency Response (44.1KHz)

Figure 10 De-Emphasis Error (44.1KHz)



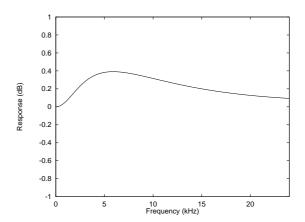


Figure 11 De-Emphasis Frequency Response (48kHz)

Figure 12 De-Emphasis Error (48kHz)

MASTER CLOCK TIMING

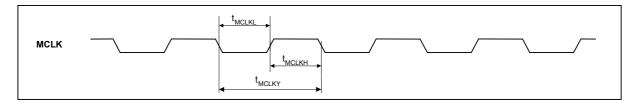


Figure 13 ADC and DAC Master Clock Timing Requirements

Test Conditions

AVDD, VREFP = 5V, DVDD = 3.3V, AGND, VREFN = 0V, AGND, DGND = 0V, T_A = +25°C, fs = 48kHz, DACMCLK and ADCMCLK = 256fs unless otherwise stated.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------------|--------------------|-----------------|-------|-----|-------|------|
| System Clock Timing Information | on | | | | | |
| MCLK System clock pulse width high | t _{MCLKH} | | 11 | | | ns |
| MCLK System clock pulse width low | t _{MCLKL} | | 11 | | | ns |
| MCLK System clock cycle time | t _{MCLKY} | | 28 | | | ns |
| MCLK Duty cycle | | | 40:60 | | 60:40 | |

Table 2 Master Clock Timing Requirements

DIGITAL AUDIO INTERFACE - MASTER MODE

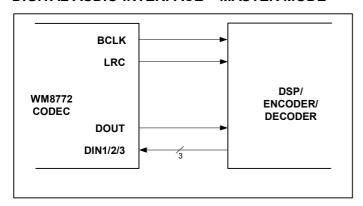


Figure 14 Audio Interface - Master Mode

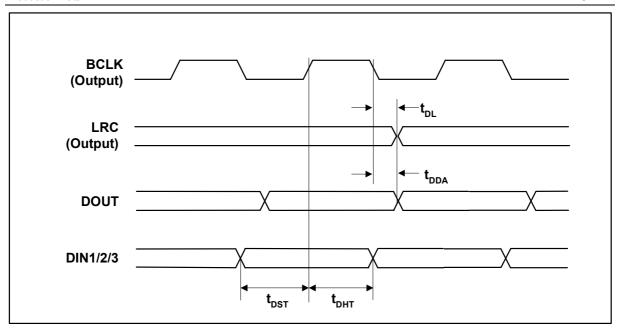


Figure 15 Digital Audio Data Timing - Master Mode

Test Conditions

AVDD, VREFP = 5V, DVDD = 3.3V, AGND, VREFN, DGND = 0V, T_A = $+25^{\circ}C$, Master Mode, fs = 48kHz, MCLK = 256fs unless otherwise stated.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT | | | |
|---|-------------------------------------|-----------------|-----|-----|-----|------|--|--|--|
| Audio Data Input Timing Info | Audio Data Input Timing Information | | | | | | | | |
| LRC propagation delay from BCLK falling edge | t _{DL} | | 0 | | 10 | ns | | | |
| DOUT propagation delay from BCLK falling edge | t _{DDA} | | 0 | | 10 | ns | | | |
| DIN1/2/3 setup time to BCLK rising edge | t _{DST} | | 10 | | | ns | | | |
| DIN1/2/3 hold time from BCLK rising edge | t _{DHT} | | 10 | | | ns | | | |

Table 3 Digital Audio Data Timing - Master Mode

DIGITAL AUDIO INTERFACE - SLAVE MODE

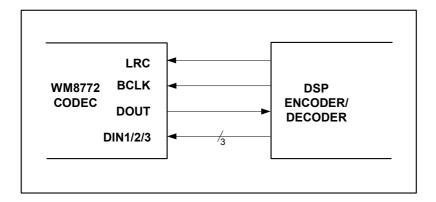


Figure 16 Audio Interface - Slave Mode

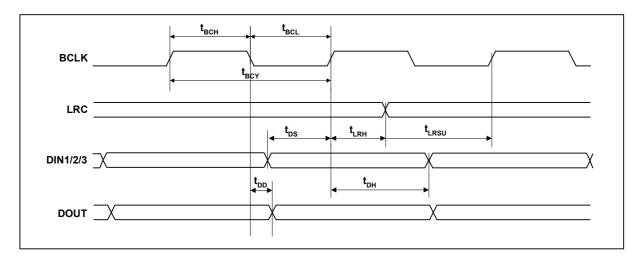


Figure 17 Digital Audio Data Timing - Slave Mode

Test Conditions

AVDD = 5V, DVDD = 3.3V, AGND = 0V, DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, MCLK = 256fs unless otherwise stated.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|-------------------|-----------------|-----|-----|-----|------|
| Audio Data Input Timing In | formation | | | | | |
| BCLK cycle time | t _{BCY} | | 50 | | | ns |
| BCLK pulse width high | t _{BCH} | | 20 | | | ns |
| BCLK pulse width low | t _{BCL} | | 20 | | | ns |
| LRC set-up time to BCLK rising edge | t _{LRSU} | | 10 | | | ns |
| LRC hold time from BCLK rising edge | t _{LRH} | | 10 | | | ns |
| DIN1/2/3 set-up time to BCLK rising edge | t _{DS} | | 10 | | | ns |
| DIN1/2/3 hold time from BCLK rising edge | t _{DH} | | 10 | | | ns |
| DOUT propagation delay from BCLK falling edge | t _{DD} | | 0 | | 10 | ns |

Table 4 Digital Audio Data Timing - Slave Mode



MPU INTERFACE TIMING

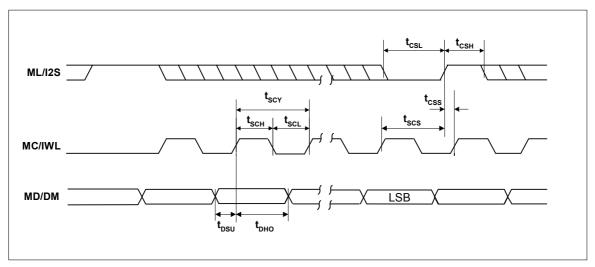


Figure 18 SPI Compatible Control Interface Input Timing

Test Conditions

AVDD = 5V, DVDD = 3.3V, AGND, DGND = 0V, $T_A = +25^{\circ}C$, fs = 48kHz, DACMCLK and ADCMCLK = 256fs unless otherwise stated

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT |
|--|------------------|-----|-----|-----|------|
| MC/IWL rising edge to ML/I2S rising edge | tscs | 60 | | | ns |
| MC/IWL pulse cycle time | t _{scy} | 80 | | | ns |
| MC/IWL pulse width low | t _{SCL} | 30 | | | ns |
| MC/IWL pulse width high | tscн | 30 | | | ns |
| MD/DM to MC/IWL set-up time | t _{DSU} | 20 | | | ns |
| MC/IWL to MD/DM hold time | t _{DHO} | 20 | | | ns |
| ML/I2S pulse width low | t _{CSL} | 20 | | | ns |
| ML/I2S pulse width high | t _{CSH} | 20 | | | ns |
| ML/I2S rising to MC/IWL rising | t _{CSS} | 20 | | | ns |

Table 5 3-Wire SPI Compatible Control Interface Input Timing Information

DEVICE DESCRIPTION

INTRODUCTION

WM8772 is a complete 6-channel DAC, 2-channel ADC audio CODEC, including digital interpolation and decimation filters, multi-bit sigma delta stereo ADC, and switched capacitor multi-bit sigma delta DACs with digital volume controls on each channel and output smoothing filters.

The device is implemented as three separate stereo DACs and a stereo ADC in a single package and controlled by a single interface.

Each stereo DAC has its own data input DIN1/2/3, the stereo ADC has it's own data output DOUT. The word clock LRC, bit clock BCLK and master clock MCLK are shared between them.

The Audio Interface may be configured to operate in either master or slave mode. In Slave mode LRC and BCLK are all inputs. In Master mode LRC and BCLK are all outputs.

Each DAC has its own digital volume control that is adjustable in 0.5dB steps. The digital volume controls may be operated independently. In addition, a zero cross detect circuit is provided for each DAC for the digital volume controls. The digital volume control detects a transition through the zero point before updating the volume. This minimises audible clicks and 'zipper' noise as the gain values change.

Control of internal functionality of the device is by 3-wire serial or pin programmable control interface. The software control interface may be asynchronous to the audio data interface as control data will be re-synchronised to the audio processing internally.

Operation using master clocks of 128fs, 192fs, 256fs, 384fs, 512fs or 768fs is provided for the DAC, for operation of both the ADC and DAC master clocks of 256fs, 384fs, 512fs and 768fs is provided. In Slave mode selection between clock rates is automatically controlled. In master mode, the sample rate is set by control bits RATE. Audio sample rates (fs) from less than 8ks/s up to 192ks/s are allowed for the DAC and from less than 32ks/s up to 96ks/s for the ADC, provided the appropriate master clock is input.

The audio data interface supports right, left and I²S interface formats along with a highly flexible DSP serial port interface.

AUDIO DATA SAMPLING RATES

In a typical digital audio system there is only one central clock source producing a reference clock to which all audio data processing is synchronised. This clock is often referred to as the audio system's Master Clock. The external master system clock can be applied directly through the MCLK input pin with no software configuration necessary. In a system where there are a number of possible sources for the reference clock it is recommended that the clock source with the lowest jitter be used to optimise the performance of the ADC and DAC.

The master clock for WM8772 supports audio sampling rates from 128fs to 768fs, where fs is the audio sampling frequency (LRC) typically 32kHz, 44.1kHz, 48kHz, 96kHz or 192kHz (for DAC operation only). For ADC operation sample rates from 256fs to 768fs are supported. The master clock is used to operate the digital filters and the noise shaping circuits.

In Slave mode the WM8772 has a master clock detection circuit that automatically determines the relationship between the system clock frequency and the sampling rate (to within +/- 32 master clocks). If there is a greater than 32 clocks error the interface defaults to 768fs mode. The master clocks must be synchronised with LRC, although the WM8772 is tolerant of phase variations or jitter on this clock. Table 6 shows the typical master clock frequency inputs for the WM8772.

The signal processing for the WM8772 typically operates at an oversampling rate of 128fs for both ADC and DAC. The exception to this for the DAC is for operation with a 128/192fs system clock, e.g. for 192kHz operation, when the oversampling rate is 64fs. For ADC operation at 96kHz it is recommended that the user set the ADCOSR bit. This changes the ADC signal processing oversample rate to 64fs.



| SAMPLING RATE | System Clock Frequency (MHz) | | | | | | | | | |
|------------------|------------------------------|--------|-------------|-------------|-------------|-------------|--|--|--|--|
| (LRC) | 128fs | 192fs | 192fs 256fs | | 512fs 768fs | | | | | |
| 32kHz | 4.096 | 6.144 | 8.192 | 12.288 | 16.384 | 24.576 | | | | |
| 44.1kHz | 5.6448 | 8.467 | 11.2896 | 16.9340 | 22.5792 | 33.8688 | | | | |
| 48kHz | 6.144 | 9.216 | 12.288 | 18.432 | 24.576 | 36.864 | | | | |
| 96kHz | 12.288 | 18.432 | 24.576 | 36.864 | Unavailable | Unavailable | | | | |
| 192kHz | 24.576 | 36.864 | Unavailable | Unavailable | Unavailable | Unavailable | | | | |

Table 6 System Clock Frequencies Versus Sampling Rate (ADC does not support 128fs and 192fs)

HARDWARE CONTROL MODES

When the MODE pin is held high, the following hardware modes of operation are available.

Note: When in hardware mode the ADC and DAC will only run in slave mode.

MUTE AND AUTOMUTE OPERATION

In both hardware and software modes, MUTE controls the selection of MUTE directly, and can be used to enable and disable the automute function. This pin becomes an output when left floating and indicates infinite ZERO detect (IZD) has been detected.

| | DESCRIPTION | | | | | | |
|----------|---|--|--|--|--|--|--|
| 0 | Normal Operation | | | | | | |
| 1 | Mute DAC channels | | | | | | |
| Floating | Enable IZD, MUTE becomes an output to indicate when IZD occurs. | | | | | | |
| | L=IZD detected, H=IZD not detected. | | | | | | |

Table 7 Mute and Automute Control

Figure 19 shows the application and release of MUTE whilst a full amplitude sinusoid is being played at 48kHz sampling rate. When MUTE (lower trace) is asserted, the output (upper trace) begins to decay exponentially from the DC level of the last input sample. The output will decay towards V_{MID} with a time constant of approximately 64 input samples. If MUTE is applied to all channels for 1024 or more input samples the outputs will be connected directly to V_{MID} if IZD is set. When MUTE is deasserted, the output will restart immediately from the current input sample.

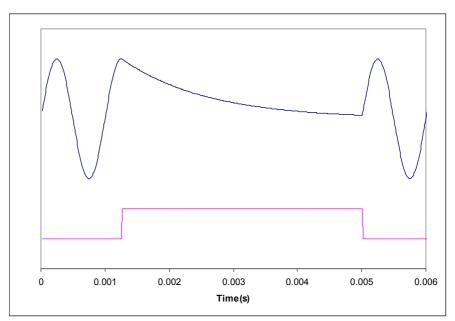


Figure 19 Application and Release of Soft Mute



The MUTE pin is an input to select mute or not mute. MUTE is active high; taking the pin high causes the filters to soft mute, ramping down the audio signal over a few milliseconds. Taking MUTE low again allows data into the filter.

The automute function detects a series of ZERO value audio samples of 1024 samples long being applied to both channels. After such an event, a latch is set whose output (AUTOMUTED) is wire OR'ed through a $10k\Omega$ resistor to the MUTE pin. Thus if the MUTE pin is not being driven, the automute function will assert mute.

If MUTE is tied low, AUTOMUTED is overridden and will not mute unless the IZD register bit is set. If MUTE is driven from a bi-directional source, then both MUTE and automute functions are available. If MUTE is not driven, AUTOMUTED appears as a weak output ($10k\Omega$ source impedance) and can be used to drive external mute circuits. AUTOMUTED will be removed as soon as any channel receives a non-ZERO input.

A diagram showing how the various Mute modes interact is shown below Figure 20.

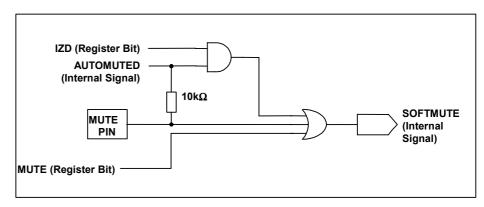


Figure 20 Selection Logic for MUTE Modes

INPUT FORMAT SELECTION

In hardware mode, ML/I2S and MC/IWL become input controls for selection of input data format type and input data word length for both the ADC and DAC.

| ML/I2S | MC/IWL | INPUT DATA MODE |
|--------|--------|-------------------------|
| 0 | 0 | 24-bit right justified |
| 0 | 1 | 20-bit right justified |
| 1 | 0 | 16-bit I ² S |
| 1 | 1 | 24-bit I ² S |

Table 8 Input Format Selection

Note:

In 24 bit I²S mode, any width of 24 bits or less is supported provided that the left/right clocks (LRC) are high for a minimum of 24 bit clocks (BCLK) and low for a minimum of 24 bit clocks.

DE-EMPHASIS CONTROL

In hardware mode, the MD/DM pin becomes an input control for selection of de-emphasis filtering to be applied.

| MD/DM | DE-EMPHASIS |
|-------|-------------|
| 0 | Off |
| 1 | On |

Table 9 De-emphasis Control



DIGITAL AUDIO INTERFACE

MASTER AND SLAVE MODES

The audio interface operates in either Slave or Master mode, selectable using the MS control bit. In both Master and Slave modes DIN1/2/3 are always inputs to the WM8772 and DOUT is always an output. The default is Slave mode.

In Slave mode, LRC and BCLK are inputs to the WM8772 (Figure 21). DIN1/2/3 and LRC are sampled by the WM8772 on the rising edge of BCLK. ADC data is output on DOUT and changes on the falling edge of BCLK.

By setting the control bit BCP the polarity of BCLK may be reversed so that DIN1/2/3 and LRC are sampled on the falling edge of BCLK and DOUT changes on the rising edge of BCLK.

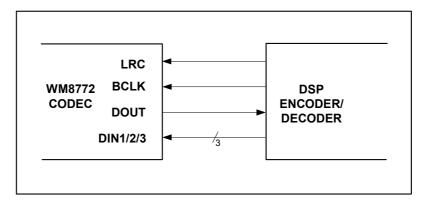


Figure 21 Slave Mode

In Master mode, LRC and BCLK are outputs from the WM8772 (Figure 22). LRC and BCLK are generated by the WM8772. DIN1/2/3 are sampled by the WM8772 on the rising edge of BCLK so the controller must output DAC data that changes on the falling edge of BCLK. ADC data is output on DOUT and changes on the falling edge of BCLK.

By setting control bit BCP the polarity of BCLK may be reversed so that DIN1/2/3 are sampled on the falling edge of BCLK, and DOUT changes on the rising edge of BCLK.

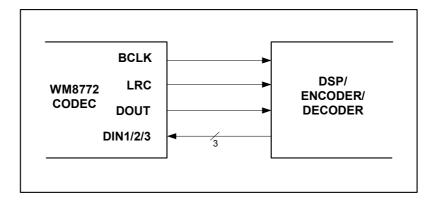


Figure 22 Master Mode

AUDIO INTERFACE FORMATS

Audio data is applied to the internal DAC filters, or output from the ADC filters, via the Digital Audio Interface. 5 popular interface formats are supported:

- Left Justified mode
- · Right Justified mode
- I²S mode
- DSP mode A
- DSP mode B

All 5 formats send the MSB first and support word lengths of 16, 20, 24 and 32 bits, with the exception of 32 bit right justified mode, which is not supported.

In left justified, right justified and I²S modes, the digital audio interface receives DAC data on the DIN1/2/3 inputs and outputs ADC data on DOUT. Audio Data for each stereo channel is time multiplexed with LRC indicating whether the left or right channel is present. LRC is also used as a timing reference to indicate the beginning or end of the data words.

In left justified, right justified and I²S modes, the minimum number of BCLKs per LRC period is 2 times the selected word length. LRC must be high for a minimum of word length BCLKs and low for a minimum of word length BCLKs. Any mark to space ratio on LRC is acceptable provided the above requirements are met.

In DSP mode A or Mode B, all 6 DAC channels are time multiplexed onto DIN1. LRC is used as a frame sync signal to identify the MSB of the first word. The minimum number of BCLKs per LRC period is 6 times the selected word length. Any mark to space ratio is acceptable on LRC provided the rising edge is correctly positioned. The ADC data may also be output in DSP mode A or mode B, with LRC used as a frame sync to identify the MSB of the first word. The minimum number of BCLKs per LRC period is 2 times the selected word length if only the ADC is being operated.

LEFT JUSTIFIED MODE

In left justified mode, the MSB of DIN1/2/3 is sampled by the WM8772 on the first rising edge of BCLK following a LRC transition. The MSB of the ADC data is output on DOUT and changes on the same falling edge of BCLK as LRC and may be sampled on the rising edge of BCLK. LRC is high during the left samples and low during the right samples (Figure 23).

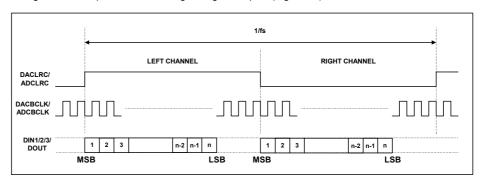


Figure 23 Left Justified Mode Timing Diagram



RIGHT JUSTIFIED MODE

In right justified mode, the LSB of DIN1/2/3 is sampled by the WM8772 on the rising edge of BCLK preceding a LRC transition. The LSB of the ADC data is output on DOUT and changes on the falling edge of BCLK preceding a LRC transition and may be sampled on the rising edge of BCLK. LRC are high during the left samples and low during the right samples (Figure 24).

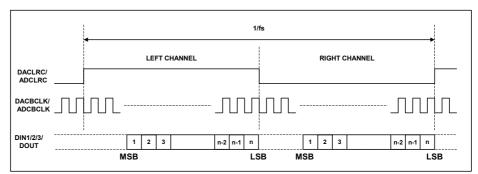


Figure 24 Right Justified Mode Timing Diagram

I2S MODE

In I^2S mode, the MSB of DIN1/2/3 is sampled by the WM8772 on the second rising edge of BCLK following a LRC transition. The MSB of the ADC data is output on DOUT and changes on the first falling edge of BCLK following an LRC transition and may be sampled on the rising edge of BCLK. LRC are low during the left samples and high during the right samples.

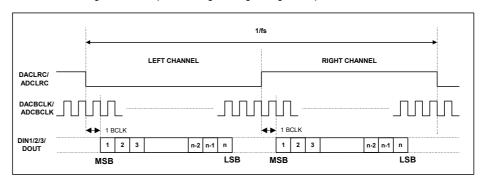


Figure 25 I²S Mode Timing Diagram

DSP MODE A

In DSP mode A, the MSB of DAC channel 1 left data is sampled by the WM8772 on the second rising edge on BCLK following a LRC rising edge. DAC channel 1 right and DAC channels 2 and 3 data follow DAC channel 1 left data (Figure 26).

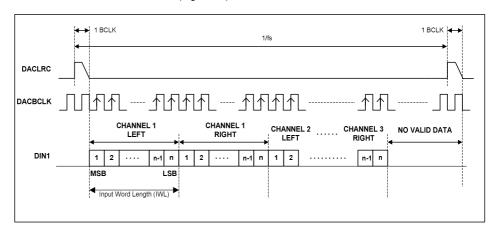


Figure 26 DSP Mode Audio Interface - Mode A Slave, DAC

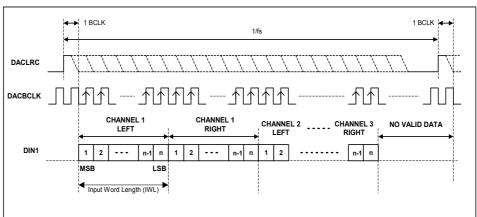


Figure 27 DSP Mode Audio Interface - Mode A Master, DAC

The MSB of the left channel ADC data is output on DOUT and changes on the first falling edge of BCLK following a low to high LRC transition and may be sampled on the rising edge of BCLK. The right channel ADC data is contiguous with the left channel data (Figure 26)

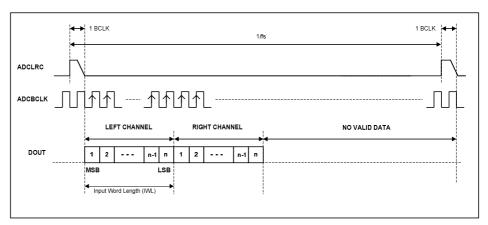


Figure 28 DSP Mode Audio Interface - Mode A Slave, ADC



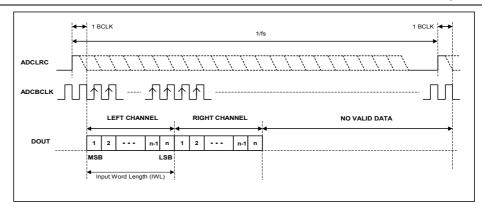


Figure 29 DSP Mode Audio Interface - Mode A Master, ADC

DSP MODE B

In DSP mode B, the MSB of DAC channel 1 left data is sampled by the WM8772 on the first BCLK rising edge following a LRC rising edge. DAC channel 1 right and DAC channels 2 and 3 data follow DAC channel 1 left data (Figure 30).

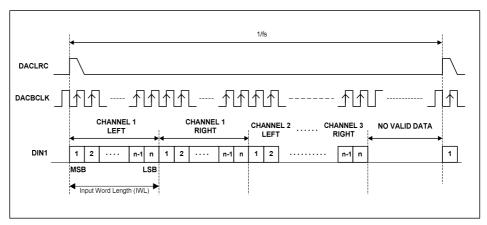


Figure 30 DSP Mode Audio Interface - Mode B Slave, DAC

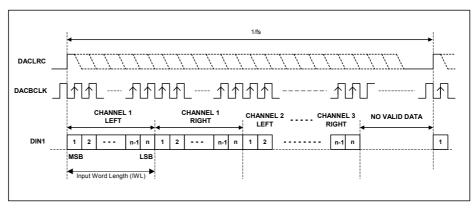


Figure 31 DSP Mode Audio Interface - Mode B Master, DAC

The MSB of the left channel ADC data is output on DOUT and changes on the same falling edge of BCLK as the low to high LRC transition and may be sampled on the rising edge of BCLK. The right channel ADC data is contiguous with the left channel data (Figure 32).



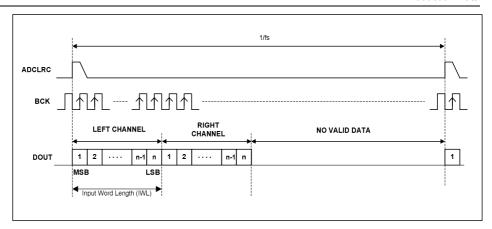


Figure 32 DSP Mode Audio Interface - Mode B Slave, ADC

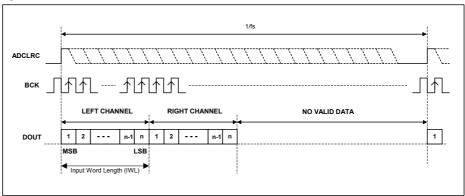


Figure 33 DSP Mode Audio Interface - Mode B Master, ADC

In both DSP mode A and mode B, DACL1 is always sent first, followed immediately by DACR1 and the data words for the other 6 channels. No BCLK edges are allowed between the data words. The word order is DAC1 left, DAC1 right, DAC2 left, DAC2 right, DAC3 left, DAC3 right.

POWERDOWN MODES

The WM8772 has powerdown control bits allowing specific parts of the WM8772 to be powered off when not being used. Control bit ADCPD powers off the ADC. The three stereo DACs each have a separate powerdown control bit, DACPD[2:0] allowing individual stereo DACs to be powered off when not in use. Setting ADCPD and DACPD[2:0] will powerdown everything except the references VMID and REFADC. These may be powered down by setting PDWN. Setting PDWN will override all other powerdown control bits. It is recommended that the ADC and DACs are powered down before setting PDWN.

ZERO DETECT

The WM8772 has a zero detect circuit for each DAC channel that detects when 1024 consecutive zero samples have been input. The MUTE pin output may be programmed to output the zero detect signal (see Table 10) which may then be used to control external muting circuits. A '1' on MUTE indicates a zero detect. The zero detect may also be used to automatically enable DAC mute by setting IZD.

| DZFM[1:0] | MUTE | | |
|-----------|-------------------|--|--|
| 00 | All channels zero | | |
| 01 | Channel 1 zero | | |
| 10 | Channel 2 zero | | |
| 11 | Channel 3 zero | | |

Table 10 Zero Flag Output Select



SOFTWARE CONTROL INTERFACE OPERATION

The WM8772 is controlled using a 3-wire serial interface in software mode or pin programmable in hardware mode.

The control mode is selected by the state of the MODE pin.

3-WIRE (SPI COMPATIBLE) SERIAL CONTROL MODE

MD/DM is used for the program data, MC/IWL is used to clock in the program data and ML/I2S is used to latch the program data. MD/DM is sampled on the rising edge of MC/IWL. The 3-wire interface protocol is shown in Figure 34.

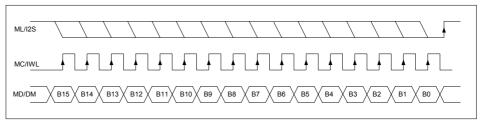


Figure 34 3-Wire SPI Compatible Interface

- 1. B[15:9] are Control Address Bits
- 2. B[8:0] are Control Data Bits
- 3. ML/I2S is edge sensitive the data is latched on the rising edge of ML/I2S.

REGISTER MAP

The complete register map is shown below. The detailed description can be found in the relevant text of the device description. The WM8772 can be configured using the Control Interface. All unused bits should be set to '0'.

| REGISTER | B15 | B14 | B13 | B12 | B11 | B10 | В9 | B8 | В7 | В6 | B5 | B4 | В3 | B2 | B1 | В0 | DEFAULT |
|----------|-----|-----|-----|-----|-----|-----|----|------------|------------------|-----|----|-----------|--------|-----------------|-----------|-----------------|-----------|
| R0(00h) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | UPDATE | PDATE LDA1[7:0] | | | | | | | 011111111 | |
| R1(01h) | 0 | 0 | 0 | 0 | 0 | 0 | 1 | UPDATE | | | | RDA1 | [7:0] | | | | 011111111 |
| R2(02h) | 0 | 0 | 0 | 0 | 0 | 1 | 0 | | PL[8:5] | | | IZD | ATC | PDWN All DAC | DEEMP | MUTE All DAC | 100100000 |
| R3(03h) | 0 | 0 | 0 | 0 | 0 | 1 | 1 | F | PHASE[8:6] | | | | [1:0] | 000000000 | | | |
| R4(04h) | 0 | 0 | 0 | 0 | 1 | 0 | 0 | UPDATE | JPDATE LDA2[7:0] | | | | | 011111111 | | | |
| R5(05h) | 0 | 0 | 0 | 0 | 1 | 0 | 1 | UPDATE | JPDATE RDA2[7:0] | | | | | 011111111 | | | |
| R6(06h) | 0 | 0 | 0 | 0 | 1 | 1 | 0 | UPDATE | JPDATE LDA3[7:0] | | | | | | 011111111 | | |
| R7(07h) | 0 | 0 | 0 | 0 | 1 | 1 | 1 | UPDATE | | | | RDA3 | [7:0] | | | | 011111111 |
| R8(08h) | 0 | 0 | 0 | 1 | 0 | 0 | 0 | UPDATE | | | | MASTD | A[7:0] | | | | 011111111 |
| R9(09h) | 0 | 0 | 0 | 1 | 0 | 0 | 1 | Г | EEMP[8:6 |] | С | MUTE[5:3] | | DZFN | M[2:1] | ZCD | 000000000 |
| R10(0Ah) | 0 | 0 | 0 | 1 | 0 | 1 | 0 | | RATE[8:6] | | MS | PWRDNALL | | DACPD[3: | 1] | ADCPD | 010000000 |
| R11(0Bh) | 0 | 0 | 0 | 1 | 0 | 1 | 1 | ADC OSR | - 010 | | | 0 | | 00 | 0 | 0 | 001000000 |
| R12(0Ch) | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | MPD | 0 | 0 | ADCHP | AMUTE ALL | AMUTEL | AMUTER | 000000000 |
| R31(1Fh) | 0 | 0 | 1 | 1 | 1 | 1 | 1 | | RESET | | | | | | | | 000000000 |



CONTROL INTERFACE REGISTERS

ATTENUATOR CONTROL MODE

Setting the ATC register bit causes the left channel attenuation settings to be applied to both left and right channel DACs from the next audio input sample. No update to the attenuation registers is required for ATC to take effect.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---------------------|-----|-------|---------|--|
| 0000010 | 3 | ATC | 0 | Attenuator Control Mode: |
| DAC Channel Control | | | | 0: Right channels use right attenuations |
| | | | | 1: Right channels use left attenuations |

INFINITE ZERO DETECT ENABLE

Setting the IZD register bit will enable the internal infinite zero detect function:

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | |
|---------------------|-----|---------|---------|---------------------------------|--|
| 0000010 | 4 | 4 IZD 0 | | Infinite Zero Mute Enable | |
| DAC Channel Control | | | | 0 : Disable inifinite zero mute | |
| | | | | 1: Enable infinite zero mute | |

With IZD enabled, applying 1024 consecutive zero input samples each stereo channel will cause that stereo channel outputs to be muted to V_{MID} . Mute will be removed as soon as that stereo channel receives a non-zero input.

DAC OUTPUT CONTROL

The DAC output control word determines how the left and right inputs to the audio Interface are applied to the left and right DACs:

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | | |
|------------------------|-----|---------|---------|-------------|----------------|-----------------|
| 0000010 DAC Control | 8:5 | PL[3:0] | 1001 | PL[3:0] | Left Output | Right Output |
| | | | | 0000 | Mute | Mute |
| | | | | 0001 | Left | Mute |
| | | | | 0010 | Right | Mute |
| | | | | 0011 | (L+R)/2 | Mute |
| | | | | 0100 | Mute | Left |
| | | | | 0101 | Left | Left |
| | | | | 0110 | Right | Left |
| | | | | 0111 | (L+R)/2 | Left |
| | | | | 1000 | Mute | Right |
| | | | | 1001 | Left | Right |
| | | | | 1010 | Right | Right |
| | | | | 1011 | (L+R)/2 | Right |
| | | | | 1100 | Mute | (L+R)/2 |
| | | | | 1101 | Left | (L+R)/2 |
| | | | | 1110 | Right | (L+R)/2 |
| | | | | 1111 | (L+R)/2 | (L+R)/2 |



ADC AND DAC DIGITAL AUDIO INTERFACE CONTROL REGISTER

Interface format is selected via the FMT[1:0] register bits:

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|-------------------|-----|-------|---------|---------------------------|
| 0000011 | 1:0 | FMT | 00 | Interface Format Select: |
| Interface Control | | [1:0] | | 00 : Right justified mode |
| | | | | 01: Left justified mode |
| | | | | 10: I ² S mode |
| | | | | 11: DSP mode A or B |

In left justified, right justified or I^2S modes, the LRP register bit controls the polarity of LRC. If this bit is set high, the expected polarity of LRC will be the opposite of that shown Figure 23, Figure 24 and Figure 25. Note that if this feature is used as a means of swapping the left and right channels, a 1 sample phase difference will be introduced. In DSP modes, the LRP register bit is used to select between mode A and mode B.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|-------------------|-----|-------|---------|---------------------------------------|
| 0000011 | 2 | LRP | 0 | In left/right/I ² S Modes: |
| Interface Control | | | | LRC Polarity (normal) |
| | | | | 0 : Normal LRC polarity |
| | | | | 1: Inverted LRC polarity |
| | | | | In DSP Mode: |
| | | | | 0 : DSP mode A |
| | | | | 1: DSP mode B |

By default, LRC and DIN1/2/3 are sampled on the rising edge of BCLK and should ideally change on the falling edge. By default, LRC and DOUT are sampled on the rising edge of BCLK and should ideally change on the falling edge. Data sources that change LRC and DOUT on the rising edge of BCLK can be supported by setting the BCP register bit. Data sources that change LRC and DIN1/2/3 on the rising edge of BCLK can be supported by setting the BCP register bit. Setting BCP to 1 inverts the polarity of BCLK to the inverse of that shown in Figure 23 to Figure 33.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|-------------------|-----|-------|---------|----------------------------|
| 0000011 | 3 | BCP | 0 | BCLK Polarity (DSP Modes): |
| Interface Control | | | | 0: Normal BCLK polarity |
| | | | | 1: Inverted BCLK polarity |

The IWL[1:0] bits are used to control the input word length.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|-------------------|-----|-------|---------|--------------------|
| 0000011 | 5:4 | IWL | 00 | Input Word Length: |
| Interface Control | | [1:0] | | 00 : 16 bit data |
| | | | | 01: 20 bit data |
| | | | | 10: 24 bit data |
| | | | | 11: 32 bit data |

Note: 32-bit right justified mode is not supported.

In all modes, the data is signed 2's complement. The digital filters always input 24-bit data. If the DAC is programmed to receive 16 or 20 bit data, the WM8772 pads the unused LSBs with zeros. If the DAC is programmed into 32 bit mode, the 8 LSBs are ignored.

Note: In 24 bit I^2S mode, any width of 24 bits or less is supported provided that LRC is high for a minimum of 24 BCLKs and low for a minimum of 24 BCLKs.

A number of options are available to control how data from the Digital Audio Interface is applied to the DAC channels.



DAC OUTPUT PHASE

The DAC Phase control word determines whether the output of each DAC is non-inverted or inverted

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | I | DESCRIPTIO | N |
|------------------|-----|-------|---------|-----|------------|------------|
| 0000011 | 8:6 | PHASE | 000 | Bit | DAC | Phase |
| DAC Phase | | [2:0] | | 0 | DAC1L/R | 1 = invert |
| | | | | 1 | DAC2L/R | 1 = invert |
| | | | | 2 | DAC3L/R | 1 = invert |

DIGITAL ZERO CROSS-DETECT

The Digital volume control also incorporates a zero cross detect circuit which detects a transition through the zero point before updating the digital volume control with the new volume. This is enabled by control bit DZCEN.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|------------------|-----|-------|---------|-------------------------------|
| 0001001 | 0 | ZCD | 0 | DAC Digital Volume Zero Cross |
| DAC Control | | | | Disable: |
| | | | | 0: Zero cross detect enabled |
| | | | | 1: Zero cross detect disabled |

MUTE FLAG OUTPUT

The DZFM control bits allow the selection of the six DAC channel zero flag bits for output on the MUTEB pin. A '1' on MUTE indicates 1024 consecutive zero input samples to the DAC channels selected.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|----------------------|-----|-----------|---------|--|
| 0001001 Zero Flag | 2:1 | DZFM[1:0] | 00 | Selects the output MUTE pin (A '1' indicates 1024 consecutive zero input samples on the DAC channels selected. 00: All channels zero 01: Channel 1 zero 10: Channel 2 zero 11: Channel 3 zero |

DAC MUTE MODES

The WM8772 has individual mutes for each of the three DAC channels. Setting MUTE for a channel will apply a 'soft' mute to the input of the digital filters of the channel muted.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|------------------|-----|-------|---------|----------------------|
| 0001001 | 5:3 | DMUTE | 000 | DAC Soft Mute Select |
| DAC Mute | | [2:0] | | |

| DMUTE [2:0] | DAC CHANNEL 1 | DAC CHANNEL 2 | DAC CHANNEL 3 |
|-------------|---------------|---------------|---------------|
| 000 | Not MUTE | Not MUTE | Not MUTE |
| 001 | MUTE | Not MUTE | Not MUTE |
| 010 | Not MUTE | Not MUTE MUTE | |
| 011 | MUTE | MUTE | Not MUTE |
| 100 | Not MUTE | Not MUTE | MUTE |
| 101 | MUTE | Not MUTE | MUTE |
| 110 | Not MUTE | MUTE | MUTE |



Setting the MUTEALL register bit will apply a 'soft' mute to the input of all the DAC digital filters:

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|------------------|-----|---------|---------|---------------------------|
| 0000010 | 0 | MUTEALL | 0 | Soft Mute Select: |
| DAC Mute | | | | 0 : Normal operation |
| | | | | 1: Soft mute all channels |

Refer to Figure 19 for the plot of application and release of soft mute.

Note that all other means of muting the DAC channels: setting the PL[3:0] bits to 0, setting the PDWN bit or setting attenuation to 0 will cause much more abrupt muting of the output.

ADC MUTE MODES

Each ADC channel also has a mute control bit, which mutes the inputs to the ADC.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|------------------|-----|----------|---------|---------------------------|
| 0001100 | 0 | AMUTER | 0 | ADC Mute Select: |
| ADC Mute | | | | 0 : Normal operation |
| | | | | 1: mute ADC right |
| | 1 | AMUTEL | 0 | ADC Mute Select: |
| | | | | 0 : Normal operation |
| | | | | 1: mute ADC left |
| | 2 | AMUTEALL | 0 | ADC Mute Select: |
| | | | | 0 : Normal operation |
| | | | | 1: mute both ADC channels |

DE-EMPHASIS MODE

Each stereo DAC channel has an individual de-emphasis control bit:

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|------------------|-------|--------|---------|-------------------------------|
| 0001001 | [8:6] | DEEMPH | 000 | De-emphasis Channel Selection |
| DAC De-Emphasis | | [1:0] | | Select: |
| Control | | | | |

| DEEMPH | DAC CHANNEL 1 | DAC CHANNEL 2 | DAC CHANNEL 3 |
|--------|-----------------|-----------------|-----------------|
| [1:0] | | | |
| 000 | Not DE-EMPHASIS | Not DE-EMPHASIS | Not DE-EMPHASIS |
| 001 | DE-EMPHASIS | Not DE-EMPHASIS | Not DE-EMPHASIS |
| 010 | Not DE-EMPHASIS | DE-EMPHASIS | Not DE-EMPHASIS |
| 011 | DE-EMPHASIS | DE-EMPHASIS | Not DE-EMPHASIS |
| 100 | Not DE-EMPHASIS | Not DE-EMPHASIS | DE-EMPHASIS |
| 101 | DE-EMPHASIS | Not DE-EMPHASIS | DE-EMPHASIS |
| 110 | Not DE-EMPHASIS | DE-EMPHASIS | DE-EMPHASIS |

Refer to Figure 7, Figure 8, Figure 9, Figure 10, Figure 11 and Figure 12 for details of the De-Emphasis performance at different sample rates.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|------------------|-----|-------|---------|-----------------------------|
| 0000010 | 1 | DEEMP | 0 | DEMMP Select: |
| DAC DEMP | | ALL | | 0 : Normal operation |
| | | | | 1: De-emphasis all channels |



POWERDOWN MODE AND ADC/DAC DISABLE

Setting the PDWN register bit immediately powers down the DAC's on the WM8772, overriding the DACD powerdown bits control bits. All trace of the previous input samples are removed, but all control register settings are preserved. When PDWN is cleared the digital filters will be reinitialised

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|-------------------|-----|-------|---------|------------------------------|
| 0000010 | 2 | PDWN | 0 | Power Down all DAC's Select: |
| Powerdown Control | | | | 0: All DAC's enabled |
| | | | | 1: All DAC's disabled |

The ADC and DACs may also be powered down individually by setting the ADCPD and DACPD disable bits. Setting ADCD will disable the ADC and select a low power mode. The ADC digital filters will be reset and will reinitialise when ADCPD is unset. Each Stereo DAC channel has a separate disable DACPD[2:0]. Setting DACPD for a channel will disable the DACs and select a low power mode.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|-------------------|-----|------------|---------|--------------|
| 0001010 | 0 | ADCPD | 0 | ADC Disable: |
| Powerdown Control | | | | 0: Active |
| | | | | 1: Disable |
| | 3:1 | DACPD[2:0] | 000 | DAC Disable |

| DACPD [2:0] | DAC CHANNEL 1 | DAC CHANNEL 2 | DAC CHANNEL 3 |
|-------------|---------------|---------------|---------------|
| 000 | Active | Active | Active |
| 001 | DISABLE | Active | Active |
| 010 | Active | DISABLE | Active |
| 011 | DISABLE | DISABLE | Active |
| 100 | Active | Active | DISABLE |
| 101 | DISABLE | Active | DISABLE |
| 110 | Active | DISABLE | DISABLE |
| 111 | DISABLE | DISABLE | DISABLE |
| | | | |

MASTER POWERDOWN

This control bit powers down the references for the whole chop. Therefore for complete powerdown, both the ADC and DACs should be powered down first before setting this bit.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|-------------------|-----|----------|---------|------------------------|
| 0001010 | 4 | PWRDNALL | 0 | Master Power Down Bit: |
| Interface Control | | | | 0: Not powered down |
| | | | | 1: Powered down |

MASTER MODE SELECT

Control bit MS selects between audio interface Master and Slave Modes. In Master mode LRC and BCLK are outputs and are generated by the WM8772. In Slave mode LRC and BCLK are inputs to WM8772.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|------------------------------|-----|-------|---------|--|
| 0001010 Interface Control | 5 | MS | 0 | DAC Audio Interface Master/Slave Mode Select: |
| | | | | 0: Slave mode |
| | | | | 1: Master mode |



MASTER MODE LRC FREQUENCY SELECT

In Master mode the WM8772 generates LRC and BCLK. These clocks are derived from the master clock and the ratio of MCLK to LRC is set by RATE.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|-------------------|-----|------------|---------|------------------------|
| 0001010 | 8:6 | RATE [2:0] | 010 | Master Mode |
| Interface Control | | | | MCLK:LRC Ratio Select: |
| | | | | 000: 128fs (DAC only) |
| | | | | 001: 192fs (DAC only) |
| | | | | 010: 256fs |
| | | | | 011: 384fs |
| | | | | 100: 512fs |
| | | | | 101: 768fs |

ADC OVERSAMPLING RATE SELECT

For ADC operation at 96kHz it is recommended that the user set the ADCOSR bit. This changes the ADC signal processing oversample rate to 64fs. The 64fs oversampling rate is only available in modes were a 96KHz rate is supported, i.e. 256fs or 384fs. In all other modes the ADC will stay in a 128fs oversampling rate irrespective of what this bit is set to.

| REGISTER ADDRESS | BIT | | DEFAULT | DESCRIPTION | |
|-----------------------|-----|--------|---------|-------------------------------|--|
| | | LABEL | | | |
| 0001011 | 8 | ADCOSR | 0 | ADC Oversampling Rate Select: | |
| ADC Oversampling Rate | | | | 0: 128x oversampling | |
| | | | | 1: 64x oversampling | |

ADC HIGHPASS FILTER DISABLE

The ADC digital filters contain a digital highpass filter. This defaults to enabled and can be disabled using software control bit ADCHPD.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|------------------|-----|--------|---------|------------------------------|
| 0001100 | 3 | ADCHPD | 0 | ADC Highpass Filter Disable: |
| ADC Control | | | | 0: Highpass filter enabled |
| | | | | 1: Highpass filter disabled |

MUTE PIN DECODE

The MUTE pin can either be used an output or an input. When used as an input the MUTE pins action can controlled by setting the DZFM bit to select the corresponding DAC for applying the MUTE to. As an output its meaning is selected by the DZFM control bits. By default selecting the MUTE to represent if DAC1 has received more than 1024 midrail samples will cause the MUTE to be asserted a softmute on DAC1. Disabling the decode block will cause any logical high on the MUTE pin to apply a softmute to all DAC's.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|------------------|-----|-------|----------------------------|----------------------------|
| 0001100 | 6 | MPD | 0 MUTE Pin Decode Disable: | |
| ADC Control | | | | 0: MUTE pin decode enable |
| | | | | 1: MUTE pin decode disable |



DAC DIGITAL VOLUME CONTROL

The DAC volume may also be adjusted in the digital domain using independent digital attenuation control registers

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|--|-----|-----------------|-------------------|---|
| 0000000 Digital | 7:0 | LDA1[7:0] | 11111111 (0dB) | Digital Attenuation data for Left channel DACL1 in 0.5dB steps. See Table 11 |
| Attenuation DACL1 | 8 | UPDATE | Not latched | Controls simultaneous update of all Attenuation Latches 0: Store LDA1 in intermediate latch (no change to output) 1: Store LDA1 and update attenuation on all channels |
| 0000001 Digital | 7:0 | RDA1[6:0] | 11111111 (0dB) | Digital Attenuation data for Right channel DACR1 in 0.5dB steps. See Table 11 |
| Attenuation DACR1 | 8 | UPDATE | Not latched | Controls simultaneous update of all Attenuation Latches 0: Store RDA1 in intermediate latch (no change to output) 1: Store RDA1 and update attenuation on all channels. |
| 0000100 Digital | 7:0 | LDA2[7:0] | 11111111 (0dB) | Digital Attenuation data for Left channel DACL2 in 0.5dB steps. See Table 11 |
| Attenuation DACL2 | 8 | UPDATE | Not latched | Controls simultaneous update of all Attenuation Latches 0: Store LDA2 in intermediate latch (no change to output) 1: Store LDA2 and update attenuation on all channels. |
| 0000101 Digital | 7:0 | RDA2[7:0] | 11111111 (0dB) | Digital Attenuation data for Right channel DACR2 in 0.5dB steps. See Table 11 |
| Attenuation DACR2 | 8 | UPDATE | Not latched | Controls simultaneous update of all Attenuation Latches 0: Store RDA2 in intermediate latch (no change to output) 1: Store RDA2 and update attenuation on all channels. |
| 0000110 Digital | 7:0 | LDA3[7:0] | 11111111 (0dB) | Digital Attenuation data for Left channel DACL3 in 0.5dB steps. See Table 11 |
| Attenuation DACL3 | 8 | UPDATE | Not latched | Controls simultaneous update of all Attenuation Latches 0: Store LDA3 in intermediate latch (no change to output) 1: Store LDA3 and update attenuation on all channels. |
| 0000111 Digital | 7:0 | RDA3[7:0] | 11111111 (0dB) | Digital Attenuation data for Right channel DACR3 in 0.5dB steps. See Table 11 |
| Attenuation DACR3 | 8 | UPDATE | Not latched | Controls simultaneous update of all Attenuation Latches 0: Store RDA3 in intermediate latch (no change to output) 1: Store RDA3 and update attenuation on all channels. |
| 0001000 Master | 7:0 | MASTDA [7:0] | 11111111 (0dB) | Digital Attenuation data for all DAC channels in 0.5dB steps. See Table 11 |
| Digital Attenuation (all channels) | 8 | UPDATE | Not latched | Controls simultaneous update of all Attenuation Latches 0: Store gain in intermediate latch (no change to output) 1: Store gain and update attenuation on all channels. |

| L/RDAX[7:0] | ATTENUATION LEVEL |
|-------------|-------------------|
| 00(hex) | -∞ dB (mute) |
| 01(hex) | -127dB |
| : | : |
| : | : |
| : | : |
| FE(hex) | -0.5dB |
| FF(hex) | 0dB |

Table 11 Digital Volume Control Attenuation Levels



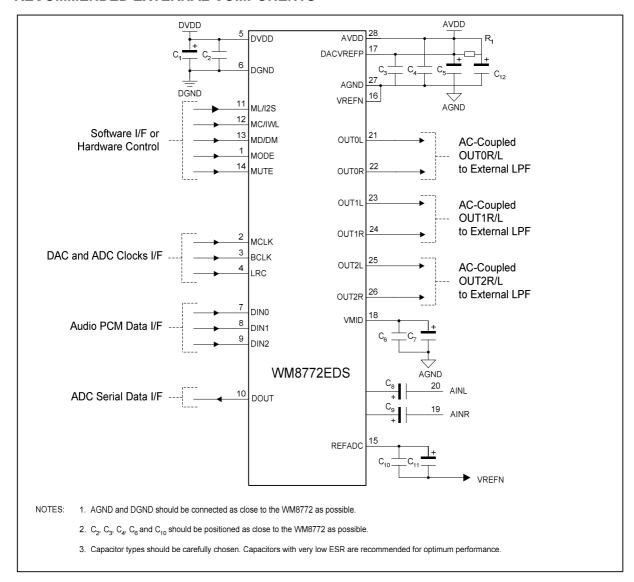
SOFTWARE REGISTER RESET

Writing to register 11111 will cause a register reset, resetting all register bits to their default values. The device will be held in this reset state until a subsequent register write to any address is completed.



APPLICATIONS INFORMATION

RECOMMENDED EXTERNAL COMPONENTS



RECOMMENDED EXTERNAL COMPONENTS VALUES

| COMPONENT REFERENCE | SUGGESTED VALUE | DESCRIPTION |
|------------------------|--------------------|---|
| C1 and C5 | 10μF | De-coupling for DVDD and AVDD. |
| C2 to C4 | 0.1μF | De-coupling for DVDD and AVDD. |
| C8 and C9 | 1μF | Analogue input high pass filter capacitors |
| C6 and C10 | 0.1μF | Reference de-coupling capacitors for VMID and ADCREF pin. |
| C7 and C11 | 10μF | |
| C12 | 10μF | Filtering for VREFP. Omit if AVDD low noise. |
| R1 | 33Ω | Filtering for VREP. Use 0Ω if AVDD low noise. |

Table 12 External Components Description



SUGGESTED ANALOGUE LOW PASS POST DAC FILTERS

It is recommended that a lowpass filter be applied to the output from each DAC channel for Hi Fi applications. Typically a second order filter is suitable and provides sufficient attenuation of high frequency components (the unique low order, high bit count multi-bit sigma delta DAC structure used in WM8772 produces much less high frequency output noise than normal sigma delta DACs. This filter is typically also used to provide the 2x gain needed to provide the standard 2Vrms output level from most consumer equipment.

Figure 35 shows a suitable post DAC filter circuit, with 2x gain. Alternative inverting filter architectures might also be used with as good results.

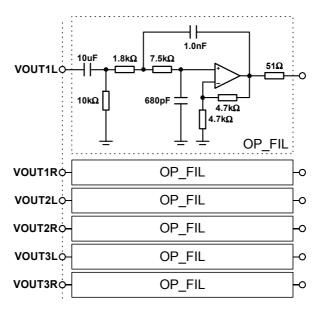


Figure 35 Recommended Post DAC Filter Circuit



To ensure that system 'pop' noise is kept to a minimum when power is applied or removed, a transistor clamp circuit arrangement may be added to the output connectors of the system. A recommended clamp circuit configuration is shown below.

Figure 36 Output Clamp Circuit

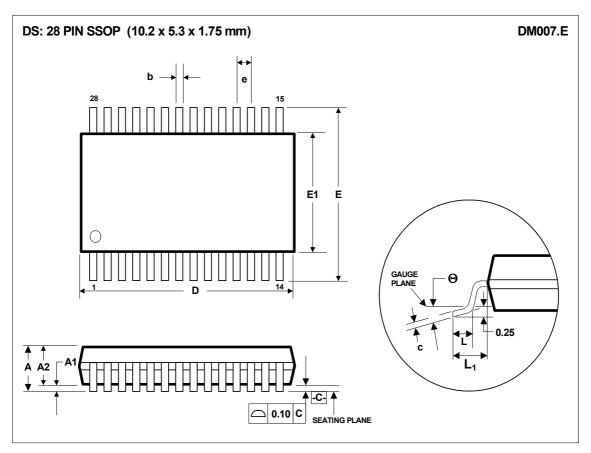
When the +VS power supply is applied, PNP transistor Q10 of the trigger circuit is held on until capacitor C49 is fully charged. With transistor Q10 held 'on', NPN transistors Q4 to Q9 of the clamp circuits are also switched on holding the system outputs near to GND. When capacitor C49 is fully charged transistors Q10 and Q4 to Q9 are switched off setting the outputs active.

When the +VS power supply is removed, PNP transistor Q11 of the trigger circuit is switched on. In turn, transistors Q4 to Q9 of the clamp circuits are switched on holding the outputs of the evaluation board near to GND until the rest of the circuitry on the board has settled.

Note: It is recommended that low Vce_{sat} switching transistors should be used in this circuit to ensure that the clamp is applied before the rest of the circuitry has time to power down.

Important: If a trigger circuit such as the one shown is to be used, it is important that the +VS supply drops quicker than any other supply to ensure that the outputs are clamped during the period when 'pop' noise may occur.

PACKAGE DIMENSIONS



| Symbols | Dimensions (mm) | | | | | | |
|-----------------------|-----------------|--------------|-------|--|--|--|--|
| | MIN | NOM | MAX | | | | |
| Α | | | 2.0 | | | | |
| A ₁ | 0.05 | | 0.25 | | | | |
| A_2 | 1.65 | 1.75 | 1.85 | | | | |
| b | 0.22 | 0.30 | 0.38 | | | | |
| С | 0.09 | | 0.25 | | | | |
| D | 9.90 | 10.20 | 10.50 | | | | |
| е | 0.65 BSC | | | | | | |
| E | 7.40 | 7.80 | 8.20 | | | | |
| E ₁ | 5.00 | 5.30 | 5.60 | | | | |
| L | 0.55 | 0.75 | 0.95 | | | | |
| L ₁ | 1.25 REF | | | | | | |
| θ | 0° 4° 8° | | | | | | |
| | | | | | | | |
| REF: | JE | EDEC.95, MO- | 150 | | | | |

NOTES:

- NO 155:

 A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.

 B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.

 C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.20MM.

 D. MEETS JEDEC.95 MO-150, VARIATION = AH. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.

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REVISION HISTORY

| DATE | REV | ORIGINATOR | CHANGES |
|----------|-----|------------|---|
| 10/03/11 | 4.6 | JMacD | Removal of WM8772SEFT (TQFP) references throughout datasheet. |

