Ultra Low Power Stereo Audio Codec With Embedded miniDSP

Check for Samples: TLV320AIC3256

FEATURES

- **Stereo Audio DAC with 100dB SNR**
- **5.0mW Stereo 48ksps DAC-to-Ground-Centered Headphone Playback**
- **Stereo Audio ADC with 93dB SNR**
- **5.2mW Stereo 48ksps ADC Record**
- **PowerTune™**
- **Extensive Signal Processing Options**
- **Embedded miniDSP**
- **Six Single-Ended or 3 Fully-Differential Analog Inputs**
- **Stereo Analog and Digital Microphone Inputs**
- **Ground-Centered Stereo Headphone Outputs**
- **Very Low-Noise PGA**
- **Low Power Analog Bypass Mode**
- **Programmable Microphone Bias**
- **Programmable PLL**
- **5mm x 5mm 40-pin QFN Package**
- **Future 3.5mm x 3.3mm 42-ball WCSP**

APPLICATIONS

- **Portable Navigation Devices (PND)**
- **Portable Media Player (PMP)**
- **Mobile Handsets**
- **Communication**
- **Portable Computing**
- **Acoustic Echo Cancellation (AEC)**
- **Active Noise Cancellation (ANC)**
- **Advanced DSP algorithms**

DESCRIPTION

The TLV320AIC3256 (sometimes referred to as the AIC3256) is a flexible, low-power, low-voltage stereo audio codec with programmable inputs and outputs, PowerTune capabilities, fully-programmable miniDSP, fixed predefined and parameterizable signal processing blocks, integrated PLL, and flexible digital interfaces.

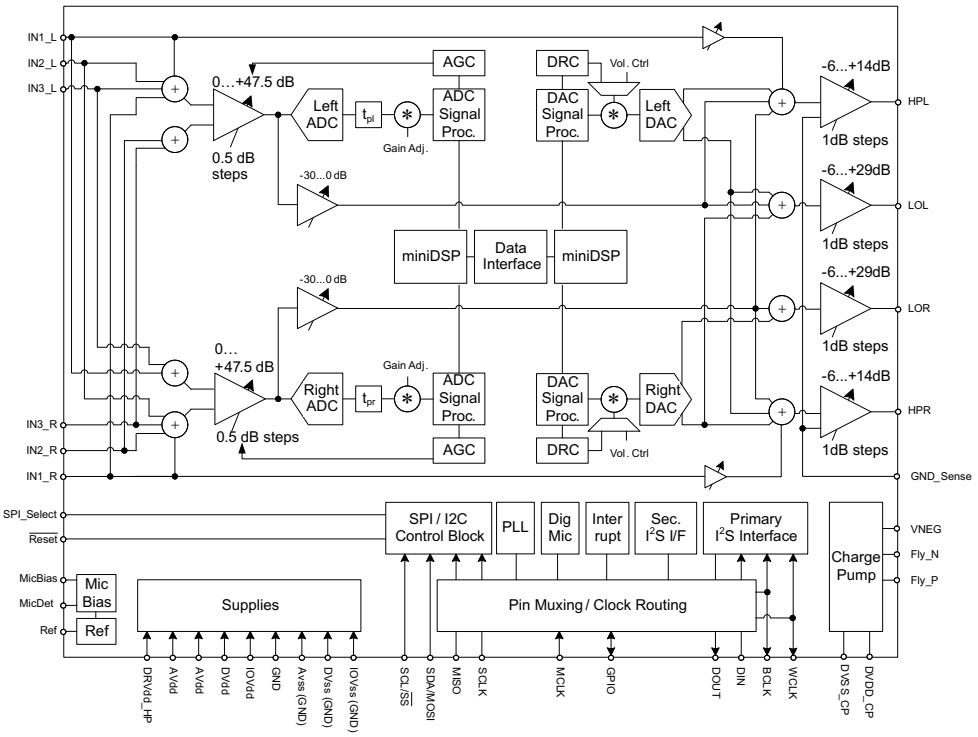

Figure 1. Simplified Block Diagram

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PowerTune is a trademark of Texas Instruments.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION (CONTINUED)

The TLV320AIC3256 features two fully-programmable miniDSP cores that support application-specific algorithms in the record and/or the playback path of the device. The miniDSP cores are fully software controlled. Target miniDSP algorithms, such as active noise cancellation, acoustic echo cancellation or advanced DSP filtering are loaded into the device after power-up.

Extensive register-based control of power, input/output channel configuration, gains, effects, pin-multiplexing and clocks is included, allowing the device to be precisely targeted to its application. The device can cover operations from 8kHz mono voice playback to audio stereo 192kHz DAC playback, making it ideal for portable battery-powered audio and telephony applications.

The record path of the TLV320AIC3256 covers operations from 8kHz mono to 192kHz stereo recording, and contains programmable input channel configurations covering single-ended and differential setups, as well as floating or mixing input signals. It also includes a digitally-controlled stereo microphone preamplifier and integrated microphone bias. Digital signal processing blocks can remove audible noise that may be introduced by mechanical coupling, e.g. optical zooming in a digital camera.

The playback path offers signal-processing blocks for filtering and effects, and supports flexible mixing of DAC and analog input signals as well as programmable volume controls. The playback path contains two high-power output drivers which eliminate the need for ac coupling capacitors. A built in charge pump generates the negative supply for the ground centered high powered output drivers. The high-power outputs can be configured in multiple ways, including stereo and mono BTL.

The device can be programmed to various power-performance trade-offs. Mobile applications frequently have multiple use cases requiring very low power operation while being used in a mobile environment. When used in a docked environment power consumption typically is less of a concern, while minimizing noise is important. The TLV320AIC3256 addresses both cases.

The device offers single supply operation from 1.5V-1.95V. Digital I/O voltages are supported in the range of 1.1V-3.6V.

The required internal clock of the TLV320AIC3256 can be derived from multiple sources, including the MCLK pin, the BCLK pin, the GPIO pin or the output of the internal PLL, where the input to the PLL again can be derived from the MCLK pin, the BCLK or GPIO pins. Although using the PLL ensures the availability of a suitable clock signal, it is not recommended for the lowest power settings. The PLL is highly programmable and can accept available input clocks in the range of 512kHz to 50MHz.

The device is available in the 5mm × 5mm, 40-pin QFN package. A 3.5mm × 3.3mm 42-ball WCSP will soon be available.

Package and Signal Descriptions

Packaging/Ordering Information

PRODUCT	PACKAGE	PACKAGE DESIGNATOR	OPERATING TEMPERATURE RANGE	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
TLV320AIC3256	QFN	RSB	–40°C to 85°C	TLV320AIC3256IRSBT	Tape and Reel, 250
				TLV320AIC3256IRSBR	Tape and Reel, 3000
TLV320AIC3256(1)	WCSP	YZF	–40°C to 85°C	TLV320AIC3256IYZFT	Tape and Reel, 250
				TLV320AIC3256IYZFR	Tape and Reel, 3000

(1) Preview information

Pin Assignments

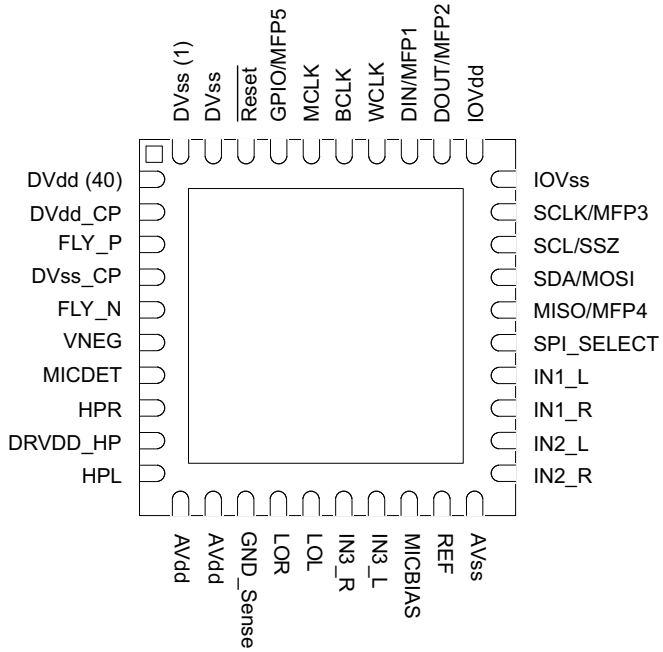


Figure 2. QFN (RSB) Package, Bottom View

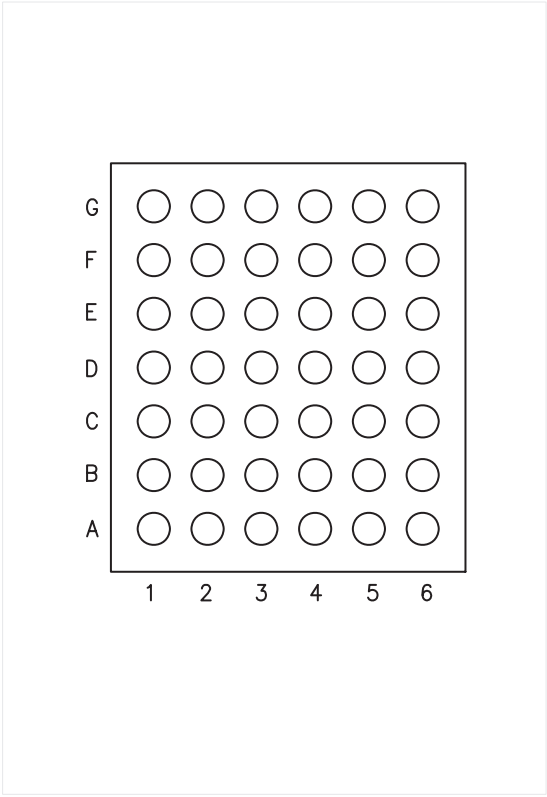


Figure 3. WCSP (YZF) Package, Bottom View (Preview)

Table 1. Ball Layout, YZF Package, Bottom View (Preview)

G	AVdd	AVdd	LOL	MICBIAS	REF	IN2_R
F	HPL	DRVdd_HP	LOR	IN3_R	IN3_L	IN2_L
E	HPR	MICDET	GND_SENSE	AVss	AVss	IN1_R
D	VNEG	FLY_N	DVss_CP	MISO	NC	IN1_L
C	DVdd_CP	FLY_P	SDA/MOSI	SCLK	$\overline{\text{RESET}}$	SPI_SELECT
B	DVdd	DVss	GPIO	BCLK	IOVss	SCL/$\overline{\text{SS}}$
A	DVss	MCLK	WCLK	DOUT	DIN	IOVdd
	1	**2**	**3**	**4**	**5**	**6**

Table 2. TERMINAL FUNCTIONS

5x5mm 40-PIN QFN (RSB) PIN NO.	WCSP (YZF) BALL NO. (Preview)	NAME	TYPE	DESCRIPTION
1	B2	DVss	GND	Digital ground. Device substrate. (1)
2	A1	DVss	GND	Digital ground (1)
3	C5	$\overline{\text{RESET}}$	I	Hardware reset
4	B3	GPIO MFP5	I/O	Primary General purpose digital IO Secondary CLKOUT output INT1 output INT2 output Audio serial data bus ADC word clock output Audio serial data bus (secondary) bit clock output Audio serial data bus (secondary) word clock output Digital microphone clock output
5	A2	MCLK	I	Master clock input
6	B4	BCLK	I/O	Audio serial data bus (primary) bit clock
7	A3	WCLK	I/O	Audio serial data bus (primary) word clock
8	A5	DIN MFP1	I	Primary function Audio serial data bus data input Secondary function Audio serial data bus (secondary) bit clock input Audio serial data bus (secondary) word clock input Digital Microphone Input Clock Input General Purpose Input
9	A4	DOUT MFP2	O	Primary Audio serial data bus data output Secondary General purpose output Clock output INT1 output INT2 output Audio serial data bus (secondary) bit clock output Audio serial data bus (secondary) word clock output
10	A6	IOVdd	PWR	Supply for IO buffers. 1.1V to 3.6V
11	B5	IOVss	GND	Ground for IO buffers.
12	C4	SCLK MFP3	I	Primary (SPI_Select = 1) SPI serial clock Secondary: (SPI_Select = 0) Digital microphone input Audio serial data bus (secondary) bit clock input Audio serial data bus (secondary) DAC/common word clock input Audio serial data bus (secondary) ADC word clock input Audio serial data bus (secondary) data input General purpose input
13	B6	SCL $\overline{\text{SS}}$	I	I^2C interface serial clock (SPI_Select = 0) SPI interface mode chip-select signal (SPI_Select = 1)
14	C3	SDA MOSI	I/O	I^2C interface mode serial data input (SPI_Select = 0) SPI interface mode serial data input (SPI_Select = 1)
15	D4	MISO	O	Primary (SPI_Select = 1)

(1) The DVss pins are not connected within the device: Must be connected on the PC board.

Table 2. TERMINAL FUNCTIONS (continued)

5x5mm 40-PIN QFN (RSB) PIN NO.	WCSP (YZF) BALL NO. (Preview)	NAME	TYPE	DESCRIPTION
		MFP4		Serial data output Secondary (SPI_Select = 0) General purpose output CLKOUT output INT1 output INT2 output Audio serial data bus (primary) ADC word clock output Digital microphone clock output Audio serial data bus (secondary) data output Audio serial data bus (secondary) bit clock output Audio serial data bus (secondary) word clock output
16	C6	SPI_SELECT	I	Control mode select pin (1 = SPI, 0 = I^2C)
17	D6	IN1_L	I	Multifunction analog input, Single-ended configuration: MIC 1 or Line 1 left Differential configuration: MIC or Line right, negative
18	E6	IN1_R	I	Multifunction analog input, Single-ended configuration: MIC 1 or Line 1 right Differential configuration: MIC or Line right, positive
19	F6	IN2_L	I	Multifunction analog input, Single-ended configuration: MIC 2 or Line 2 right Differential configuration: MIC or Line left, positive
20	G6	IN2_R	I	Multifunction analog input, Single-ended configuration: MIC 2 or Line 2 right Differential configuration: MIC or Line left, negative
21	E4, E5	AVss	GND	Analog Ground
22	G5	REF	O	Reference voltage output for filtering
23	G4	MICBIAS	O	Microphone bias voltage output
24	F5	IN3_L	I	Multifunction analog input, Single-ended configuration: MIC3 or Line 3 left, Differential configuration: MIC or Line left, positive, Differential configuration: MIC or Line right, negative
25	F4	IN3_R	I	Multifunction analog input, Single-ended configuration: MIC3 or Line 3 right, Differential configuration: MIC or Line left, negative, Differential configuration: MIC or Line right, positive
26	G3	LOL	O	Left line output
27	F3	LOR	O	Right line output
28	E3	GND_SENSE	I	External ground reference for headphone interface –0.5V to 0.5V
29, 30	G2, G1	AVdd	PWR	Analog voltage supply 1.5V–1.95V(2)
31	F1	HPL	O	Left headphone output
32	F2	DRVdd_HP	PWR	Power supply for headphone output stage Ground-centered circuit configuration, 1.5V to 1.95V Unipolar circuit configuration, 1.5V to 3.6V
33	E1	HPR	O	Right headphone output
34	E2	MICDET	I	Microphone detection
35	D1	VNEG	PWR	Negative supply for headphones. –1.8V to 0V Input when charge pump is disabled, Filtering output when charge pump is enabled
36	D2	FLY_N	PWR	Negative terminal for charge-pump flying capacitor
37	D3	DVss_CP	GND	Charge pump ground

(2) The AVdd pins are not connected within the device: Must be connected on the PC board.

Table 2. TERMINAL FUNCTIONS (continued)

5x5mm 40-PIN QFN (RSB) PIN NO.	WCSP (YZF) BALL NO. (Preview)	NAME	TYPE	DESCRIPTION
38	C2	FLY_P	PWR	Positive terminal for charge pump flying capacitor
39	C1	DVdd_CP	PWR	Charge Pump supply; recommended to connect to DVdd
40	B1	DVdd	PWR	Digital voltage supply 1.26V – 1.95V

Electrical Characteristics

Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		VALUE	UNIT
AVdd to AVss		–0.3 to 2.2	V
DVdd to DVss		–0.3 to 2.2	V
IOVDD to IOVSS		–0.3 to 3.9	V
Digital Input voltage		IOVSS to IOVDD + 0.3	V
Analog input voltage		AVSS to AVdd + 0.3	V
Operating temperature range		–40 to 85	°C
Storage temperature range		–55 to 150	°C
Junction temperature (T_J Max)		105	°C
QFN package (RSB)	Power dissipation	(T_J Max – TA)/ θ_{JA}	W
	θ_{JA} Thermal impedance	35	C/W
WCSP package (YZF)	Power dissipation	(T_J Max – TA)/ θ_{JA}	W
	θ_{JA} Thermal impedance	50	C/W

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

				MIN	NOM	MAX	UNIT
AVdd	Power Supply Voltage Range	Referenced to AVss (1)		1.5	1.8	1.95	V
IOVDD		Referenced to IOVSS (1)		1.1		3.6	
DVdd (2)		Referenced to DVss (1)		1.26	1.8	1.95	
DVDD_CP	Power Supply Voltage Range	Referenced to DVss (1)		1.26	1.8	1.95	V
DRVDD_HP		Referenced to AVss (1)	Ground-centered config	1.5	1.8	1.95	
			Unipolar config	1.5		3.6	
	PLL Input Frequency	Clock divider uses fractional divide (D > 0), P=1, D_{Vdd} ≥ 1.65V (Refer to table in SLAU306, *Maximum TLV320AIC3256 Clock Frequencies*)		10		20	MHz
		Clock divider uses integer divide (D = 0), P=1, D_{Vdd} ≥ 1.65V (Refer to table in SLAU306, *Maximum TLV320AIC3256 Clock Frequencies*)		0.512		20	MHz
MCLK	Master Clock Frequency	MCLK; Master Clock Frequency; D_{Vdd} ≥ 1.65V				50	MHz
		MCLK; Master Clock Frequency; D_{Vdd} ≥ 1.26V				25	
SCL	SCL Clock Frequency					400	kHz
LOL, LOR	Stereo line output load resistance			0.6	10		kΩ
HPL, HPR	Stereo headphone output load resistance	Single-ended configuration		14.4	16		Ω
	Headphone output load resistance	Differential configuration		24.4	32		Ω
C_{Lout}	Digital output load capacitance				10		pF
TOPR	Operating Temperature Range			–40		85	°C

(1) All grounds on board are tied together; they must not differ in voltage by more than 0.2V max, for any combination of ground signals.
(2) At DVdd values lower than 1.65V, the PLL does not function. Please see table in SLAU306, *Maximum TLV320AIC3256 Clock Frequencies* for details on maximum clock frequencies.

Electrical Characteristics, ADC

At 25°C, AVdd, DVdd, IOVdd,DVdd_CP, DRVdd_HP = 1.8V, fs (Audio) = 48kHz, Cref = 1µF on REF PIN, PLL and Charge pump disabled unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AUDIO ADC (CM = 0.9V)						
	Input signal level (for 0dB output)	Single-ended, CM = 0.9V		0.5		V_{RMS}
	Device Setup	1kHz sine wave input Single-ended Configuration IN1R to Right ADC and IN1L to Left ADC, R_{in} = 20K, f_s = 48kHz, AOSR = 128, MCLK = 256*f_s, PLL Disabled; AGC = OFF, Channel Gain = 0dB, Processing Block = PRB_R1, Power Tune = PTM_R4				
SNR	Signal-to-noise ratio, A-weighted(1) (2)	Inputs ac-shorted to ground	80	93		dB
		IN2R, IN3R routed to Right ADC and ac-shorted to ground IN2L, IN3L routed to Left ADC and ac-shorted to ground		93		
DR	Dynamic range A-weighted(1) (2)	–60dB full-scale, 1-kHz input signal		93		dB
THD+N	Total Harmonic Distortion plus Noise	–3 dB full-scale, 1-kHz input signal		–84	–70	dB
		IN2R,IN3R routed to Right ADC IN2L, IN3L routed to Left ADC –3dB full-scale, 1-kHz input signal		–84		
AUDIO ADC (CM=0.75V)						
	Input signal level (for 0dB output)	Single-ended, CM=0.75V, AVdd = 1.5V		0.375		V_{RMS}
	Device Setup	1kHz sine wave input Single-ended Configuration INR, IN2R, IN3R routed to Right ADC INL, IN2L, IN3L routed to Left ADC R_{in} = 20K, f_s = 48kHz, AOSR=128, MCLK = 256* f_s, PLL Disabled, AGC = OFF, Channel Gain = 0dB, Processing Block = PRB_R1 Power Tune = PTM_R4				
SNR	Signal-to-noise ratio, A-weighted (1) (2)	Inputs ac-shorted to ground		90		dB
DR	Dynamic range A-weighted(1) (2)	–60dB full-scale, 1-kHz input signal		90		dB
THD+N	Total Harmonic Distortion plus Noise	–3dB full-scale, 1-kHz input signal		–81		dB

(1) Ratio of output level with 1-kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A-weighted over a 20-Hz to 20-kHz bandwidth using an audio analyzer.

(2) All performance measurements done with 20-kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values

Electrical Characteristics, ADC (continued)

At 25°C, AVdd, DVdd, IOVdd,DVdd_CP, DRVdd_HP = 1.8V, fs (Audio) = 48kHz, Cref = 1µF on REF PIN, PLL and Charge pump disabled unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AUDIO ADC (Gain=40dB)						
	Input signal level (for 0dB output)	Differential Input, CM=0.9V, Channel Gain=40dB		10		mV_{RMS}
	Device Setup	1kHz sine wave input Differential configuration IN1L and IN1R routed to Right ADC IN2L and IN2R routed to Left ADC R_{in} =10K, f_s =48kHz, AOSR=128 MCLK = 256* f_s PLL Disabled AGC = OFF Processing Block = PRB_R1, Power Tune = PTM_R4				
ICN	Idle-Channel Noise, A-weighted(3) (4)	Inputs ac-shorted to ground, input referred noise		2.8		μV_{RMS}
AUDIO ADC						
	Gain Error	1kHz sine wave input Single-ended configuration R_{in} = 20K f_s = 48kHz, AOSR=128, MCLK = 256* f_s, PLL Disabled AGC = OFF, Channel Gain=0dB Processing Block = PRB_R1, Power Tune = PTM_R4, CM=0.9V		0.1		dB
	Input Channel Separation	1kHz sine wave input at -3dBFS Single-ended configuration IN1L routed to Left ADC IN1R routed to Right ADC, R_{in} = 20K AGC = OFF, AOSR = 128, Channel Gain=0dB, CM=0.9V		109		dB
	Input Pin Crosstalk	1kHz sine wave input at –3dBFS on IN2L, IN2L internally not routed. IN1L routed to Left ADC ac-coupled to ground 1kHz sine wave input at –3dBFS on IN2R, IN2R internally not routed. IN1R routed to Right ADC ac-coupled to ground Single-ended configuration R_{in} = 20K, AOSR=128 Channel, Gain=0dB, CM=0.9V		108		dB
	PSRR	217Hz, 100mVpp signal on AVdd, Single-ended configuration, Rin=20K, Channel Gain=0dB; CM=0.9V		55		dB
	ADC programmable gain amplifier gain	Single-Ended, Rin = 10K, PGA gain set to 0dB		0		dB
		Single-Ended, Rin = 10K, PGA gain set to 47.5dB		47.5		dB
		Single-Ended, Rin = 20K, PGA gain set to 0dB		–6		dB
		Single-Ended, Rin = 20K, PGA gain set to 47.5dB		41.5		dB
		Single-Ended, Rin = 40K, PGA gain set to 0dB		–12		dB
		Single-Ended, Rin = 40K, PGA gain set to 47.5dB		35.5		dB
	ADC programmable gain amplifier step size	1-kHz tone		0.5		dB

(3) Ratio of output level with 1-kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A-weighted over a 20-Hz to 20-kHz bandwidth using an audio analyzer.

(4) All performance measurements done with 20-kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values

Electrical Characteristics, Bypass Outputs

At 25°C, AVdd, DVdd, IOVdd,DVdd_CP, DRVdd_HP = 1.8V, fs (Audio) = 48kHz, Cref = 1µF on REF PIN, PLL and Charge pump disabled unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG BYPASS TO HEADPHONE AMPLIFIER, DIRECT MODE						
	Device Setup	Load = 16Ω (single-ended), 50pF; Input and Output CM=0.9V; Headphone Output on DRVdd_HP Supply; IN1L routed to HPL and IN1R routed to HPR; Channel Gain=0dB				
	Gain Error			0.8		dB
	Noise, A-weighted(1)	Idle Channel, IN1L and IN1R ac-shorted to ground		3.3		μV_{RMS}
THD	Total Harmonic Distortion	446mVrms, 1-kHz input signal		–81		dB
ANALOG BYPASS TO LINE-OUT AMPLIFIER, PGA MODE						
	Device Setup	Load = 10KOhm (single-ended), 50pF; Input and Output CM=0.9V; LINE Output on DRVdd_HP Supply; IN1L, IN1R routed to line out Channel Gain = 0dB				
	Gain Error Gain Error			0.8		dB
	Noise, A-weighted(1)	Idle Channel, IN1L and IN1R ac-shorted to ground		6.7		μV_{RMS}
		Channel Gain=40dB, Input Signal (0dB) = $5mV_{rms}$ Inputs ac-shorted to ground, Input Referred		3		μV_{RMS}

(1) All performance measurements done with 20-kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values

Electrical Characteristics, Microphone Interface

At 25°C, AVdd, DVdd, IOVdd,DVdd_CP, DRVdd_HP = 1.8V, fs (Audio) = 48kHz, Cref = 1µF on REF PIN, PLL and Charge pump disabled unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
MICROPHONE BIAS					
Bias voltage	*Bias voltage CM=0.9V, DRVdd_HP = 1.8V*				
	Micbias Mode 0, Connect to AVdd or DRVdd_HP		1.5		V
	Micbias Mode 3, Connect to AVdd		AVdd		V
	Micbias Mode 3, Connect to DRVdd_HP		DRVdd_HP		V
	CM=0.75V, DRVdd_HP = 1.8V				
	Micbias Mode 0, Connect to AVdd or DRVdd_HP		1.23		V
	Micbias Mode 1, Connect to AVdd or DRVdd_HP		1.43		V
	Micbias Mode 3, Connect to AVdd		AVdd		V
	Micbias Mode 3, Connect to DRVdd_HP		DRVdd_HP		V
MICROPHONE BIAS					
Bias voltage	*Bias voltage CM=0.9V, DRVdd_HP = 3.3V*				
	Micbias Mode 0, Connect to DRVdd_HP		1.5		V
	Micbias Mode 1, Connect to DRVdd_HP		1.7		V
	Micbias Mode 2, Connect to DRVdd_HP		2.5		V
	Micbias Mode 3, Connect to DRVdd_HP		DRVdd_HP		V
	CM=0.75V, DRVdd_HP = 3.3V				
	Micbias Mode 0, Connect to DRVdd_HP		1.23		V
	Micbias Mode 1, Connect to DRVdd_HP		1.43		V
	Micbias Mode 2, Connect to DRVdd_HP		2.1		V
	Micbias Mode 3, Connect to DRVdd_HP		DRVdd_HP		V
Output Noise	CM=0.9V, Micbias Mode 2, A-weighted, 20Hz to 20kHz bandwidth, Current load = 0mA.		9.5		μV_{RMS}
Current Sourcing	Micbias Mode 2, Connect to DRVdd_HP		3		mA
Inline Resistance	Micbias Mode 3, Connect to AVdd		131		Ω
	Micbias Mode 3, Connect to DRVdd_HP		89		Ω

Electrical Characteristics, Audio DAC Outputs

At 25°C, AVdd, DVdd, IOVdd,DVdd_CP, DRVdd_HP = 1.8V, fs (Audio) = 48kHz, Cref = 1µF on REF PIN, PLL and Charge pump disabled unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AUDIO DAC – STEREO SINGLE-ENDED LINE OUTPUT (CM=0.9V)						
	Device Setup	Load = 10 kΩ (single-ended), 56pF Line Output on AVdd Supply Input & Output CM=0.9V DOSR = 128, MCLK=256* f_s, Channel Gain = 0dB, word length = 16 bits, Processing Block = PRB_P1, Power Tune = PTM_P3				
	Full scale output voltage (0dB)			0.5		V_{RMS}
SNR	Signal-to-noise ratio A-weighted (1) (2)	All zeros fed to DAC input	87	100		dB
DR	Dynamic range, A-weighted (1) (2)	–60dB 1kHz input full-scale signal, Word length=20 bits		100		dB
THD+N	Total Harmonic Distortion plus Noise	–3dB full-scale, 1-kHz input signal		–81	–70	dB
	DAC Gain Error	0 dB, 1kHz input full scale signal		0.5		dB
	DAC Mute Attenuation	Mute		121		dB
	DAC channel separation	–1 dB, 1kHz signal, between left and right HP out		108		dB
	DAC PSRR	100mVpp, 1kHz signal applied to AVdd		72		dB
		100mVpp, 217Hz signal applied to AVdd		80		dB
AUDIO DAC – STEREO SINGLE-ENDED LINE OUTPUT (CM=0.75V)						
	Device Setup	Load = 10 kΩ (single-ended), 56pF Line Output on AVdd Supply Input & Output CM=0.75V; AVdd=1.5V DOSR = 128 MCLK=256* fs Channel Gain = 0dB word length = 20-bits Processing Block = PRB_P1 Power Tune = PTM_P4				
	Full scale output voltage (0dB)			0.375		V_{RMS}
SNR	Signal-to-noise ratio, A-weighted (1) (2)	All zeros fed to DAC input		99		dB
DR	Dynamic range, A-weighted (1) (2)	–60dB 1 kHz input full-scale signal		98		dB
THD+N	Total Harmonic Distortion plus Noise	–1 dB full-scale, 1-kHz input signal		–77		dB
AUDIO DAC – STEREO SINGLE-ENDED HEADPHONE OUTPUT (GROUND-CENTERED CIRCUIT CONFIGURATION)						
	Device Setup	Load = 16Ω (single-ended), 56pF Input CM=0.9V, Output CM=0V DOSR = 128, MCLK=256* f_s, Channel Gain=0dB word length = 16 bits; Processing Block = PRB_P1 Power Tune = PTM_P3				
FS1	Full scale output voltage (for THD ≤ –40dB)			0.65		V_{RMS}
SNR	Signal-to-noise ratio, A-weighted (1) (2)	All zeros fed to DAC input	85	95		dB
DR	Dynamic range, A-weighted (1) (2)	–60dB 1kHz input full-scale signal, Word Length = 20 bits, Power Tune = PTM_P4		93		dB
THD+N	Total Harmonic Distortion plus Noise	500mV_{RMS} output (corresponds to FS1 – 2.3dB), 1-kHz input signal		–70	–55	dB

(1) Ratio of output level with 1-kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A-weighted over a 20-Hz to 20-kHz bandwidth using an audio analyzer.

(2) All performance measurements done with 20-kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values

Electrical Characteristics, Audio DAC Outputs (continued)

At 25°C, AVdd, DVdd, IOVdd,DVdd_CP, DRVdd_HP = 1.8V, fs (Audio) = 48kHz, Cref = 1µF on REF PIN, PLL and Charge pump disabled unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	DAC Gain Error	500mV$_{RMS}$ output, 1kHz input full scale signal		0.5		dB
	DAC Mute Attenuation	Mute		118		dB
	DAC channel separation	–3dB, 1kHz signal, between left and right HP out		102		dB
	DAC PSRR	100mVpp, 1kHz signal applied to AVdd		66		dB
		100mVpp, 217Hz signal applied to AVdd		77		dB
	Power Delivered	THD ≤ –40dB		26.5		mW
FS2	Full scale output voltage (for THD ≤ –40dB)	Load = 32Ω		0.85		V
SNR	Signal-to-noise ratio, A-weighted(1) (2)	All zeros fed to DAC input, Load = 32Ω		96		dB
	Power Delivered	THD ≤ –40dB, Load = 32Ω		22.5		mW
AUDIO DAC – STEREO SINGLE-ENDED HEADPHONE OUTPUT (UNIPOLAR CIRCUIT CONFIGURATION)						
	Device Setup	Load = 16Ω (single-ended), 56pF, Headphone Output on AVdd Supply, Input & Output CM=0.9V DOSR = 128, MCLK=256* f_s, Channel Gain = 0dB Processing Block = PRB_P1, Power Tune = PTM_P3				
	Full scale output voltage (0dB)			0.5		V_{RMS}
SNR	Signal-to-noise ratio, A-weighted(3) (4)	All zeros fed to DAC input	87	100		dB
DR	Dynamic range, A-weighted (3) (4)	-60dB 1 kHz input full-scale signal		100		dB
THD+N	Total Harmonic Distortion plus Noise	–3dB full-scale, 1-kHz input signal		–83	–70	dB

(3) Ratio of output level with 1-kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A-weighted over a 20-Hz to 20-kHz bandwidth using an audio analyzer.

(4) All performance measurements done with 20-kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values

Electrical Characteristics, Misc.

At 25°C, AVdd, DVdd, IOVdd,DVdd_CP, DRVdd_HP = 1.8V, fs (Audio) = 48kHz, Cref = 1µF on REF PIN, PLL and Charge pump disabled unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE					
Reference Voltage Settings	CMMode = 0 (0.9V)		0.9		V
	CMMode = 1 (0.75V)		0.75		
Reference Noise	CM=0.9V, A-weighted, 20Hz to 20kHz bandwidth, C_{ref} = 1µF		1.1		μV_{RMS}
Decoupling Capacitor			1		µF
Bias Current			120		µA
miniDSP(1)					
Maximum miniDSP clock frequency - ADC	DVdd = 1.65V	58.9			MHz
Maximum miniDSP clock frequency - DAC	DVdd = 1.65V	58.9			MHz
Shutdown Current					
Device Setup	DVdd is provided externally, no clocks supplied, no digital activity, register values are retained				
I(total)	Sum of all supply currents, all supplies at 1.8V		<10		µA

(1) The miniDSP clock speed is specified by design and not tested in production.

Electrical Characteristics, Logic Levels

At 25°C, AVdd, DVdd, IOVDD = 1.8V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC FAMILY			**CMOS**		
V_{IH} Logic Level	I_{IH} = 5 µA, IOVDD > 1.6V	0.7 × IOVDD			V
	I_{IH} = 5µA, 1.2V ≤ IOVDD <1.6V	0.9 × IOVDD			V
	I_{IH} = 5µA, IOVDD < 1.2V	IOVDD			V
V_{IL}	I_{IL} = 5 µA, IOVDD > 1.6V	–0.3		0.3 × IOVDD	V
	I_{IL} = 5µA, 1.2V ≤ IOVDD <1.6V			0.1 × IOVDD	V
	I_{IL} = 5µA, IOVDD < 1.2V			0	V
V_{OH}	I_{OH} = 2 TTL loads	0.8 × IOVDD			V
V_{OL}	I_{OL} = 2 TTL loads			0.1 × IOVDD	V
Capacitive Load			10		pF

Interface Timing

Typical Timing Characteristics — Audio Data Serial Interface Timing (I^2S)

All specifications at 25°C, DVdd = 1.8V

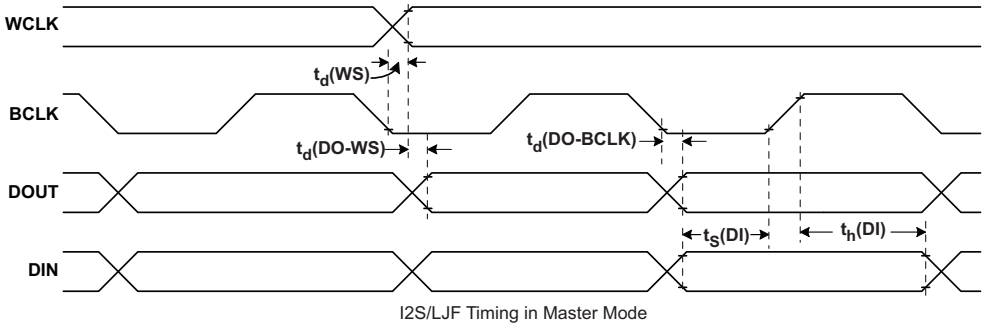


Figure 4. I^2S/LJF/RJF Timing in Master Mode

Table 3. I^2S/LJF/RJF Timing in Master Mode (see Figure 4)

PARAMETER		IOVDD=1.8V		IOVDD=3.3V		UNITS
		MIN	MAX	MIN	MAX	
t_d(WS)	WCLK delay		30		20	ns
t_d (DO-WS)	WCLK to DOUT delay (For LJF Mode only)		20		20	ns
t_d (DO-BCLK)	BCLK to DOUT delay		22		20	ns
t_s(DI)	DIN setup	8		8		ns
t_h(DI)	DIN hold	8		8		ns
t_r	Rise time		24		12	ns
t_f	Fall time		24		12	ns

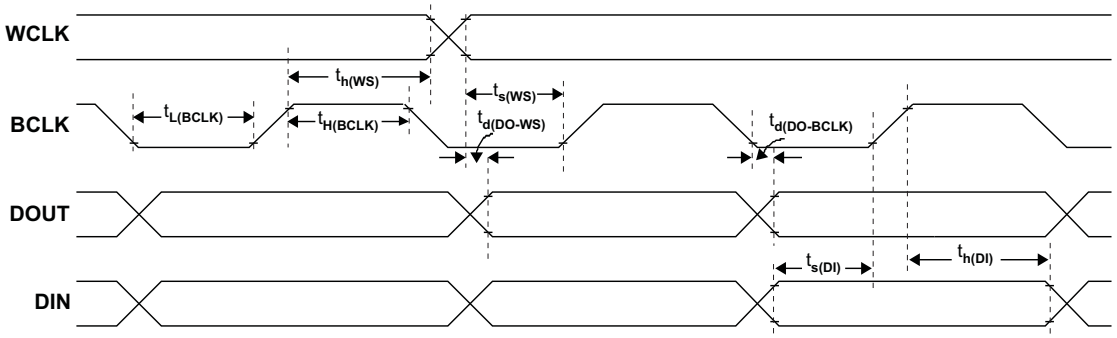


Figure 5. I^2S/LJF/RJF Timing in Slave Mode

Table 4. I^2S/LJF/RJF Timing in Slave Mode (see Figure 5)

PARAMETER		IOVDD=1.8V		IOVDD=3.3V		UNITS
		MIN	MAX	MIN	MAX	
t_H (BCLK)	BCLK high period	35		35		ns
t_L (BCLK)	BCLK low period	35		35		
t_s (WS)	WCLK setup	8		8		
t_h (WS)	WCLK hold	8		8		
t_d (DO-WS)	WCLK to DOUT delay (For LJF mode only)		20		20	
t_d (DO-BCLK)	BCLK to DOUT delay		22		22	
t_s(DI)	DIN setup	8		8		
t_h(DI)	DIN hold	8		8		
t_r	Rise time		4		4	
t_f	Fall time		4		4	

Typical DSP Timing Characteristics

All specifications at 25°C, DVdd = 1.8V

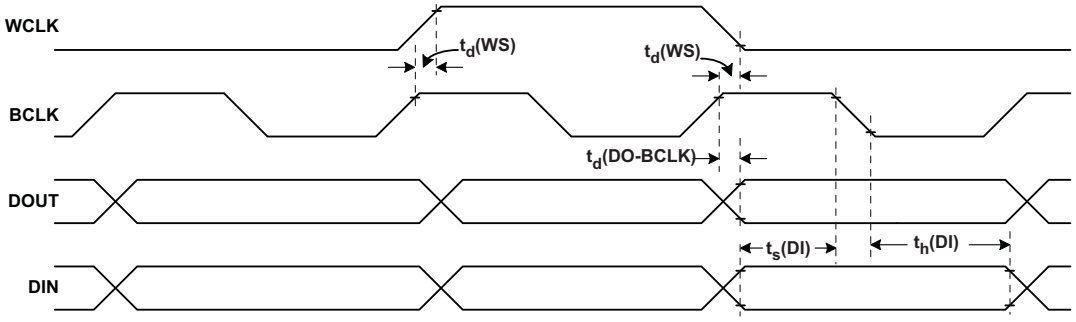


Figure 6. DSP Timing in Master Mode

Table 5. DSP Timing in Master Mode (see Figure 6)

PARAMETER		IOVDD=1.8V		IOVDD=3.3V		UNITS
		MIN	MAX	MIN	MAX	
t_d (WS)	WCLK delay		30		20	ns
t_d (DO-BCLK)	BCLK to DOUT delay		22		20	ns
t_s(DI)	DIN setup	8		8		ns
t_h(DI)	DIN hold	8		8		ns
t_r	Rise time		24		12	ns
t_f	Fall time		24		12	ns

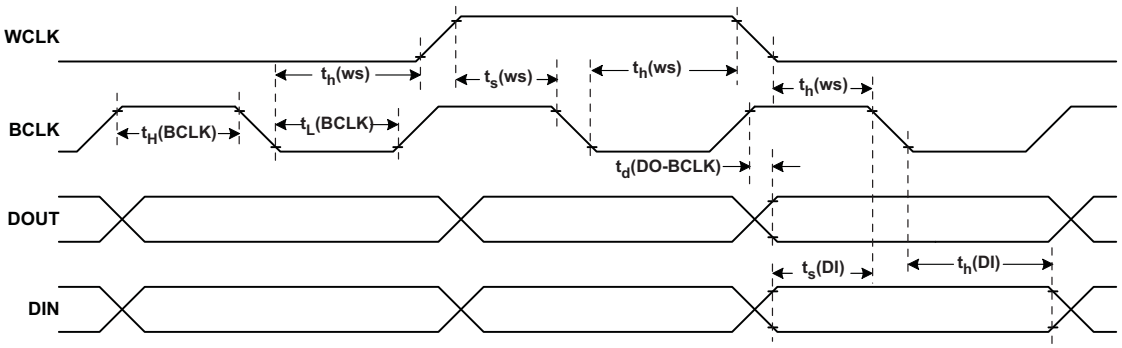


Figure 7. DSP Timing in Slave Mode

Table 6. DSP Timing in Slave Mode (see Figure 7)

PARAMETER		IOVDD=1.8V		IOVDD=3.3V		UNITS
		MIN	MAX	MIN	MAX	
t_H (BCLK)	BCLK high period	35		35		ns
t_L (BCLK)	BCLK low period	35		35		ns
t_s(WS)	WCLK setup	8		8		ns
t_h(WS)	WCLK hold	8		8		ns
t_d (DO-BCLK)	BCLK to DOUT delay		22		22	ns
t_s(DI)	DIN setup	8		8		ns
t_h(DI)	DIN hold	8		8		ns
t_r	Rise time		4		4	ns
t_f	Fall time		4		4	ns

I²C Interface Timing

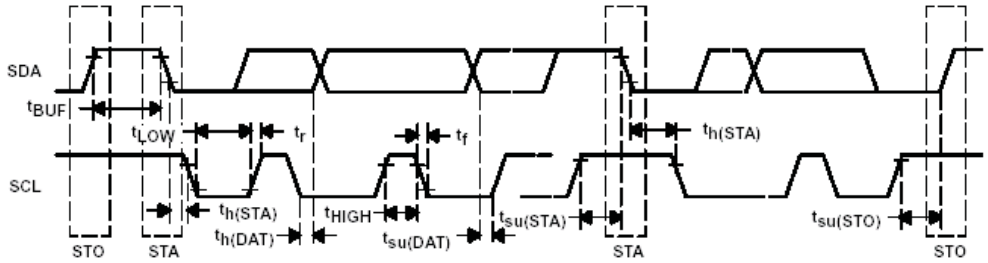


Figure 8. I²C Interface Timing

Table 7. I²C Interface Timing

PARAMETER		TEST CONDITION	Standard-Mode			Fast-Mode			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{SCL}	SCL clock frequency		0		100	0		400	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.		4.0			0.8			µs
t_{LOW}	LOW period of the SCL clock		4.7			1.3			µs
t_{HIGH}	HIGH period of the SCL clock		4.0			0.6			µs
$t_{SU;STA}$	Setup time for a repeated START condition		4.7			0.8			µs
$t_{HD;DAT}$	Data hold time: For I2C bus devices		0		3.45	0		0.9	µs
$t_{SU;DAT}$	Data set-up time		250			100			ns
t_r	SDA and SCL Rise Time				1000	$20+0.1C_b$		300	ns
t_f	SDA and SCL Fall Time				300	$20+0.1C_b$		300	ns
$t_{SU;STO}$	Set-up time for STOP condition		4.0			0.8			µs
t_{BUF}	Bus free time between a STOP and START condition		4.7			1.3			µs
C_b	Capacitive load for each bus line				400			400	pF

SPI Interface Timing

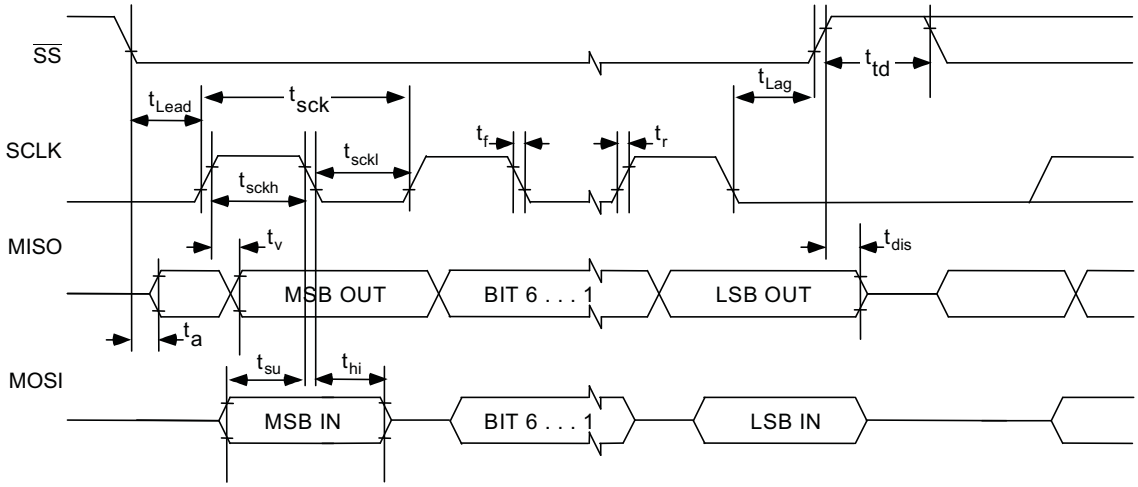


Figure 9. SPI Interface Timing Diagram

Timing Requirements (See Figure 9)

At 25°C, DVdd = 1.8V

Table 8. SPI Interface Timing

PARAMETER		TEST CONDITION	IOVDD=1.8V			IOVDD=3.3V			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{sck}	SCLK Period(1)		100			50			ns
t_{sckh}	SCLK Pulse width High		50			25			ns
t_{sckl}	SCLK Pulse width Low		50			25			ns
t_{lead}	Enable Lead Time		30			20			ns
t_{lag}	Enable Lag Time		30			20			ns
t_d	Sequential Transfer Delay		40			20			ns
t_a	Slave DOUT access time				40			20	ns
t_{dis}	Slave DOUT disable time				40			20	ns
t_{su}	DIN data setup time		15			10			ns
t_{hi}	DIN data hold time		15			10			ns
$t_{v;DOUT}$	DOUT data valid time				25			18	ns
t_r	SCLK Rise Time				4			4	ns
t_f	SCLK Fall Time				4			4	ns

(1) These parameters are based on characterization and are not tested in production.

Typical Characteristics

Device Power Consumption

Device power consumption largely depends on PowerTune configuration. For information on device power consumption, see the *TLV320AIC3256 Application Reference Guide*, literature number SLAU306.

Typical Performance

ADC SNR vs CHANNEL GAIN

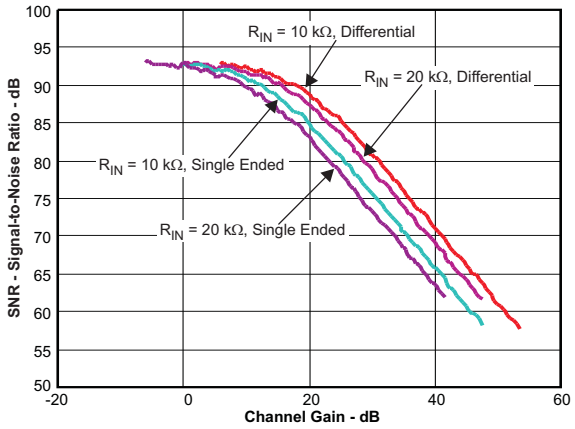


Figure 10.

TOTAL HARMONIC DISTORTION GCHP CONFIGURATION vs HEADPHONE OUTPUT POWER

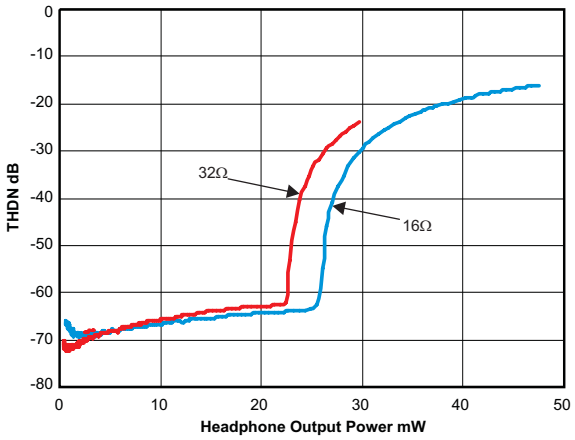


Figure 11.

TOTAL HARMONIC DISTORTION UNIPOLAR CONFIGURATION vs HEADPHONE OUTPUT POWER

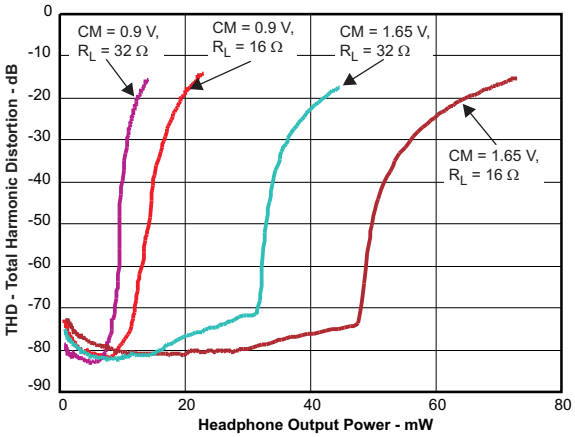


Figure 12.

TOTAL HARMONIC DISTORTION vs HEADPHONE OUTPUT POWER

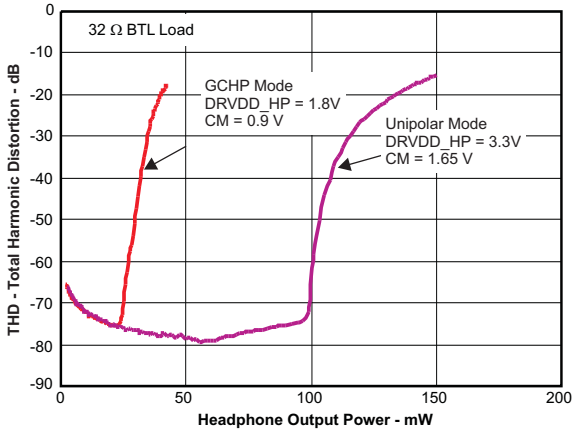


Figure 13.

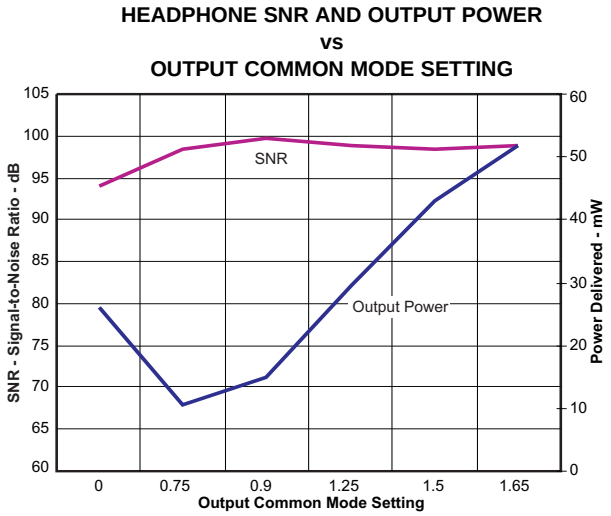


Figure 14.

FFT

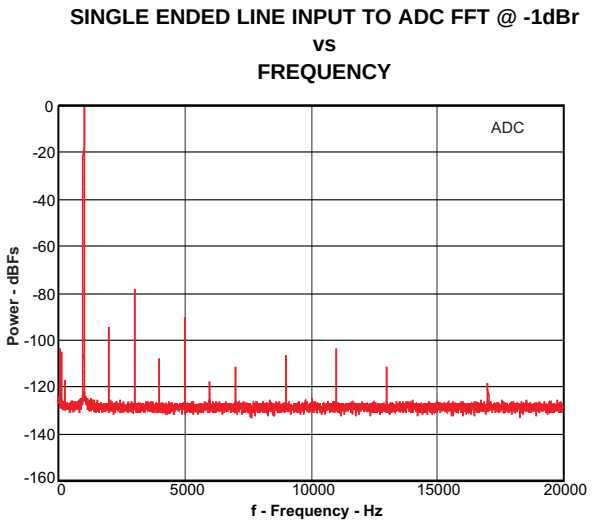


Figure 15.

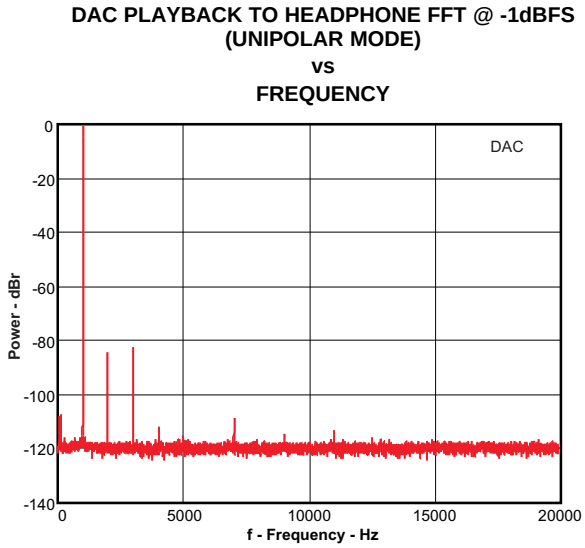


Figure 16.

DAC PLAYBACK TO HEADPHONE FFT @ -1dBFS
(GROUND-CENTERED MODE)
vs
FREQUENCY

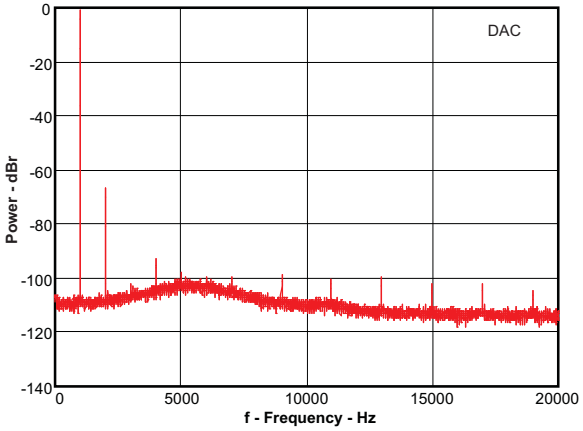


Figure 17.

DAC PLAYBACK TO LINE-OUT FFT @ -1dBFS
vs
FREQUENCY

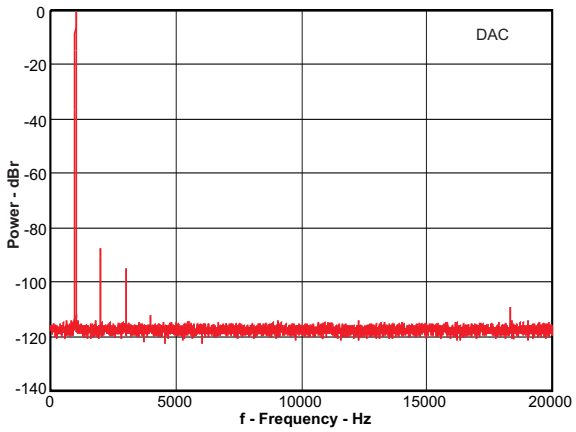


Figure 18.

LINE INPUT TO HEADPHONE FFT @ 446mVrms
(UNIPOLAR MODE)
vs
FREQUENCY

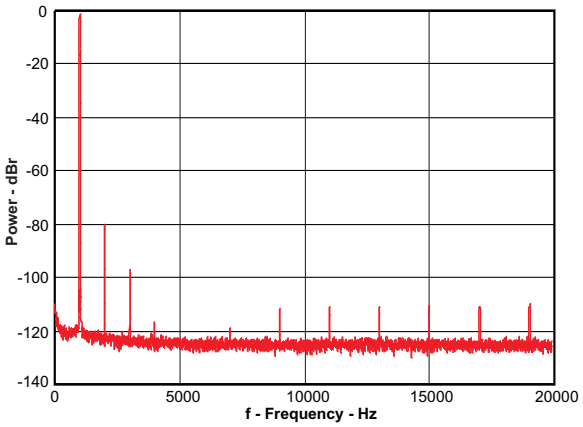


Figure 19.

LINE INPUT TO LINE-OUT FFT @ 446mVrms (PGA MODE)
vs
FREQUENCY

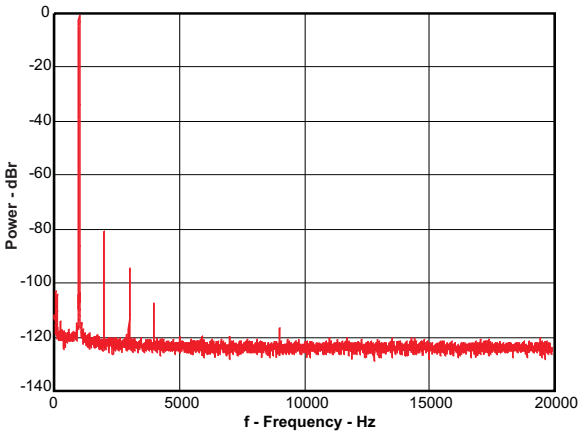


Figure 20.

Typical Circuit Configuration

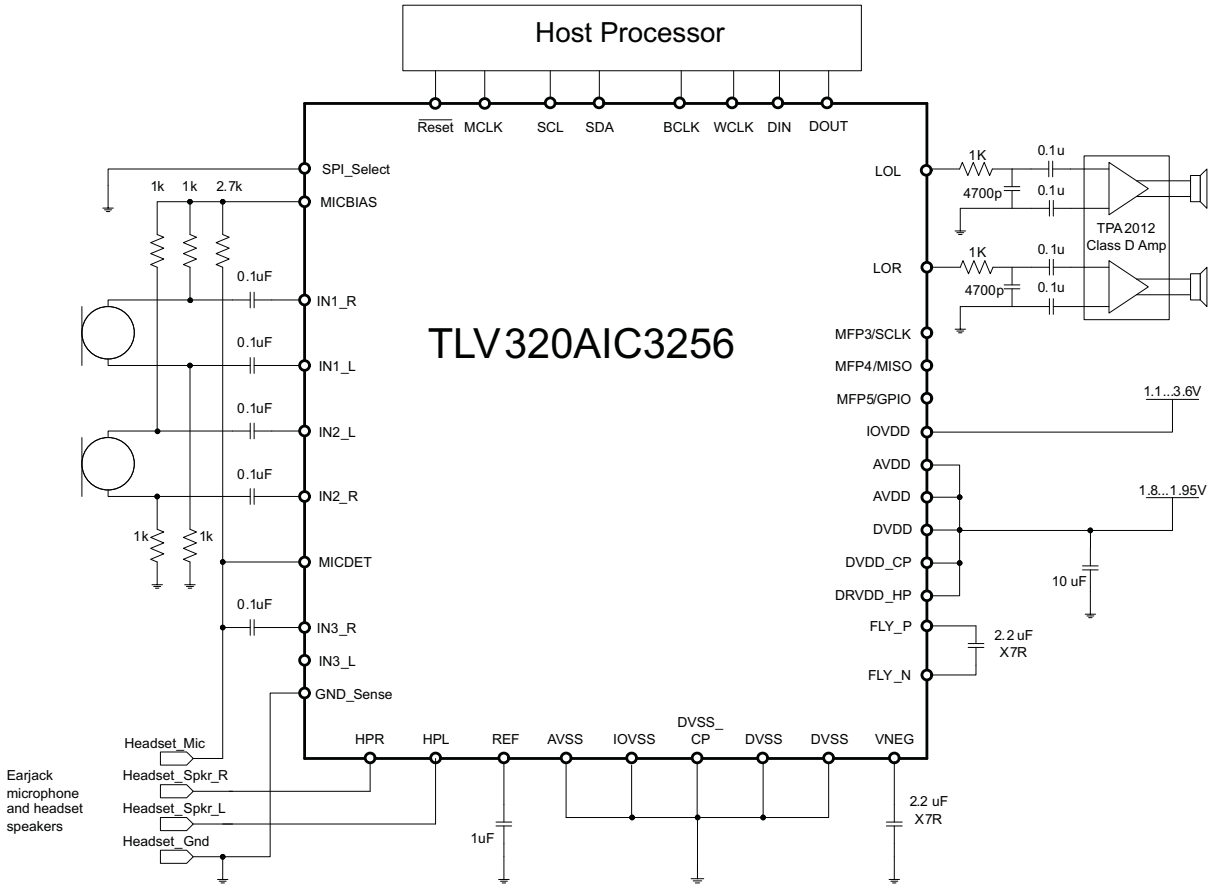


Figure 21. Typical Circuit Configuration

APPLICATION OVERVIEW

The TLV320AIC3256 offers a wide range of configuration options. Figure 1 shows the basic functional blocks of the device.

Device Connections

Digital Pins

Only a small number of digital pins are dedicated to a single function; whenever possible, the digital pins have a default function, and also can be reprogrammed to cover alternative functions for various applications.

The fixed-function pins are Reset and the SPI_Select pin, which are HW control pins. Depending on the state of SPI_Select, the two control-bus pins SCL/$\overline{SS}$ and SDA/MOSI are configured for either I^2C or SPI protocol.

Other digital IO pins can be configured for various functions via register control. An overview of available functionality is given in Multifunction Pins.

Analog Pins

Analog functions can also be configured to a large degree. For minimum power consumption, analog blocks are powered down by default. The blocks can be powered up with fine granularity according to the application needs.

Multifunction Pins

Table 9 shows the possible allocation of pins for specific functions. The PLL input, for example, can be programmed to be any of 4 pins (MCLK, BCLK, DIN, GPIO).

Table 9. Multifunction Pin Assignments

		1	2	3	4	5	6	7	8
	Pin Function	**MCLK**	**BCLK**	**WCLK**	**DIN MFP1**	**DOUT MFP2**	**DMDIN/ MFP3/ SCLK**	**DMCLK/ MFP4/ MISO**	**GPIO MFP5**
A	PLL Input	S(1)	S(2)		E				S(3)
B	Codec Clock Input	S(1) ,D(4)	S(2)						S(3)
C	I^2S BCLK input		S(2),D						
D	I^2S BCLK output		E(5)						
E	I^2S WCLK input			E, D					
F	I^2S WCLK output			E					
G	I^2S ADC word clock input						E		E
H	I^2S ADC WCLK out							E	E
I	I^2S DIN				E, D				
J	I^2S DOUT					E, D			
K	General Purpose Output I					E			
K	General Purpose Output II							E	
K	General Purpose Output III								E
L	General Purpose Input I				E				
L	General Purpose Input II						E		
L	General Purpose Input III								E
M	INT1 output					E		E	E
N	INT2 output					E		E	E
Q	Secondary I^2S BCLK input						E		E
R	Secondary I^2S WCLK in						E		E
S	Secondary I^2S DIN						E		E
T	Secondary I^2S DOUT							E	
U	Secondary I^2S BCLK OUT					E		E	E
V	Secondary I^2S WCLK OUT					E		E	E
X	Aux Clock Output					E		E	E

(1) S(1): The MCLK pin can be used to drive the PLL and Codec Clock inputs **simultaneously**
(2) S(2): The BCLK pin can be used to drive the PLL and Codec Clock and audio interface bit clock inputs **simultaneously**
(3) S(3): The GPIO/MFP5 pin can be used to drive the PLL and Codec Clock inputs simultaneously
(4) D: Default Function
(5) E: The pin is **exclusively** used for this function, no other function can be implemented with the same pin (e.g. if GPIO/MFP5 has been allocated for General Purpose Output, it cannot be used as the INT1 output at the same time)

Analog Audio I/O

The analog I/O path of the TLV320AIC3256 features a large set of options for signal conditioning as well as signal routing:

- 6 analog inputs which can be mixed and/or multiplexed in single-ended and/or differential configuration
- 2 programmable gain amplifiers (PGA) with a range of 0 to +47.5dB
- 2 mixer amplifiers for analog bypass
- 2 low power analog bypass channels
- Mute function
- Channel-to-channel phase adjustment
- Fast charge of ac-coupling capacitors
- Anti thump

Analog Low Power Bypass

The TLV320AIC3256 offers two analog-bypass modes. In either of the modes, an analog input signal can be routed from an analog input pin to an amplifier driving an analog output pin. Neither the ADC nor the DAC resources are required for such operation; this supports low-power operation during analog-bypass mode.

In analog low-power bypass mode, line-level signals can be routed directly from the analog inputs IN1_L to the left headphone amplifier (HPL) and IN1_R to HPR.

ADC Bypass Using Mixer Amplifiers

In addition to the low-power bypass mode, there is a bypass mode that uses the programmable gain amplifiers of the input stage in conjunction with a mixer amplifier. With this mode, microphone-level signals can be amplified and routed to the line or headphone outputs, fully bypassing the ADC and DAC.

To enable this mode, the mixer amplifiers are powered on via software command.

Headphone Output

The stereo headphone drivers on pins HPL and HPR can drive loads with impedances down to 16Ω in single-ended DC-coupled headphone configurations. An integral charge pump generates the negative supply required to operate the headphone drivers in dc-coupled mode, where the common mode of the output signal is made equal to the ground of the headphone load using a ground-sense circuit. Operation of headphone drivers in dc-coupled (ground centered mode) eliminates the need for large dc-blocking capacitors.

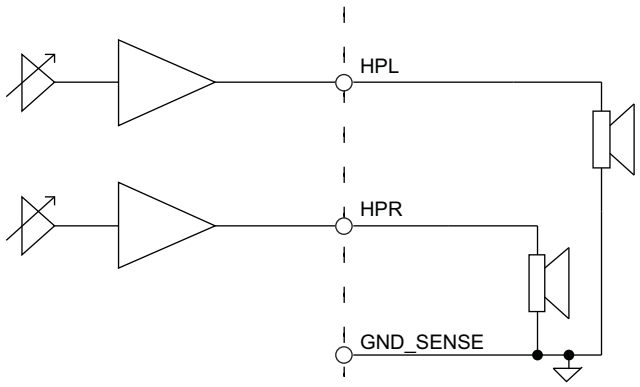


Figure 22. TLV320AIC3256 Ground-Centered Headphone Output

Alternatively the headphone amplifier can also be operated in a unipolar circuit configuration using DC blocking capacitors.

Line Outputs

Line Out Amplifier Overview

The stereo line level drivers on LOL and LOR pins can drive a wide range of line level resistive impedances in the range of 600Ω to 10kΩ. The output common modes of line level drivers can be configured to equal either the analog input common-mode setting, or 1.65V. With output common-mode setting of 1.65V and DRVdd_HP supply at 3.3V the line-level drivers can drive up to 1Vrms output signal. The line-level drivers can drive out a mixed combination of DAC signal and attenuated ADC PGA signal. Signal mixing is register-programmable.

ADC

The TLV320AIC3256 includes a stereo audio ADC, which uses a delta-sigma modulator with a programmable oversampling ratio, followed by a digital decimation filter. The ADC supports sampling rates from 8kHz to 192kHz. In order to provide optimal system power management, the stereo recording path can be powered up one channel at a time, to support the case where only mono record capability is required.

The ADC path of the TLV320AIC3256 features a large set of options for signal conditioning as well as signal routing:

- 2 ADCs
- 6 analog inputs which can be mixed and/or multiplexed in single-ended and/or differential configuration
- 2 programmable gain amplifiers (PGA) with a range of 0 to +47.5dB
- 2 mixer amplifiers for analog bypass
- 2 low power analog bypass channels
- Fine gain adjust of digital channels with 0.1 dB step size
- Digital volume control with a range of -12 to +20dB
- Mute function

In addition to the standard set of ADC features the TLV320AIC3256 also offers the following special functions:

- Channel-to-channel phase adjustment
- Fast charge of ac-coupling capacitors
- Anti thump
- Adaptive filter mode

ADC Processing

The TLV320AIC3256 ADC channel includes a built-in digital decimation filter to process the oversampled data from the to generate digital data at Nyquist sampling rate with high dynamic range. The decimation filter can be chosen from three different types, depending on the required frequency response, group delay and sampling rate.

ADC Processing Blocks

The TLV320AIC3256 offers a range of processing blocks which implement various signal processing capabilities along with decimation filtering. These processing blocks give users the choice of how much and what type of signal processing they may use and which decimation filter is applied.

The choice between these processing blocks is part of the PowerTune strategy to balance power conservation and signal-processing flexibility. Less signal-processing capability reduces the power consumed by the device. Table 10 gives an overview of the available processing blocks of the ADC channel and their properties. The Resource Class Column (RC) gives an approximate indication of power consumption.

The signal processing blocks available are:

- First-order IIR
- Scalable number of biquad filters
- Variable-tap FIR filter

The processing blocks are tuned for common cases and can achieve high anti-alias filtering or low-group delay in combination with various signal processing effects such as audio effects and frequency shaping. The available first order IIR, BiQuad and FIR filters have fully user-programmable coefficients. The Resource Class Column (RC) gives an approximate indication of power consumption.

Table 10. ADC Processing Blocks

Processing Blocks	Channel	Decimation Filter	1st Order IIR Available	Number BiQuads	FIR	Required AOSR Value	Resource Class
PRB_R1(1)	Stereo	A	Yes	0	No	128,64	6
PRB_R2	Stereo	A	Yes	5	No	128,64	8
PRB_R3	Stereo	A	Yes	0	25-Tap	128,64	8
PRB_R4	Right	A	Yes	0	No	128,64	3
PRB_R5	Right	A	Yes	5	No	128,64	4
PRB_R6	Right	A	Yes	0	25-Tap	128,64	4
PRB_R7	Stereo	B	Yes	0	No	64	3
PRB_R8	Stereo	B	Yes	3	No	64	4
PRB_R9	Stereo	B	Yes	0	20-Tap	64	4
PRB_R10	Right	B	Yes	0	No	64	2
PRB_R11	Right	B	Yes	3	No	64	2
PRB_R12	Right	B	Yes	0	20-Tap	64	2
PRB_R13	Stereo	C	Yes	0	No	32	3
PRB_R14	Stereo	C	Yes	5	No	32	4
PRB_R15	Stereo	C	Yes	0	25-Tap	32	4
PRB_R16	Right	C	Yes	0	No	32	2
PRB_R17	Right	C	Yes	5	No	32	2
PRB_R18	Right	C	Yes	0	25-Tap	32	2

(1) Default

For more detailed information see the Application Reference Guide, SLAU306

DAC

The TLV320AIC3256 includes a stereo audio DAC supporting data rates from 8kHz to 192kHz. Each channel of the stereo audio DAC consists of a signal-processing engine with fixed processing blocks, a programmable miniDSP, a digital interpolation filter, multi-bit digital delta-sigma modulator, and an analog reconstruction filter. The DAC is designed to provide enhanced performance at low sampling rates through increased oversampling and image filtering, thereby keeping quantization noise generated within the delta-sigma modulator and signal images strongly suppressed within the audio band to beyond 20kHz. To handle multiple input rates and optimize power dissipation and performance, the TLV320AIC3256 allows the system designer to program the oversampling rates over a wide range from 1 to 1024. The system designer can choose higher oversampling ratios for lower input data rates and lower oversampling ratios for higher input data rates.

The TLV320AIC3256 DAC channel includes a built-in digital interpolation filter to generate oversampled data for the sigma-delta modulator. The interpolation filter can be chosen from three different types depending on required frequency response, group delay and sampling rate.

The DAC path of the TLV320AIC3256 features many options for signal conditioning and signal routing:

- 2 headphone amplifiers
  - Ground-centered, bipolar operation or unipolar operation
  - Usable in single-ended or differential mode
  - Analog volume setting with a range of -6 to +14 dB
- 2 line-out amplifiers
  - Usable in single-ended or differential mode
  - Analog volume setting with a range of -6 to +29 dB
- Digital volume control with a range of -63.5 to +24dB
- Mute function
- Dynamic range compression (DRC)

In addition to the standard set of DAC features the TLV320AIC3256 also offers the following special features:

- Built in sine wave generation (beep generator)
- Digital auto mute
- Adaptive filter mode

DAC Processing Blocks — Overview

The TLV320AIC3256 implements signal processing capabilities and interpolation filtering via processing blocks. These fixed processing blocks give users the choice of how much and what type of signal processing they may use and which interpolation filter is applied.

The choice between these processing blocks is part of the PowerTune strategy balancing power conservation and signal processing flexibility. Less signal processing capability will result in less power consumed by the device. Table 11 gives an overview over all available processing blocks of the DAC channel and their properties. The Resource Class Column (RC) gives an approximate indication of power consumption.

The signal processing blocks available are:

- First-order IIR
- Scalable number of biquad filters
- 3D – Effect
- Beep Generator

The processing blocks are tuned for typical cases and can achieve high image rejection or low group delay in combination with various signal processing effects such as audio effects and frequency shaping. The available first-order IIR and biquad filters have fully user-programmable coefficients. The Resource Class Column (RC) gives an approximate indication of power consumption.

Table 11. Overview – DAC Predefined Processing Blocks

Processing Block No.	Interpolation Filter	Channel	1st Order IIR Available	Num. of Biquads	DRC	3D	Beep Generator	Resource Class
PRB_P1(1)	A	Stereo	No	3	No	No	No	8
PRB_P2	A	Stereo	Yes	6	Yes	No	No	12
PRB_P3	A	Stereo	Yes	6	No	No	No	10
PRB_P4	A	Left	No	3	No	No	No	4
PRB_P5	A	Left	Yes	6	Yes	No	No	6
PRB_P6	A	Left	Yes	6	No	No	No	6
PRB_P7	B	Stereo	Yes	0	No	No	No	6
PRB_P8	B	Stereo	No	4	Yes	No	No	8
PRB_P9	B	Stereo	No	4	No	No	No	8
PRB_P10	B	Stereo	Yes	6	Yes	No	No	10
PRB_P11	B	Stereo	Yes	6	No	No	No	8
PRB_P12	B	Left	Yes	0	No	No	No	3
PRB_P13	B	Left	No	4	Yes	No	No	4
PRB_P14	B	Left	No	4	No	No	No	4
PRB_P15	B	Left	Yes	6	Yes	No	No	6
PRB_P16	B	Left	Yes	6	No	No	No	4
PRB_P17	C	Stereo	Yes	0	No	No	No	3
PRB_P18	C	Stereo	Yes	4	Yes	No	No	6
PRB_P19	C	Stereo	Yes	4	No	No	No	4
PRB_P20	C	Left	Yes	0	No	No	No	2
PRB_P21	C	Left	Yes	4	Yes	No	No	3
PRB_P22	C	Left	Yes	4	No	No	No	2
PRB_P23	A	Stereo	No	2	No	Yes	No	8
PRB_P24	A	Stereo	Yes	5	Yes	Yes	No	12
PRB_P25	A	Stereo	Yes	5	Yes	Yes	Yes	12

(1) Default

For more detailed information see the Application Reference Guide, SLAU306

Digital Audio I/O Interface

Audio data is transferred between the host processor and the TLV320AIC3256 via the digital audio data serial interface, or audio bus. The audio bus on this device is very flexible, including left or right-justified data options, support for I^2S or PCM protocols, programmable data length options, a TDM mode for multichannel operation, very flexible master/slave configurability for each bus clock line, and the ability to communicate with multiple devices within a system directly.

The audio bus of the TLV320AIC3256 can be configured for left or right-justified, I^2S, DSP, or TDM modes of operation, where communication with standard PCM interfaces is supported within the TDM mode. These modes are all MSB-first, with data width programmable as 16, 20, 24, or 32 bits by configuring Page 0, Register 27, D(5:4). In addition, the word clock and bit clock can be independently configured in either Master or Slave mode, for flexible connectivity to a wide variety of processors. The word clock is used to define the beginning of a frame, and may be programmed as either a pulse or a square-wave signal. The frequency of this clock corresponds to the maximum of the selected ADC and DAC sampling frequencies.

The bit clock is used to clock in and clock out the digital audio data across the serial bus. When in Master mode, this signal can be programmed to generate variable clock pulses by controlling the bit-clock divider in Page 0, Register 30. The number of bit-clock pulses in a frame may need adjustment to accommodate various word-lengths as well as to support the case when multiple TLV320AIC3256s may share the same audio bus.

The TLV320AIC3256 also includes a feature to offset the position of start of data transfer with respect to the word-clock. This offset can be controlled in terms of number of bit-clocks and can be programmed in Page 0, Register 28.

The TLV320AIC3256 also has the feature of inverting the polarity of the bit-clock used for transferring the audio data as compared to the default clock polarity used. This feature can be used independently of the mode of audio interface chosen. This can be configured via Page 0, Register 29, D(3).

The TLV320AIC3256 further includes programmability (Page 0, Register 27, D0) to place the DOUT line into a hi-Z (3-state) condition during all bit clocks when valid data is not being sent. By combining this capability with the ability to program at what bit clock in a frame the audio data begins, time-division multiplexing (TDM) can be accomplished, enabling the use of multiple codecs on a single audio serial data bus. When the audio serial data bus is powered down while configured in master mode, the pins associated with the interface are put into a hi-Z output condition.

By default when the word-clocks and bit-clocks are generated by the TLV320AIC3256, these clocks are active only when the codec (ADC, DAC or both) are powered up within the device. This is done to save power. However, it also supports a feature when both the word clocks and bit-clocks can be active even when the codec in the device is powered down. This is useful when using the TDM mode with multiple codecs on the same bus, or when word-clock or bit-clocks are used in the system as general-purpose clocks.

Clock Generation and PLL

The TLV320AIC3256 supports a wide range of options for generating clocks for the ADC and DAC sections as well as interface and other control blocks. The clocks for ADC and DAC require a source reference clock. This clock can be provided on variety of device pins such as MCLK, BCLK or GPI pins. The CODEC_CLKIN can then be routed through highly-flexible clock dividers to generate the various clocks required for ADC, DAC and the miniDSP sections. In the event that the desired audio or miniDSP clocks cannot be generated from the reference clocks on MCLK BCLK or GPIO, the TLV320AIC3256 also provides the option of using the on-chip PLL which supports a wide range of fractional multiplication values to generate the required clocks. Starting from CODEC_CLKIN the TLV320AIC3256 provides several programmable clock dividers to help achieve a variety of sampling rates for ADC, DAC and clocks for the miniDSP .

To minimize power consumption, the system ideally provides a master clock that is a suitable integer multiple of the desired sampling frequencies. In such cases, internal dividers can be programmed to set up the required internal clock signals at very low power consumption. For cases where such master clocks are not available, the built-in PLL can be used to generate a clock signal that serves as an internal master clock. In fact, this master clock can also be routed to an output pin and may be used elsewhere in the system. The clock system is flexible enough that it even allows the internal clocks to be derived directly from an external clock source, while the PLL is used to generate some other clock that is only used outside the TLV320AIC3256.

For more detailed information see the Application Reference Guide, SLAU306

Control Interfaces

The TLV320AIC3256 control interface supports SPI or I^2C communication protocols, with the protocol selectable using the SPI_SELECT pin. For SPI, SPI_SELECT should be tied high; for I^2C, SPI_SELECT should be tied low. It is not recommended to change the state of SPI_SELECT during device operation.

I^2C Control

The TLV320AIC3256 supports the I^2C control protocol, and will respond to the I^2C address of 0011000. I^2C is a two-wire, open-drain interface supporting multiple devices and masters on a single bus. Devices on the I^2C bus only drive the bus lines LOW by connecting them to ground; they never drive the bus lines HIGH. Instead, the bus wires are pulled HIGH by pullup resistors, so the bus wires are HIGH when no device is driving them LOW. This way, two devices cannot conflict; if two devices drive the bus simultaneously, there is no driver contention.

SPI Control

In the SPI control mode, the TLV320AIC3256 uses the pins SCL/$\overline{SS}$ as $\overline{SS}$, SCLK as SCLK, MISO as MISO, SDA/MOSI as MOSI; a standard SPI port with clock polarity setting of 0 (typical microprocessor SPI control bit CPOL = 0). The SPI port allows full-duplex, synchronous, serial communication between a host processor (the master) and peripheral devices (slaves). The SPI master (in this case, the host processor) generates the synchronizing clock (driven onto SCLK) and initiates transmissions. The SPI slave devices (such as the TLV320AIC3256) depend on a master to start and synchronize transmissions. A transmission begins when initiated by an SPI master. The byte from the SPI master begins shifting in on the slave MOSI pin under the control of the master serial clock (driven onto SCLK). As the byte shifts in on the MOSI pin, a byte shifts out on the MISO pin to the master shift register.

For more detailed information see the Application Reference Guide, SLAU306

Power Supply

The device has an integrated charge pump. Using the device in ground-centered headphone configuration, it can be conveniently supplied from a single 1.5V to 1.95V rail. It has separate power domains for digital IO, digital core, analog core, charge-pump input and headphone drive, all of which can be connected together and be supplied from one source. For improved power efficiency, the digital core voltage can range from 1.26V to 1.95V. The IO voltage can be supplied in the range of 1.1V to 3.6V.

For more detailed information see the TLV320AIC3256Application Reference Guide, SLAU306

Device Special Functions

The following special functions are available to support advanced system requirements:

- Headset detection
- Interrupt generation
- Flexible pin multiplexing

For more detailed information see the Application Reference Guide, SLAU306

Register Map Summary

Table 12. Summary of Register Map

Decimal		Hex		DESCRIPTION
PAGE NO.	REG. NO.	PAGE NO.	REG. NO.	
0	0	0x00	0x00	Page Select Register
0	1	0x00	0x01	Software Reset Register
0	2	0x00	0x02	Reserved Register
0	3	0x00	0x03	Reserved Register
0	4	0x00	0x04	Clock Setting Register 1, Multiplexers
0	5	0x00	0x05	Clock Setting Register 2, PLL P&R Values
0	6	0x00	0x06	Clock Setting Register 3, PLL J Values
0	7	0x00	0x07	Clock Setting Register 4, PLL D Values (MSB)
0	8	0x00	0x08	Clock Setting Register 5, PLL D Values (LSB)
0	9-10	0x00	0x09-0x0A	Reserved Register
0	11	0x00	0x0B	Clock Setting Register 6, NDAC Values
0	12	0x00	0x0C	Clock Setting Register 7, MDAC Values
0	13	0x00	0x0D	DAC OSR Setting Register 1, MSB Value
0	14	0x00	0x0E	DAC OSR Setting Register 2, LSB Value
0	15	0x00	0x0F	miniDSP_D Instruction Control Register 1
0	16	0x00	0x10	miniDSP_D Instruction Control Register 2
0	17	0x00	0x11	miniDSP_D Interpolation Factor Setting Register

Table 12. Summary of Register Map (continued)

Decimal		Hex		DESCRIPTION
PAGE NO.	REG. NO.	PAGE NO.	REG. NO.	
0	18	0x00	0x12	Clock Setting Register 8, NADC Values
0	19	0x00	0x13	Clock Setting Register 9, MADC Values
0	20	0x00	0x14	ADC Oversampling (AOSR) Register
0	21	0x00	0x15	miniDSP_A Instruction Control Register 1
0	22	0x00	0x16	miniDSP_A Instruction Control Register 2
0	23	0x00	0x17	miniDSP_A Decimation Factor Setting Register
0	24	0x00	0x18	Reserved Register
0	25	0x00	0x19	Clock Setting Register 10, Multiplexers
0	26	0x00	0x1A	Clock Setting Register 11, CLKOUT M divider value
0	27	0x00	0x1B	Audio Interface Setting Register 1
0	28	0x00	0x1C	Audio Interface Setting Register 2, Data offset setting
0	29	0x00	0x1D	Audio Interface Setting Register 3
0	30	0x00	0x1E	Clock Setting Register 12, BCLK N Divider
0	31	0x00	0x1F	Audio Interface Setting Register 4, Secondary Audio Interface
0	32	0x00	0x20	Audio Interface Setting Register 5
0	33	0x00	0x21	Audio Interface Setting Register 6
0	34	0x00	0x22	Digital Interface Misc. Setting Register
0	35	0x00	0x23	Reserved Register
0	36	0x00	0x24	ADC Flag Register
0	37	0x00	0x25	DAC Flag Register 1
0	38	0x00	0x26	DAC Flag Register 2
0	39-41	0x00	0x27-0x29	Reserved Register
0	42	0x00	0x2A	Sticky Flag Register 1
0	43	0x00	0x2B	Interrupt Flag Register 1
0	44	0x00	0x2C	Sticky Flag Register 2
0	45	0x00	0x2D	Sticky Flag Register 3
0	46	0x00	0x2E	Interrupt Flag Register 2
0	47	0x00	0x2F	Interrupt Flag Register 3
0	48	0x00	0x30	INT1 Interrupt Control Register
0	49	0x00	0x31	INT2 Interrupt Control Register
0	50-51	0x00	0x32-0x33	Reserved Register
0	52	0x00	0x34	GPIO/MFP5 Control Register
0	53	0x00	0x35	DOUT/MFP2 Function Control Register
0	54	0x00	0x36	DIN/MFP1 Function Control Register
0	55	0x00	0x37	MISO/MFP4 Function Control Register
0	56	0x00	0x38	SCLK/MFP3 Function Control Register
0	57-59	0x00	0x39-0x3B	Reserved Registers
0	60	0x00	0x3C	DAC Signal Processing Block Control Register
0	61	0x00	0x3D	ADC Signal Processing Block Control Register
0	62	0x00	0x3E	miniDSP_A and miniDSP_D Configuration Register
0	63	0x00	0x3F	DAC Channel Setup Register 1
0	64	0x00	0x40	DAC Channel Setup Register 2
0	65	0x00	0x41	Left DAC Channel Digital Volume Control Register
0	66	0x00	0x42	Right DAC Channel Digital Volume Control Register
0	67	0x00	0x43	Headset Detection Configuration Register
0	68	0x00	0x44	DRC Control Register 1

Table 12. Summary of Register Map (continued)

Decimal		Hex		DESCRIPTION
PAGE NO.	REG. NO.	PAGE NO.	REG. NO.	
0	69	0x00	0x45	DRC Control Register 2
0	70	0x00	0x46	DRC Control Register 3
0	71	0x00	0x47	Beep Generator Register 1
0	72	0x00	0x48	Beep Generator Register 2
0	73	0x00	0x49	Beep Generator Register 3
0	74	0x00	0x4A	Beep Generator Register 4
0	75	0x00	0x4B	Beep Generator Register 5
0	76	0x00	0x4C	Beep Generator Register 6
0	77	0x00	0x4D	Beep Generator Register 7
0	78	0x00	0x4E	Beep Generator Register 8
0	79	0x00	0x4F	Beep Generator Register 9
0	80	0x00	0x50	Reserved Register
0	81	0x00	0x51	ADC Channel Setup Register
0	82	0x00	0x52	ADC Fine Gain Adjust Register
0	83	0x00	0x53	Left ADC Channel Volume Control Register
0	84	0x00	0x54	Right ADC Channel Volume Control Register
0	85	0x00	0x55	ADC Phase Adjust Register
0	86	0x00	0x56	Left Channel AGC Control Register 1
0	87	0x00	0x57	Left Channel AGC Control Register 2
0	88	0x00	0x58	Left Channel AGC Control Register 3
0	89	0x00	0x59	Left Channel AGC Control Register 4
0	90	0x00	0x5A	Left Channel AGC Control Register 5
0	91	0x00	0x5B	Left Channel AGC Control Register 6
0	92	0x00	0x5C	Left Channel AGC Control Register 7
0	93	0x00	0x5D	Left Channel AGC Control Register 8
0	94	0x00	0x5E	Right Channel AGC Control Register 1
0	95	0x00	0x5F	Right Channel AGC Control Register 2
0	96	0x00	0x60	Right Channel AGC Control Register 3
0	97	0x00	0x61	Right Channel AGC Control Register 4
0	98	0x00	0x62	Right Channel AGC Control Register 5
0	99	0x00	0x63	Right Channel AGC Control Register 6
0	100	0x00	0x64	Right Channel AGC Control Register 7
0	101	0x00	0x65	Right Channel AGC Control Register 8
0	102	0x00	0x66	DC Measurement Register 1
0	103	0x00	0x67	DC Measurement Register 2
0	104	0x00	0x68	Left Channel DC Measurement Output Register 1
0	105	0x00	0x69	Left Channel DC Measurement Output Register 2
0	106	0x00	0x6A	Left Channel DC Measurement Output Register 3
0	107	0x00	0x6B	Right Channel DC Measurement Output Register 1
0	108	0x00	0x6C	Right Channel DC Measurement Output Register 2
0	109	0x00	0x6D	Right Channel DC Measurement Output Register 3
0	110-127	0x00	0x6E-0x7F	Reserved Register
1	0	0x01	0x00	Page Select Register
1	1	0x01	0x01	Power Configuration Register 1
1	2	0x01	0x02	Power Configuration Register 2
1	3	0x01	0x03	Playback Configuration Register 1

Table 12. Summary of Register Map (continued)

Decimal		Hex		DESCRIPTION
PAGE NO.	REG. NO.	PAGE NO.	REG. NO.	
1	4	0x01	0x04	Playback Configuration Register 2
1	5-8	0x01	0x05-0x08	Reserved Register
1	9	0x01	0x09	Output Driver Power Control Register
1	10	0x01	0x0A	Common Mode Control Register
1	11	0x01	0x0B	Over Current Protection Configuration Register
1	12	0x01	0x0C	HPL Routing Selection Register
1	13	0x01	0x0D	HPR Routing Selection Register
1	14	0x01	0x0E	LOL Routing Selection Register
1	15	0x01	0x0F	LOR Routing Selection Register
1	16	0x01	0x10	HPL Driver Gain Setting Register
1	17	0x01	0x11	HPR Driver Gain Setting Register
1	18	0x01	0x12	LOL Driver Gain Setting Register
1	19	0x01	0x13	LOR Driver Gain Setting Register
1	20	0x01	0x14	Headphone Driver Startup Control Register
1	21	0x01	0x15	Reserved Register
1	22	0x01	0x16	IN1L to HPL Volume Control Register
1	23	0x01	0x17	IN1R to HPR Volume Control Register
1	24	0x01	0x18	Mixer Amplifier Left Volume Control Register
1	25	0x01	0x19	Mixer Amplifier Right Volume Control Register
1	26-50	0x01	0x1A-0x32	Reserved Register
1	51	0x01	0x33	MICBIAS Configuration Register
1	52	0x01	0x34	Left MICPGA Positive Terminal Input Routing Configuration Register
1	53	0x01	0x35	Reserved Register
1	54	0x01	0x36	Left MICPGA Negative Terminal Input Routing Configuration Register
1	55	0x01	0x37	Right MICPGA Positive Terminal Input Routing Configuration Register
1	56	0x01	0x38	Reserved Register
1	57	0x01	0x39	Right MICPGA Negative Terminal Input Routing Configuration Register
1	58	0x01	0x3A	Floating Input Configuration Register
1	59	0x01	0x3B	Left MICPGA Volume Control Register
1	60	0x01	0x3C	Right MICPGA Volume Control Register
1	61	0x01	0x3D	ADC Power Tune Configuration Register
1	62	0x01	0x3E	ADC Analog Volume Control Flag Register
1	63	0x01	0x3F	DAC Analog Gain Control Flag Register
1	64-70	0x01	0x40-0x46	Reserved Register
1	71	0x01	0x47	Analog Input Quick Charging Configuration Register
1	72-122	0x01	0x48-0x7A	Reserved Register
1	123	0x01	0x7B	Reference Power-up Configuration Register
1	124	0x01	0x7C	Charge Pump Control
1	125	0x01	0x7D	Headphone Driver Configuration
1	126-127	0x01	0x7E-0x7F	Reserved Register
26-34	0	0x1A-0x22	0x00	Page Select Register
26-34	1-7	0x1A-0x22	0x01-0x07	Reserved.
26-34	8-127	0x1A-0x22	0x08-0x7F	ADC Coefficients Buffer-B C(0:255)
44	0	0x2C	0x00	Page Select Register
44	1	0x2C	0x01	DAC Adaptive Filter Configuration Register
44	2-7	0x2C	0x02-0x07	Reserved

Table 12. Summary of Register Map (continued)

Decimal		Hex		DESCRIPTION
PAGE NO.	REG. NO.	PAGE NO.	REG. NO.	
44	8-127	0x2C	0x08-0x7F	DAC Coefficients Buffer-A C(0:29)
45-52	0	0x2D-0x34	0x00	Page Select Register
45-52	1-7	0x2D-0x34	0x01-0x07	Reserved.
45-52	8-127	0x2D-0x34	0x08-0x7F	DAC Coefficients Buffer-A C(30:255)
62-70	0	0x3E-0x46	0x00	Page Select Register
62-70	1-7	0x3E-0x46	0x01-0x07	Reserved.
62-70	8-127	0x3E-0x46	0x08-0x7F	DAC Coefficients Buffer-B C(0:255)
80-114	0	0x50-0x72	0x00	Page Select Register
80-114	1-7	0x50-0x72	0x01-0x07	Reserved.
80-114	8-127	0x50-0x72	0x08-0x7F	miniDSP_A Instructions
152-186	0	0x98-0xBA	0x00	Page Select Register
152-186	1-7	0x98-0xBA	0x01-0x07	Reserved.
152-186	8-127	0x98-0xBA	0x08-0x7F	miniDSP_D Instructions

Additional Package Data, YZK Package

Table 13.

Dim	Value	Unit
X max:	3499.00	µm
X min:	3439.00	
Y max:	3229.00	
Y min:	3239.00	
Notes:		
	Step X:3509.00 x Y:3309.00 µm	
	Step -40µm + 30 µm=max	µm
	Step -40µm – 30 µm=min	

REVISION HISTORY

Changes from Revision initial (December 2010) to Revision A **Page**

- Changed "mV" to "mVRMS" for Input signal level units 9
- Changed Gain Error value from 0.7 to 0.8 10
- Changed Gain Error value from 0.5 to 0.8 10
- Changed Noise, Idle Channel value from 6.9 to 6.7 10
- Changed Bias voltage, Micbias Mode 0 value from 1.25 to 1.23 11
- Changed Bias voltage, Micbias Mode 0 value from 1.25 to 1.23 11
- Changed DAC Gain Error value from 0.4 to 0.5 12
- Changed DAC Gain Error value from 0.1 to 0.5 13
- Changed DAC channel separation condition from –1dB to –3dB 13
- Changed 10µF to 1µF in Reference Noise conditions statement 14
- Deleted min value from Decoupling Capacitor, changed typ value from 10 to 1µF 14
- Moved value from typ to min 14
- Moved value from typ to min 14
- Changed WCLK delay min from 14 to 30ns 15

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TLV320AIC3256IRSBR	ACTIVE	WQFN	RSB	40	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples
TLV320AIC3256IRSBT	ACTIVE	WQFN	RSB	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Request Free Samples

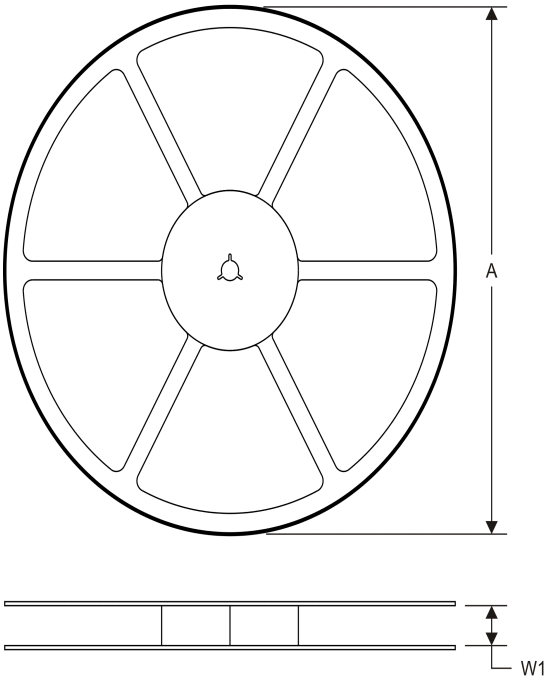
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

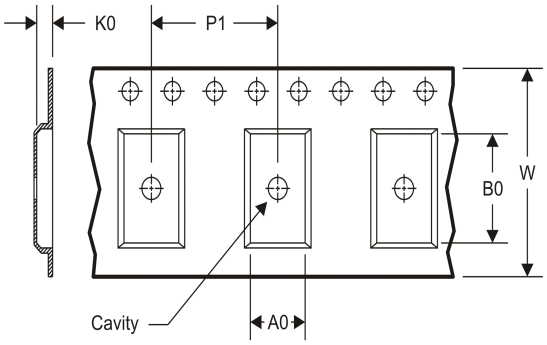
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



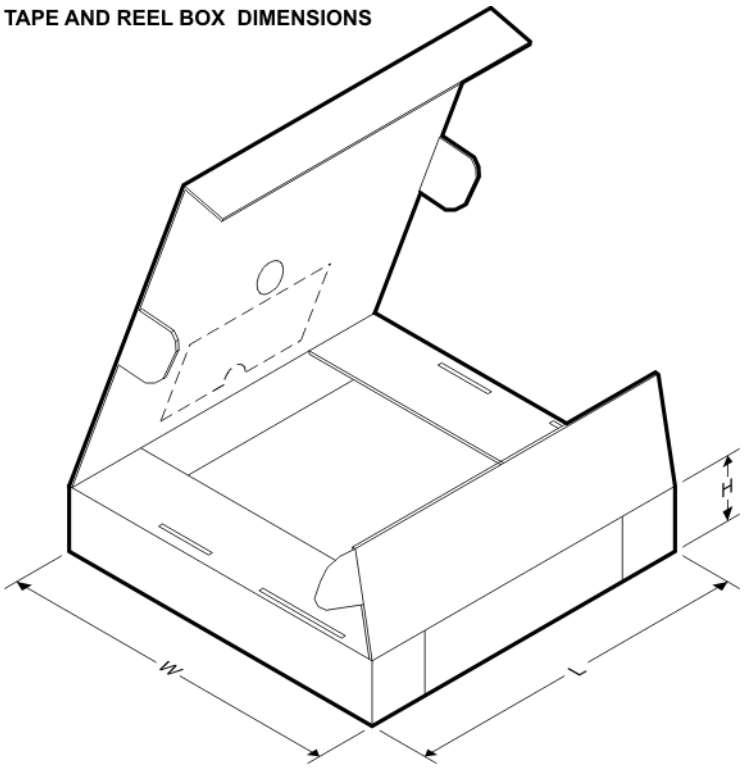
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV320AIC3256IRSBR	WQFN	RSB	40	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TLV320AIC3256IRSBT	WQFN	RSB	40	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

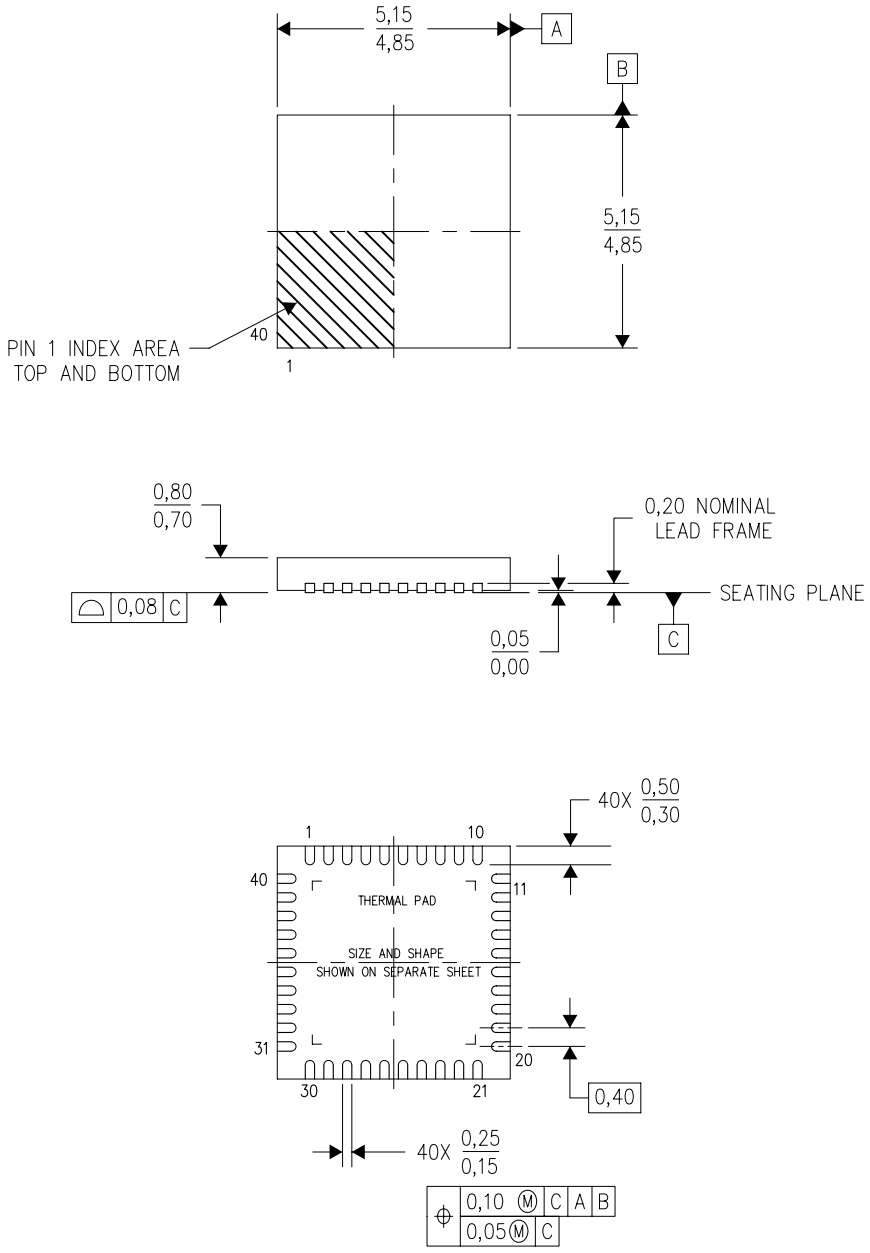
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV320AIC3256IRSBR	WQFN	RSB	40	3000	346.0	346.0	29.0
TLV320AIC3256IRSBT	WQFN	RSB	40	250	210.0	185.0	35.0

RSB (S–PWQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD



4207182/C 05/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

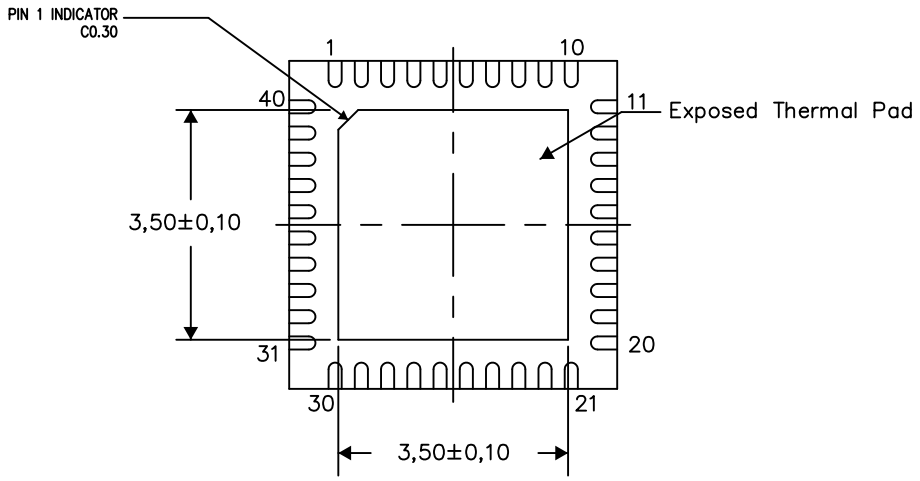
RSB (S–PWQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



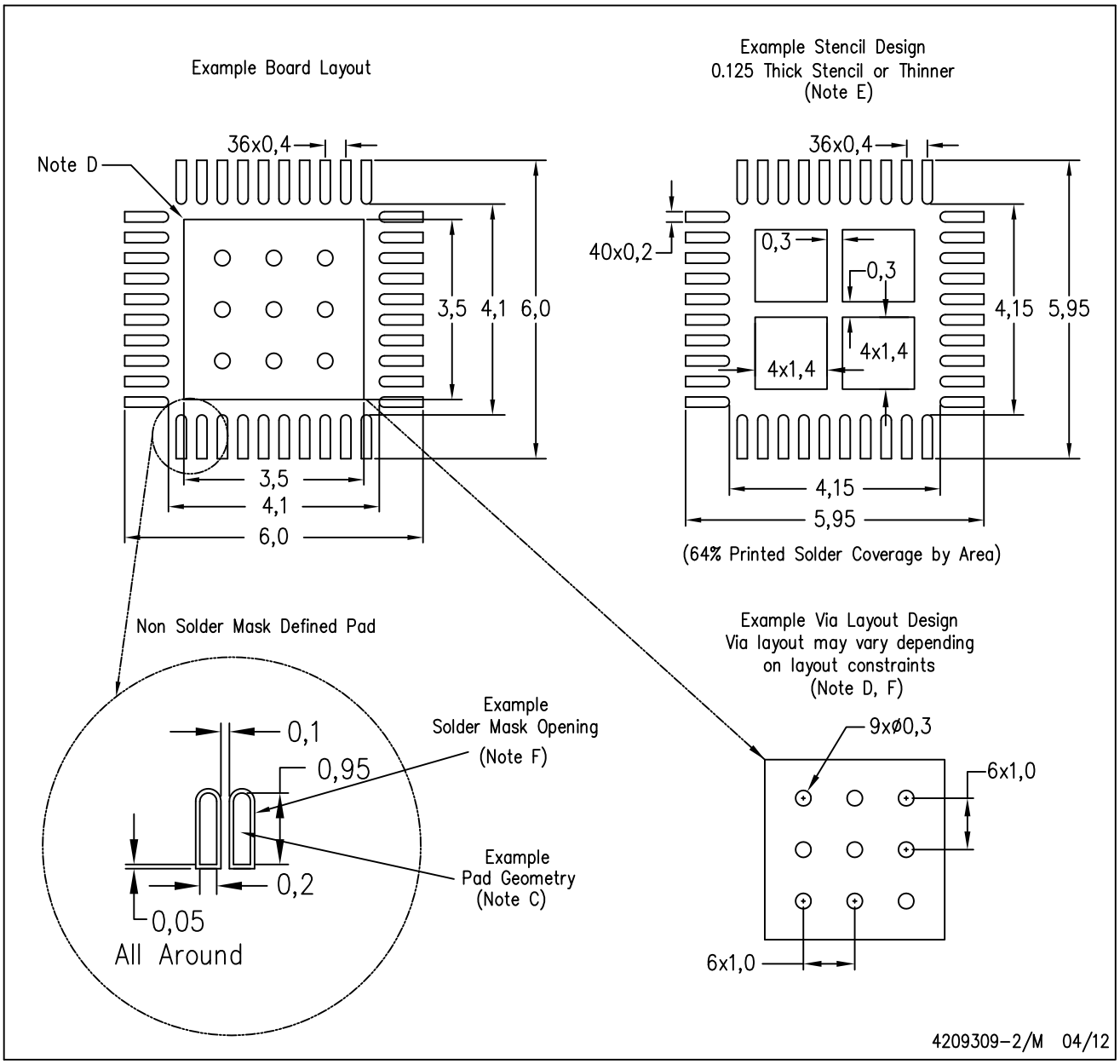
Bottom View

Exposed Thermal Pad Dimensions

4207183–2/N 04/12

NOTE: All linear dimensions are in millimeters

RSB (S–PWQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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