

SBOS035A - DECEMBER 1995 - REVISED APRIL 2007

# **Dual, Low Power INSTRUMENTATION AMPLIFIER**

# **FEATURES**

● LOW OFFSET VOLTAGE: 50µV max

■ LOW DRIFT: 0.5μV/°C max

● LOW INPUT BIAS CURRENT: 5nA max

HIGH CMR: 120dB min

● INPUTS PROTECTED TO ±40V

 WIDE SUPPLY RANGE: ±2.25V to ±18V LOW QUIESCENT CURRENT: 700μA / IA

• 16-PIN PLASTIC DIP, SOL-16

## **APPLICATIONS**

- SENSOR AMPLIFIER THERMOCOUPLE, RTD, BRIDGE
- MEDICAL INSTRUMENTATION
- MULTIPLE-CHANNEL SYSTEMS
- BATTERY OPERATED EQUIPMENT

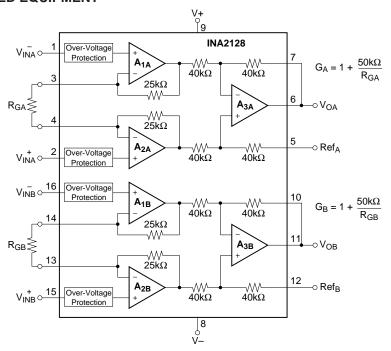
### DESCRIPTION

The INA2128 is a dual, low power, general purpose instrumentation amplifier offering excellent accuracy. Its versatile 3-op amp design and small size make it ideal for a wide range of applications. Current-feedback input circuitry provides wide bandwidth even at high gain (200kHz at G = 100).

A single external resistor sets any gain from 1 to 10,000. Internal input protection can withstand up to ±40V without damage.

The INA2128 is laser-trimmed for very low offset voltage (50μV), drift (0.5μV/°C) and high common-mode rejection (120dB at  $G \ge 100$ ). It operates with power supplies as low as ±2.25V, and quiescent current is only 700μA per IA—ideal for battery-operated and multiple-channel systems.

The INA2128 is available in SOL-16 packages, specified for the -40°C to +85°C temperature range.





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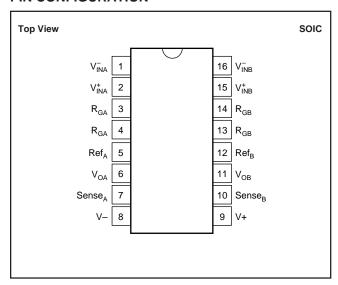


#### **ABSOLUTE MAXIMUM RATINGS(1)**

	Supply Voltage	±40V Continuous —40°C to +125°C
ı	Storage Temperature	
ı	Junction Temperature	+150°C

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.

#### **PIN CONFIGURATION**





# ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	TEMPERATURE RANGE
INA2128UA	SOIC-16	DW	-40°C to +85°C
INA2128U	SOIC-16	DW	-40°C to +85°C

NOTES: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

# **ELECTRICAL CHARACTERISTICS**

At T<sub>A</sub> = +25°C, V<sub>S</sub> =  $\pm 15$ V, R<sub>L</sub> = 10k $\Omega$ , unless otherwise noted.

		INA2128U				INA2128UA		
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT Offset Voltage, RTI								
Initial vs Temperature vs Power Supply Long-Term Stability Impedance, Differential Common-Mode	$T_A = +25^{\circ}\text{C}$ $T_A = T_{MIN} \text{ to } T_{MAX}$ $V_S = \pm 2.25 \text{V to } \pm 18 \text{V}$		±10 ±100/G ±0.2 ± 2/G ±0.2 ±20/G ±0.1 ±3/G 10 <sup>10</sup>    2 10 <sup>11</sup>    9	±50 ±500/G ±0.5 ± 20/G ±1 ±100/G		±25 ±100/G ±0.2 ± 5/G * * * *	±125 ±1000/G   ±1 ± 20/G   ±2 ±200/G	μV μV/°C μV/V μV/mo Ω    pF
Common-Mode Voltage Range Safe Input Voltage	$V_O = 0V$	(V+) - 2 (V-) + 2	(V+) - 1.4 (V-) + 1.7	±40	*	* *	*	Ω    pF V V V
Common-Mode Rejection	$V_{CM} = \pm 13V, \Delta R_S = 1k\Omega$ G=1 G=10 G=100 G=1000	80 100 120 120	86 106 125 130	210	73 93 110 110	* * * *	·	dB dB dB dB
BIAS CURRENT vs Temperature Offset Current vs Temperature			±2 ±30 ±1 ±30	±5 ±5		* * * *	±10 ±10	nA pA/°C nA pA/°C
NOISE VOLTAGE, RTI f = 10Hz f = 100Hz f = 1kHz $f_B = 0.1Hz$ to $10Hz$ Noise Current	$G = 1000, R_S = 0\Omega$		10 8 8 0.2			* * *		nV/√ <u>Hz</u> nV/√ <u>Hz</u> nV/√Hz μV <sub>PP</sub>
f=10Hz f=1kHz f <sub>B</sub> = 0.1Hz to 10Hz			0.9 0.3 30			* * *		pA/√ <u>Hz</u> pA/√Hz pA <sub>PP</sub>
GAIN Gain Equation Range of Gain Gain Error	G=1 G=10 G=100 G=1000	1	1 + (50kΩ/R <sub>G</sub> ) ±0.01 ±0.02 ±0.05	10000 ±0.024 ±0.4 ±0.5	*	* * * *	* ±0.1 ±0.5 ±0.7	V/V V/V % %
Gain vs Temperature <sup>(2)</sup> $50 \text{k}\Omega$ Resistance <sup>(2, 3)</sup> Nonlinearity	G=1000 G=1 V <sub>O</sub> = ±13.6V, G=1 G=10 G=100 G=1000		±0.5 ±1 ±25 ±0.0001 ±0.0003 ±0.0005	±1 ±100 ±1000 ±0.001 ±0.002 ±0.002 (Note 4)		* * * * * * *	±2 * ±0.002 ±0.004 ±0.004 *	% ppm/°C ppm/°C % of FSR % of FSR % of FSR % of FSR
OUTPUT Voltage: Positive Negative Load Capacitance Stability Short-Circuit Current	$R_{L} = 10k\Omega$ $R_{L} = 10k\Omega$	(V+) - 1.4 (V-) + 1.4	(V+) - 0.9 (V-) + 0.8 1000 +6/-15		*	* * * *		V V pF mA
FREQUENCY RESPONSE Bandwidth, -3dB	G=1 G=10 G=100 G=1000		1.3 700 200 20			* * *		MHz kHz kHz kHz
Slew Rate Settling Time, 0.01%	$V_{O} = \pm 10V$ , G=10 G=1 G=10 G=100 G=1000		4 7 7 9 80			* * * *		V/μs μs μs μs μs
Overload Recovery  POWER SUPPLY  Voltage Range Current, Total	50% Overdrive  V <sub>IN</sub> = 0V	±2.25	±15 ±1.4	±18 ±1.5	*	* *	*	μs V mA
TEMPERATURE RANGE Specification Operating $\theta_{\rm JA}$	nv	-40 -40	80	85 125	*	*	*	°C °C °C/W

<sup>\*</sup> Specification same as INA2128P, U.

NOTE: (1) Input common-mode range varies with output voltage—see Electrical Characteristics.



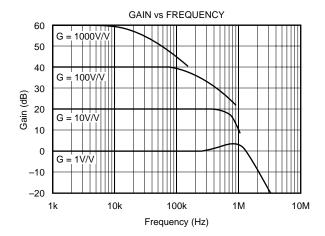
<sup>(2)</sup> Ensured by wafer test.

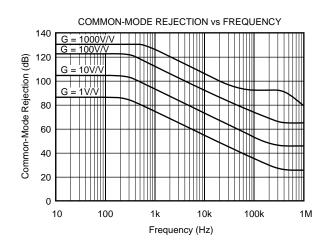
<sup>(3)</sup> Temperature coefficient of the  $50k\Omega$  term in the gain equation.

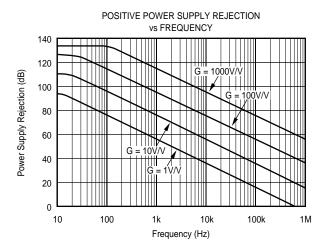
<sup>(4)</sup> Nonlinearity measurements in G = 1000 are dominated by noise. Typical nonlinearity is  $\pm 0.001\%$ .

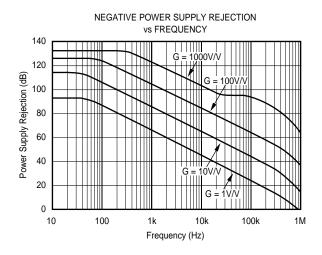
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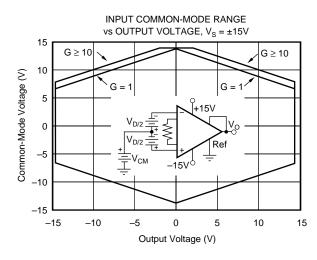
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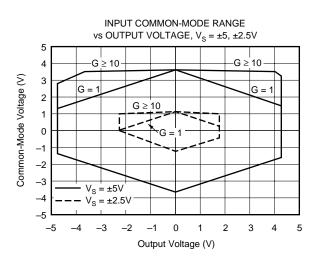






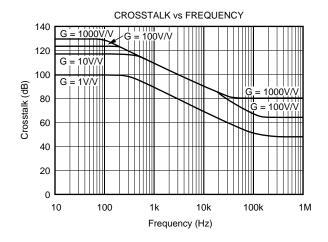


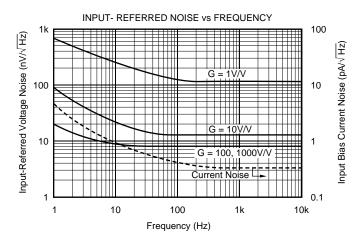


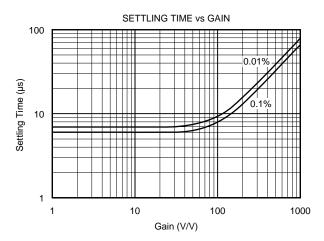


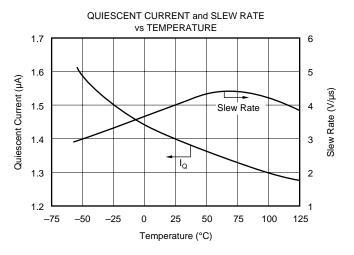
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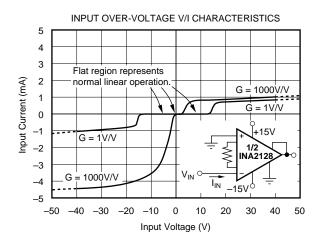
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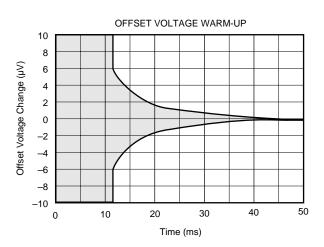






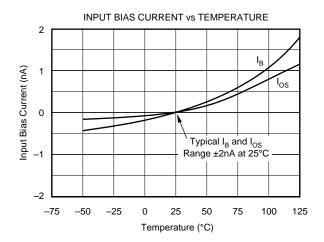


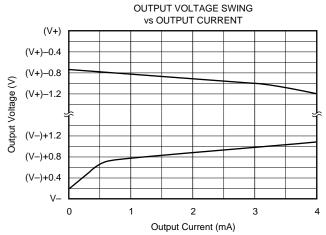


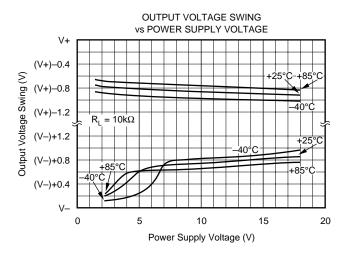


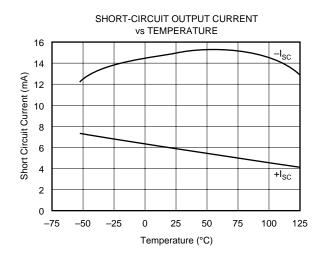
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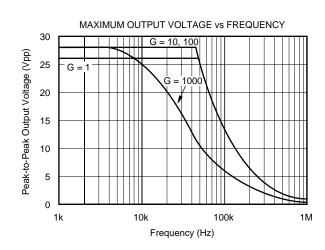
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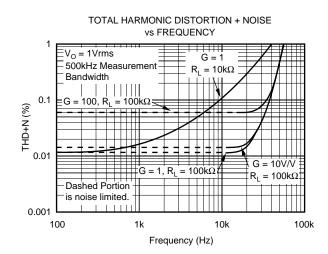






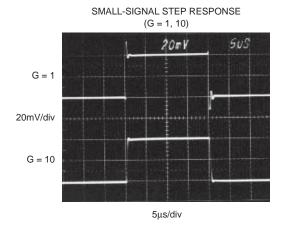


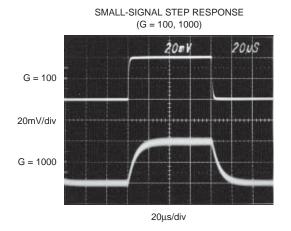


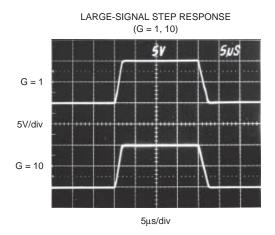


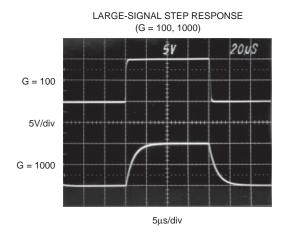
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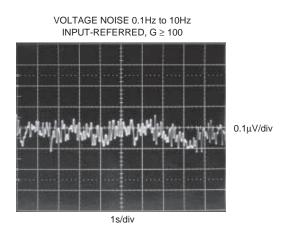
At  $T_A$  = +25°C,  $V_S$  = ±15V, unless otherwise noted.













## APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the INA2128. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the output reference (Ref) terminals (Ref<sub>A</sub> and Ref<sub>B</sub>) which are normally grounded. These must be low-impedance connections to assure good common-mode rejection. A resistance of  $8\Omega$  in series with a Ref pin will cause a typical device to degrade to approximately 80dB CMR (G = 1).

The INA2128 has separate output sense feedback connections, Sense<sub>A</sub> and Sense<sub>B</sub>. These must be connected to their respective output terminals for proper operation. The output sense connection can be used to sense the output voltage directly at the load for best accuracy.

#### **SETTING THE GAIN**

Gain of the INA2128 is set by connecting a single external resistor,  $R_G$ , connected as shown:

$$G = 1 + \frac{50k\Omega}{R_G} \tag{1}$$

Commonly-used gains and resistor values are shown in Figure 1.

The  $50k\Omega$  term in Equation 1 comes from the sum of the two

internal feedback resistors,  $A_1$  and  $A_2$ . These on-chip metal film resistors are laser-trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA2128.

The stability and temperature drift of the external gain setting resistor,  $R_G$ , also affects gain.  $R_G$ 's contribution to gain accuracy and drift can be directly inferred from the gain equation (1). Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance which will contribute additional gain error in gains of approximately 100 or greater.

#### **DYNAMIC PERFORMANCE**

The typical performance curve "Gain vs Frequency" shows that despite its low quiescent current, the INA2128 achieves wide bandwidth, even at high gain. This is due to its current-feedback topology. Settling time also remains excellent at high gain—see "Settling Time vs Gain."

#### NOISE PERFORMANCE

The INA2128 provides very low noise in most applications. Low frequency noise is approximately  $0.2\mu V_{PP}$  measured from 0.1 to 10Hz (G  $\geq$  100). This provides dramatically improved noise when compared to state-of-the-art chopper-stabilized amplifiers.

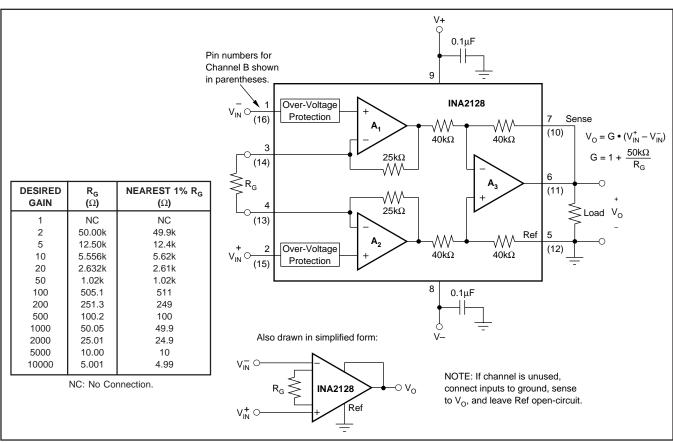


FIGURE 1. Basic Connections.



#### **OFFSET TRIMMING**

The INA2128 is laser-trimmed for low offset voltage and offset voltage drift. Most applications require no external offset adjustment. Figure 2 shows an optional circuit for trimming the output offset voltage. The voltage applied to Ref terminal is summed with the output. The op amp buffer provides low impedance at the Ref terminal to preserve good common-mode rejection.

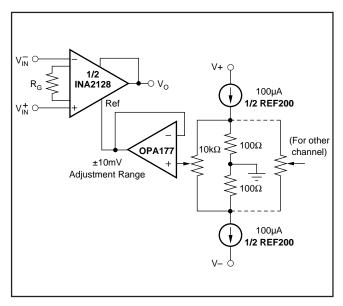


FIGURE 2. Optional Trimming of Output Offset Voltage.

#### INPUT BIAS CURRENT RETURN PATH

The input impedance of the INA2128 is extremely high—approximately  $10^{10}\Omega$ . However, a path must be provided for the input bias current of both inputs. This input bias current is approximately  $\pm 2nA$ . High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. Figure 3 shows various provisions for an input bias current path. Without a bias current path, the inputs will float to a potential which exceeds the commonmode range of the INA2128 and the input amplifiers will saturate.

If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in Figure 3). With higher source impedance, using two equal resistors provides a balanced input with possible advantages of lower input offset voltage due to bias current and better high-frequency common-mode rejection.

#### INPUT COMMON-MODE RANGE

The linear input voltage range of the input circuitry of the INA2128 is from approximately 1.4V below the positive supply voltage to 1.7V above the negative supply. As a differential input voltage causes the output voltage increase, however, the linear input range will be limited by the output

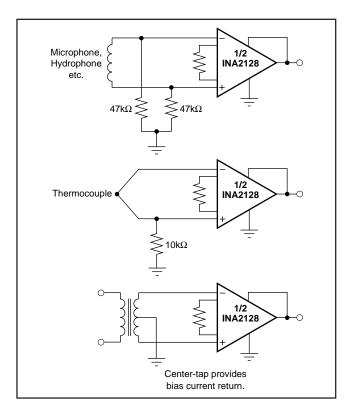


FIGURE 3. Providing an Input Common-Mode Current Path.

voltage swing of amplifiers  $A_1$  and  $A_2$ . So the linear common-mode input range is related to the output voltage of the complete amplifier. This behavior also depends on supply voltage—see performance curves "Input Common-Mode Range vs Output Voltage."

Input-overload can produce an output voltage that appears normal. For example, if an input overload condition drives both input amplifiers to their positive output swing limit, the difference voltage measured by the output amplifier will be near zero. The output of the INA2128 will be near 0V even though both inputs are overloaded.

#### LOW VOLTAGE OPERATION

The INA2128 can be operated on power supplies as low as  $\pm 2.25$ V. Performance remains excellent with power supplies ranging from  $\pm 2.25$ V to  $\pm 18$ V. Most parameters vary only slightly throughout this supply voltage range—see typical performance curves. Operation at very low supply voltage requires careful attention to assure that the input voltages remain within their linear range. Voltage swing requirements of internal nodes limit the input commonmode range with low power supply voltage. Typical performance curves, "Input Common-Mode Range vs Output Voltage," show the range of linear operation for  $\pm 15$ V,  $\pm 5$ V, and  $\pm 2.5$ V supplies.



#### INPUT PROTECTION

The inputs of the INA2128 are individually protected for voltages up to ±40V. For example, a condition of –40V on one input and +40V on the other input will not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. To provide equivalent protection, series input resistors would contribute excessive noise. If the input is overloaded, the protection circuitry limits the input current to a safe value of approximately 1.5mA to 5mA. The typical performance curve "Input Bias Current vs Common-Mode Input Voltage" shows this input current limit behavior. The inputs are protected even if the power supplies are disconnected or turned off.

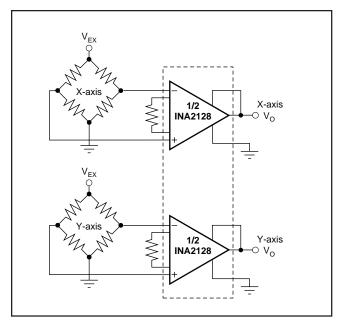


FIGURE 4. Two-Axis Bridge Amplifier.

#### CHANNEL CROSSTALK

The two channels of the INA2128 are completely independent, including all bias circuitry. At DC and low frequency there is virtually no signal coupling between channels. Crosstalk increases with frequency and is dependent on circuit gain, source impedance and signal characteristics.

As source impedance increases, careful circuit layout will help achieve lowest channel crosstalk. Most crossstalk is produced by capacitive coupling of signals from one channel to the input section of the other channel. To minimize coupling, separate the input traces as far as practical from any signals associated with the opposite channel. A grounded guard trace surrounding the inputs helps reduce stray coupling between channels. Run the differential inputs of each channel parallel to each other or directly adjacent on top and bottom side of a circuit board. Stray coupling then tends to produce a common-mode signal which is rejected by the IA's input.

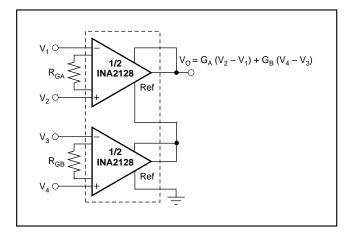


FIGURE 5. Sum of Differences Amplifier.

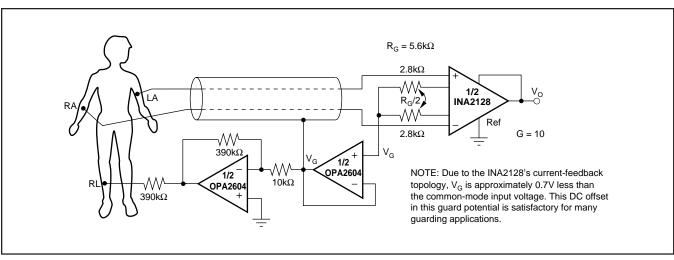


FIGURE 6. ECG Amplifier With Right-Leg Drive.







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#### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
INA2128U	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR	Contact TI Distributor or Sales Office
INA2128U/1K	ACTIVE	SOIC	DW	16	1000	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR	Purchase Samples
INA2128U/1KE4	ACTIVE	SOIC	DW	16	1000	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR	Purchase Samples
INA2128UA	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR	Request Free Samples
INA2128UA/1K	ACTIVE	SOIC	DW	16	1000	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR	Purchase Samples
INA2128UA/1KG4	ACTIVE	SOIC	DW	16	1000	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR	Purchase Samples
INA2128UAG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR	Contact TI Distributor or Sales Office
INA2128UG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR	Contact TI Distributor or Sales Office

<sup>&</sup>lt;sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.



## **PACKAGE OPTION ADDENDUM**

21-Aug-2010

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

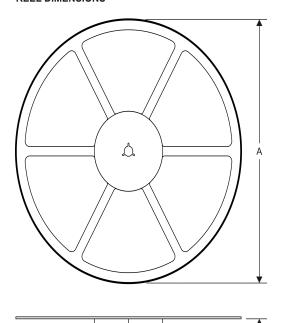
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

# PACKAGE MATERIALS INFORMATION

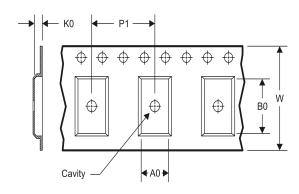
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### TAPE AND REEL INFORMATION

#### **REEL DIMENSIONS**



#### **TAPE DIMENSIONS**



A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### TAPE AND REEL INFORMATION

#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA2128U/1K	SOIC	DW	16	1000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
INA2128UA/1K	SOIC	DW	16	1000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

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#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA2128U/1K	SOIC	DW	16	1000	346.0	346.0	33.0
INA2128UA/1K	SOIC	DW	16	1000	346.0	346.0	33.0

DW (R-PDSO-G16)

# PLASTIC SMALL OUTLINE



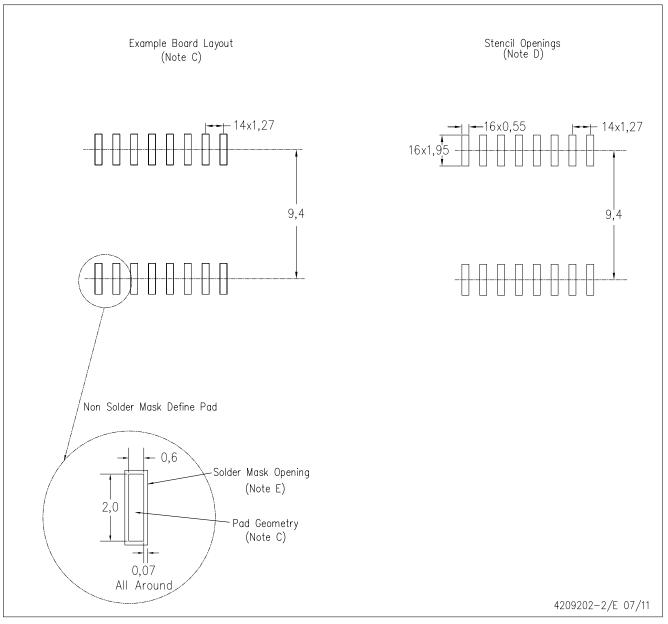
NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AA.



DW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC—7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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