



SLES193C-AUGUST 2006-REVISED FEBRUARY 2007

# 16-Bit, Low-Power Stereo Audio CODEC With Microphone Bias, Headphone, and Digital Speaker Amplifier

#### **FEATURES**

- Analog Front End:
  - Stereo Single-Ended Input With Multiplexer
  - Mono Differential Input
  - Stereo Programmable Gain Amplifier
  - Microphone Boost Amplifier (20 dB) and Bias
- Analog BackEnd:
  - Stereo/Mono Line Output With Volume
  - Stereo/Mono Headphone Amplifier With Volume and Capless Mode
  - Stereo/Mono Digital Speaker Amplifier (BTL) With Volume (PCM3793)
- Analog Performance:
  - Dynamic Range: 93 dB (DAC)
  - Dynamic Range: 90 dB (ADC)
  - 40-mW + 40-mW Headphone Output at  $R_L = 16 \Omega$
  - 700-mW + 700-mW Speaker Output at  $R_L = 8 \Omega$
- Power Supply Voltage
  - 1.71 V to 3.6 V for Digital I/O Section
  - 1.71 V to 3.6 V for Digital Core Section
  - 2.4 V to 3.6 V for Analog Section
  - 2.4 V to 3.6 V for Power Amplifier Section
- Low Power Dissipation:
  - 7 mW in Playback, 1.8 V/2.4 V, 48 kHz
  - 13 mW in Record, 1.8 V/2.4 V, 48 kHz
  - 30 μW in Power Down
- Sampling Frequency: 5 kHz to 50 kHz
- Automatic Level Control for Recording
- Operation From a Single Clock Input Without PLL
- System Clock:
  - Common-Audio Clock (256 f<sub>s</sub>/384 f<sub>s</sub>), 12/24, 13/26, 13.5/27, 19.2/38.4, 19.68/39.36 MHz
- Headphone Plug Insert Detection

- 2 (I<sup>2</sup>C) or 3 (SPI) Wire Serial Control
- Programmable Function by Register Control:
  - Digital Attenuation of DAC: 0 dB to -62 dB
  - Power Up/Down Control for Each Module
  - 6-dB to -70-dB Gain for Analog Outputs
  - 30-dB to -12-dB Gain for Analog Inputs
  - 0/20 dB Boost Selectable for Microphone Input
  - 0-dB to -21-dB Gain for Analog Mixing
  - Parameter Settings for ALC
  - Three-Band Tone Control and 3D Sound
  - High-Pass Filter and Two-Stage Notch Filter
  - Analog Mixing
- Pop-Noise Reduction Circuit
- Short and Thermal Protection Circuit
- Package: 5-mm × 5-mm QFN Pacakge
- Operation Temperature Range: –40°C to 85°C

#### **APPLICATIONS**

- Portable Audio Player, Cellular Phone
- Video Camcorder, Digital Still Camera
- PMP/DMB

#### DESCRIPTION

The PCM3793/94 is a low-power stereo CODEC designed for portable digital audio applications. The device integrates stereo digital speaker amplifier, headphone amplifier, line amplifier, line input, boost amplifier, microphone bias, programmable gain control, analog mixing, sound effects, and automatic level control (ALC). It is available in a small-footprint, 5-mm × 5-mm QFN package. The PCM3793/94 accepts right-justified, left-justified, l²S, and DSP formats, providing easy interfacing to audio DSP, decoder, and encoder chips. Sampling rates up to 50 kHz are supported. The user-programmable functions are accessible through a two- or three-wire serial control port.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE CODE	OPERATION TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER <sup>(1)</sup>	TRANSPORT MEDIA		
PCM3793RHB	32 QFN	RHB	−40°C to 85°C	PCM3793	PCM3793RHBT	Small tape and reel		
PCIVIS/93KHB	32 QI N	SKIID 32 QFN KIID	KIID	-40°C 10 65°C	-40 C to 65 C		PCM3793RHBR	Large tape and reel
PCM3794RHB	32 QFN	RHB	40°C to 95°C	PCM3794	PCM3794RHBT	Small tape and reel		
PCIVI3/94RHB	32 QFN	KHD	–40°C to 85°C	PCIVI3794	PCM3794RHBR	Large tape and reel		

<sup>(1)</sup> For the most current specification and package information, see the TI Web site at www.ti.com.

#### ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		PCM3793/94	UNIT	
Supply voltage	$V_{DD}$ , $V_{IO}$ , $V_{CC}$ , $V_{PA}$	-0.3 to 4	V	
Ground voltage differe	nces: DGND, AGND, PGND	±0.1	V	
Input voltage	nput voltage			
Input current (any pins	Input current (any pins except supplies and SPK out)			
Ambient temperature u	under bias	-40 to 110	°C	
Storage temperature		-55 to 150	°C	
Junction temperature		150	°C	
Lead temperature (soldering)		260	°C, 5 s	
Package temperature	260	°C		

<sup>(1)</sup> Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute—maximum—rated conditions for extended periods may affect device reliability.

#### RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V <sub>CC</sub> , V <sub>PA</sub>	Analog supply voltage		2.4	3.3	3.6	V
$V_{DD}$ , $V_{IO}$	Digital supply voltage	Digital supply voltage		3.3	3.6	V
	Digital input logic family			CMOS		
	Digital input clock frequency  Analog output load resistance	SCKI system clock	3.072		18.432	MHz
		LRCK sampling clock	8		48	kHz
		LOL and LOR	10			kΩ
		HPOL and HPOR	16			Ω
		SPOLP, SPOLN, SPORP and SPORN	8			Ω
	Analog output load capacitance				30	pF
	Digital output load capacitance				10	pF
T <sub>A</sub>	Operating free-air temperature		-40		85	°C



# **ELECTRICAL CHARACTERISTICS**

All specifications at  $T_A = 25$ °C,  $V_{DD} = V_{IO} = V_{CC} = V_{PA} = 3.3$  V,  $f_S = 48$  kHz, system clock = 256  $f_S$ , and 16-bit data (unless otherwise noted).

		TEST CONDITIONS	PCM3793RHB, PCM3794RHB				
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Audio D	Oata Characteristics				·		
DATA F	ORMAT						
	Resolution			16		Bits	
	Audio data interface format		I <sup>2</sup> S, left-, riç	ght-justified, DSI	Р		
	Audio data bit length			16		Bits	
	Audio data format		MSB first,	2s complement			
	Sampling frequency (f <sub>S</sub> )		5		50	kHz	
	0	V <sub>DD</sub> < 2 V			27	27	
	System clock	V <sub>DD</sub> > 2 V			40	MHz	
Digital I	nput/Output				l .		
	Logic family		CMOS	S compatible			
√ <sub>IH</sub>			0.7 V <sub>IO</sub>			VDC	
V <sub>IL</sub>	Input logic level		· · · · · · · · · · · · · · · · · · ·		0.3 V <sub>IO</sub>	VDC	
IH		V <sub>IN</sub> = 3.3 V			10		
IL	Input logic current	V <sub>IN</sub> = 0 V			-10	μΑ	
V <sub>OH</sub>		I <sub>OH</sub> = -2 mA	0.75 V <sub>IO</sub>			VDC	
V <sub>OL</sub>	Output logic level	I <sub>OL</sub> = 2 mA	-	0	.25 V <sub>IO</sub>	VDC	
	nput to Line Output Through DAG	C (LOL, LOR, and MONO)					
$R_1 = 10$	$k\Omega$ , ALC = OFF, volume = 0 dB, sp	eaker = powered down, analog mixing = d	isabled				
DYNAM	IC PERFORMANCE						
		0 dB		2.828		Vp-p	
	Full-scale output voltage			1		Vrms	
	Dynamic range	EIAJ, A-weighted		93		dB	
SNR	Signal-to-noise ratio	EIAJ, A-weighted	86	93		dB	
	Channel separation	-		91		dB	
THD+N	Total harmonic distortion + noise	0 dB		0.008%			
	Load resistance		10			kΩ	
Line Inp	out to Line Output Through Mixing	g Path (LOL, LOR, and MONO)					
-		eaker = powered down, analog mixing = e	nabled				
	IC PERFORMANCE						
	Full-scale input and output			2.828		Vp-p	
	voltage	0 dB		1		Vrms	
SNR	Signal-to-noise ratio	EIAJ, A-weighted	84	93		dB	

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# **ELECTRICAL CHARACTERISTICS (continued)**

All specifications at  $T_A = 25$ °C,  $V_{DD} = V_{IO} = V_{CC} = V_{PA} = 3.3$  V,  $f_S = 48$  kHz, system clock = 256  $f_S$ , and 16-bit data (unless otherwise noted).

	2.2.4	TT0T 0011D1T10110	PCM3793RHB, PCM3794RHB		НВ	
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital I	nput to Headphone Output Throu	igh DAC (HPOL and HPOR)				
R <sub>L</sub> = 16	$\Omega$ or 32 $\Omega$ , ALC = OFF, volume = 0	dB, speaker = powered down, analog mix	xing = disabled, no	t capless mode	)	
DYNAM	IC PERFORMANCE					
	Full scale output voltage	0 dB		2.828		Vp-p
	Full-scale output voltage	U UB		1		Vrms
SNR	Signal-to-noise ratio	EIAJ, A-weighted	84	93		dB
TUD.N	Total harmonic distortion I naise	30 mW, $R_L = 32 \Omega$ , volume = 0 dB		0.1%		
THD+N	Total harmonic distortion + noise	40 mW, $R_L$ = 16 Ω, volume = -1 dB		0.03%		
	Load resistance		16			Ω
		200 Hz, 140 mVp-p		-40		
PSRR	Power-supply rejection ratio	1 kHz, 140 mVp-p		-45		dB
		20 kHz, 140 mVp-p		-32		
Line Inp	out to Headphone Output Through	h Mixing Path (HPOL and HPOR)	•		'	
R <sub>L</sub> = 16	$\Omega$ or 32 $\Omega$ , ALC = OFF, volume = 0	dB, speaker = powered down, analog mix	xing = enabled, no	t capless mode		
DYNAM	IC PERFORMANCE					
		0.40		2.828		Vp-p
	Full-scale output voltage	0 dB		1		Vrms
SNR	Signal-to-noise ratio	EIAJ, A-weighted	84	93		dB
	Load resistance		16			Ω
Digital I	nput to Speaker Output Through	DAC (SPOLP, SPOLN, SPORP, and SP	ORN): PCM3793		I_	
$R_1 = 8 \Omega$	Ω, ALC = OFF, volume = 0 dB, head	dphone = powered down, analog mixing =	disabled			
			uisabieu			
DYNAM	IC PERFORMANCE		uisabieu			
DYNAM			disabled	2.52		Vp-p
DYNAM	Full-scale output voltage	0 dB	uisableu	2.52		Vp-p Vrms
DYNAM	Full-scale output voltage		uisableu 84			
		EIAJ, A-weighted		0.9		Vrms
SNR	Full-scale output voltage  Signal-to-noise ratio  Total harmonic distortion + noise			0.9		Vrms
SNR	Full-scale output voltage Signal-to-noise ratio	EIAJ, A-weighted 400 mW, $R_L = 8\Omega$ , volume = 0 dB	84	0.9		Vrms dB
SNR THD+N	Full-scale output voltage  Signal-to-noise ratio  Total harmonic distortion + noise  Load resistance	EIAJ, A-weighted 400 mW, $R_L = 8\Omega$ , volume = 0 dB 200 Hz, 140 mVp-p	84	0.9 93 0.3%		Vrms dB
SNR	Full-scale output voltage  Signal-to-noise ratio  Total harmonic distortion + noise	EIAJ, A-weighted 400 mW, $R_L = 8\Omega$ , volume = 0 dB 200 Hz, 140 mVp-p 1 kHz, 140 mVp-p	84	0.9 93 0.3% -50 -45		Vrms dB
SNR THD+N PSRR	Full-scale output voltage  Signal-to-noise ratio  Total harmonic distortion + noise  Load resistance  Power-supply rejection ratio	EIAJ, A-weighted $400 \text{ mW, R}_{L} = 8\Omega, \text{ volume} = 0 \text{ dB}$ $200 \text{ Hz, } 140 \text{ mVp-p}$ $1 \text{ kHz, } 140 \text{ mVp-p}$ $20 \text{ kHz, } 140 \text{ mVp-p}$	84	0.9 93 0.3% -50 -45 -25		Vrms dB
SNR THD+N PSRR	Full-scale output voltage  Signal-to-noise ratio  Total harmonic distortion + noise Load resistance  Power-supply rejection ratio  put to Speaker Output Through M	EIAJ, A-weighted  400 mW, R <sub>L</sub> = 8Ω, volume = 0 dB  200 Hz, 140 mVp-p  1 kHz, 140 mVp-p  20 kHz, 140 mVp-p  ixing Path (SPOLP, SPOLN, SPORP, and	84 8 ad SPORN): PCM3	0.9 93 0.3% -50 -45 -25		Vrms dB
SNR THD+N  PSRR  Line Inp $R_L = 8\Omega$	Full-scale output voltage  Signal-to-noise ratio  Total harmonic distortion + noise  Load resistance  Power-supply rejection ratio  out to Speaker Output Through M  ALC = OFF, volume = 0 dB, head	EIAJ, A-weighted $400 \text{ mW, R}_{L} = 8\Omega, \text{ volume} = 0 \text{ dB}$ $200 \text{ Hz, } 140 \text{ mVp-p}$ $1 \text{ kHz, } 140 \text{ mVp-p}$ $20 \text{ kHz, } 140 \text{ mVp-p}$	84 8 ad SPORN): PCM3	0.9 93 0.3% -50 -45 -25		Vrms dB
SNR THD+N  PSRR  Line Inp $R_L = 8\Omega$	Full-scale output voltage  Signal-to-noise ratio  Total harmonic distortion + noise Load resistance  Power-supply rejection ratio  put to Speaker Output Through M	EIAJ, A-weighted  400 mW, R <sub>L</sub> = 8Ω, volume = 0 dB  200 Hz, 140 mVp-p  1 kHz, 140 mVp-p  20 kHz, 140 mVp-p  ixing Path (SPOLP, SPOLN, SPORP, and	84 8 ad SPORN): PCM3	0.9 93 0.3% -50 -45 -25		Vrms dB Ω dB
SNR THD+N  PSRR  Line Inp $R_L = 8\Omega$	Full-scale output voltage  Signal-to-noise ratio  Total harmonic distortion + noise  Load resistance  Power-supply rejection ratio  out to Speaker Output Through M  ALC = OFF, volume = 0 dB, head	EIAJ, A-weighted  400 mW, R <sub>L</sub> = 8Ω, volume = 0 dB  200 Hz, 140 mVp-p  1 kHz, 140 mVp-p  20 kHz, 140 mVp-p  ixing Path (SPOLP, SPOLN, SPORP, and	84 8 ad SPORN): PCM3	0.9 93 0.3% -50 -45 -25		Vrms dB



# **ELECTRICAL CHARACTERISTICS (continued)**

All specifications at  $T_A = 25^{\circ}C$ ,  $V_{DD} = V_{IO} = V_{CC} = V_{PA} = 3.3 \text{ V}$ ,  $f_S = 48 \text{ kHz}$ , system clock = 256  $f_S$ , and 16-bit data (unless otherwise noted).

	DADAMETER	PCI	PCM3793RHB, PCM3794RHB		UNIT	
	PARAMETER	TEST CONDITIONS	MIN TYP	MAX	UNIT	
Line Inp	out to Digital Output Through AD	(AIN1L/R, AIN2L/R, AIN3L, and AIN3L/R)				
ALC = C	DFF, microphone boost = 0 dB, PGA	a = 0 dB, speaker and headphone = powered down,	analog mixing = disab	oled		
DYNAM	IIC PERFORMANCE					
	Full cools input valtage	0.40	2.828		Vp-p	
	Full-scale input voltage	0 dB	1		Vrms	
	Dynamic range	EIAJ, A-weighted	90		dB	
SNR	Signal-to-noise ratio	EIAJ, A-weighted	83 90		dB	
	Channel separation		87		dB	
THD+N	Total harmonic distortion + noise	–1 dB	0.009%			
ANALO	G INPUT	-		"		
	Center voltage		0.5 V <sub>CC</sub>		V	
	Input impedance		10 20		kΩ	
Microph	none Bias					
ALC = C	OFF, microphone boost = 0 dB, PGA	a = 0 dB, speaker and headphone = powered down,	analog mixing = disab	oled		
	Bias voltage		0.75 V <sub>CC</sub>		V	
	Bias source current		2		mA	
	Output noise		14		μV	
Filter Cl	haracteristics				·	
INTERP	OLATION FILTER FOR DAC					
	Pass band			0.454 f <sub>S</sub>		
	Stop band	0.54	6 f <sub>S</sub>	-		
	Pass-band ripple		<del></del>	±0.04	dB	
	Stop-band attenuation		-50		dB	
	Group delay		19/f <sub>s</sub>		S	
	De-emphasis error		±0.1		dB	
ANALO	G FILTER FOR DAC	<u> </u>				
	Frequency response	f = 20 kHz	±0.2		dB	
DECIMA	ATION FILTER FOR ADC	<u> </u>				
	Pass band			0.408 f <sub>S</sub>		
	Stop band	0.59	1 f <sub>S</sub>	-		
	Pass-band ripple		<del>-</del>	±0.02	dB	
	Stop-band attenuation	f < 3.268 f <sub>S</sub>	-60		dB	
	Group delay		17/f <sub>S</sub>		s	
HIGH-P	ASS FILTER FOR ADC		. 3		-	
	<del>-</del>	$-3 \text{ dB, } f_c = 4 \text{ Hz}$	3.74			
		$-0.5 \text{ dB, } f_c = 4 \text{ Hz}$	10.66			
		$-0.1 \text{ dB}, f_c = 4 \text{ Hz}$	24.2			
	Frequency response	-3 dB, f <sub>c</sub> = 240 Hz	235.68		Hz	
		$-0.5 \text{ dB}, t_c = 240 \text{ Hz}$	609.95			
		5.5 52, ic - 2 10 112	505.50			

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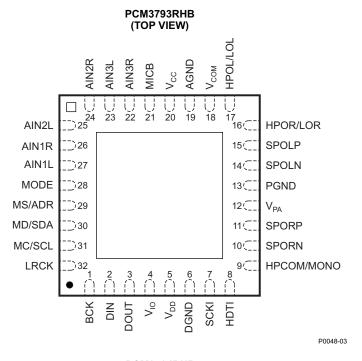
# **ELECTRICAL CHARACTERISTICS (continued)**

All specifications at  $T_A = 25$ °C,  $V_{DD} = V_{IO} = V_{CC} = V_{PA} = 3.3$  V,  $f_S = 48$  kHz, system clock = 256  $f_S$ , and 16-bit data (unless otherwise noted).

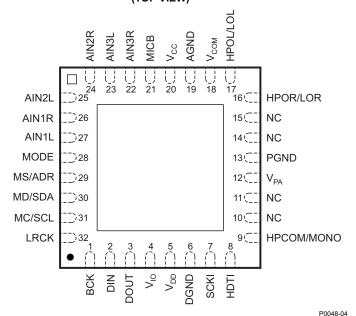
	DADAMETED	TEST COMPLIANCE	PCM3793RI	HB, PCM3794	IRHB	LINUT
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Powe	r Supply and Supply Current		·			
V <sub>IO</sub>		V <sub>IO</sub>	1.71	3.3	3.6	
$V_{DD}$	Voltage range	$V_{DD}$	1.71	3.3	3.6	VDC
$V_{CC}$		V <sub>CC</sub>	2.4	3.3	3.6	VDC
$V_{PA}$		$V_{PA}$	2.4	3.3	3.6	
	Complex accompant	BPZ input, all active, no load		24.3	35	mA
	Supply current	All inputs are held static		9	50	μΑ
	Daniel Parkardan	BPZ input		80.2	115.5	mW
	Power dissipation	All inputs are held static		30	165	μW
Temp	erature Condition					
	Operation temperature		-40		85	°C
$\theta_{JA}$	Thermal resistance			30		°C/W



#### **PIN ASSIGNMENTS**



#### PCM3794RHB (TOP VIEW)



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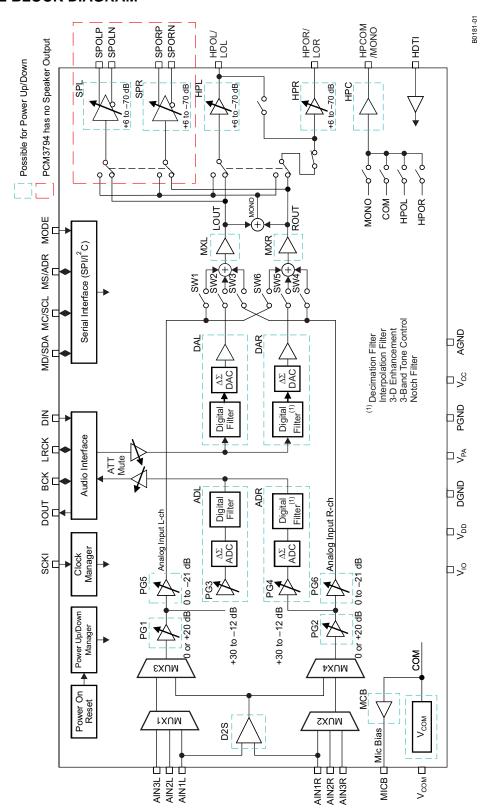


#### **Table 1. TERMINAL FUNCTIONS**

	TERMINAL			DEGODITECT
NAME	PCM3793RHB	PCM3794RHB	I/O	DESCRIPTION
AGND	19	19	_	Ground for analog
AIN1L	27	27	ı	Analog input 1 for L-channel
AIN1R	26	26	ı	Analog input 1 for R-channel
AIN2L	25	25	I	Analog input 2 for L-channel
AIN2R	24	24	ı	Analog input 2 for R-channel
AIN3L	23	23	ı	Analog input 3 for L-channel
AIN3R	22	22	ı	Analog input 3 for R-channel
BCK	1	1	I/O	Serial bit clock
DGND	6	6	-	Digital ground
DIN	2	2	I	Serial audio data input
DOUT	3	3	0	Serial audio data output
HDTI	8	8	I	Headphone plug insertion detection
HPCOM/MONO	9	9	0	Headphone common/mono line output
HPOL/LOL	17	17	0	Headphone/lineout for R-channel
HPOR/LOR	16	16	0	Headphone/lineout for L-channel
LRCK	32	32	I/O	Left and right channel clock
MC/SCL	31	31	ı	Mode control clock for three-wire/two-wire interface
MD/SDA	30	30	I/O	Mode control data for three-wire/two-wire interface
MICB	21	21	0	Microphone bias source output
MODE	28	28	I	Two- or three-wire interface selection (LOW: SPI, HIGH: I <sup>2</sup> C)
MS/ADR	29	29	ı	Mode control select for three-wire/two-wire interface
PGND	13	13	_	Ground for speaker power amplifier
SCKI	7	7	ı	System clock
SPOLN	14	_	0	Speaker output L-channel for negative (PCM3793)
SPOLP	15	_	0	Speaker output L-channel for positive (PCM3793)
SPORN	10	_	0	Speaker output R-channel for negative (PCM3793)
SPORP	11	_	0	Speaker output R-channel for positive (PCM3793)
V <sub>CC</sub>	20	20	-	Analog power supply
V <sub>COM</sub>	18	18	_	Analog common voltage
$V_{DD}$	5	5	-	Power supply for digital core
V <sub>IO</sub>	4	4	_	Power supply for digital I/O
$V_{PA}$	12	12	-	Power supply for power amplifier



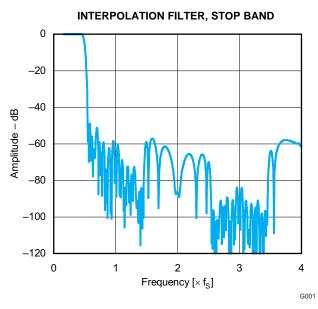
#### **FUNCTIONAL BLOCK DIAGRAM**





#### **TYPICAL PERFORMANCE CURVES**

All specifications at  $T_A = 25^{\circ}C$ ,  $V_{DD} = V_{IO} = V_{CC} = V_{PA} = 3.3 \text{ V}$ ,  $f_S = 8 \text{ to } 48 \text{ kHz}$ , system clock = 256  $f_S$ , and 16-bit data, unless otherwise noted.





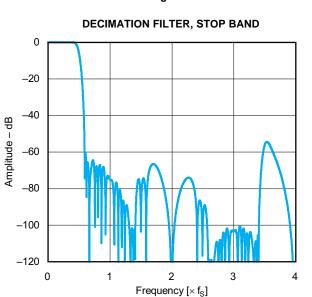


Figure 3.

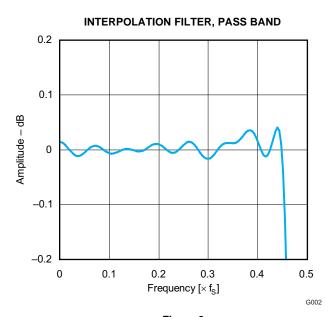


Figure 2.

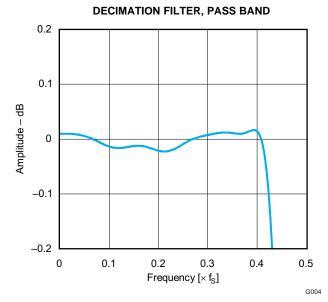
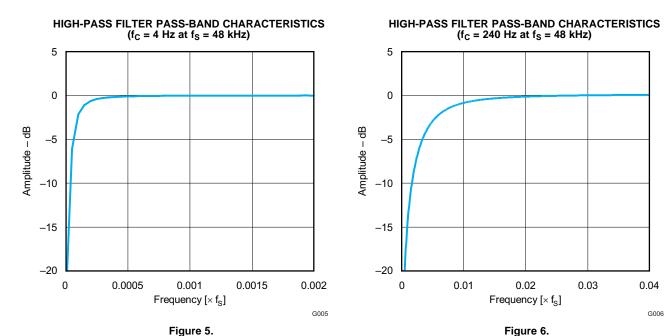


Figure 4.

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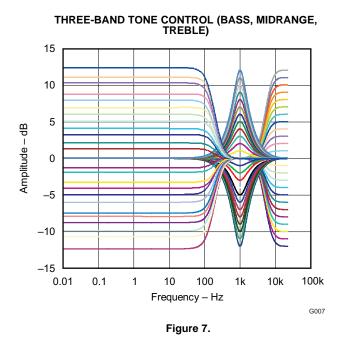


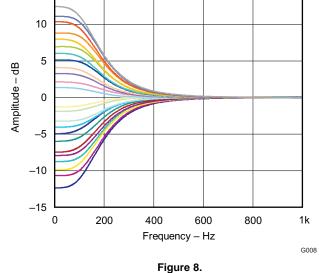
All specifications at  $T_A = 25^{\circ}C$ ,  $V_{DD} = V_{IO} = V_{CC} = V_{PA} = 3.3 \text{ V}$ ,  $f_S = 8 \text{ to } 48 \text{ kHz}$ , system clock = 256  $f_S$ , and 16-bit data, unless otherwise noted.



All specifications at  $T_A = 25^{\circ}C$ ,  $V_{DD} = V_{IO} = V_{CC} = V_{PA} = 3.3 \text{ V}$ ,  $f_S = 44.1 \text{ kHz}$ , system clock = 256  $f_S$ , and 16-bit data, unless otherwise noted.

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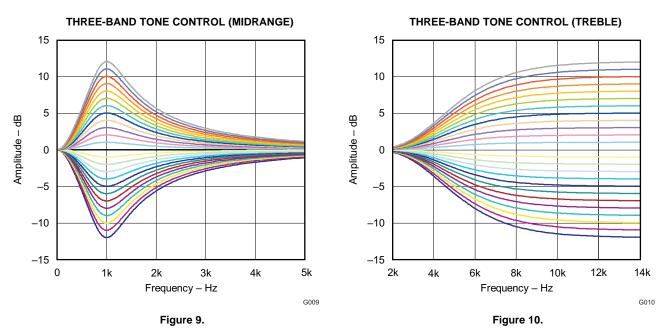




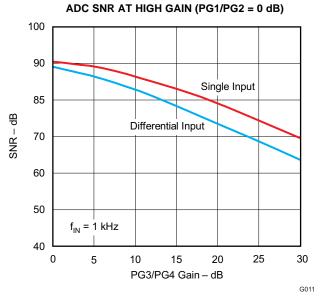
THREE-BAND TONE CONTROL (BASS)



All specifications at  $T_A = 25$ °C,  $V_{DD} = V_{IO} = V_{CC} = V_{PA} = 3.3$  V,  $f_S = 44.1$  kHz, system clock = 256  $f_S$ , and 16-bit data, unless otherwise noted.



All specifications at  $T_A = 25^{\circ}C$ ,  $V_{DD} = V_{IO} = V_{CC} = V_{PA} = 3.3 \text{ V}$ ,  $f_S = 48 \text{ kHz}$ , system clock = 256  $f_S$ , and 16-bit data, unless otherwise noted.





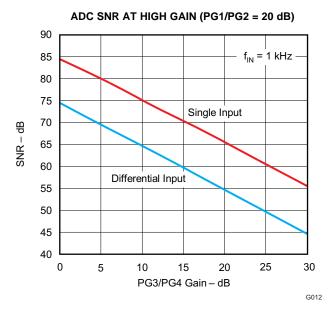


Figure 12.



All specifications at  $T_A = 25^{\circ}C$ ,  $V_{DD} = V_{IO} = V_{CC} = V_{PA} = 3.3 \text{ V}$ ,  $f_S = 48 \text{ kHz}$ , system clock = 256  $f_S$ , and 16-bit data, unless otherwise noted.

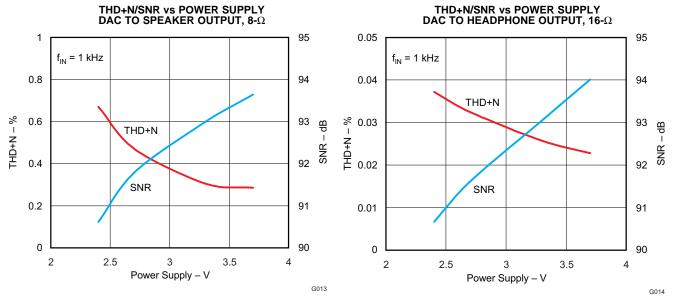


Figure 13. Figure 14.

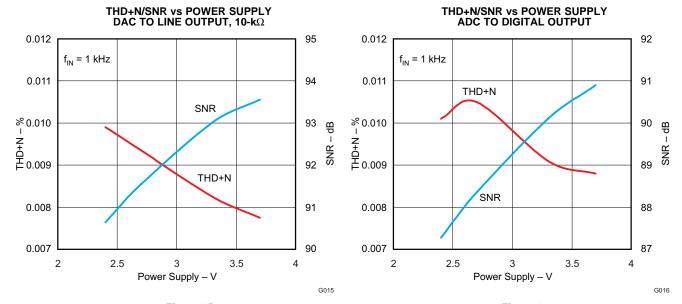


Figure 15. Figure 16.



All specifications at  $T_A = 25$  °C,  $V_{DD} = V_{IO} = V_{CC} = V_{PA} = 3.3$  V,  $f_S = 48$  kHz, system clock = 256  $f_S$ , and 16-bit data, unless otherwise noted.

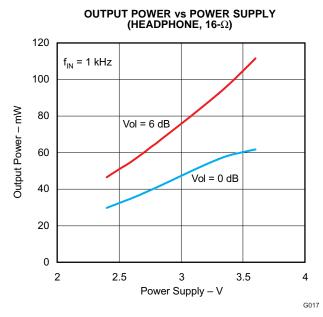


Figure 17.

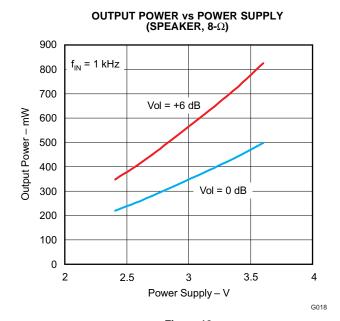


Figure 18.

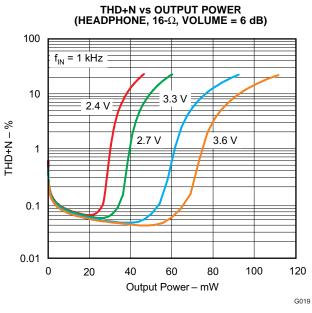


Figure 19.

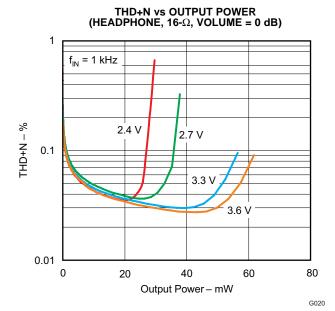
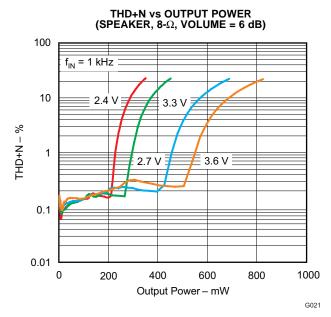


Figure 20.



All specifications at  $T_A = 25^{\circ}C$ ,  $V_{DD} = V_{IO} = V_{CC} = V_{PA} = 3.3 \text{ V}$ ,  $f_S = 48 \text{ kHz}$ , system clock = 256  $f_S$ , and 16-bit data, unless otherwise noted.



#### Figure 21.

# OUTPUT SPECTRUM (DAC TO HEADPHONE OUTPUT, 16- $\Omega$ )

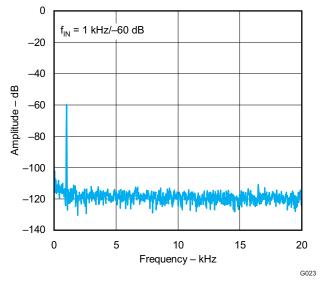


Figure 23.

# THD+N vs OUTPUT POWER (SPEAKER, 8- $\Omega$ , VOLUME = 0 dB)

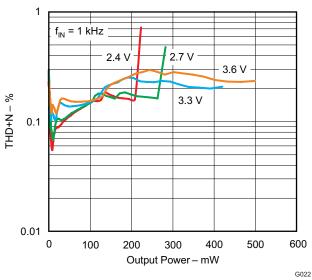


Figure 22.

# OUTPUT SPECTRUM (DAC TO SPEAKER OUTPUT, $8-\Omega$ )

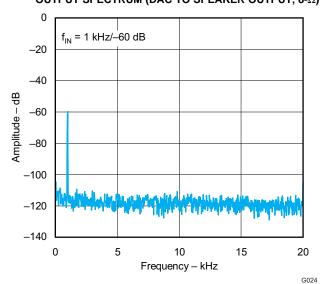


Figure 24.

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#### PCM3793/94 DESCRIPTION

#### **Analog Input**

The AIN1L, AIN1R, AIN2L, AIN2R, AIN3L, and AIN3R pins can be used as microphone or line inputs with selectable 0- or 20-dB boost and 1-Vrms input. All analog inputs have high input impedance (20  $k\Omega$ ), which is not changed by gain settings. One pair of inputs is selected by register 87 (AIL[1:0], AIR[1:0]). AIN1L and AIN1R can be used as monaural differential inputs.

#### **Gain Settings for Analog Input**

Analog signals can be adjusted from 30 dB to -12 dB in 1-dB steps following the 0- or 20-dB boost amplifier. The gain level can be set for each channel by registers 79 and 80 (ALV[5:0], ARV[5:0]).

#### A/D Converter

The ADC includes a multilevel delta-sigma modulator, aliasing filter, decimation filter, high-pass filter, and notch filter and can accept a 1-Vrms full-scale voltage input. The decimation filter has a digital soft mute controlled by register 81 (RMUL, RMUR). The high-pass filter can be disabled by register 81 (HPF[1:0]) and the notch filter can be disabled by registers 96 to 104 if it is not necessary to cancel a dc offset or compensate for wind noise.

#### **D/A Converter**

The DAC includes a multilevel delta-sigma modulator and interpolation filter. These can be used to obtain high PSRR, low jitter sensitivity, and low out-of-band noise quickly and easily. The interpolation filter includes digital attenuator, digital soft mute, three-band tone control (bass, midrange and treble), and 3-D sound controlled by registers 92 to 95. The de-emphasis filter (32, 44.1 and 48 kHz) is controlled by registers 68 to 70 (ATL[5:0], ATR[5:0], PMUL, PMUR, DEM[1:0]). Oversampling rate control can reduce out-of-band noise when operating at low sampling rate by using register 70 (OVER).

#### **Common Voltage**

The  $V_{COM}$  pin is normally biased to 0.5  $V_{CC}$ , and it provides the common voltage to internal circuitry. It is recommended that a 10- $\mu$ F capacitor be connected between this pin and ground to provide clean voltage and avoid pop noise. The PCM3793/94 may have a little pop noise on each analog output if a capacitor smaller than 10  $\mu$ F is used.

#### **Line Output**

The HPOL/LOL and HPOR/LOR and HPCOM/MONO pins can be used as a monaural single-ended, monaural differential, or stereo single-line output with 1- $V_{rms}$  output by register 74 (HPS[1:0]). The line outputs can drive a 10- $k\Omega$  load. These outputs include an analog volume amplifier, except for the HPCOM/MONO pin that can be set from 6 dB to -70 dB and mute with 0.5-, 1-, 2- or 4-dB steps for each output, as controlled by registers 64 and 65 (HLV[5:0], HRV[5:0], HMUL, HMUR). A dc blocking capacitor is not required when connecting to an external speaker amplifier with monaural differential input. The center voltage is 0.5  $V_{CC}$  with zero data input.

#### **Headphone Output**

The HPOL/LOL, HPOR/LOR, and HPCOM/MONO pins are stereo, monaural, or monaural differential headphone outputs with more than 30 or 40 mWrms output power into a 32- or 16- $\Omega$  load, either through a dc blocking capacitor or without a capacitor, as selected by register 74 (HPS[2:0]). These outputs include analog volume amplifiers, except for the HPCOM/MONO pin, which can be set from 6 dB to –70 dB with 0.5-, 1-, 2- or 4-dB steps for each output using registers 64 and 65 (HLV[5:0], HRV[5:0], HMUL, HMUR). The center voltage is 0.5  $V_{CC}$  with zero data input.

#### **Headphone Plug Insertion Detection**

The HDTI pin detects the insertion status of headphone plug and writes the status to register 77 (HPDS), which can be read by the I<sup>2</sup>C interface. The polarity of the status indication can be inverted by register 75 (HPDP). The headphone and speaker amplifiers are disabled or enabled automatically by headphone plug insertion/extractrion if register 75, HPDE = 1. They are controlled by register settings if register 75, HPDE = 0. HPCOM/MONO is not affected by the status when register 74, CMS[0] = 1.





#### Speaker Output (Class-D, PCM3793)

The SPOLP, SPOLN and SPORP, SPORN pins are stereo or mono speaker differential outputs (BTL) with a maximum of 700 mWrms ( $V_{PA} = 3.6$  V, volume = 6 dB) into an 8- $\Omega$  load. The digital speaker amplifier offers maximum battery life and minimum heat, eliminates the LC low-pass filter, and includes analog volume amplification for each output from 6 dB to -70 dB with 0.5-, 1-, 2- or 4-dB steps, which can be set by register 66, 67 (SLV[5:0], SLR[5:0]). Spectrum spreading technology and selectable switching frequency to reduce EMI noise is controlled by register 71 (DFQ[2:0], SPS[1:0] and SPSE). The speaker amplifiers have a thermal shutdown circuit which detects when the device temperature reaches approximately 150°C; then the speaker amplifier is powered down.

#### **Analog Mixing and Bypass**

Mixing amplifiers (MXL, MXR) mix gain-controlled analog inputs from the AIN pins which have bypassed ADC and DAC and direct the mixed signal to the headphone or speaker outputs. Analog mixing is controlled by register 87 (AD2S, AIR[1:0], AIL[1:0]), register 88 (MXR[2:0], MXL[2:0]), and register 89 (GMR[2:0], GML[2:0]). The analog mixing functions are suitable for FM radio, headset, and another analog sources without an ADC.

#### Microphone Bias

The MICB pin is the microphone bias source for an external microphone and can provide 2 mA (typical) bias current.

#### Automatic Level Control (ALC) for Recording

The sound for microphone recording should be expanded to a suitable level without saturation. The digitally controlled automatic level control (ALC) provides automatic expansion for small input signals and compression for large input signals while recording. The expansion level, compression level, attack time, and recovery time can be selected by register 83. The register 83 description explains the details of these settings.

#### 3-D Sound

A 3-D sound effect is provided by mixing L-channel and R-channel data with band pass filter that can be controlled two parameters, mixing ratio and band pass filter characteristic by register 95 (3DP[3:0], 3FLO). The 3-D sound effect can be applied to the DAC digital input or ADC digital output, as selected by register 95 (SDAS).

#### **Three-Band Tone Control**

Tone control has bass, midrange, and treble controls that can be adjusted from 12 dB to -12 dB in 1-dB steps by registers 92 to 94 (LGA[4:0], MGA[4:0] and HGA[4:0]). Register 92 (LPAE) attenuates the digital input signal automatically to prevent clipping of the output signal at settings above 0 dB for bass control. LPAE has no effect on midrange and treble controls.

#### **High-Pass Filter and Notch Filter**

The high-pass filter eliminates the dc offset of the ADC analog signal and can be set for a cutoff frequency of 4 Hz or 240 Hz at of 48-kHz sampling frequency by register 81 (HPF[1:0]). A register 95 (SDAS) selection applies the filter to either the DAC digital input or the ADC digital output.

Notch filters are provided to remove noise of a particular frequency, such as CCD noise, motor noise, or other mechanical noise in a particular application. The PCM3793/94 has two notch filters for which the center frequency and frequency bandwidth can be programmed by registers 96 to 104. A register 95 (SDAS) selection applies the filter to either the DAC digital input or the ADC digital output.

#### **Digital Monaural Mixing**

Register 96 (MXEN) enables or disables the internal mixing of stereo digital data to monaural digital data.

#### **Zero-Cross Detection**

Zero-cross detection minimizes audible zipper noise while changing analog volume and digital attenuation. This function can be applied to digital input or digital output by register 86 (ZCRS).

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#### **Short Protection**

The short-circuit protection on each headphone output prevents damage to the device while an output is shorted to  $V_{PA}$ , an output is shorted to PGND, or any two outputs are shorted together. When the short circuit is detected on the outputs, the PCM3793/94 powers down the shorted amplifier at once. The short-protection status can be monitored by reading register 77 (STHC, STHL, SCHR) through the  $I^2C$  interface. Short-circuit protection operates in any enabled headphone amplifier.

#### **Thermal Protection**

The thermal protection on the speaker amplifier prevents damage to the device when the internal die temperature exceeds approximately 150°C. Once the die temperature exceeds the thermal set point, all analog outputs are powered down. This status can be reset by setting register 76 (RLSR, RLSL) and can be watched by reading register 77 (STSR, STSL) on the two-wire (I<sup>2</sup>C) interface. Thermal protection operates in any enabled speaker amplifier.

#### **Pop-Noise Reduction Circuit**

The pop-noise reduction circuit prevents audible noise when turning the power supply on/off and powering the device up/down in portable applications. It is recommended to establish the register settings in the sequence that is shown in Table 3 and Table 4. No particular external parts are required, and power-supply sequencing is not necessary.

#### Power Up/Down for Each Module

Using register 72 (PMXL, PMXR), register 73 (PBIS, PDAR, PDAL, PHPC, PHPR, PHPL, PSPR, PSPL), register 82 (PAIR, PAIL, PADS, PMCB, PADL), and register 90 (PCOM), unused modules can be powered down to minimize power consumption (7 mW during playback only and 13 mW when recording only).

#### **Digital Interface**

All digital I/O pins can interface at various power supply voltages. The  $V_{IO}$  pin can be connected to a 1.71-V to 3.6-V power supply.

#### **Power Supply**

The  $V_{CC}$  pin and the  $V_{PA}$  pin can be connected to 2.4 V to 3.6 V. The same voltage must be applied to both pins. The  $V_{DD}$  pin and the  $V_{IO}$  pin can be connected to 1.71 V to 3.6 V. A different voltage can be applied to each of these pins (for example,  $V_{DD} = 1.8$  V,  $V_{IO} = 3.3$  V).

#### **DESCRIPTION OF OPERATION**

#### **System Clock Input**

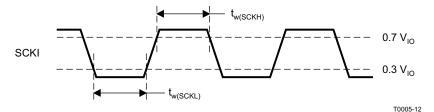
The PCM3793/94 can accept clocks of various frequencies without a PLL. They are used for clocking the digital filters and automatic level control and delta-sigma modulators and are classified as common-audio and application-specific clocks. Table 2 shows frequencies of the common-audio clock and application-specific clock. Figure 25 shows the timing requirements for system clock inputs. The sampling rate and frequency of the system clocks are determined by the settings of register 86 (MSR[2:0]) and register 85 (NPR[5:0]). Note that the sampling rate of the application-specific clock has a little sampling error.

Table 2. System Clock Frequencies

CLOCK	FREQUENCIES
Common-audio clock	11.2896, 12.288, 16.9344, 18.432 MHz
Application-specific clock	12, 13, 13.5, 24, 26, 27, 19.2, 19.68, 38.4, 39.36 MHz







PARAMETERS	SYMBOL	MIN	UNITS
System-clock pulse duration, high	t <sub>w(SCKH)</sub>	7	ns
System-clock pulse duration, low	t <sub>w(SCKL)</sub>	7	ns

Figure 25. System Clock Timing

#### **Power-On Reset and System Reset**

The power-on-reset circuit outputs a reset signal, typically at  $V_{DD} = 1.2 \text{ V}$ , and this circuit does not depend on the voltage of other power supplies (V<sub>CC</sub>, V<sub>PA</sub> and V<sub>IO</sub>). Internal circuits are cleared to default status, then signals are removed from all analog and digital outputs. The PCM3793/94 does not require any power supply sequencing. Register data must be written after turning all power supplies on.

System reset is enabled by setting register 85 (SRST), and all register are cleared automatically. All circuits are reset to their default status at once. Note that the PCM3793/94 has audible pop noise on the analog outputs when enabling SRST.

#### Power On/Off Sequence

To reduce audible pop noise, a sequence of register settings is required after turning all power supplies on when powering up, or before turning the power supplies off when powering down. If some modules are not required for a particular application or operation, they should be placed in the power-down state after performing the power-on sequence. The recommended power-on and power-off sequences are shown in Table 3 and Table 4, respectively.

**Table 3. Recommended Power-On Sequence** 

STEP	REGISTER SETTINGS	NOTE
1	_	Turn on all power supplies <sup>(1)</sup>
2	4027h	Headphone amplifier L-ch volume (–6 dB) <sup>(2)</sup>
3	4127h	Headphone amplifier R-ch volume (–6 dB) <sup>(2)</sup>
4	4227h	Speaker amplifier L-ch volume (–6 dB) <sup>(2)</sup>
5	4327h	Speaker amplifier R-ch volume (–6 dB) <sup>(2)</sup>
6	4427h	Digital attenuator L-ch (–24 dB) <sup>(2)</sup>
7	4527h	Digital attenuator R-ch (–24 dB) <sup>(2)</sup>
8	4620h	DAC audio interface format (left-justified) <sup>(3)</sup>
9	4BC0h	Headphone detection enable and inverting polarity. Short and thermal detection enable
10	5102h	ADC audio interface format (left-justified) <sup>(3)</sup>
11	5A10h	V <sub>COM</sub> ramp up/down time control. PG1, PG2 gain control (0 dB)
12	49E0h	DAC (DAL, DAR) and analog bias power up
13	5601h	Zero-cross detection enable
14	4803h	Analog mixer (MXL, MXR) power up
15	5811h	Analog mixer input (SW2, SW5) select
16	49FCh	Headphone amplifier (HPL, HPR, HPC) power up

<sup>(1)</sup> Power supply sequencing is not required. It is recommended to set register data with system clock input after turning all power supplies

Any level is acceptable for volume or attenuation. Level should be resumed by register data recorded when system power off.

Audio interface format should be set to match the DSP or decoder being used. (3)

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#### Table 3. Recommended Power-On Sequence (continued)

STEP	REGISTER SETTINGS	NOTE			
17	4C03h	Speaker amplifier shut down release			
18	4A01h	V <sub>COM</sub> power up			
19	523Fh	Analog front end (ADL, ADR, D2S, MCB, PG1, 2, 5, 6) power up			
20	5711h	Analog input (MUX3, MUX4) select. Analog input (MUX1, MUX2) select			
21	4F0Ch	Analog input L-ch (PG3) volume (0 dB) <sup>(2)</sup>			
22	22 500Ch Analog input R-ch (PG4) volume (0 dB) <sup>(2)</sup>				
23	_	Any settings for other devices or wait time <sup>(4)(5)</sup>			
24	49FFh	Speaker amplifier (SPL, SPR) power up (5)			

<sup>(4)</sup> The PCM3793 requires time for  $V_{COM}$  to reach the common level from GND level. The delay depends on the capacitor value for  $V_{COM}$  and the setting of register 90 CMT[1:0]. Wait time [s] =  $4 \times C_{VCOM} \times R_{CMT}$ 

#### **Table 4. Recommended Power-Off Sequence**

STEP	REGISTER SETTINGS	NOTE
1	447Fh	DAC L-ch digital soft-mute enable <sup>(1)</sup>
2	457Fh	DAC R-ch digital soft-mute enable <sup>(1)</sup>
3	5132h	ADC L-ch/R-ch digital soft-mute enable, ADC audio interface format (left-justified) (2)
4	5811h	Analog mixer input (SW2, SW5) Select
5	49FFh	Headphone amplifier (HPL, HPR, HPC) power up (4), speaker amplifier (SPL, SPR) power up (3)(4)
6	5200h	Analog front end (ADL, ADR, D2S, MCB, PG1, 2, 5, 6) power down
7	5A10h	V <sub>COM</sub> ramp up/down time control, PG1, PG2 gain control (0 dB)
8	4A00h	V <sub>COM</sub> power down
9	_	Wait time (100 ms)
10	5A00h	V <sub>COM</sub> ramp up/down time control
11	_	Wait time (100 ms)
12	5A20h	V <sub>COM</sub> ramp up/down time control
13	_	Wait time (4000 ms)
14	5A30h	V <sub>COM</sub> ramp up/down time control
15	49E0h	Headphone amplifier (HPL, HPR, HPC) power down, speaker amplifier (SPL, SPR) power down
16	4800h	Analog mixer (MXL, MXR) power down
17	4900h	DAC (DAL, DAR) and analog bias power down
18	_	Turn off all power supplies (5)

- (1) Any level is acceptable for volume or attenuation.
- (2) Audio interface format should be set according to DSP or decoder.
- (3) PCM3794 has no speaker amplifier.
- (4) These modules must be powered up during the power-down sequence.
- (5) Power supply sequencing is not required. It is recommended to turn off all power supply after register settings with system clock input.

#### **Power-Supply Current**

The current consumption of the PCM3793/94 depends on power up/down status of each circuit module. In order to reduce the power consumption, disabling each module is recommended when it is not used in an application or operation. Table 5 shows the current consumption in some states.

<sup>(5)</sup> The PCM3794 does not require this setting because it has no speaker output.

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# **Table 5. Power Consumption Table**

OPERATION MODE	F	OWER SU	PPLY CURI	RENT [mA]		PD [mW]	PD [mW]
	V <sub>DD</sub> (1.8 V)	V <sub>DD</sub> (3.3 V)	V <sub>CC</sub> (3.3 V)	V <sub>PA</sub> (3.3 V)	V <sub>IO</sub> (3.3 V)	TOTAL (V <sub>DD</sub> = 1.8 V)	TOTAL (V <sub>DD</sub> = 3.3 V)
All Power Down	0	0	0.007	0.002	0	0.03	0.03
All Active	2.5	5.1	7.5	11.6	0.1	67.7	80.2
PLAYBACK WITH DIGITAL INPUT			•				
Line output and headphone output	1.18	2.51	1.79	0.54	0.09	10.1	16.3
Headphone output with sound effect	1.81	3.84	1.79	0.54	0.09	11.2	20.7
Capless headphone output	1.18	2.51	1.8	0.75	0.09	10.8	17.0
Headphone output with line input (AIN2L/AIN2R)	1.18	2.52	2.09	0.54	0.09	11.1	17.3
Headphone output with mono microphone input (AIN1L, 20 dB)	1.18	2.52	2.5	0.54	0.09	12.5	18.6
Headphone output with mono differential microphone input (AIN1L/AIN1R, 20 dB)	1.18	2.52	2.8	0.54	0.09	13.4	19.6
Stereo speaker output	1.21	2.58	2.18	10.94	0.09	45.8	52.1
Mono speaker output	1.20	2.57	2.01	5.61	0.09	27.6	33.9
Speaker output with line input (AIN2L/AIN2R)	1.21	2.57	2.48	10.95	0.09	46.8	53.1
Speaker output with mono microphone input (AIN1L, 20 dB)	1.21	2.58	2.89	10.96	0.09	48.2	54.5
Speaker output with mono differential microphone input (AIN1L/AIN1R, 20 dB)	1.2	2.58	3.2	10.98	0.09	49.3	55.6
PLAYBACK WITHOUT DIGITAL INPUT							
Line input (AIN2L/AIN2R) to headphone output	0	0	0.76	0.53	0	4.3	4.3
Mono line input (AIN2L) to headphone output	0	0	0.61	0.53	0	3.8	3.8
Mono microphone Input (AIN1L, 20 dB) to headphone output	0	0	1.18	0.53	0	5.6	5.6
Mono differential microphone input (AIN1L/AIN1R, 20 dB) to headphone output	0	0	1.48	0.53	0	6.6	6.6
Mono microphone input (AIN1L, 20 dB) to speaker output	0	0	1.57	10.92	0	41.2	41.2
RECORDING							
Line input (AIN3L/AIN3R)	1.86	3.89	4.58	0.13	0.1	19.2	28.7
Microphone input (AIN1L/AIN1R, 20 dB)	1.86	3.91	5.14	0.13	0.1	21.1	30.6
Microphone input (AIN1L/AIN1R, 20 dB) with ALC	2.78	5.77	5.14	0.13	0.1	22.7	36.8
Mono microphone input (AIN1L, 20 dB)	1.4	2.93	3.6	0.13	0.1	15.2	22.3
Mono microphone input (AIN1L, 20 dB) with ALC	2.2	4.74	3.6	0.13	0.1	16.6	28.3
Mono differential microphone input (AIN1L/AIN1R, 20 dB)	1.4	2.94	3.96	0.13	0.1	16.3	23.5
Mono differential microphone input (AIN1L/AIN1R, 20 dB) with ALC	2.2	4.74	3.96	0.13	0.1	17.8	29.5
Conditions: 48 kHz/256 f <sub>S</sub> , 16 bits, slave mode, zero data input, n	o load						

#### **Audio Serial Interface**

The audio serial interface for the PCM3793/94 comprises LRCK, BCK, DIN, and DOUT. Sampling rate ( $f_S$ ), left and right channel are present on LRCK. DIN receives the serial data for the DAC interpolation filter, and DOUT transmits the serial data from the ADC decimation filter. BCK clocks the transfer of serial audio data on DIN and DOUT in its high-to-low transition. BCK and LRCK should be synchronized with audio system clock. Ideally, it is recommended that they be derived from it.

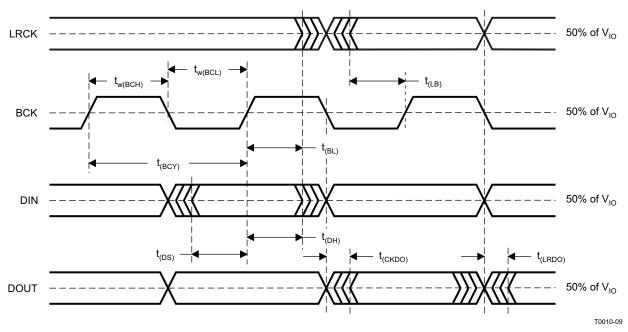
The PCM3793/94 requires LRCK to be synchronized with the system clock. The PCM3793/94 does not require a specific phase relationship between LRCK and the system clock.

The PCM3793/94 has both master mode and slave mode interface formats, which can be selected by register 84, MSTR. In master mode, the PCM3793/94 generates LRCK and BCK from the system clock.

#### **Audio Data Formats and Timing**

The PCM3793/94 supports I<sup>2</sup>S, right-justified, left-justified and DSP formats. The data formats are shown in Figure 28 and are selected using register 70 (RFM[1:0], PFM[1:0]). All formats require binary 2s-complement, MSB-first audio data. The default format is I<sup>2</sup>S. Figure 26 shows a detailed timing diagram.



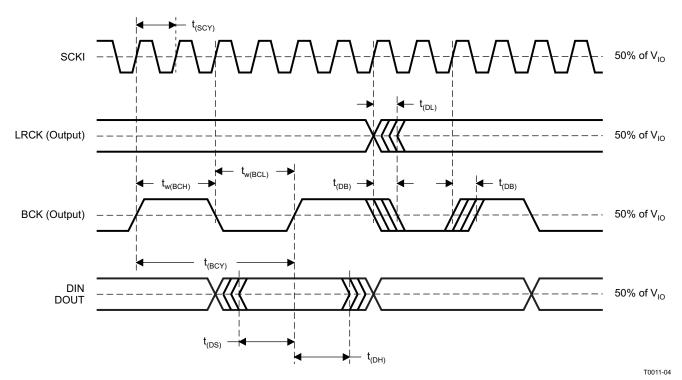


	PARAMETERS	MIN	MAX	UNITS
	BCK pulse cycle time (I <sup>2</sup> S, left- and right-justified formats)	1/(64 f <sub>S</sub> ) <sup>(1)</sup>		
t <sub>(BCY)</sub>	BCK pulse cycle time (DSP format)	1/(256 f <sub>S</sub> ) <sup>(1)</sup>		
t <sub>w(BCH)</sub>	BCK high-level time	35		ns
t <sub>w(BCL)</sub>	BCK low-level time	35		ns
t <sub>(BL)</sub>	BCK rising edge to LRCK edge	10		ns
t <sub>(LB)</sub>	LRCK edge to BCK rising edge	10		ns
t <sub>(DS)</sub>	DIN set up time	10		ns
t <sub>(DH)</sub>	DIN hold time	10		ns
t <sub>(CKDO)</sub>	DOUT delay time from BCK falling edge		15	ns
t <sub>(LRDO)</sub>	DOUT delay time from LRCK falling edge		15	ns
t <sub>r</sub>	Rising time of all signals		10	ns
t <sub>f</sub>	Falling time of all signals		10	ns

(1)  $f_S$  is the sampling frequency.

Figure 26. Audio Interface Timing (Slave Mode)

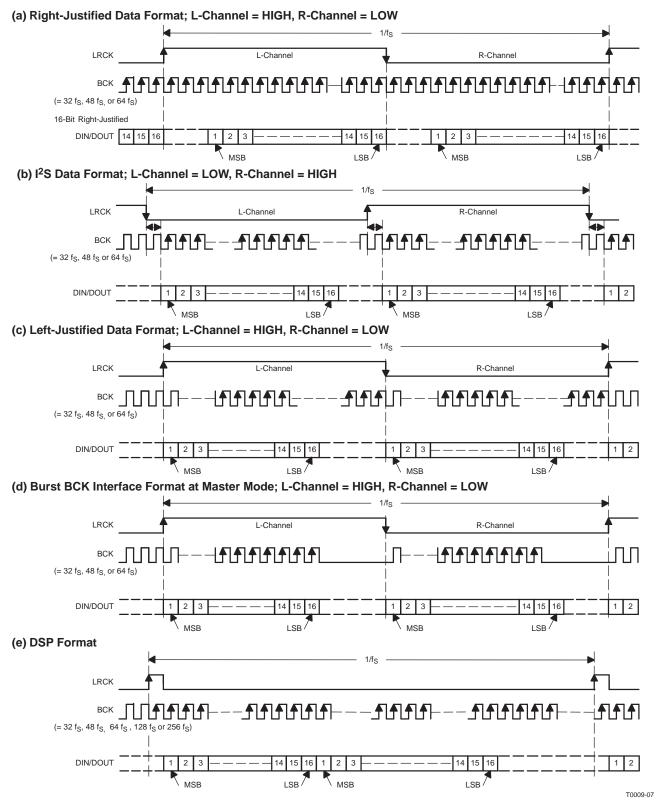




	PARAMETERS	MIN	MAX	UNIT
t <sub>(SCY)</sub>	SCKI pulse cycle time	1/(256 f <sub>S</sub> ) <sup>(1)</sup>		
t <sub>(DL)</sub>	LRCK edge from SCKI rising edge	0	40	ns
t <sub>(DB)</sub>	BCK edge from SCKI rising edge	0	40	ns
t <sub>(BCY)</sub>	BCK pulse cycle time	1/(64 f <sub>S</sub> ) <sup>(1)</sup>		
t <sub>w(BCH)</sub>	BCK high level time	146		ns
t <sub>w(BCL)</sub>	BCK low level time	146		ns
t <sub>(DS)</sub>	DATA setup time	10		ns
t <sub>(DH)</sub>	DATA hold time	10		ns

(1)  $f_S$  is up to 48 kHz.  $f_S$  is the sampling frequency. Figure 27. Audio Interface Timing (Master Mode)





NOTE: All audio interface formats support BCK = 64  $f_S$  in master mode (register 69, MSTR = 1). When setting the multisampling rate, the  $f_S$  of BCK is set to half the rate of the DSM operation frequency.

Figure 28. Audio Data Input and Output Formats



# THREE-WIRE INTERFACE (SPI, MODE (PIN 28) = LOW)

All write operations for the serial control port use 16-bit data words. Figure 29 shows the control data word format. The most significant bit must be 0. There are seven bits, labeled IDX[6:0], that set the register address for the write operation. The least significant eight bits, D[7:0], contain the data to be written to the register specified by IDX[6:0].

Figure 30 shows the functional timing diagram for writing to the serial control port. To write the data into the mode register, the data is clocked into an internal shift register on the rising edge of the MC clock. The serial data should change on the falling edge of MC clock and should be LOW during write mode. The rising edge of MS should be aligned with the falling edge of the last MC clock pulse in the 16-bit frame. MC can run continuously between transactions while MS is in the LOW state.

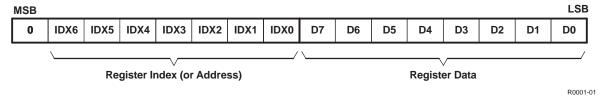
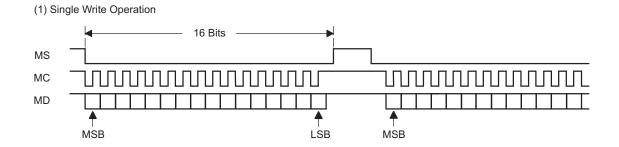


Figure 29. Control Data Word Format for MD



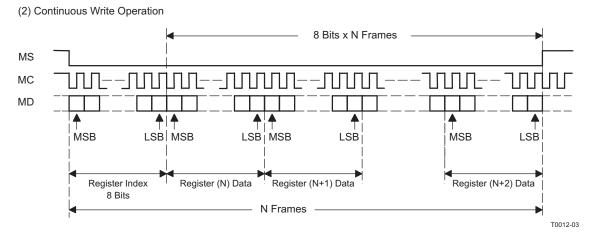
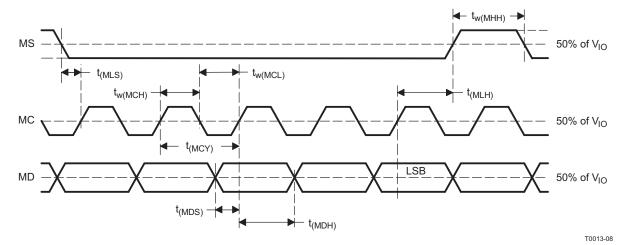


Figure 30. Register Write Operation



#### Three-Wire Interface (SPI) Timing Requirements

Figure 31 shows a detailed timing diagram for the serial control interface. These timing parameters are critical for proper control port operation.



	PARAMETERS	MIN	TYP	MAX	UNIT
t <sub>(MCY)</sub>	MC pulse cycle time	500 <sup>(1)</sup>			ns
t <sub>w(MCL)</sub>	MC low level time	50			ns
t <sub>w(MCH)</sub>	MC high level time	50			ns
t <sub>w(MHH)</sub>	MS high level time	(1)			ns
t <sub>(MLS)</sub>	MS falling edge to MC rising edge	20			ns
t <sub>(MLH)</sub>	MS hold time	20			ns
t <sub>(MDH)</sub>	MD hold time	15			ns
t <sub>(MDS)</sub>	MD setup time	20			ns

<sup>(1)</sup>  $3/(128 f_S)$  s (min), where  $f_S$  is sampling rate.

Figure 31. SPI Interface Timing

#### TWO-WIRE INTERFACE [I<sup>2</sup>C, MODE (PIN 28) = HIGH]

The PCM3793/94 supports the I<sup>2</sup>C serial bus and the data transmission protocol for the I<sup>2</sup>C standard as a slave device. This protocol is explained in I<sup>2</sup>C specification 2.0.

In I<sup>2</sup>C mode, the control terminals are changed as follows.

TERMINAL NAME	PROPERTY	DESCRIPTION
MS/ADR	Input	I <sup>2</sup> C address
MD/SDA	Input/output	I <sup>2</sup> C data
MC/SCL	Input	I <sup>2</sup> C clock

#### **SLAVE ADDRESS**

MSB							LSB
1	0	0	0	1	1	ADR	R/W

The PCM3793/94 has its own 7-bit slave address. The first six bits (MSBs) of the slave address are factory preset to 100011. The last bit of the address byte is the device select bit, which can be user-defined by the ADR terminal. A maximum of two PCM3793/94s can be connected on the same bus at one time. Each PCM3793/94 responds when it receives its own slave address.



#### **Packet Protocol**

The master device must control packet protocol, which consists of start condition, slave address with read/write bit, data if write or acknowledgement if read, and stop condition. The PCM3793/94 supports only slave receiver and slave transmitter.

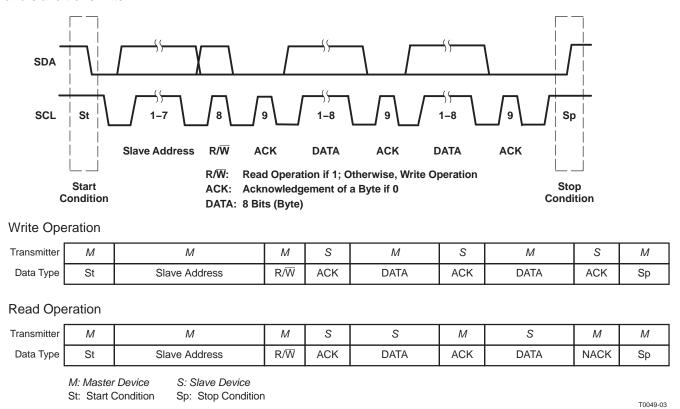


Figure 32. Basic I<sup>2</sup>C Framework

#### **WRITE OPERATION**

A master can write any PCM3793/94 registers using single access. The master sends a PCM3793/94 slave address with a write bit, a register address, and the data. When undefined registers are accessed, the PCM3793/94 does not send an acknowledgement. Figure 33 shows a diagram of the write operation.

Transmitter	М	М	М	S	М	S	М	S	М
Data Type	St	Slave Address	W	ACK	Reg Address	ACK	Write Data	ACK	Sp

M: Master Device S: Slave Device

St: Start Condition W: Write ACK: Acknowledge Sp: Stop Condition

R0002-01

Figure 33. Framework for Write Operation

#### **READ OPERATION**

A master can read the PCM3793/94 register. The value of the register address is stored in an indirect index register in advance. The master sends a PCM3793/94 slave address with a read bit after storing the register address. Then the PCM3793/94 transfers the data which the index register points to. Figure 34 shows a diagram of the write operation.

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Transmitter	М	М	М	S	М	S	М	М	М	S	S	М	М
Data Type	St	Slave Address	W	ACK	Reg Address	ACK	Sr	Slave Address	R	ACK	Read Data	NACK	Sp

M: Master Device S: Slave Device St: Start Condition

Sr: Repeated Start Condition ACK: Acknowledge Sp: Stop Condition NACK: Not Acknowledge

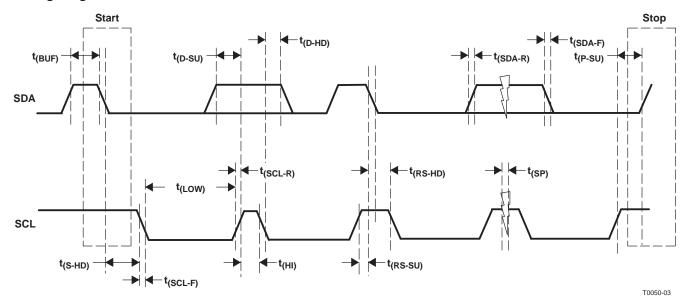
W: Write R: Read

R0002-02

NOTE: The slave address after the repeated start condition must be the same as the previous slave address.

Figure 34. Read Operation

#### **Timing Diagram**



**PARAMETERS** CONDITIONS MIN MAX UNIT SCL clock frequency Standard 100 kHz  $f_{SCL}$ Bus free time between a STOP and START condition Standard 4.7 μs t<sub>(BUF)</sub> Low period of the SCL clock Standard 4.7 μs  $t_{(LOW)}$ High period of the SCL clock Standard 4 t<sub>(HI)</sub> μs Setup time for START condition Standard 4.7  $\mu$ s t<sub>(RS-SU)</sub> Hold time for START condition Standard 4 μs t<sub>(S-HD)</sub> Data setup time Standard 250 ns t<sub>(D-SU)</sub> Data hold time Standard 900 ns t<sub>(D-HD)</sub> Rise time of SCL signal Standard 20 + 0.1 C<sub>B</sub> 1000 ns t(SCL-R) Rise time of SCL signal after a repeated START condition and Standard  $20 + 0.1 C_{B}$ 1000 ns t(SCL-R1) after an acknowledge bit Fall time of SCL signal Standard 20 + 0.1 C<sub>B</sub> 1000 ns t<sub>(SCL-F)</sub> Rise time of SDA signal Standard  $20 + 0.1 C_{B}$ 1000 ns t(SDA-R) 1000 Fall time of SDA signal Standard 20 + 0.1 C<sub>B</sub> ns t(SDA-F) Setup time for STOP condition Standard t<sub>(P-SU)</sub> μs Capacitive load for SDA and SCL line  $C_B$ 400 pF Pulse duration of suppressed spike 25 ns t<sub>(SP)</sub>

Figure 35. I<sup>2</sup>C Interface Timing

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#### **USER-PROGRAMMABLE MODE CONTROLS**

#### **Register Map**

The mode control register map is shown in Table 6. Each register includes an index (or address) indicated by the IDX[6:0] bits.

**Table 6. Mode Control Register Map** 

REGISTER	IDX[6:0] (B14-B8)	DESCRIPTION	В7	В6	В5	B4	В3	B2	B1	В0
Register 64	40h	Volume for HPA (L-ch)	RSV	HMUL	HLV5	HLV4	HLV3	HLV2	HLV1	HLV0
Register 65	41h	Volume for HPA (R-ch)	RSV	HMUR	HRV5	HRV4	HRV3	HRV2	HRV1	HRV0
Register 66	42h	Volume for SPA (L-ch)	RSV	SMUL	SLV5	SLV4	SLV3	SLV2	SLV1	SLV0
Register 67	43h	Volume for SPA (R-ch)	RSV	SMUR	SRV5	SRV4	SRV3	SRV2	SRV1	SRV0
Register 68	44h	DAC digital attenuation and soft mute (L-ch)	RSV	PMUL	ATL5	ATL4	ATL3	ATL2	ATL1	ATL0
Register 69	45h	DAC digital attenuation and soft mute (R-ch)	RSV	PMUR	ATR5	ATR4	ATR3	ATR2	ATR1	ATR0
Register 70	46h	DAC over sampling, de-emphasis, audio interface	DEM1	DEM0	PFM1	PFM0	RSV	RSV	RSV	OVER
Register 71	47h	SPA (class-D) switching frequency	RSV	RSV	RSV	SPSE	SPS1	SPS0	DFQ1	DFQ0
Register 72	48h	Analog mixer power up/down	RSV	RSV	RSV	RSV	RSV	RSV	PMXR	PMXL
Register 73	49h	DAC, SPA and HPA power up/down	PBIS	PDAR	PDAL	PHPC	PHPR	PHPL	PSPR	PSPL
Register 74	4Ah	Analog output configuration select	RSV	CMS2	CMS1	CMS0	HPS1	HPS0	SPKS	PCOM
Register 75	4Bh	HPA insertion detection, short/thermal protection	HPDP	HPDE	RSV	SDHC	SDHR	SDHL	SDSR	SDSL
Register 76	4Ch	SPA shutdown release	RSV	RSV	RSV	RSV	RSV	RSV	RLSR	RLSL
Register 77	4Dh	Shut down status read back	HPDS	RSV	RSV	STHC	STHR	STHL	STSR	STSL
Register 79	4Fh	Volume for ADC input (L-ch)	RSV	RSV	ALV5	ALV4	ALV3	ALV2	ALV1	ALV0
Register 80	50h	Volume for ADC input (R-ch)	RSV	RSV	ARV5	ARV4	ARV3	ARV2	ARV1	ARV0
Register 81	51h	ADC high-pass filter, soft mute, audio interface	HPF1	HPF0	RMUL	RMUR	RSV	DSMC	RFM1	RFM0
Register 82	52h	ADC, MCB, PG1, 2, 5, 6, D2S power up/down	RSV	RSV	PAIR	PAIL	PADS	PMCB	PADR	PADL
Register 83	53h	Automatic level control for recording	RALC	RSV	RRTC	RATC	RCP1	RCP0	RLV1	RLV0
Register 84	54h	Master mode	RSV	RSV	RSV	RSV	RSV	MSTR	RSV	BIT0
Register 85	55h	System reset, sampling rate control	SRST	RSV	NPR5	NPR4	NPR3	NPR2	NPR1	NPR0
Register 86	56h	BCK configuration, sampling rate control, zero-cross	MBST	MSR2	MSR1	MSR0	ATOD	RSV	RSV	ZCRS
Register 87	57h	Analog input select (MUX1, 2, 3, 4)	AD2S	RSV	AIR1	AIR0	RSV	RSV	AIL1	AIL0
Register 88	58h	Analog mixing switch (SW1, 2, 3, 4, 5, 6)	RSV	MXR2	MXR1	MXR0	RSV	MXL2	MXL1	MXL0
Register 89	59h	Analog to analog path (PG5, 6) gain	RSV	GMR2	GMR1	GMR0	RSV	GML2	GML1	GML0
Register 90	5Ah	V <sub>COM</sub> power up/down, ramp up/down time, boost	RSV	RSV	CMT1	CMT0	RSV	RSV	G20R	G20L
Register 92	5Ch	Bass boost gain level	LPAE	RSV	RSV	LGA4	LGA3	LGA2	LGA1	LGA0
Register 93	5Dh	Middle boost gain level	RSV	RSV	RSV	MGA4	MGA3	MGA2	MGA1	MGA0
Register 94	5Eh	Treble boost gain level	RSV	RSV	RSV	HGA4	HGA3	HGA2	HGA1	HGA0
Register 95	5Fh	Sound effect source select, 3D sound	SDAS	3DEN	RSV	3FL0	3DP3	3DP2	3DP1	3DP0
Register 96	60h	2-stage notch filter, digital monaural mixing	NEN2	NEN1	NUP2	NUP1	RSV	RSV	RSV	MXEN
Register 97	61h	1st stage notch filter lower coefficient (a1)	F107	F106	F105	F104	F103	F102	F101	F100
Register 98	62h	1st stage notch filter upper coefficient (a1)	F115	F114	F113	F112	F111	F110	F109	F108
Register 99	63h	1st stage notch filter lower coefficient (a2)	F207	F206	F205	F204	F203	F202	F201	F200
Register 100	64h	1st stage notch filter upper coefficient (a2)	F215	F214	F213	F212	F211	F210	F209	F208
Register 101	65h	2nd stage notch filter lower coefficient (a1)	S107	S106	S105	S104	S103	S102	S101	S100
Register 102	66h	2nd stage notch filter upper coefficient (a1)	S115	S114	S113	S112	S111	S110	S109	S108
Register 103	67h	2nd stage notch filter lower coefficient (a2)	S207	S206	S205	S204	S203	S202	S201	S200
Register 104	68h	2nd stage notch filter upper coefficient (a2)	S215	S214	S213	S212	S211	S210	S209	S208
HPA: Headphone single-ended am		A: Speaker amplifier DAC: D/A converter ADC: A/D converter	MCB: N	licrophone	bias PGx	: Analog in	put buffer	D2S: Diffe	erential to	

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#### **Register Definitions**

B15 B14 B13 B12 B11 B10 В9 В8 B7 В6 В5 B4 ВЗ B2 В1 В0 0 IDX6 IDX5 IDX4 IDX3 IDX2 IDX1 IDX0 RSV HMUL HLV5 HLV4 HLV3 HLV2 HLV1 HLV0 Register 64 0 IDX6 IDX5 IDX4 IDX3 RSV HMUR HRV5 HRV4 HRV3 HRV2 HRV1 HRV0 Register 65 IDX2 IDX1 IDX0

IDX[6:0]: 100 0000b (40h): Register 64 IDX[6:0]: 100 0001b (41h): Register 65

HMUL: Analog Mute Control for HPL (Line or Headphone L-Channel)
HMUR: Analog Mute Control for HPR (Line or Headphone R-Channel)

Default value: 1

HPOL/LOL and HPOR/LOR can be independently muted to zero level when HMUL and HMUR = 1. The HMUx mute takes precedence over analog volume level settings.

HMUL, HMUR = 0 Mute disabled
HMUL, HMUR = 1 Mute enabled (default)

HLV[5:0]: Analog Volume for HPL (Headphone L-Channel)
HRV[5:0]: Analog Volume for HPR (Headphone R-Channel)

Default value: 00 0000.

HPOL/LOL and HPOR/LOR can be independently controlled from 6 dB to -70 dB, with step size depending on the gain level. Outputs may have zipper noise while changing levels. In the PCM3793/94, the noise can be reduced when making the change by using zero-cross detection (register 85, ZCRS).

Table 7. Headphone Gain Level Setting

HLV[5:0 HRV[5:0		STEP	GAIN LEVEL SETTING	HLV[5:0] HRV[5:0		STEP	GAIN LEVEL SETTING	HLV[5:0 HRV[5:0		STEP	GAIN LEVEL SETTING
11 1111	3F		6 dB	10 1001	29		−5 dB	01 0011	13		–21 dB
11 1110	3E		5.5 dB	10 1000	28		−5.5 dB	01 0010	12	1 dB	–22 dB
11 1101	3D		5 dB	10 0111	27		−6 dB	01 0001	11	IUB	-23 dB
11 1100	3C		4.5 dB	10 0110	26		−6.5 dB	01 0000	10		-24 dB
11 1011	3B		4 dB	10 0101	25		−7 dB	00 1111	0F		-26 dB
11 1010	3A		3.5 dB	10 0100	24		−7.5 dB	00 1110	0E		–28 dB
11 1001	39		3 dB	10 0011	23	0.5 dB	-8 dB	00 1101	0D		-30 dB
11 1000	38		2.5 dB	10 0010	22		−8.5 dB	00 1100	0C		−32 dB
11 0111	37		2 dB	10 0001	21		−9 dB	00 1011	0B	2 dB	-34 dB
11 0110	36		1.5 dB	10 0000	20		−9.5 dB	00 1010	0A		-36 dB
11 0101	35	0.5 dB	1 dB	01 1111	1F		-10 dB	00 1001	09		-38 dB
11 0100	34	0.5 db	0.5 dB	01 1110	1E		−10.5 dB	00 1000	08		-40 dB
11 0011	33		0 dB	01 1101	1D		-11 dB	00 0111	07		-42 dB
11 0010	32		−0.5 dB	01 1100	1C		−12 dB	00 0110	06		-46 dB
11 0001	31		-1 dB	01 1011	1B		-13 dB	00 0101	05		-50 dB
11 0000	30		−1.5 dB	01 1010	1A		−14 dB	00 0100	04		−54 dB
10 1111	2F		–2 dB	01 1001	19		−15 dB	00 0011	03	4 dB	−58 dB
10 1110	2E		−2.5 dB	01 1000	18	1 dB	−16 dB	00 0010	02		−62 dB
10 1101	2D		−3 dB	01 0111	17		–17 dB	00 0001	01		-66 dB
10 1100	2C		−3.5 dB	01 0110	16		–18 dB	00 0000	00		-70 dB
10 1011	2B		−4 dB	01 0101	15		−19 dB				
10 1010	2A		– 4.5 dB	01 0100	14		-20 dB				-



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	B15	B14	B13	B12	B11	B10	В9	B8	B7	B6	B5	B4	В3	B2	B1	В0
Register 66	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	SMUL	SLV5	SLV4	SLV3	SLV2	SLV1	SLV0
Register 67	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	SMUR	SRV5	SRV4	SRV3	SRV2	SRV1	SRV0

**IDX[6:0]:** 100 0010b (42h): Register 66 **IDX[6:0]:** 100 0011b (43h): Register 67

SMUL: Digital Soft Mute Control for SPL (Speaker Output, L-Channel) SMUR: Digital Soft Mute Control for SPR (Speaker Output R-Channel)

Default value: 1

SPOLP/SPOLN and SPORP/SPORN can be independently muted to the zero level when HMUL and HMUR = 1. The SMUx mute takes precedence over analog volume level settings.

SMUL, SMUR = 0 Mute disabled
SMUL, SMUR = 1 Mute enabled (default)

SLV[5:0]: Gain Setting for SPL (Speaker Output L-Channel) SRV[5:0]: Gain Setting for SPR (Speaker Output R-Channel)

Default value: 00 0000.

SPOLP/SPOLN and SPORP/SPORN can be independently controlled from 6 dB to -70 dB, with step size depending on the gain level. Outputs may have zipper noise while changing levels. In the PCM3793, the noise can be reduced when making the change by using zero-cross detection (register 85, ZCRS).

**Table 8. Speaker Gain Level Setting** 

SLV[5:0 SRV[5:0		STEP	GAIN LEVEL SETTING	SLV[5:0] SRV[5:0		STEP	GAIN LEVEL SETTING	SLV[5:0] SRV[5:0		STEP	GAIN LEVEL SETTING
11 1111	3F		6 dB	10 1001	29		–5 dB	01 0011	13		–21 dB
11 1110	3E		5.5 dB	10 1000	28		−5.5 dB	01 0010	12	1 dB	-22 dB
11 1101	3D		5 dB	10 0111	27		−6 dB	01 0001	11	TUB	-23 dB
11 1100	3C		4.5 dB	10 0110	26		−6.5 dB	01 0000	10		-24 dB
11 1011	3B		4 dB	10 0101	25		–7 dB	00 1111	0F		-26 dB
11 1010	ЗА		3.5 dB	10 0100	24		-7.5 dB	00 1110	0E		-28 dB
11 1001	39		3 dB	10 0011	23	0.5 dB	–8 dB	00 1101	0D		-30 dB
11 1000	38		2.5 dB	10 0010	22		−8.5 dB	00 1100	0C		-32 dB
11 0111	37		2 dB	10 0001	21		−9 dB	00 1011	0B	2 dB	-34 dB
11 0110	36		1.5 dB	10 0000	20		−9.5 dB	00 1010	0A		-36 dB
11 0101	35	0.5 dB	1 dB	01 1111	1F		-10 dB	00 1001	09		-38 dB
11 0100	34	0.5 dB	0.5 dB	01 1110	1E		-10.5 dB	00 1000	08		-40 dB
11 0011	33		0 dB	01 1101	1D		–11 dB	00 0111	07		-42 dB
11 0010	32		−0.5 dB	01 1100	1C		–12 dB	00 0110	06		-46 dB
11 0001	31		–1 dB	01 1011	1B		–13 dB	00 0101	05		–50 dB
11 0000	30		−1.5 dB	01 1010	1A		–14 dB	00 0100	04		–54 dB
10 1111	2F		−2 dB	01 1001	19		–15 dB	00 0011	03	4 dB	–58 dB
10 1110	2E		-2.5 dB	01 1000	18	1 dB	–16 dB	00 0010	02		–62 dB
10 1101	2D		−3 dB	01 0111	17		–17 dB	00 0001	01		–66 dB
10 1100	2C		−3.5 dB	01 0110	16		–18 dB	00 0000	00		-70 dB
10 1011	2B		–4 dB	01 0101	15		–19 dB				
10 1010	2A		– 4.5 dB	01 0100	14		-20 dB				



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	B15	B14	B13	B12	B11	B10	В9	B8	B7	B6	B5	B4	В3	B2	B1	В0
Register 68	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	PMUL	ATL5	ATL4	ATL3	ATL2	ATL1	ATL0
Register 69	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	PMUR	ATR5	ATR4	ATR3	ATR2	ATR1	ATR0

IDX[6:0]: 100 0100b (44h): Register 68 IDX[6:0]: 100 0101b (45h): Register 69

PMUL: Digital Soft Mute Control for DAL (DAC, L-Channel)
PMUR: Digital Soft Mute Control for DAR (DAC R-Channel)

Default value: 0

The digital input to the DAC can be independently muted or unmuted. The transition from the current volume level to mute, or the return to the previous volume setting from mute, occurs at the rate of one 1-dB step for each  $8/f_S$  time period. When PMUL and PMUR = 0, the digital data is increased from mute to the previous attenuation level, and when PMUL and PMUR = 1, the digital data is decreased from the current attenuation level to mute. In the PCM3793/94, audible zipper noise can be reduced by using zero-cross detection (register 85, ZCRS).

PMUL, PMUR = 0	Mute disabled (default)
PMUL, PMUR = 1	Mute enabled

ATL[5:0]: Digital Attenuation Setting for DAL (L-Channel DAC)
ATR[5:0]: Digital Attenuation Setting for DAR (R-Channel DAC)

Default value: 11 1111b

The digital inputs to the DAC can be independently attenuated. The attenuation of each digital input is controlled in 1-dB step for every 8/f<sub>S</sub> time period. Audible zipper noise in the PCM3793/94 can be reduced by changing the attenuation with zero-cross detection (register 85, ZCRS).

**Table 9. Digital Attenuation Setting** 

ATL[5:0 ATR[5:0		ATTENUATION LEVEL SETTING	ATL[5:0] ATR[5:0		ATTENUATION LEVEL SETTING	ATL[5:0] ATR[5:0		ATTENUATION LEVEL SETTING		
11 1111	3F	0 dB (default)	10 1001	29	–22 dB	01 0011	13	-44 dB		
11 1110	3E	−1 dB	10 1000	28	–23 dB	01 0010	12	-45 dB		
11 1101	3D	−2 dB	10 0111	27	–24 dB	01 0001	11	-46 dB		
11 1100	3C	−3 dB	10 0110	26	–25 dB	01 0000	10	–47 dB		
11 1011	3B	−4 dB	10 0101	25	–26 dB	00 1111	0F	–48 dB		
11 1010	3A	−5 dB	10 0100	24	–27 dB	00 1110	0E	-49 dB		
11 1001	39	−6 dB	10 0011	23	–28 dB	00 1101	0D	–50 dB		
11 1000	38	−7 dB	10 0010	22	–29 dB	00 1100	0C	–51 dB		
11 0111	37	−8 dB	10 0001	21	-30 dB	00 1011	0B	–52 dB		
11 0110	36	−9 dB	10 0000	20	−31 dB	00 1010	0A	–53 dB		
11 0101	35	-10 dB	01 1111	1F	-32 dB	00 1001	09	-54 dB		
11 0100	34	–11 dB	01 1110	1E	–33 dB	00 1000	08	–55 dB		
11 0011	33	−12 dB	01 1101	1D	−34 dB	00 0111	07	–56 dB		
11 0010	32	–13 dB	01 1100	1C	–35 dB	00 0110	06	–57 dB		
11 0001	31	−14 dB	01 1011	1B	−36 dB	00 0101	05	–58 dB		
11 0000	30	−15 dB	01 1010	1A	−37 dB	00 0100	04	–59 dB		
10 1111	2F	−16 dB	01 1001	19	–38 dB	00 0011	03	-60 dB		
10 1110	2E	–17 dB	01 1000	18	-39 dB	00 0010	02	-61 dB		
10 1101	2D	–18 dB	01 0111	17	-40 dB	00 0001	01	-62 dB		
10 1100	2C	–19 dB	01 0110	16	-41 dB	00 0000	00	Mute		
10 1011	2B	–20 dB	01 0101	15	-42 dB					
10 1010	2A	–21 dB	01 0100	14	-43 dB					



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	B15	B14	B13	B12	B11	B10	В9	В8	В7	В6	B5	B4	В3	B2	B1	В0
Register 70	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	DEM1	DEM0	PFM1	PFM0	RSV	RSV	RSV	OVER

IDX[6:0]: 100 0110b (46h): Register 70
DEM[1:0]: De-Emphasis Filter Selection

Default value: 00

The digital de-emphasis filter is in front of the interpolation filter. One of three de-emphasis filters can be selected, corresponding to sampling rate, 32 kHz, 44.1 kHz, or 48 kHz.

DEM[1:0]	De-Emphasis Filter Selection
00	OFF (default)
01	32 kHz
10	44.1 kHz
11	48 kHz

#### PFM[1:0]: Audio Interface Selection for DAC (Digital Input)

Default value: 00

The audio interface for the DAC digital input has I<sup>2</sup>S, right-justified, left-justified, and DSP formats.

PFM[1:0]	Audio Interface Selection for DAC Digital Input
00	I <sup>2</sup> S format (default)
01	Right-justified format
10	Left-justified format
11	DSP format

#### **OVER: Oversampling Control for Delta-Sigma DAC**

Default value: 0

This bit is used to control the oversampling rate of delta-sigma DAC. When the PCM3793/94 operates at low sampling rates, less than 24 kHz with SCKI frequency less than 12.5 MHz, using this function with OVER = 1 is recommended.

OVER = 0	128 f <sub>S</sub> (default)
OVER = 1	192 f <sub>S</sub> , 256 f <sub>S</sub> , 384 f <sub>S</sub>



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	B15	B14	B13	B12	B11	B10	В9	B8	B7	B6	B5	B4	В3	B2	B1	В0
Register 71	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	RSV	SPSE	SPS1	SPS0	DFQ1	DFQ0

IDX[6:0]: 100 0111b (47h): Register 71 SPSE: Enable of Spectrum Spreading

Default value: 0

The class-D speaker amplifier output can cause RF interference due to switching noise. The PCM3793 can reduce peak noise by the use of spectrum spreading technology when SPSE = 1.

SPSE = 0	Disable (default)
SPSE = 1	Enable

#### SPS[1:0]: Spectrum Spreading Efficiency

Default value: 00

The efficiency of spectrum spreading technology can be changed to low, medium, or high.

SPS[1:0]	Spectrum Spreading Efficiency	
00	Low (default)	
01	Medium	
10	High	
11	Reserved	

#### DFQ[1:0]: Switching Frequency for Speaker Amplifier (Class-D)

Default value: 00

Switching frequency for the class-D speaker amplifier can be selected to avoid interference with other equipment.

DFQ[1:0]			Class [	) Amplif	ier Swit	ching	Freque	ncy								
00		1.5 MHz (default)														
01			2.25 MI	Ηz												
10			2.65 MI	Ηz												
11			3 MHz													
	B15	B14	B13	B12	B11	B10	В9	В8	В7	В6	B5	B4	В3	B2	B1	В0
Register 72	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	RSV	RSV	RSV	RSV	PMXR	PMXL

IDX[6:0]: 100 1000b (48h) Register 72

PMXR: Power Up/Down for MXR (Mixer R-Channel)
PMXL: Power Up/Down for MXL (Mixer L-Channel)

Default value: 0

These bits are used to control power up and down for the analog mixer.

PMXL, PMXR = 0	Power down (default)
PMXL, PMXR = 1	Power up



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B15 В0 B14 B13 B12 B11 B10 В9 B8 B7 B6 B5 B4 ВЗ B2 B1 0 IDX6 IDX5 IDX4 IDX3 IDX2 IDX1 IDX0 PBIS PDAR PDAL PHPC PHPR PHPL PSPR PSPL Register 73

IDX[6:0]: 100 1001b (49h): Register 73
PBIS: Power Up/Down Control for Bias

Default value: 0

This bit is used to control power up/down for the analog bias circuit.

PBIS = 0 Power down (default)

PBIS = 1 Power up

PDAR: Power Up/Down Control for DAR (DAC and R-Channel Digital Filter)
PDAL: Power Up/Down Control for DAL (DAC and L-Channel Digital Filter)

Default value: 0

This bit is used to control power up/down for the DAC and interpolation filter.

PDAR, PDAL = 0 Power down (default)

PDAR, PDAL = 1 Power up

PHPC: Power Up/Down Control for HPC (Headphone COM/Monaural Output)

Default value: 0

This bit is used to control power up/down for the headphone COM or monaural line amplifier.

PHPC = 0 Power down (default)

PHPC = 1 Power up

PHPR: Power Up/Down Control for HPR (Line or R-Channel Headphone Output)

PHPL: Power Up/Down Control for HPL (Line or L-Channel Headphone Output)

Default value: 0

This bit is used to control power up/down for the headphone amplifier.

PHPR, PHPL = 0 Power down (default)

PHPR, PHPL = 1 Power up

PSPR: Power Up/Down Control for SPR (R-Channel Speaker Output, PCM3793)

PSPL: Power Up/Down Control for SPL (L-Channel Speaker Output, PCM3793)

Default value: 0

This bit is used to control power up/down for the PCM3793 speaker amplifier. This bit is should be set to 0 for the PCM3794, because it has no speaker outputs.

PSPR, PSPL = 0 Power down (default)

PSPR, PSPL = 1 Power up



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	B15	B14	B13	B12	B11	B10	В9	B8	B7	B6	B5	B4	В3	B2	B1	В0
Register 74	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	CMS2	CMS1	CMS0	HPS1	HPS0	SPKS	PCOM

IDX[6:0]: 100 1010b (4Ah): Register 74

#### CMS[2:0]: Output Selection for HPC (Headphone COM/Monaural Output)

Default value: 000

HPCOM/MONO output can be selected from several input analog sources, including inverted HPOR output, inverted HPOL output, and monaural output.

CMS[2:0]	HPCOM/MONO Output Selection
0 0 0	Common voltage (0.5 V <sub>CC</sub> ) output for capless mode (default)
0 0 1	Monaural output
0 1 0	Inverted HPOL output
1 0 0	Inverted HPOR output
Others	Reserved

#### HPS[1:0]: Line or Headphone Output Configuration

Default value: 00

The HPOL/LOL and HPOR/LOR output configuration can be selected as follows.

HPS[1:0]	Line or Headphone Output Configuration
0 0	Stereo output (default)
0 1	Single monaural output
1 0	Differential monaural output
1 1	Reserved

#### **SPKS: Speaker Output Configuration**

Default value: 00

The SPOLP/SPOLN and SPORP/SPORN output configuration can be selected as follows.

SPKS = 0	Stereo output (default)
SPKS = 1	Monaural output

# PCOM: Power Up/Down Control for V<sub>COM</sub>

Default value: 0

This bit is used to control power up/down for V<sub>COM</sub>.

PCOM = 0	Power down (default)
PCOM = 1	Power up



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	B15	B14	B13	B12	B11	B10	B9	В8	B7	B6	B5	B4	В3	B2	B1	B0
Register 75	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	HPDP	HPDE	RSV	SDHC	SDHR	SDHL	SDSR	SDSL

IDX[6:0]: 1001011b (4Bh): Register 75

HPDP: Headphone Insertion Detection Polarity
HPDE: Enable for Headphone Insertion Detection

Default value: 0

**Table 10. Headphone Insertion Detection** 

HPDE	HPDP	HDTI (PIN 8)	HP OUTPUT	SP OUTPUT
1	0	0	Down	Up
1	0	1	Up	Down
1	1	0	Up	Down
1	1	1	Down	Up
0	X	Х	Headphone insertio	n detection disabled

SDHC: Short Protection Disable for HPC (Headphone COM/Monaural Output)

SDHR: Short Protection Disable for HPR (R-Channel Headphone) SDHL: Short Protection Disable for HPL (L-Channel Headphone)

Default value: 0

Short-circuit protection can be disabled if this function is not needed in an application.

SDHC, SDHR, SDHL = 0 Enabled (default)
SDHC, SDHR, SDHL = 1 Disabled

SDSR: Thermal Protection Disable for SPR (Speaker Amplifier R-Channel)

SDSL: Thermal Protection Disable for SPL (Speaker Amplifier L-Channel)

Default value: 0

The thermal protection circuit can be disabled if this function is not needed in an application.

SDSR, SDSL = 0 Enabled (default)
SDSR, SDSL = 1 Disabled



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	B15	B14	B13	B12	B11	B10	В9	В8	В7	В6	B5	B4	В3	B2	B1	В0
Register 76	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	RSV	RSV	RSV	RSV	RLSR	RLSL

IDX[6:0]: 100 1100b (4Ch): Register 76

RLSR: Reset Thermal Protection Circuit for SPR (R-Channel Speaker Amplifier) RLSL: Reset Thermal Protection Circuit for SPL (L-Channel Speaker Amplifier)

Default value: 0

Short-circuit protection puts the device in power-down status after it detects a temperature of approximately 150°C on the die. These bits must be set to 1 to restore power to the speaker amplifier.

RLSR, RLSL	= 0		Operation (default)													
RLSR, RLSL	= 1		Reset (set to 0 automatically after being set to 1)													
	B15	B14	B13	B12	B11	B10	В9	В8	В7	В6	B5	B4	В3	B2	B1	В0
Register 77	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	HPDS	RSV	RSV	STHC	STHR	STHL	STSR	STSL

IDX[6:0]: 100 1101b (4Dh): Register 77 HPDS: Headphone Detection Status

Default value: 0

The HPDS bit shows the status of insert detection for the headphone. This is a read-only bit. The polarity depends on register 75 HPDP setting.

HPDS = 0	HDTI input (when HPDP = 0) (default)
HPDS = 1	Inverted HDTI input (When HPDP = 1)

STHC: Short Protection Status for HPC (Headphone COM/Monaural Output)

STHR: Short Protection Status for HPR (R-Channel Headphone)

STHL: Short Protection Status for HPL (L-Channel Headphone)

These bits can be read through the I<sup>2</sup>C interface to determine short protection status.

STHC, STHR, STHL = 0	Detect short circuit
STHC, STHR, STHL = 1	Not detect short circuit

STSR: Thermal Protection Status for SPR (R-Channel Speaker)

STSL: Thermal Protection Status for SPL (L-Channel Speaker)

These bits can be read through the I<sup>2</sup>C interface to determine thermal protection status.

STSR, STSL = 0	Detect thermal protection
STSR, STSL = 1	Not detect thermal protection



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	B15	B14	B13	B12	B11	B10	В9	B8	В7	B6	B5	B4	В3	B2	B1	В0
Register 79	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	ALV5	ALV4	ALV3	ALV2	ALV1	ALV0
Register 80	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	ARV5	ARV4	ARV3	ARV2	ARV1	ARV0

**IDX[6:0]:** 100 1111b (4Fh): Register 79 **IDX[6:0]:** 101 0000b (50h): Register 80

ALV[5:0]: Gain Control for PG3 (R-Channel ADC Analog Input)
ARV[5:0]: Gain Control for PG4 (L-Channel ADC Analog Input)

Default value: 00

PG3 and PG4 can be independently controlled for ADC input from 30 dB to −12 dB in 1-dB steps. The ADC output may have zipper noise while changing the level. In the PCM3793/94, the noise can be reduced when making the change by using zero-cross detection (register 85, ZCRS).

**Table 11. Gain Level Setting** 

ALV[5:0], ARV[5:0]		GAIN LEVEL SETTING	ALV[5:0], ARV[5:0]		GAIN LEVEL SETTING
10 1010	2A	30 dB	01 0100	14	8 dB
10 1001	29	29 dB	01 0011	13	7 dB
10 1000	28	28 dB	01 0010	12	6 dB
10 0111	27	27 dB	01 0001	11	5 dB
10 0110	26	26 dB	01 0000	10	4 dB
10 0101	25	25 dB	00 1111	0F	3 dB
10 0100	24	24 dB	00 1110	0E	2 dB
10 0011	23	23 dB	00 1101	0D	1 dB
10 0010	22	22 dB	00 1100	0C	0 dB
10 0001	21	21 dB	00 1011	0B	–1 dB
10 0000	20	20 dB	00 1010	0A	–2 dB
01 1111	1F	19 dB	00 1001	09	−3 dB
01 1110	1E	18 dB	00 1000	08	–4 dB
01 1101	1D	17 dB	00 0111	07	−5 dB
01 1100	1C	16 dB	00 0110	06	−6 dB
01 1011	1B	15 dB	00 0101	05	–7 dB
01 1010	1A	14 dB	00 0100	04	−8 dB
01 1001	19	13 dB	00 0011	03	−9 dB
01 1000	18	12 dB	00 0010	02	-10 dB
01 0111	17	11 dB	00 0001	01	-11 dB
01 0110	16	10 dB	00 0000	00	-12 dB (default)
01 0101	15	9 dB			



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	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	В3	B2	B1	В0
Register 81	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	HPF1	HPF0	RMUL	RMUR	RSV	DSMC	RFM1	RFM0

IDX[6:0]: 101 0001b (51h): Register 81 HPF[1:0]: High-Pass Filter Selection

Default value: 00

PCM3793/94 has digital high-pass filter to remove dc voltage at the input of the ADC. The cutoff frequency of the high-pass filter can be selected.

HPF [1:0]	High-Pass Filter Selection	
0 0	$f_C = 4 \text{ Hz at } 48 \text{ kHz (default)}$	
0 1	$f_C = 240 \text{ Hz at } 48 \text{ kHz}$	
1 0	Reserved	
1 1	High-pass filter disabled	

RMUL: Digital Soft Mute Control for L-Channel ADC RMUR: Digital Soft Mute Control for R-Channel ADC

Default value: 1

The digital output of the ADC can be independently muted or unmuted. The transition from the current volume level to mute, or the return to the previous volume setting from mute, occurs at the rate of one 1-dB step for each  $8/f_S$  time period. When PMUL and PMUR = 0, the digital data is increased from mute to the previous attenuation level, and when PMUL and PMUR = 1, the digital data is decreased from the current attenuation level to mute. In the PCM3793/94, audible zipper noise can be reduced by using zero-cross detection (register 85, ZCRS).

RMUL, RMUR = 0	Mute disabled
RMUL, RMUR = 1	Mute enabled (default)

## DSMC: Waiting Time for ADC Mute Off at Power Up

Default value: 0

The ADC digital output has an optional delay after power up when DSMC = 0. It is recommended to set DSMC = 0.

DSMC = 0	10 ms at 48 kHz (default)
DSMC = 1	No delay

## RFM[1:0]: Audio Interface Selection for ADC (Digital Output)

Default value: 00

The audio interface for the ADC digital input supports I<sup>2</sup>S, right-justified, left-justified, and DSP formats.

RFM [1:0]	Audio Interface Selection for ADC Digital Output
0 0	I <sup>2</sup> S format (default)
0 1	Right-justified format
1 0	Left-justified format
1 1	DSP format

# PCM3793 is Not Recommended for New Designs



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	B15	B14	B13	B12	B11	B10	В9	В8	B7	В6	B5	B4	В3	B2	B1	В0
Register 82	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	PAIR	PAIL	PADS	PMCB	PADR	PADL

IDX[6:0]: 101 0010b (52h): Register 82

PAIR: Power Up/Down for PG2 and PG6 (Gain Amplifier for R-Channel Analog Input)
PAIL: Power Up/Down for PG1 and PG5 (Gain Amplifier for L-Channel Analog Input)

Default value: 0

This bit is used to control power up/down for PG2 and PG6 (gain amplifier for analog input).

PAIR, PAIL = 0	Power down (default)
PAIR, PAIL = 1	Power up

## PADS: Power Up/Down for D2S (Differential Amplifier) of AIN1L and AIN1R

Default value: 0

This bit is used to control power up/down for D2S (differential-to-single amplifier).

PADS = 0	Power down (default)
PADS = 1	Power up

#### PMCB: Power Up/Down Control for Microphone Bias Source

Default value: 0

This bit is used to control power up/down for the microphone bias source.

PMCB = 0	Power down (default)
PMCB = 1	Power up

## PADR: Power Up/Down Control for ADR (ADC and R-Channel Digital Filter)

## PADL: Power Up/Down Control for ADL (ADC and L-Channel Digital Filter)

Default value: 0

This bit is used to control power up/down for the ADC and decimation filter.

PADR, PADL = 0	Power down (default)
PADR, PADL = 1	Power up



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	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	В3	B2	B1	В0
Register 83	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RALC	RSV	RRTC	RATC	RCP1	RCP0	RLV1	RLV0

IDX[6:0]: 101 0011b (53h): Register 83

## RALC: Automatic Level Control (ALC) Enable for Recording

Default value: 0

Automatic level control can be enabled with some parameters for microphone input or lower analog source level.

RALC = 0	Disable (default)
RALC = 1	Enable

## **RRTC: ALC Recovery Time Control for Recording**

Default value: 0

This bit is used to select the recovery time for the ALC. The response is shown in Figure 36.

RRTC = 0	3.4 s (default)
RRTC = 1	13.6 s

## **RATC: ALC Attack Time Control for Recording**

Default value: 0

This bit is used to select the attack time for the ALC. The response is shown in Figure 36.



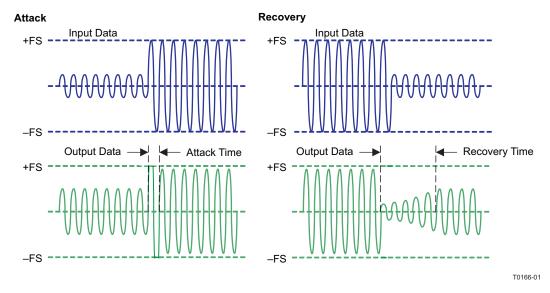


Figure 36. Attack and Recovery Time Response



## RCP[1:0]: ALC Compression Level Control for Recording

Default value: 00

These bits are used to set the compression level for the ALC. The characteristic is shown in Figure 37.

RCP[1:0]	ALC Compression Level Control for Recording
0 0	-2 dB (default)
0 1	−6 dB
1 0	–12 dB
1 1	Reserved

## RLV[1:0]: ALC Expansion Level Control for Recording

Default value: 00

These bits are used to set the expansion level for the ALC. The characteristic is shown in Figure 37.

RLV[1:0]	ALC Gain Level Control for Recording
0 0	0 dB (default)
0 1	6 dB
1 0	14 dB
1 1	24 dB

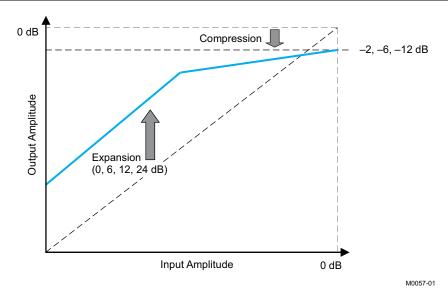


Figure 37. Compression and Expansion Characteristics

# PCM3793 is Not Recommended for New Designs

# PCM3793 PCM3794



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Register 84 Register 85 Register 86

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	В3	B2	B1	В0
0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	RSV	RSV	RSV	MSTR	RSV	BIT0
0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	SRST	RSV	NPR5	NPR4	NPR3	NPR2	NPR1	NPR0
0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	MBST	MSR2	MSR1	MSR0	ATOD	RSV	RSV	ZCRS

IDX[6:0]: 101 0100b (54h): Register 84 IDX[6:0]: 101 0101b (55h): Register 85 IDX[6:0]: 101 0110b (56h): Register 86

MSTR: Master or Slave Selection for Audio Interface

Default value: 0

This bit is used to select either master or slave mode for the audio interface. In master mode, the PCM3793/94 generates LRCK and BCK from the system clock. In slave mode, it receives LRCK and BCK from another device.

MSTR = 0	Slave interface (default)
MSTR = 1	Master interface

## **BIT0: Bit Length Selection for Audio Interface**

Default value: 1

This bit is used to select the data bit length for DAC input.

BIT0 = 0	Reserved
BIT0 = 1	16 bits (default)

## **SRST: System Reset**

Default value: 0

This bit is used to enable system reset. All circuits are reset by setting SRST = 1. After completing the reset sequence, SRST is set to 0 automatically.

SRST = 0	Reset disabled (default)
SRST = 1	Reset enabled

## NPR[5:0]: System Clock Rate Selection

Default value: 000000

#### MSR[2:0]: System Clock Dividing Rate Selection in Master Mode (Register 70)

Default value: 000

These bits are used to select the system clock rate and the dividing rate of the input system clock. See Table 12 for the details.



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# Table 12. System Clock Frequency for Common-Audio Clock

SYSTEM CLOCK	ADC SAMPLING RATE	DAC SAMPLING RATE	REGISTER S	BIT CLOCK		
SCK (MHz)	ADC f <sub>S</sub> (kHz)	DAC f <sub>S</sub> (kHz)	MSR[2:0]	NPR[5:0]	BCK (f <sub>S</sub> )	
	24 (SC	K/256)	010	00 0000	64	
	16 (SC	CK/384)	011	00 0000	64	
6.144	12 (SC	CK/512)	100	00 0000	64	
0.144	8 (SC	K/768)	101	00 0000	64	
	6 (SCF	(/1024)	110	00 0000	64	
	4 (SCF	(/1536)	111	00 0000	64	
	32 (SC	K/256)	010	00 0000	64	
8.192	16 (SC	CK/512)	100	00 0000	64	
	8 (SCF	(/1024)	110	00 0000	64	
	48 (SC	CK/256)	010	00 0000	64	
	32 (SC	CK/384)	011	00 0000	64	
40.000	24 (SC	CK/512)	100 00 0000		64	
12.288	16 (SC	CK/768)	101	00 0000	64	
	12 (SC	K/1024)	110	00 0000	64	
	8 (SCF	(/1536)	111	00 0000	64	
	48 (SC	CK/384)	011	00 0000	64	
18.432	24 (SC	K/768)	101	00 0000	64	
	12 (SC	K/1536)	111	00 0000	64	
	22.05 (S	6CK/256)	010	00 0000	64	
	14.7 (S	CK/384)	011	00 0000	64	
5.6448	11.025 (\$	SCK/512)	100	00 0000	64	
5.0446	7.35 (S	CK/768)	101	00 0000	64	
	5.5125 (S	SCK/1024)	110	00 0000	64	
	3.675 (S	CK/1536)	111	00 0000	64	
	44.1 (S	CK/256)	010	00 0000	64	
	29.4 (S	CK/384)	011	00 0000	64	
11 2006	22.05 (S	SCK/512)	100	00 0000	64	
11.2896	14.7 (S	CK/768)	101	00 0000	64	
	11.025 (S	SCK/1024)	110	00 0000	64	
	7.35 (SC	CK/1536)	111	00 0000	64	

<sup>(1)</sup> Other settings are reserved.

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# Table 13. System Clock Frequency for Application-Specific Clock

SYSTEM CLOCK	ADC SAMPLING RATE	DAC SAMPLING RATE	REGISTER	BIT CLOCK		
SCK (MHz)	ADC f <sub>S</sub> (kHz)	DAC f <sub>S</sub> (kHz)	MSR[2:0]	NPR[5:0]	BCK (f <sub>S</sub> )	
	48.214 (	SCK/280)	010	00 0010	70	
	44.407 (	SCK/304)	010	00 0001	76	
	32.142 (	SCK/420)	010	10 0010	70	
40.5	24.107 (	SCK/560)	100	00 0010	70	
13.5	22.203 (\$	SCK/608)	100	00 0001	76	
	16.071 (\$	SCK/840)	100	10 0010	70	
	12.053 (S	SCK/1120)	110	00 0010	70	
	8.035 (S	CK/1680)	110	10 0010	70	
	48.214 (	SCK/560)	010	01 0010	70	
	44.407 (	SCK/608)	010	01 0001	76	
	32.142 (	SCK/840)	010	11 0010	70	
-	24.107 (S	SCK/1120)	100	01 0010	70	
27	22.203 (S	SCK/1216)	100	01 0001	76	
	16.071 (S	SCK/1680)	100	11 0010	70	
	12.053 (\$	SCK/2240)	110	01 0010	70	
	8.035 (S	CK/3360)	110	11 0010	70	
	48.387 (	SCK/248)	010	00 0100	62	
	44.117 (	SCK/272)	010	00 0011	68	
	32.258 (	SCK/372)	010	10 0100	62	
40	24.193 (	SCK/496)	100	00 0100	62	
12	22.058 (\$	SCK/544)	100	00 0011	68	
	16.129 (	SCK/744)	100	10 0100	62	
	12.096 (	SCK/992)	110	00 0100	62	
	8.064 (S	CK/1488)	110	10 0100	62	
	48.387 (	SCK/496)	010	01 0100	62	
	44.117 (	SCK/544)	010	01 0011	68	
	32.258 (	SCK/744)	010	11 0100	62	
0.4	24.193 (	SCK/992)	100	01 0100	62	
24	22.058 (\$	SCK/1088)	100	01 0011	68	
	16.129 (S	SCK/1488)	100	11 0100	62	
	12.096 (S	SCK/1984)	110	01 0100	62	
	8.064 (S	CK/2976)	110	11 0100	62	
	48.484 (\$	SCK/396)	011	00 0110	66	
	44.444 (	SCK/432)	011	00 0101	72	
	32.323 (	SCK/594)	011	10 0110	66	
40.0	24.242 (	SCK/792)	101	00 0110	66	
19.2	22.222 (	SCK/864)	101	00 0101	72	
	16.161 (S	SCK/1188)	101	10 0110	66	
	12.121 (S	SCK/1584)	111	00 0110	66	
	8.080 (S	CK/2376)	111	10 0110	66	



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# Table 13. System Clock Frequency for Application-Specific Clock (continued)

SYSTEM CLOCK	ADC SAMPLING RATE	DAC SAMPLING RATE	REGISTER	SETTINGS	BIT CLOCK
SCK (MHz)	ADC f <sub>S</sub> (kHz)	DAC f <sub>S</sub> (kHz)	MSR[2:0]	BCK (f <sub>S</sub> )	
	48.484 (	SCK/792)	011	01 0110	66
	44.444 (	SCK/864)	011	01 0101	72
	32.323 (S	SCK/1188)	011	11 0110	66
00.4	24.242 (S	SCK/1584)	101	01 0110	66
38.4	22.222 (S	SCK/1728)	101	01 0101	72
	16.161 (S	SCK/2376)	101	11 0110	66
	12.121 (S	SCK/3168)	111	01 0110	66
	8.080 (S	CK/4752)	111	11 0110	66
	47.794 (	SCK/272)	010	00 1000	68
	43.918 (	SCK/296)	010	00 0111	74
	31.862 (	SCK/408)	010	10 1000	68
13	23.897 (	SCK/544)	100	00 1000	68
13	21.959 (	SCK/592)	100	00 0111	74
	15.931 (	SCK/816)	100	10 1000	68
	11.948 (S	SCK/1088)	110	00 1000	68
	7.965 (S	CK/1632)	110	10 1000	68
	47.794 (	SCK/544)	010	01 1000	68
	43.918 (	SCK/592)	010	01 0111	74
	31.862 (	SCK/816)	010	11 1000	68
26	23.897 (S	SCK/1088)	100	01 1000	68
20	21.959 (S	SCK/1184)	100	01 0111	74
	15.931 (S	SCK/1632)	100	11 1000	68
	11.948 (S	SCK/2176)	110	01 1000	68
	7.965 (S	CK/3264)	110	11 1000	68
	48.235 (	SCK/408)	011	00 1010	68
	44.324 (	SCK/444)	011	00 1001	74
	32.156 (	SCK/612)	011	10 1010	68
19.68	24.117 (	SCK/816)	101	00 1010	68
19.00	22.162 (	SCK/888)	101	00 1001	74
	16.078 (S	SCK/1224)	101	10 1010	68
	12.058 (S	SCK/1632)	111	00 1010	68
	8.039 (S	CK/2448)	111	10 1010	68
	48.235 (	SCK/816)	011	01 1010	68
	44.324 (	SCK/888)	011	01 1001	74
	32.156 (S	SCK/1224)	011	11 1010	68
39.36	24.117 (S	SCK/1632)	101	01 1010	68
33.30	22.162 (\$	SCK/1776)	101	01 1001	74
	16.078 (S	SCK/2448)	101	11 1010	68
	12.058 (S	SCK/3264)	111	01 1010	68
	8.039 (S	CK/4896)	111	11 1010	68

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## **MBST: BCK Output Configuration in Master Mode**

Default value: 0

This bit is used to control the BCK output configuration in master mode. In master mode, this bit sets the BCK output configuration to normal mode or burst mode. In normal mode (MBST = 0), the BCK clock runs continuously. In burst mode (MBST = 1), the BCK clock runs intermittently, and the number of clock cycles per LRCK period is reduced to equal the number of bits of audio data being transmitted. Operating in burst mode reduces the power consumption of  $V_{IO}$  (I/O cell power supply). This is effective in master mode (register 69 MSTR = 1).

MBST = 0	Normal output (default)
MBST = 1	Burst output

## ATOD: ADC Digital Output to DAC Digital Input (Loopback)

Default value: 0

The ADC digital output is internally connected to the DAC digital input by setting ATOD = 1. This setting can be used to debug ADC functions or to monitor a recording.

ATOD= 0	Disabled (default)
ATOD= 1	Enabled

## ZCRS: Zero-Cross for Digital Attenuation/Mute and Analog Gain Setting

Default value: 0

This bit is used to enablethe zero-cross detector, which reduces zipper noise while the digital soft mute, digital attenuation analog gain setting, or analog volume setting is being changed. If no zero-cross data is input for a 512/f<sub>S</sub> period (10.6 ms at a 48-kHz sampling rate), then a time-out occurs and the PCM3793/94 starts changing the attenuation, gain, or volume level. The zero-cross detector cannot be used with continuous-zero and dc data.

ZCRS = 0	Zero cross disabled (default)
ZCRS = 1	Zero cross enabled



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	B15	B14	B13	B12	B11	B10	В9	B8	В7	B6	B5	B4	В3	B2	B1	В0
Register 87	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AD2S	RSV	AIR1	AIR0	RSV	RSV	AIL1	AIL0

IDX[6:0]: 101 0111b (57h): Register 87

## AD2S: Differential Amplifier Selector (MUX3 and MUX4)

Default value: 0

The PCM3793/94 has stereo single-input amplifiers (PG1, PG2) and a monaural differential-input amplifier (D2S) which can be used as ADC inputs. MUX3 and MUX4 can be selected as the monaural differential input by setting AD2S = 1.

AD2S = 0	Single-input amplifiers (default)
AD2S = 1	Differential-input amplifier

## AIL[1:0]: AIN1L, AIN2L, and AIN3L Selector (MUX1)

Default value: 00

This bit is used to select one of the three analog inputs, AIN1L, AIN2L, or AIN3L.

AIL[1:0]	AIN L-channel Select
0 0	Disconnect (default)
0 1	AIN1L
1 0	AIN2L
1 1	AIN3L

## AIR[1:0]: AIN1R, AIN2R, and AIN3R Selector (MUX2)

Default value: 00

This bit is used to select one of the three stereo analog inputs, AIN1R, AIN2R, or AIN3R.

AIR[1:0]	AIN R-channel Select	
0 0	Disconnect (default)	
0 1	AIN1R	
1 0	AIN2R	
1 1	AIN3R	



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	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	В3	B2	B1	В0
Register 88	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	MXR2	MXR1	MXR0	RSV	MXL2	MXL1	MXL0

IDX[6:0]: 101 1000b (58h): Register 88

MXR2: Mixing SW6 to MXR (R-Channel Mixing Amplifier) From L-Channel Analog Input

Default value: 0

This bit is used to connect an analog source to MXR (R-ch mixing amplifier) from the L-ch analog input.

MXR2 = 0	Disable (default)
MXR2 = 1	Enable

#### MXR1: Mixing SW4 to MXR (R-Channel Mixing Amplifier) From R-Channel Analog Input

Default value: 0

This bit is used to connect an analog source to MXR (R-ch mixing amplifier) from the R-ch analog input.

MXR1 = 0	Disable (default)
MXR1 = 1	Enable

#### MXR0: Mixing SW5 to MXR (R-Channel Mixing Amplifier) From R-Channel DAC

Default value: 0

This bit is used to connect an analog source to MXR (R-ch mixing amplifier) from the R-ch DAC.

MXR0 = 0	Disable (default)
MXR0 = 1	Enable

## MXL2: Mixing SW3 to MXL (L-Channel Mixing Amplifier) From R-Channel Analog Input

Default value: 0

This bit is used to connect an analog source to MXL (L-ch mixing amplifier) from the R-ch analog input.

MXL2 = 0	Disable (default)
MXL2 = 1	Enable

## MXL1: Mixing SW1 to MXL (L-Channel Mixing Amplifier) From L-Channel Analog Input

Default value: 0

This bit is used to connect an analog source to MXR (L-ch mixing amplifier) from the L-ch analog input.

MXL1 = 0	Disable (default)
MXL1 = 1	Enable

## MXL0: Mixing SW2 to MXL (L-Channel Mixing Amplifier) From L-Channel DAC

Default value: 0

This bit is used to connect an analog source to MXR (L-ch mixing amplifier) from the L-ch DAC.

MXL0 = 0	Disable (default)
MXL0 = 1	Enable



	B15	B14	B13	B12	B11	B10	В9	B8	B7	B6	B5	B4	В3	B2	B1	B0
Register 89	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	GMR2	GMR1	GMR0	RSV	GML2	GML1	GML0

IDX[6:0]: 101 1001b (59h): Register 89

GMR[2:0]: Gain Level Control for PG6 (Gain Amplifier for Analog Input or R-Channel Bypass) GML[2:0]: Gain Level Control for PG5 (Gain Amplifier for Analog Input or L-Channel Bypass)

Default value: 111

These bits are used for setting the gain level of the analog source to the mixing amplifier. It is recommended to set the gain level to avoid saturation in the analog mixer.

GMR[2:0] GML[2:0]	Gain Level Control for PG6 Gain Level Control for PG5	
0 0 0	–21 dB	
0 0 1	–18 dB	
0 1 0	–15 dB	
0 1 1	–12 dB	
1 0 0	−9 dB	
1 0 1	−6 dB	
110	−3 dB	
1 1 1	0 dB (default)	

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	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	В3	B2	B1	В0
Register 90	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	CMT1	CMT0	RSV	RSV	G20R	G20L

IDX[6:0]: 1011010b (5Ah): Register 90

CMT[1:0]: V<sub>COM</sub> Ramp Up/Down Time Control

Default value: 00

These bits are used for selecting ramp up/down time from ground level to the common-voltage level or from the common-voltage to ground level during the power up/down sequence, in order to reduce audible pop noise.

CMT[1:0]	V <sub>COM</sub> Ramp Up/Down Time Control	
0 0	Nominal; $R_{CMT} = 60 \text{ k}\Omega$ (default)	
0 1	Slow; $R_{CMT} = 120 \text{ k}\Omega$	
1 0	Fast; $R_{CMT} = 30 \text{ k}\Omega$	
1 1	Fastest; $R_{CMT} = 2.73 \text{ k}\Omega$	

## G20R: 20-dB Boost for PG2 (Gain Amplifier for AIN1R, AIN2R, and AIN3R)

Default value: 0

This bit is used to boost the microphone signal when the analog input is small.

G20R = 0	0 dB (default)
G20R = 1	20-dB boost

## G20L: 20-dB Boost for PG1 (Gain Amplifier for AIN1L, AIN2L, and AIN3L)

Default value: 0

This bit is used to boost the microphone signal when the analog input is small.

G20L = 0	0 dB (default)
G20L = 1	20-dB boost



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	B15	B14	B13	B12	B11	B10	В9	B8	B7	B6	B5	B4	В3	B2	B1	В0
Register 92	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	LPAE	RSV	RSV	LGA4	LGA3	LGA2	LGA1	LGA0

IDX[6:0]: 101 1100b (5Ch): Register 92

LPAE: Gain Adjustment for Bass Boost Gain Control

Default value: 0

A gain setting for bass boost may cause digital data may saturation, depending on the input data level. Where this could occur, LPAE can be used to set the same attenuation level as the bass boost gain level for the digital input data.

LPAE = 0	Disable (default)
LPAE = 1	Enable

## LGA[4:0]: Bass Boost Gain Control

Default value: 0 0000

These bits are used to set the bass boost gain level for digital data. The detailed characteristic is shown in the *Typical Performance Curves*.

LGA[4:0]	TONE CONTROL GAIN (BASS)	LGA[4:0]	TONE CONTROL GAIN (BASS)		
0 0000	0 dB (default)	0 1111	0 dB		
0 0011	12 dB	1 0000	–1 dB		
0 0100	11 dB	1 0001	–2 dB		
0 0101	10 dB	1 0010	−3 dB		
0 0110	9 dB	1 0011	–4 dB		
0 0111	8 dB	1 0100	–5 dB		
0 1000	7 dB	1 0101	−6 dB		
0 1001	6 dB	1 0110	−7 dB		
0 1010	5 dB	1 0111	–8 dB		
0 1011	4 dB	1 1000	−9 dB		
0 1100	3 dB	1 1001 –10 dB			
0 1101	2 dB	1 1010	–11 dB		
0 1110	1 dB	1 1011	–12 dB		



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B15 B12 B10 В9 В8 В7 В6 В5 В4 ВЗ B2 В0 B14 B13 B1 Register 93 IDX6 IDX5 IDX4 IDX3 IDX2 IDX1 IDX0 RSV RSV RSV MGA4 MGA3 MGA2 MGA1 MGA0

IDX[6:0]: 101 1101b (5Dh): Register 93
MGA[4:0]: Middle Boost Gain Control

Default value: 00000

These bits are used to set middle boost gain level to digital data. The detailed characteristic is shown in the *Typical Performance Curves*.

MGA[4:0	)]	TO	NE CO	NTROL	GAIN (	<b>IIDRAN</b>	GE)		MGA[4	:0]	TC	NE CO	NTROL (	3 dB						
0 0000				0 dB (	default)				0 111	1			C	) dB						
0 0011				12	2 dB				1 000	0			-1	dB						
0 0100				11	l dB				1 000	1	−2 dB									
0 0101				10	) dB				1 001	0	−3 dB									
0 0110				,	9 dB				1 001	1		–4 dB								
0 0111				1	3 dB				1 010	0			-5	dB						
0 1000					7 dB				1 010	1			-6	dB						
0 1001				(	6 dB				1 011	0			-7	'dB						
0 1010				ţ	5 dB				1 011	1	-8 dB									
0 1011					4 dB				1 100	0	−9 dB									
0 1100				;	3 dB				1 100	1			-10	dB						
0 1101		2 dB							1 101	0	-11 dB									
0 1110		1 dB							1 101	1	–12 dB									
	B15	B14	B13	B12	B11	B10	В9	В8	В7	B6	B5	B4	В3	B2	B1	В0				
Register 94	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	RSV	HGA4	HGA3	HGA2	HGA1	HGA0				

IDX[6:0]: 101 1110b (5Eh): Register 94

HGA[4:0]: Treble Boost Gain Control (f<sub>C</sub> = 5 kHz)

Default value: 00000

These bits are used to set middle boost gain level to digital data. The detailed characteristic is shown in the *Typical Performance Curves*.

HGA[4:0]	TONE CONTROL GAIN (TREBLE)	HGA[4:0]	TONE CONTROL GAIN (TREBLE)
0 0000	0 dB (default)	0 1111	0 dB
0 0011	12 dB	1 0000	–1 dB
0 0100	11 dB	1 0001	−2 dB
0 0101	10 dB	1 0010	–3 dB
0 0110	9 dB	1 0011	–4 dB
0 0111	8 dB	1 0100	–5 dB
0 1000	7 dB	1 0101	−6 dB
0 1001	6 dB	1 0110	–7 dB
0 1010	5 dB	1 0111	–8 dB
0 1011	4 dB	1 1000	−9 dB
0 1100	3 dB	1 1001	–10 dB
0 1101	2 dB	1 1010	–11 dB
0 1110	1 dB	1 1011	–12 dB



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	B15	B14	B13	B12	B11	B10	В9	B8	B7	B6	B5	B4	В3	B2	B1	В0
Register 95	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	SDAS	3DEN	RSV	3FL0	3DP3	3DP2	3DP1	3DP0

IDX[6:0]: 101 1111b (5Fh): Register 95

## SDAS: Source Select for Sound Effect (Tone Control, 3-D Sound, Notch Filter, Mono Mix)

Default value: 0

The PCM3793/94 includes sound effect circuits (tone control, 3-D sound, notch filter, mono mix) which can be used to filter either the digital input to the DAC or the digital output from the ADC. This bit selects the signal source of the sound effect circuit.

SDAS = 0	DAC digital input (default)
SDAS = 1	ADC digital output

## 3DEN: 3-D Sound Effect Enable

Default value: 0

This bit is used for enabling the 3-D sound effect filter. This filter has two independently controlled parameters.

3DEN = 0	Disable (default)
3DEN = 1	Enable

#### 3FL0: Filter Selection for 3-D Sound

Default value: 0

This bit is used for selecting fron two kinds of filter type, narrow and wide. These filters have a different 3-D effect performance.

3FL0 = 0	Narrow (default)
3FL0 = 1	Wide

#### 3DP[3:0]: Efficiency for 3-D Sound Effects

Default value: 0000

These bits are used for adjusting the 3-D sound efficiency. Higher percentages have greater efficiency.

3DP[3:0]	3D Sound Effect Efficiency	
0000	0% (default)	
0 0 0 1	10%	
0010	20%	
0 0 1 1	30%	
0 1 0 0	40%	
0 1 0 1	50%	
0 1 1 0	60%	
0 1 1 1	70%	
1000	80%	
1001	90%	
1010	100%	
1011	Reserved	
: 1111	: Reserved	

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	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	В3	B2	B1	В0
Register 96	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	NEN2	NEN1	NUP2	NUP1	RSV	RSV	RSV	MXEN

IDX[6:0]: 110 0000b (60h): Register 96

## **NEN2: Second-Stage Notch Filter Enable**

Default value: 0

PCM3793/94 has two notch filters with characteristics that can be set separately. This bit is used to enable the second stage.

NEN2 = 0	Disable (default)
NEN2 = 1	Enable

#### **NEN1: First-Stage Notch Filter Enable**

Default value: 0

PCM3793/94 has two notch filters with characteristics that can be set separately. This bit is used to enable the first stage.

NEN1 = 0	Disable (default)
NEN1 = 1	Enable

## NUP2: Second-Stage Notch Filter Coefficients Update

Default value: 0

This bit is used to update the coefficients for 2nd stage notch filter. The coefficients written to registers 101, 102, 103, and 104 are updated when NUP2 = 1.

NUP2 = 0	No Update (default)
NUP2 = 1	Update (set to 0 automatically after set to 1)

#### **NUP1: First-Stage Notch Filter Coefficients Update**

Default value: 0

This bit is used to update the coefficients for the second-stage notch filter. The coefficients written to registers 97, 98, 99, and 100 are updated when NUP1 = 1.

NUP1 = 0	No Update (default)
NUP1 = 1	Update (set to 0 automatically after set to 1)

## **MXEN: Digital Monaural Mixing**

Default value: 0

This bit is used to enable or disable monaural mixing in the section that combines L-ch data and R-ch data.

MXEN = 0	Stereo (default)
MXEN = 1	Monaural Mixing



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B15	B14	B13	B12	B11	B10	В9	B8	B7	B6	B5	B4	В3	B2	B1	В0
0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	F107	F106	F105	F104	F103	F102	F101	F100
0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	F115	F114	F113	F112	F111	F110	F109	F108
0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	F207	F206	F205	F204	F203	F202	F201	F200
0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	F215	F214	F213	F212	F211	F210	F209	F208

IDX[6:0]: 110 0001b (61h): Register 97 IDX[6:0]: 110 0010b (62h): Register 98 IDX[6:0]: 110 0011b (63h): Register 99 IDX[6:0]: 110 0100b (64h): Register 100

F[107:100]: Lower 8 Bits of Coefficient a<sub>1</sub> for First-Stage Notch Filter F[115:108]: Upper 8 Bits of Coefficient a<sub>1</sub> for First-Stage Notch Filter F[207:200]: Lower 8 Bits of Coefficient a<sub>2</sub> for First-Stage Notch Filter F[215:208]: Upper 8 Bits of Coefficient a<sub>2</sub> for First-Stage Notch Filter

Default value: 0000 0000

These bits are used to change the characteristics of the first-stage notch filter. See Figure 38 for details.



#### SLES193C-AUGUST 2006-REVISED FEBRUARY 2007

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	В3	B2	B1	В0
Register 101	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	S107	S106	S105	S104	S103	S102	S101	S100
Register 102	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	S115	S114	S113	S112	S111	S110	S109	S108
Register 103	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	S207	S206	S205	S204	S203	S202	S201	S200
Register 104	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	S215	S214	S213	S212	S211	S210	S209	S208

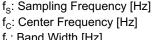
IDX[6:0]: 110 0101b (65h): Register 101 IDX[6:0]: 110 0110b (66h): Register 102 IDX[6:0]: 110 0111b (67h): Register 103 IDX[6:0]: 110 1000b (68h): Register 104

S[107:100]: Lower 8 bits of Coefficient a<sub>1</sub> for Second-Stage Notch Filter S[115:108]: Upper 8 bits of Coefficient a₁ for Second-Stage Notch Filter S[207:200]: Lower 8 bits of Coefficient a<sub>2</sub> for Second-Stage Notch Filter S[215:208]: Upper 8 bits of Coefficient a<sub>2</sub> for Second-Stage Notch Filter

Default value: 00000000

These bits are used to change the characteristics of the second-stage notch filter. See Figure 38 for details.

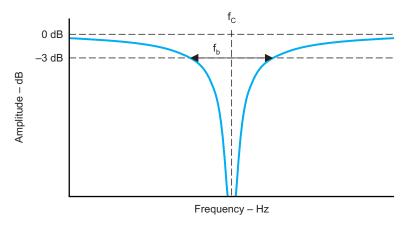
The PCM3793/94 provides two notch filters for the digital input to the DAC or the digital output from the ADC. The optional filter characteristics of each filter are programmable. The characteristics are given by calculating the coefficients for three parameters, sampling frequency, center frequency, and bandwidth, as shown in Figure 38. All coefficients must be written as 2s-complement binary data into registers 97, 98, 99, 100, 101, 102, 103, and 104.



fh: Band Width [Hz]

$$a_1 = -(1 + a_2) \cos \left(\frac{2\pi f_C}{f_S}\right)$$
 (Equation 1)

$$a_2 = \frac{1 - \tan\left(\frac{2\pi f_b/f_S}{2}\right)}{1 + \tan\left(\frac{2\pi f_b/f_S}{2}\right)}$$
 (Equation 2)



M0058-01

Figure 38. Parameter Settings for Notch Filter

The coefficients are calculated using Equation 1 and Equation 2 in Figure 38. An example follows:

 $f_S = 16 \text{ kHz}, f_C = 0.5 \text{ kHz}, f_b = 0.2 \text{ kHz}$ 

 $a_2 = 0.924390492 \rightarrow Decimal to Hex \rightarrow 3B29h$ 

 $a_1 = -1.887413868 \rightarrow Decimal to Hex \rightarrow 8735h$ 

 $a_2$ : F[215:208] = 3Bh, F[207:200] = 29h

 $a_1$ : F[115:108] = 87h, F[107:100] = 35h



## **CONNECTION DIAGRAM**

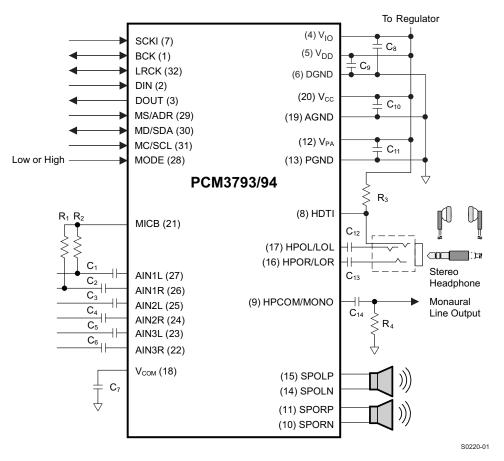
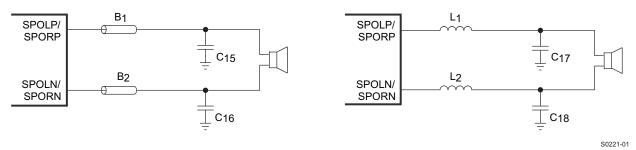


Figure 39. Connection Diagram

**Table 14. Recommended External Parts** 

C <sub>1</sub> –C <sub>6</sub>	1 μF	C <sub>12</sub> , C <sub>13</sub>	10 μF–220 μF
C <sub>7</sub>	1 μF–10 μF <sup>(1)</sup>	C <sub>14</sub>	1 μF–10 μF
C <sub>8</sub>	0.1 μF	R <sub>1</sub> , R <sub>2</sub>	2.2 kΩ
C <sub>9</sub> , C <sub>10</sub>	1 μF–4.7 μF	R <sub>3</sub>	33 kΩ
C <sub>11</sub>	4.7 μF–10 μF	R <sub>4</sub>	10 kΩ

(1)  $10 \mu F$  is recommended to reduce audible pop noise.



NOTE:  $C_{15}$ ,  $C_{16}$  = 1 nF  $C_{17}$ ,  $C_{18}$ : 1  $\mu$ F  $B_1$ ,  $B_2$ : NEC/Tokin N2012ZPS121  $L_1$ ,  $L_2$ : 22 to 33  $\mu$ H

Figure 40. Filter Consideration for Speaker Output

Capless Mode

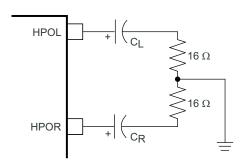


S0222-01

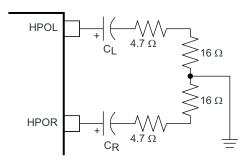
## Conventional Mode

# HDTI HP Jack HPOL HPOR HPOR HPOCM HPCOM HP

Figure 41. Connection for Headphone Output and Insertion Detection



$C_L$ , $C_R - \mu F$	f <sub>C</sub> – Hz
10	995
47	212
100	100
220	45



<b>C</b> <sub>L</sub> , <b>C</b> <sub>R</sub> – μ <b>F</b>	f <sub>C</sub> – Hz
10	770
47	163
100	77
220	35

S0223-01

Figure 42. High-Pass Filter for Headphone Output



23-Feb-2012

#### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
PCM3793RHB	NRND	QFN	RHB	32		TBD	Call TI	Call TI	
PCM3793RHBR	NRND	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
PCM3793RHBRG4	NRND	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
PCM3793RHBT	NRND	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
PCM3793RHBTG4	NRND	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
PCM3794RHBR	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	
PCM3794RHBRG4	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	
PCM3794RHBT	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	
PCM3794RHBTG4	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.



## **PACKAGE OPTION ADDENDUM**

23-Feb-2012

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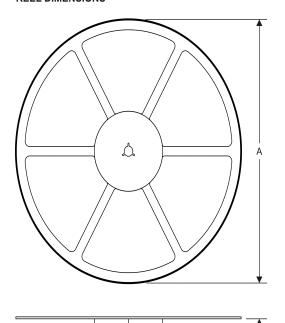
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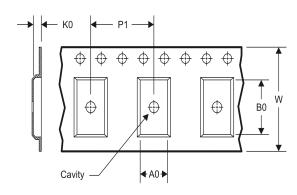
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## TAPE AND REEL INFORMATION

## **REEL DIMENSIONS**



## **TAPE DIMENSIONS**



A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

## TAPE AND REEL INFORMATION

\*All dimensions are nominal

All dimensions are nominal												
Device	_	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM3793RHBR	QFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
PCM3793RHBT	QFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
PCM3794RHBR	QFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
PCM3794RHBT	QFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

www.ti.com 17-Dec-2011



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM3793RHBR	QFN	RHB	32	3000	346.0	346.0	29.0
PCM3793RHBT	QFN	RHB	32	250	210.0	185.0	35.0
PCM3794RHBR	QFN	RHB	32	3000	346.0	346.0	29.0
PCM3794RHBT	QFN	RHB	32	250	210.0	185.0	35.0

# RHB (S-PVQFN-N32)

# PLASTIC QUAD FLATPACK NO-LEAD



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.

- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) Package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO-220.



# RHB (S-PVQFN-N32)

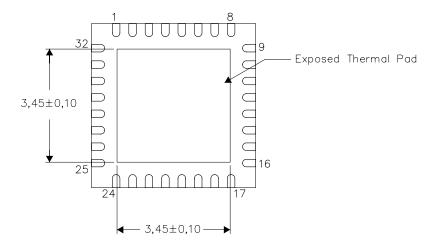
## PLASTIC QUAD FLATPACK NO-LEAD

#### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No—Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

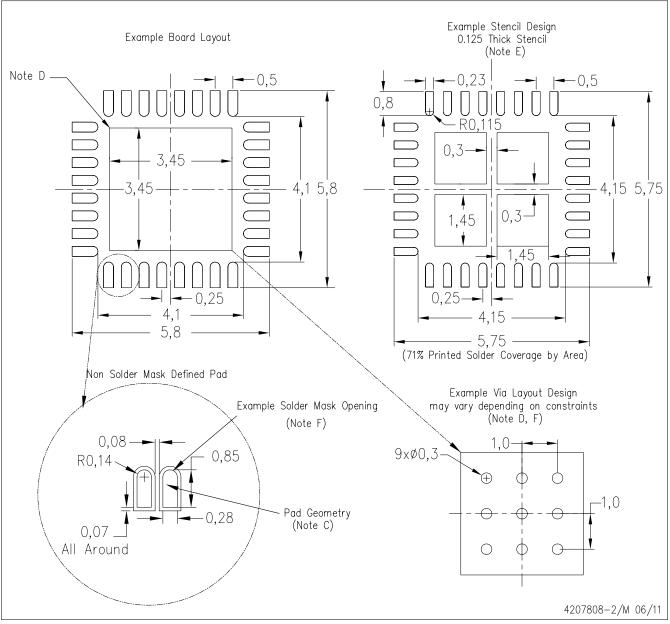
4206356-2/U 06/11

NOTE: A. All linear dimensions are in millimeters



# RHB (S-PVQFN-N32)

# PLASTIC QUAD FLATPACK NO-LEAD



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat—Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <a href="http://www.ti.com">http://www.ti.com</a>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.



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