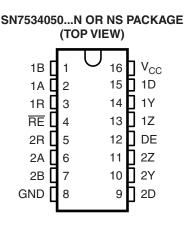


FEATURES

- Meet or Exceed Standards TIA/EIA-422-B and ITU Recommendation V.11
- Operate From Single 5-V Power Supply
- Driver Positive and Negative Current Limiting



- Receiver Input Sensitivity: ±200mV
- Receiver Input Impedance: 12 k Ω Min
- Driver 3-State Outputs
- Receiver 3-State Outputs (SN7534050 Only)

SN7534051...N OR NS PACKAGE (TOP VIEW)

10		10	
1A	2	15	1D
1R	3	14] 1Y
1DE	4	13	1Z
2R	5	12	2DE
2A	6	11	2Z
2B	7	10	2Y
GND	8	9	2D

DESCRIPTION/ORDERING INFORMATION

The SN7534050 and SN7534051 dual differential drivers and receivers are monolithic integrated circuits designed to meet the requirements of ANSI standards TIA/EIA-422-B and ITU Recommendations V.11.

The driver outputs provide limiting for both positive and negative currents and thermal shutdown protection from line fault conditions on transmission bus line.

The SN7534050 combines dual 3-state differential drivers and dual 3-state differential input receivers. The drivers and receivers have active-high and active-low enables, respectively which can be externally connected together to function as direction control. SN7534051 drivers each have an individual active-high enable.

ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
	PDIP – N	Tube of 25	SN7534050N	SN7534050N
	SOP – NS	Reel of 1000	SN7534050NS	SN7534050
–20°C to 85°C	50P - N5	Reel of 2000	SN7534050NSR	SN7534050
-20°C 10 85°C	PDIP – N	Tube of 25	SN7534051N	SN7534051N
	SOP – NS	Reel of 1000	SN7534051NS	SN7534051
	30F - N3	Reel of 2000	SN7534051NSR	SN7534051

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

FUNCTION TABLES

SN7534050, SN7534051 Each Driver⁽¹⁾

INPUT	ENABLE	OUT	PUTS
D	DE	Y	z
Н	Н	Н	L
L	Н	L	Н
Х	L	Z	Z

 (1) H = high level, L = low level, X = irrelevant, Z = high impedance (off)

SN7534050 Each Receiver⁽¹⁾

DIFFERENTIAL INPUTS, A-B	ENABLE RE	OUTPUT R
$V_{ID} \ge 0.2 V$	L	Н
$-0.2 \text{ V} < \text{V}_{\text{ID}} < 0.2 \text{ V}$	L	?
$V_{ID} \leq -0.2 V$	L	L
X	н	Z

(1) H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

SN7534051 Each Receiver⁽¹⁾

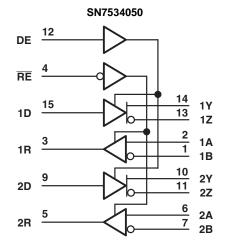
DIFFERENTIAL INPUTS, A–B	OUTPUT R
$V_{ID} \ge 0.2 V$	Н
$-0.2 \text{ V} < \text{V}_{\text{ID}} < 0.2 \text{ V}$?
$V_{ID} \leq -0.2 V$	L

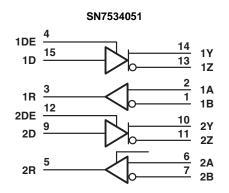
(1) H = high level, L = low level,? = indeterminate

2

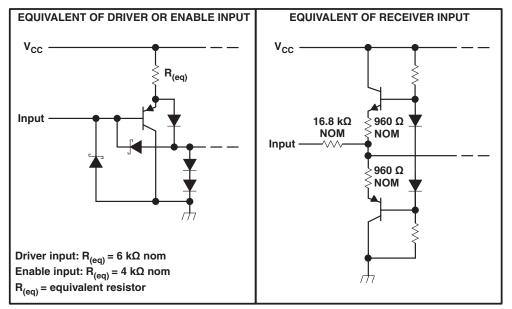


LOGIC DIAGRAMS





SCHEMATIC OF INPUTS

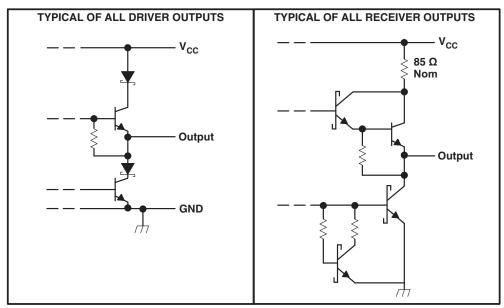


All resistor values are nominal.

SN7534050, SN7534051 **DUAL DIFFERENTIAL DRIVERS AND RECEIVERS** SLLS833-MAY 2007



SCHEMATIC OF OUTPUTS



All resistor values are nominal.

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage ⁽²⁾			7	V
VI	Input voltage	DE, RE, D inputs		7	V
Vi	Receiver input voltage	A or B inputs		±25	V
V _{ID}	Receiver differential output voltage ⁽³⁾			±25	V
Vo	Driver output voltage range		-10	15	V
I _{OL}	Receiver low-level output current			50	mA
0	Deckage thermal impedance ⁽⁴⁾	N package		66	°C/W
θ_{JA}	Package thermal impedance ⁽⁴⁾	NS package		68	°C/w
	Operating free-air temperature range		-20	85	°C
T _{stg}	Storage temperature range		-65	150	°C
	Lead temperature, 1.6 mm (1/16 in) from	case for 10 s		260	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages, except differential input voltage, are with respect to the network GND.

(3) Differential input voltage is measured at the noninverting terminal, with respect to the inverting terminal.

(4) The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

SLLS833-MAY 2007

Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage		4.75	5		V5.25
V _{IH}	High-level input voltage	DE, RE, D	2			V
VIL	Low-level input voltage	DE, RE, D			0.8	V
V _{IC}	Common-mode input voltage ⁽¹⁾	Receiver			±7	V
V_{ID}	Differential input voltage	Receiver			±12	V
	Llich lovel output ourrest	Driver			40	mA
IOH	High-level output current	Receiver			-400	μA
		Driver			-40	~ ^
IOL	Low-level output current	Receiver			16	mA
T _A	Operating free-air temperature	· · ·	-20		85	°C

(1) Refer to TIA/EIA-422-B for exact conditions.

DRIVER SECTION

Electrical Characteristics

over recommended supply voltage and operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST	CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}	High-level output voltage	$V_{IH} = 2 V, V_{IL} = 0.$	8 V, I _{OH} = –20 mA		3.7		V
V _{OL}	Low-level output voltage	$V_{IH} = 2 V, V_{IL} = 0.$	8 V, I _{OL} = 20 mA		1.1		V
V _{OD1}	Differential output voltage	$I_0 = 0 \text{ mA}$		1.5		6	V
V _{OD2}	Differential output voltage ⁽²⁾	R _L = 100 Ω,	See Figure 1	2			V
ΔV_{OD}	Change in magnitude of differential output voltage ⁽²⁾	R _L = 100 Ω,	See Figure 1			±0.4	V
V _{OC}	Common-mode output voltage ⁽²⁾	R _L = 100 Ω,	See Figure 1			±3	V
ΔV_{OC}	Change in magnitude of differential common-mode voltage ⁽²⁾	R _L = 100 Ω,	See Figure 1			±0.4	V
	\mathbf{O} the formula $\mathbf{U}^{(2)}$	N/ 0.1/	V _O = 6 V			100	•
l _{off}	Output current with power off ⁽²⁾	$V_{CC} = 0 V$	V _O = -0.25 V			-100	μA
I _{OZ}	High-impedance-state output current	$V_{\rm O} = -0.25$ V to 6	V			±100	μA
I _{IH}	High-level input current	V _I = 2.7 V				20	μΑ
I _{IL}	Low-level input current	V ₁ = 0.4 V				-100	μΑ
I _{OS}	Short-circuit output current ⁽²⁾⁽³⁾	$V_{O} = V_{CC}$ or GND		-30		-150	mA
	Supply current (total package)	Nolood	Output enabled		80	110	~ ^
I _{CC}		No load	Output disabled		50	80	mA

All typical values are at V_{CC} = 5 V and T_A = 25°C.
Refer to TIA-EIA-422-B for exact conditions.
Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

SN7534050, SN7534051 DUAL DIFFERENTIAL DRIVERS AND RECEIVERS

SLLS833-MAY 2007

Switching Characteristics

 V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{d(OD)}	Differential output delay time	$R_L = 100 \Omega$, $C_L = 50 pF$, See Figure 3		20	25	ns
t _{t(OD)}	Differential output transition time	$R_L = 100 \Omega$, $C_L = 50 pF$, See Figure 3		27	35	ns
t _{PLH}	Propagation delay time, low- to high-level output	$R_L = 27 \Omega$, See Figure 4		20	25	ns
t _{PHL}	Propagation delay time, high- to low-level output	$R_L = 27 \Omega$, See Figure 4		20	25	ns
t _{PZH}	Output enable time to high level	$R_L = 110 \Omega$, See Figure 5		80	120	ns
t _{PZL}	Output enable time to low level	$R_L = 110 \Omega$, See Figure 6		40	60	ns
t _{PHZ}	Output disable time from high level	$R_L = 110 \Omega$, See Figure 5		90	120	ns
t _{PLZ}	Output disable time from low level	$R_L = 110 \Omega$, See Figure 6		30	45	ns

RECEIVER SECTION

Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST COND	ITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{IT+}	Positive-going input threshold voltage, diff					0.2	V	
V _{IT-}	Negative-going input threshold voltage, dil input	fferential			-0.2 ⁽²⁾			V
V _{hys}	Input hysteresis (V _{IT+} – V _{IT} –)					50		mV
V _{IK}	Input clamp voltage, RE	SN7534050	I _I = -18 mA				-1.5	V
V _{OH}			$V_{ID} = 200 \text{ mV},$ $I_{OH} = -400 \mu\text{A},$	See Figure 2	2.7			V
V		$V_{ID} = -200 \text{ mV},$ $I_{OL} = -200 \text{ mV},$	I _{OL} = 8 mA			0.45	V	
V _{OL}	Low-level output voltage		See Figure 2 I _{OL} = 16 mA				0.5	v
I _{OZ}	High-impedance-state output current	SN7534050	$V_{O} = 0.4 \text{ V}$ to 2.4 V				±20	μA
	Line input current		Other input at 0 V	$V_{I} = 10 V$			1.5	mA
II.				$V_{I} = -10 V$			-2.5	ША
I _{IH}	High-level enable input current, RE	SN7534050	V _{IH} = 2.7 V				20	μΑ
I	I _{IL} Low-level enable input current, RE SN7534050		V _{IL} = 0.4 V				-100	μΑ
r _l	Input resistance				12			kΩ
I _{OS}	I _{OS} Short circuit output current				-15		-85	mA
I _{CC}	Supply current (total package)		No load, enabled			80	110	mA

(1) All typical values are at $V_{CC} = 5$ V and $T_A = 25^{\circ}C$. (2) The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels.

Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
t _{PLH}			$V_{ID} = 1.5 V, C_{L} = 15 pF,$ See Figure 7		20	35	ns
		$V_{ID} = 1.5 V, C_L = 15 pF,$ See Figure 7		22	35	ns	
t _{PZH}	Output enable time to high level	SN7534050	$C_L = 15 \text{ pF}$, see Figure 8		17	25	ns
t _{PZL}	Output enable time to low level	SN7534050	C _L = 15 pF, See Figure 8		20	27	ns
t _{PHZ}	Output disable time from high level	SN7534050	C _L = 15 pF, See Figure 8		25	40	ns
t _{PLZ}	Output disable time from low level	SN7534050	C _L = 15 pF, See Figure 8		30	40	ns

PARAMETER MEASUREMENT INFORMATION

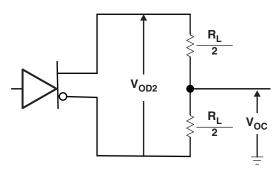


Figure 1. Driver Test Circuit, V_{OD} and V_{OC}

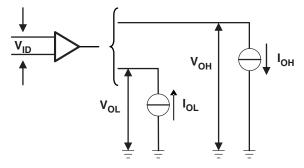
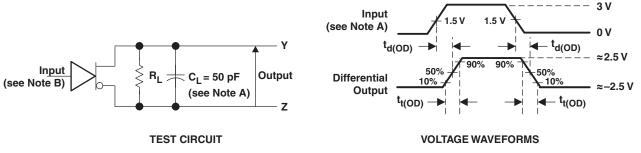


Figure 2. Receiver Test Circuit, $V_{\rm OH}$ and $V_{\rm OL}$



A. C_L includes probe and jig capacitance.

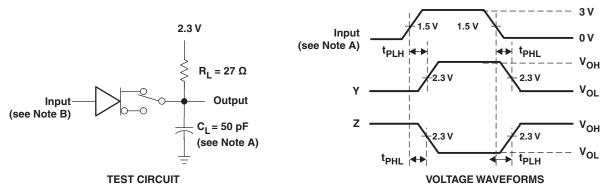
B. The pulse generator has the following characteristics: PRR \leq 1 MHz, duty cycle = 50%, t_r = t_r \leq 6 ns.

Figure 3. Driver Test Circuit and Voltage Waveforms, $t_{d(\text{OD})}$ and $t_{t(\text{OD})}$

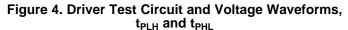
SN7534050, SN7534051 **DUAL DIFFERENTIAL DRIVERS AND RECEIVERS**

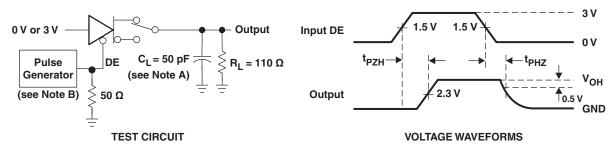
SLLS833-MAY 2007

PARAMETER MEASUREMENT INFORMATION (continued)



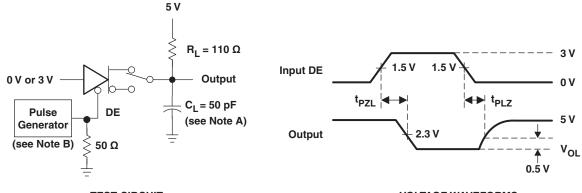
- C₁ includes probe and jig capacitance. Α.
- The pulse generator has the following characteristics: PRR \leq 1 MHz, duty cycle = 50%, t_r = t_r \leq 6 ns. Β.





- Α. C₁ includes probe and jig capacitance.
- The pulse generator has the following characteristics: PRR \leq 1 MHz, duty cycle = 50%, t_r = t_r \leq 6 ns. Β.

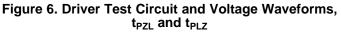
Figure 5. Driver Test Circuit and Voltage Waveforms, t_{PZH} and t_{PHZ}



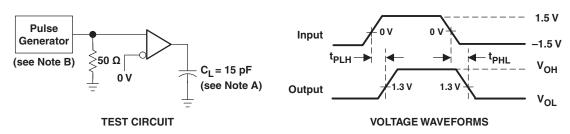
TEST CIRCUIT

VOLTAGE WAVEFORMS

- C_L includes probe and jig capacitance. Α.
- The pulse generator has the following characteristics: PRR \leq 1 MHz, duty cycle = 50%, t_r = t_r \leq 6 ns. В.



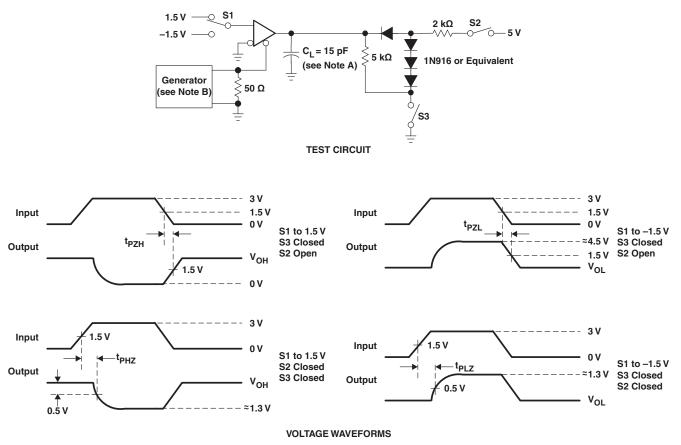
PARAMETER MEASUREMENT INFORMATION (continued)



A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR \leq 1 MHz, duty cycle = 50%, t_r = t_r \leq 6 ns.

Figure 7. Receiver Test Circuit and Voltage Waveforms, t_{PLH} and t_{PHL}



A. C₁ includes probe and jig capacitance.

B. The pulse generator has the following characteristics: $PRR \le 1$ MHz, duty cycle = 50%, $t_r = t_r \le 6$ ns.

Figure 8. Receiver Test Circuit and Voltage Waveforms, t_{PZH}, t_{PZL}, t_{PHZ}, t_{PLZ} (SN7534050)

V IEXAS NSTRUMENTS www.ti.com

4-Jun-2007

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN7534050N	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN7534050NE4	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN7534050NS	ACTIVE	SO	NS	16	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN7534050NSE4	ACTIVE	SO	NS	16	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN7534050NSG4	ACTIVE	SO	NS	16	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN7534050NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN7534050NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN7534050NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN7534051N	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN7534051NE4	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN7534051NS	ACTIVE	SO	NS	16	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN7534051NSE4	ACTIVE	SO	NS	16	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN7534051NSG4	ACTIVE	SO	NS	16	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN7534051NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN7534051NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN7534051NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

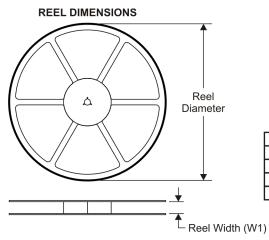


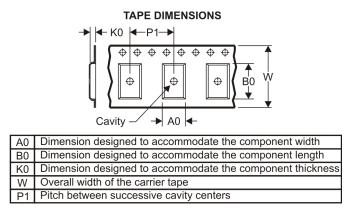
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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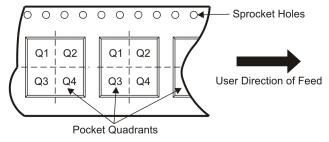
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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dim	nensions are nominal												
	Device		Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
S	N7534050NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
S	N7534051NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1



PACKAGE MATERIALS INFORMATION

11-Mar-2008



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN7534050NSR	SO	NS	16	2000	346.0	346.0	33.0
SN7534051NSR	SO	NS	16	2000	346.0	346.0	33.0

MECHANICAL DATA

PLASTIC SMALL-OUTLINE PACKAGE

0,51 0,35 ⊕0,25⊛ 1,27 8 14 0,15 NOM 5,60 8,20 5,00 7,40 \bigcirc Gage Plane ₽ 0,25 7 1 1,05 0,55 0°-10° Δ 0,15 0,05 Seating Plane — 2,00 MAX 0,10PINS ** 14 16 20 24 DIM 10,50 10,50 12,90 15,30 A MAX A MIN 9,90 9,90 12,30 14,70 4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.

NS (R-PDSO-G**)

14-PINS SHOWN

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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