

# TP3064, TP3067

*Enhanced Serial Interface CMOS CODEC/Filter COMBO*



Literature Number: SNAS570

# TP3064, TP3067 "Enhanced" Serial Interface CMOS CODEC/Filter COMBO®

## General Description

The TP3064 ( $\mu$ -law) and TP3067 (A-law) are monolithic PCM CODEC/Filters utilizing the A/D and D/A conversion architecture shown in *Figure 1*, and a serial PCM interface. The devices are fabricated using National's advanced double-poly CMOS process (microCMOS).

Similar to the TP305X family, these devices feature an additional Receive Power Amplifier to provide push-pull balanced output drive capability. The receive gain can be adjusted by means of two external resistors for an output level of up to  $\pm 6.6V$  across a balanced  $600\Omega$  load.

Also included is an Analog Loopback switch and a  $\overline{TSx}$  output.

See also AN-370, "Techniques for Designing with CODEC/Filter COMBO Circuits."

## Features

- Complete CODEC and filtering system including:
  - Transmit high-pass and low-pass filtering
  - Receive low-pass filter with  $\sin x/x$  correction
  - Active RC noise filters
  - $\mu$ -law or A-law compatible COder and DECoder
  - Internal precision voltage reference
  - Serial I/O interface
  - Internal auto-zero circuitry
  - Receive push-pull power amplifiers
- $\mu$ -law—TP3064
- A-law—TP3067
- Designed for D3/D4 and CCITT applications
- $\pm 5V$  operation
- Low operating power—typically 70 mW
- Power-down standby mode—typically 3 mW
- Automatic power-down
- TTL or CMOS compatible digital interfaces
- Maximizes line interface card circuit density

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## Block Diagram

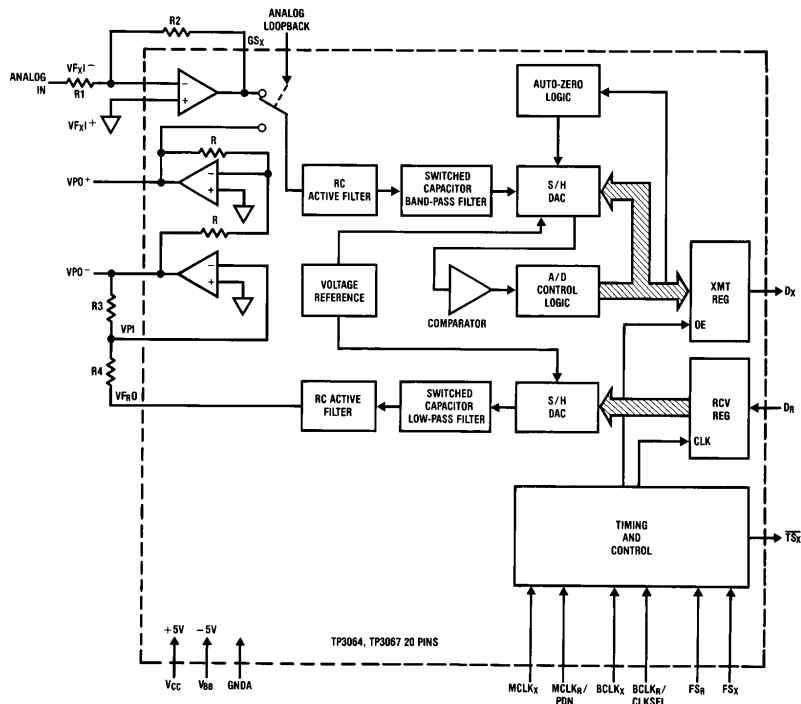
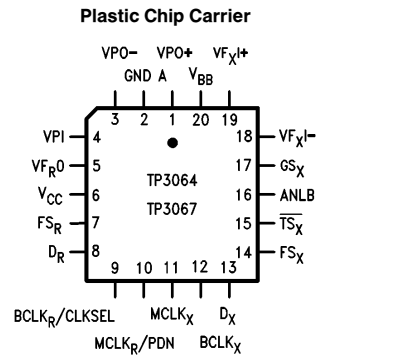
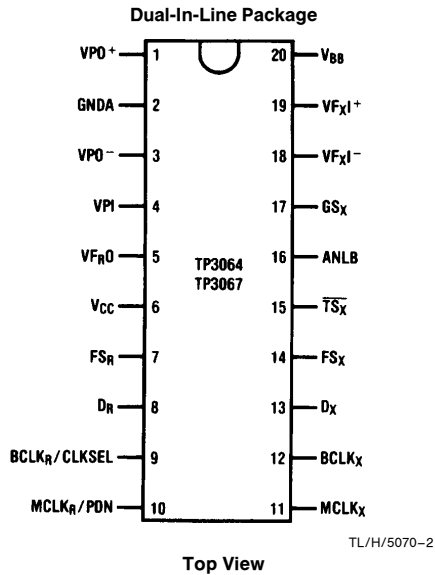


FIGURE 1

TL/H/5070-1

TP3064, TP3067 "Enhanced" Serial Interface CMOS CODEC/Filter COMBO

## Connection Diagrams



Order Number TP3064J or TP3067J  
See NS Package J20A

Order Number TP3064WM or TP3067WM  
See NS Package M20B

Order Number TP3064N or TP3067N  
See NS Package N20A

Order Number TP3064V or TP3067V  
See NS Package V20A

## Pin Description

Symbol	Function	Symbol	Function
VPO <sup>+</sup>	The non-inverted output of the receive power amplifier.	MCLK <sub>x</sub>	Transmit master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with MCLK <sub>R</sub> . Best performance is realized from synchronous operation.
GNDA	Analog ground. All signals are referenced to this pin.	BCLK <sub>x</sub>	The bit clock which shifts out the PCM data on D <sub>x</sub> . May vary from 64 kHz to 2.048 MHz, but must be synchronous with MCLK <sub>x</sub> .
VPO <sup>-</sup>	The inverted output of the receive power amplifier.	D <sub>x</sub>	The TRI-STATE <sup>®</sup> PCM data output which is enabled by FS <sub>x</sub> .
VPI	Inverting input to the receive power amplifier.	FS <sub>x</sub>	Transmit frame sync pulse input which enables BCLK <sub>x</sub> to shift out the PCM data on D <sub>x</sub> . FS <sub>x</sub> is an 8 kHz pulse train, see Figures 2 and 3 for timing details.
VFR0	Analog output of the receive filter.	TS <sub>x</sub>	Open drain output which pulses low during the encoder time slot.
VCC	Positive power supply pin. V <sub>CC</sub> = +5V ± 5%.	ANLB	Analog Loopback control input. Must be set to logic '0' for normal operation. When pulled to logic '1', the transmit filter input is disconnected from the output of the transmit preamplifier and connected to the VPO <sup>+</sup> output of the receive power amplifier.
FSR	Receive frame sync pulse which enables BCLK <sub>R</sub> to shift PCM data into D <sub>R</sub> . FSR is an 8 kHz pulse train. See Figures 2 and 3 for timing details.	GS <sub>x</sub>	Analog output of the transmit input amplifier. Used to externally set gain.
DR	Receive data input. PCM data is shifted into D <sub>R</sub> following the FSR leading edge.	VFxI <sup>-</sup>	Inverting input of the transmit input amplifier.
BCLK <sub>R</sub> /CLKSEL	The bit clock which shifts data into D <sub>R</sub> after the FSR leading edge. May vary from 64 kHz to 2.048 MHz. Alternatively, may be a logic input which selects either 1.536 MHz/1.544 MHz or 2.048 MHz for master clock in synchronous mode and BCLK <sub>x</sub> is used for both transmit and receive directions (see Table I).	VFxI <sup>+</sup>	Non-inverting input of the transmit input amplifier.
MCLK <sub>R</sub> /PDN	Receive master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with MCLK <sub>x</sub> , but should be synchronous with MCLK <sub>x</sub> for best performance. When MCLK <sub>R</sub> is connected continuously low, MCLK <sub>x</sub> is selected for all internal timing. When MCLK <sub>R</sub> is connected continuously high, the device is powered down.	VBB	Negative power supply pin. V <sub>BB</sub> = -5V ± 5%.

## Functional Description

### POWER-UP

When power is first applied, power-on reset circuitry initializes the COMBO™ and places it into a power-down state. All non-essential circuits are deactivated and the  $D_X$ ,  $V_{FO}$ ,  $V_{PO-}$  and  $V_{PO+}$  outputs are put in high impedance states. To power-up the device, a logical low level or clock must be applied to the  $MCLK_R$ /PDN pin and  $FS_X$  and/or  $FS_R$  pulses must be present. Thus, 2 power-down control modes are available. The first is to pull the  $MCLK_R$ /PDN pin high; the alternative is to hold both  $FS_X$  and  $FS_R$  inputs continuously low—the device will power-down approximately 2 ms after the last  $FS_X$  or  $FS_R$  pulse. Power-up will occur on the first  $FS_X$  or  $FS_R$  pulse. The TRI-STATE PCM data output,  $D_X$ , will remain in the high impedance state until the second  $FS_X$  pulse.

### SYNCHRONOUS OPERATION

For synchronous operation, the same master clock and bit clock should be used for both the transmit and receive directions. In this mode, a clock must be applied to  $MCLK_X$  and the  $MCLK_R$ /PDN pin can be used as a power-down control. A low level on  $MCLK_R$ /PDN powers up the device and a high level powers down the device. In either case,  $MCLK_X$  will be selected as the master clock for both the transmit and receive circuits. A bit clock must also be applied to  $BCLK_X$  and the  $BCLK_R$ /CLKSEL can be used to select the proper internal divider for a master clock of 1.536 MHz, 1.544 MHz or 2.048 MHz. For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame.

With a fixed level on the  $BCLK_R$ /CLKSEL pin,  $BCLK_X$  will be selected as the bit clock for both the transmit and receive directions. Table I indicates the frequencies of operation which can be selected, depending on the state of  $BCLK_R$ /CLKSEL. In this synchronous mode, the bit clock,  $BCLK_X$ , may be from 64 kHz to 2.048 MHz, but must be synchronous with  $MCLK_X$ .

Each  $FS_X$  pulse begins the encoding cycle and the PCM data from the previous encode cycle is shifted out of the enabled  $D_X$  output on the positive edge of  $BCLK_X$ . After 8 bit clock periods, the TRI-STATE  $D_X$  output is returned to a high impedance state. With an  $FS_R$  pulse, PCM data is latched via the  $D_R$  input on the negative edge of  $BCLK_X$  (or  $BCLK_R$  if running).  $FS_X$  and  $FS_R$  must be synchronous with  $MCLK_X/R$ .

TABLE I. Selection of Master Clock Frequencies

BCLK <sub>R</sub> /CLKSEL	Master Clock Frequency Selected	
	TP3067	TP3064
Clocked	2.048 MHz	1.536 MHz or 1.544 MHz
0	1.536 MHz or 1.544 MHz	2.048 MHz
1	2.048 MHz	1.536 MHz or 1.544 MHz

### ASYNCHRONOUS OPERATION

For asynchronous operation, separate transmit and receive clocks may be applied.  $MCLK_X$  and  $MCLK_R$  must be 2.048 MHz for the TP3067, or 1.536 MHz, 1.544 MHz for the TP3064, and need not be synchronous. For best transmis-

sion performance, however,  $MCLK_R$  should be synchronous with  $MCLK_X$ , which is easily achieved by applying only static logic levels to the  $MCLK_R$ /PDN pin. This will automatically connect  $MCLK_X$  to all internal  $MCLK_R$  functions (see Pin Description). For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame.  $FS_X$  starts each encoding cycle and must be synchronous with  $MCLK_X$  and  $BCLK_X$ .  $FS_R$  starts each decoding cycle and must be synchronous with  $BCLK_R$ .  $BCLK_R$  must be a clock, the logic levels shown in Table I are not valid in asynchronous mode.  $BCLK_X$  and  $BCLK_R$  may operate from 64 kHz to 2.048 MHz.

### SHORT FRAME SYNC OPERATION

The COMBO can utilize either a short frame sync pulse (the same as the TP3020/21 CODECs) or a long frame sync pulse. Upon power initialization, the device assumes a short frame mode. In this mode, both frame sync pulses,  $FS_X$  and  $FS_R$ , must be one bit clock period long, with timing relationships specified in Figure 2. With  $FS_X$  high during a falling edge of  $BCLK_X$ , the next rising edge of  $BCLK_X$  enables the  $D_X$  TRI-STATE output buffer, which will output the sign bit. The following seven rising edges clock out the remaining seven bits, and the next falling edge disables the  $D_X$  output. With  $FS_R$  high during a falling edge of  $BCLK_R$  ( $BCLK_X$  in synchronous mode), the next falling edge of  $BCLK_R$  latches in the sign bit. The following seven falling edges latch in the seven remaining bits. All devices may utilize the short frame sync pulse in synchronous or asynchronous operating mode.

### LONG FRAME SYNC OPERATION

To use the long (TP5116A/56 CODECs) frame mode, both the frame sync pulses,  $FS_X$  and  $FS_R$ , must be three or more bit clock periods long, with timing relationships specified in Figure 3. Based on the transmit frame sync,  $FS_X$ , the COMBO will sense whether short or long frame sync pulses are being used. For 64 kHz operation, the frame sync pulse must be kept low for a minimum of 160 ns. The  $D_X$  TRI-STATE output buffer is enabled with the rising edge of  $FS_X$  or the rising edge of  $BCLK_X$ , whichever comes later, and the first bit clocked out is the sign bit. The following seven  $BCLK_X$  rising edges clock out the remaining seven bits. The  $D_X$  output is disabled by the falling  $BCLK_X$  edge following the eighth rising edge, or by  $FS_X$  going low, whichever comes later. A rising edge on the receive frame sync pulse,  $FS_R$ , will cause the PCM data at  $D_R$  to be latched in on the next eight falling edges of  $BCLK_R$  ( $BCLK_X$  in synchronous mode). All devices may utilize the long frame sync pulse in synchronous or asynchronous mode.

### TRANSMIT SECTION

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors, see Figure 4. The low noise and wide bandwidth allow gains in excess of 20 dB across the audio passband to be realized. The op amp drives a unity-gain filter consisting of RC active pre-filter, followed by an eighth order switched-capacitor bandpass filter clocked at 256 kHz. The output of this filter directly drives the encoder sample-and-hold circuit. The A/D is of companding type according to  $\mu$ -law (TP3064) or A-law (TP3067) coding conventions. A precision voltage reference is trimmed in manufacturing to provide an input overload ( $t_{MAX}$ ) of nominally 2.5V peak (see

## Functional Description (Continued)

table of Transmission Characteristics). The  $FS_X$  frame sync pulse controls the sampling of the filter output, and then the successive-approximation encoding cycle begins. The 8-bit code is then loaded into a buffer and shifted out through  $D_X$  at the next  $FS_X$  pulse. The total encoding delay will be approximately  $165 \mu s$  (due to the transmit filter) plus  $125 \mu s$  (due to encoding delay), which totals  $290 \mu s$ . Any offset voltage due to the filters or comparator is cancelled by sign bit integration.

### RECEIVE SECTION

The receive section consists of an expanding DAC which drives a fifth order switched-capacitor low pass filter clocked at 256 kHz. The decoder is A-law (TP3067) or  $\mu$ -law (TP3064) and the 5th order low pass filter corrects for the  $\sin x/x$  attenuation due to the 8 kHz sample/hold. The filter is then followed by a 2nd order RC active post-filter with its output at  $VF_{RO}$ . The receive section is unity-gain, but gain can be added by using the power amplifiers. Upon the occurrence of  $FS_R$ , the data at the  $D_R$  input is clocked in on the falling edge of the next eight  $BCLK_R$  ( $BCLK_X$ ) peri-

ods. At the end of the decoder time slot, the decoding cycle begins, and  $10 \mu s$  later the decoder DAC output is updated. The total decoder delay is  $\sim 10 \mu s$  (decoder update) plus  $110 \mu s$  (filter delay) plus  $62.5 \mu s$  ( $1/2$  frame), which gives approximately  $180 \mu s$ .

### RECEIVE POWER AMPLIFIERS

Two inverting mode power amplifiers are provided for directly driving a matched line interface transformer. The gain of the first power amplifier can be adjusted to boost the  $\pm 2.5V$  peak output signal from the receive filter up to  $\pm 3.3V$  peak into an unbalanced  $300\Omega$  load, or  $\pm 4.0V$  into an unbalanced  $15 k\Omega$  load. The second power amplifier is internally connected in unity-gain inverting mode to give 6 dB of signal gain for balanced loads.

Maximum power transfer to a  $600\Omega$  subscriber line termination is obtained by differentially driving a balanced transformer with a  $\sqrt{2}:1$  turns ratio, as shown in *Figure 4*. A total peak power of 15.6 dBm can be delivered to the load plus termination.

### ENCODING FORMAT AT $D_X$ OUTPUT

	TP3064 $\mu$ -Law								TP3067 A-Law (Includes Even Bit Inversion)							
$V_{IN} = +\text{Full-Scale}$	1	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0
$V_{IN} = 0V$	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1
	0	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1
$V_{IN} = -\text{Full-Scale}$	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0

## Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

$V_{CC}$ to GNDA	7V
$V_{BB}$ to GNDA	-7V
Voltage at any Analog Input or Output	$V_{CC} + 0.3V$ to $V_{BB} - 0.3V$

Voltage at any Digital Input or Output	$V_{CC} + 0.3V$ to $GNDA - 0.3V$
Operating Temperature Range	-25°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temp. (Soldering, 10 sec.)	300°C
ESD (Human Body Model) J	1000V
ESD (Human Body Model) N	1500V
Latch-Up Immunity	100 mA on Any Pin

**Electrical Characteristics** Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for  $V_{CC} = +5.0V \pm 5\%$ ,  $V_{BB} = -5.0V \pm 5\%$ ;  $T_A = 0^\circ C$  to  $70^\circ C$  by correlation with 100% electrical testing at  $T_A = 25^\circ C$ . All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GNDA. Typical values specified at  $V_{CC} = +5.0V$ ,  $V_{BB} = -5.0V$ ,  $T_A = 25^\circ C$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>POWER DISSIPATION (ALL DEVICES)</b>						
$I_{CC0}$	Power-Down Current	(Note)		0.5	<b>1.5</b>	mA
$I_{BB0}$	Power-Down Current	(Note)		0.05	<b>0.3</b>	mA
$I_{CC1}$	Active Current	$V_{PI} = 0V$ ; $V_{FRO}$ , $V_{PO}^+$ and $V_{PO}^-$ unloaded		7.0	<b>10.0</b>	mA
$I_{BB1}$	Active Current	$V_{PI} = 0V$ ; $V_{FRO}$ , $V_{PO}^+$ and $V_{PO}^-$ unloaded		7.0	<b>10.0</b>	mA
<b>DIGITAL INTERFACE</b>						
$V_{IL}$	Input Low Voltage				<b>0.6</b>	V
$V_{IH}$	Input High Voltage		<b>2.2</b>			V
$V_{OL}$	Output Low Voltage	$D_X$ , $I_L = 3.2$ mA			<b>0.4</b>	V
		$\overline{TS}_X$ , $I_L = 3.2$ mA, Open Drain			<b>0.4</b>	V
$V_{OH}$	Output High Voltage	$D_X$ , $I_H = -3.2$ mA	<b>2.4</b>			V
$I_{IL}$	Input Low Current	$GNDA \leq V_{IN} \leq V_{IL}$ , All Digital Inputs	<b>-10</b>		<b>10</b>	$\mu A$
$I_{IH}$	Input High Current	$V_{IH} \leq V_{IN} \leq V_{CC}$	<b>-10</b>		<b>10</b>	$\mu A$
$I_{OZ}$	Output Current in High Impedance State (TRI-STATE)	$D_X$ , $GNDA \leq V_O \leq V_{CC}$	<b>-10</b>		<b>10</b>	$\mu A$

Note:  $I_{CC0}$  and  $I_{BB0}$  are measured after first achieving a power-up state.

## Electrical Characteristics (Continued)

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for  $V_{CC} = +5.0V \pm 5\%$ ,  $V_{BB} = -5.0V \pm 5\%$ ;  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$  by correlation with 100% electrical testing at  $T_A = 25^\circ\text{C}$ . All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GNDA. Typical values specified at  $V_{CC} = +5.0V$ ,  $V_{BB} = -5.0V$ ,  $T_A = 25^\circ\text{C}$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>ANALOG INTERFACE WITH TRANSMIT INPUT AMPLIFIER (ALL DEVICES)</b>						
$I_{IXA}$	Input Leakage Current	$-2.5V \leq V \leq +2.5V$ , $V_{FXL}^+$ or $V_{FXL}^-$	<b>-200</b>		<b>200</b>	nA
$R_{IXA}$	Input Resistance	$-2.5V \leq V \leq +2.5V$ , $V_{FXL}^+$ or $V_{FXL}^-$	10			M $\Omega$
$R_{OXA}$	Output Resistance	Closed Loop, Unity Gain		1	3	$\Omega$
$R_{LXA}$	Load Resistance	$GS_X$	10			k $\Omega$
$C_{LXA}$	Load Capacitance	$GS_X$			50	pF
$V_{OXA}$	Output Dynamic Range	$GS_X$ , $R_L \geq 10$ k $\Omega$	<b>-2.8</b>		<b>+2.8</b>	V
$A_{VXA}$	Voltage Gain	$V_{FXL}^+$ to $GS_X$	<b>5000</b>			V/V
$F_{UXA}$	Unity-Gain Bandwidth		1	2		MHz
$V_{OSXA}$	Offset Voltage		<b>-20</b>		<b>20</b>	mV
$V_{CMXA}$	Common-Mode Voltage	CMRRXA > 60 dB	<b>-2.5</b>		<b>2.5</b>	V
CMRRXA	Common-Mode Rejection Ratio	DC Test	<b>60</b>			dB
PSRRXA	Power Supply Rejection Ratio	DC Test	<b>60</b>			dB
<b>ANALOG INTERFACE WITH RECEIVE FILTER (ALL DEVICES)</b>						
$R_{ORF}$	Output Resistance	Pin $V_{FR0}$		1	3	$\Omega$
$R_{LRF}$	Load Resistance	$V_{FR0} = \pm 2.5V$	10			k $\Omega$
$C_{LRF}$	Load Capacitance	Connect from $V_{FR0}$ to GNDA			25	pF
$V_{OSR0}$	Output DC Offset Voltage	Measure from $V_{FR0}$ to GNDA	<b>-200</b>		<b>200</b>	mV
<b>ANALOG INTERFACE WITH POWER AMPLIFIERS (ALL DEVICES)</b>						
$I_{PI}$	Input Leakage Current	$-1.0V \leq V_{PI} \leq 1.0V$	<b>-100</b>		<b>100</b>	nA
$R_{PI}$	Input Resistance	$-1.0V \leq V_{PI} \leq 1.0V$	10			M $\Omega$
$V_{IOS}$	Input Offset Voltage		<b>-25</b>		<b>25</b>	mV
$R_{OP}$	Output Resistance	Inverting Unity-Gain at $V_{PO}^+$ or $V_{PO}^-$		1		$\Omega$
$F_C$	Unity-Gain Bandwidth	Open Loop ( $V_{PO}^-$ )		400		kHz
$C_{LP}$	Load Capacitance				100	pF
$GA_{P^+}$	Gain from $V_{PO}^-$ to $V_{PO}^+$	$R_L = 600\Omega$ $V_{PO}^+$ to $V_{PO}^-$ Level at $V_{PO}^- = 1.77$ Vrms		-1		V/V
PSRR <sub>P</sub>	Power Supply Rejection of $V_{CC}$ or $V_{BB}$	$V_{PO}^-$ Connected to $V_{PI}$ 0 kHz – 4 kHz	60			dB
		4 kHz – 50 kHz	36			dB
$R_{LP}$	Load Resistance	Connect from $V_{PO}^+$ to $V_{PO}^-$	600			$\Omega$

## Timing Specifications

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for  $V_{CC} = +5.0V \pm 5\%$ ,  $V_{BB} = -5.0V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$  by correlation with 100% electrical testing at  $T_A = 25^\circ C$ . All other limits are assured by correlation with other production tests and/or product design and characterization. All signals are referenced to GND. Typical values specified at  $V_{CC} = +5.0V$ ,  $V_{BB} = -5.0V$ ,  $T_A = 25^\circ C$ . All timing parameters are measured at  $V_{OH} = 2.0V$  and  $V_{OL} = 0.7V$ .

See Definitions and Timing Conventions section for test methods information.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$1/t_{PM}$	Frequency of Master Clock	MCLK <sub>X</sub> and MCLK <sub>R</sub>		1.536 1.544 <b>2.048</b>		MHz MHz MHz
$t_{RM}$	Rise Time of Master Clock	MCLK <sub>X</sub> and MCLK <sub>R</sub>			50	ns
$t_{FM}$	Fall Time of Master Clock	MCLK <sub>X</sub> and MCLK <sub>R</sub>			50	ns
$t_{PB}$	Period Bit of Clock		485	<b>488</b>	15725	ns
$t_{RB}$	Rise Time of Bit Clock	BCLK <sub>X</sub> and BCLK <sub>R</sub>			50	ns
$t_{FB}$	Fall Time of Bit Clock	BCLK <sub>X</sub> and BCLK <sub>R</sub>			50	ns
$t_{WMH}$	Width of Master Clock High	MCLK <sub>X</sub> and MCLK <sub>R</sub>	<b>160</b>			ns
$t_{WML}$	Width of Master Clock Low	MCLK <sub>X</sub> and MCLK <sub>R</sub>	<b>160</b>			ns
$t_{SBFM}$	Set-Up Time from BCLK <sub>X</sub> High to MCLK <sub>X</sub> Falling Edge		<b>100</b>			ns
$t_{SFFM}$	Set-Up Time from FS <sub>X</sub> High to MCLK <sub>X</sub> Falling Edge	Long Frame Only	<b>100</b>			ns
$t_{WBH}$	Width of Bit Clock High		<b>160</b>			ns
$t_{WBL}$	Width of Bit Clock Low		<b>160</b>			ns
$t_{HBFL}$	Holding Time from Bit Clock Low to Frame Sync	Long Frame Only	<b>0</b>			ns
$t_{HBFS}$	Holding Time from Bit Clock High to Frame Sync	Short Frame Only	<b>0</b>			ns
$t_{SFB}$	Set-Up Time for Frame Sync to Bit Clock Low	Long Frame Only	<b>80</b>			ns
$t_{DBD}$	Delay Time from BCLK <sub>X</sub> High to Data Valid	Load = 150 pF plus 2 LSTTL Loads	0		180	ns
$t_{DBTS}$	Delay Time to $\overline{TS}_X$ Low	Load = 150 pF plus 2 LSTTL Loads			140	ns
$t_{DZC}$	Delay Time from BCLK <sub>X</sub> Low to Data Output Disabled		50		165	ns
$t_{DZF}$	Delay Time to Valid Data from FS <sub>X</sub> or BCLK <sub>X</sub> , Whichever Comes Later	$C_L = 0$ pF to 150 pF	20		165	ns
$t_{SDB}$	Set-Up Time from D <sub>R</sub> Valid to BCLK <sub>R/X</sub> Low		<b>50</b>			ns
$t_{HBD}$	Hold Time from BCLK <sub>R/X</sub> Low to D <sub>R</sub> Invalid		<b>50</b>			ns
$t_{SF}$	Set-Up Time from FS <sub>X/R</sub> to BCLK <sub>X/R</sub> Low	Short Frame Sync Pulse (1 Bit Clock Period Long)	<b>50</b>			ns
$t_{HF}$	Hold Time from BCLK <sub>X/R</sub> Low to FS <sub>X/R</sub> Low	Short Frame Sync Pulse (1 Bit Clock Period Long)	<b>100</b>			ns
$t_{HBF1}$	Hold Time from 3rd Period of Bit Clock Low to Frame Sync (FS <sub>X</sub> or FS <sub>R</sub> )	Long Frame Sync Pulse (from 3 to 8 Bit Clock Periods Long)	<b>100</b>			ns
$t_{WFL}$	Minimum Width of the Frame Sync Pulse (Low Level)	64k Bit/s Operating Mode	<b>160</b>			ns



# Timing Diagrams

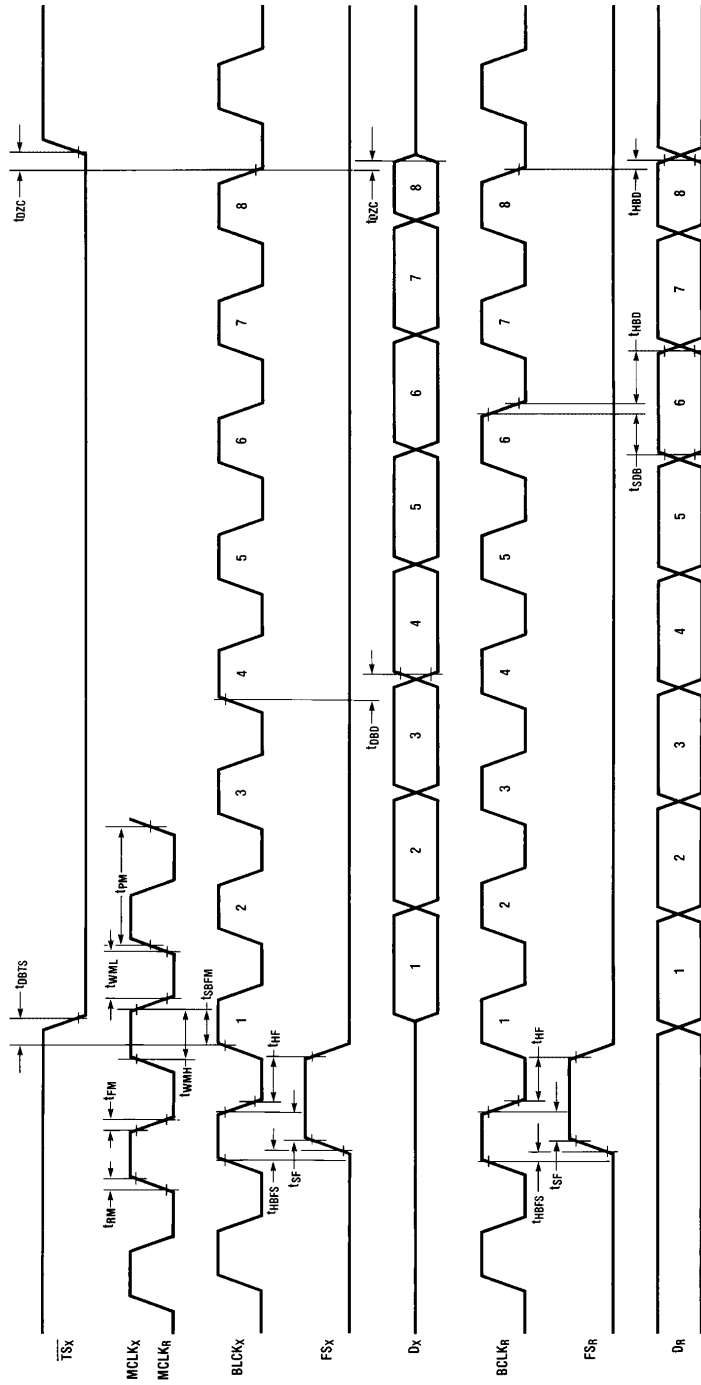


FIGURE 2. Short Frame Sync Timing

TL/H/5070-3

# Timing Diagrams (Continued)

TL/H/5070-4

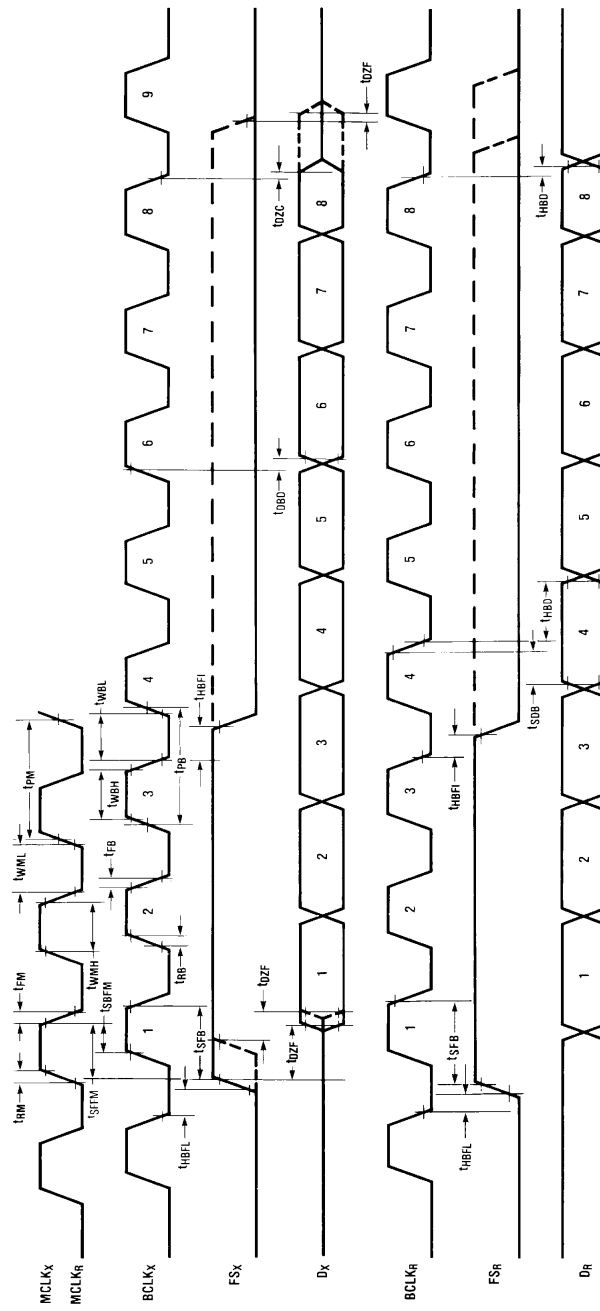


FIGURE 3. Long Frame Sync Timing

## Transmission Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for  $V_{CC} = +5.0V \pm 5\%$ ,  $V_{BB} = -5.0V \pm 5\%$ ;  $T_A = 0^\circ C$  to  $70^\circ C$  by correlation with 100% electrical testing at  $T_A = 25^\circ C$ . All other limits are assured by correlation with other production tests and/or product design and characterization.  $G_{NDA} = 0V$ ,  $f = 1.02$  kHz,  $V_{IN} = 0$  dbm0, transmit input amplifier connected for unity gain non-inverting. Typicals specified at  $V_{CC} = +5.0V$ ,  $V_{BB} = -5.0V$ ,  $T_A = 25^\circ C$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>AMPLITUDE RESPONSE</b>						
	Absolute Levels (Definition of nominal gain)	Nominal 0 dBm0 Level is 4 dBm (600Ω) 0 dBm0		1.2276		Vrms
$t_{MAX}$	Virtual Decision Value Defined per CCITT Rec. G711	Max Transmit Overload Level TP3064 (3.17 dBm0) TP3067 (3.14 dBm0)		2.501 2.492		$V_{PK}$ $V_{PK}$
$G_{XA}$	Transmit Gain, Absolute	$T_A = 25^\circ C$ , $V_{CC} = 5V$ , $V_{BB} = -5V$	<b>-0.15</b>		<b>0.15</b>	dB
$G_{XR}$	Transmit Gain, Relative to $G_{XA}$	f = 16 Hz f = 50 Hz f = 60 Hz f = 200 Hz f = 300 Hz-3000 Hz f = 3300 Hz f = 3400 Hz f = 4000 Hz f = 4600 Hz and Up, Measure Response from 0 Hz to 4000 Hz	<b>-1.8</b> <b>-0.15</b> <b>-0.35</b> <b>-0.7</b>		-40 -30 <b>-26</b> <b>-0.1</b> <b>0.15</b> <b>0</b> <b>-14</b> <b>-32</b>	dB dB dB dB dB dB dB dB
$G_{XAT}$	Absolute Transmit Gain Variation with Temperature	Relative to $G_{XA}$	-0.1		0.1	dB
$G_{XAV}$	Absolute Transmit Gain Variation with Supply Voltage	Relative to $G_{XA}$	<b>-0.05</b>		<b>0.05</b>	dB
$G_{XRL}$	Transmit Gain Variations with Level	Sinusoidal Test Method Reference Level = -10 dBm0 $V_{FXL}^+ = -40$ dBm0 to +3 dBm0 $V_{FXL}^+ = -50$ dBm0 to -40 dBm0 $V_{FXL}^+ = -55$ dBm0 to -50 dBm0	<b>-0.2</b> <b>-0.4</b> <b>-1.2</b>		<b>0.2</b> <b>0.4</b> <b>1.2</b>	dB dB dB
$G_{RA}$	Receive Gain, Absolute	$T_A = 25^\circ C$ , $V_{CC} = 5V$ , $V_{BB} = -5V$ Input = Digital Code Sequence for 0 dBm0 Signal	<b>-0.15</b>		<b>0.15</b>	dB
$G_{RR}$	Receive Gain, Relative to $G_{RA}$	f = 0 Hz to 3000 Hz f = 3300 Hz f = 3400 Hz f = 4000 Hz	<b>-0.15</b> <b>-0.35</b> <b>-0.7</b>		<b>0.15</b> <b>0.05</b> <b>0</b> <b>-14</b>	dB dB dB dB
$G_{RAT}$	Absolute Receive Gain Variation with Temperature	Relative to $G_{RA}$	-0.1		0.1	dB
$G_{RAV}$	Absolute Receive Gain Variation with Supply Voltage	Relative to $G_{RA}$	<b>-0.05</b>		<b>0.05</b>	dB
$G_{RRLL}$	Receive Gain Variations with Level	Sinusoidal Test Method; Reference Input PCM Code Corresponds to an Ideally Encoded -10 dBm0 Signal PCM Level = -40 dBm0 to +3 dBm0 PCM Level = -50 dBm0 to -40 dBm0 PCM Level = -55 dBm0 to -50 dBm0	<b>-0.2</b> <b>-0.4</b> <b>-1.2</b>		<b>0.2</b> <b>0.4</b> <b>1.2</b>	dB dB dB
$V_{RO}$	Receive Filter Output at $V_{FRO}$	$R_L = 10$ kΩ	-2.5		2.5	V

## Transmission Characteristics (Continued)

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for  $V_{CC} = +5.0V \pm 5\%$ ,  $V_{BB} = -5.0V \pm 5\%$ ;  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$  by correlation with 100% electrical testing at  $T_A = 25^\circ\text{C}$ . All other limits are assured by correlation with other production tests and/or product design and characterization.  $G_{ND A} = 0V$ ,  $f = 1.02\text{ kHz}$ ,  $V_{IN} = 0\text{ dBm0}$ , transmit input amplifier connected for unity gain non-inverting. Typical values specified at  $V_{CC} = +5.0V$ ,  $V_{BB} = -5.0V$ ,  $T_A = 25^\circ\text{C}$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>ENVELOPE DELAY DISTORTION WITH FREQUENCY</b>						
$D_{XA}$	Transmit Delay, Absolute	$f = 1600\text{ Hz}$		290	315	$\mu\text{s}$
$D_{XR}$	Transmit Delay, Relative to $D_{XA}$	$f = 500\text{ Hz} - 600\text{ Hz}$		195	220	$\mu\text{s}$
		$f = 600\text{ Hz} - 800\text{ Hz}$		120	145	$\mu\text{s}$
		$f = 800\text{ Hz} - 1000\text{ Hz}$		50	75	$\mu\text{s}$
		$f = 1000\text{ Hz} - 1600\text{ Hz}$		20	40	$\mu\text{s}$
		$f = 1600\text{ Hz} - 2600\text{ Hz}$		55	75	$\mu\text{s}$
		$f = 2600\text{ Hz} - 2800\text{ Hz}$		80	105	$\mu\text{s}$
		$f = 2800\text{ Hz} - 3000\text{ Hz}$		130	155	$\mu\text{s}$
$D_{RA}$	Receive Delay, Absolute	$f = 1600\text{ Hz}$		180	200	$\mu\text{s}$
$D_{RR}$	Receive Delay, Relative to $D_{RA}$	$f = 500\text{ Hz} - 1000\text{ Hz}$	-40	-25		$\mu\text{s}$
		$f = 1000\text{ Hz} - 1600\text{ Hz}$	-30	-20		$\mu\text{s}$
		$f = 1600\text{ Hz} - 2600\text{ Hz}$		70	90	$\mu\text{s}$
		$f = 2600\text{ Hz} - 2800\text{ Hz}$		100	125	$\mu\text{s}$
		$f = 2800\text{ Hz} - 3000\text{ Hz}$		145	175	$\mu\text{s}$
<b>NOISE</b>						
$N_{XC}$	Transmit Noise, C Message Weighted	TP3064 (Note 1)		12	<b>15</b>	dBrnC0
$N_{XP}$	Transmit Noise, Psophometric Weighted	TP3067 (Note 1)		-74	<b>-67</b>	dBm0p
$N_{RC}$	Receive Noise, C Message Weighted	PCM Code Equals Alternating Positive and Negative Zero TP3064		8	<b>11</b>	dBrnC0
$N_{RP}$	Receive Noise, Psophometric Weighted	PCM Code Equals Positive Zero TP3067		-82	<b>-79</b>	dBm0p
$N_{RS}$	Noise, Single Frequency	$f = 0\text{ kHz}$ to $100\text{ kHz}$ , Loop Around Measurement, $V_{FXI} = 0\text{ Vrms}$			-53	dBm0
$PPSR_X$	Positive Power Supply Rejection, Transmit	$V_{CC} = 5.0\text{ V}_{DC} + 100\text{ mVrms}$ $f = 0\text{ kHz} - 50\text{ kHz}$ (Note 2)	<b>40</b>			dB
$NPSR_X$	Negative Power Supply Rejection, Transmit	$V_{BB} = -5.0\text{ V}_{DC} + 100\text{ mVrms}$ $f = 0\text{ kHz} - 50\text{ kHz}$ (Note 2)	<b>40</b>			dB
$PPSR_R$	Positive Power Supply Rejection, Receive	PCM Code Equals Positive Zero $V_{CC} = 5.0\text{ V}_{DC} + 100\text{ mVrms}$ Measure $V_{FR0}$ $f = 0\text{ Hz} - 4000\text{ Hz}$ $f = 4\text{ kHz} - 50\text{ kHz}$	<b>38</b> <b>25</b>			dB dB
$NPSR_R$	Negative Power Supply Rejection, Receive	PCM Code Equals Positive Zero $V_{BB} = -5.0\text{ V}_{DC} + 100\text{ mVrms}$ Measure $V_{FR0}$ $f = 0\text{ Hz} - 4000\text{ Hz}$ $f = 4\text{ kHz} - 25\text{ kHz}$ $f = 25\text{ kHz} - 50\text{ kHz}$	<b>40</b> <b>40</b> <b>36</b>			dB dB dB
SOS	Spurious Out-of-Band Signals at the Channel Output	0 dBm0, 300 Hz - 3400 Hz Input PCM Code Applied at DR Measure Individual Image Signals at $V_{FR0}$ 4600 Hz - 7600 Hz 7600 Hz - 8400 Hz 8400 Hz - 100,000 Hz			<b>-32</b> -40 <b>-32</b>	dB dB dB

## Transmission Characteristics (Continued)

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for  $V_{CC} = +5.0V \pm 5\%$ ,  $V_{BB} = -5.0V \pm 5\%$ ;  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$  by correlation with 100% electrical testing at  $T_A = 25^\circ\text{C}$ . All other limits are assured by correlation with other production tests and/or product design and characterization.  $G_{NDA} = 0V$ ,  $f = 1.02\text{ kHz}$ ,  $V_{IN} = 0\text{ dBm0}$ , transmit input amplifier connected for unity gain non-inverting. Typicals specified at  $V_{CC} = +5.0V$ ,  $V_{BB} = -5.0V$ ,  $T_A = 25^\circ\text{C}$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>DISTORTION</b>						
STD <sub>X</sub> , STD <sub>R</sub>	Signal to Total Distortion Transmit or Receive Half-Channel	Sinusoidal Test Method (Note 3) Level = 3.0 dBm0 = 0 dBm0 to -30 dBm0 = -40 dBm0 XMT RCV = -55 dBm0 XMT RCV	<b>33</b> <b>36</b> <b>29</b> <b>30</b> <b>14</b> <b>15</b>			dBC dBC dBC dBC dBC dBC
SFD <sub>X</sub>	Single Frequency Distortion, Transmit				<b>-46</b>	dB
SFD <sub>R</sub>	Single Frequency Distortion, Receive				<b>-46</b>	dB
IMD	Intermodulation Distortion	Loop Around Measurement, $V_{FXI}^+ = -4\text{ dBm0}$ to $-21\text{ dBm0}$ , Two Frequencies in the Range 300 Hz - 3400 Hz			-41	dB
<b>CROSSTALK</b>						
CT <sub>X-R</sub>	Transmit to Receive Crosstalk	$f = 300\text{ Hz} - 3000\text{ Hz}$ $D_R = \text{Quiet PCM Code}$		-90	<b>-75</b>	dB
CT <sub>R-X</sub>	Receive to Transmit Crosstalk	$f = 300\text{ Hz} - 3000\text{ Hz}$ , $V_{FXI} = 0V$ (Note 2)		-90	<b>-70</b>	dB
<b>POWER AMPLIFIERS</b>						
V <sub>OPA</sub>	Maximum 0 dBm0 Level (Better than $\pm 0.1\text{ dB}$ Linearity over the Range $-10\text{ dBm0}$ to $+3\text{ dBm0}$ )	Balanced Load, $R_L$ Connected Between $V_{PO}^+$ and $V_{PO}^-$ . $R_L = 600\Omega$ $R_L = 1200\Omega$	<b>3.3</b> 3.5			Vrms Vrms
S/D <sub>P</sub>	Signal/Distortion	$R_L = 600\Omega$	50			dB

**Note 1:** Measured by extrapolation from the distortion test result at  $-50\text{ dBm0}$ .

**Note 2:** PPSR<sub>X</sub>, NPSR<sub>X</sub>, and CT<sub>R-X</sub> are measured with a  $-50\text{ dBm0}$  activation signal applied to  $V_{FXI}^+$ .

**Note 3:** TP3064 is measured using C message weighted filter. TP3067 is measured using psophometric weighted filter.

## Applications Information

### POWER SUPPLIES

While the pins of the TP3060 family are well protected against electrical misuse, it is recommended that the standard CMOS practice be followed, ensuring that ground is connected to the device before any other connections are made. In applications where the printed circuit board may be plugged into a "hot" socket with power and clocks already present, an extra long ground pin in the connector should be used.

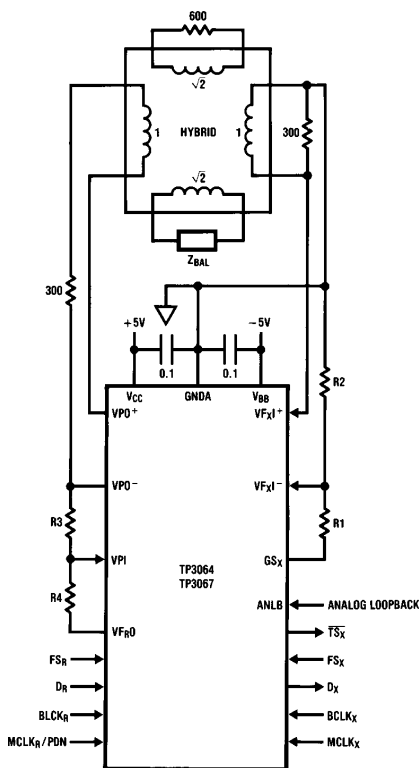
All ground connections to each device should meet at a common point as close as possible to the GNDA pin. This

minimizes the interaction of ground return currents flowing through a common bus impedance. 0.1  $\mu\text{F}$  supply decoupling capacitors should be connected from this common ground point to  $V_{CC}$  and  $V_{BB}$ , as close to the device as possible.

For best performance, the ground point of each CODEC/FILTER on a card should be connected to a common card ground in "STAR" formation, rather than via a ground bus. This common ground point should be decoupled to  $V_{CC}$  and  $V_{BB}$  with 10  $\mu\text{F}$  capacitors.

**Note:** See Application Note 370 for further details

### Typical Asynchronous Application



TL/H/5070-5

**Note 1:** Transmit gain =  $20 \times \log \left( \frac{R1 + R2}{R2} \right)$ ,  $(R1 + R2) \geq 10 \text{ k}\Omega$

**Note 2:** Receive gain =  $20 \times \log \left( \frac{2 \times R3}{R4} \right)$ ,  $R4 \geq 10 \text{ k}\Omega$

**FIGURE 4**

## Definitions and Timing Conventions

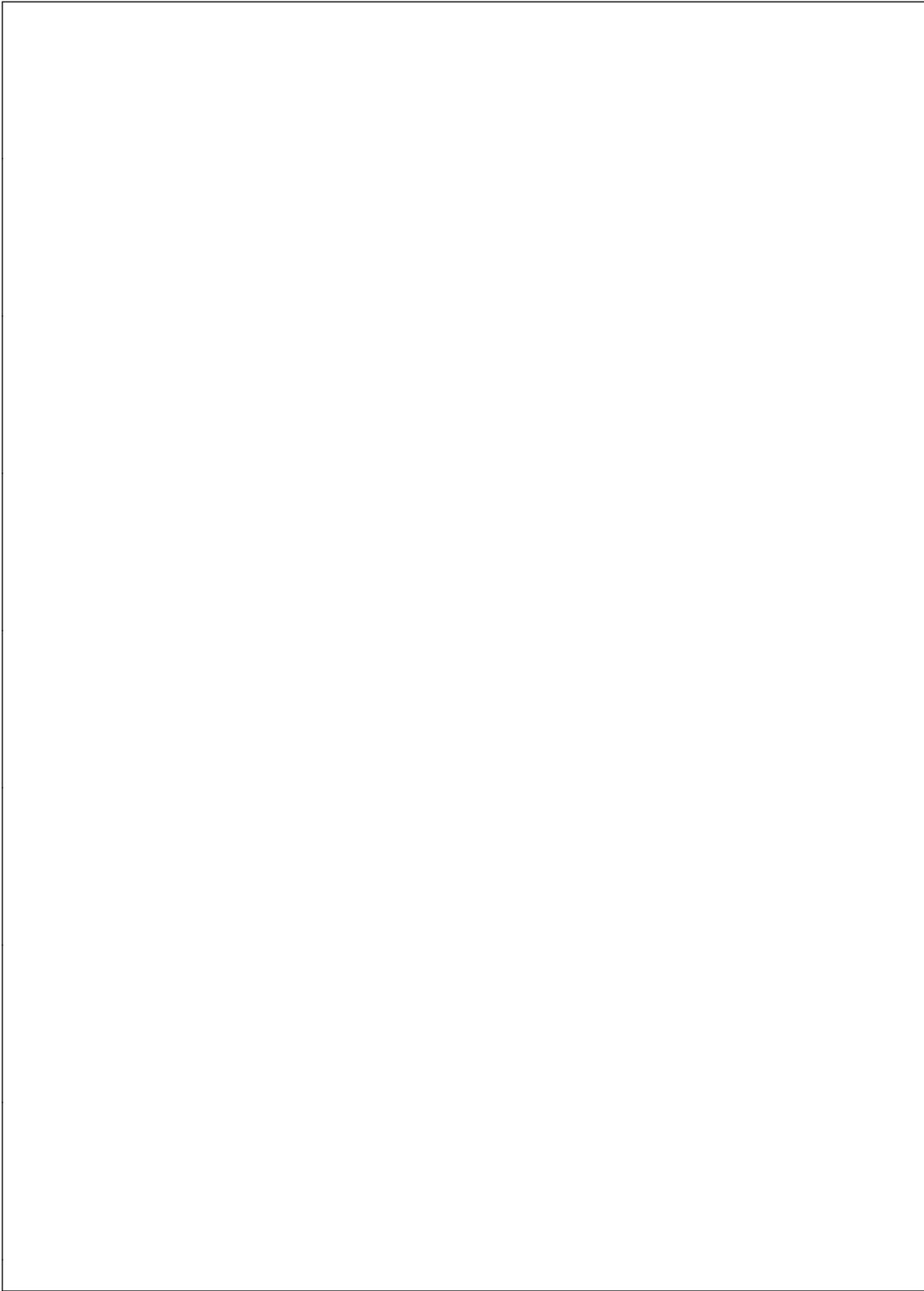
### DEFINITIONS

$V_{IH}$	$V_{IH}$ is the d.c. input level above which an input level is guaranteed to appear as a logical one. This parameter is to be measured by performing a functional test at reduced clock speeds and nominal timing, (i.e. not minimum setup and hold times or output strobes), with the high level of all driving signals set to $V_{IH}$ and maximum supply voltages applied to the device
$V_{IL}$	$V_{IL}$ is the d.c. input level below which an input level is guaranteed to appear as a logical zero to the device. This parameter is measured in the same manner as $V_{IH}$ but with all driving signal low levels set to $V_{IL}$ and minimum supply voltages applied to the device.
$V_{OH}$	$V_{OH}$ is the minimum d.c. output level to which an output placed in a logical one state will converge when loaded at the maximum specified load current.
$V_{OL}$	$V_{OL}$ is the maximum d.c. output level to which an output placed in a logical zero state will converge when loaded at the maximum specified load current.
Threshold Region	The threshold region is the range of input voltages between $V_{IL}$ and $V_{IH}$ .
Valid Signal	A signal is Valid if it is in one of the valid logic states, (i.e. above $V_{IH}$ or below $V_{IL}$ ). In timing specifications, a signal is deemed valid at the instant it enters a valid state.
Invalid Signal	A signal is Invalid if it is not in a valid logic state, i.e. when it is in the threshold region between $V_{IL}$ and $V_{IH}$ . In timing specifications, a signal is deemed Invalid at the instant it enters the threshold region.

### TIMING CONVENTIONS

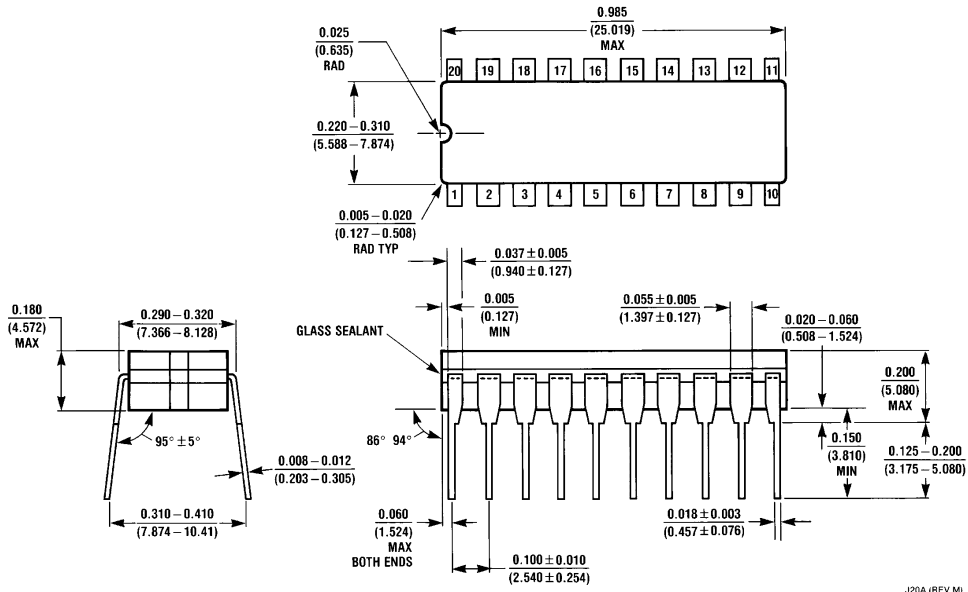
For the purposes of this timing specification, the following conventions apply:

Input Signals	All input signals may be characterized as: $V_L = 0.4V$ , $V_H = 2.4V$ , $t_R < 10$ ns, $t_F < 10$ ns.
Period	The period of clock signal is designated as $t_{Pxx}$ where xx represents the mnemonic of the clock signal being specified.
Rise Time	Rise times are designated as $t_{Ryy}$ , where yy represents a mnemonic of the signal whose rise time is being specified. $t_{Ryy}$ is measured from $V_{IL}$ to $V_{IH}$ .
Fall Time	Fall times are designated as $t_{Fyy}$ , where yy represents a mnemonic of the signal whose fall time is being specified. $t_{Fyy}$ is measured from $V_{IH}$ to $V_{IL}$ .
Pulse Width High	The high pulse width is designated as $t_{WzzH}$ , where zz represents the mnemonic of the input or output signal whose pulse width is being specified. High pulse widths are measured from $V_{IH}$ to $V_{IH}$ .
Pulse Width Low	The low pulse width is designated as $t_{WzzL}$ , where zz represents the mnemonic of the input or output signal whose pulse width is being specified. Low pulse widths are measured from $V_{IL}$ to $V_{IL}$ .
Setup Time	Setup times are designated as $t_{Swwxx}$ , where ww represents the mnemonic of the input signal whose setup time is being specified relative to a clock or strobe input represented by mnemonic xx. Setup times are measured from the ww Valid to xx Invalid.
Hold Time	Hold times are designated as $t_{Hxxww}$ , where ww represents the mnemonic of the input signal whose hold time is being specified relative to a clock or strobe input represented by mnemonic xx. Hold times are measured from xx Valid to ww Invalid.
Delay Time	Delay times are designated as $t_{Dxxyy}$ Hi to Low, where xx represents the mnemonic of the input reference signal and yy represents the mnemonic of the output signal whose timing is being specified relative to xx. The mnemonic may optionally be terminated by an H or L to specify the high going or low going transition of the output signal. Maximum delay times are measured from xx Valid to yy Valid. Minimum delay times are measured from xx Valid to yy Invalid. This parameter is tested under the load conditions specified in the Conditions column of the Timing Specifications section of this data sheet.

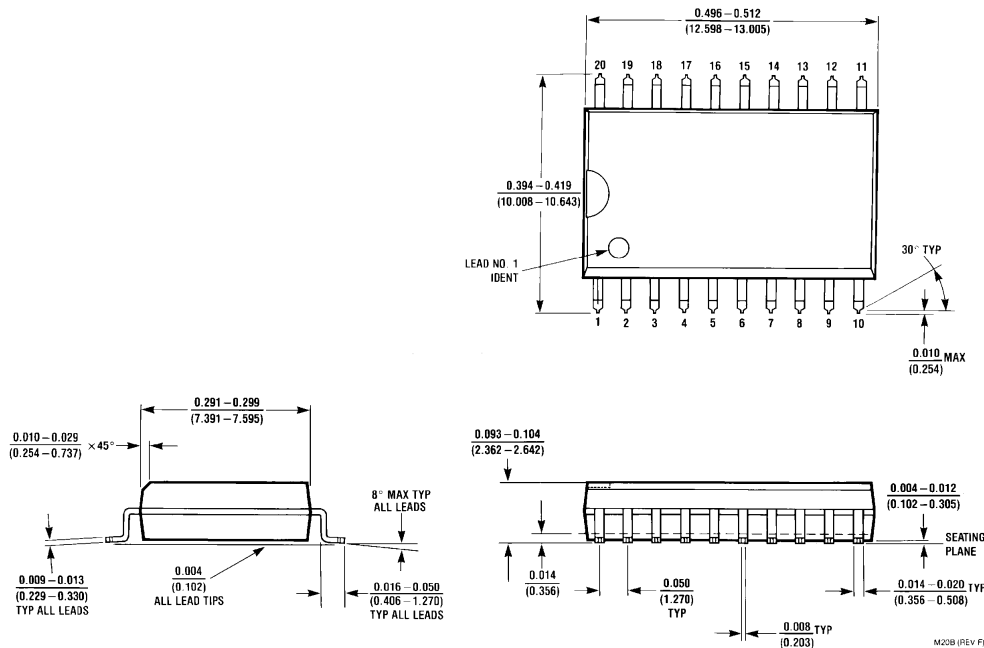




**Physical Dimensions** inches (millimeters)

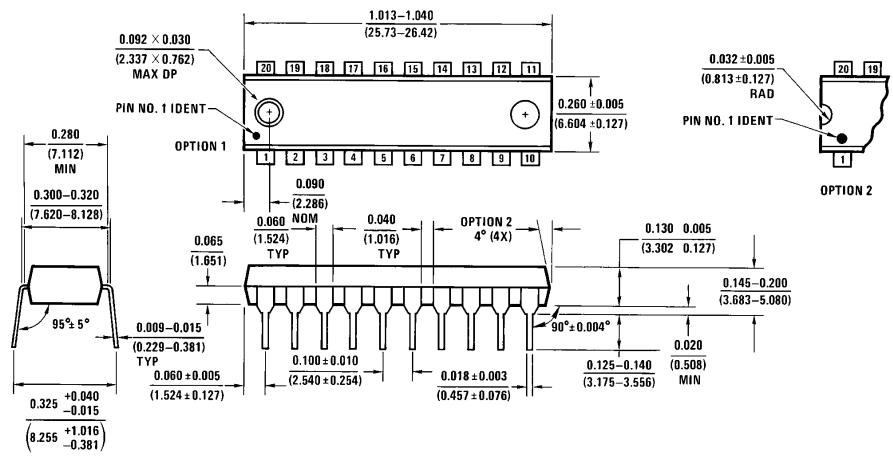


**Cavity Dual-In-Line Package (J)**  
 Order Number TP3064J or TP3067J  
 NS Package Number J20A



**Molded Small Outline Package (WM)**  
 Order Number TP3064WM or TP3067WM  
 NS Package Number M20B

**Physical Dimensions** inches (millimeters) (Continued)

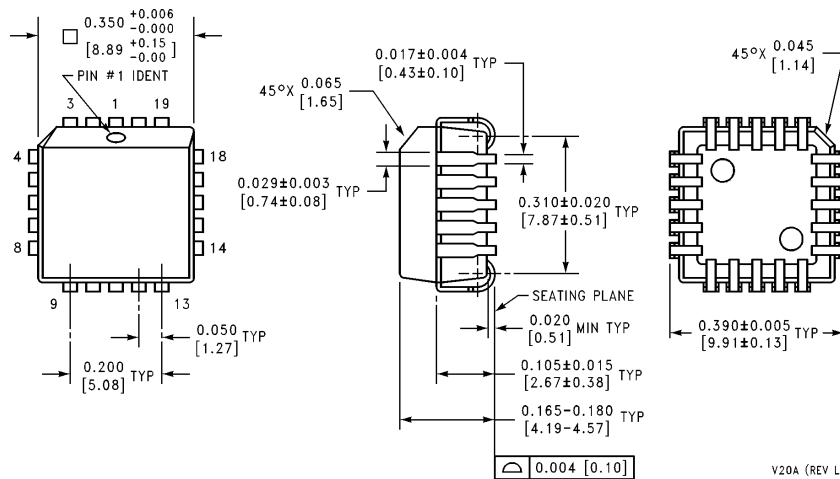


**Molded Dual-In-Line Package (N)**  
**Order Number TP3064N or TP3067N**  
**NS Package Number N20A**

N20A (REV. GI)

**Physical Dimensions** inches (millimeters) (Continued)

Lit. # 113975



**Plastic Chip Carrier (V)**  
**Order Number TP3064V or TP3067V**  
**NS Package Number V20A**

V20A (REV L)

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