TP3052-X,TP3054-X,TP3057-X

TP3054-X, TP3057-X Extended Temperature Serial Interface CODEC/Filter

COMBO Family



Literature Number: SNOSBY2B



TP3054-X, TP3057-X

Extended Temperature Serial Interface CODEC/Filter COMBO® Family

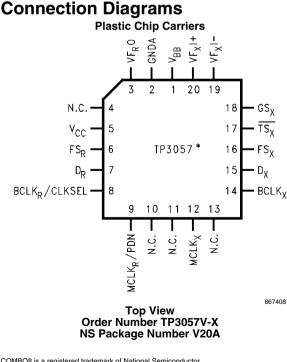
General Description

The TP3054, TP3057 family consists of μ -law and A-law monolithic PCM CODEC/filters utilizing the A/D and D/A conversion architecture shown in *Figure 1*, and a serial PCM interface. The devices are fabricated using National's advanced double-poly CMOS process (microCMOS).

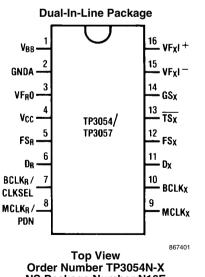
The encode portion of each device consists of an input gain adjust amplifier, an active RC pre-filter which eliminates very high frequency noise prior to entering a switched-capacitor band-pass filter that rejects signals below 200 Hz and above 3400 Hz. Also included are auto-zero circuitry and a companding coder which samples the filtered signal and encodes it in the companded µ-law or A-law PCM format. The decode portion of each device consists of an expanding decoder. which reconstructs the analog signal from the companded ulaw or A-law code, a low-pass filter which corrects for the sin x/x response of the decoder output and rejects signals above 3400 Hz followed by a single-ended power amplifier capable of driving low impedance loads. The devices require two 1.536 MHz, 1.544 MHz or 2.048 MHz transmit and receive master clocks, which may be asynchronous; transmit and receive bit clocks, which may vary from 64 kHz to 2.048 MHz; and transmit and receive frame sync pulses. The timing of the frame sync pulses and PCM data is compatible with both industry standard formats.

Features

- -40°C to +85°C operation
- Complete CODEC and filtering system (COMBO) including:
 - Transmit high-pass and low-pass filtering
 - Receive low-pass filter with sin x/x correction
 - Active RC noise filters
 - µ-law or A-law compatible COder and DECoder
 - Internal precision voltage reference
 - Serial I/O interface
 - Internal auto-zero circuitry
- µ-law, 16-pin—TP3054
- A-law, 16-pin—TP3057
- Designed for D3/D4 and CCITT applications
- ±5V operation
- Low operating power—typically 50 mW
- Power-down standby mode—typically 3 mW
- Automatic power-down
- TTL or CMOS compatible digital interfaces
- Maximizes line interface card circuit density
- Dual-In-Line or PCC surface mount packages
- See also AN-370, "Techniques for Designing with CODEC/Filter COMBO Circuits"

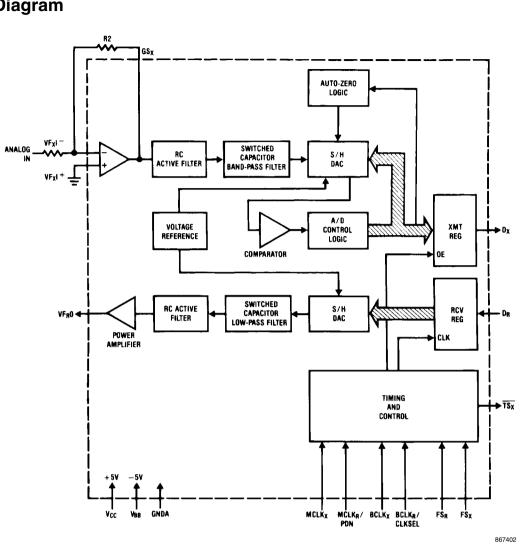


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Order Number TP3054N-X NS Package Number N16E Order Number TP3054WM-X NS Package Number M16B P3054-X, TP3057-X Extended Temperature Serial Interface CODEC/Filter COMBO Family

Block Diagram





Pin Desci	riptions	Symbol	Function
Symbol V _{BB} GNDA VF _R O	FunctionNegative power supply pin. $V_{BB} = -5V \pm 5\%$.Analog ground. All signals are referencedto this pin.Analog output of the receive poweramplifier.	BCLK _R /CLKSEL	The bit clock which shifts data into D_R after the FS _R leading edge. May vary from 64 kHz to 2.048 MHz. Alternatively, may be a logic input which selects either 1.536 MHz/1.544 MHz or 2.048 MHz for master clock in synchronous mode and BCLK _X is used for both transmit and receive directions (see <i>Table 1</i>).
V _{cc}	Positive power supply pin. $V_{CC} = +5V \pm 5\%$.	MCLK _R /PDN	Receive master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be
FS _R	Receive frame sync pulse which enables $BCLK_R$ to shift PCM data into D_R . FS _R is an 8 kHz pulse train. See <i>Figure 2</i> and <i>Figure 3</i> for timing details.		asynchronous with MCLK _X , but should be synchronous with MCLK _X for best performance. When MCLK _R is connected continuously low, MCLK _X is selected for
D _R	Receive data input. PCM data is shifted into ${\rm D_R}$ following the ${\rm FS_R}$ leading edge.		all internal timing. When $MCLK_R$ is connected continuously high, the device is powered down.

Symbol	Function
MCLK _X	Transmit master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with MCLK _R . Best performance is realized from synchronous operation.
FS _X	Transmit frame sync pulse input which enables $BCLK_X$ to shift out the PCM data on D_X . FS _X is an 8 kHz pulse train, see <i>Figure 2</i> and <i>Figure 3</i> for timing details.
BCLK _X	The bit clock which shifts out the PCM data on D_X . May vary from 64 kHz to 2.048 MHz, but must be synchronous with MCLK _x .
D _X	The TRI-STATE® PCM data output which is enabled by FS _x .
$\overline{TS_X}$	Open drain output which pulses low during the encoder time slot.
GS _x	Analog output of the transmit input amplifier. Used to externally set gain.
VF _X I−	Inverting input of the transmit input amplifier.
VF _X I+	Non-inverting input of the transmit input amplifier.

Functional Description

POWER-UP

When power is first applied, power-on reset circuitry initializes the COMBO and places it into a power-down state. All nonessential circuits are deactivated and the D_X and VF_RO outputs are put in high impedance states. To power-up the device, a logical low level or clock must be applied to the MCLK_R/PDN pin and FS_X and/or FS_R pulses must be present. Thus, 2 power-down control modes are available. The first is to pull the MCLK_R/PDN pin high; the alternative is to hold both FS_X and FS_R inputs continuously low—the device will powerdown approximately 1 ms after the last FS_X or FS_R pulse. Power-up will occur on the first FS_X or FS_R pulse. The TRI-STATE PCM data output, D_X, will remain in the high impedance state until the second FS_X pulse.

SYNCHRONOUS OPERATION

For synchronous operation, the same master clock and bit clock should be used for both the transmit and receive directions. In this mode, a clock must be applied to MCLK_X and the MCLK_R/PDN pin can be used as a power-down control. A low level on MCLK_R/PDN powers up the device and a high level powers down the device. In either case, MCLK_X will be selected as the master clock for both the transmit and receive circuits. A bit clock must also be applied to BCLK_X and the BCLK_R/CLKSEL can be used to select the proper internal divider for a master clock of 1.536 MHz, 1.544 MHz or 2.048 MHz. For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame.

With a fixed level on the BCLK_R/CLKSEL pin, BCLK_X will be selected as the bit clock for both the transmit and receive directions. *Table 1* indicates the frequencies of operation which can be selected, depending on the state of BCLK_R/CLKSEL. In this synchronous mode, the bit clock, BCLK_X, may be from 64 kHz to 2.048 MHz, but must be synchronous with MCLK_X.

Each FS_X pulse begins the encoding cycle and the PCM data from the previous encode cycle is shifted out of the enabled D_X output on the positive edge of BCLK_X. After 8 bit clock periods, the TRI-STATE D_X output is returned to a high impedance state. With an FS_R pulse, PCM data is latched via the D_R input on the negative edge of BCLK_X (or BCLK_R if running). FS_x and FS_R must be synchronous with MCLK_{X/R}.

TABLE 1. Selection of Master Clock Frequencies

BCLK _R /CLKSEL	Master Clock Frequency Selected				
	TP3057	TP3054			
Clocked	2.048 MHz	1.536 MHz or			
		1.544 MHz			
0	1.536 MHz or	2.048 MHz			
	1.544 MHz				
1	2.048 MHz	1.536 MHz or			
		1.544 MHz			

ASYNCHRONOUS OPERATION

For asynchronous operation, separate transmit and receive clocks may be applied. $MCLK_X$ and $MCLK_R$ must be 2.048 MHz for the TP3057, or 1.536 MHz, 1.544 MHz for the TP3054, and need not be synchronous. For best transmission performance, however, $MCLK_R$ should be synchronous with $MCLK_X$, which is easily achieved by applying only static logic levels to the $MCLK_R/PDN$ pin. This will automatically connect $MCLK_X$ to all internal $MCLK_R$ functions (see Pin Description). For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame. FS_X starts each encoding cycle and must be synchronous with $MCLK_X$. FS_R starts each decoding cycle and must be synchronous with $BCLK_X$. FS_R at the encoding cycle and must be synchronous with $BCLK_R$. BCLK_R must be a clock, the logic levels shown in *Table 1* are not valid in asynchronous mode. BCLK_X and BCLK_R may operate from 64 kHz to 2.048 MHz.

SHORT FRAME SYNC OPERATION

The COMBO can utilize either a short frame sync pulse or a long frame sync pulse. Upon power initialization, the device assumes a short frame mode. In this mode, both frame sync pulses, FS_X and FS_R , must be one bit clock period long, with timing relationships specified in *Figure 2*. With FS_X high during a falling edge of BCLK_X, the next rising edge of BCLK_X enables the D_X TRI-STATE output buffer, which will output the sign bit. The following seven rising edges clock out the remaining seven bits, and the next falling edge of BCLK_R (BCLK_X in synchronous mode), the next falling edge of BCLK_R latches in the sign bit. The following seven falling edge of BCLK_R in the seven remaining bits. All four devices may utilize the short frame sync pulse in synchronous or asynchronous operating mode.

LONG FRAME SYNC OPERATION

To use the long frame mode, both the frame sync pulses, FS_x and FS_R , must be three or more bit clock periods long, with timing relationships specified in *Figure 3*. Based on the transmit frame sync, FS_x , the COMBO will sense whether short or long frame sync pulses are being used. For 64 kHz operation, the frame sync pulse must be kept low for a minimum of 160 ns. The D_x TRI-STATE output buffer is enabled with the rising edge of FS_x or the rising edge of BCLK_x, whichever comes later, and the first bit clocked out is the sign bit. The following seven BCLK_x rising edges clock out the remaining seven bits. The D_x output is disabled by the falling

 BCLK_X edge following the eighth rising edge, or by FS_X going low, whichever comes later. A rising edge on the receive frame sync pulse, FS_R , will cause the PCM data at D_R to be latched in on the next eight falling edges of BCLK_R (BCLK_X in synchronous mode). All four devices may utilize the long frame sync pulse in synchronous or asynchronous mode.

In applications where the LSB bit is used for signalling, with FS_R two bit clock periods long, the decoder will interpret the lost LSB as "½" to minimize noise and distortion.

TRANSMIT SECTION

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors, see *Figure 4.* The low noise and wide bandwidth allow gains in excess of 20 dB across the audio passband to be realized. The op amp drives a unity-gain filter consisting of RC active pre-filter, followed by an eighth order switched-capacitor bandpass filter clocked at 256 kHz. The output of this filter directly drives the encoder sample-and-hold circuit. The A/D is of companding type according to μ -law (TP3057) coding conventions. A precision voltage reference is trimmed in manufacturing to provide an input overload (t_{MAX}) of nominally 2.5V peak (see table of Transmission Characteristics). The FS_X frame sync pulse controls the sam-

pling of the filter output, and then the successive-approximation encoding cycle begins. The 8-bit code is then loaded into a buffer and shifted out through D_X at the next FS_X pulse. The total encoding delay will be approximately 165 μ s (due to the transmit filter) plus 125 μ s (due to encoding delay), which totals 290 μ s. Any offset voltage due to the filters or comparator is cancelled by sign bit integration.

RECEIVE SECTION

The receive section consists of an expanding DAC which drives a fifth order switched-capacitor low pass filter clocked at 256 kHz. The decoder is A-law (TP3057) or μ -law (TP3054) and the 5th order low pass filter corrects for the sin x/x attenuation due to the 8 kHz sample/hold. The filter is then followed by a 2nd order RC active post-filter/power amplifier capable of driving a 600 Ω load to a level of 7.2 dBm. The receive section is unity-gain. Upon the occurrence of FS_R, the data at the D_R input is clocked in on the falling edge of the next eight BCLK_R (BCLK_X) periods. At the end of the decoder time slot, the decoding cycle begins, and 10 µs later the decoder DAC output is updated. The total decoder delay is ~10 µs (decoder update) plus 110 µs (filter delay) plus 62.5 µs (½ frame), which gives approximately 180 µs.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

V _{CC} to GNDA	7V
V _{BB} to GNDA	–7V
Voltage at any Analog Input or Output	$V_{\rm CC}\text{+}0.3\text{V}$ to $V_{\rm BB}\text{-}0.3\text{V}$

Voltage at any Digital Input or
OutputV
CC+0.3V to GNDA-0.3VOperating Temperature Range-55°C to + 125°CStorage Temperature Range-65°C to +150°CLead Temperature
(Soldering, 10 sec.)300°C

Electrical Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for $V_{CC} = +5.0V \pm 5\%$, $V_{BB} = -5.0V \pm 5\%$; $T_A = -40^{\circ}C$ to +85°C by correlation with 100% electrical testing at $T_A = 25^{\circ}C$. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GNDA. Typicals specified at $V_{CC} = +5.0V$, $V_{BB} = -5.0V$, $T_A = 25^{\circ}C$.

Symbol	Parameter	Conditions	Min	Тур	Max	Units
DIGITAL I	NTERFACE					
V _{IL}	Input Low Voltage				0.6	V
V _{IH}	Input High Voltage		2.2			V
V _{OL}	Output Low Voltage	D _X , I _L =3.2 mA			0.4	V
		SIG _R , I _L =1.0 mA			0.4	V
		$\overline{TS_{X}}$, I _L =3.2 mA, Open Drain			0.4	V
V _{OH}	Output High Voltage	D _X , I _H =–3.2 mA	2.4			V
		SIG _R , I _H =–1.0 mA	2.4			V
I _{IL}	Input Low Current	GNDA≤V _{IN} ≤V _{IL} , All Digital Inputs	-10		10	μA
I _{IH}	Input High Current	V _{IH} ≤V _{IN} ≤V _{CC}	-10		10	μA
I _{OZ}	Output Current in High Impedance State (TRI-STATE)		-10		10	μA
ANALOG I	NTERFACE WITH TRANSMIT INPUT AI					
I _I XA	Input Leakage Current	–2.5V≤V≤+2.5V, VF _x I+ or VF _x I-	-200		200	nA
R _I XA	Input Resistance	–2.5V≤V≤+2.5V, VF _x I+ or VF _x I-	10			MΩ
R _O XA	Output Resistance	Closed Loop, Unity Gain		1	3	Ω
R _L XA	Load Resistance	GS _x	10			kΩ
	Load Capacitance	GS _x			50	pF
V _o XA	Output Dynamic Range	 GS _X , R _L ≥ 10 kΩ	-2.8		2.8	V
A _V XA	Voltage Gain	VF _x I+ to GS _x	5000			V/V
F _U XA	Unity Gain Bandwidth		1	2		MHz
V _{OS} XA	Offset Voltage		-20		20	mV
V _{CM} XA	Common-Mode Voltage	CMRRXA > 60 dB	-2.5		2.5	V
CMRRXA	Common-Mode Rejection Ratio	DC Test	60			dB
PSRRXA	Power Supply Rejection Ratio	DC Test	60			dB
ANALOG I	NTERFACE WITH RECEIVE FILTER (A	LL DEVICES)	•			
R _O RF	Output Resistance	Pin VF _R O		1	3	Ω
R _L RF	Load Resistance	VF _R O=±2.5V	600			Ω
C _L RF	Load Capacitance				500	pF
VOS _R O	Output DC Offset Voltage		-200		200	mV
POWER D	ISSIPATION (ALL DEVICES)					
I _{CC} 0	Power-Down Current	No Load (Note 2)		0.65	2.0	mA
I _{BB} 0	Power-Down Current	No Load (Note 2)		0.01	0.33	mA
I _{CC} 1	Power-Up (Active) Current	No Load(-40°C to 85°C)		5.0	11.0	mA
I _{BB} 1	Power-Up (Active) Current	No Load (–40°C to 85°C)		5.0	11.0	mA

Timing Specifications

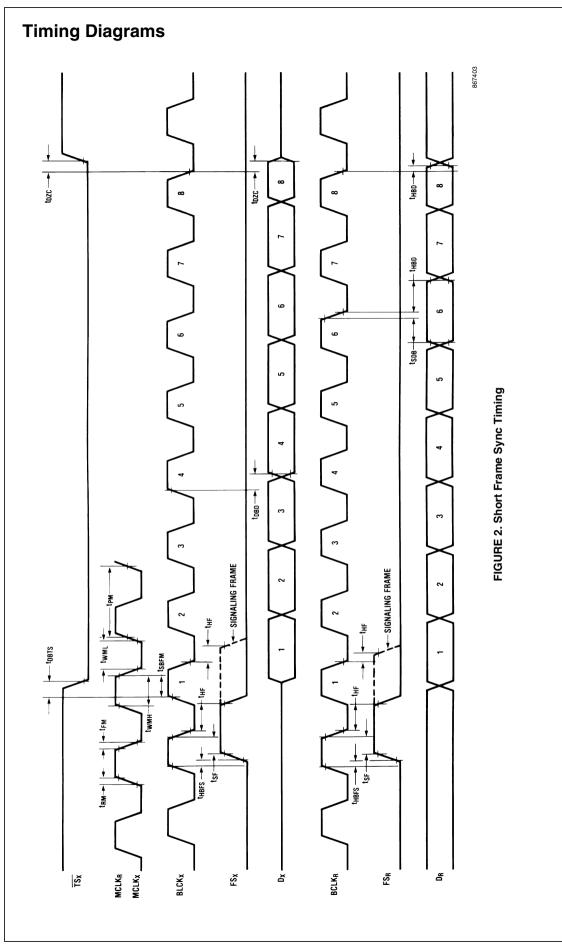
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Symbol	Parameter	Conditions	Min	Тур	Max	Units
1/t _{PM}	Frequency of Master Clocks	Depends on the Device Used and the		1.536		MHz
		BCLK _R /CLKSEL Pin.		1.544		MHz
		MCLK _X and MCLK _R		2.048		MHz
t _{RM}	Rise Time of Master Clock	MCLK _X and MCLK _R			50	ns
t _{FM}	Fall Time of Master Clock	MCLK _x and MCLK _R			50	ns
t _{PB}	Period of Bit Clock		485	488	15725	ns
t _{RB}	Rise Time of Bit Clock	BCLK _X and BCLK _R			50	ns
t _{FB}	Fall Time of Bit Clock	BCLK _X and BCLK _R			50	ns
t _{WMH}	Width of Master Clock High	MCLK _x and MCLK _R	160			ns
t _{WML}	Width of Master Clock Low	MCLK _x and MCLK _R	160			ns
t _{SBFM}	Set-Up Time from BCLK _X High to MCLK _X Falling Edge	First Bit Clock after Short Frame the Leading Edge	100			ns
	······································	of FS _x Long Frame	125			
t _{SFFM}	Setup Time from FS_X High to $MCLK_X$ Falling Edge	Long Frame Only	100			ns
t _{WBH}	Width of Bit Clock High	V _{IH} =2.2V	160			ns
t _{WBL}	Width of Bit Clock Low	V _{IL} =0.6V	160			ns
t _{HBFL}	Holding Time from Bit Clock Low to Frame Sync	Long Frame Only	0			ns
t _{HBFS}	Holding Time from Bit Clock High to Frame Sync	Short Frame Only	0			ns
t _{SFB}	Set-Up Time from Frame Sync to Bit Clock Low	Long Frame Only	115			ns
t _{DBD}	Delay Time from BCLK _X High to Data Valid	Load=150 pF plus 2 LSTTL Loads	0		140	ns
t _{DBTS}	Delay Time to $\overline{TS_X}$ Low	Load=150 pF plus 2 LSTTL Loads			140	ns
t _{DZC}	Delay Time from BCLK _X Low to Data Output Disabled	C _L =0 pF to 150 pF	50		165	ns
t _{DZF}	Delay Time to Valid Data from FS_X or $BCLK_X$, Whichever Comes Later	C _L =0 pF to 150 pF	20		165	ns
t _{SDB}	Set-Up Time from D _R Valid to BCLK _{R/X} Low		50			ns
t _{HBD}	Hold Time from BCLK _{R/X} Low to D _R Invalid		50			ns
t _{SF}	Set-Up Time from FS _{X/R} to BCLK _{X/R} Low	Short Frame Sync Pulse (1 Bit Clock Period Long)	50			ns
t _{HF}	Hold Time from BCLK _{X/R} Low to FS _{X/R} Low	Short Frame Sync Pulse (1 Bit Clock Period Long)	100			ns
t _{HBFI}	Hold Time from 3rd Period of Bit Clock Low to Frame Sync (FS _x or FS _R)	Long Frame Sync Pulse (from 3 to 8 Bit Clock Periods Long)	100			ns
t _{WFL}	Minimum Width of the Frame Sync Pulse (Low Level)	64k Bit/s Operating Mode	160			ns

Note 1: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

Note 2: $I_{\rm CC0}$ and $I_{\rm BB0}$ are measured after first achieving a power-up state.

ТР3054-Х, ТР3057-Х



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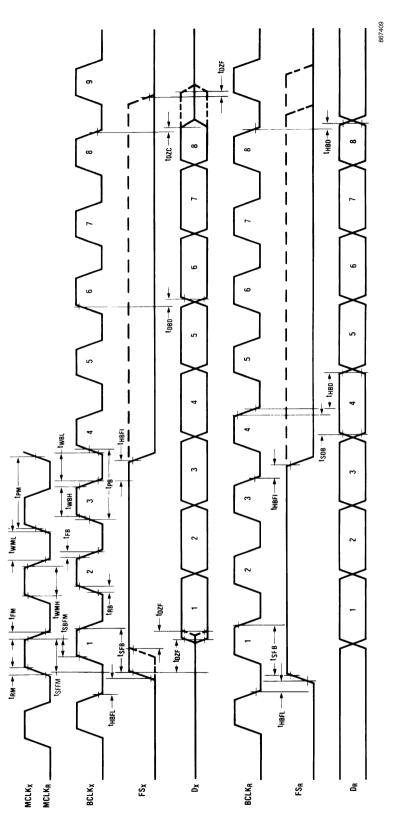


FIGURE 3. Long Frame Sync Timing

Transmission Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for $V_{CC} = +5.0V \pm 5\%$, $V_{BB} = -5.0V \pm 5\%$; $T_A = -40^{\circ}C$ to +85°C by correlation with 100% electrical testing at $T_A = 25^{\circ}C$. All other limits are assured by correlation with other production tests and/or product design and characterization. GNDA = 0V, f = 1.02 kHz, $V_{IN} = 0$ dBm0, transmit input amplifier connected for unity gain non inverting. Typicals are specified at $V_{CC} = +5.0V$, $V_{BB} = -5.0V$, $T_A = 25^{\circ}C$.

Symbol	Parameter	Conditions	Min	Тур	Max	Units
AMPLITU	DE RESPONSE		-	-		
	Absolute Levels	Nominal 0 dBm0 Level is 4 dBm				
	(Definition of nominal gain)	(600Ω)				
		0 dBm0		1.2276		Vrms
t _{MAX}		Max Overload Level				
-MAX		TP3054 (3.17 dBm0)		2.501		V _{PK}
		TP3057 (3.14 dBm0)		2.492		V _{PK}
<u> </u>	Transmit Cain Abasluta	$T_{A}=25^{\circ}C, V_{CC}=5V, V_{BB}=-5V$		2.402		* PK
G _{XA}	Transmit Gain, Absolute		0.15		0.15	ЧD
		Input at GS _x =0 dBm0 at 1020 Hz	-0.15		0.15	dB
G _{XR}	Transmit Gain, Relative to G _{XA}	f=16 Hz			-40	dB
		f=50 Hz			-30	dB
		f=60 Hz			-26	dB
		f=200 Hz	-1.8		-0.1	dB
		f=300 Hz-3000 Hz	-0.15		0.15	dB
		f=3152 Hz	-0.15		0.20	dB
		f=3300 Hz	-0.35		0.1	dB
		f=3400 Hz	-0.7		0	dB
		f=4000 Hz			-14	dB
		f=4600 Hz and Up, Measure			-32	dB
		Response from 0 Hz to 4000 Hz				
G _{XAT}	Absolute Transmit Gain Variation	Relative to G _{XA}	-0.15		0.15	dB
	with Temperature					
G _{XAV}	Absolute Transmit Gain Variation	Relative to G _{XA}	-0.05		0.05	dB
	with Supply Voltage					
G _{XRL}	Transmit Gain Variations with	Sinusoidal Test Method				
	Level	Reference Level=-10 dBm0				
		$VF_{x}I^{+}=-40 \text{ dBm0 to }+3 \text{ dBm0}$	-0.2		0.2	dB
		VF _x I+=-50 dBm0 to -40 dBm0	-0.4		0.4	dB
		$VF_{x}I^{+}=-55 \text{ dBm0 to } -50 \text{ dBm0}$	-1.2		1.2	dB
G _{RA}	Receive Gain, Absolute	$T_{A}=25^{\circ}C, V_{CC}=5V, V_{BB}=-5V$				
u _{RA}	neceive dain, Absolute	Input=Digital Code Sequence				
		for 0 dBm0 Signal at 1020 Hz	-0.20		0.20	dB
	Dessive Coin Deletive to C	-				
G _{RR}	Receive Gain, Relative to G _{RA}	f=0 Hz to 3000 Hz	-0.15		0.15	dB
		f=3300 Hz	-0.35		0.1	dB
		f=3400 Hz	-0.7		0	dB
_		f=4000 Hz			-14	dB
G _{RAT}	Absolute Receive Gain Variation	Relative to G _{RA}	-0.15		0.15	dB
	with Temperature				L	
G _{RAV}	Absolute Receive Gain Variation	Relative to G _{RA}	-0.05		0.05	dB
	with Supply Voltage					
G _{RRL}	Receive Gain Variations with	Sinusoidal Test Method; Reference				
	Level	Input PCM Code Corresponds to an				
		Ideally Encoded				
		PCM Level =-40 dBm0 to +3 dBm0	-0.2		0.2	dB
		PCM Level =-50 dBm0 to -40 dBm0	-0.4		0.4	dB
		PCM Level =-55 dBm0 to -50 dBm0	-1.2		1.2	dB

Symbol	Parameter	Conditions	Min	Тур	Max	Units
V _{RO}	Receive Output Drive Level	R _L =600Ω	-2.5		2.5	V
ENVELOF	PE DELAY DISTORTION WITH FREQ	UENCY	•			.
D _{XA}	Transmit Delay, Absolute	f=1600 Hz		290	315	μs
D _{XR}	Transmit Delay, Relative to D _{XA}	f=500 Hz-600 Hz		195	220	μs
		f=600 Hz-800 Hz		120	145	μs
		f=800 Hz-1000 Hz		50	75	μs
		f=1000 Hz–1600 Hz		20	40	μs
		f=1600 Hz-2600 Hz		55	75	μs
		f=2600 Hz-2800 Hz		80	105	μs
		f=2800 Hz-3000 Hz		130	155	μs
D _{RA}	Receive Delay, Absolute	f=1600 Hz		180	200	μs
D _{RR}	Receive Delay, Relative to D _{BA}	f=500 Hz-1000 Hz	-40	-25		μs
- нн		f=1000 Hz-1600 Hz	-30	-20		μs
		f=1600 Hz-2600 Hz		70	90	μs
		f=2600 Hz-2800 Hz		100	125	μs
		f=2800 Hz-3000 Hz		145	175	
NOISE				140	1/0	μs
N _{xc}	Transmit Noise, C Message	TP3054		12	16	dBrnC0
▼ XC	Weighted	(<i>Note 3</i>)		12		
N _{XP}	Transmit Noise, P Message	TP3057		-74	-67	dBm0p
™ XP	Weighted	-		-/-		
N _{RC}	Receive Noise, C Message	PCM Code is Alternating				
RC	Weighted Positive and Negative Zero — TP3054			8	11	dBrnC
N _{RP}	Receive Noise, P Message	TP3057 PCM Code Equals Positive		0		abinot
RP	Weighted	Zero —		-82	-79	dBm0p
N _{RS}	Noise, Single Frequency	f=0 kHz to 100 kHz, Loop Around		-02	-53	dBm0
*RS		Measurement, VF _x I+=0 Vrms			-50	
PPSR _x	Positive Power Supply Rejection,	$V_{cc}=5.0 V_{Dc}+100 \text{ mVrms}$				
rron _x	Transmit	f=0 kHz-50 kHz (Note 4)	40			dBC
NPSR _x	Negative Power Supply Rejection,	$V_{BB} = -5.0 V_{DC} + 100 \text{ mVrms}$	40			
NEONX	Transmit	f=0 kHz-50 kHz (<i>Note 4</i>)	40			dBC
PPSR _R	Positive Power Supply Rejection,	PCM Code Equals Positive Zero				ub0
rr on _R	Receive	V_{cc} =5.0 V_{Dc} +100 mVrms				
		Measure VF _B 0				
		f=0 Hz-4000 Hz	38			dBC
		f=4 kHz-25 kHz	38			dB
		f=25 kHz-50 kHz	35			dB
NPSR _R	Negative Power Supply Rejection,	PCM Code Equals Positive Zero				
	Receive	V_{BB} =-5.0 V_{DC} +100 mVrms				
		Measure VF _B 0				
		f=0 Hz-4000 Hz	38			dBC
		f=4 kHz–25 kHz	38			dB
		f=25 kHz-50 kHz	35			dB
SOS	Spurious Out-of-Band Signals	Loop Around Measurement, 0 dBm0,			-30	dB
	at the Channel Output	300 Hz to 3400 Hz Input PCM Code				
		Applied at D _R .			1	
		4600 Hz–7600 Hz			-30	dB
		7600 Hz–8400 Hz			-40	dB
		8400 Hz–100,000 Hz			-30	dB

TP3054-X, TP3057-X

Symbol	Parameter	Condition	s	Min	Тур	Max	Unit
DISTOR	TION	•		•			L
STD _{X.}	Signal to Total Distortion	Sinusoidal Test Method (Note 6)				
STD _R	Transmit or Receive	Level=3.0 dBm0		33			dB
	Half-Channel	=0 dBm0 to -30 dB	m0	36			dB
		=-40 dBm0	XMT	28			dB
			RCV	29			dB
		=-55 dBm0	XMT	13			dB
			RCV	14			dB
SFD _x	Single Frequency Distortion,					-43	dl
A	Transmit						
SFD _R	Single Frequency Distortion,					-43	dl
	Receive						
IMD Intermodulation Distortion		Loop Around Measureme	ent,			-41	dl
		VF _X I+=-4 dBm0 to -21 dl	Bm0, Two				
		Frequencies in the Range	e				
		300 Hz–3400 Hz					
CROSST	ALK				-	-	
CT _{X-R}	Transmit to Receive Crosstalk,	f=300 Hz-3400 Hz			-90	-70	dE
	0 dBm0 Transmit Level	D _R =Quiet PCM Code (No	ote 6)				
CT _{R-X}	Receive to Transmit Crosstalk,	f=300 Hz–3400 Hz, VF _X I=	=Multitone		-90	-70	dE
	0 dBm0 Receive Level	(Note 4)					
Enc	oding Format at D _x Ou	-					
		TP3054			TP3057		
		µ-Law			A-Law		

					054 .aw								8057 Law			
						(Inc	ludes	Ever	n Bit I	nvers	ion)					
V _{IN} (at GS _X)=+Full-Scale	1	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0
V _{IN} (at GS _X)=0V	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1
	0	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1
V _{IN} (at GS _X)=-Full-Scale	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0

Note 3: Measured by extrapolation from the distortion test result at -50 dBm0.

Note 4: $PPSR_X$, $NPSR_X$, and CT_{R-X} are measured with a -50 dBm0 activation signal applied to VF_XI^* .

Note 5: TP3054/57 are measured using C message weighted filter for μ -law and psophometric weighted filter for A-law.

Note 6: CT_{X-R} @ 1.544 MHz MCLK_{X} freq. is –70 dB max. 50% $\pm 5\%$ BCLK_{X} duty cycle.

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Applications Information

POWER SUPPLIES

While the pins of the TP3050 family are well protected against electrical misuse, it is recommended that the standard CMOS practice be followed, ensuring that ground is connected to the device before any other connections are made. In applications where the printed circuit board may be plugged into a "hot" socket with power and clocks already present, an extra long ground pin in the connector should be used.

All ground connections to each device should meet at a common point as close as possible to the GNDA pin. This minimizes the interaction of ground return currents flowing through a common bus impedance. 0.1 μ F supply decoupling capacitors should be connected from this common ground point to V_{CC} and V_{BB}, as close to device pins as possible.

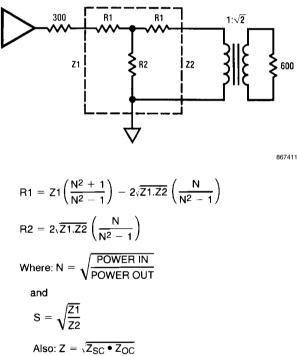
For best performance, the ground point of each CODEC/FIL-TER on a card should be connected to a common card ground in star formation, rather than via a ground bus.

T-Pad Attenuator

This common ground point should be decoupled to V_{CC} and V_{BB} with 10 μF capacitors.

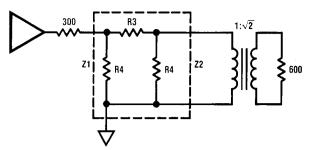
RECEIVE GAIN ADJUSTMENT

For applications where a TP3050 family CODEC/filter receive output must drive a 600Ω load, but a peak swing lower than $\pm 2.5V$ is required, the receive gain can be easily adjusted by inserting a matched T-pad or π -pad at the output. *Table 2* lists the required resistor values for 600Ω terminations. As these are generally non-standard values, the equations can be used to compute the attenuation of the closest practical set of resistors. It may be necessary to use unequal values for the R1 or R4 arms of the attenuators to achieve a precise attenuation. Generally it is tolerable to allow a small deviation of the input impedance from nominal while still maintaining a good return loss. For example a 30 dB return loss against 600Ω is obtained if the output impedance of the attenuator is in the range 282Ω to 319Ω (assuming a perfect transformer).



Where Z_{SC} = impedance with short circuit termination and Z_{OC} = impedance with open circuit termination

π-Pad Attenuator



867412

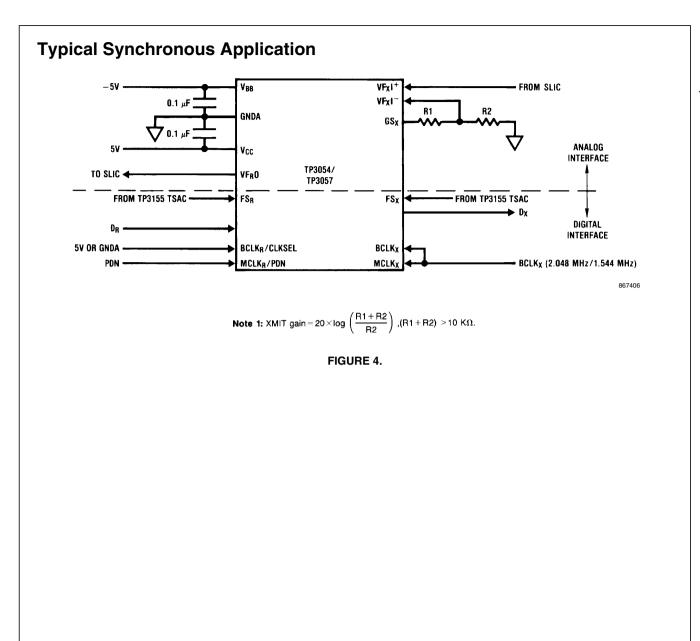
Note: See Application Note 370 for further details.

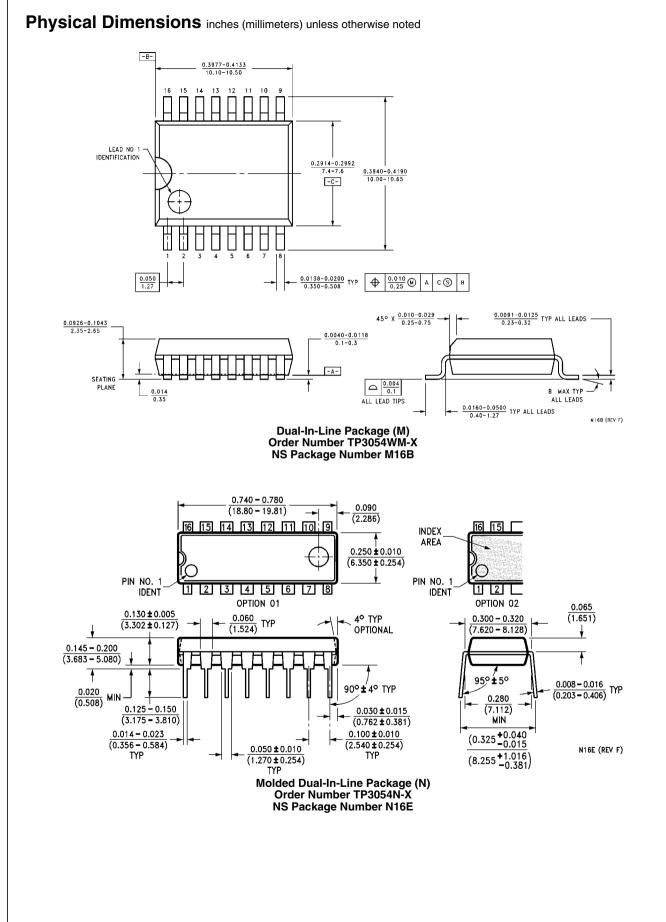
$$R3 = \sqrt{\frac{Z1.Z2}{2}} \left(\frac{N^2 - 1}{N}\right)$$
$$R3 = Z1 \left(\frac{N^2 - 1}{N^2 - 2NS + 1}\right)$$

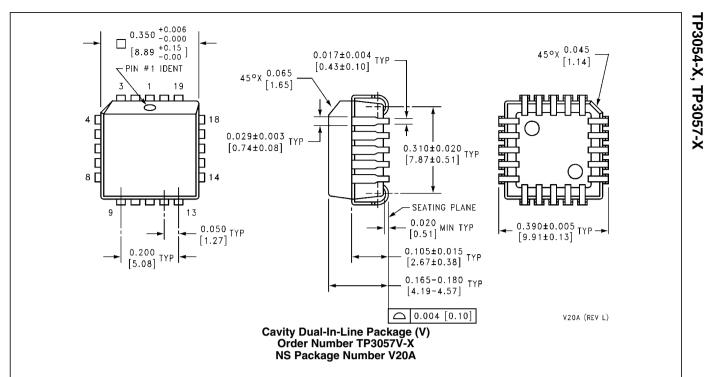
TABLE 2. Attentuator Tables for Z1=Z2=300 Ω (All Values in Ω)

dB	R1	R2	R3	R4
0.1	1.7	26k	3.5	52k
0.2	3.5	13k	6.9	26k
0.3	5.2	8.7k	10.4	17.4k
0.4	6.9	6.5k	13.8	13k
0.5	8.5	5.2k	17.3	10.5k
0.6	10.4	4.4k	21.3	8.7k
0.7	12.1	3.7k	24.2	7.5k
0.8	13.8	3.3k	27.7	6.5k
0.9	15.5	2.9k	31.1	5.8k
1.0	17.3	2.61	34.6	5.2k
2	34.4	1.3k	70	2.6k
3	51.3	850	107	1.8k
4	68	650	144	1.3k
5	84	494	183	1.1k
6	100	402	224	900
7	115	380	269	785
8	379	284	317	698
9	143	244	370	630
10	156	211	427	527
11	168	184	490	535
12	180	161	550	500
13	190	142	635	473
14	200	125	720	450
15	210	110	816	430
16	218	98	924	413
18	233	77	1.17k	386
20	246	61	1.5k	366

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Notes

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