

Stereo Audio DAC with USB Interface, Single-Ended Headphone Output and S/PDIF Output

Check for Samples: PCM2704C, PCM2705C, PCM2706C, PCM2707C

FEATURES

- · On-Chip USB Interface:
 - No Dedicated Device Driver Needed
 - Full-Speed Transceivers
 - Fully Compliant with USB 1.1 Specification
 - Certified by USB-IF
 - Partially Programmable Descriptors
 - Adaptive Isochronous Transfer for Playback
 - Bus-Powered or Self-Powered Operation
- Sampling Rates: 32 kHz, 44.1 kHz, 48 kHz
- On-Chip Clock Generator with Single 12-MHz Clock Source
- Single Power Supply:
 - Bus-Powered: 5 V, Typical (V_{BUS})
 - Self-Powered: 3.3 V, Typical
- 16-Bit Delta-Sigma Stereo DAC
 - Analog Performance at 5 V (Bus-Powered),
 3.3 V (Self-Powered):
 - $\quad \text{THD+N: 0.006\% R}_{L} > \text{10 k}\Omega, \\ \text{Self-Powered}$
 - THD+N: 0.025% R_1 = 32 Ω
 - SNR = 98 dB
 - Dynamic Range: 98 dB
 - P_O = 12 mW, R_L = 32 Ω
 - Oversampling Digital Filter
 - Passband Ripple = ±0.04 dB
 - Stop-Band Attenuation = -50 dB
 - Single-Ended Voltage Output
 - Analog LPF Included
- Multiple Functions:
 - Up to Eight Human Interface Device (HID)

Interfaces (Model and Setting Dependent)

- Suspend Flag
- S/PDIF Out with SCMS
- External ROM Interface (PCM2704C/6C)
- Serial Programming Interface (PCM2705C/7C)
- I²S™ Interface (Selectable on PCM2706C/7C)
- · Packages:
 - 28-Pin SSOP (PCM2704C/5C)
 - 32-Pin TQFP (PCM2706C/7C)

APPLICATIONS

- USB Headphones
- USB Audio Speaker
- USB CRT/LCD Monitor
- USB Audio Interface Box
- USB-Featured Consumer Audio Product

DESCRIPTION

The PCM2704C/5C/6C/7C are TI's single-chip USB stereo audio digital-to-analog converters (DACs) with USB-compliant full-speed protocol controller and S/PDIF. The USB-protocol controller works with no software code, but USB descriptors can be modified in some areas (for example, vendor ID/product ID) through the use of an external ROM (PCM2704C/6C) serial peripheral interface SPI™)(PCM2705C/7C). The PCM2704C/5C/6C/7C also employ SpAct™ architecture, TI's unique system that recovers the audio clock from USB packet data. On-chip analog phase-locked loops (PLLs) with SpAct enable playback with low clock jitter.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

For the most current specification and package information, refer to the Package Option Addendum located at the end of this data sheet or see the respective device product folders at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range unless otherwise noted

		VALUE	UNIT
Cupply voltage	V _{BUS}	-0.3 to 6.5	V
Supply voltage	V _{CCP} , V _{CCL} , V _{CCR} , V _{DD}	-0.3 to 4	V
Supply voltage differences	V _{CCP} , V _{CCL} , V _{CCR} , V _{DD}	±0.1	V
Ground voltage differences	PGND, AGNDL, AGNDR, DGND, ZGND	±0.1	V
	HOST	-0.3 to 6.5	V
Digital input voltage	D+, D-, HID0/MS, HID1/MC, HID2/MD, XTI, XTO, DOUT, SSPND, CK, DT, PSEL, FSEL, TEST, TEST0, TEST1, FUNC0, FUNC1, FUNC2, FUNC3	-0.3 to (V _{DD} + 0.3) < 4	V
	V _{COM}	-0.3 to $(V_{CCP} + 0.3) < 4$	V
Analog input voltage	V _{OUT} R	-0.3 to (V _{CCR} + 0.3) < 4	V
	V _{OUT} L	-0.3 to $(V_{CCL} + 0.3) < 4$	V
Input current (any pins except	ot supplies)	±10	mA
Ambient temperature under bias		-40 to +125	°C
Storage temperature		-55 to +150	°C
Junction temperature		+150	°C
Package temperature (IR ref	low, peak)	+260	°C

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range.

		MIN	NOM	MAX	UNIT
Cumply voltage	V _{BUS}	4.35	5	5.25	V
Supply voltage	$V_{CCP}, V_{CCL}, V_{CCR}, V_{DD}$	3	3.3	3.6	V
Digital input logic level	TTL	-compatible			
Digital input clock frequency		11.994	12	12.006	MHz
Analog output load resistance		16	32		Ω
Analog output load capacitance			100	pF	
Digital output load capacitance			20	pF	
Operating free-air temperature, T _A		-25		85	°C

STRUMENTS



ELECTRICAL CHARACTERISTICS

All specifications at $T_A = +25$ °C, $V_{BUS} = 5$ V, $f_S = 44.1$ kHz, $f_{IN} = 1$ kHz, and 16-bit data (unless otherwise noted).

	PARAMETER		The state of the s		OB, PCM270 JT, PCM270		UNIT	
				MIN	TYP	MAX		
DIGITAL	L INPUT/OUTPUT							
	Host interface			Apply USB rev	vision 1.1, fu	ıll-speed		
	Audio data format			USB isochro	onous data f	ormat		
INPUT L	_OGIC							
V_{IH}				2		3.3		
V_{IL}	Input logic level			-0.3		8.0	V	
$V_{IH}^{(1)}$				2		5.5	V_{DC}	
$V_{IL}^{(1)}$				-0.3		8.0		
$I_{IH}^{(2)}$			$V_{IN} = 3.3 V$			±10		
$I_{IL}^{\ (2)}$	Input logic current		$V_{IN} = 0 V$			±10		
I _{IH}	Input logic current		$V_{IN} = 3.3 V$		65	100	μΑ	
I _{IL}			$V_{IN} = 0 V$			±10		
OUTPU	T LOGIC							
V _{OH} ⁽³⁾			$I_{OH} = -2 \text{ mA}$	2.8				
$V_{OL}^{(3)}$	Output logic level		$I_{OL} = 2 \text{ mA}$			0.3	V_{DC}	
V _{OH}	Output logic level		$I_{OH} = -2 \text{ mA}$	2.4				
V_{OL}			$I_{OL} = 2 \text{ mA}$			0.4		
CLOCK	FREQUENCY							
	Input clock frequency,	XTI		11.994	12	12.006	MHz	
f _S	Sampling frequency			32,	44.1, 48		kHz	
DAC CH	HARACTERISTICS			•		·		
	Resolution				16		Bits	
	Audio data channel				1, 2		Channel	
DC ACC	CURACY							
	Gain mismatch, chann	el-to-channel			±2	±8	% of FSR	
	Gain error				±2	±8	% of FSR	
	Bipolar zero error				±3	±6	% of FSR	
DYNAM	IC PERFORMANCE (4)							
		Line (5)	$R_L > 10 \text{ k}\Omega$, self-powered, $V_{OUT} = 0 \text{ dB}$		0.006	0.01	%	
THD+N	HD+N Total harmonic distortion + noise	Lifte (-/	$R_L > 10 \text{ k}\Omega$, bus-powered, $V_{OUT} = 0 \text{ dB}$		0.012	0.02	%	
		Headphone	$R_L = 32 \Omega$, self-/ bus-powered, $V_{OUT} = 0 dB$		0.025		%	
THD+N	Total harmonic distortion	on + noise	$V_{OUT} = -60 \text{ dB}$		2		%	
	Dynamic range		EIAJ, A-weighted	90	98		dB	
SNR	Signal-to-noise ratio		EIAJ, A-weighted	90	98		dB	
	Channel separation			60	70		dB	

⁽¹⁾ HOST pin.

D+, D-, HOST, TEST, TEST0, TEST1, DT, PSEL, FSEL, XTI pins. FUNC0, FUNC1, FUNC2 pins.

f_{IN} = 1 kHz, using the System Two™ Cascade audio measurement system by Audio Precision™ in RMS mode with a 20-kHz low-pass filter (LPF) and 400-Hz high-pass filter (HPF).

⁽⁵⁾ THD+N performance varies slightly, depending on the effective output load, including dummy load R7, R8 in Figure 34.



All specifications at $T_A = +25$ °C, $V_{BUS} = 5$ V, $f_S = 44.1$ kHz, $f_{IN} = 1$ kHz, and 16-bit data (unless otherwise noted).

PARAMET	ER	TEST CONDITIONS	PCM2704CDB, PCM2705CDB PCM2706CPJT, PCM2707CPJT			UNIT
			MIN	TYP	MAX	
NALOG OUTPUT						
Output voltage			0.55 V _C	_{CCL} , 0.55 V _{CC}	CR	V_{PP}
Center voltage			0	.5 V _{CCP}		V
Load impadance	Line	AC-coupling	10			kΩ
Load impedance	Headphone	AC-coupling	16	32		Ω
LDE fraguency roopen		-3 dB		140		kHz
LPF frequency respon-	Se	f = 20 kHz		-0.1		dB
IGITAL FILTER PERFORMAN	ICE					
Passband					0.454 f _S	Hz
Stop band			0.546 f _S			Hz
Passband ripple					±0.04	dB
Stop band attenuation	Stop band attenuation		-50			dB
Delay time				20/f _S		s
OWER SUPPLY REQUIREME	NTS					
	V _{BUS}	Bus-powered	4.35	5	5.25	V_{DC}
Voltage range	$V_{CCP}, V_{CCL}, V_{CCR}, V_{DD}$	Self-powered	3	3.3	3.6	
	Line	DAC operation		23	30	mA
Supply current	Headphone	DAC operation ($R_L = 32 \Omega$)		35	46	
	Line/headphone	Suspend mode (6)		150	190	μΑ
	Line	DAC operation		76	108	\^/
Power dissipation (self-powered)	Headphone	DAC operation ($R_L = 32 \Omega$)		116	166	mW
(Scii powerca)	Line/headphone	Suspend mode (6)		495	684	μW
_	Line	DAC operation		115	158	.c-144
Power dissipation (bus-powered)	Headphone	DAC operation ($R_L = 32 \Omega$)		175	242	mW
(bus-powereu)	Line/headphone	Suspend mode (6)		750	998	μW
Internal power-supply voltage (7)	V _{CCP} , V _{CCL} , V _{CCR} , V _{DD}	Bus-powered	3.2	3.35	3.5	V_{DC}
EMPERATURE RANGE	•	·			1	
Operating temperature)		-25		+85	°C

⁽⁶⁾ In USB suspended state.

⁽⁷⁾ V_{DD}, V_{CCP}, V_{CCL}, V_{CCR} pins. These pins work as output pins of internal power supply for bus-powered operation.



THERMAL INFORMATION

	40	PCM2704C, PCM2705C	
	THERMAL METRIC ⁽¹⁾	DB	UNITS
		32 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	68.2	
θ_{JCtop}	Junction-to-case (top) thermal resistance	27.2	
θ_{JB}	Junction-to-board thermal resistance	29.5	°C/W
ΨЈТ	Junction-to-top characterization parameter	2.7	C/VV
ΨЈВ	Junction-to-board characterization parameter	29.1	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	

⁽¹⁾ For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

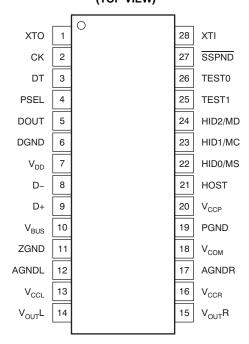
THERMAL INFORMATION

	w	PCM2706C, PCM2707C	
	THERMAL METRIC ⁽¹⁾	PJT	UNITS
		32 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	TBD	
θ_{JCtop}	Junction-to-case (top) thermal resistance	TBD	
θ_{JB}	Junction-to-board thermal resistance	TBD	°C/W
ΨЈТ	Junction-to-top characterization parameter	TBD	C/VV
ΨЈВ	Junction-to-board characterization parameter	TBD	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	TBD	

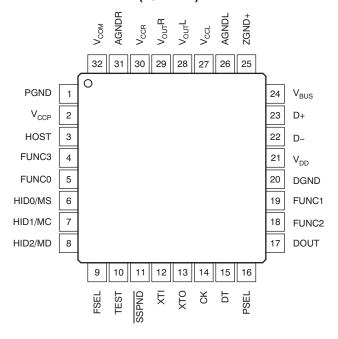
⁽¹⁾ For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

DEVICE INFORMATION

PCM2704C, PCM2705C DB PACKAGE (TOP VIEW)



PCM2706C, PCM2707C PJT PACKAGE (TOP VIEW)



Instruments



Table 1. Pin Descriptions: DB Package (PCM2704C/PCM2705C)

TERMINA	\L		
NAME	NO.	I/O	DESCRIPTION
AGNDL	12	_	Analog ground for headphone amplifier of L-channel
AGNDR	17	_	Analog ground for headphone amplifier of R-channel
СК	2	0	Clock output for external ROM (PCM2704C). Must be left open (PCM2705C).
D+	9	I/O	USB differential input/output plus ⁽¹⁾
D-	8	I/O	USB differential input/output minus ⁽¹⁾
DGND	6	_	Digital ground
DOUT	5	0	S/PDIF output
DT	3	I/O	Data input/output for external ROM (PCM2704C). Must be left open with pull-up resistor (PCM2705C). (1)
HID0/MS	22	I	HID key state input (mute), active high (PCM2704C). MS input (PCM2705C). (2)
HID1/MC	23	I	HID key state input (volume up), active high (PCM2704C). MC input (PCM2705C). (2)
HID2/MD	24	I	HID key state input (volume down), active high (PCM2704C). MD input (PCM2705C). (2)
HOST	21	I	Host detection during self-powered operation (connect to V _{BUS}). Max power select during bus-powered operation (low: 100 mA, high: 500 mA). (3)
PGND	19	_	Analog ground for DAC, OSC, and PLL
PSEL	4	I	Power source select (low: self-power, high: bus-power) ⁽¹⁾
SSPND	27	0	Suspend flag, active low (low: suspend, high: operational)
TEST0	26	I	Test pin. Must be set high ⁽¹⁾
TEST1	25	I	Test pin. Must be set high ⁽¹⁾
V _{BUS}	10	_	Connect to USB power (V _{BUS}) for bus-powered operation. Connect to V _{DD} for self-powered operation.
V _{CCL}	13	—	Analog power supply for headphone amplifier of L-channel (4)
V _{CCP}	20	_	Analog power supply for DAC, OSC, and PLL ⁽⁴⁾
V _{CCR}	16	—	Analog power supply for headphone amplifier of R-channel (4)
V _{COM}	18	_	Common voltage for DAC (V _{CCP} /2). Connect decoupling capacitor to PGND.
V_{DD}	7	_	Digital power supply ⁽⁴⁾
V _{OUT} L	14	0	DAC analog output for L-channel
V _{OUT} R	15	0	DAC analog output for R-channel
XTI	28	I	Crystal oscillator input ⁽¹⁾
XTO	1	0	Crystal oscillator output
ZGND	11	_	Ground for internal regulator

LV-TTL level.

LV-TTL level with internal pulldown.

LV-TTL level, 5-V tolerant.

Connect decoupling capacitor to GND. Supply 3.3 V for self-powered applications.



Table 2. Pin Descriptions: PJT Package (PCM2706C/PCM2707C)

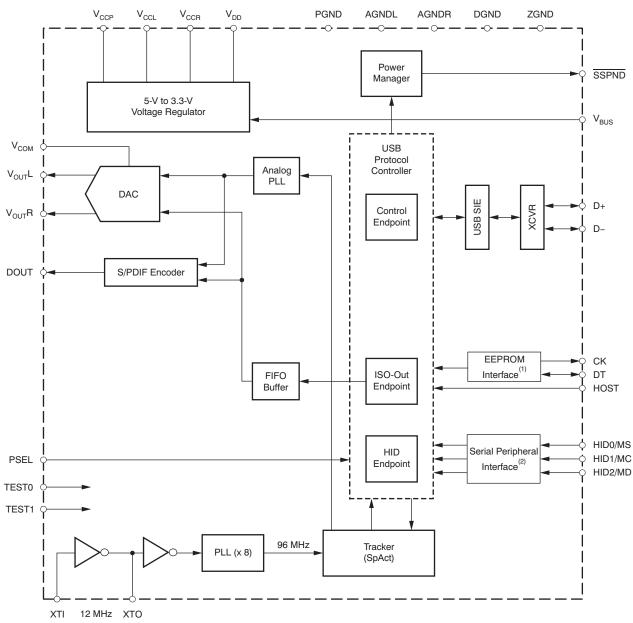
TERMINA	AL		
NAME	NO.	1/0	DESCRIPTION
AGNDL	26	_	Analog ground for headphone amplifier of L-channel
AGNDR	31	_	Analog ground for headphone amplifier of R-channel
СК	14	0	Clock output for external ROM (PCM2706C). Must be left open (PCM2707C).
D+	23	I/O	USB differential input/output plus ⁽¹⁾
D-	22	I/O	USB differential input/output minus ⁽¹⁾
DGND	20	_	Digital ground
DOUT	17	0	S/PDIF output/l ² S data output
DT	15	I/O	Data input/output for external ROM (PCM2706C). Must be left open with pull-up resistor (PCM2707C). (1)
FSEL	9	I	Function select (low: I ² S data output, high: S/PDIF output) ⁽¹⁾
FUNC0	5	I/O	HID key state input (next track), active high (FSEL = 1). I ² S LR clock output (FSEL = 0). (2)
FUNC1	19	I/O	HID key state input (previous track), active high (FSEL = 1). I ² S bit clock output (FSEL = 0). (2)
FUNC2	18	I/O	HID key state input (stop), active high (FSEL = 1). I ² S system clock output (FSEL = 0). (2)
FUNC3	4	I	HID key state input (play/pause), active high (FSEL = 1). I ² S data input (FSEL = 0). (2)
HID0/MS	6	ı	HID key state input (mute), active high (PCM2706C). MS input (PCM2707C). (2)
HID1/MC	7	ı	HID key state input (volume up), active high (PCM2706C). MC input (PCM2707C). (2)
HID2/MD	8	ı	HID key state input (volume down), active high (PCM2706C). MD input (PCM2707C). (2)
HOST	3	ı	Host detection during self-powered operation (connect to V _{BUS}). Max power select during bus-powered operation. (low: 100 mA, high: 500 mA). (3)
PGND	1	_	Analog ground for DAC, OSC, and PLL
PSEL	16	ı	Power source select (low: self-power, high: bus-power) ⁽¹⁾
SSPND	11	0	Suspend flag, active low (low: suspend, high: operational)
TEST	10	- 1	Test pin. Must be set high ⁽¹⁾
V _{BUS}	24	_	Connect to USB power (V _{BUS}) for bus-powered operation. Connect to V _{DD} for self-powered operation.
V _{CCL}	27	_	Analog power supply for headphone amplifier of L-channel (4)
V _{CCP}	2	_	Analog power supply for DAC, OSC, and PLL ⁽⁴⁾
V _{CCR}	30	_	Analog power supply for headphone amplifier of R-channel (4)
V_{COM}	32	_	Common voltage for DAC (V _{CCP} /2). Connect decoupling capacitor to PGND.
V_{DD}	21	_	Digital power supply ⁽⁴⁾
V _{OUT} L	28	0	DAC analog output for L-channel
V _{OUT} R	29	0	DAC analog output for R-channel
XTI	12	I	Crystal oscillator input ⁽¹⁾
XTO	13	0	Crystal oscillator output
ZGND	25		Ground for internal regulator

- (1) LV-TTL level.
- (2) LV-TTL level with internal pulldown.
- (3) LV-TTL level, 5-V tolerant.
- (4) Connect decoupling capacitor to GND. Supply 3.3 V for self-powered applications.

ISTRUMENTS

FUNCTIONAL BLOCK DIAGRAMS

PCM2704C/PCM2705C

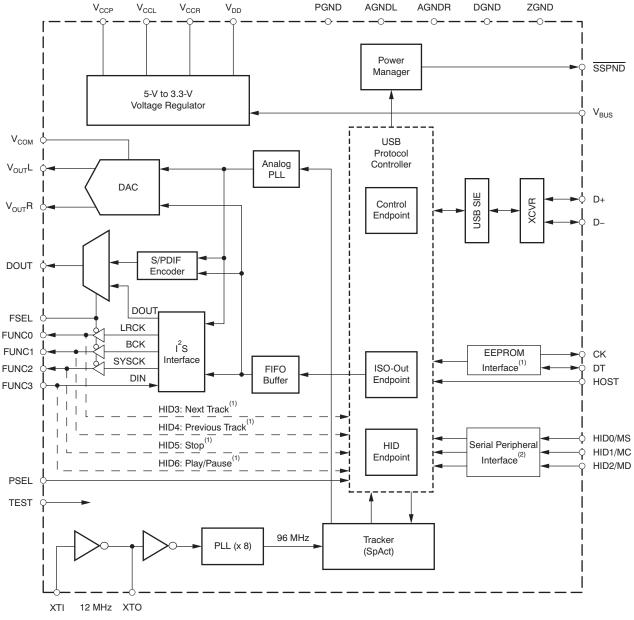


- (1) Applies to PCM2704CDB.
- (2) Applies to PCM2705CDB.

Figure 1.

PCM2706C/PCM2707C





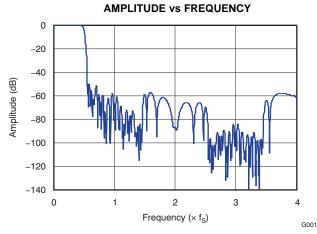
- (1) Applies to PCM2706CPJT.
- (2) Applies to PCM2707CPJT.

Figure 2.

TYPICAL CHARACTERISTICS: INTERNAL FILTER

All specifications at $T_A = 25$ °C, $V_{BUS} = 5$ V, $f_S = 44.1$ kHz, $f_{IN} = 1$ kHz, 16-bit data (unless otherwise noted).

DAC Digital Interpolation Filter Frequency Response



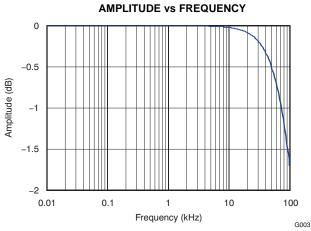
AMPLITUDE vs FREQUENCY

0.05
0.04
0.03
0.02
0.01
0.01
0.02
0.01
0.02
0.03
0.04
0.03
0.04
0.05
Frequency (× f_S)

Figure 3. Frequency Response

Figure 4. Passband Ripple

DAC Analog Low-Pass Filter Frequency Response





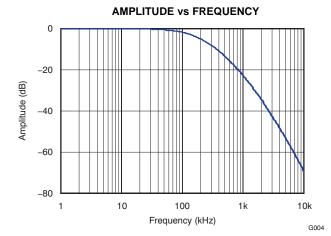


Figure 6. Stop Band Characteristics

TYPICAL CHARACTERISTICS: GENERAL

All specifications at $T_A = +25$ °C, $V_{BUS} = 5$ V, $f_S = 44.1$ kHz, $f_{IN} = 1$ kHz, and 16-bit data (unless otherwise noted).

TOTAL HARMONIC DISTORTION + NOISE vs FREE-AIR TEMPERATURE

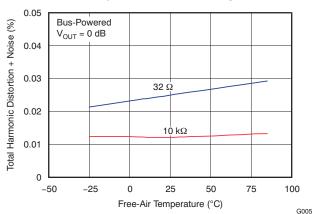


Figure 7.

TOTAL HARMONIC DISTORTION + NOISE VS FREE-AIR TEMPERATURE

NSTRUMENTS

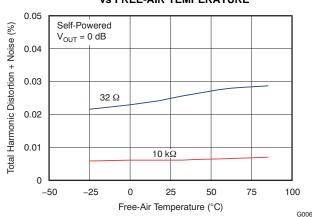


Figure 8.

TOTAL HARMONIC DISTORTION + NOISE vs SUPPLY VOLTAGE

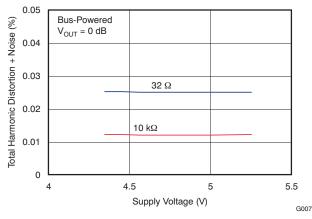


Figure 9.

TOTAL HARMONIC DISTORTION + NOISE vs SUPPLY VOLTAGE

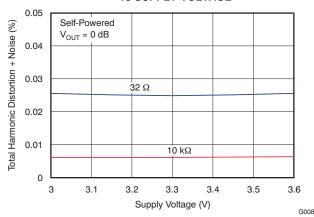
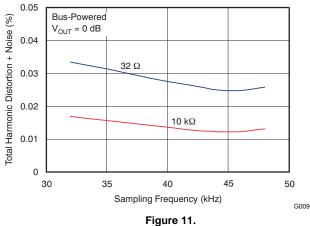


Figure 10.

TOTAL HARMONIC DISTORTION + NOISE vs SAMPLING FREQUENCY



TOTAL HARMONIC DISTORTION + NOISE vs SAMPLING FREQUENCY

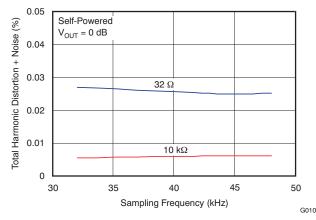


Figure 12.

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TYPICAL CHARACTERISTICS: GENERAL (continued)

All specifications at $T_A = +25$ °C, $V_{BUS} = 5$ V, $f_S = 44.1$ kHz, $f_{IN} = 1$ kHz, and 16-bit data (unless otherwise noted).

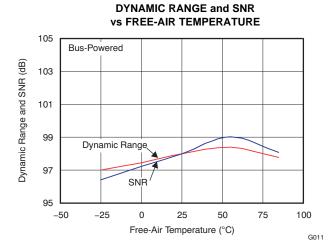
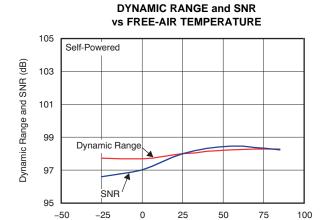


Figure 13.



Free-Air Temperature (°C)

Figure 14.



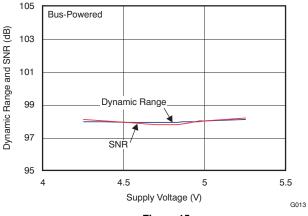


Figure 15.

DYNAMIC RANGE and SNR vs SUPPLY VOLTAGE

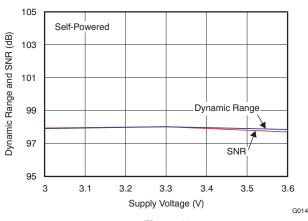


Figure 16.

DYNAMIC RANGE and SNR vs SAMPLING FREQUENCY

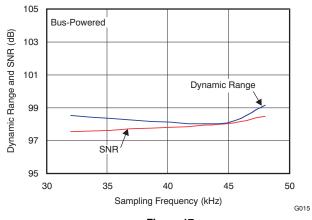


Figure 17.

DYNAMIC RANGE and SNR vs SAMPLING FREQUENCY

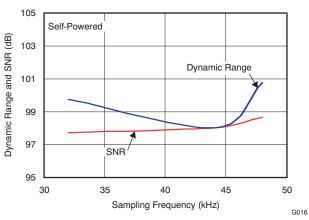
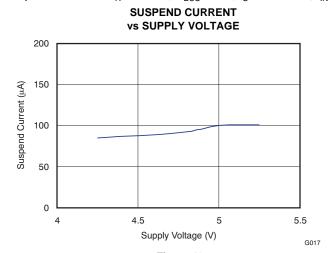


Figure 18.

TYPICAL CHARACTERISTICS: GENERAL (continued)

All specifications at $T_A = +25$ °C, $V_{BUS} = 5$ V, $f_S = 44.1$ kHz, $f_{IN} = 1$ kHz, and 16-bit data (unless otherwise noted).





NSTRUMENTS

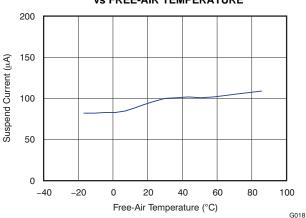


Figure 20.



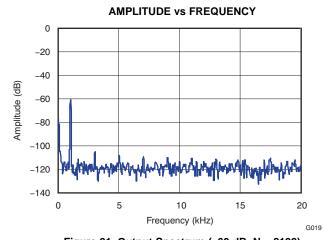


Figure 21. Output Spectrum (-60 dB, N = 8192)

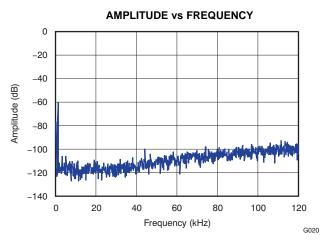


Figure 22. Output Spectrum (-60 dB, N = 8192)

DETAILED DESCRIPTION

Clock and Reset

For both USB and audio functions, the PCM2704C/5C/6C/7C require a 12-MHz (±500 ppm) clock that can be generated by the onboard oscillator using a 12-MHz crystal resonator. The 12-MHz crystal resonator must be connected to the XTI pin (pin 28 for the PCM2704C/5C, pin 12 for the PCM2706C/7C) and the XTO pin (pin 1 for the PCM2704C/5C, pin 13 for the PCM2706C/7C) with one large (1-MΩ) resistor and two small capacitors; the capacitance of these components depends on the specified load capacitance of the crystal resonator. An external clock can be supplied from XTI (pin 28 for the PCM2704C/5C, pin 12 for the PCM2706C/7C). If an external clock is supplied, XTO (pin 1 for the PCM2704C/5C, pin 13 for the PCM2706C/7C) must be left open. No clock disabling pin is provided; therefore, it is not recommended to use the external clock supply. SSPND (pin 27 for the PCM2704C/5C, pin 11 for the PCM2706C/7C) cannot use clock disabling.

The PCM2704C/5C/6C/7C have an internal power-on reset circuit, and it works automatically when V_{DD} (pin 7 for the PCM2704C/5C, pin 21 for the PCM2706C/7C) exceeds 2-V typical (1.6 V to 2.4 V), which is equivalent to V_{BUS} (pin 10 for the PCM2704C/5C, pin 24 for the PCM2706C/7C) exceeding 3-V typical for bus-powered applications. Approximately 700 μ s is required until an internal reset release occurs.

Operation Mode Selection

The PCM2704C/5C/6C/7C have the following mode-select pins.

Power Configuration Select/Host Detection

PSEL (pin 4 for the PCM2704C/5C, pin 16 for the PCM2706C/7C) is dedicated to selecting the power source. This selection affects the configuration descriptor. While in bus-powered operation, the maximum power consumption from V_{BUS} is determined by the HOST pin (pin 21 for the PCM2704C/5C, pin 3 for the PCM2706C/7C). For self-powered operation, the HOST pin must be connected to V_{BUS} of the USB bus with a pulldown resistor to detect attach and detach. (To avoid excessive suspend current, the pulldown should be a high-value resistor.) Table 3 summarizes the power configuration select options.

 PSEL
 DESCRIPTION

 0
 Self-powered

 1
 Bus-powered

 HOST
 DESCRIPTION

 0
 Detached from USB (self-powered)/100 mA (bus-powered)

 1
 Attached to USB (self-powered)/500 mA (bus-powered)

Table 3. Power Configuration Select

Function Select (PCM2706C/7C Only)

FSEL (pin 9) determines the function of the FUNC0–FUNC3 pins (pins 4, 5, 18, and 19) and DOUT (pin 17). When the I^2S interface is required, FSEL must be low. Otherwise, FSEL must be high. Table 4 lists the functionality of the FUNC0-FUNC3 pins, based on the FSEL pin.

Table 4. Function Select

FSEL	DOUT	FUNC0	FUNC1	FUNC2	FUNC3
0	Data out (I ² S)	LRCK (I ² S)	BCK (I ² S)	SYSCK (I ² S)	Data in (I ² S)
1	S/PDIF data	Next track (HID) (1)	Previous track (HID) (1)	Stop (HID) (1)	Play/pause (HID) (1)

(1) Valid on the PCM2706C only; no function assigned on the PCM2707C.



USB Interface

Control data and audio data are transferred to the PCM2704C/5C/6C/7C via the D+ pin (pin 9 for the PCM2704C/5C, pin 23 for the PCM2706C/7C) and D– pin (pin 8 for the PCM2704C/5C, pin 22 for the PCM2706C/7C). D+ should be pulled up with a 1.5-k Ω (±5%) resistor. To avoid back voltage in self-powered operation, the device must not provide power to the pull-up resistor on D+ while V_{BUS} of the USB port is inactive.

All data to/from the PCM2704C/5C/6C/7C are transferred at full speed. The information shown in Table 5 is provided in the device descriptor. Some parts of the device descriptor can be modified through external ROM (PCM2704C/6C) or SPI (PCM2705C/7C).

Table 5. Device Descriptor

DEVICE DESCRIPTOR	DESCRIPTION
USB revision	1.1 compliant
Device class	0x00 (device defined interface level)
Device subclass	0x00 (not specified)
Device protocol	0x00 (not specified)
Max packet size for endpoint 0	8 bytes
Vendor ID	0x08BB (default value, can be modified)
Product ID	0x27C4/0x27C5/0x27C6/0x27C7 (These values correspond to the model number, and the value can be modified.)
Device release number	1.0 (0x0100)
Number of configurations	1
Vendor strings	BurrBrown from Texas Instruments (default value, can be modified)
Product strings	USB AUDIO DAC (default value, can be modified)
Serial number	Not supported

The information given in Table 6 is contained in the configuration descriptor. Some parts of the configuration descriptor can be modified through external ROM (PCM2704C/6C) or SPI (PCM2705C/7C).

Table 6. Configuration Descriptor

CONFIGURATION DESCRIPTOR	DESCRIPTION
Interface	Three interfaces
Power attribute	0x80 or 0xC0 (bus-powered or self-powered, depending on PSEL; no remote wake up. This value can be modified.)
Max power	0x0A, 0x32, or 0xFA (20 mA for self-powered, 100 mA or 500 mA for bus-powered, depending on PSEL and HOST. This value can be modified.)

The information listed in Table 7 is contained in the string descriptor. Some parts of the string descriptor can be modified through external ROM (PCM2704C/6C) or SPI (PCM2705C/7C).

Table 7. String Descriptor

STRING DESCRIPTOR	DESCRIPTION
#0	0x0409
#1	BurrBrown from Texas Instruments (default value, can be modified)
#2	USB AUDIO DAC (default value, can be modified)

Device Configuration

Figure 23 illustrates the USB audio function topology. The PCM2704C/5C/6C/7C have three interfaces. Each interface is enabled by different alternative settings.

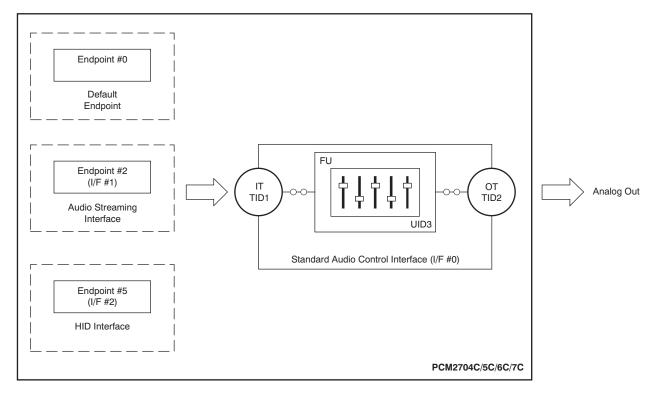


Figure 23. USB Audio Function Topology

Interface #0 (Default/Control Interface)

Interface #0 is the control interface. Setting #0 is the only possible setting for interface #0. Setting #0 describes the standard audio control interface. The audio control interface consists of a terminal. The PCM2704C/5C/6C/7C have three terminals:

- Input terminal (IT #1) for isochronous-out stream
- Output terminal (OT #2) for audio analog output
- Feature unit (FU #3) for DAC digital attenuator

Input terminal #1 is defined as a USB stream (terminal type 0x0101). Input terminal #1 can accept two-channel audio streams consisting of left and right channels. Output terminal #2 is defined as a speaker (terminal type 0x0301). Feature unit #3 supports these sound control features:

- Volume control
- Mute control

The built-in digital volume controller can be manipulated by an audio-class-specific request from 0 dB to -64 dB in steps of 1 dB. Changes are made by incrementing or decrementing one step (that is, 1 dB) for every $1/f_S$ time interval, until the volume level reaches the requested value. Each channel can be set to a separate value. The master volume control is not supported. A request to the master volume is stalled and ignored. The built-in digital mute controller can be manipulated by an audio-class-specific request. A master mute control request is acceptable. A mute control request to an individual channel is stalled and ignored. The digital volume control does not affect either the S/PDIF or I^2S outputs (PCM2706C/7C only).



Interface #1 (Isochronous-Out Interface)

Interface #1 is for the audio-streaming data-out interface. Interface #1 has the alternative settings described in Table 8. Alternative setting #0 is the zero-bandwidth setting. All other alternative settings are operational settings.

Table 8. Interface #1 Parameters

ALTERNATIVE SETTING		DATA FORM	TRANSFER MODE	SAMPLING RATE (kHz)						
00		Zero bandwidth								
01	16-bit	Stereo	Twos complement (PCM)	Adaptive	32, 44.1, 48					
02	16-bit	Mono	Twos complement (PCM)	Adaptive	32, 44.1, 48					

Interface #2 (HID Interface)

Interface #2 is the interrupt-data-in interface. The HID consumer control device consists of interface #2. Alternative setting #0 is the only possible setting for interface #2.

On the HID device descriptor, eight HID items are reported for any model, in any configuration.

HID Items Reported

Basic HID Operation

Interface #2 can report these three key statuses for any model. These statuses can be set by the HID0–HID2 pins (PCM2704C/6C) or the SPI port (PCM2705C/7C).

- Mute (0xE2)
- Volume up (0xE9)
- Volume down (0xEA)

Extended HID Operation (PCM2705/6/7)

By using the FUNC0–FUNC3 pins (PCM2706C) or the SPI port (PCM2705C/7C), these additional conditions can be reported to the host.

- Play/Pause (0xCD)
- Stop (0xB7)
- Previous (0xB6)
- Next (0xB5)

Auxiliary HID Status Report (PCM2705C/7C)

One additional HID status can be reported to the host though the SPI port. This status flag is defined by SPI command or external ROM. This definition must be described as on the report descriptor with a three-byte usage ID. *AL A/V Capture* (0x0193) is assigned as the default value for this status flag.

Endpoints

The PCM2704C/5C/6C/7C has three endpoints:

- Control endpoint (EP #0)
- Isochronous-out audio data-stream endpoint (EP #2)
- HID endpoint (EP #5)

The control endpoint is a default endpoint. The control endpoint controls all functions of the PCM2704C/5C/6C/7C by standard USB request and USB audio-class-specific request from the host. The isochronous-out audio data-stream endpoint is an audio sink endpoint that receives the PCM audio data. The isochronous-out audio data-stream endpoint accepts the adaptive transfer mode. The HID endpoint is an interrupt-in endpoint. The HID endpoint reports HID status every 10 ms.

The HID endpoint is defined as a consumer-control device. The HID function is designed as an independent endpoint from the isochronous-out endpoint. This configuration means that the effect of HID operation depends on the host software. Typically, the HID function controls the primary audio-out device.

DAC

The PCM2704C/5C/6C/7C have a DAC that uses an oversampling technique with 128-f_S, second-order, multi-bit noise shaping. This technique provides extremely low quantization noise in the audio band, and the built-in analog low-pass filter removes the high-frequency components of the noise-shaping signal. The DAC analog outputs, $V_{OUT}L$ and $V_{OUT}R$, are sent through the headphone amplifier and can provide 12 mW at 32 Ω as well as 1.8 V_{PP} into a 10-k Ω load.

Digital Audio Interface: S/PDIF Output

The PCM2704C/5C/6C/7C employ S/PDIF output. Isochronous-out data from the host are encoded to S/PDIF output DOUT, as well as to DAC analog outputs $V_{OUT}L$ and $V_{OUT}R$. The interface format and timing follow the IEC-60958 standard. Monaural data are converted to the stereo format at the same data rate. S/PDIF output is not supported in the I²S I/F enable mode. The implementation of this feature is optional. Note that it is the responsibility of the user to determine whether or not to implement this feature in the end application.

Channel Status Information

Channel status information is fixed, and includes consumer application, PCM mode, copyright, and digital/digital converter data. All other bits are fixed as 0s, except for the sample frequency, which is set automatically according to the data received through the USB.

Copyright Management

Digital audio data output always is encoded as original with SCMS control. Only one generation of digital duplication is allowed.

Digital Audio Interface: I²S Interface Output (PCM2706C/7C)

The PCM2706C and PCM2707C can support the I²S interface, which is enabled by the FSEL pin (pin 9). In the I²S interface-enabled mode, pins 4, 18, 19, 5, and 17 are assigned as DIN, SYSCK, BCK, LRCK, and DOUT, respectively. These pins provide digital output/input data in the 16-bit I²S format, which also is accepted by the internal DAC. I²S interface format and timing are shown in Figure 24, Figure 25, and Figure 26. Table 9 and Table 10 list the audio interface timing and audio clock timing characteristics, respectively.

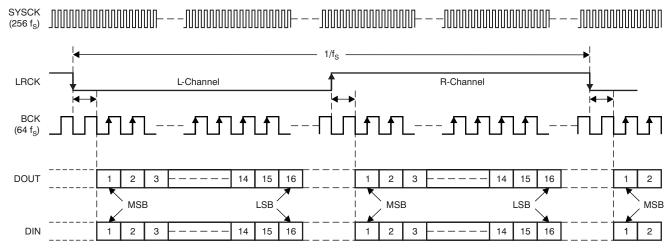


Figure 24. Audio Data Interface Format



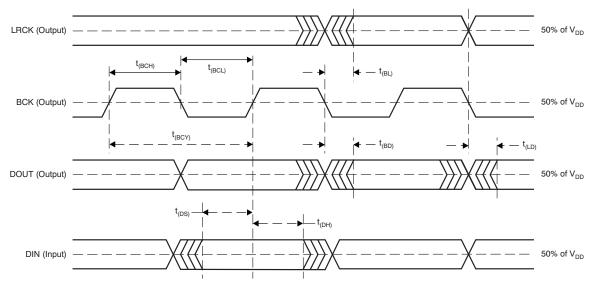


Figure 25. Audio Interface Timing

Table 9. Audio Interface Timing Characteristics (1)

SYMBOL	PARAMETER	MIN	MAX	UNIT
t _(BCY)	BCK pulse cycle time	300		ns
t _(BCH)	BCK pulse duration, high	100		ns
t _(BCL)	BCK pulse duration, low	100		ns
t _(BL)	LRCK delay time from BCK falling edge	-20	40	ns
t _(BD)	DOUT delay time from BCK falling edge	-20	40	ns
t _(LD)	DOUT delay time from LRCK edge	-20	40	ns
t _(DS)	DIN setup time	20		ns
t _(DH)	DIN hold time	20		ns

(1) Load capacitance of LRCK, BCK, and DOUT is 20 pF.

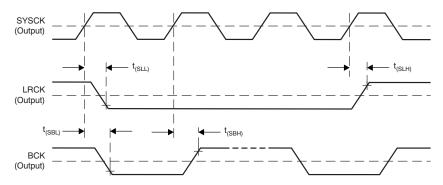


Figure 26. Audio Clock Timing

Table 10. Audio Clock Timing Characteristics (1)

SYMBOL	PARAMETER	MIN	MAX	UNIT
$t_{(SLL)}, t_{(SLH)}$	LRCK delay time from SYSCK rising edge	-5	10	ns
t _(SBL) , t _(SBH)	BCK delay time from SYSCK rising edge	- 5	10	ns

(1) Load capacitance is 20 pF.



DESCRIPTOR DATA MODIFICATION

The descriptor data can be modified through the I^2C^{TM} port by external ROM (PCM2704C/6C) or through the SPI port by an SPI host such as an MCU (PCM2705C/7C) under a particular configuration of the PSEL and HOST pins. Setting both the PSEL and the HOST pins high is necessary to modify the descriptor data; the D+ pin pull-up resistor must not be activated before programming the descriptor data through the external ROM or SPI port is completed. The descriptor data must be sent from an external ROM to the PCM2704C/6C or from the SPI host to the PCM2705C/7C in LSB first format, with a specified byte order. Additionally, the power attribute and max power contents must be consistent with the PSEL setting and the power usage from the USB V_{BUS} of the end application. Therefore, descriptor data modification in self-powered configuration (PSEL = low) is not supported.

External ROM Descriptor (PCM2704C/6C)

The PCM2704C/6C support an external ROM interface to override internal descriptors. Pin 3 (for the PCM2704C) or pin 15 (for the PCM2706C) is assigned as DT (serial data), and pin 2 (for the PCM2704C) or pin 14 (for the PCM2706C) is assigned as CK (serial clock) of the I²C interface when using the external ROM descriptor. Descriptor data are transferred from the external ROM to the PCM2704C/6C through the I²C interface the first time when the device is activate after a power-on reset. Before completing a read of the external ROM, the PCM2704C/6C reply with *NACK* for any USB command request from the host to the device itself. The descriptor data, which can be in the external ROM, must meet these parameters:

- String descriptors must be described in ANSI ASCII code (1 byte for each character).
- String descriptors are converted automatically to unicode strings for transmission to the host.
- The device address of the external ROM is fixed as 0xA0.

The data bits must be sent from LSB to MSB on the I^2C bus. This condition means that each byte of data must be stored with its bits in reverse order. A read operation is performed at a frequency of XTI/384 (approximately 30 kHz). The power attribute and max power contents must be consistent with the end application circuit configuration (the PSEL setting and the actual power usage from V_{BUS} of the USB connector); otherwise, it may cause improper or unexpected PCM2704C/6C operation.

The data must be stored from address 0x00 and must consist of 57 bytes, according to the parameters listed below:

- Vendor ID (2 bytes)
- · Product ID (2 bytes)
- Product string (16 bytes in ANSI ASCII code)
- Vendor string (32 bytes in ANSI ASCII code)
- Power attribute (1 byte)
- Max power (1 byte)
- Auxiliary HID usage ID in report descriptor (3 bytes)

Figure 27 illustrates the timing for an external ROM read operation. The timing characteristics are summarized in Table 11.

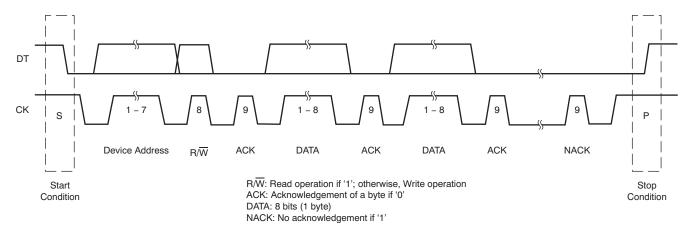


Figure 27. External ROM Read Operation

Table 11. External ROM Read Operation Characteristics

М	М	М	S	S	M	S	M	S	M	М
S	Device address	R/W	ACK	DATA	ACK	DATA	ACK		NACK	Р

Figure 28 shows the timing for an external ROM read interface. The respective timing characteristics are summarized in Table 12.

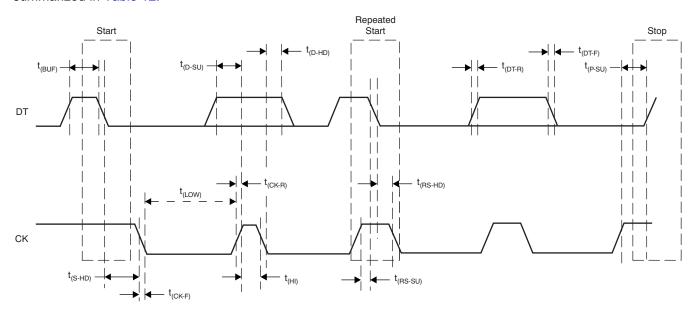


Figure 28. External ROM Read Interface Timing Requirements

Table 12. External ROM Read Interface Timing Chara	acteristics
--	-------------

SYMBOL	PARAMETER	MIN	MAX	UNIT
f _(CK)	CK clock frequency		100	kHz
t _(BUF)	Bus free time between a STOP and a START condition	4.7		μs
t _(LOW)	Low period of the CK clock	4.7		μs
t _(HI)	High period of the CK clock	4		μs
t _(RS-SU)	Setup time for START/repeated START condition	4.7		μs
t _(S-HD) t _(RS-HD)	Hold time for START/repeated START condition	4		μs
t _(D-SU)	Data setup time	250		ns
$t_{(D-HD)}$	Data hold time	0	900	ns
t _(CK-R)	Rise time of CK signal	20 + 0.1 C _B	1000	ns
t _(CK-F)	Fall time of CK signal	20 + 0.1 C _B	1000	ns
t _(DT-R)	Rise time of DT signal	20 + 0.1 C _B	1000	ns
t _(DT-F)	Fall time of DT signal	20 + 0.1 C _B	1000	ns
t _(P-SU)	Setup time for STOP condition	4		μs
C _B	Capacitive load for DT and CK lines		400	pF
V_{NH}	Noise margin at high level for each connected device (including hysteresis)	0.2 V _{DD}		V

INSTRUMENTS

External ROM Example

External ROM data (sample set)

```
0xBB, 0x08, 0x04, 0x27, 0x50, 0x72, 0x65, 0x64, 0x75, 0x63, 0x74, 0x20, 0x73, 0x74, 0x72, 0x69, 0x6E, 0x67, 0x73, 0x2E, 0x56, 0x65, 0x6E, 0x64, 0x6F, 0x72, 0x20, 0x73, 0x74, 0x72, 0x69, 0x6E, 0x67, 0x73, 0x20, 0x61, 0x72, 0x65, 0x20, 0x70, 0x6C, 0x61, 0x63, 0x65, 0x64, 0x20, 0x68, 0x65, 0x72, 0x65, 0x2E, 0x20, 0x70, 0x93, 0x93, 0x01
```

Explanation

Data are stored beginning at address 0x00.

Vendor ID: 0x08BB Product ID: 0x2704

Product string: Product strings (16 bytes).

Vendor string: Vendor strings are placed here (32 bytes, 31 visible characters are followed by 1 space).

Power attribute (bmAttribute): 0x80 (Bus-powered).

Max power (maxPower): 0x7D (250 mA).

Auxiliary HID usage ID: 0x0A, 0x93, 0x01 (AL A/V capture).

Note that the data bits must be sent from LSB to MSB on the I²C bus. Therefore, each data byte must be stored with its bits in reverse order.

Serial Programming Interface (PCM2705C/7C)

The PCM2705C/7C supports a serial interface (SPI) to program the descriptor and to set the HID state. Descriptor data are described in the *External ROM Descriptor* section. Figure 29 illustrates the SPI timing; Table 13 lists the respective timing characteristics.

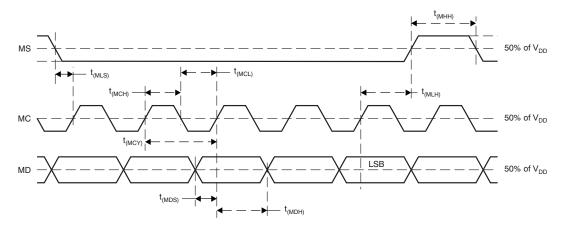


Figure 29. SPI Timing Diagram

Table 13. SPI Timing Characteristics

SYMBOL	PARAMETER	MIN	MAX	UNIT
t _(MCY)	MC pulse cycle time	100		ns
t _(MCL)	MC low-level time	50	ns	
t _(MCH)	MC high-level time	50	ns	
t _(MHH)	MS high-level time	100	ns	
t _(MLS)	MS falling edge to MC rising edge	20		ns
t _(MLH)	MS hold time	20		ns
t _(MDH)	MD hold time	15		ns
t _(MDS)	MD setup time	20	ns	

Figure 30 shows the SPI write timing sequence.

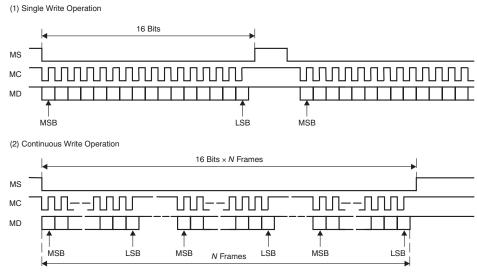


Figure 30. SPI Write Operation

SPI Register (PCM2705C/7C)

Table 14. SPI Register Description

					-	В9				_		_			-
0	0	0	0	ST	0	ADDR	0	D0	D1	D2	D3	D4	D5	D6	D7

D[7:0] Function of the lower 8 bits depends on the value of the ST (B11) bit.

ST = 0 (HID status write)

- D7 Reports MUTE HID status to the host (active high)
- D6 Reports volume-up HID status to the host (active high)
- D5 Reports volume-down HID status to the host (active high)
- D4 Reports next-track HID status to the host (active high)
- D3 Reports previous-track HID status to the host (active high)
- D2 Reports stop HID status to the host (active high)
- D1 Reports play/pause HID status to the host (active high)
- D0 Reports extended command status to the host (active high)

ST = 1 (ROM data write)

D[7:0] Internal descriptor ROM data, D0:LSB, D7:MSB

Contents of the power attribute and max power must be consistent with the actual application circuit configuration (the PSEL setting and the actual power usage from V_{BUS} of the USB connector); otherwise, it may cause improper or unexpected PCM2705C/7C operation.

ADDR Starts write operation for internal descriptor reprogramming (active high)

This bit resets the descriptor ROM address counter and indicates that subsequent words should be ROM data (described in the *External ROM Example* section). 456 bits of ROM data must be continuously followed after this bit has been asserted. The data bits must be sent from LSB (D0) to MSB (D7).

To set ADDR high, ST must be set low. Note that the lower 8 bits are still active as an HID status write when ST is set low.

ST Determines the function of the lower 8-bit data. Table 15 summarizes the functionality of ST and ADDR bit combinations.

0: HID status write

1: Descriptor ROM data write

Table 15. Functionality of ST and ADDR Bit Combinations

ST	ADDR	FUNCTION
0	0	HIS status write
0	1	HIS status write and descriptor ROM address reset
1	0	Descriptor ROM data write
1	1	Reserved

STRUMENTS

USB Host Interface Sequence

Power-On, Attach, and Playback Sequence

The PCM2704C/5C/6C/7C are ready for setup when the reset sequence has finished and the USB bus is attached. After a connection has been established (through the set-up process), the PCM2704C/5C/6C/7C are ready to accept USB audio data. While waiting for the audio data (that is, the device is in an idle state), the analog output is set to bipolar zero (BPZ).

Upon receiving the audio data, the PCM2704C/5C/6C/7C stores the first audio packet into the internal storage buffer. The packet contains 1 ms of audio data. The PCM2704C/5C/6C/7C start playing the audio data after detecting the next subsequent start-of-frame (SOF) packet. Figure 31 shows the initial operation sequence for the device.

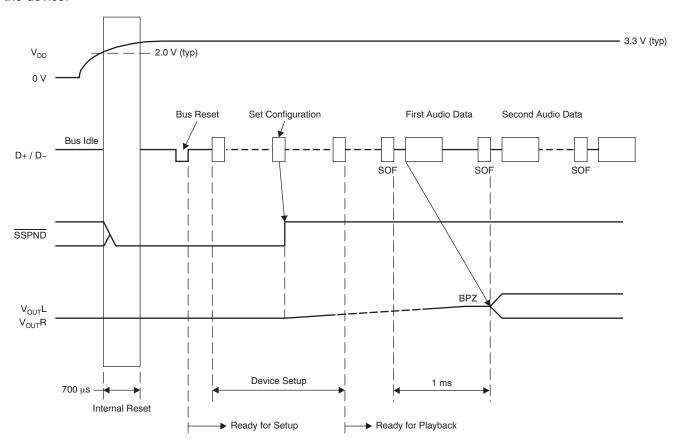


Figure 31. Initial Sequence

INSTRUMENTS

Play, Stop, and Detach Sequence

When the host finishes or aborts playback, the PCM2704C/5C/6C/7C stop playing after the last audio data output is complete. Figure 32 illustrates the play, stop, and detach sequence.

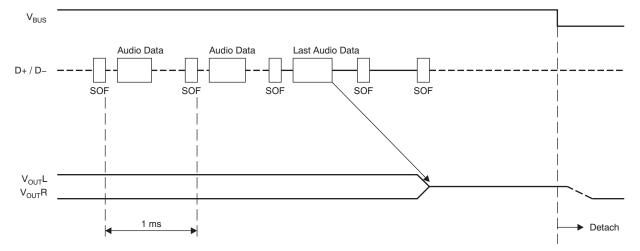


Figure 32. Play, Stop, and Detach Sequence

Suspend and Resume Sequence

The PCM2704C/5C/6C/7C enter a suspended state after the USB bus has been in a constant idle state for approximately 5 ms. While the PCM2704C/5C/6C/7C are in this suspended state, the SSPND flag (pin 27 for the PCM2704C/5C, pin 11 for the PCM2706C/7C) is asserted. The PCM2704C/5C/6C/7C wake up immediately when detecting a non-idle state on the USB bus. Figure 33 shows the operating sequence for the suspend and resume process.

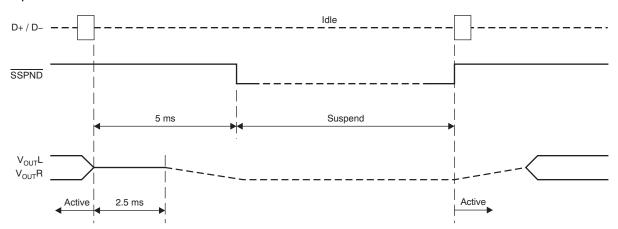


Figure 33. Suspend and Resume

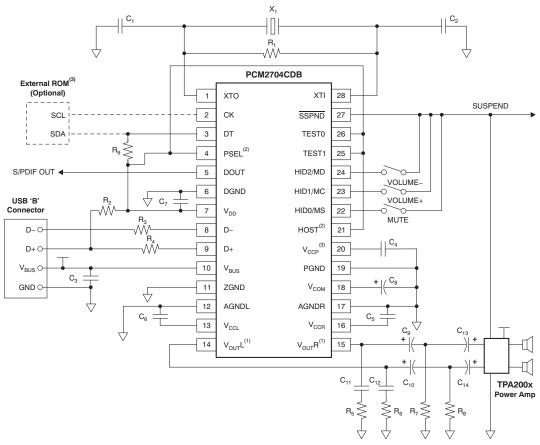
EXAMPLE CIRCUITS

Operating Environment

For current information on the PCM2704C/2705C/2706C/2707C operating environments, see the *Updated Operating Environments for PCM270X, PCM290X Applications* application report, SLAA374, available through the TI website at www.ti.com.

Typical Circuit Connection 1: USB Speaker

Figure 34 illustrates a typical circuit connection for an internal-descriptor, bus-powered, 500-mA application.



NOTE: X_1 : 12-MHz crystal resonator. C_1 , C_2 : 10-pF to 33-pF capacitors (depending on load capacitance of crystal resonator). C_3 to C_7 : 1- μ F ceramic capacitors. C_8 : 10- μ F electrolytic capacitor. C_9 , C_{10} : 100- μ F electrolytic capacitors (depending on tradeoff between required frequency response and discharge time for resume). C_{11} , C_{12} : 0.022- μ F ceramic capacitors. C_{13} , C_{14} : 1- μ F electrolytic capacitors. C_{11} , C_{12} : 0.022- μ F ceramic capacitors. C_{13} , C_{14} : 1- μ F electrolytic capacitors. C_{11} C_{12} : 0.022- C_{11} C_{12} : 0.022- C_{13} C_{13} C_{14} : 1- C_{12} C_{13} C_{14} : 1- C_{15} C_{15

- (1) Output impedance of $V_{OUT}L$ and $V_{OUT}R$ during suspended mode or lack of power supply is 26 k Ω ±20%, which is the discharge path for C_9 and C_{10} .
- (2) Descriptor programming through external ROM is only available when PSEL and HOST are high.
- (3) External ROM power can be supplied from V_{CCP} , but any other active component must not use V_{CCP} , V_{CCL} , V_{CCR} , or V_{DD} as a power source.

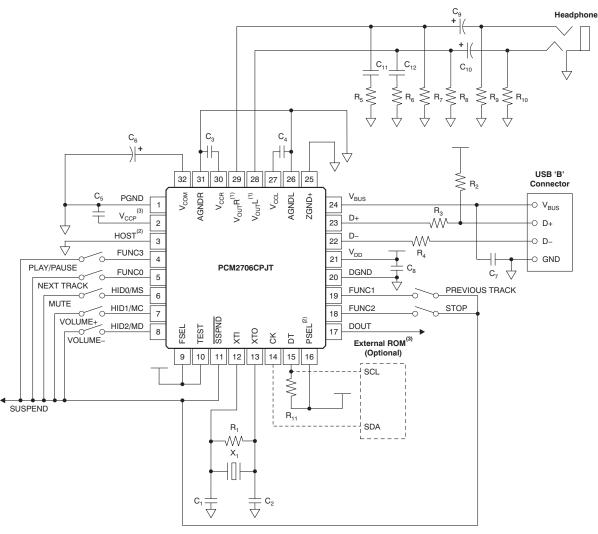
Figure 34. Bus-Powered Application

NOTE

The circuit illustrated in Figure 34 is for information only. The entire board design should be considered to meet the USB specification as a USB-compliant product.

Typical Circuit Connection 2: Remote Headphone

Figure 35 illustrates a typical circuit connection for a bus-powered, 100-mA headphone with seven HIDs.



NOTE: X_1 : 12-MHz crystal resonator. C_1 , C_2 : 10-pF to 33-pF capacitors (depending on load capacitance of crystal resonator). C_3 to C_5 , C_7 , C_8 : 1-µF ceramic capacitors. C_6 : 10-µF electrolytic capacitor. C_9 , C_{10} : 100-µF electrolytic capacitors (depending on required frequency response). C_{11} , C_{12} : 0.022-µF ceramic capacitors. C_{11} : 1-M Ω resistor. C_{12} : 1.5-k Ω resistors. C_{13} : 22- Ω resistors. C_{14} : 1.6- C_{15} : 1.

- (1) Output impedance of $V_{OUT}L$ and $V_{OUT}R$ during suspend mode or lack of power supply is 26 k Ω ±20%, which is the discharge path for C_9 and C_{C_9}
- (2) Descriptor programming through external ROM is only available when PSEL and HOST are high.
- (3) External ROM power can be supplied from V_{CCP} , but any other active component must not use V_{CCP} , V_{CCL} , V_{CCR} , or V_{DD} as a power source.

Figure 35. Bus-Powered Application

NOTE

The circuit illustrated in Figure 35 is for information only. The entire board design should be considered to meet the USB specification as a USB-compliant product.

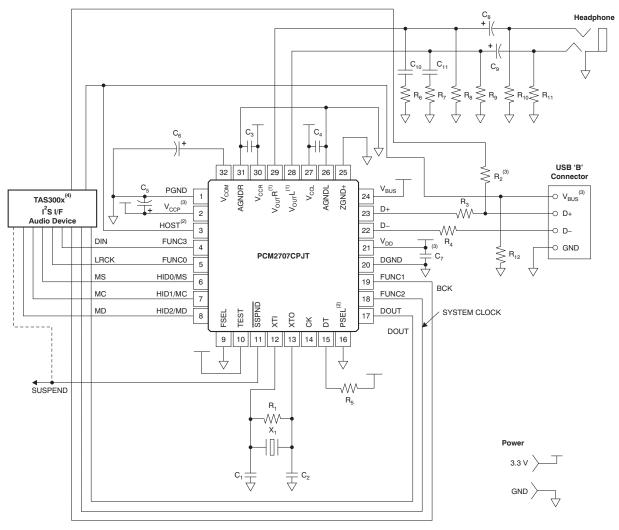
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NSTRUMENTS



Typical Circuit Connection 3: DSP Surround Processing Amplifier

Figure 36 illustrates a typical circuit connection for an I²S- and SPI-enabled self-powered application.



NOTE: X_1 : 12-MHz crystal resonator. C_1 , C_2 : 10-pF to 33-pF capacitors (depending on load capacitance of crystal resonator). C_3 , C_4 : 1- μ F ceramic capacitors. C_5 , C_7 : 0.1- μ F ceramic capacitor and 10- μ F electrolytic capacitor. C_6 : 10- μ F electrolytic capacitors. C_8 , C_9 : 100- μ F electrolytic capacitors (depending on required frequency response). C_{10} , C_{11} : 0.022- μ F ceramic capacitors. C_1 , C_1 : 1-M Ω resistors. C_2 , C_3 : 1.5- C_1 0 resistors. C_4 1, C_1 1 resistors. C_5 2 resistors. C_7 3 resistors. C_7 4 resistors. C_7 5 resistors. C_7 6 resistors. C_7 6 resistors. C_7 7 resistors. C_7 8 resistors. C_7 8 resistors. C_7 9 resistors.

- (1) Output impedance of $V_{OUT}L$ and $V_{OUT}R$ during suspend mode or lack of power supply is 26 k Ω ±20%, which is the discharge path for C_8 and C_9 .
- (2) Descriptor programming through SPI is only available when PSEL and HOST are high.
- (3) D+ pull-up must not be activated (high: 3.3 V) while the device is detached from USB or power supply is not applied on V_{DD} and V_{CCx} . V_{BUS} of USB (5 V) can be used to detect USB power status.
- (4) MS must be high until the PCM2707C power supply is ready and the SPI host (the DSP) is ready to send data. Also, the SPI host must handle the D+ pull-up if the descriptor is programmed through the SPI. D+ pull-up must not be activated (high = 3.3 V) before programming of the PCM2707C through the SPI is complete.

Figure 36. Self-Powered Application

NOTE

The circuit illustrated in Figure 36 is for information only. The entire board design should be considered to meet the USB specification as a USB-compliant product.





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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
PCM2704CDB	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
PCM2704CDBR	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
PCM2705CDB	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
PCM2705CDBR	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
PCM2706CPJT	PREVIEW	TQFP	PJT	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
PCM2706CPJTR	PREVIEW	TQFP	PJT	32	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
PCM2707CPJT	PREVIEW	TQFP	PJT	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
PCM2707CPJTR	PREVIEW	TQFP	PJT	32	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.



PACKAGE OPTION ADDENDUM

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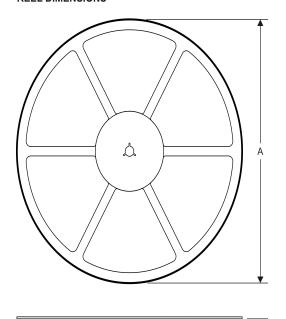
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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter	Reel Width	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
	,,,,					W1 (mm)	,,	`,	`,	,,	,,	
PCM2704CDBR	SSOP	DB	28	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
PCM2705CDBR	SSOP	DB	28	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

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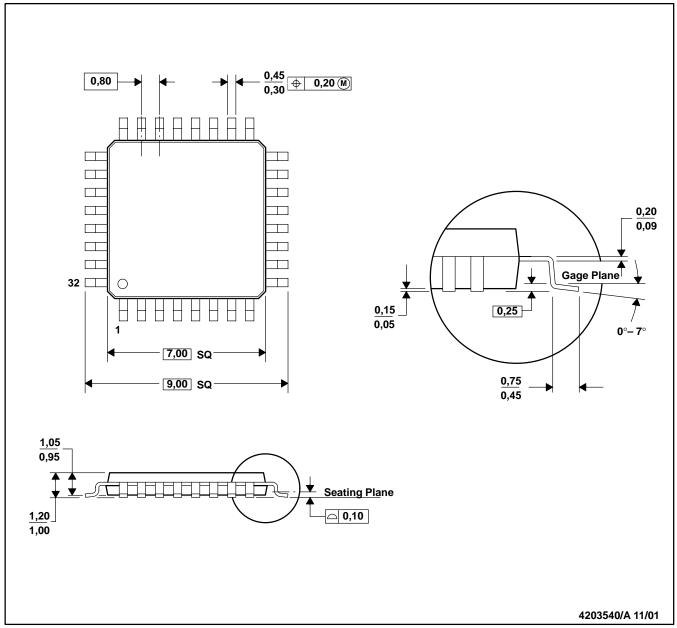


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM2704CDBR	SSOP	DB	28	2000	346.0	346.0	33.0
PCM2705CDBR	SSOP	DB	28	2000	346.0	346.0	33.0

PJT (S-PQFP-N32)

PLASTIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Falls within JEDEC MS-026

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-150

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