



32-Bit, 192-kHz Sampling, Advanced Segment, Stereo Audio Digital-to-Analog Converter

FEATURES

- 32-Bit Resolution
- Analog Performance:
 - Dynamic Range: 123 dB
 - THD+N: 0.0005%
- Differential Current Output: 3.9 mApp
- 8x Oversampling Digital Filter:
 - Stop Band Attenuation: -98 dB
 - Passband Ripple: ±0.0002 dB
- Sampling Frequency: 10 kHz to 200 kHz
- System Clock: 128, 192, 256, 384, 512, or 768 f_S With Autodetect
- Accepts 16-, 24-, and 32-Bit Audio Data
- PCM Data Formats: Standard, I²S™, and Left-Justified
- DSD Format Interface Available
- Interface Available for Optional External Digital Filter or DSP
- TDMCA or Serial Port (SPI™/I²C™)
- User-Programmable Mode Controls:
 - Digital Attenuation: 0 dB to -120 dB, 0.5-dB/Step
 - Digital De-Emphasis
 - Digital Filter Roll-Off: Sharp or Slow
 - Soft Mute
 - Zero Flag for Each Output
- Compatible With PCM1792A and PCM1796 (Pins and Mode Controls)
- Dual Supply Operation:
 - 5-V Analog, 3.3-V Digital
- 5-V Tolerant Digital Inputs
- Small SSOP-28 Package

APPLICATIONS

- A/V Receivers
- SACD Players
- DVD Players
- HDTV Receivers
- Car Audio Systems
- Digital Multitrack Recorders
- Other Applications Requiring 32-Bit Audio

DESCRIPTION

The PCM1795 is a monolithic CMOS integrated circuit that includes stereo digital-to-analog converters (DACs) and support circuitry in a small SSOP-28 package. The data converters use TI's advanced segment DAC architecture to achieve excellent dynamic performance and improved tolerance to clock jitter. The PCM1795 provides balanced current outputs, allowing the user to optimize analog performance externally. PCM1795 accepts pulse code modulation (PCM) and direct stream digital (DSD) audio data formats, providing an easy interface to audio digital signal processors (DSPs) and decoder chips. The PCM1795 also interfaces with external digital filter devices such as the DF1704, DF1706, and the PMD200 from Pacific Microsonics™. Sampling rates up to 200 kHz are supported. A full set of user-programmable functions is accessible through an SPI or I²C serial control port that supports register write and readback PCM1795 functions. The also supports time-division-multiplexed (TDM) command and audio (TDMCA) data format.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

System Two, Audio Precision are trademarks of Audio Precision, Inc. SPI is a trademark of Motorola.

I2S, I2C are trademarks of NXP Semiconductors.

Pacific Microsonics is a trademark of Pacific Microsonics, Inc.

Super Audio CD is a trademark of Sony Corporation.

All other trademarks are the property of their respective owners.





This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE- LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
PCM1795	SSOP-28	DB	–25°C to +85°C	DCM1705	PCM1795DB	Tube
PCIVIT/95	33UF-20	DB	-25 C 10 +65 C	PCM1795	PCM1795DBR	Tape and Reel

For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI
web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		VALUE	UNIT
Cumply voltage	V _{CC} 1, V _{CC} 2L, V _{CC} 2R	-0.3 to +6.5	V
Supply voltage	V_{DD}	-0.3 to +4	V
Supply voltage differences	V _{CC} 1, V _{CC} 2L, V _{CC} 2R	±0.1	V
Ground voltage differences	AGND1, AGND2, AGND3L, AGND3R, DGND	±0.1	V
Digital input voltage	LRCK, DATA, BCK, SCK, MSEL, $\overline{\rm RST}$, $\overline{\rm MS}^{(2)}$, MDI, MC, MDO $^{(2)}$, ZEROL $^{(2)}$, ZEROR $^{(2)}$	-0.3 to +6.5	V
	ZEROL ⁽³⁾ , ZEROR ⁽³⁾ , MDO ⁽³⁾ , MS ⁽³⁾	-0.3 to $(V_{DD} + 0.3) < 4$	V
Analog input voltage		-0.3 to $(V_{CC} + 0.3) < 6.5$	V
Input current (any pins excep	t supplies)	±10	mA
Ambient temperature under b	ias	-40 to +125	°C
Storage temperature		-55 to +150	°C
Junction temperature		+150	°C
Package temperature (IR refl	ow, peak)	+260	°C

⁽¹⁾ Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Submit Documentation Feedback

Copyright © 2009, Texas Instruments Incorporated

⁽²⁾ Input mode or I²C mode.

⁽³⁾ Output mode except for I²C mode.



ELECTRICAL CHARACTERISTICS

All specifications at $T_A = +25$ °C, $V_{CC}1 = V_{CC}2L = V_{CC}2R = 5$ V, $V_{DD} = 3.3$ V, $f_S = 48$ kHz, system clock = 256 f_S , and 32-bit data, unless otherwise noted.

			PC	M1795 DB		
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
RESOL	LUTION				-	
	Resolution			32		Bits
DATA	FORMAT (PCM Mode)				·	
	Audio data interface format		Standard	, I ² S, left-just	tified	
	Audio data bit length		16-, 24-,	32-bit select	able	
	Audio data format		MSB first,	twos comple	ement	
f _S	Sampling frequency		10		200	kHz
	System clock frequency		128, 192, 2	256, 384, 512	2, 768	f _S
DATA	FORMAT (DSD Mode)				·	
	Audio data interface format		DSD (dire	ct stream di	gital)	
	Audio data bit length			1		Bit
f _S	Sampling frequency			2.8224		MHz
	System clock frequency		2.8224		11.2986	MHz
DIGITA	L INPUT/OUTPUT				-	
	Logic family		Co	TTL ompatible		
V _{IH}			2			VDC
V _{IL}	Input logic level				0.8	VDC
Ін	Level Levis comment	$V_{IN} = V_{DD}$			10	μΑ
l _{IL}	Input logic current	V _{IN} = 0 V			-10	μΑ
V _{OH}	Output la cia laval	I _{OH} = -2 mA	2.4			VDC
V _{OL}	Output logic level	I _{OL} = 2 mA			0.4	VDC
DYNAN	MIC PERFORMANCE (PCM MODE)(1)(2)			<u> </u>	
		f _S = 48 kHz		0.0005	0.001	%
	THD+N at $V_{OUT} = 0$ dB	f _S = 96 kHz		0.001		%
		f _S = 192 kHz		0.0015		%
		EIAJ, A-weighted, f _S = 48 kHz	120	123		dB
	Dynamic range	EIAJ, A-weighted, f _S = 96 kHz		123		dB
	-	EIAJ, A-weighted, f _S = 192 kHz		123		dB
		EIAJ, A-weighted, f _S = 48 kHz	120	123		dB
	Signal-to-noise ratio	EIAJ, A-weighted, f _S = 96 kHz		123		dB
		EIAJ, A-weighted, f _S = 192 kHz		123		dB
		f _S = 48 kHz	116	119		dB
	Channel separation	f _S = 96 kHz		118		dB
	•	f _S = 192 kHz		117		dB
	Level linearity error	$V_{OUT} = -120 \text{ dB}$		±1		dB

(1) Filter condition:

THD+N: 20-Hz high-pass filter (HPF), 20-kHz AES17 low-pass filter (LPF)

Dynamic range: 20-Hz HPF, 20-kHz AES17 LPF, A-weighted Signal-to-noise ratio: 20-Hz HPF, 20-kHz AES17 LPF, A-weighted Channel separation: 20-Hz HPF, 20-kHz AES17 LPF

Analog performance specifications are measured using the System Two™ Cascade audio measurement system by Audio Precision™ in the averaging mode.

Dynamic performance and dc accuracy are specified at the output of the post-amplifier as shown in Figure 52.



ELECTRICAL CHARACTERISTICS (continued)

All specifications at $T_A = +25$ °C, $V_{CC}1 = V_{CC}2L = V_{CC}2R = 5$ V, $V_{DD} = 3.3$ V, $f_S = 48$ kHz, system clock = 256 f_S , and 32-bit data, unless otherwise noted.

		PC	M1795 DB		
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE (MONO MODE)(3)(4)(5)				
	f _S = 48 kHz		0.0005		%
THD+N at $V_{OUT} = 0 \text{ dB}$	f _S = 96 kHz		0.001		%
	f _S = 192 kHz		0.0015		%
	EIAJ, A-weighted, f _S = 48 kHz		126		dB
Dynamic range	EIAJ, A-weighted, f _S = 96 kHz		126		dB
	EIAJ, A-weighted, f _S = 192 kHz		126		dB
	EIAJ, A-weighted, f _S = 48 kHz		126		dB
Signal-to-noise ratio	EIAJ, A-weighted, f _S = 96 kHz		126		dB
	EIAJ, A-weighted, f _S = 192 kHz		126		dB
DSD MODE DYNAMIC PERFORMANCE (44.1 kH					
THD+N at FS	2 V rms		0.0007		%
Dynamic range	-60 dB, EIAJ, A-weighted		122		dB
Signal-to-noise ratio	EIAJ, A-weighted		122		dB
ANALOG OUTPUT	-				
Gain error		-7	±2	7	% of FSR
Gain mismatch, channel-to-channel		-3	±0.5	3	% of FSR
Bipolar zero error	At BPZ	-2	±0.5	2	% of FSR
Output current	Full-scale (0 dB)		4		mA _{PP}
Center current	At BPZ		-3.5		mA
DIGITAL FILTER PERFORMANCE					
De-emphasis error				±0.1	dB
FILTER CHARACTERISTICS-1: SHARP ROLL-0	OFF				
	±0.0002 dB			0.454	f _S
Passband	-3 dB			0.49	f _S
Stop band		0.546			f _S
Passband ripple				±0.0002	dB
Stop-band attenuation	Stop band = 0.546 f _S	-98			dB
Delay time	,		38/f _S		s
FILTER CHARACTERISTICS-2: SLOW ROLL-OI	FF				
	±0.001 dB			0.21	f _S
Passband	−3 dB			0.448	f _S
Stop band	-	0.79		-	f _S
Passband ripple				±0.001	dB
Stop-band attenuation	Stop band = 0.732 f _S	-80			dB
Delay time			38/f _S		S

(3) Filter condition:

THD+N: 20-Hz high-pass filter (HPF), 20-kHz AES17 low-pass filter (LPF)

Dynamic range: 20-Hz HPF, 20-kHz AES17 LPF, A-weighted Signal-to-noise ratio: 20-Hz HPF, 20-kHz AES17 LPF, A-weighted

Channel separation: 20-Hz HPF, 20-kHz AES17 LPF

Analog performance specifications are measured using the System Two™ Cascade audio measurement system by Audio Precision™ in the averaging mode.

- (4) Dynamic performance and dc accuracy are specified at the output of the post-amplifier as shown in Figure 52.
- (5) Dynamic performance and dc accuracy are specified at the output of the measurement circuit as shown in Figure 54.
- Dynamic performance and dc accuracy are specified at the output of the post-amplifier as shown in Figure 53.

Submit Documentation Feedback

Copyright © 2009, Texas Instruments Incorporated



ELECTRICAL CHARACTERISTICS (continued)

All specifications at $T_A = +25$ °C, $V_{CC}1 = V_{CC}2L = V_{CC}2R = 5$ V, $V_{DD} = 3.3$ V, $f_S = 48$ kHz, system clock = 256 f_S , and 32-bit data, unless otherwise noted.

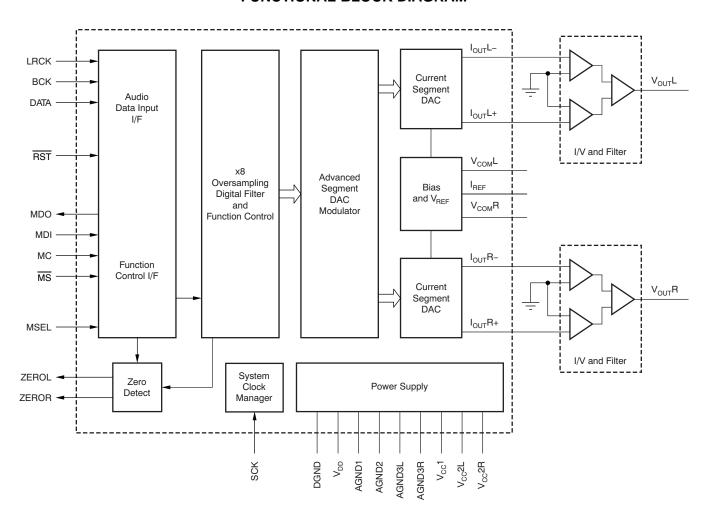
			PCI	M1795 DB		
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER-	SUPPLY REQUIREMENTS					
V_{DD}			3	3.3	3.6	VDC
V _{CC} 1	Valta va va va					
V _{CC} 2L	Voltage range		4.75	5	5.25	VDC
V _{CC} 2R						
I _{DD}		f _S = 48 kHz		6	8	mA
		f _S = 96 kHz		11		mA
	Complete suggest (7)	f _S = 192 kHz		21		mA
	Supply current ⁽⁷⁾	f _S = 44.1 kHz		18	23	mA
cc		f _S = 96 kHz		19		mA
		f _S = 192 kHz		20		mA
		f _S = 48 kHz		110	141	mW
	Power dissipation ⁽⁷⁾	f _S = 96 kHz		131		mW
		f _S = 192 kHz		166		mW
TEMPER	ATURE RANGE					
	Operating temperature		-25		+85	°C
θ_{JA}	Thermal resistance	SSOP-28		+100		°C/W

⁽⁷⁾ Input is bipolar zero (BPZ) data.

Submit Documentation Feedback



FUNCTIONAL BLOCK DIAGRAM





PIN CONFIGURATION

DB PACKAGE SSOP-28 (TOP VIEW)

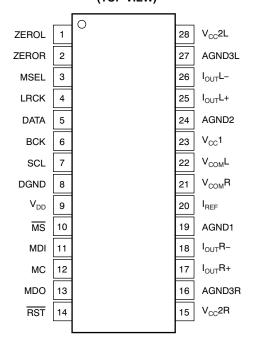


Table 1. TERMINAL FUNCTIONS

TER	RMINAL		
NAME	NO.	I/O	DESCRIPTION
AGND1	19	_	Analog ground (internal bias)
AGND2	24	_	Analog ground (internal bias)
AGND3L	27	_	Analog ground (left channel DACFF)
AGND3R	16	_	Analog ground (right channel DACFF)
BCK	6	I	Bit clock input ⁽¹⁾
DATA	5	I	Serial audio data input ⁽²⁾
DGND	8	_	Digital ground
I _{OUT} L+	25	0	Left channel analog current output+
I _{OUT} L-	26	0	Left channel analog current output-
I _{OUT} R+	17	0	Right channel analog current output+
I _{OUT} R-	18	0	Right channel analog current output-
I _{REF}	20	_	Output current reference bias pin
LRCK	4	I	Left and right clock (f _S) input ⁽²⁾
MC	12	I	Mode control clock input ⁽²⁾
MDI	11	I	Mode control data input ⁽²⁾
MDO	13	I/O	Mode control readback data output ⁽³⁾
MS	10	I/OI	Mode control chip-select input ⁽⁴⁾ ; active low
MSEL	3	I	I ² C/ SPI select ⁽²⁾ ; active low SPI select
RST	14	I	Reset ⁽²⁾ ; active low

- (1) Schmitt-trigger input, 5-V tolerant.
- (2) Schmitt-trigger input, 5-V tolerant.
- (3) Schmitt-trigger input and output. 5-V tolerant input. In I²C mode, this pin becomes an open-drain 3-state output; otherwise, this pin is a CMOS output.
- (4) Schmitt-trigger input and output. 5-V tolerant input and CMOS output.



Table 1. TERMINAL FUNCTIONS (continued)

TE	TERMINAL		
NAME	NO.	I/O	DESCRIPTION
SCK	7	ı	System clock input ⁽²⁾
V _{CC} 1	23	_	Analog power supply, 5 V
V _{CC} 2L	28	_	Analog power supply (left channel DACFF), 5 V
V _{CC} 2R	15	_	Analog power supply (right channel DACFF), 5 V
$V_{COM}L$	22	_	Left channel internal bias decoupling pin
$V_{COM}R$	21	_	Right channel internal bias decoupling pin
V_{DD}	9	_	Digital power supply, 3.3 V
ZEROL	1	I/O	Zero flag for left channel (4)
ZEROR	2	I/O	Zero flag for right channel (4)

TIMING CHARACTERISTICS

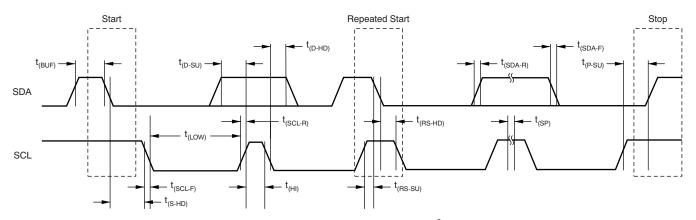


Figure 1. Timing Definition on the I²C Bus

TIMING REQUIREMENTS

	PARAMETER	CONDITIONS	MIN	MAX	UNIT
	COL alask framusa su	Standard		100	kHz
(SCL)	SCL clock frequency	Fast		400	kHz
	Des for the between started and start and fifteen	Standard	4.7		μs
(BUF)	Bus free time between stop and start conditions	Fast	1.3		μs
	Lawrenciad of the COL short	Standard	4.7		μs
(LOW)	High period of the SCL clock Setup time for (repeated) start condition Hold time for (repeated) start condition	Fast	1.3		μs
	High region of the COL sheet.	Standard	4		μs
(HI)	High period of the SCL clock	Fast	600		ns
Setup time for (repeated) start condition (S-HD) (RS-HD) Hold time for (repeated) start condition		Standard	4.7		μs
(RS-SU)	Setup time for (repeated) start condition	Fast	600		ns
(S-HD)	Hold time for (reported) etait and distant	Standard	4		μs
(RS-HD)	note time for (repeated) start condition	Fast	600		ns
	Data action times	Standard	250		ns
(D-SU)	Data setup time	Fast	100		ns
t _(D-HD)	Data hold time	Standard	0	900	ns
		Fast	0	900	ns
SCL-R) Rise time of SCL signal	Disa time of COI sime!	Standard	20 + 0.1 C _B	1000	ns
(SCL-R)	Rise time of SCL signal	Fast	20 + 0.1 C _B	300	ns
	Rise time of SCL signal after a repeated start condition	Standard	20 + 0.1 C _B	1000	ns
(SCL-R1)	and after an acknowledge bit	Fast	20 + 0.1 C _B	300	ns
and after an acknowledge bit		Standard	20 + 0.1 C _B	1000	ns
(SCL-F)	Fall time of SCL signal	Fast	20 + 0.1 C _B	300	ns
	Discribed of ODA sixed	Standard	20 + 0.1 C _B	1000	ns
(SDA-R)	Rise time of SDA signal	Fast	20 + 0.1 C _B	300	ns
	Fall time of CDA signal	Standard	20 + 0.1 C _B	1000	ns
(SDA-F)	Fall time of SDA signal	Fast	20 + 0.1 C _B	300	ns
	Cation times for stan acceptition	Standard	4		μs
(P-SU)	Setup time for stop condition	Fast	600		ns
C _(B)	Capacitive load for SDA and SCL line			400	pF
(SP)	Pulse duration of suppressed spike	Fast		50	ns
V _{NH}	Noise margin at high level for each connected device (including hysteresis)		0.2 V _{DD}		V

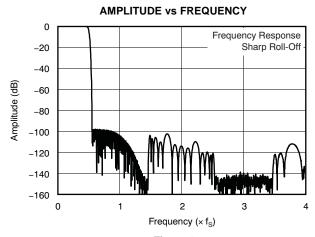
SLES248-MAY 2009



www.ti.com

TYPICAL CHARACTERISTICS: DIGITAL FILTER

Digital Filter Response





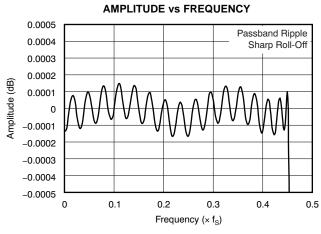


Figure 3.

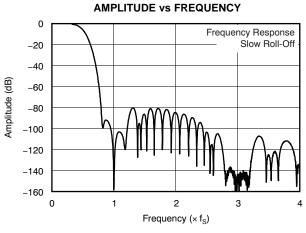


Figure 4.

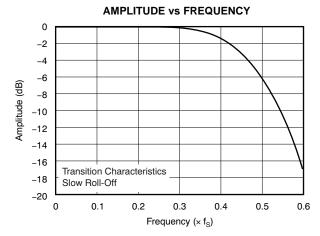
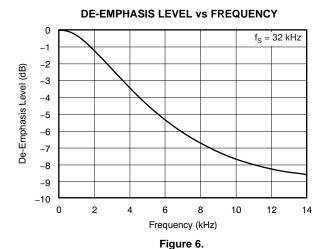


Figure 5.

 www.ti.com
 SLES248-MAY 2009

TYPICAL CHARACTERISTICS: DIGITAL FILTER

De-Emphasis Filter



DE-EMPHASIS LEVEL vs FREQUENCY

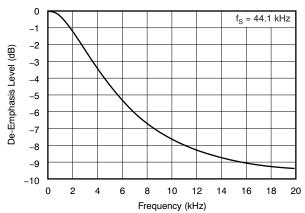
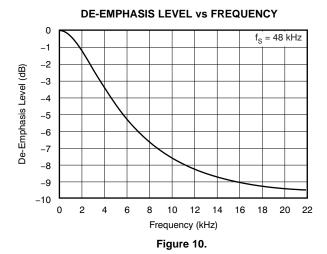


Figure 8.



DE-EMPHASIS ERROR vs FREQUENCY

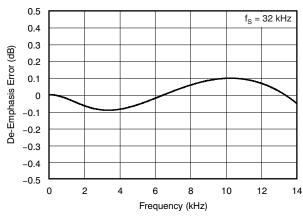


Figure 7.

DE-EMPHASIS ERROR vs FREQUENCY

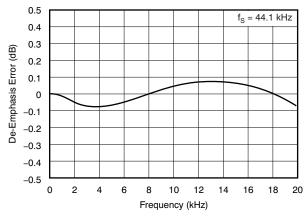


Figure 9.

DE-EMPHASIS ERROR vs FREQUENCY

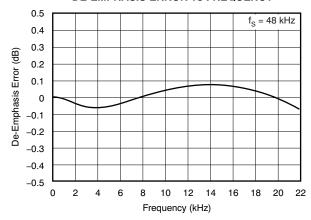


Figure 11.



INSTRUMENTS

5.50

5.25

SLES248-MAY 2009 www.ti.com

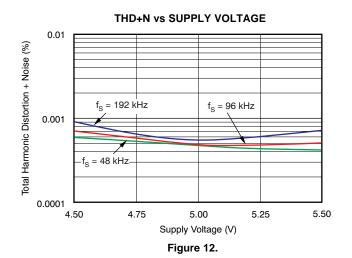
TYPICAL CHARACTERISTICS: ANALOG DYNAMIC PERFORMANCE

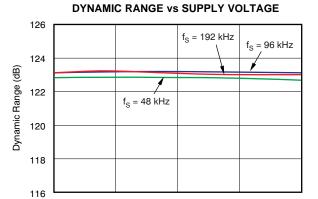
4.50

4.75

Supply Voltage Characteristics

PCM mode, $T_A = +25$ °C, and $V_{DD} = 3.3$ V; measured with circuit shown in Figure 52, unless otherwise noted.

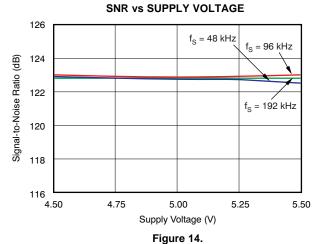




Supply Voltage (V) Figure 13.

5.00





CHANNEL SEPARATION vs SUPPLY VOLTAGE

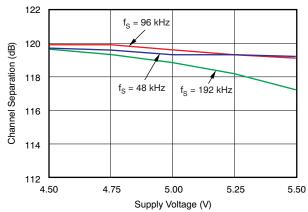


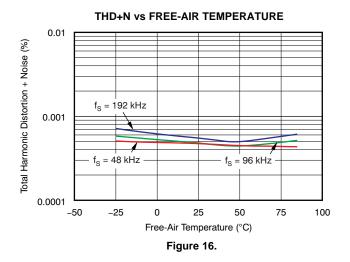
Figure 15.

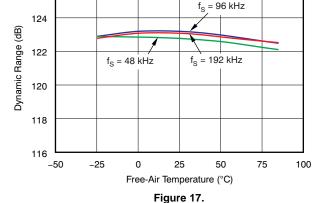
TYPICAL CHARACTERISTICS: ANALOG DYNAMIC PERFORMANCE

126

Temperature Characteristics

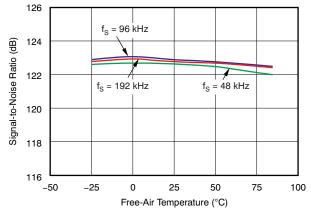
PCM mode, V_{DD} = 3.3 V, and V_{CC} = 5 V; measured with circuit shown in Figure 52, unless otherwise noted.





DYNAMIC RANGE vs FREE-AIR TEMPERATURE

SNR vs FREE-AIR TEMPERATURE



CHANNEL SEPARATION vs FREE-AIR TEMPERATURE

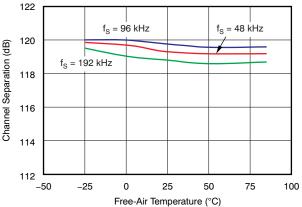
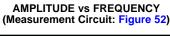
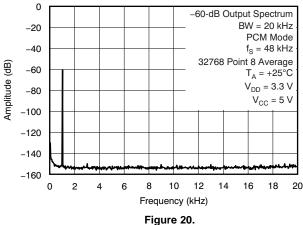
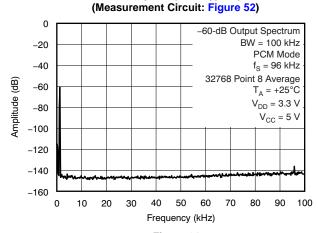


Figure 18.

Figure 19.







AMPLITUDE vs FREQUENCY

Figure 21.



TYPICAL CHARACTERISTICS: ANALOG DYNAMIC PERFORMANCE (continued)

PCM mode, V_{DD} = 3.3 V, and V_{CC} = 5 V; measured with circuit shown in Figure 52, unless otherwise noted.

AMPLITUDE vs FREQUENCY (Measurement Circuit: Figure 52) -120 -144-dB Output Spectrum -124 BW = 20 kHzPCM Mode -128 $f_S = 48 \text{ kHz}$ -132 32768 Point 8 Average Amplitude (dB) $T_A = +25^{\circ}C$ -136 $V_{DD} = 3.3 \text{ V}$ -140 $V_{CC} = 5 V$ -144 -148 Thappy -152 -156 -160 100 1 k 10 k Frequency (Hz)

Figure 22.

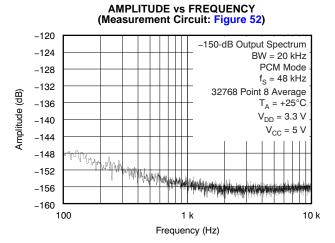


Figure 23.

THD+N vs INPUT LEVEL (Measurement Circuit: Figure 52)

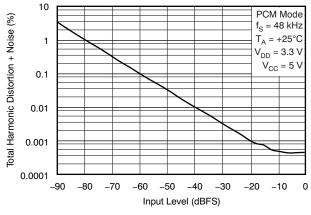


Figure 24.

AMPLITUDE vs FREQUENCY (Measurement Circuit: Figure 53)

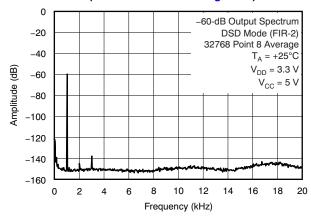


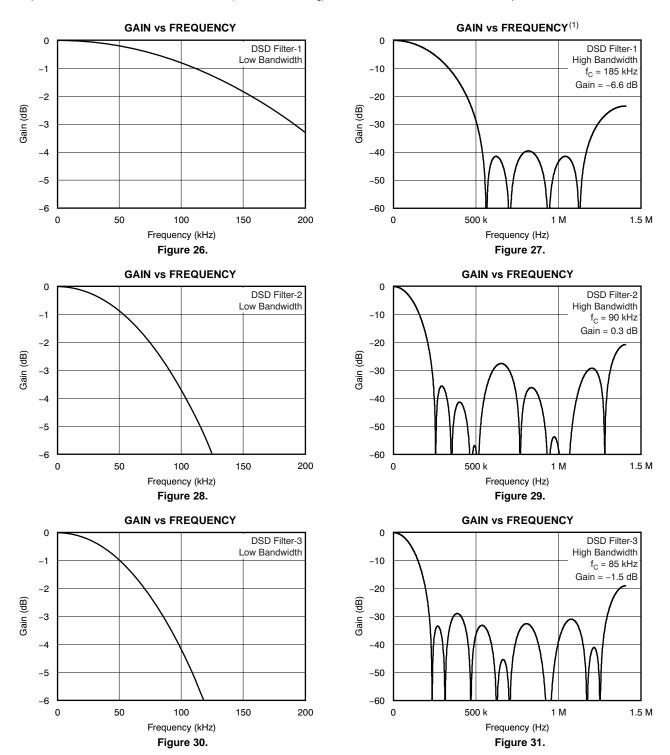
Figure 25.

Submit Documentation Feedback



TYPICAL CHARACTERISTICS: ANALOG FIR FILTER PERFORMANCE IN DSD MODE

All specifications at DBCK = 2.8224 MHz (44.1 kHz × 64 f_S), and 50% modulation DSD data input, unless otherwise noted.

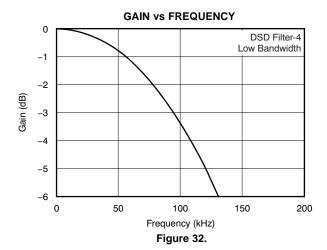


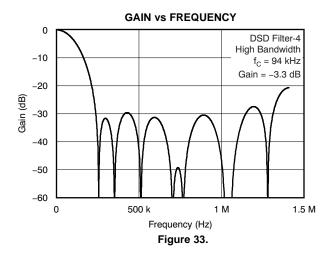
⁽¹⁾ This gain is in comparison to PCM 0 dB, when the DSD input signal efficiency is 50%.



TYPICAL CHARACTERISTICS: ANALOG FIR FILTER PERFORMANCE IN DSD MODE (continued)

All specifications at DBCK = 2.8224 MHz (44.1 kHz \times 64 f_S), and 50% modulation DSD data input, unless otherwise noted.





GENERAL DESCRIPTION

SYSTEM CLOCK AND RESET FUNCTIONS

System Clock Input

The PCM1795 requires a system clock to operate the digital interpolation filters and advanced segment DAC modulators. The system clock is applied at the SCK input (pin 7). The PCM1795 has a system clock detection circuit that automatically senses the frequency at which the system clock is operating. Table 2 shows examples of system clock frequencies for common audio sampling rates. If the oversampling rate of the delta-sigma ($\Delta\Sigma$) modulator is selected as 128 f_S, the system clock frequency is required to be greater than 256 f_S.

Figure 34 and Table 3 show the timing requirements for the system clock input. For optimal performance, it is important to use a clock source with low phase jitter and noise. The Texas Instruments PLL1700 family of multiclock generators is an excellent choice to provide the PCM1795 system clock.

SAMPLING FREQUENCY	SYSTEM CLOCK FREQUENCY (f _{SCK}) (MHz)						
(kHz)	128 f _S	192 f _S	256 f _S	384 f _S	512 f _S	768 f _S	
32	4.096 ⁽¹⁾	6.144 ⁽¹⁾	8.192	12.288	16.384	24.576	
44.1	5.6488 ⁽¹⁾	8.4672	11.2896	16.9344	22.5792	33.8688	
48	6.144 ⁽¹⁾	9.216	12.288	18.432	24.576	36.864	
96	12.288	18.432	24.576	36.864	49.152 ⁽¹⁾	73.728 ⁽¹⁾	
192	24.576	36.864	49.152 ⁽¹⁾	73.728 ⁽¹⁾	X ⁽²⁾	X ⁽²⁾	

- (1) This system clock rate is not supported in I²C fast mode.
- (2) This system clock rate is not supported for the given sampling frequency.

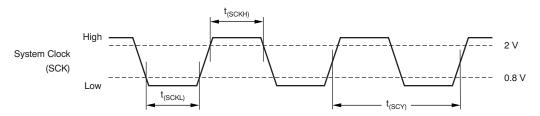


Figure 34. System Clock Input Timing

Table 3. Timing Characteristics for Figure 34

	PARAMETER	MIN	MAX	UNIT
t _(SCY)	System clock pulse cycle time	13		ns
t _(SCKH)	System clock pulse duration, high	0.4t _(SCY)		ns
t _(SCKL)	System clock pulse duration, low	0.4t _(SCY)		ns



Power-On and External Reset Functions

The PCM1795 includes a power-on reset function, as shown in Figure 35. With $V_{DD} > 2$ V, the power-on reset function is enabled. The initialization sequence requires 1024 system clocks from the time $V_{DD} > 2$ V. After the initialization period, the PCM1795 is set to its default reset state, as described in the *Mode Control Registers* section.

The PCM1795 also includes an external reset capability using the \overline{RST} input (pin 14). This feature allows an external controller or master reset circuit to force the PCM1795 to initialize to the default reset state.

Figure 36 and <u>Table 4</u> show the external reset operation and timing. The <u>RST</u> pin is set to logic 0 for a minimum of 20 ns. The <u>RST</u> pin is then set to a logic 1 state, thus starting the initialization sequence that requires 1024 system clock periods. The external reset is especially useful in applications where there is a delay between the PCM1795 power-up and system clock activation.

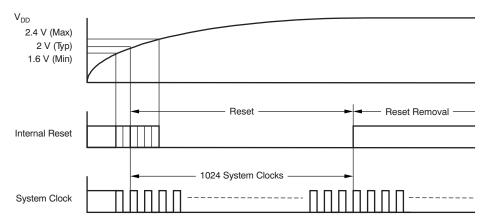


Figure 35. Power-On Reset Timing

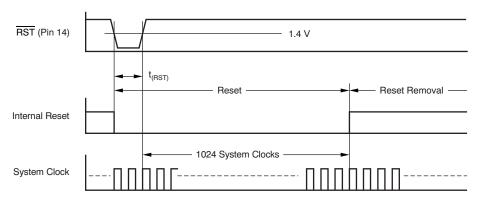


Figure 36. External Reset Timing

Table 4. Timing Characteristics for Figure 36

	PARAMETER	MIN	MAX	UNIT
$t_{(RST)}$	Reset pulse duration, low	20		ns

18 Subi

AUDIO DATA INTERFACE

Audio Serial Interface

The audio interface port is a three-wire serial port. It includes LRCK (pin 4), BCK (pin 6), and DATA (pin 5). BCK is the serial audio bit clock, and it is used to clock the serial data present on DATA into the serial shift register of the audio interface. Serial data are clocked into the PCM1795 on the rising edge of BCK. LRCK is the serial audio left/right word clock.

The PCM1795 requires the synchronization of LRCK and the system clock, but does not need a specific phase relation between LRCK and the system clock.

If the relationship between LRCK and the system clock changes more than ± 6 BCK, internal operation is initialized within $1/f_S$ and analog outputs are forced to the bipolar zero level until resynchronization between LRCK and the system clock is completed.

PCM Audio Data Formats and Timing

The PCM1795 supports industry-standard audio data formats, including standard right-justified, I²S, and left-justified. The data formats are illustrated in Figure 38 to Figure 40. Data formats are selected using the format bits, FMT[2:0], in control register 18. The default data format is 32-bit I²S. All formats require binary twos complement, MSB-first audio data. Figure 37 and Table 5 show a detailed timing diagram for the serial audio interface.

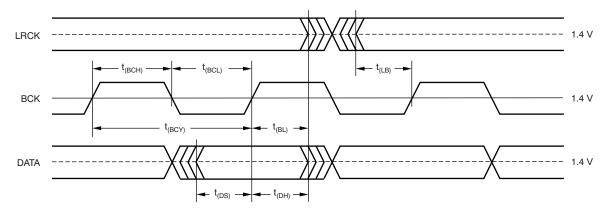


Figure 37. Audio Interface Timing

Table 5. Timing Characteristics for Figure 37

	PARAMETER	MIN	MAX	UNIT
t _(BCY)	BCK pulse cycle time	70		ns
t _(BCL)	BCK pulse duration, low	30		ns
t _(BCH)	BCK pulse duration, high	30		ns
t _(BL)	BCK rising edge to LRCK edge	10		ns
t _(LB)	LRCK edge to BCK rising edge	10		ns
t _(DS)	DATA setup time	10		ns
t _(DH)	DATA hold time	10		ns
_	LRCK clock data	50% ±	2 bit clocks	

Copyright © 2009, Texas Instruments Incorporated



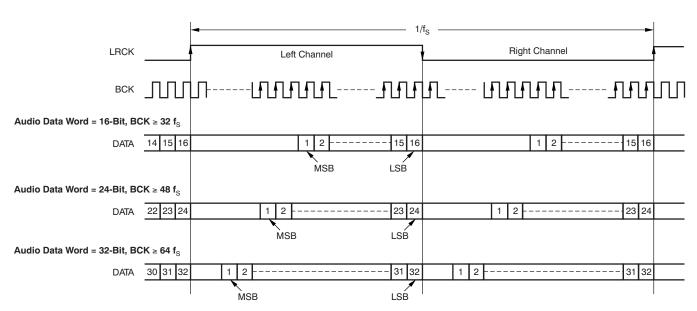


Figure 38. Audio Data Input Format: Standard Data Format (Right-Justified), Left Channel = High, Right Channel = Low

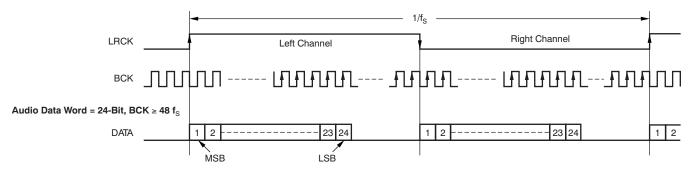


Figure 39. Audio Data Input Format: Left-Justified Data Format, Left Channel = High, Right Channel = Low

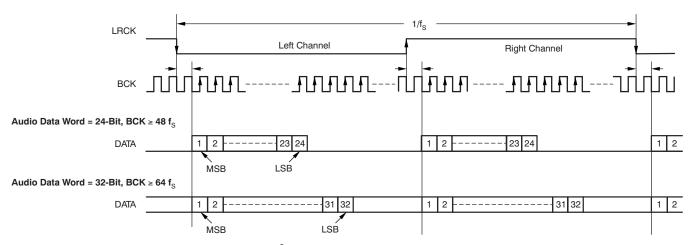


Figure 40. Audio Data Input Format: I²S Data Format, Left Channel = Low, Right Channel = High

Product Folder Link(s): PCM1795



External Digital Filter Interface and Timing

The PCM1795 supports an external digital filter interface that consists of a three- or four-wire synchronous serial port that allows the use of an external digital filter. External filters include the Texas Instruments' DF1704 and DF1706, the Pacific Microsonics PMD200, or a programmable digital signal processor.

In the external DF mode, LRCK (pin 4), BCK (pin 6) and DATA (pin 5) are defined as: WDCK, the word clock; BCK, the bit clock; and DATA, the monaural data. The external digital filter interface is selected by using the DFTH bit of control register 20, which functions to bypass the internal digital filter of the PCM1795.

When the DFMS bit of control register 19 is set, the PCM1795 can process stereo data. In this case, ZEROL (pin 1) and ZEROR (pin 2) are defined as left-channel data and right-channel data input, respectively.

Detailed information for the external digital filter interface mode is provided in the *Application For External Digital Filter Interface* section.

Direct Stream Digital (DSD) Format Interface and Timing

The PCM1795 supports the DSD format interface operation, which includes out-of-band noise filtering using an internal analog FIR filter. For DSD operation, SCK (pin 7) is redefined as BCK, DATA (pin 5) as DATAL (left channel audio data), and LRCK (pin 4) as DATAR (right channel audio data). BCK (pin 6) must be forced low in the DSD mode. The DSD format interface is activated by setting the DSD bit of control register 20.

Detailed information for the DSD mode is provided in the Application For DSD Format (DSD Mode) Interface section.

TDMCA Interface

The PCM1795 supports the time-division-multiplexed command and audio (TDMCA) data format to enable control of and communication with a number of external devices over a single serial interface.

Detailed information for the TDMCA format is provided in the TDMCA Interface Format section.

FUNCTION DESCRIPTIONS

Zero Detect

The PCM1795 has a zero-detect function. When the PCM1795 detects the zero conditions as shown in Table 6, the PCM1795 sets ZEROL (pin 1) and ZEROR (pin 2) high.

MO	DE	DETECTING CONDITION AND TIME						
PC	CM	DATA is continuously low for 1024 LRCKs.						
External DF mode		DATA is continuously low for 1024 WDCKs.						
DSD	DZ0	There are an equal number of 1s and 0s in every 8 bits of DSD input data for 23 ms.						
	DZ1	The input data are continuously 1001 0110 for 23 ms.						

Table 6. Zero Conditions

SERIAL CONTROL INTERFACE

The PCM1795 supports both SPI and I²C interfaces that set the mode control registers; see Table 9. The serial control interface is selected by MSEL (pin 3); SPI is activated when MSEL is set low, and I²C is activated when MSEL is set high.

SPI Interface

The SPI interface is a four-wire synchronous serial port that operates asynchronously to the serial audio interface and the system clock (SCK). The serial control interface is used to program and read the on-chip mode registers. The control interface includes MDO (pin 13), MDI (pin 11), MC (pin 12), and MS (pin 10). MDO is the serial data output, used to read back the values of the mode registers; MDI is the serial data input, used to program the mode registers; MC is the serial bit clock, used to shift data in and out of the control port; and MS is the mode control enable, used to enable the internal mode register access.

Register Read/Write Operation

All read/write operations for the serial control port use 16-bit data words. Figure 41 shows the control data word format. The most significant bit (MSB) is the read/write (R/W) bit. For write operations, the R/W bit must be set to '0'. For read operations, the R/W bit must be set to '1'. There are seven bits, labeled IDX[6:0], that hold the register index (or address) for the read and write operations. The least significant eight bits, D[7:0], contain the data to be written to, or the data that was read from, and the register specified by IDX[6:0].

Figure 42 shows the functional timing diagram for writing or reading the serial control port. $\overline{\text{MS}}$ is held at a logic 1 state until a register must be written to or read from. To start the register write or read cycle, $\overline{\text{MS}}$ is set to logic 0. Sixteen clocks are then provided on MC, corresponding to the 16 bits of the control data word on MDI and readback data on MDO. After the eighth clock cycle has completed, the data from the indexed-mode control register appears on MDO during the read operation. After the 16th clock cycle has completed, the data are latched into the indexed-mode control register during the write operation. To write or read subsequent data, $\overline{\text{MS}}$ must be set to '1' once.

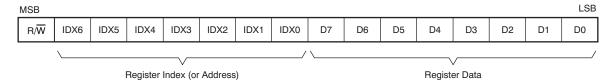
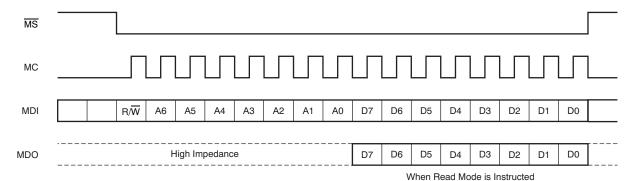


Figure 41. Control Data Word Format for MDI



NOTE: Bit 15 is used for selection of write or read. Setting $R/\overline{W} = 0$ indicates a write, while $R/\overline{W} = 1$ indicates a read. Bits 14–8 are used for the register address. Bits 7–0 are used for register data.

Figure 42. Serial Control Format

22

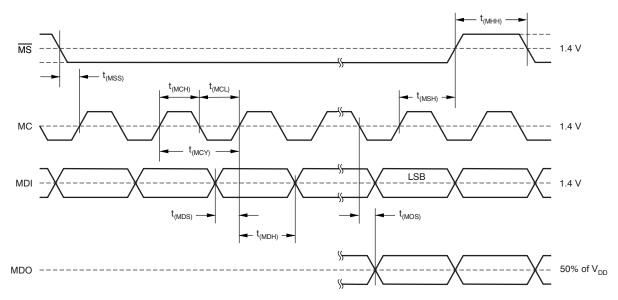


Figure 43. Control Interface Timing

Timing Characteristics for Figure 43

	PARAMETER	MIN	MAX	UNIT
t _(MCY)	MC pulse cycle time	100		ns
t _(MCL)	MC low-level time	40		ns
(MCH)	MC high-level time	40		ns
(MHH)	MS high-level time	80		ns
(MSS)	MS falling edge to MC rising edge	15		ns
(MSH)	MS hold time ⁽¹⁾	15		ns
(MDH)	MDI hold time	15		ns
(MDS)	MDI setup time	15		ns
(MOS)	MC falling edge to MDO stable		30	ns

⁽¹⁾ MC rising edge for LSB to $\overline{\text{MS}}$ rising edge.

I²C INTERFACE

The PCM1795 supports the I^2C serial bus and the data transmission protocol for standard and fast mode as a slave device. This protocol is explained in the I^2C specification 2.0.

In I²C mode, the control terminals are changed as described in Table 7.

Table 7. Control Terminals

TERMINAL NAME	TDMCA NAME	PROPERTY	DESCRIPTION					
MS	ADR0	Input	I ² C address 0					
MDI	ADR1	Input	I ² C address 1					
MC	SCL	Input	I ² C clock					
MDO	SDA	Input/output	I ² C data					

Copyright © 2009, Texas Instruments Incorporated

Slave Address

The PCM1795 has seven bits for its own slave address, as shown in Figure 44. The first five bits (MSBs) of the slave address are factory preset to 10011. The next two bits of the address byte are the device select bits that can be user-defined by the ADR1 and ADR0 terminals. A maximum of four PCM1795s can be connected on the same bus at one time. Each PCM1795 responds when it receives its own slave address.

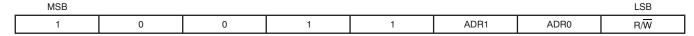


Figure 44. Slave Address

Packet Protocol

A master device must control packet protocol that consists of a start condition, slave address, read/write bit, data if write or acknowledge if read, and stop condition. The PCM1795 supports only slave receivers and slave transmitters.

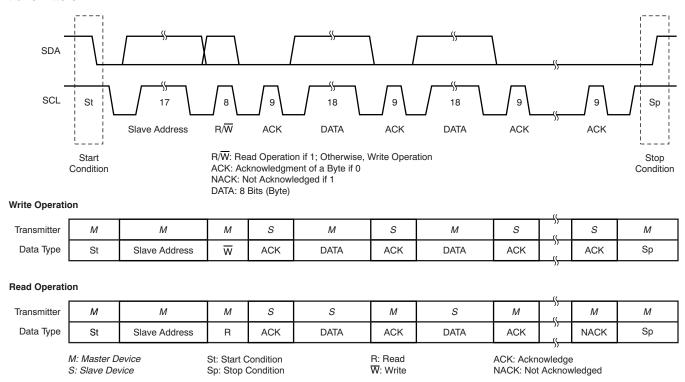


Figure 45. Basic I²C Framework

24



Write Register

A master can write to any PCM1795 registers using single or multiple accesses. The master sends a PCM1795 slave address with a write bit, a register address, and the data. If multiple access is required, the address is that of the starting register, followed by the data to be transferred. When the data are received properly, the index register is incremented by '1' automatically. When the index register reaches 0x7F, the next value is 0x00. When undefined registers are accessed, the PCM1795 does not send an acknowledgment. Figure 46 shows a diagram of the write operation.

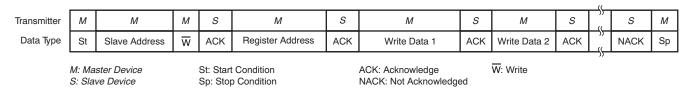


Figure 46. Write Operation

Read Register

A master can read the PCM1795 register. The value of the register address is stored in an indirect index register in advance. The master sends a PCM1795 slave address with a read bit after storing the register address. Then the PCM1795 transfers the data that the index register points to. When the data are transferred during a multiple access, the index register is incremented by '1' automatically. (When first going into read mode immediately following a write, the index register is not incremented. The master can read the register that was previously written.) When the index register reaches 0x7F, the next value is 0x00. The PCM1795 outputs some data when the index register is 0x10 to 0x1F, even if it is not defined in Table 9. Figure 47 shows a diagram of the read operation.

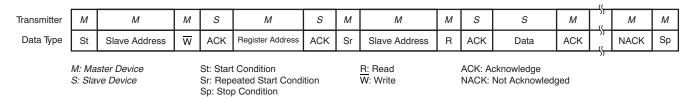


Figure 47. Read Operation

Noise Suppression

The PCM1795 incorporates noise suppression using the system clock (SCK). However, there must be no more than two noise spikes in 600 ns. The noise suppression works for SCK frequencies between 8 MHz and 40 MHz in fast mode. However, it works incorrectly under the following conditions:

Case 1:

- 1. $t_{(SCK)} > 120$ ns $(t_{(SCK)}$: period of SCK)
- 2. $t_{(HI)} + t_{(D-HD)} < t_{(SCK)} \times 5$
- 3. Spike noise exists on the first half of the SCL high pulse.
- 4. Spike noise exists on the SDA high pulse just before SDA goes low.

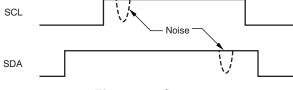


Figure 48. Case 1

When these conditions occur at the same time, the data are recognized as low.

Copyright © 2009, Texas Instruments Incorporated



Case 2:

- 1. $t_{(SCK)} > 120 \text{ ns}$
- 2. $t_{(S-HD)}$ or $t_{(RS-HD)} < t_{(SCK)} \times 5$
- 3. Spike noise exists on both SCL and SDA during the hold time.

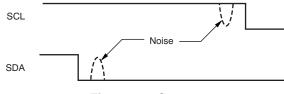


Figure 49. Case 2

When these conditions occur at the same time, the PCM1795 fails to detect a start condition.

Case 3:

- 1. $t_{(SCK)} < 50 \text{ ns}$
- 2. $t_{(SP)} > t_{(SCK)}$
- 3. Spike noise exists on SCL just after SCL goes low.
- 4. Spike noise exists on SDA just before SCL goes low.

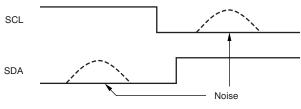


Figure 50. Case 3

When these conditions occur at the same time, the PCM1795 erroneously detects a start or stop condition.

MODE CONTROL REGISTERS

User-Programmable Mode Controls

The PCM1795 includes a number of user-programmable functions that are accessed via mode control registers. The registers are programmed using the serial control interface, as previously discussed in the SPI Interface and I₂C Interface sections. Table 8 lists the available mode-control functions, along with the default reset conditions and associated register index.

Table 8. User-Programmable Function Controls

FUNCTION	DEFAULT	REGISTER	ВІТ	РСМ	DSD	DF BYPASS
Digital attenuation control 0 dB to -120 dB and mute, 0.5-dB step	0 dB	Register 16 Register 17	ATL[7:0] (for left channel) ATR[7:0] (for right channel)	Yes	No	No
Attenuation load control Disabled, enabled	Attenuation disabled	Register 18	ATLD	Yes	No	No
Input audio data format selection 16-, 20-, 32-bit standard (right-justified) format 24-bit MSB-first left-justified format 16-/32-bit I ² S format	24-bit I ² S format	Register 18	FMT[2:0]	Yes	No	Yes
Sampling rate selection for de-emphasis Disabled, 44.1 kHz, 48 kHz, 32 kHz	De-emphasis disabled	Register 18	DMF[1:0]	Yes	Yes ⁽¹⁾	No
De-emphasis control Disabled, enabled	De-emphasis disabled	Register 18	DME	Yes	No	No
Soft mute control Soft mute disabled, enabled	Mute disabled	Register 18	MUTE	Yes	No	No
Output phase reversal Normal, reverse	Normal	Register 19	REV	Yes	Yes	Yes
Attenuation speed selection $\times 1f_S$, $\times (1/2)f_S$, $\times (1/4)f_S$, $\times (1/8)f_S$	×1 f _S	Register 19	ATS[1:0]	Yes	No	No
DAC operation control Enabled, disabled	DAC operation enabled	Register 19	OPE	Yes	Yes	Yes
Stereo DF bypass mode select Monaural, stereo	Monaural	Register 19	DFMS	Yes	No	Yes
Digital filter roll-off selection Sharp roll-off, slow roll-off	Sharp roll-off	Register 19	FLT	Yes	No	No
Infinite zero mute control Disabled, enabled	Disabled	Register 19	INZD	Yes	No	Yes
System reset control Reset operation, normal operation	Normal operation	Register 20	SRST	Yes	Yes	Yes
DSD interface mode control DSD enabled, disabled	Disabled	Register 20	DSD	Yes	Yes	No
Digital-filter bypass control DF enabled, DF bypass	DF enabled	Register 20	DFTH	Yes	No	Yes
Monaural mode selection Stereo, monaural	Stereo	Register 20	MONO	Yes	Yes	Yes
Channel selection for monaural mode data Left channel, Right channel	Left channel	Register 20	CHSL	Yes	Yes	Yes
$\Delta\Sigma$ oversampling rate selection x64 f _S , x128 f _S , x32 f _S	×64 f _S	Register 20	OS[1:0]	Yes	Yes ⁽²⁾	Yes
PCM zero output enable	Enabled	Register 21	PCMZ	Yes	No	Yes
DSD zero output enable	Disabled	Register 21	DZ[1:0]	Yes	Yes	No

When in DSD mode, DMF[1:0] is defined as DSD filter (analog FIR) performance selection. When in DSD mode, OS[1:0] is defined as DSD filter (analog FIR) operating rate selection.



Table 8. User-Programmable Function Controls (continued)

FUNCTION FUNCTION AVAILABLE ONLY FOR READ	DEFAULT	REGISTER	BIT	PCM	DSD	DF BYPASS
Zero detection flag Not zero, zero detected	Not zero = 0 Zero detected = 1	Register 22	ZFGL (for left channel) ZFGR (for right channel)	Yes	Yes	Yes
Device ID (at TDMCA)	_	Register 23	ID[4:0]	Yes	No	No

Register Map

The mode control register map is shown in Table 9. Registers 16 to 21 include an R/W bit that determines whether a register read $(R/\overline{W} = 1)$ or write $(R/\overline{W} = 0)$ operation is performed. Registers 22 and 23 are read-only.

Table 9. Mode Control Register Map

REGISTER	B15	B14	B13	B12	B11	B10	В9	B8	B7	В6	B5	B4	В3	B2	B1	В0
Register 16	R/W	0	0	1	0	0	0	0	ATL7	ATL6	ATL5	ATL4	ATL3	ATL2	ATL1	ATL0
Register 17	R/W	0	0	1	0	0	0	1	ATR7	ATR6	ATR5	ATR4	ATR3	ATR2	ATR1	ATR0
Register 18	R/W	0	0	1	0	0	1	0	ATLD	FMT2	FMT1	FMT0	DMF1	DMF0	DME	MUTE
Register 19	R/W	0	0	1	0	0	1	1	REV	ATS1	ATS0	OPE	RSV	DFMS	FLT	INZD
Register 20	R/W	0	0	1	0	1	0	0	RSV	SRST	DSD	DFTH	MONO	CHSL	OS1	OS0
Register 21	R/W	0	0	1	0	1	0	1	RSV	RSV	RSV	RSV	RSV	DZ1	DZ0	PCMZ
Register 22	R	0	0	1	0	1	1	0	RSV	RSV	RSV	RSV	RSV	RSV	ZFGR	ZFGL
Register 23	R	0	0	1	0	1	1	1	RSV	RSV	RSV	ID4	ID3	ID2	ID1	ID0

Register Definitions

	B15	B14	B13	B12	B11	B10	В9	В8	B7	B6	B 5	B4	B3	B2	B1	B0
Register 16	R/W	0	0	1	0	0	0	0	ATL7	ATL6	ATL5	ATL4	ATL3	ATL2	ATL1	ATL0
Register 17	R/W	0	0	1	0	0	0	1	ATR7	ATR6	ATR5	ATR4	ATR3	ATR2	ATR1	ATR0

R/W: Read/Write Mode Select

When $R/\overline{W} = 0$, a write operation is performed.

When $R/\overline{W} = 1$, a read operation is performed.

Default value: 0

ATx[7:0]: Digital Attenuation Level Setting

These bits are available for read and write.

Default value: 1111 1111b

Each DAC output has a digital attenuator associated with it. The attenuator can be set from 0 dB to -120 dB, in 0.5-dB steps. Alternatively, the attenuator can be set to infinite attenuation (or mute). The attenuation data for each channel can be set individually. However, the data load control (the ATLD bit of control register 18) is common to both attenuators. ATLD must be set to '1' in order to change an attenuator setting. The attenuation level can be set using Equation 1:

Attenuation level (dB) = $0.5 \text{ dB} \times (ATx[7:0]_{DEC} - 255)$

Where,

 $ATx[7:0]_{DEC} = 0$ through 255

For ATx[7:0]_{DEC} = 0 through 14, the attenuator is set to infinite attenuation. Table 10 lists the attenuation levels for various settings.

Submit Documentation Feedback



Table 10. Attenuation Levels

DECIMAL VALUE	ATTENUATION LEVEL SETTING
255	0 dB, no attenuation (default)
254	-0.5 dB
253	-1.0 dB
_	_
16	-119.5 dB
15	-120.0 dB
14	Mute
_	_
0	Mute
	255 254 253 — 16 15 14 —

	B15	B14	B13	B12	B11	B10	В9	B8	В7	B6	B5	В4	В3	B2	B1	B0	
Register 18	R/W	0	0	1	0	0	1	0	ATLD	FMT2	FMT1	FMT0	DMF1	DMF0	DME	MUTE	

R/W: Read/Write Mode Select

When $R/\overline{W} = 0$, a write operation is performed.

When $R/\overline{W} = 1$, a read operation is performed.

Default value: 0

ATLD: Attenuation Load Control

This bit is available for read and write.

Default value: 0

ATLD	Attenuation Control Setting
ATLD = 0	Attenuation control disabled (default)
ATLD = 1	Attenuation control enabled

The ATLD bit is used to enable loading of the attenuation data contained in registers 16 and 17. When ATLD = 0, the attenuation settings remain at the previously programmed levels, ignoring new data loaded from registers 16 and 17. When ATLD = 1, attenuation data written to registers 16 and 17 is loaded normally.

FMT[2:0]: Audio Interface Data Format

These bits are available for read and write.

Default value: 101

FMT[2:0]	Audio Data Format Selection
000	16-bit standard format, right-justified data, BCK ≥ x32 f _S
001	32-bit standard format, right-justified data, BCK ≥ x64 f _S
010	24-bit standard format, right-justified data, BCK ≥ x48 f _S
011	24-bit MSB-first, left-justified format data, BCK ≥ x48 f _S
100	32-bit I^2 S format data, BCK ≥ x64 f_S
101	24-bit I ² S format data (default), BCK ≥ x48 f _S
110	Reserved
111	Reserved



The FMT[2:0] bits are used to select the data format for the serial audio interface.

For the external digital filter interface mode (DFTH mode), this register is operated as shown in the *Application* for External Digital Filter Interface section.

DMF[1:0]: Sampling Frequency Selection for the De-Emphasis Function

These bits are available for read and write.

Default value: 00

DMF[1:0]	De-Emphasis Sampling Frequency Selection
00	Disabled (default)
01	48 kHz
10	44.1 kHz
11	32 kHz

The DMF[1:0] bits are used to select the sampling frequency used by the digital de-emphasis function when it is enabled by setting the DME bit. The de-emphasis curves are shown in the *Typical Characteristics* section.

For the DSD mode, analog FIR filter performance can be selected using this register. A register map and filter response plots are shown in the *Application For DSD Format (DSD Mode) Interface* section.

DME: Digital De-Emphasis Control

This bit is available for read and write.

Default value: 0

DME	De-Emphasis Setting
DME = 0	De-emphasis disabled (default)
DME = 1	De-emphasis enabled

The DME bit is used to enable or disable the de-emphasis function for both channels.

MUTE: Soft Mute Control

This bit is available for read and write.

Default value: 0

MUTE	Soft Mute Setting
MUTE = 0	Soft mute disabled (default)
MUTE = 1	Soft mute enabled

The MUTE bit is used to enable or disable the soft mute function for both channels.

Soft mute is operated as a 256-step attenuator. The speed for each step to $-\infty$ dB (mute) is determined by the attenuation rate selected in the ATS register.

	B15	B14	B13	B12	B11	B10	В9	B8	B7	B6	B5	B4	В3	B2	B1	B0	_
Register 19	R/W	0	0	1	0	0	1	1	REV	ATS1	ATS0	OPE	RSV	DMFS	FLT	INZD	l

R/W: Read/Write Mode Select

When $R/\overline{W} = 0$, a write operation is performed.

When $R/\overline{W} = 1$, a read operation is performed.

Default value: 0

30



REV: Output Phase Reversal

This bit is available for read and write.

Default value: 0

REV	Output Setting
REV = 0	Normal output (default)
REV = 1	Inverted output

The REV bit is used to invert the output phase for both channels.

ATS[1:0]: Attenuation Rate Select

These bits are available for read and write.

Default value: 00

ATS[1:0]	Attenuation Rate Selection
00	Every LRCK (default)
01	LRCK/2
10	LRCK/4
11	LRCK/8

The ATS[1:0] bits are used to select the rate at which the attenuator is decremented/incremented during level transitions.

OPE: DAC Operation Control

This bit is available for read and write.

Default value: 0

OPE	DAC Operation Control
OPE = 0	DAC operation enabled (default)
OPE = 1	DAC operation disabled

The OPE bit is used to enable or disable the analog output for both channels. Disabling the analog outputs forces them to the bipolar zero level (BPZ) even if audio data are present on the input.

DFMS: Stereo DF Bypass Mode Select

This bit is available for read and write.

Default value: 0

DFMS	Mode Selection
DFMS = 0	Monaural (default)
DFMS = 1	Stereo input enabled

The DFMS bit is used to enable stereo operation in DF bypass mode. In the DF bypass mode, when DFMS is set to '0', the pin for the input data are DATA (pin 5) only; therefore, the PCM1795 operates as a monaural DAC. When DFMS is set to '1', the PCM1795 can operate as a stereo DAC with inputs of the left channel and right channel data on ZEROL (pin 1) and ZEROR (pin 2), respectively.

Copyright © 2009, Texas Instruments Incorporated



FLT: Digital Filter Roll-Off Control

This bit is available for read and write.

Default value: 0

FLT	Roll-Off Control
FLT = 0	Sharp roll-off (default)
FLT = 1	Slow roll-off

The FLT bit is used to select the digital filter roll-off characteristic. The filter responses for these selections are shown in the *Typical Characteristics* section.

INZD: Infinite Zero Detect Mute Control

This bit is available for read and write.

Default value: 0

INZD	Infinite Zero Detect Mute Setting
INZD = 0	Infinite zero detect mute disabled (default)
INZD = 1	Infinite zero detect mute enabled

The INZD bit is used to enable or disable the zero detect mute function. Setting INZD to '1' forces muted analog outputs to hold a bipolar zero level when the PCM1795 detects a zero condition in both channels. The infinite zero detect mute function is not available in the DSD mode.

	B15	B14	B13	B12	B11	B10	В9	B8	B7	B6	B 5	B4	B3	B2	B1	B0	_
Register 20	R/W	0	0	1	0	1	0	0	RSV	SRST	DSD	DFTH	MONO	CHSL	OS1	OS0	1

R/W: Read/Write Mode Select

When $R/\overline{W} = 0$, a write operation is performed.

When $R/\overline{W} = 1$, a read operation is performed.

Default value: 0

SRST: System Reset Control

This bit is available for write only.

Default value: 0

SRST	System Reset Control
SRST = 0	Normal operation (default)
SRST = 1	System reset operation (generate one reset pulse)

The SRST bit is used to reset the PCM1795 to the initial system condition.

DSD: DSD Interface Mode Control

This bit is available for read and write.

Default value: 0

DSD	DSD Interface Mode Control
DSD = 0	DSD interface mode disabled (default)
DSD = 1	DSD interface mode enabled

The DSD bit is used to enable or disable the DSD interface mode.

32



DFTH: Digital Filter Bypass (or Through Mode) Control

This bit is available for read and write.

Default value: 0

DFTH	Digital Filter Control
DFTH = 0	Digital filter enabled (default)
DFTH = 1	Digital filter bypassed for external digital filter

The DFTH bit is used to enable or disable the external digital filter interface mode.

MONO: Monaural Mode Selection

This bit is available for read and write.

Default value: 0

MONO	Mode Selection
MONO = 0	Stereo mode (default)
MONO = 1	Monaural mode

The MONO function is used to change operation mode from the normal stereo mode to the monaural mode. When the monaural mode is selected, both DACs operate in a balanced mode for one channel of audio input data. Channel selection is available for left-channel or right-channel data, determined by the *CHSL bit*.

CHSL: Channel Selection for Monaural Mode

This bit is available for read and write.

Default value: 0

CHSL	Channel Selection
CHSL = 0	Left channel selected (default)
CHSL = 1	Right channel selected

This bit is available when MONO = 1.

The CHSL bit selects left-channel or right-channel data to be used in monaural mode.

OS[1:0]: ΔΣ Oversampling Rate Selection

These bits are available for read and write.

Default value: 00

OS[1:0]	Operating Speed Selection
00	64 times f _S (default)
01	32 times f _S
10	128 times f _S
11	Reserved

The OS bits are used to change the oversampling rate of $\Delta\Sigma$ modulation. Use of this function enables the designer to stabilize the conditions at the post low-pass filter for different sampling rates. As an application example, programming to set 128 times in 44.1-kHz operation, 64 times in 96-kHz operation, or 32 times in 192-kHz operation allows the use of only a single type (cut-off frequency) of post low-pass filter. The 128-f_S oversampling rate is not available at sampling rates above 100 kHz. If the 128-f_S oversampling rate is selected, a system clock of more than 256 f_S is required.

In DSD mode, these bits are used to select the speed of the bit clock for DSD data coming into the analog FIR filter.



	B15	B14	B13	B12	B11	B10	В9	B8	B7	B6	B5	B4	В3	B2	B1	В0
Register 21	R/W	0	0	1	0	1	0	1	RSV	RSV	RSV	RSV	RSV	DZ1	DZ0	PCMZ

R/W: Read/Write Mode Select

When $R/\overline{W} = 0$, a write operation is performed.

When $R/\overline{W} = 1$, a read operation is performed.

Default value: 0

DZ[1:0]: DSD Zero Output Enable

These bits are available for read and write.

Default value: 00

DZ[1:0]	Zero Output Enable
00	Disabled (default)
01	Even pattern detect 1 x 96h pattern detect

The DZ bits are used to enable or disable the output zero flags and to select the zero pattern in DSD mode.

PCMZ: PCM Zero Output Enable

These bits are available for read and write.

Default value: 1

PCMZ	PCM Zero Output Setting
PCMZ = 0	PCM zero output disabled
PCMZ = 1	PCM zero output enabled (default)

The PCMZ bit is used to enable or disable the output zero flags in PCM mode and the external DF mode.

	B15	B14	B13	B12	B11	B10	В9	B8	B7	B6	B5	B4	В3	B2	B1	B0	
Register 22	R	0	0	1	0	1	1	0	RSV	RSV	RSV	RSV	RSV	RSV	ZFGR	ZFGL	1

R: Read Mode Select

Value is always '1', specifying the readback mode.

ZFGx: Zero-Detection Flag

Where x = L or R, corresponding to the DAC output channel. These bits are available only for readback.

Default value: 00

ZFGx	Zero Detection
ZFGx = 0	Not zero
ZFGx = 1	Zero detected

These bits show zero conditions. The status is the same as that of the zero flags at ZEROL (pin 1) and ZEROR (pin 2). See *Zero Detect* in the *Function Descriptions* section.

Submit Documentation Feedback



	B15	B14	B13	B12	B11	B10	В9	B8	B7	B6	B5	B4	В3	B2	B1	В0
Register 23	R	0	0	1	0	1	1	1	RSV	RSV	RSV	ID4	ID3	ID2	ID1	ID0

Read Mode Select

Value is always '1', specifying the readback mode.

ID[4:0]: Device ID

The ID[4:0] bits hold a device ID in the TDMCA mode.

APPLICATION INFORMATION

TYPICAL CONNECTION DIAGRAM IN PCM MODE

Figure 51 shows a typical application circuit for PCM mode operation.

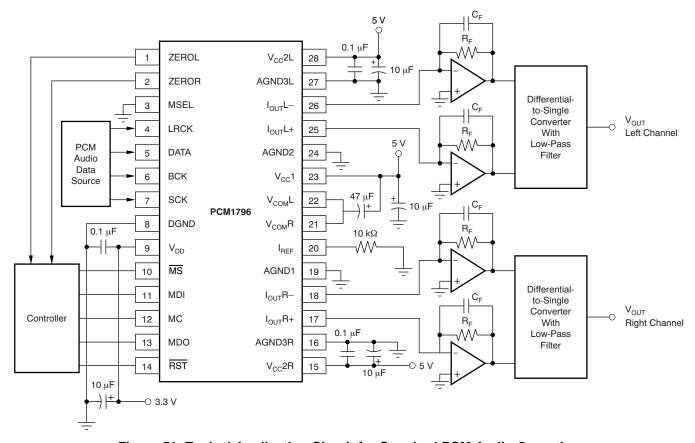


Figure 51. Typical Application Circuit for Standard PCM Audio Operation



APPLICATION CIRCUIT

The design of the application circuit is very important in order to actually realize the high S/N ratio of which the PCM1795 is capable, because noise and distortion that are generated in an application circuit are not negligible.

In the third-order, low-pass filter (LPF) circuit of Figure 52, the output level of 2.1 V RMS and 123-dB signal-to-noise ratio is achieved.

Figure 53 shows a circuit for the DSD mode, which is a fourth-order LPF in order to reduce the out-of-band noise.

I/V Section

The current of the PCM1795 on each of the output pins ($I_{OUT}L+$, $I_{OUT}L-$, $I_{OUT}R+$, $I_{OUT}R-$) is 4 mA_{PP} at 0 dB (full-scale). The voltage output level of the current-to-voltage (I/V) converter, V_I , is given by Equation 2: $V_I = 4 \text{ mA}_{PP} \times R_F$

Where:

R_F = feedback resistance of the I/V converter

An NE5534 operational amplifier is recommended for the I/V circuit to obtain the specified performance. Dynamic performance such as the gain bandwidth, settling time, and slew rate of the operational amplifier affects the audio dynamic performance of the I/V section.

Differential Section

The PCM1795 voltage outputs are followed by differential amplifier stages that sum the differential signals for each channel, creating a single-ended I/V op-amp output. In addition, the differential amplifiers provide a low-pass filter function.

The operational amplifier recommended for the differential circuit is the low-noise type.

3

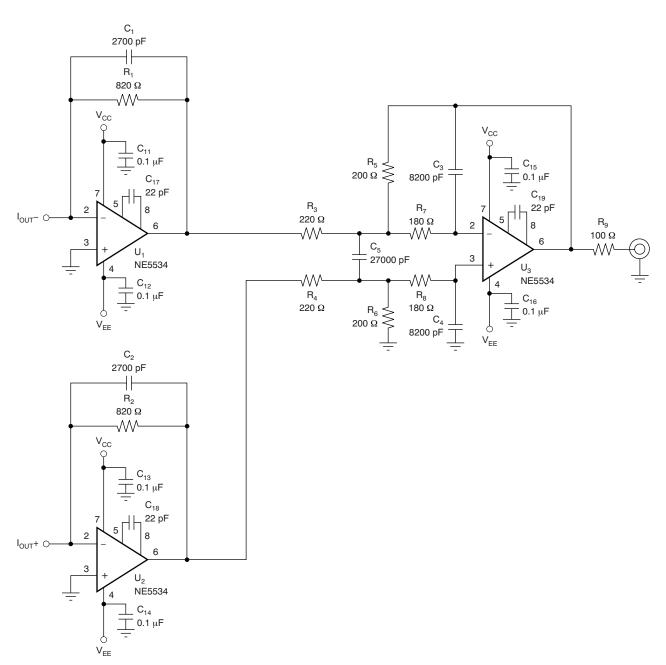


Figure 52. Measurement Circuit for PCM





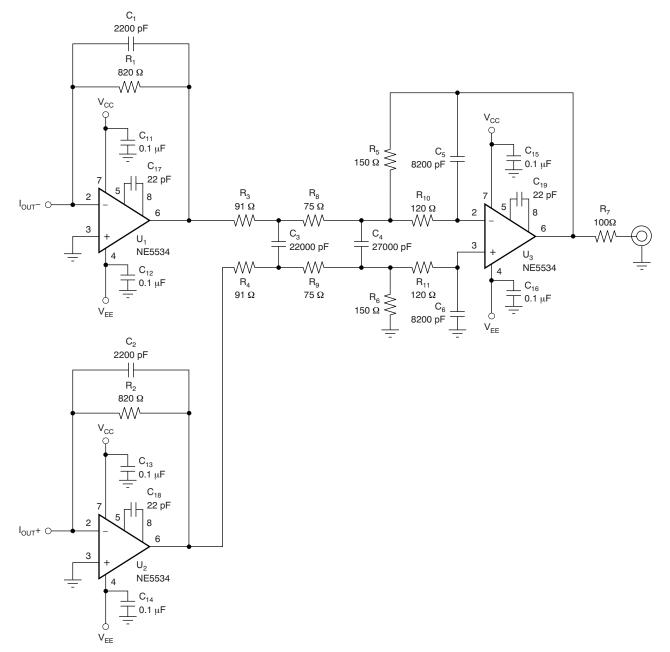
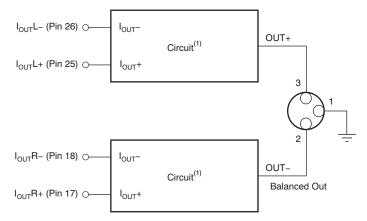


Figure 53. Measurement Circuit for DSD



(1) Circuit corresponds to Figure 52.

Figure 54. Measurement Circuit for Monaural Mode

APPLICATION FOR EXTERNAL DIGITAL FILTER INTERFACE

Figure 55 shows the connection diagram for an external digital filter.

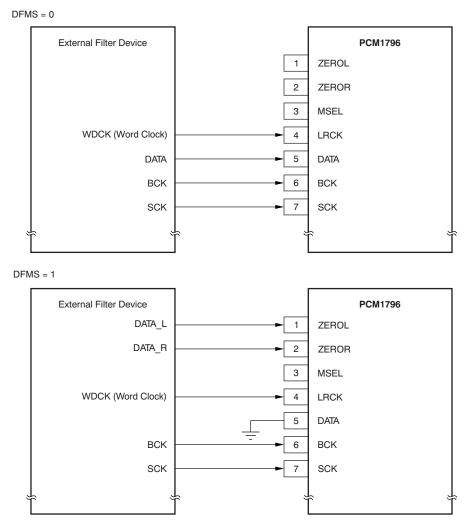


Figure 55. Connection Diagram for External Digital Filter (Internal DF Bypass Mode) Application



Application for Interfacing With an External Digital Filter

For some applications, it may be desirable to use an external digital filter to perform the interpolation function, as it can provide improved stop-band attenuation when compared to the internal digital filter of the PCM1795.

The PCM1795 supports several external digital filters, including:

- Texas Instruments DF1704 and DF1706
- Pacific Microsonics PMD200 HDCD filter/decoder IC
- Programmable digital signal processors (DSPs)

The external digital filter application mode is accessed by programming the following bits in the corresponding control register:

• DFTH = 1 (register 20)

The pins used to provide the serial interface for the external digital filter are illustrated in Figure 55. The word clock (WDCK) signal must be operated at 8 times or 4 times the desired sampling frequency, f_S.

Pin Assignment When Using the External Digital Filter Interface

- · LRCK (pin 4): WDCK as word clock input
- BCK (pin 6): Bit clock for audio data
- DATA (pin 5): Monaural audio data input when the DFMS bit is not set to '1'
- ZEROL (pin 1): DATAL as left channel audio data input when the DFMS bit is set to '1'
- ZEROR (pin 2): DATAR as right channel audio data input when the DFMS bit is set to '1'

Audio Format

The PCM1795 in the external digital filter interface mode supports right-justified audio formats including 16-bit, 24-bit, and 32-bit audio data, as shown in Figure 56. The audio format is selected by the FMT[2:0] bits of control register 18.

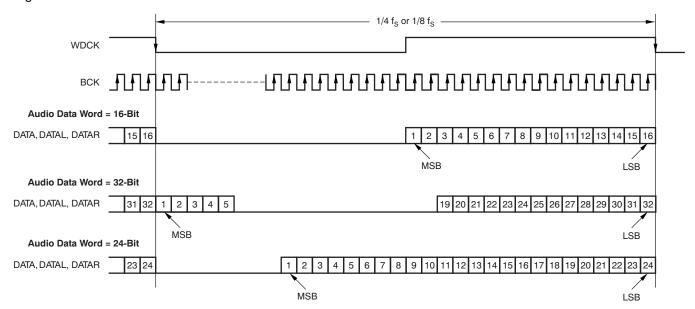


Figure 56. Audio Data Input Format for External Digital Filter (Internal DF Bypass Mode) Application

40

System Clock (SCK) and Interface Timing

The PCM1795 in an application using an external digital filter requires the synchronization of WDCK and the system clock. The system clock is phase-free with respect to WDCK. Interface timing among WDCK, BCK, DATA, DATAL, and DATAR is shown in Figure 57 and Table 11.

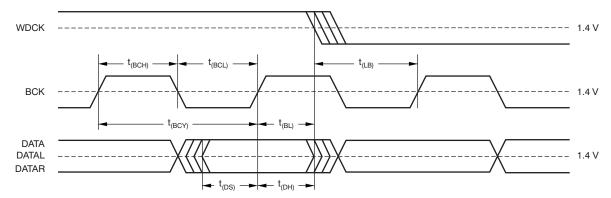


Figure 57. Audio Interface Timing for External Digital Filter (Internal DF Bypass Mode) Application

Table 11. Timing Characteristics for Figure 57

	PARAMETER	MIN	MAX	UNIT
t _(BCY)	BCK pulse cycle time	20		ns
t _(BCL)	BCK pulse duration, low	7		ns
t _(BCH)	BCK pulse duration, high	7		ns
t _(BL)	BCK rising edge to WDCK falling edge	5		ns
t _(LB)	WDCK falling edge to BCK rising edge	5		ns
t _(DS)	DATA, DATAL, DATAR setup time	5		ns
t _(DH)	DATA, DATAL, DATAR hold time	5		ns



FUNCTIONS AVAILABLE IN THE EXTERNAL DIGITAL FILTER MODE

The external digital filter mode is selected by setting DSD = 0 (register 20, B5) and DFTH = 1 (register 20, B4).

The external digital filter mode allows access to the majority of the PCM1795 mode control functions.

Table 12 shows the register mapping available when the external digital filter mode is selected, along with descriptions of functions that are modified when using this mode selection.

Table 12. External Digital Filter Register Map

REGISTER	B15	B14	B13	B12	B11	B10	В9	В8	B7	В6	B5	B4	В3	B2	B1	В0
Register 16	R/W	0	0	1	0	0	0	0	X ⁽¹⁾	Х	Х	Х	Х	Х	Х	Х
Register 17	R/W	0	0	1	0	0	0	1	Х	Х	Х	Х	Х	Х	Х	Х
Register 18	R/W	0	0	1	0	0	1	0	Х	FMT2	FMT1	FMT0	Х	Х	Х	Х
Register 19	R/W	0	0	1	0	0	1	1	REV	Х	Х	OPE	Х	DFMS	Х	INZD
Register 20	R/W	0	0	1	0	1	0	0	Х	SRST	0	1	MONO	CHSL	OS1	OS0
Register 21	R/W	0	0	1	0	1	0	1	Х	Х	Х	Х	Х	Х	Х	PCMZ
Register 22	R	0	0	1	0	1	1	0	Х	X	Х	Х	X	Χ	ZFGR	ZFGL

⁽¹⁾ Function is disabled. No operation even if data bit is set.

FMT[2:0]: Audio Data Format Selection

Default value: 000

FMT[2:0]	Audio Data Format Selection
000	16-bit right-justified format
001	32-bit right-justified format
010	24-bit right-justified format (default)
Other	N/A

OS[1:0]: ΔΣ Modulator Oversampling Rate Selection

Default value: 00

OS[1:0]	Operation Speed Selection
00	8 times WDCK (default)
01	4 times WDCK
10	16 times WDCK
11	Reserved

The effective oversampling rate is determined by the oversampling performed by both the external digital filter and the $\Delta\Sigma$ modulator. For example, if the external digital filter is 8× oversampling, and OS[1:0] = 00 is selected, then the $\Delta\Sigma$ modulator oversamples by 8×, resulting in an effective oversampling rate of 64×. The 16× WDCK oversampling rate is not available above a 100-kHz sampling rate. If the oversampling rate selected is 16× WDCK, the system clock frequency must be over 256 f_S.

42

Product Folder Link(s): PCM1795

APPLICATION FOR DSD FORMAT (DSD MODE) INTERFACE

Figure 58 shows a connection diagram for DSD mode.

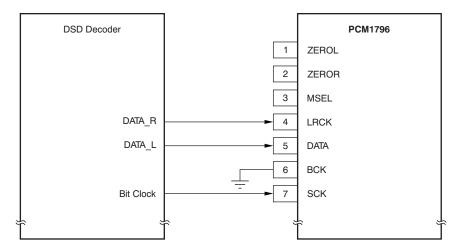


Figure 58. Connection Diagram in DSD Mode

Feature

This mode is used for interfacing directly to a DSD decoder, which is found in Super Audio CD™ (SACD) applications.

The DSD mode is accessed by programming the following bit in the corresponding control register.

DSD = 1 (register 20)

The DSD mode provides a low-pass filtering function. The filtering is provided using an analog FIR filter structure. Four FIR responses are available and are selected by the DMF[1:0] bits of control register 18.

The DSD bit must be set before inputting DSD data; otherwise, the PCM1795 erroneously detects the TDMCA mode and commands are not accepted through the serial control interface.

Pin Assignment When Using DSD Format Interface

Several pins are redefined for DSD mode operation. These include:

- DATA (pin 5): DSDL as left-channel DSD data input
- LRCK (pin 4): DSDR as right-channel DSD data input
- SCK (pin 7): DBCK as bit clock for DSD data
- BCK (pin 6): Set low (N/A)

Requirements for System Clock

For operation in DSD mode, the bit clock (DBCK) is required on pin 7 of the PCM1795. The frequency of the bit clock can be *N* times the sampling frequency. Generally, *N* is 64 in DSD applications.

The interface timing between the bit clock and DSDL and DSDR is required to meet the setup and hold time specifications shown in Figure 60 and Table 13.

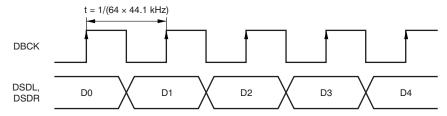


Figure 59. Normal Data Output Form From DSD Decoder

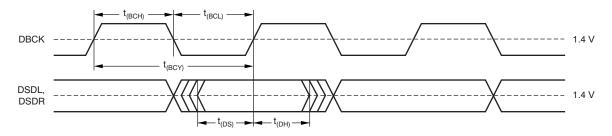


Figure 60. Timing for DSD Audio Interface

Table 13. Timing Characteristics for Figure 60

	PARAMETER	MIN	MAX	UNIT
t _(BCY)	DBCK pulse cycle time	85 ⁽¹⁾		ns
t _(BCH)	DBCK high-level time	30		ns
t _(BCL)	DBCK low-level time	30		ns
t _(DS)	DSDL, DSDR setup time	10		ns
t _(DH)	DSDL, DSDR hold time	10		ns

^{(1) 2.8224} MHz × 4. (2.8224 MHz = 64 × 44.1 kHz. This value is specified as a sampling rate of DSD.

DSD MODE CONFIGURATION AND FUNCTION CONTROLS

Configuration for the DSD Interface Mode

The DSD interface mode is selected by setting DSD = 1 (register 20, B5).

Table 14. DSD Mode Register Map

REGISTER	B15	B14	B13	B12	B11	B10	В9	В8	B7	В6	В5	B4	В3	B2	B1	В0
Register 16	R/W	0	0	1	0	0	0	0	X ⁽¹⁾	Х	Х	Х	Х	Х	Х	Х
Register 17	R/W	0	0	1	0	0	0	1	Х	Х	Х	Х	Х	Х	Х	Х
Register 18	R/W	0	0	1	0	0	1	0	Х	Х	Х	Х	DMF1	DMF0	Х	Х
Register 19	R/W	0	0	1	0	0	1	1	REV	Х	Х	OPE	Х	Х	Х	Х
Register 20	R/W	0	0	1	0	1	0	0	Х	SRST	1	Х	MONO	CHSL	OS1	OS0
Register 21	R	0	0	1	0	1	0	1	Х	Х	Х	Х	Х	DZ1	DZ0	Х
Register 22	R	0	0	1	0	1	1	0	Х	Х	Х	Х	Х	Х	ZFGR	ZFGL

(1) Function is disabled. No operation even if data bit is set.

Submit Documentation Feedback



DMF[1:0]: Analog-FIR Performance Selection

Default value: 00

DMF[1:0]	Analog-FIR Performance Selection
00	FIR-1 (default)
01	FIR-2
10	FIR-3
11	FIR-4

Plots for the four analog finite impulse response (FIR) filter responses are shown in the *Analog FIR Filter Performance in DSD Mode* section of the Typical Characteristics.

OS[1:0]: Analog-FIR Operation-Speed Selection

Default value: 00

OS[1:0]	Operating Speed Selection
00	f _{DBCK} (default)
01	f _{DBCK} /2
10	Reserved
11	f _{DBCK} /4

The OS bit in the DSD mode is used to select the operating rate of the analog FIR. The OS bits must be set before setting the DSD bit to '1'.

TDMCA INTERFACE FORMAT

The PCM1795 supports the time-division-multiplexed command and audio (TDMCA) data format to simplify the host control serial interface. TDMCA format is designed not only for the multichannel buffered serial port description (McBSP) of TI DSPs but also for any programmable devices. TDMCA format can transfer not only audio data but also command data, so that it can be used together with any kind of device that supports TDMCA format. The TDMCA frame consists of a command field, extended command field, and some audio data fields. Those audio data are transported to IN devices (such as a DAC) and/or from OUT devices (such as an ADC). The PCM1795 is an IN device. LRCK and BCK are used with both IN and OUT devices so that the sample frequency of all devices in a system must be the same. The TDMCA mode supports a maximum of 30 device IDs. The maximum number of audio channels depends on the BCK frequency.

TDMCA Mode Determination

The PCM1795 recognizes the TDMCA mode automatically when it receives an LRCK signal with a pulse duration of two BCK clocks. If the TDMCA mode operation is not needed, the duty cycle of LRCK must be 50%. Figure 61 shows the LRCK and BCK timing that determines the TDMCA mode. The PCM1795 enters TDMCA mode after two continuous TDMCA frames. Any TDMCA commands can be issued during the next TDMCA frame after entering TDMCA mode.

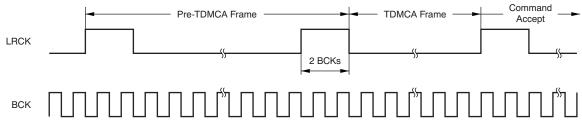


Figure 61. LRCK and BCK Timing for Determination of TDMCA Mode



TDMCA Terminals

TDMCA requires six signals: four signals are for the command and audio data interface, and one pair for daisy-chaining. These signals can be shared as shown in Table 15. The DO signal has a 3-state output so that it can be connected directly to other devices.

Tabla	15	TDMC	Δ T_{Δ}	rmina	le
Iable	IJ.		A 16	: : : : : : : : : a	13

TERMINAL NAME	TDMCA NAME	PROPERTY	DESCRIPTION
LRCK	LRCK	Input	TDMCA frame start signal; it must be the same as the sampling frequency
ВСК	вск	Input	TDMCA clock; its frequency must be high enough to communicate a TDMCA frame within an LRCK cycle
DATA	DI	Input	TDMCA command and audio data input signal
MDO	DO	Output	TDMCA command data 3-state output signal
MC	DCI	Input	TDMCA daisy-chain input signal
MS	DCO	Output	TDMCA daisy-chain output signal

Device ID Determination

TDMCA mode also supports a multichip implementation in one system. This capability means that a host controller (DSP) can simultaneously support several TDMCA devices, which can be of the same type or different types, including PCM devices. The PCM devices are categorized as either IN devices, OUT devices, IN/OUT devices, and NO devices. The IN device has an input port to receive audio data; the OUT device has an output port to supply audio data; the IN/OUT device has both input and output ports for audio data; and the NO device has no port for audio data, but requires command data from the host. A DAC is an IN device; an ADC is an OUT device; a codec is an IN/OUT device; and a PLL is a NO device. The PCM1795 is an IN device. For the host controller to distinguish the devices, each device is assigned its own device ID by the daisy-chain. The devices obtain their own device IDs automatically by connecting the DCI to the DCO of the preceding device and the DCO to the DCI of the following device in the daisy-chain. The daisy-chains are categorized as the IN chain and the OUT chain, which are completely independent and equivalent. Figure 62 shows an example daisy-chain connection. If a system must chain the PCM1795 and a NO device in the same IN or OUT chain, the NO device must be chained at the back end of the chain because it does not require any audio data. Figure 63 shows an example TDMCA system including an IN chain and an OUT chain with a TI DSP. For a device to get its own device ID, the DID signal must be set to '1' (see the Command Field section for details), and LRCK and BCK must be driven in the TDMCA mode for all PCM devices that are chained. The device at the top of the chain knows its device ID is '1' because its DCI is fixed high. Other devices count the BCK pulses and observe the respective DCI signal to determine ID and position in the chain. Figure 64 shows the initialization of each device ID.

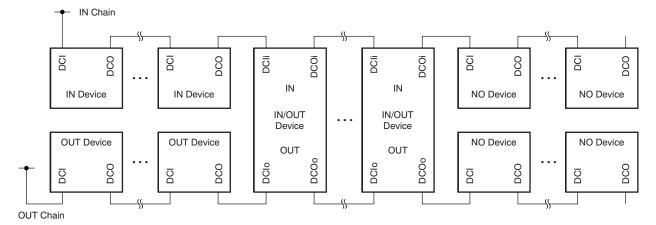


Figure 62. Daisy-Chain Connection Example

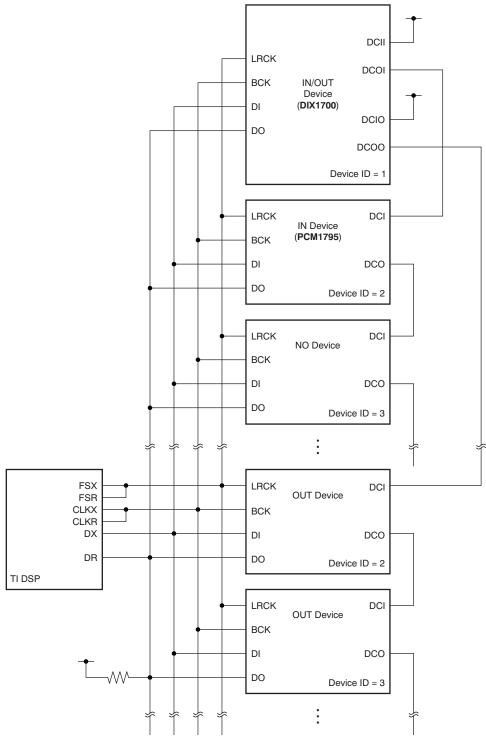


Figure 63. IN Daisy-Chain and OUT Daisy-Chain Connection Example for a Multichip System



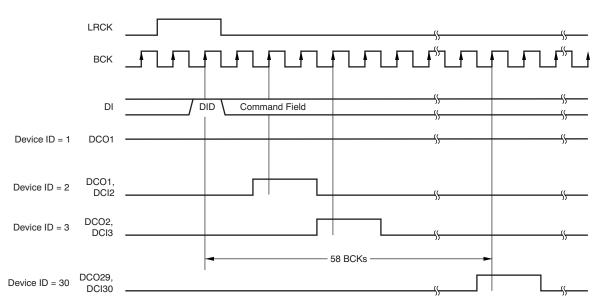


Figure 64. Device ID Determination Sequence

TDMCA Frame

In general, the TDMCA frame consists of the command field, extended command (EMD) field, and audio data fields. All fields are 32 bits in length, but the lowest byte has no meaning. The MSB is transferred first for each field. The command field is always transferred as the first packet of the frame. The EMD field is transferred if the EMD flag of the command field is high. If any EMD packets are transferred, no audio data follow the EMD packets. This frame is for quick system initialization. All devices of a daisy-chain should respond to the command field and extended command field. The PCM1795 has two audio channels that can be selected by OPE (register 19). If the OPE bit is not set to high, those audio channels are transferred. Figure 65 shows the general TDMCA frame. If some DACs are enabled, but corresponding audio data packets are not transferred, the analog outputs are unpredictable.

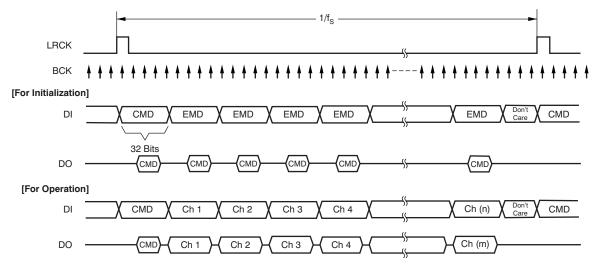


Figure 65. General TDMCA Frame

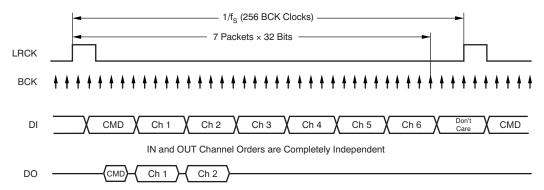


Figure 66. TDMCA Frame Example of Six-Channel DAC and Two-Channel ADC With Command Read

Command Field

The normal command field is defined as shown in Figure 67. When the DID bit (MSB) is '1', this frame is used only for device ID determination, and all remaining bits in the field are ignored.



Figure 67. Normal Command Field

Bit 31: Device ID enable flag

The PCM1795 operates to get its own device ID for TDMCA initialization if this bit is high.

Bit 30: Extended command enable flag

The EMD packet is transferred if this bit is high; otherwise, it is skipped. Once this bit is high, this frame does not contain any audio data. This is for system initialization.

Bit 29: Daisy-chain selection flag

A high setting designates OUT-chain devices, low designates IN-chain devices. The PCM1795 is an IN device, so the DCS bit must be set low.

Bits[28:24]: Device ID

The device ID is five bits in length and it can be defined. These bits identify the order of a device in the IN or OUT daisy-chain. The top of the daisy-chain defines device ID 1 and successive devices are numbered 2, 3, 4, etc. All devices for which the DCI is fixed high are also defined as ID 1. The maximum device ID is 30 each in the IN and OUT chains. If a device ID of 0x1F is used, all devices are selected as broadcast when in the write mode. If a device ID of 0x00 is used, no device is selected.

Bit 23: Command Read/Write flag

If this bit is high, the command is a read operation.

Bits[22:16]: Register ID

The register ID is seven bits in length.

Bits[15:8]: Command data

The command data are eight bits in length. Any valid data can be chosen for each register.

Bits[7:0]: Not used

These bits are never transported when a read operation is performed.

Extended Command Field

The extended command field is the same as the command field, except that it does not have a DID flag. Figure 68 defines the extended command field.

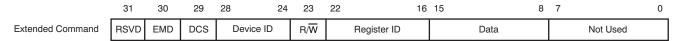


Figure 68. Extended Command Field

Audio Fields

The audio field is 32 bits in length and the audio data are transferred MSB first, so the other fields must be filled with 0s as shown in Figure 69.



Figure 69. Audio Field Example

TDMCA Register Requirements

The TDMCA mode requires device ID and audio channel information, as previously described. The OPE bit in register 19 indicates audio channel availability and register 23 indicates the device ID. Register 23 is used only in the TDMCA mode; see the mode control register map of Table 9.

Register Write/Read Operation

The command supports register write and read operations. If the command requests to read one register, the read data are transferred on DO during the data phase of the timing cycle. The DI signal can be retrieved at the positive edge of BCK, and the DO signal is driven at the negative edge of BCK. DO is activated one BCK cycle early to compensate for the output delay caused by high impedance. Figure 70 shows the TDMCA write and read timing.

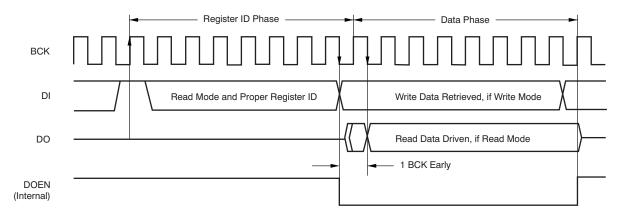


Figure 70. TDMCA Write and Read Operation Timing

50

TDMCA Mode Operation

DCO specifies the owner of the next audio channel in TDMCA mode operation. When a device retrieves its own audio channel data, DCO goes high during the last audio channel period. Figure 71 shows the DCO output timing in TDMCA mode operation. The host controller ignores the behavior of DCI and DCO. DCO indicates the last audio channel of each device. Therefore, DCI means the next audio channel is allocated.

If some devices are skipped because of no active audio channel, the skipped devices must notify the next device that the DCO will be passed through the next DCI. Figure 72 and Figure 73 show DCO timing with skip operation. Figure 74 and Table 16 show the ac timing of the daisy-chain signals.

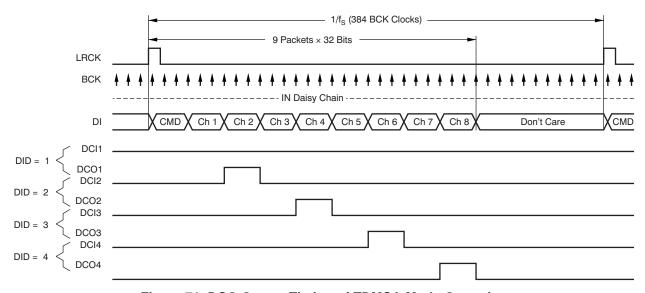


Figure 71. DCO Output Timing of TDMCA Mode Operation

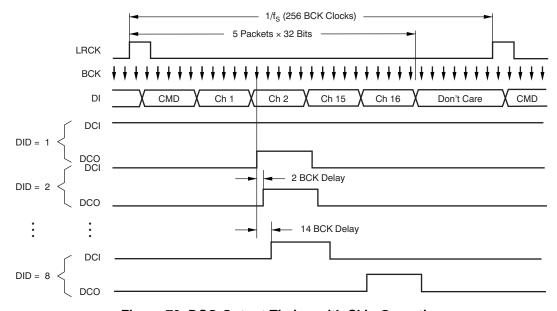


Figure 72. DCO Output Timing with Skip Operation



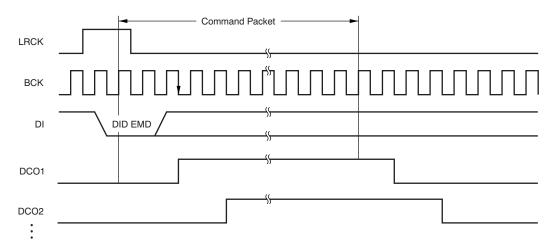


Figure 73. DCO Output Timing with Skip Operation (for Command Packet 1)

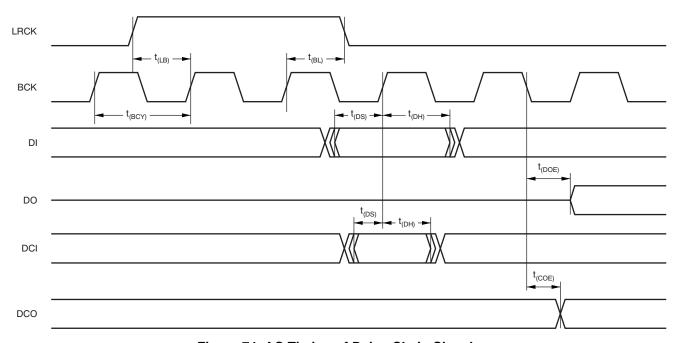


Figure 74. AC Timing of Daisy-Chain Signals

Table 16. Timing Characteristics for Figure 74

	PARAMETER	MIN	MAX	UNIT
t _(BCY)	BCK pulse cycle time	20		ns
t _(LB)	LRCK setup time	0		ns
t _(BL)	LRCK hold time	3		ns
t _(DS)	DI setup time	0		ns
t _(DH)	DI hold time	3		ns
t _(DS)	DCI setup time	0		ns
t _(DH)	DCI hold time	3		ns
t _(DOE)	DO output delay ⁽¹⁾		8	ns
t _(COE)	DCO output delay ⁽¹⁾		6	ns

(1) Load capacitance is 10 pF.

2 Submit Documentation Feedback

ANALOG OUTPUT

Table 17 and Figure 75 show the relationship between the digital input code and analog output.

Table 17. Analog Output Current and Voltage⁽¹⁾

PARAMETER	800000 (-FS)	000000 (BPZ)	7FFFFF (+FS)
I _{OUT} N (mA)	-1.5	-3.5	-5.5
I _{OUT} P (mA)	-5.5	3.5	-1.5
V _{OUT} N (V)	-1.23	-2.87	-4.51
V _{OUT} P (V)	-4.51	-2.87	-1.23
V _{OUT} (V)	-2.91	0	2.91

(1) $V_{OUT}N$ is the output of U1, $V_{OUT}P$ is the output of U2, and V_{OUT} is the output of U3 in the measurement circuit of Figure 52.

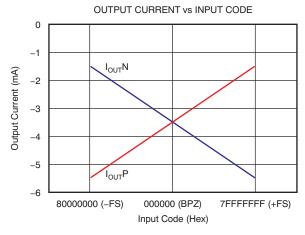


Figure 75. Relationship Between Digital Input and Analog Output

PACKAGE OPTION ADDENDUM

www.ti.com 19-Oct-2009

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
PCM1795DB	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCM1795DBR	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

www.ti.com 7-Dec-2011

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM1795DBR	SSOP	DB	28	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

PACKAGE MATERIALS INFORMATION

www.ti.com 7-Dec-2011



*All dimensions are nominal

	Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
I	PCM1795DBR	SSOP	DB	28	2000	346.0	346.0	33.0	

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-150

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products Applications

Audio www.ti.com/audio Communications and Telecom www.ti.com/communications **Amplifiers** amplifier.ti.com Computers and Peripherals www.ti.com/computers dataconverter.ti.com Consumer Electronics www.ti.com/consumer-apps **Data Converters DLP® Products** www.dlp.com **Energy and Lighting** www.ti.com/energy DSP dsp.ti.com Industrial www.ti.com/industrial Clocks and Timers www.ti.com/clocks Medical www.ti.com/medical

Interface interface.ti.com Security www.ti.com/security

Logic Space, Avionics and Defense www.ti.com/space-avionics-defense

Power Mgmt power.ti.com Transportation and Automotive www.ti.com/automotive
Microcontrollers Microcontroller.ti.com Video and Imaging www.ti.com/video

RFID <u>www.ti-rfid.com</u>

OMAP Mobile Processors www.ti.com/omap

Wireless Connectivity www.ti.com/wirelessconnectivity

TI E2E Community Home Page <u>e2e.ti.com</u>