

24-Bit, 192-kHz Sampling, Enhanced Multi-Level ΔΣ, Stereo, Audio Digital-to-Analog Converter

FEATURES

- Enhanced Multi-Level Delta-Sigma DAC:
 - High Performance: Differential, f_s = 48 kHz
 - THD+N: -94 dB
 - SNR: 113 dB
 - Dynamic Range: 113 dB
 - Sampling Rate: 8 kHz to 192 kHz
 - System Clock: 128 $f_{S},$ 192 $f_{S},$ 256 $f_{S},$ 384 $f_{S},$ 512 $f_{S},$ 768 $f_{S},$ 1152 f_{S}
 - Differential Voltage Output: 8 V_{PP}
 - Analog Low-Pass Filter Included
 - 4x/8x Oversampling Digital Filter:
 - Passband Ripple: ±0.0018 dB
 - Stop Band Attenuation: -75 dB
 - Zero Flags (16-/20-/24-Bits)
- Flexible Audio Interface:
 - I/F Format: I²S[™], Left-/Right-Justified, DSP
 - Data Length: 16, 20, 24, 32 Bits
- Flexible Mode Control:
 - 3-Wire SPI[™], 2-Wire I²C[™]-Compatible Serial Control Interface, or Hardware Control
 - Connect Up To 4 Devices on One SPI Bus
- Multi Functions via SPI or I²C I/F:
 - Audio I/F Format Select: I²S, Left-Justified, Right-Justified, DSP
 - Digital Attenuation and Soft Mute
 - Digital De-Emphasis: 32 kHz, 44.1 kHz, 48 kHz
 - Data Polarity Control
 - Power-Save Mode
- Multi Functions via Hardware Control:
 - Audio I/F Format Select: I²S, Left-Justified
 - Digital De-Emphasis Filter: 44.1 kHz
- Analog Mute by Clock Halt Detection

- External Reset Pin
- Power Supplies:
 - 5 V for Analog and 3.3 V for Digital
- Package: TSSOP-24
- Operating Temperature Range:
 - –40°C to +85°C

APPLICATIONS

- Blu-ray Disc[™] Players
- DVD Players
- AV Receivers
- Home Theaters
- Car Audio External Amplifiers
- Car Audio AVN Applications

DESCRIPTION

The PCM1789 is a high-performance, single-chip, 24-bit, stereo, audio digital-to-analog converter (DAC) with differential outputs. The two-channel, 24-bit DAC employs an enhanced multi-level, delta-sigma ($\Delta\Sigma$) modulator, and supports 8 kHz to 192 kHz sampling rates and a 16-/20-/24-/32-bit width digital audio input word on the audio interface. The audio interface of PCM1789 supports a 24-bit, DSP format in addition to I²S, left-justified, and right-justified formats.

The PCM1789 can be controlled through a three-wire, SPI-compatible or two-wire, I²C-compatible serial interface in software, which provides access to all functions including digital attenuation, soft mute, de-emphasis, and so forth. Also, hardware control mode provides two user-programmable functions through two control pins. The PCM1789 is available in a 24-pin TSSOP package.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PRODUCT	PACKAGE- LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
PCM1789	TSSOP-24	PW	–40°C to +85°C	PCM1789	PCM1789PW	Tube, 60
FCIVIT709	1330F-24	FVV	-40 C 10 +65 C		PCM1789PWR	Tape and Reel, 2000

ORDERING INFORMATION⁽¹⁾

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Over operating free-air temperature range (unless otherwise noted).

	PARAMETER	PCM1789	UNIT
Supply voltage	VCC1, VCC2	-0.3 to +6.5	V
Supply voltage	VDD	-0.3 to +4.0	V
Ground voltage difference	es: AGND1, AGND2, DGND	±0.1	V
Supply voltage differences	s: VCC1, VCC2	±0.1	V
Digital input voltage	RST, ADR5, MS, MC, MD, SCKI, AMUTEI	-0.3 to +6.5	V
Digital liput voltage	BCK, LRCK, DIN, MODE, ZERO1, ZERO2	-0.3 to (VDD + 0.3) < +4.0	V
Analog input voltage: VCC	DM, VOUTL±, VOUTR±	-0.3 to (VCC + 0.3) < +6.5	V
Input current (all pins exce	ept supplies)	±10	mA
Ambient temperature und	er bias	-40 to +125	°C
Storage temperature		-55 to +150	°C
Junction temperature		+150	°C
Lead temperature (solderi	ing, 5s)	+260	°C
Package temperature (IR	reflow, peak)	+260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range (unless otherwise noted).

			PCM1789		
Р	MIN	TYP	MAX	UNIT	
Analog supply voltage, VCC	4.5	5.0	5.5	V	
Digital supply voltage, VDD		3.0	3.3	3.6	V
Digital Interface		L	/TTL-compat	ble	
Digital input clock frequency	Sampling frequency, LRCK	8		192	kHz
Digital input clock frequency	System clock frequency, SCKI	2.048		36.864	MHz
Analog output voltage	Differential		8		V _{PP}
	To ac-coupled GND	5			kΩ
Analog output load resistance	To dc-coupled GND	15			kΩ
Analog output load capacitance				50	pF
Digital output load capacitance				20	pF
Operating free-air temperature	PCM1789 consumer grade	-40	+25	+85	°C



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ELECTRICAL CHARACTERISTICS: Digital Input/Output

All specifications at $T_A = +25^{\circ}$ C, VCC1 = VCC2 = 5 V, VDD = 3.3 V, $f_S = 48$ kHz, SCKI = 512 f_S , 24-bit data, and Sampling mode = Auto, unless otherwise noted.

				PCM1789		
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DATA FORMAT	L		-	4		
Audio data interface format			l ²	² S, LJ, RJ, D	SP	
Audio data word length				16, 20, 24, 3	2	Bits
Audio data format			MSB fi	rst, twos com	plement	
Sampling frequency	f _S		8	48	192	kHz
System clock frequency		128 f _S , 192 f _S , 256 f _S , 384 f _S , 512 f _S , 768 f _S , 1152 f _S	2.048		36.864	MHz
INPUT LOGIC						
	V _{IH} ⁽¹⁾⁽²⁾		2.0		VDD	VDC
Input logic level	V _{IL} ⁽¹⁾⁽²⁾				0.8	VDC
	V _{IH} ⁽³⁾⁽⁴⁾		2.0		5.5	VDC
Input logic level	V _{IL} ⁽³⁾⁽⁴⁾				0.8	VDC
	I _{IH} ⁽²⁾⁽³⁾	V _{IN} = VDD			±10	μA
Input logic current	I _{IL} ⁽²⁾⁽³⁾	$V_{IN} = 0 V$			±10	μA
lanut la sia auroat	I _{IH} ⁽¹⁾⁽⁴⁾	V _{IN} = VDD		+65	+100	μA
Input logic current	I _{IL} ⁽¹⁾⁽⁴⁾	$V_{IN} = 0 V$			±10	μA
OUTPUT LOGIC						
Output logic lovel	V _{OH} ⁽⁵⁾	$I_{OUT} = -4 \text{ mA}$	2.4			VDC
Output logic level	V _{OL} ⁽⁵⁾⁽⁶⁾	I _{OUT} = +4 mA			0.4	VDC
REFERENCE OUTPUT	· · ·					
VCOM output voltage				0.5 × VCC1		V
VCOM output impedance				7.5		kΩ
Allowable VCOM output source/s	ink current				1	μA

BCK and LRCK (Schmitt trigger input with 50-kΩ typical internal pull-down resistor). (1)

(2)

DIN (Schmitt trigger input). SCKI, ADR5/ADR1/RSV, MC/SCL/FMT, MD/SDA/DEMP, and AMUTEI (Schmitt trigger input, 5-V tolerant). (3)

RST and MS/ADR0/RSV (Schmitt trigger input with 50-kΩ typical internal pull-down resistor, 5-V tolerant). (4)

(5) ZERO1 and ZERO2.

AMUTEO and SDA (I²C mode, open-drain low output). (6)



ELECTRICAL CHARACTERISTICS: DAC

All specifications at $T_A = +25$ °C, VCC1 = VCC2 = 5 V, VDD = 3.3 V, $f_S = 48$ kHz, SCKI = 512 f_S , 24-bit data, and Sampling mode = Auto, unless otherwise noted.

					PCM1789		
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
RESOLUTION				16	24		Bits
DC ACCURACY							
Gain mismatch channel-to-channe	el l				±2.0	±6.0	% of FSR
Gain error					±2.0	±6.0	% of FSR
Bipolar zero error					±1.0		% of FSR
DYNAMIC PERFORMANCE ⁽¹⁾⁽²⁾							
			f _S = 48 kHz		-94	-88	dB
Total harmonic distortion + noise	THD+N	$V_{OUT} = 0 \text{ dB}$	f _S = 96 kHz		-94		dB
			f _S = 192 kHz		-94		dB
		f _S = 48 kHz, E	AJ, A-weighted	106	113		dB
Dynamic range		f _S = 96 kHz, E	IAJ, A-weighted		113		dB
		f _S = 192 kHz, EIAJ, A-weighted			113		dB
		f _S = 48 kHz, E	IAJ, A-weighted	106	113		dB
Signal-to-noise ratio	SNR	$f_{S} = 96 \text{ kHz}, \text{ EIAJ}, \text{ A-weighted}$			113		dB
		f _S = 192 kHz, E	IAJ, A-weighted		113		dB
· · ·		f _S = 48 kHz		103	109		dB
Channel separation		f _S = 96 kHz			109		dB
		f _S = 192 kHz			108		dB
ANALOG OUTPUT							
Output voltage		Differential			1.6 × VCC1		V _{PP}
Center voltage					0.5 × VCC1		V
Landimpedance		To ac-coup	oled GND ⁽³⁾	5			kΩ
Load impedance		To dc-coup	oled GND ⁽³⁾	15			kΩ
		f = 2	0 kHz		-0.04		dB
LPF frequency response		f = 4	4 kHz		-0.18		dB
DIGITAL FILTER PERFORMANC	E WITH SH	ARP ROLL-OFF					
Passband (single_dual)		Except SCKI = 7	128 f _S and 192 f _S			0.454 × f _S	Hz
Passband (single, dual)		SCKI = 128	f _S and 192 f _S			0.432 × f _S	Hz
Passband (quad)						0.432 × f _S	Hz
Stop bond (single dual)		Except SCKI = 7	128 f _S and 192 f _S	0.546 × f _S			Hz
Stop band (single, dual)		SCKI = 128	f _S and 192 f _S	0.569 × f _S			Hz
Stop band (quad)				0.569 × f _S			Hz
Passband ripple		< 0.454 × f _S , 0.432 × f _S				±0.0018	dB
Stop band attenuation		> 0.546 × f _S , 0.569 × f _S		-75			dB

(1)

(2) (3)

In differential mode at VOUTx± pin, $f_{OUT} = 1$ kHz, using Audio Precision System II, Average mode with 20-kHz LPF and 400-Hz HPF. $f_S = 48$ kHz: SCKI = 512 f_S (single), $f_S = 96$ kHz : SCKI = 256 f_S (dual), $f_S = 192$ kHz : SCKI = 128 f_S (quad). Allowable minimum input resistance of differential-to-single-ended converter with D-to-S gain = G is calculated as $(1 + 2G)/(1 + G) \times 5k$ for ac-coupled, and $(1+0.9G)/(1 + G) \times 15k$ for dc-coupled connection; refer to Figure 38 and Figure 39.



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ELECTRICAL CHARACTERISTICS: DAC (continued)

All specifications at $T_A = +25^{\circ}$ C, VCC1 = VCC2 = 5 V, VDD = 3.3 V, $f_S = 48$ kHz, SCKI = 512 f_S , 24-bit data, and Sampling mode = Auto, unless otherwise noted.

			PCM1789			
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
DIGITAL FILTER PERFORMANCE WIT	TH SLOW ROLL-OFF					
Passband				0.328 × f _S	Hz	
Stop band		0.673 × f _S			Hz	
Passband ripple	< 0.328 × f _S			±0.0013	dB	
Stop band attenuation	> 0.673 × f _S	-75			dB	
DIGITAL FILTER PERFORMANCE						
	Except SCKI = 128 f _S and 192 f _S		28/f _S		sec	
Group delay time (single, dual)	SCKI = 128 f_S and 192 f_S		19/f _S		sec	
Group delay time (quad)			19/f _S		sec	
De-emphasis error			±0.1		dB	

ELECTRICAL CHARACTERISTICS: Power-Supply Requirements

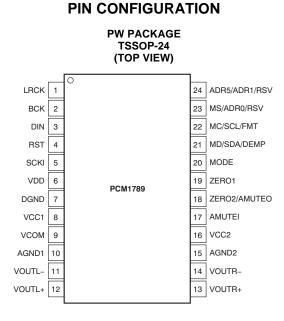
All specifications at $T_A = +25^{\circ}$ C, VCC1 = VCC2 = 5 V, VDD = 3.3 V, $f_S = 48$ kHz, SCKI = 512 f_S , 24-bit data, and Sampling mode = Auto, unless otherwise noted.

			PCM1789				
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
POWER-SUPPLY REQUIREMEN	тѕ						
	VCC1/2		4.5	5.0	5.5	VDC	
Voltage range	VDD		3.0	3.3	3.6	VDC	
		f _S = 48 kHz		19	28	mA	
	I _{CC}	f _S = 192 kHz		19		mA	
0		Full power-down ⁽¹⁾		170		μΑ	
Supply current		f _S = 48 kHz		18	30	mA	
	I _{DD}	f _S = 192 kHz		22		mA	
		Full power-down ⁽¹⁾		60		μΑ	
	I	f _S = 48 kHz		154	239	mW	
Power dissipation		f _S = 192 kHz		168		mW	
		Full power-down ⁽¹⁾		1.05		mW	
TEMPERATURE RANGE	L						
Operating temperature		PCM1789 consumer grade	-40		+85	°C	
Thermal resistance	θ_{JA}	TSSOP-24		115		°C/W	

(1) SCKI, BCK, and LRCK stopped.

TEXAS INSTRUMENTS

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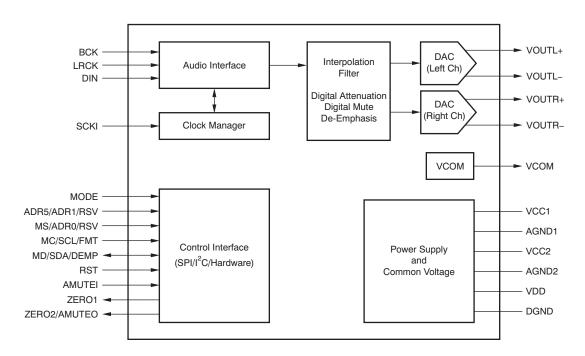
TERMINAL FUNCTIONS

TERMINAL			PULL-	5-V	
NAME	PIN	I/O	DOWN	TOLERANT	DESCRIPTION
LRCK	1	I	Yes	No	Audio data word clock input
BCK	2	I	Yes	No	Audio data bit clock input
DIN	3	I	No	No	Audio data input
RST	4	I	Yes	Yes	Reset and power-down control input with active low
SCKI	5	I	No	Yes	System clock input
VDD	6	—	_	—	Digital power supply, +3.3 V
DGND	7	_	—	_	Digital ground
VCC1	8	—	—	_	Analog power supply 1, +5 V
VCOM	9	—	—	_	Voltage common decoupling
AGND1	10	_	_	—	Analog ground 1
VOUTL-	11	0	No	No	Negative analog output from DAC left channel
VOUTL+	12	0	No	No	Positive analog output from DAC left channel
VOUTR+	13	0	No	No	Positive analog output from DAC right channel
VOUTR-	14	0	No	No	Negative analog output from DAC right channel
AGND2	15	_	_	—	Analog ground 2
VCC2	16	_	_	—	Analog power supply 2, +5 V
AMUTEI	17	I	No	Yes	Analog mute control input with active low
ZERO2/AMUTEO	18	0	No	No	Zero detect flag output 2/Analog mute control output ⁽¹⁾ with active low
ZERO1	19	0	No	No	Zero detect flag output 1
MODE	20	I	No	No	Control port mode selection. Tied to VDD: SPI, ADR6 = 1, pull-up: SPI, ADR6 = 0, pull-down: H/W auto mode, tied to DGND: I^2C
MD/SDA/DEMP	21	I/O	No	Yes	Input data for SPI, data for $I^2C^{(1)}$, de-emphasis control for hardware control mode
MC/SCL/FMT	22	I	No	Yes	Clock for SPI, clock for I ² C, format select for hardware control mode
MS/ADR0/RSV	23	I	Yes	Yes	Chip Select for SPI, address select 0 for I ² C, reserve (set low) for hardware control mode
ADR5/ADR1/RSV	24	I	No	Yes	Address select 5 for SPI, address select 1 for $I^2C,$ reserve (set low) for hardware control mode

(1) Open-drain configuration in out mode.

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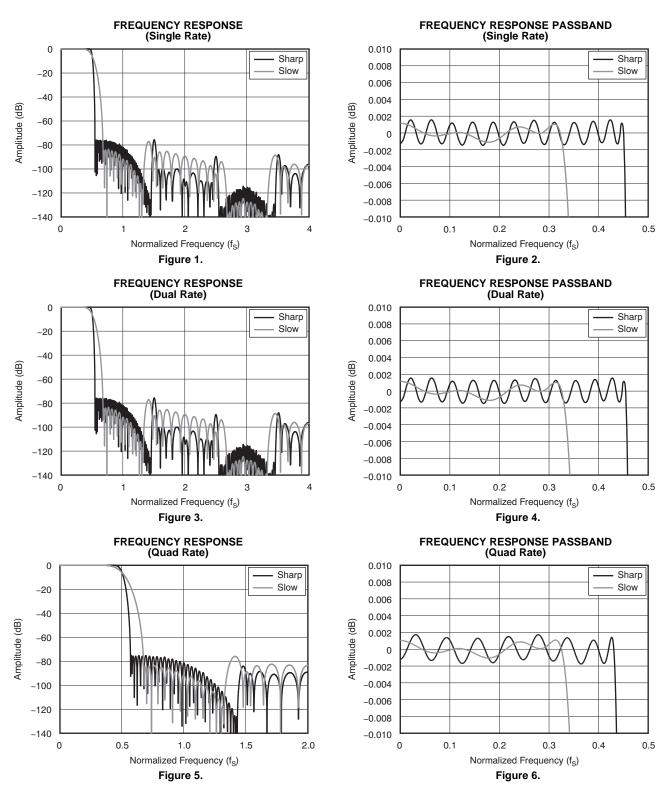


FUNCTIONAL BLOCK DIAGRAM





All specifications at $T_A = +25^{\circ}$ C, VCC1 = VCC2 = 5 V, VDD = 3.3 V, $f_S = 48$ kHz, SCKI = 512 f_S , 24-bit data, and Sampling mode = Auto, unless otherwise noted.





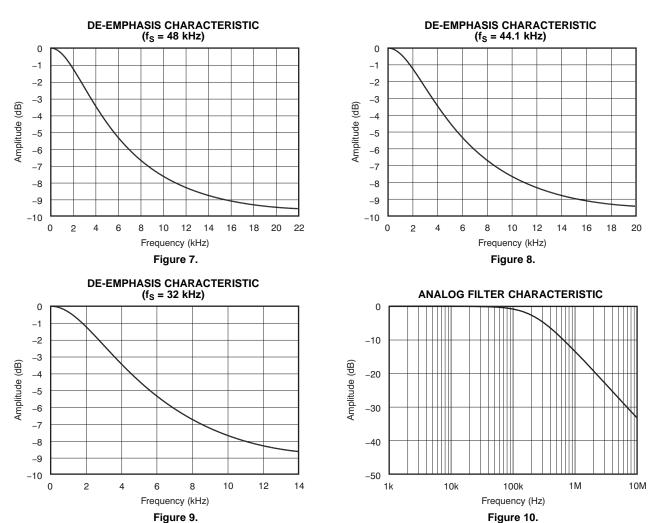
TEXAS INSTRUMENTS

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TYPICAL CHARACTERISTICS: Digital De-Emphasis Filter

All specifications at $T_A = +25^{\circ}$ C, VCC1 = VCC2 = 5 V, VDD = 3.3 V, $f_S = 48$ kHz, SCKI = 512 f_S , 24-bit data, and Sampling mode = Auto, unless otherwise noted.

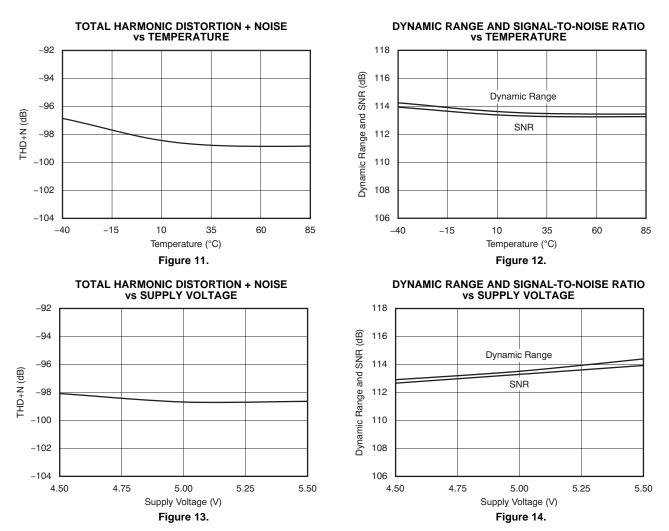


INSTRUMENTS

EXAS

TYPICAL CHARACTERISTICS: Dynamic Performance

All specifications at $T_A = +25^{\circ}$ C, VCC1 = VCC2 = 5 V, VDD = 3.3 V, $f_S = 48$ kHz, SCKI = 512 f_S , 24-bit data, and Sampling mode = Auto, unless otherwise noted.



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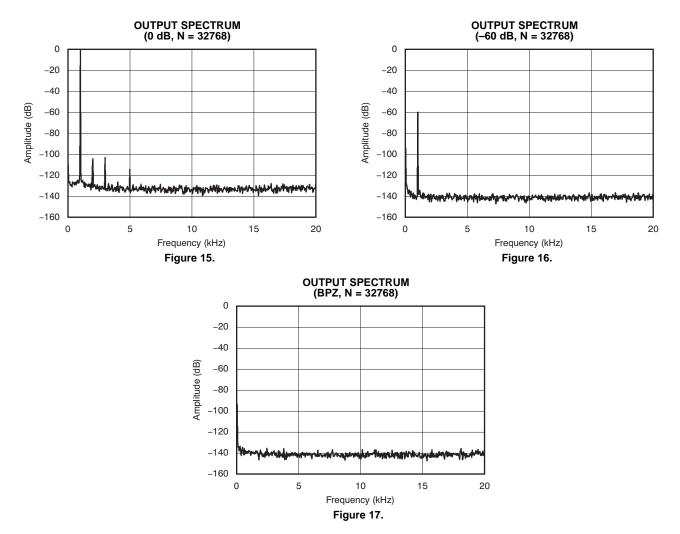




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TYPICAL CHARACTERISTICS: Output Spectrum

All specifications at $T_A = +25^{\circ}$ C, VCC1 = VCC2 = 5 V, VDD = 3.3 V, $f_S = 48$ kHz, SCKI = 512 f_S , 24-bit data, and Sampling mode = Auto, unless otherwise noted.





PRODUCT OVERVIEW

The PCM1789 is a high-performance stereo DAC targeted for consumer audio applications such as Blu-ray Disc players and DVD players, as well as home multi-channel audio applications (such as home theater and A/V receivers). The PCM1789 consists of a two-channel DAC. The DAC output type is fixed with a differential configuration. The PCM1789 supports 16-/20-/24-/32-bit linear PCM input data in I²S and left-justified audio formats, and 24-bit linear PCM input data in right-justified and DSP formats with various sampling frequencies from 8 kHz to 192 kHz. The PCM1789 offers three modes for device control: two-wire I²C software, three-wire SPI software, and hardware.

ANALOG OUTPUTS

The PCM1789 includes a two-channel DAC, with a pair of differential voltage outputs pins. The full-scale output voltage is (1.6 × VCC1) V_{PP} in differential output mode. A dc-coupled load is allowed in addition to an ac-coupled load, if the load resistance conforms to the specification. These balanced outputs are each capable of driving 0.8 VCC1 (4 V_{PP}) typical into a 5-k Ω ac-coupled or 15-k Ω dc-coupled load with VCC1 = +5 V. The internal output amplifiers for VOUTL and VOUTR are biased to the dc common voltage, equal to 0.5 VCC1.

The output amplifiers include an RC continuous-time filter that helps to reduce the out-of-band noise energy present at the DAC outputs as a result of the noise shaping characteristics of the PCM1789 delta-sigma ($\Delta\Sigma$) DACs. The frequency response of this filter is shown in the *Analog Filter Characteristic* (Figure 10) of the Typical Characteristics. By itself, this filter is not enough to attenuate the out-of-band noise to an acceptable level for most applications. An external low-pass filter is required to provide sufficient out-of-band noise rejection. Further discussion of DAC post-filter circuits is provided in the *Application Information* section.

VOLTAGE REFERENCE VCOM

The PCM1789 includes a pin for the common-mode voltage output, VCOM. This pin should be connected to the analog ground via a decoupling capacitor. This pin can also be used to bias external high-impedance circuits, if they are required.



SYSTEM CLOCK INPUT

The PCM1789 requires an external system clock input applied at the SCKI input for DAC operation. The system clock operates at an integer multiple of the sampling frequency, or f_S . The multiples supported in DAC operation include 128 f_S , 192 f_S , 256 f_S , 384 f_S , 512 f_S , 768 f_S , and 1152 f_S . Details for these system clock multiples are shown in Table 1. Figure 18 and Table 2 show the SCKI timing requirements.

DEFAULT	SAMPLING	SYSTEM CLOCK FREQUENCY (MHz)							
SAMPLING MODE	FREQUENCY, f _S (kHz)	128 f _S	192 f _S	256 f _S	384 f _S	512 f _S	768 f _S	1152 f _S	
	8	N/A	N/A	2.0480	3.0720	4.0960	6.1440	9.2160	
	16	2.0480	3.0720	4.0960	6.1440	8.1920	12.2880	18.4320	
Single rate	32	4.0960	6.1440	8.1920	12.2880	16.3840	24.5760	36.8640	
	44.1	5.6448	8.4672	11.2896	16.9344	22.5792	33.8688	N/A	
	48	6.1440	9.2160	12.2880	18.4320	24.5760	36.8640	N/A	
Dual rate	88.2	11.2896	16.9344	22.5792	33.8688	N/A	N/A	N/A	
Duarrale	96	12.2880	18.4320	24.5760	36.8640	N/A	N/A	N/A	
Quad rate	176.4	22.5792	33.8688	N/A	N/A	N/A	N/A	N/A	
Quad Tale	192	24.5760	36.8640	N/A	N/A	N/A	N/A	N/A	

 Table 1. System Clock Frequencies for Common Audio Sampling Rates

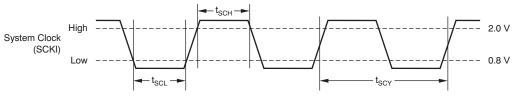


Figure 18. System Clock Timing Diagram

Table 2.	Timing	Requirements	for Figure 18	
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SYMBOL	PARAMETER	MIN	MAX	UNIT
t _{SCY}	System clock cycle time	27		ns
t _{SCH}	System clock width high	10		ns
t _{SCL}	System clock width low	10		ns
_	System clock duty cycle	40	60	%



SAMPLING MODE

The PCM1789 supports three sampling modes (single rate, dual rate, and quad rate) in DAC operation. In single rate mode, the DAC operates at an oversampling frequency of x128 (except when SCKI = 128 f_s and 192 f_s); this mode is supported for sampling frequencies less than 50 kHz. In dual rate mode, the DAC operates at an oversampling frequencies less than 50 kHz. In dual rate mode, the DAC operates at an oversampling frequency of x32. The sampling mode is automatically selected according to the ratio of system clock frequency and sampling frequency by default (that is, single rate for 512 f_s , 768 f_s , and 1152 f_s ; dual rate for 256 f_s and 384 f_s ; and quad rate for 128 f_s and 192 f_s), but manual selection is also possible for specified combinations through the serial mode control register.

Table 3 and Figure 19 show the relationship among the oversampling rate (OSR) of the digital filter and $\Delta\Sigma$ modulator, the noise-free shaped bandwidth, and each sampling mode setting.

SAMPLING MODE	SYSTEM CLOCK	NOISE-FI	REE SHAPED BAN (kHz)	DWIDTH ⁽¹⁾			
REGISTER SETTING	FREQUENCY (xf _S)	f _S = 48 kHz	f _S = 96 kHz	f _S = 192 kHz	DIGITAL FILTER OSR	MODULATOR OSR	
	512, 768, 1152	40	N/A	N/A	×8	x128	
Auto	256, 384	20	40	N/A	x8	x64	
	128, 192 ⁽²⁾	10	20	40	x4	x32	
	512, 768, 1152	40	N/A	N/A	x8	x128	
Single	256, 384	40	N/A	N/A	x8	x128	
	128, 192 ⁽²⁾	20	N/A	N/A	x4	x64	
Dual	256, 384	20	40	N/A	x8	x64	
Dual	128, 192 ⁽²⁾	20	40	N/A	x4	x64	
Quad	128, 192 ⁽²⁾	10	20	40	x4	x32	

Table 3. Digital Filter OSR, Modulator OSR, and Noise-Free Shaped Bandwidth for Each Sampling Mode

(1) Bandwidth in which noise is shaped out.

(2) Quad mode filter characteristic is applied.

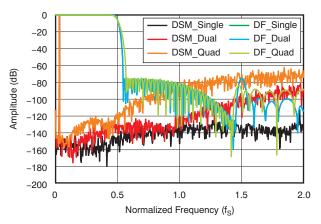


Figure 19. ΔΣ Modulator and Digital Filter Characteristic



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RESET OPERATION

The PCM1789 has both an internal power-on reset circuit and an external reset circuit. The sequences for both reset circuits are shown in Figure 20 and Figure 21. Figure 20 illustrates the timing at the internal power-on reset. Initialization is triggered automatically at the point where VDD exceeds 2.2 V typical, and the internal reset is released after 3846 SCKI clock cycles from power-on, if RST is held high and SCKI is provided. VOUTx from the DAC is forced to the VCOM level initially (that is, 0.5 × VCC1) and settles at a specified level according to the rising VCC. If synchronization among SCKI, BCK, and LRCK is maintained, VOUT provides an output that corresponds to DIN after 3846 SCKI clocks from power-on. If the synchronization is not held, the internal reset is not released, and both operating modes are maintained at reset and power-down states. After synchronization forms again, the DAC returns to normal operation with the previous sequences.

Figure 21 illustrates a timing diagram at the external reset. RST accepts an externally-forced reset with RST low, and provides a device reset and power-down state that achieves the lowest power dissipation state available in the PCM1789. If RST goes from high to low under synchronization among SCKI, BCK, and LRCK, the internal reset is asserted, all registers and memory are reset, and finally, the PCM1789 enters into all power-down states. At the same time, VOUT is immediately forced into the AGND1 level. To begin normal operation again, toggle RST high; the same power-up sequence is performed as the power-on reset shown in Figure 20.

The PCM1789 does not require particular power-on sequences for VCC and VDD; it allows VDD on and then VCC on, or VCC on and then VDD on. From the viewpoint of the Absolute Maximum Ratings, however, simultaneous power-on is recommended for avoiding unexpected responses on VOUTx. Figure 20 illustrates the response for VCC on with VDD on.

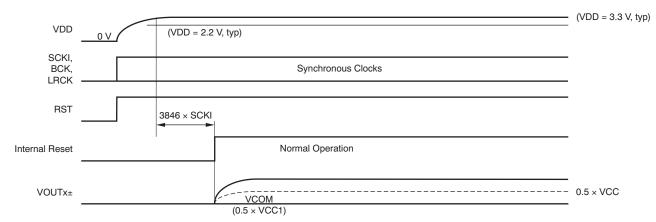
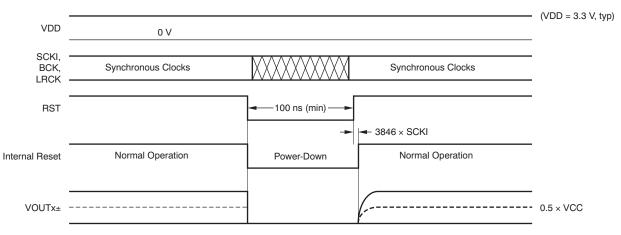


Figure 20. Power-On-Reset Timing Requirements







AUDIO SERIAL PORT OPERATION

The PCM1789 audio serial port consists of three signals: BCK, LRCK, and DIN. BCK is a bit clock input. LRCK is a left/right word clock or frame synchronization clock input. DIN is the audio data input for VOUTL/R.

AUDIO DATA INTERFACE FORMATS AND TIMING

The PCM1789 supports six audio data interface formats: 16-/20-/24-/32-bit l²S, 16-/20-/24-/32-bit left-justified, 24-bit right-justified, 16-bit right-justified, 24-bit left-justified mode DSP, and 24-bit l²S mode DSP. In the case of l²S, left-justified, and right-justified data formats, 64 BCKs, 48 BCKs, and 32 BCKs per LRCK period are supported; however, 48 BCKs are limited to 192/384/768 f_S SCKI, and 32 BCKs are limited to 16-bit right-justified only. The audio data formats are selected by MC/SCL/FMT in hardware control mode and by the FMTDA[2:0] bits in control register 17 (11h) in software control mode. All data must be in binary twos complement and MSB first.

Table 4 summarizes the applicable formats and describes the relationships among them and the respective restrictions with mode control. Figure 22 through Figure 26 show six audio interface data formats.

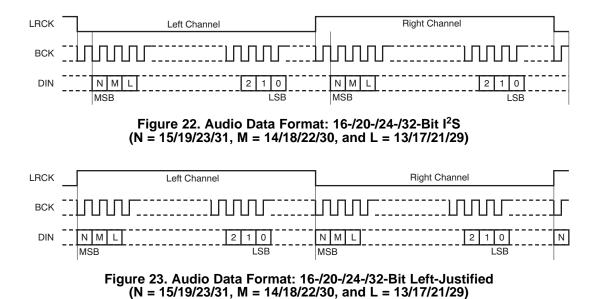
Table 4. Audio Data Interface	Formats and Sampline	a Rate. Bit Clock. and S	vstem Clock Restrictions
Tuble II / luule Bulu III el lue			

CONTROL MODE	FORMAT	DATA BITS	MAX LRCK FREQUENCY (f _s)	SCKI RATE (xf _s)	BCK RATE (xf _s)
	I ² S/Left-Justified	16/20/24/32 ⁽¹⁾	192 kHz	128 to 1152 ⁽²⁾	64, 48
Software control	Right-Justified	24, 16	192 kHz	128 to 1152 ⁽²⁾	64, 48, 32 (16 bit) ⁽³⁾
	I ² S/Left-Justified DSP	24	192 kHz	128 to 768	64
Hardware control	I ² S/Left-Justified	16/20/24/32 ⁽¹⁾	192 kHz	128 to 1152 ⁽²⁾	64, 48

(1) 32-bit data length is acceptable only for BCK = 64 f_S and when using I^2S or Left-Justified format.

(2) 1152 f_s is acceptable only for $f_s = 32$ kHz, BCK = 64 f_s , and when using I^2S , Left-Justified, or 24-bit Right-Justified format.

(3) BCK = 32 f_S is supported only for 16-bit data length.





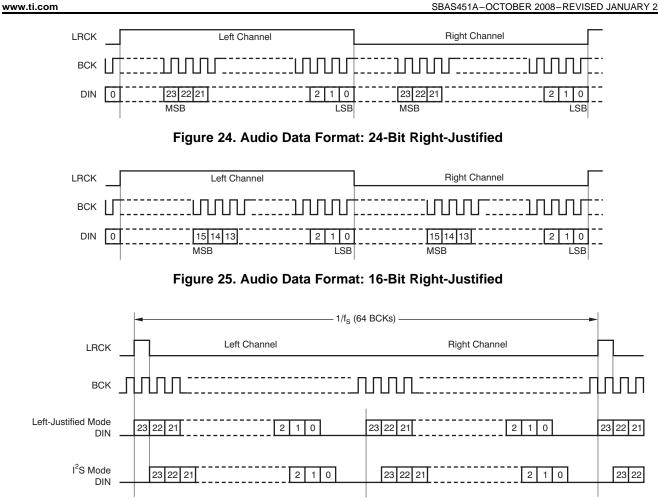


Figure 26. Audio Data Format: 24-Bit DSP Format

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AUDIO INTERFACE TIMING

Figure 27 and Table 5 describe the detailed audio interface timing specifications.

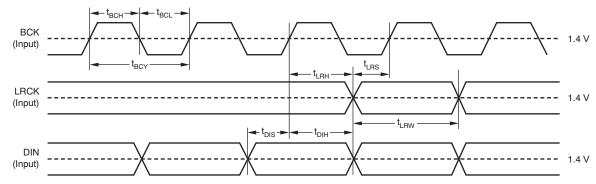


Figure 27. Audio Interface Timing Diagram for Left-Justified, Right-Justified, I²S, and DSP Data Formats

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t _{BCY}	BCK cycle time	75			ns
t _{BCH}	BCK pulse width high	35			ns
t _{BCL}	BCK pulse width low	35			ns
	LRCK pulse width high (LJ, RJ and I ² S formats)	$1/(2 \times f_{S})$		$1/(2 \times f_{S})$	sec
t _{LRW}	LRCK pulse width high (DSP format)	t _{BCY}		t _{BCY}	sec
t _{LRS}	LRCK setup time to BCK rising edge	10			ns
t _{LRH}	LRCK hold time to BCK rising edge	10			ns
t _{DIS}	DIN setup time to BCK rising edge	10			ns
t _{DIH}	DIN hold time to BCK rising edge	10			ns



SYNCHRONIZATION WITH THE DIGITAL AUDIO SYSTEM

The PCM1789 operates under the system clock (SCKI) and the audio sampling rate (LRCK). Therefore, SCKI and LRCK must have a specific relationship. The PCM1789 does not need a specific phase relationship between the audio interface clocks (LRCK, BCK) and the system clock (SCKI), but does require a specific frequency relationship (ratiometric) between LRCK, BCK, and SCKI.

If the relationship between SCKI and LRCK changes more than ± 2 BCK clocks because of jitter, sampling frequency change, etc., the DAC internal operation stops within 1/f_S, and the analog output is forced into VCOM (0.5 VCC1) until re-synchronization among SCKI, LRCK, and BCK completes, and then either 38/f_S (single, dual rate) or 29/f_S (quad rate) passes. In the event the change is less than ± 2 BCKs, re-synchronization does not occur, and this analog output control and discontinuity does not occur.

Figure 28 shows the DAC analog output during loss of synchronization. During undefined data periods, some noise may be generated in the audio signal. Also, the transition of normal to undefined data and undefined (or zero) data to normal data creates a discontinuity of data on the analog outputs, which may then generate some noise in the audio signal.

The DAC outputs (VOUTx) hold the previous state if the system clock halts, but the asynchronous and re-synchronization processes will occur after the system clock resumes.

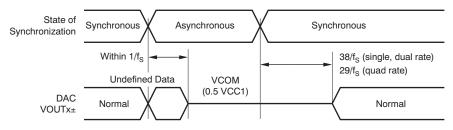


Figure 28. DAC Outputs During Loss of Synchronization

ZERO FLAG

The PCM1789 has two ZERO flag pins (ZERO1 and ZERO2) that can be assigned to the combinations shown in Table 6. Zero flag combinations are selected through the AZRO bit in control register 22 (16h). If the input data of all the assigned channels remain at '0' for 1024 sampling periods (LRCK clock periods), the ZERO1/2 bits are set to a high level, logic '1' state. Furthermore, if the input data of any of the assigned channels read '1', the ZERO1/2 are set to a low level, logic '0' state, immediately. Zero data detection is supported for 16-/20-/24-bit data width, but is not supported for 32-bit data width.

The active polarity of the zero flag output can be inverted through the ZREV bit in control register 22 (16h). The reset default is active high for zero detection.

In parallel hardware control mode, ZERO1 and ZERO2 are fixed with combination A, shown in Table 6.

ZERO FLAG COMBINATION	ZERO1	ZERO2
A	Left channel	Right channel
В	Left channel or right channel	Left channel and right channel

Table 6. Zero Flag Outputs Combination

Note that the ZERO2 pin is multiplexed with AMUTEO pin. Selection of ZERO2 or AMUTEO can be changed through the MZSEL bit in control register 22 (16h). The default setting after reset is the selection of ZERO2.



AMUTE CONTROL

The PCM1789 has an AMUTE control input, status output pins, and functionality. AMUTEI is the input control pin of the internal analog mute circuit. An AMUTEI low input causes the DAC output to cut-off from the digital input and forces it to the center level (0.5 VCC1). AMUTEO is the status output pin of the internal analog mute circuit. AMUTEO low indicates the analog mute control circuit is active because of a programmed condition (such as an SCKI halt, asynchronous detect, zero detect, or by the DAC disable command) that forces the DAC outputs to a center level. Because AMUTEI is not terminated internally and AMUTEO is an open-drain output, pull-ups by the appropriate resistors are required for proper operation.

Note that the AMUTEO pin is multiplexed with the ZERO2 pin. The desired pin is selected through the MZSEL bit in control register 22 (16h). The default setting is the selection of the ZERO2 pin.

Additionally, because the AMUTEI pin control and power-down control in register (OPEDA when high, PSMDA when low) do not function together, AMUTEI takes priority over power-down control. Therefore, power-down control is ignored during AMUTEI low, and AMUTEI low forces the DAC output to a center level (0.5 VCC1) even if power-down control is asserted.

MODE CONTROL

The PCM1789 includes three mode control interfaces with three oversampling configurations, depending on the input state of the MODE pin, as shown in Table 7. The pull-up and pull-down resistors must be 220 k Ω ±5%.

MODE	MODE CONTROL INTERFACE
Tied to DGND	Two-wire (I ² C) serial control, selectable oversampling configuration
Pull-down resistor to DGND	Two-wire parallel control, auto mode oversampling configuration
Pull-up resistor to VDD	Three-wire (SPI) serial control, selectable oversampling configuration, ADR6 = '0'
Tied to VDD	Three-wire (SPI) serial control, selectable oversampling configuration, ADR6 = '1'

Table 7. Interface Mode Control Selection

The input state of the MODE pin is sampled at the moment of power-on, or during a low-to-high transition of the RST pin, with the system clock input. Therefore, input changes after reset are ignored until the next power-on or reset. From the mode control selection described in Table 7, the functions of four pins are changed, as shown in Table 8.

		PIN ASSIGNMENTS				
PIN	SPI	l ² C	H/W			
21	MD (input)	SDA (input/output)	DEMP (input)			
22	MC (input)	SCL (input)	FMT (input)			
23	MS (input)	ADR0 (input)	RSV (input, low)			
24	ADR5 (input)	ADR1 (input)	RSV (input, low)			

Table 8. Pin Functions for Interface Mode

In serial mode control, the actual mode control is performed by register writes (and reads) through the SPI- or I²C-compatible serial control port. In parallel mode control, two specific functions are controlled directly through the high/low control of two specific pins, as described in the following section.

PARALLEL HARDWARE CONTROL

The functions shown in Table 9 and Table 10 are controlled by two pins, DEMP and FMT, in parallel hardware control mode. The DEMP pin controls the 44.1-kHz digital de-emphasis function of both channels. The FMT pin controls the audio interface format for both channels.

Table 9. DEMP Functionality

DEMP	DESCRIPTION
Low	De-emphasis off
High	44.1 kHz de-emphasis on

Table 10. FMT Functionality

FMT	DESCRIPTION
Low	16-/20-/24-/32-bit I ² S format
High	16-/20-/24-/32-bit left-justified format

THREE-WIRE (SPI) SERIAL CONTROL

The PCM1789 includes an SPI-compatible serial port that operates asynchronously with the audio serial interface. The control interface consists of MD/SDA/DEMP, MC/SCL/FMT, and MS/ADR0/RSV. MD is the serial data input used to program the mode control registers. MC is the serial bit clock that shifts the data into the control port. MS is the select input used to enable the mode control port.

CONTROL DATA WORD FORMAT

All single write operations via the serial control port use 16-bit data words. Figure 29 shows the control data word format. The first bit (fixed at '0') is for write operation. After the first bit are seven other bits, labeled ADR[6:0], that set the register address for the write operation. ADR6 is determined by the status of the MODE pin. ADR5 is determined by the state of the ADR5/ADR1/RSV pin. A maximum of four PCM1789s can be connected on the same bus at any one time. Each PCM1789 responds when receiving its own register address. The eight least significant bits (LSBs), D[7:0] on MD, contain the data to be written to the register address specified by ADR[6:0].

_	MSB															LSB	
	0	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	D7	D6	D5	D4	D3	D2	D1	D0	
			•	·													
				Reg	ister Add	ress						Registe	er Data				

Figure 29. Control Data Word Format for MD

REGISTER WRITE OPERATION

Figure 30 shows the functional timing diagram for single write operations on the serial control port. MS is held at a high state until a register is to be written to. To start the register write cycle, MS is set to a low state. 16 clocks are then provided on MC, corresponding to the 16 bits of the control data word on MD. After the 16th clock cycle has been completed, MS is set high to latch the data into the indexed mode control register.

In addition to single write operations, the PCM1789 also supports multiple write operations, which can be performed by sending the N-bytes (where $N \le 9$) of the 8-bit register data that follow after the first 16-bit register address and register data, while keeping the MC clocks and MS at a low state. Ending a multiple write operation can be accomplished by setting MS to a high state.

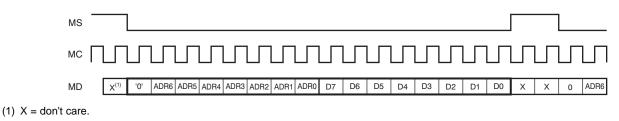


Figure 30. Register Write Operation

INSTRUMENTS

Texas

TIMING REQUIREMENTS

Figure 31 shows a detailed timing diagram for the three-wire serial control interface. These timing parameters are critical for proper control port operation.

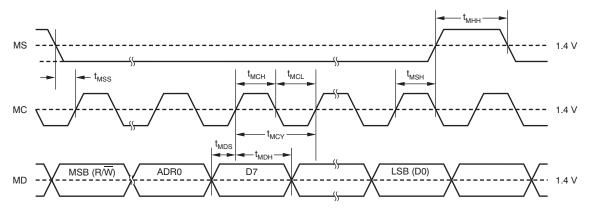


Figure 31. Three-Wire Serial Control Interface Timing

Table 11. Timing Requirements for Figure 3	Table 11.	Timing	Requirements	for	Figure 31	
--	-----------	--------	--------------	-----	-----------	--

SYMBOL	PARAMETER	MIN	MAX	UNIT
t _{MCY}	MC pulse cycle time	100		ns
t _{MCL}	MC low-level time	40		ns
t _{MCH}	MC high-level time	40		ns
t _{MHH}	MS high-level time	t _{MCY}		ns
t _{MSS}	MS falling edge to MC rising edge	30		ns
t _{MSH}	MS rising edge from MC rising edge for LSB	15		ns
t _{MDH}	MD hold time	15		ns
t _{MDS}	MD setup time	15		ns

TWO-WIRE (I²C) SERIAL CONTROL

The PCM1789 supports an I²C-compatible serial bus and data transmission protocol for fast mode configured as a slave device. This protocol is explained in the I²C specification 2.0.

The PCM1789 has a 7-bit slave address, as shown in Figure 32. The first five bits are the most significant bits (MSBs) of the slave address and are factory-preset to '10011'. The next two bits of the address byte are selectable bits that can be set by MS/ADR0/RSV and ADR5/ADR1/RSV. A maximum of four PCM1789s can be connected on the same bus at any one time. Each PCM1789 responds when it receives its own slave address.

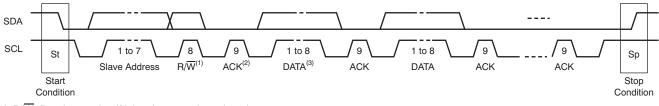
MSB							LSB	_
1	0	0	1	1	ADR1	ADR0	R/W	

Figure 32. Slave Address



PACKET PROTOCOL

A master device must control the packet protocol, which consists of a start condition, a slave address with the read/write bit, data if a write operation is required, an acknowledgment if a read operation is required, and a stop condition. The PCM1789 supports both slave receiver and transmitter functions. Details about DATA for both write and read operations are described in Figure 33.



(1) R/\overline{W} : Read operation if '1'; write operation otherwise.

(2) ACK: Acknowledgment of a byte if '0', not Acknowledgment of a byte if '1'.

(3) DATA: Eight bits (byte); details are described in the *Write Operation* and *Read Operation* sections.

Figure 33. I²C Packet Control Protocol

WRITE OPERATION

The PCM1789 supports a receiver function. A master device can write to any PCM1789 register using single or multiple accesses. The master sends a PCM1789 slave address with a write bit, a register address, and the data. If multiple access is required, the address is that of the starting register, followed by the data to be transferred. When valid data are received, the index register automatically increments by one. When the register address reaches &h4F, the next value is &h40. When undefined registers are accessed, the PCM1789 does not send an acknowledgment. Figure 34 illustrates a diagram of the write operation. The register address and write data are in 8-bit, MSB-first format.

Transmitter	М	М	М	S	М	S	М	S	М	S	 S	М
Data Type	St	Slave Address	W	ACK	Reg Address	ACK	Write Data 1	ACK	Write Data 2	ACK	 ACK	Sp

NOTE: M = Master device, S = Slave device, St = Start condition, \overline{W} = Write, ACK = Acknowledge, and Sp = Stop condition.

Figure 34. Framework for Write Operation

READ OPERATION

A master device can read the registers of the PCM1789. The value of the register address is stored in an indirect index register in advance. The master sends the PCM1789 slave address with a read bit after storing the register address. Then the PCM1789 transfers the data that the index register points to. Figure 35 shows a diagram of the read operation.

Transmitter	М	М	М	S	М	S	М	М	М	S	S	М	м
Data Type	St	Slave Address	\overline{W}	ACK	Reg Address	ACK	Sr	Slave Address ⁽¹⁾	R	ACK	Read Data	NACK	Sp

(1) The slave address after the repeated start condition must be the same as the previous slave address.

NOTE: M = Master device, S = Slave device, St = Start condition, Sr = Repeated start condition, \overline{W} = Write, R = Read, ACK = Acknowledge, NACK = Not acknowledge, and Sp = Stop condition.

Figure 35. Framework for Read Operation

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TIMING REQUIREMENTS: SCL AND SDA

A detailed timing diagram for SCL and SDA is shown in Figure 36.

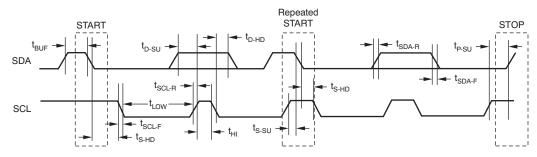


Figure 36. SCL and SDA Control Interface Timing

		STANDAR	RD MODE	FAST N	IODE	
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNIT
f _{SCL}	SCL clock frequency		100		400	kHz
t _{BUF}	Bus free time between STOP and START condition	4.7		1.3		μs
t _{LOW}	Low period of the SCL clock	4.7		1.3		μs
t _{HI}	High period of the SCL clock	4.0		0.6		μs
t _{S-SU}	Setup time for START/Repeated START condition	4.7		0.6		μs
t _{S-HD}	Hold time for START/Repeated START condition	4.0		0.6		μs
t _{D-SU}	Data setup time	250		100		ns
t _{D-HD}	Data hold time	0	3450	0	900	ns
t _{SCL-R}	Rise time of SCL signal		1000	20 + 0.1 C _B	300	ns
t _{SCL-F}	Fall time of SCL signal		1000	20 + 0.1 C _B	300	ns
t _{SDA-R}	Rise time of SDA signal		1000	20 + 0.1 C _B	300	ns
t _{SDA-F}	Fall time of SDA signal		1000	20 + 0.1 C _B	300	ns
t _{P-SU}	Setup time for STOP condition	4.0		0.6		μs
t _{GW}	Allowable glitch width		N/A		50	ns
C _B	Capacitive load for SDA and SCL line		400		100	pF
V _{NH}	Noise margin at high level for each connected device (including hysteresis)	0.2 × VDD		0.2 × VDD		V
V _{NL}	Noise margin at low level for each connected device (including hysteresis)	0.1 × VDD		0.1 × VDD		V
V _{HYS}	Hysteresis of Schmitt trigger input	N/A		0.05 × VDD		V

Table 12. Timing Requirements for Figure 36



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CONTROL REGISTER DEFINITIONS (SOFTWARE MODE ONLY)

The PCM1789 has many user-programmable functions that are accessed via control registers, and are programmed through the SPI or I²C serial control port. Table 13 shows the available mode control functions along with reset default conditions and associated register addresses. Table 14 lists the register map.

Table 13. User-Programmable Mode Control Functions

FUNCTION	RESET DEFAULT	REGISTER ⁽¹⁾	LABEL
Mode control register reset	Normal operation	16	MRST
System reset	Normal operation	16	SRST
Analog mute function control	Mute disabled	16	AMUTE[3:0]
Sampling mode selection	Auto	16	SRDA[1:0]
Power-save mode selection	Power save	17	PSMDA
Audio interface format selection	l ² S	17	FMTDA[2:0]
Operation control	Normal operation	18	OPEDA
Digital filter roll-off control	Sharp roll-off	18	FLT
Output phase selection	Normal	19	REVDA[2:1]
Soft mute control	Mute disabled	20	MUTDA[2:1]
Zero flag	Not detected	21	ZERO[2:1]
Digital attenuation mode	0 dB to -63 dB, 0.5-dB step	22	DAMS
Digital de-emphasis function control	Disabled	22	DEMP[1:0]
AMUTEO/ZERO flag selection	ZERO2	22	MZSEL
Zero flog function coloction	ZERO1: left-channel	22	AZRO
Zero flag function selection	ZERO2: right-channel	operation16operation16isabled16isabled16ito16r save17S17operation18roll-off18mal19isabled20tected213, 0.5-dB step22bled22color22off-channel22off-channel22ofdetection22	AZRO
Zero flag polarity selection	High for detection	22	ZREV
Digital attenuation level setting	0 dB, no attenuation	24, 25	ATDAx[7:0]

(1) If ADR6 or ADR5 is high, the register address must be changed to the number shown + offset; offset is 32, 64 and 96 according to state of ADR6, 5 (01, 10 and 11).

)] B3 B2 B1 B0
B3 B2 B1 B0
MUTE1 AMUTE0 SRDA1 SRDA0
RSV ⁽²⁾ FMTDA2 FMTDA1 FMTDA0
RSV ⁽²⁾ RSV ⁽²⁾ RSV ⁽²⁾ FLT
RSV ⁽²⁾ RSV ⁽²⁾ REVDA2 REVDA1
RSV ⁽²⁾ RSV ⁽²⁾ MUTDA2 MUTDA1
RSV ⁽²⁾ RSV ⁽²⁾ ZERO2 ZERO1
AZSEL RSV ⁽²⁾ AZRO ZREV
RSV ⁽²⁾ RSV ⁽²⁾ RSV ⁽²⁾ RSV ⁽²⁾
TDA13 ATDA12 ATDA11 ATDA10
TDA23 ATDA22 ATDA21 ATDA20

Table 14. Register Map

(1) If ADR6 or ADR5 is high, the register address must be changed to the number shown + offset; offset is 32, 64 and 96 according to state of ADR6, 5 (01, 10 and 11).

(2) RSV must be set to '0'.



REGISTER DEFINITIONS

DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0
16	10	MRST	SRST	AMUTE3	AMUTE2	AMUTE1	AMUTE0	SRDA1	SRDA0

MRST Mode control register reset

This bit sets the mode control register reset to the default value. Pop noise may be generated. Returning the MRST bit to '1' is unnecessary because it is automatically set to '1' after the mode control register is reset.

Default value = 1.

MRST Mode control register reset

- 0 Set default value
- 1 Normal operation (default)

SRST System reset

This bit controls the system reset, which includes the resynchronization between the system clock and sampling clock, and DAC operation restart. The mode control register is not reset and the PCM1789 does not go into a power-down state. Returning the SRST bit to '1' is unnecessary; it is automatically set to '1' after triggering a system reset.

Default value = 1.

SRST System reset

- 0 Resynchronization
- 1 Normal operation (default)

AMUTE[3:0] Analog mute function control

These bits control the enabling/disabling of each source event that triggers the analog mute control circuit.

Default value = 0000.

AMUTE Analog mute function control

- xxx0 Disable analog mute control by SCKI halt
- xxx1 Enable analog mute control by SCKI halt
- xx0x Disable analog mute control by asynchronous detect
- xx1x Enable analog mute control by asynchronous detect
- x0xx Disable analog mute control by ZERO1 and ZERO2 detect
- x1xx Enable analog mute control by ZERO1 and ZERO2 detect
- 0xxx Disable analog mute control by DAC disable command
- 1xxx Enable analog mute control by DAC disable command



SRDA[1:0] Sampling mode selection

These bits control the sampling mode of DAC operation. In Auto mode, the sampling mode is automatically set according to multiples between the system clock and sampling clock: single rate for 512 f_S , 768 f_S , and 1152 f_S , dual rate for 256 f_S or 384 f_S , and quad rate for 128 f_S and 192 f_S . Default value = 00.

	SRD	A Sam	pling mod	e selection	l				
	00	Auto	(default)						
	01	Sing	le rate						
	10	Dua	l rate						
	11	Qua	d rate						
DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0
17	11	PSMDA	RSV	RSV	RSV	RSV	FMTDA2	FMTDA1	FMTDA0

PSMDA Power-save mode selection

This bit selects the power-save mode for the OPEDA function. When PSMDA = 0, OPEDA controls the power-save mode and normal operation. When PSMDA = 1, OPEDA functions controls the DAC disable (not power-save mode) and normal operation.

Default value: 0.

PSMDA Power-save mode selection

- 0 Power-save enable mode (default)
- 1 Power-save disable mode

RSV Reserved

Reserved; do not use.

FMTDA[2:0] Audio interface format selection

These bits control the audio interface format for DAC operation. Details of the format and any related restrictions with the system clock are described in the *Audio Data Interface Formats and Timing* section.

Default value: 0000 (16-/20-/24-/32-bit I²S format).

FMTDA	Audio interface format selection
000	16-/20-/24-/32-bit I ² S format (default)
001	16-/20-/24-/32-bit left-justified format
010	24-bit right-justified format
011	16-bit right-justified format
100	24-bit I ² S mode DSP format

- 101 24-bit left-justified mode DSP format
- 110 Reserved
- 111 Reserved



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DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0
18	12	RSV	RSV	RSV	OPEDA	RSV	RSV	RSV	FLT

RSV Reserved

Reserved; do not use.

OPEDA Operation control

This bit controls the DAC operation mode. In operation disable mode, the DAC output is cut off from DIN and the internal DAC data are reset. If PSMDA = 1, the DAC output is forced into VCOM. If PSMDA = 0, the DAC output is forced into AGND and the DAC goes into a power-down state. For normal operating mode, this bit must be '0'. The serial mode control is effective during operation disable mode.

Default value: 0.

OPEDA Operation control

- 0 Normal operation
- 1 Operation disable with or without power save

FLT Digital filter roll-off control

This bit allows users to select the digital filter roll-off that is best suited to their applications. Sharp and slow filter roll-off selections are available. The filter responses for these selections are shown in the Typical Characteristics sections of this data sheet.

Default value: 0.

FLT Digital filte	er roll-off control
-------------------	---------------------

- 0 Sharp roll-off
- 1 Slow roll-off

DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0
19	13	RSV	RSV	RSV	RSV	RSV	RSV	REVDA2	REVDA1

RSV Reserved

Reserved; do not use.

REVDA[2:1] Output phase selection

These bits are used to control the phase of the DAC analog signal outputs.

Default value: 00.

REVDA Output phase selection

- x0 Left channel normal output
- x1 Left channel inverted output
- 0x Right channel normal output
- 1x Right channel inverted output



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DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0
20	14	RSV	RSV	RSV	RSV	RSV	RSV	MUTDA2	MUTDA1

RSV Reserved

Reserved; do not use.

MUTDA[2:1] Soft Mute control

These bits are used to enable or disable the Soft Mute function for the corresponding DAC outputs, VOUTx. The Soft Mute function is incorporated into the digital attenuators. When mute is disabled (MUTDA[2:1] = 0), the attenuator and DAC operate normally. When mute is enabled by setting MUTDA[2:1] = 1, the digital attenuator for the corresponding output is decreased from the current setting to infinite attenuation. By setting MUTDA[2:1] = 0, the attenuator is increased to the last attenuation level in the same manner as it is for decreasing levels. This configuration reduces *pop and zipper noise* during muting of the DAC output. This Soft Mute control uses the same resource of digital attenuation level setting. Mute control has priority over the digital attenuation level setting.

Default value: 00.

MUTDA	Sof	t Mute cont	rol				
x0	Left	Left channel mute disabled					
x1	Left	channel mu	te enabled				
0x	Rigl	Right channel mute disabled					
1x	Rigl	Right channel mute enabled					
FX	B7	B6	B5				

DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0
21	15	RSV	RSV	RSV	RSV	RSV	RSV	ZERO2	ZERO1

RSV Reserved

Reserved; do not use.

ZERO[2:1] Zero flag (read-only)

These bits indicate the present status of the zero detect circuit for each DAC channel; these bits are read-only.

ZERO Zero flag

- x0 Left channel zero input not detected
- x1 Left channel zero input detected
- 0x Right channel zero input not detected
- 1x Right channel zero input detected

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DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0
22	16	DAMS	RSV	DEMP1	DEMP0	MZSEL	RSV	AZRO	ZREV

DAMS Digital attenuation mode

This bit selects the attenuation mode.

Default value: 0.

DAMS Digital attenuation mode

- 0 Fine step: 0.5-dB step for 0 dB to -63 dB range (default)
- 1 Wide range: 1-dB step for 0 dB to -100 dB range

RSV Reserved

Reserved; do not use.

DEMP[1:0] Digital de-emphasis function/sampling rate control

These bits are used to disable and enable the various sampling frequencies of the digital de-emphasis function.

Default value: 00.

DEMP Digital de-emphasis function/sampling rate control

- 00 Disable (default)
- 01 48 kHz enable
- 10 44.1 kHz enable
- 11 32 kHz enable

MZSEL AMUTEO/ZERO flag selection

This bit is used to select the function of the ZERO2 pin.

Default value: 0.

MZSEL AMUTEO/ZERO flag selection

- 0 The ZERO2 pin functions as ZERO2 (default).
- 1 The ZERO2 pin functions as AMUTEO.

AZRO Zero flag channel combination selection

This bit is used to select the zero flag channel combination for ZERO1 and ZERO2.

Default value: 0.

AZRO Zero flag combination selection

- 0 Combination A: ZERO1 = left channel, ZERO2 = right channel (default)
- 1 Combination B: ZERO1 = left channel or right channel, ZERO2 = left channel and right channel

ZREV Zero flag polarity selection

This bit controls the polarity of the zero flag pin.

Default value: 0.

ZREV Zero flag polarity selection

- 0 High for zero detect (default)
- 1 Low for zero detect

DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0
23	17	RSV							
24	18	ATDA17	ATDA16	ATDA15	ATDA14	ATDA13	ATDA12	ATDA11	ATDA10
25	19	ATDA27	ATDA26	ATDA25	ATDA24	ATDA23	ATDA22	ATDA21	ATDA20

RSV Reserved

NSTRUMENTS

Reserved; do not use.

ATDAx[7:0] Digital attenuation level setting

Where x = 1 to 2, corresponding to the DAC output (VOUTx).

Both DAC outputs (VOUTL and VOUTR) have a digital attenuation function. The attenuation level can be set from 0 dB to R dB, in S-dB steps. Changes in attenuator levels are made by incrementing or decrementing one step (S dB) for every $8/f_S$ time interval until the programmed attenuator setting is reached. Alternatively, the attenuation level can be set to infinite attenuation (or mute). R (range) and S (step) is -63 and 0.5 for DAMS = 0, and -100 and 1.0 for DAMS = 1, respectively. The DAMS bit is defined in register 22 (16h). Table 15 shows attenuation levels for various settings.

The attenuation level for each channel can be set individually using the following formula:

Attenuation level (dB) = $S \times (ATDAx[7:0]_{DEC} - 255)$

where $ATDAx[7:0]_{DEC} = 0$ through 255.

For $ATDAx[7:0]_{DEC} = 0$ through 128 with DAMS = 0, or 0 through 154 with DAMS = 1, attenuation is set to infinite attenuation (mute).

Default value: 1111 1111.

ATDA	x[7:0]	ATTENUATION	LEVEL SETTING
BINARY	DECIMAL	DAMS = 0	DAMS = 1
1111 1111	255	0 dB, no attenuation (default)	0 dB, no attenuation (default)
1111 1110	254	-0.5 dB	-1 dB
1111 1101	253	-1.0 dB	-2 dB
1001 1100	156	-45.9 dB	–99 dB
1001 1011	155	–50.0 dB	-100 dB
1001 1010	154	–50.5 dB	Mute
1000 0010	130	–62.5 dB	Mute
1000 0001	129	–63.0 dB	Mute
0000 0000	128	Mute	Mute
0000 0000	0	Mute	Mute

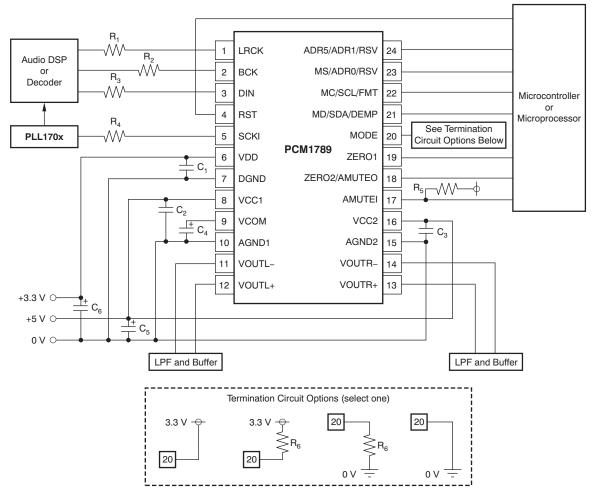
Table 15. Attenuation Levels for Various Settings



APPLICATION INFORMATION

CONNECTION DIAGRAMS

A basic connection diagram is shown in Figure 37, with the necessary power-supply bypassing and decoupling components. Texas Instruments' PLL170X is used to generate the system clock input at SCKI, as well as to generate the clock for the audio signal processor. The use of series resistors (22Ω to 100Ω) are recommended for SCKI, LRCK, BCK, and DIN for electromagnetic interference (EMI) reduction.



NOTE: C_1 through C_3 are 1- μ F ceramic capacitors. C_4 through C_6 are 10- μ F electrolytic capacitors. R_1 through R_4 are 22- Ω to 100- Ω resistors. R_5 is a resistor appropriate for pull-up. R_6 is a 220-k Ω resistor, ±5%. An appropriate resistor is required for pull-up, if ZERO2/AMUTEO pin is used as AMUTEO.



POWER SUPPLY AND GROUNDING

The PCM1789 requires +5 V for the analog supply and +3.3 V for the digital supply. The +5-V supply is used to power the DAC analog and output filter circuitry, and the +3.3-V supply is used to power the digital filter and serial interface circuitry. For best performance, it is recommended to use a linear regulator (such as the REG101-5/33, REG102-5/33, or REG103-5/33) with the +5-V and +3.3-V supplies.

Five capacitors are required for supply bypassing, as shown in Figure 37. These capacitors should be located as close as possible to the PCM1789 package. The 10- μ F capacitors are aluminum electrolytic, while the three 1- μ F capacitors are ceramic.

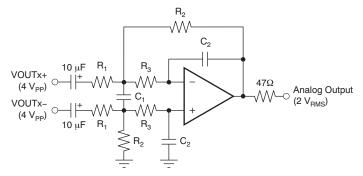


LOW-PASS FILTER AND DIFFERENTIAL-TO-SINGLE-ENDED CONVERTER FOR DAC OUTPUTS

 $\Delta\Sigma$ DACs use noise-shaping techniques to improve in-band signal-to-noise ratio (SNR) performance at the expense of generating increased out-of-band noise above the Nyquist frequency, or f_S/2. The out-of-band noise must be low-pass filtered in order to provide optimal converter performance. This filtering is accomplished by a combination of on-chip and external low-pass filters.

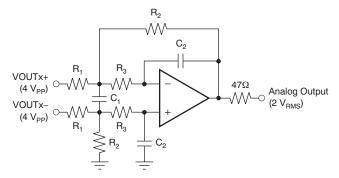
Figure 38 and Figure 39 show the recommended external differential-to-single-ended converter with low-pass active filter circuits for ac-coupled and dc-coupled applications. These circuits are second-order Butterworth filters using a multiple feedback (MFB) circuit arrangement that reduces sensitivity to passive component variations over frequency and temperature. For more information regarding MFB active filter designs, please refer to Applications Bulletin SBAA055, *Dynamic Performance Testing of Digital Audio D/A Converters*, available from the TI web site (www.ti.com) or your local Texas Instruments' sales office.

Because the overall system performance is defined by the quality of the DACs and the associated analog output circuitry, high-quality audio op amps are recommended for the active filters. Texas Instruments' OPA2134, OPA2353, and NE5532A dual op amps are shown in Figure 38 and Figure 39, and are recommended for use with the PCM1789.



NOTE: Amplifier is an NE5532A x 1/2 or OPA2134 x1/2; $R_1 = 7.5 \text{ k}\Omega$; $R_2 = 5.6 \text{ k}\Omega$; $R_3 = 360 \Omega$; $C_1 = 3300 \text{ pF}$; $C_2 = 680 \text{ pF}$; Gain = 0.747; $f_{-3 \text{ dB}} = 53 \text{ kHz}$.

Figure 38. AC-Coupled, Post-LPF and Differential to Single-Ended Buffer



NOTE: Amplifier is an NE5532A x 1/2 or OPA2134 x1/2; $R_1 = 15 \text{ k}\Omega$; $R_2 = 11 \text{ k}\Omega$; $R_3 = 820 \Omega$; $C_1 = 1500 \text{ pF}$; $C_2 = 330 \text{ pF}$; Gain = 0.733; $f_{-3 \text{ dB}} = 54 \text{ kHz}$.

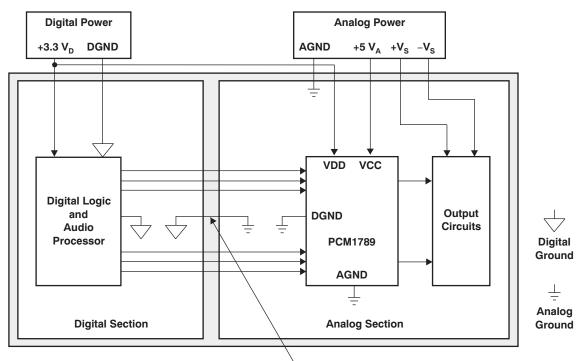
Figure 39. DC-Coupled, Post-LPF and Differential to Single-Ended Buffer



PCB LAYOUT GUIDELINES

A typical printed circuit board (PCB) layout for the PCM1789 is shown in Figure 40. A ground plane is recommended, with the analog and digital sections being isolated from one another using a split or cut in the circuit board. The PCM1789 should be oriented with the digital I/O pins facing the ground plane split/cut to allow for short, direct connections to the digital audio interface and control signals originating from the digital section of the board.

Separate power supplies are recommended for the digital and analog sections of the board. This configuration prevents the switching noise present on the digital supply from contaminating the analog power supply and degrading the dynamic performance of the PCM1789.



Return Path for 3.3 $\rm V_{\rm D}$ and Digital Signals

Figure 40. Recommended PCB Layout



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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (October 2008) to Revision A					
•	Changed Figure 37	32			



PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
PCM1789PW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Request Free Samples
PCM1789PWG4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Request Free Samples
PCM1789PWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples
PCM1789PWRG4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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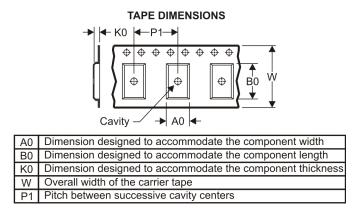
PACKAGE MATERIALS INFORMATION

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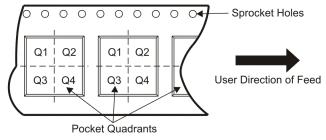
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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal				
Device	Package	Package	Pins	SPQ

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM1789PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TEXAS INSTRUMENTS

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PACKAGE MATERIALS INFORMATION

20-Jul-2010

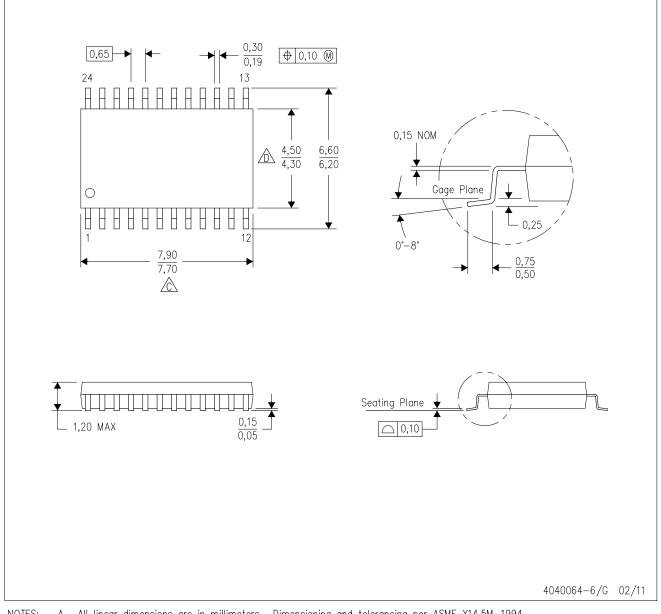


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM1789PWR	TSSOP	PW	24	2000	346.0	346.0	33.0

PW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 B. This drawing is subject to change without notice.

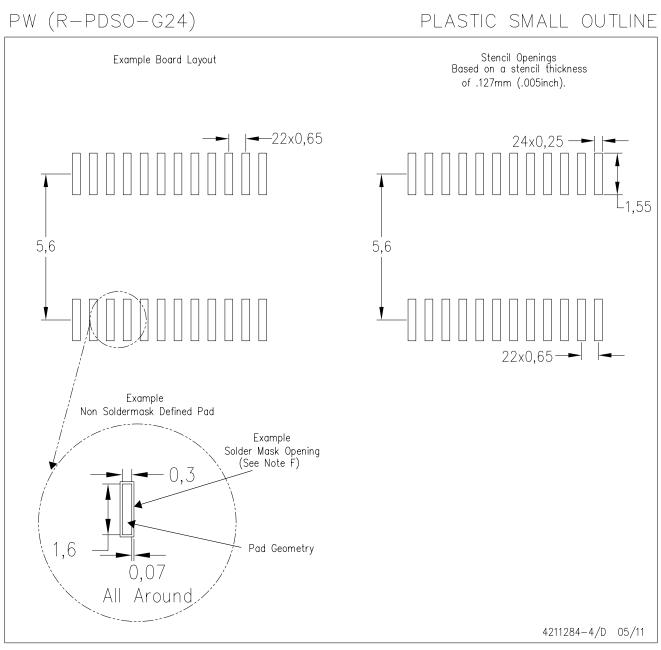
Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153



LAND PATTERN DATA



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication $\ensuremath{\mathsf{IPC-7351}}$ is recommended for alternate design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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