

LOW-VOLTAGE AND LOW-POWER STEREO AUDIO DIGITAL-TO-ANALOG CONVERTER WITH LINEOUT AMPLIFIER

FEATURES

- Multilevel DAC Including Lineout Amplifier
- Analog Performance (V_{CC1}, V_{CC2} = 2.4 V):
 - Dynamic Range: 98 dB Typ
 - THD+N at 0 dB: 0.007% Typ
- 1.6-V to 3.6-V Single Power Supply
- Low Power Dissipation:
 6 mW at V_{CC1}, V_{CC2} = 2.4 V
- System Clock: 128 f_S, 192 f_S, 256 f_S, 384 f_S
- Sampling Frequency: 5 kHz to 50 kHz
- Software Control (PCM1772):
 - 16-, 20-, 24-Bit Word Available
 - Left-, Right-Justified, and I²S
 - Slave/Master Selectable
 - Digital Attenuation: 0 dB to -62 dB,
 1 dB/Step
 - 44.1-kHz Digital De-Emphasis
 - Zero Cross Attenuation
 - Digital Soft Mute
 - Monaural Analog-In With Mixing
 - Monaural Speaker Mode
- Hardware Control (PCM1773):
 - Left-Justified and I²S
 - 44.1-kHz Digital De-Emphasis
 - Monaural Analog-In With Mixing
- Pop-Noise-Free Circuit
- 3.3-V Tolerant
- Packages: TSSOP-16 and VQFN-20

APPLICATIONS

- Portable Audio Player
- Cellular Phone
- PDA
- Other Applications Requiring Low-Voltage Operation

DESCRIPTION

The PCM1772 and PCM1773 devices are CMOS, monolithic, integrated circuits which include stereo digital-to-analog converters, lineout circuitry, and support circuitry in small TSSOP-16 and VQFN-20 packages.

The data converters use Tl's enhanced multilevel Δ - Σ architecture, which employs noise shaping and multilevel amplitude quantization to achieve excellent dynamic performance and improved tolerance to clock jitter. The PCM1772 and PCM1773 devices accept several industry standard audio data formats with 16- to 24-bit data, left-justified, l²S, etc., providing easy interfacing to audio DSP and decoder devices. Sampling rates up to 50 kHz are supported. A full set of user-programmable functions is accessible through a 3-wire serial control port, which supports register write functions.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

| | PCM1772 PCM1773 |
|---|--------------------|
| Supply voltage: V _{CC1} , V _{CC2} | -0.3 V to 4 V |
| Supply voltage differences: V _{CC1} , V _{CC2} | ±0.1 V |
| Ground voltage differences | ±0.1 V |
| Digital input voltage | -0.3 V to 4 V |
| Input current (any terminals except supplies) | ±10 mA |
| Operating temperature | -40°C to 125°C |
| Storage temperature | −55°C to 150°C |
| Junction temperature | 150°C |
| Lead temperature (soldering) | 260°C, 5 s |
| Package temperature (IR reflow, peak) | 260°C |

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range

| | | MIN | NOM | MAX | UNIT |
|--|---|------|------|------|------|
| Supply voltage: V _{CC} 1, V _{CC} 2 | | 1.6 | 2.4 | 3.6 | V |
| Digital input logic family | | | CMOS | | |
| Digital input clock frequency | System clock | 0.64 | | 19.2 | MHz |
| Digital input clock frequency | gic family ock frequency System clock Sampling clock load resistance evel (V _{CC} 2 = 2.4 V) | 5 | | 50 | kHz |
| Analog output load resistance | | 10 | | | kΩ |
| Analog input level (V _{CC} 2 = 2.4 V) | | | | 1.4 | Vp-p |
| Operating free-air temperature, T _A | | -25 | | 85 | °C |



ELECTRICAL CHARACTERISTICS

all specifications at T_A = 25°C, V_{CC1} = V_{CC2} = 2.4 V, f_S = 44.1 kHz, system clock = 256 f_S and 24-bit data, R_L = 10 k Ω , unless otherwise noted

| | PARAMETER | TEST CONDITIONS | | 72PW, PCM1 2RGA, PCM | | UNIT |
|-----------------|--------------------------------------|--|-------------------------|----------------------------|-----------------------------------|------------------|
| | | | MIN | TYP | MAX | |
| | Resolution | | | 24 | | Bits |
| OPERAT | TING FREQUENCY | | | | | |
| | Sampling frequency (f _S) | | 5 | | 50 | kHz |
| | System clock frequency | | 128 f _S , | 192 f _S , 256 f | _S , 384 f _S | |
| DIGITAL | INPUT/OUTPUT ⁽¹⁾⁽²⁾ | | | | | |
| V _{IH} | Input logic level | | 0.7 V _{CC1} | | | Vdc |
| V _{IL} | | | | | 0.3 V _{CC1} | Vdc |
| I _{IH} | Land Indianament | $V_{IN} = V_{CC1}$ | | | 10 | μΑ |
| I _{IL} | Input logic current | V _{IN} = 0 V | | | -10 | μΑ |
| V _{OH} | Output logic level ⁽³⁾ | I _{OH} = -2 mA | 0.7 V _{CC1} | | | Vdc |
| V _{OL} | | I _{OL} = 2 mA | | | 0.3 V _{CC1} | Vdc |
| DYNAMI | IC PERFORMANCE (LINE OUTPUT) | | | | | I. |
| | Full-scale output voltage | 0 dB | | 0.77 V _{CC2} | | V _{P-P} |
| | Dynamic range | EIAJ, A-weighted | 90 | 98 | | dB |
| | Signal-to-noise ratio | EIAJ, A-weighted | 90 | 98 | | dB |
| | THD+N | 0 dB | | 0.007% | 0.015% | |
| | Channel separation | | 70 | 80 | | dB |
| | Load resistance | | 10 | | | kΩ |
| DC ACC | URACY | | <u> </u> | | | |
| | Gain error | | | ±2 | ±8 | % of FSR |
| | Gain mismatch, channel-to-channel | | | ±2 | ±8 | % of FSR |
| | Bipolar zero error | V _{OUT} = 0.5 V _{CC1} at BPZ | | ±30 | ±75 | mV |
| ANALO | G LINE INPUT (MIXING CIRCUIT) | | | | | I. |
| | Analog input voltage range | | | 0 | .584 V _{CC2} | V _{P-P} |
| | Gain (analog input to line output) | | | 0.91 | | |
| | Analog input impedance | | | 10 | | kΩ |
| | THD+N | AIN = 0.56 V _{CC2} (peak-to-peak) | | 0.1% | | |
| DIGITAL | FILTER PERFORMANCE | | П | | | ı |
| | Pass band | | | | 0.454 f _S | |
| | Stop band | | 0.546 f _S | | | |
| | Pass-band ripple | | | | ±0.04 | dB |
| | Stop-band attenuation | | -50 | | | dB |
| | Group delay | | | 20/f _S | | |
| | 44.1-kHz de-emphasis error | | | ±0.1 | | dB |
| ANALO | G FILTER PERFORMANCE | | I . | | | 1 |
| | Frequency response | at 20 kHz | | ±0.2 | | dB |

- (1) Digital inputs and outputs are CMOS compatible.
 (2) All logic inputs are 3.3-V tolerant and not terminated internally.
 (3) LRCK and BCK terminals



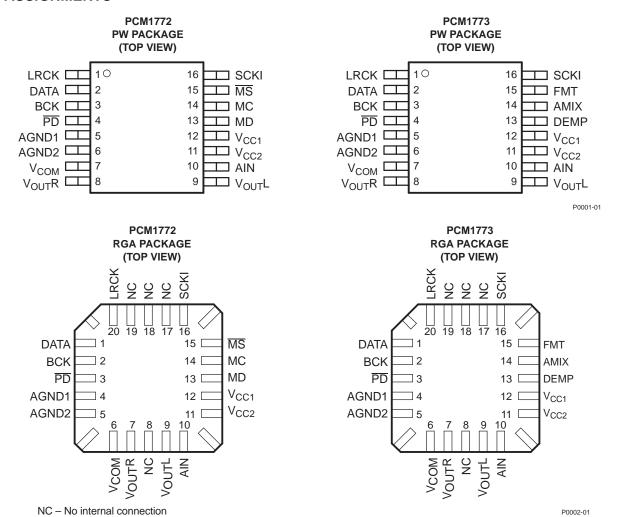
ELECTRICAL CHARACTERISTICS (continued)

all specifications at T_A = 25°C, V_{CC1} = V_{CC2} = 2.4 V, f_S = 44.1 kHz, system clock = 256 f_S and 24-bit data, R_L = 10 k Ω , unless otherwise noted

| PARAMETER | | TEST CONDITIONS | PCM1772I PCM1772R | UNIT | | | |
|-------------------------------------|--|--------------------------------------|----------------------|------|-----|------|--|
| | | | MIN TYP | | MAX | | |
| POWER SU | PPLY REQUIREMENTS | | | | | | |
| | Voltage range, V _{CC1} , V _{CC2} | | 1.6 | 2.4 | 3.6 | Vdc | |
| I _{CC1} | | BPZ input | | 1.5 | 2.5 | A | |
| I _{CC2} | Supply current | BPZ input | | 1 | 2.5 | mA | |
| I _{CC1} + I _{CC2} | | Power down ⁽⁴⁾ | | 5 | 15 | μΑ | |
| | Dower discination | BPZ input | | 6 | 12 | mW | |
| | Power dissipation | Power down ⁽⁴⁾ | | 12 | 36 | μW | |
| TEMPERAT | URE RANGE | | | | | | |
| | Operation temperature | | -25 | | 85 | °C | |
| 0 | Thermal resistance | PCM1772PW, -73PW: 16-terminal TSSOP | | 150 | | °C/M | |
| θ_{JA} | mermai resistance | PCM1772RGA, -73RGA: 20-terminal VQFN | | 130 | | °C/W | |

⁽⁴⁾ All input signals are held static.

PIN ASSIGNMENTS





TERMINAL FUNCTIONS

PCM1772PW

| TERMI | NAL | 1/0 | DESCRIPTION | | |
|--------------------|-----|-----|---|--|--|
| NAME | NO. | 1/0 | DESCRIPTION | | |
| AGND1 | 5 | _ | nalog ground. This is a return for V _{CC1} . | | |
| AGND2 | 6 | _ | g ground. This is a return for V _{CC2} . | | |
| AIN | 10 | I | Monaural analog signal mixer input. The signal can be mixed with the output of the L- and R-channel DACs. | | |
| BCK | 3 | I/O | Serial bit clock. Clocks the individual bits of the audio data input, DATA. In the slave interface mode, this clock is input from an external device. In master interface mode, the PCM1772 device generates the BCK output to an external device. | | |
| DATA | 2 | I | Serial audio data input | | |
| LRCK | 1 | I/O | Left and right clock. Determines which channel is being input on the audio data input, DATA. The frequency of LRCK must be the same as the audio sampling rate. In the slave interface mode, this clock is input from an external device. In the master interface mode, the PCM1772 device generates the LRCK output to an external device. | | |
| MC | 14 | I | Mode control port serial bit clock input. Clocks the individual bits of the control data input, MD. | | |
| MD | 13 | I | Mode control port serial data input. Controls the operation mode on the PCM1772 device. | | |
| MS | 15 | I | Mode control port select. The control port is active when this terminal is low. | | |
| PD | 4 | I | Reset input. When low, the PCM1772 device is powered down, and all mode control registers are reset to default settings. | | |
| SCKI | 16 | I | System clock input | | |
| V _{CC1} | 12 | _ | Power supply for all analog circuits except the lineout amplifier. | | |
| V _{CC2} | 11 | _ | Analog power supply for the lineout amplifier circuits. The voltage level must be the same as V _{CC1} . | | |
| V _{COM} | 7 | _ | Decoupling capacitor connection. An external 10- μ F capacitor connected from this terminal to analog ground is required for noise filtering. Voltage level of this terminal is 0.5 V_{CC2} nominal. | | |
| V _{OUT} L | 9 | 0 | L-channel analog signal output of the lineout amplifiers | | |
| V _{OUT} R | 8 | 0 | R-channel analog signal output of the lineout amplifiers | | |

PCM1772, PCM1773





PCM1772RGA

| TERMINAL | | 1/0 | DECORPTION | |
|--------------------|------------------|-----|---|--|
| NAME | NO. | I/O | DESCRIPTION | |
| AGND1 | 4 | _ | nalog ground. This is a return for V _{CC1} . | |
| AGND2 | 5 | _ | Analog ground. This is a return for V _{CC2} . | |
| AIN | 10 | I | Monaural analog signal mixer input. The signal can be mixed with the output of the L- and R-channel DACs. | |
| BCK | 2 | I/O | Serial bit clock. Clocks the individual bits of the audio data input, DATA. In the slave interface mode, this clock is input from an external device. In the master interface mode, the PCM1772 device generates the BCK output to an external device. | |
| DATA | 1 | - | Serial audio data input | |
| LRCK | 20 | I/O | Left and right clock. Determines which channel is being input on the audio data input, DATA. The frequency of LRCK must be the same as the audio sampling rate. In the slave interface mode, this clock is input from an external device. In the master interface mode, the PCM1772 device generates the LRCK output to an external device. | |
| MC | 14 | I | Mode control port serial bit clock input. Clocks the individual bits of the control data input, MD. | |
| MD | 13 | - | Mode control port serial data input. Controls the operation mode on the PCM1772 device. | |
| MS | 15 | - | Mode control port select. The control port is active when this terminal is low. | |
| NC | 8, 17, 18, 19 | _ | No connect | |
| PD | 3 | I | Reset input. When low, the PCM1772 device is powered down, and all mode control registers are reset to default settings. | |
| SCKI | 16 | I | System clock input | |
| V _{CC1} | 12 | _ | Power supply for all analog circuits except lineout amplifier. | |
| V _{CC2} | 11 | _ | Analog power supply for lineout amplifier circuits. The voltage level must be the same as V _{CC1} . | |
| V _{COM} | 6 | _ | Decoupling capacitor connection. An external 10- μ F capacitor connected from this terminal to analog ground is required for noise filtering. Voltage level of this terminal is 0.5 V_{CC2} nominal. | |
| V _{OUT} L | 9 | 0 | L-channel analog signal output of lineout amplifiers. | |
| $V_{OUT}R$ | 7 | 0 | R-channel analog signal output of lineout amplifiers. | |



PCM1773PW

| TERMI | TERMINAL | | DESCRIPTION |
|--------------------|----------|-----|--|
| NAME | NO. | I/O | DESCRIPTION |
| AGND1 | 5 | _ | Analog ground. This is a return for V_{CC1} . |
| AGND2 | 6 | _ | Analog ground. This is a return for V_{CC2} . |
| AIN | 10 | I | Monaural analog signal mixer input. The signal can be mixed with the output of the L- and R-channel DACs. |
| AMIX | 14 | I | Analog mixing control |
| BCK | 3 | I | Serial bit clock. Clocks the individual bits of the audio data input, DATA. |
| DATA | 2 | I | Serial audio data input |
| DEMP | 13 | I | De-emphasis control |
| FMT | 15 | I | Data format select |
| LRCK | 1 | I | Left and right clock. Determines which channel is being input on the audio data input, DATA. The frequency of LRCK must be the same as the audio sampling rate. |
| PD | 4 | I | Reset input. When low, the PCM1773 device is powered down, and all mode control registers are reset to default settings. |
| SCKI | 16 | I | System clock input |
| V _{CC1} | 12 | _ | Power supply for all analog circuits except the lineout amplifier |
| V _{CC2} | 11 | _ | Analog power supply for the lineout amplifier circuits. The voltage level must be the same as V _{CC1} . |
| V _{COM} | 7 | _ | Decoupling capacitor connection. An external 10- μ F capacitor connected from this terminal to analog ground is required for noise filtering. Voltage level of this terminal is 0.5 V_{CC2} nominal. |
| V _{OUT} L | 9 | 0 | L-channel analog signal output of the lineout amplifiers |
| V _{OUT} R | 8 | 0 | R-channel analog signal output of the lineout amplifiers |

PCM1773RGA

| - | | | |
|--------------------|------------------|-----|--|
| TERM | INAL | 1/0 | DESCRIPTION |
| NAME | NO. | | |
| AGND1 | 4 | _ | Analog ground. This is a return for V _{CC1} . |
| AGND2 | 5 | | Analog ground. This is a return for V _{CC2} . |
| AIN | 10 | Ι | Monaural analog signal mixer input. The signal can be mixed with the output of the L- and R-channel DACs. |
| AMIX | 14 | Ι | Analog mixing control |
| BCK | 2 | Ι | Serial bit clock. Clocks the individual bits of the audio data input, DATA. |
| DATA | 1 | Ι | Serial audio data input |
| DEMP | 13 | I | De-emphasis control |
| FMT | 15 | I | Data format select |
| LRCK | 20 | I | Left and right clock. Determines which channel is being input on the audio data input, DATA. The frequency of LRCK must be the same as the audio sampling rate. |
| NC | 8, 17, 18, 19 | | No connect |
| PD | 3 | I | Reset input. When low, the PCM1773 device is powered down, and all mode control registers are reset to default settings. |
| SCKI | 16 | I | System clock input |
| V _{CC1} | 12 | _ | Power supply for all analog circuits except the lineout amplifier |
| V _{CC2} | 11 | | Analog power supply for the lineout amplifier circuits. The voltage level must be the same as V _{CC1} . |
| V _{COM} | 6 | _ | Decoupling capacitor connection. An external 10- μ F capacitor connected from this terminal to analog ground is required for noise filtering. Voltage level of this terminal is 0.5 V_{CC2} nominal. |
| V _{OUT} L | 9 | 0 | L-channel analog signal output of the lineout amplifiers |
| V _{OUT} R | 7 | 0 | R-channel analog signal output of the lineout amplifiers |
| | | | |

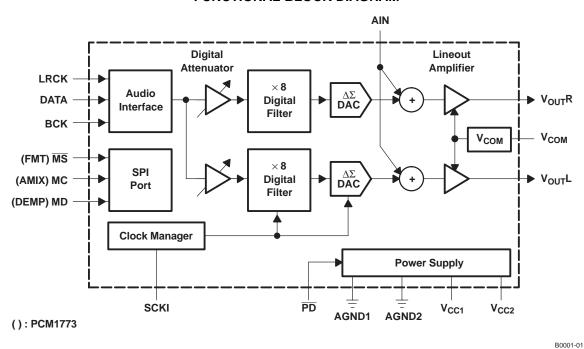


0.4

0.5

G002

FUNCTIONAL BLOCK DIAGRAM

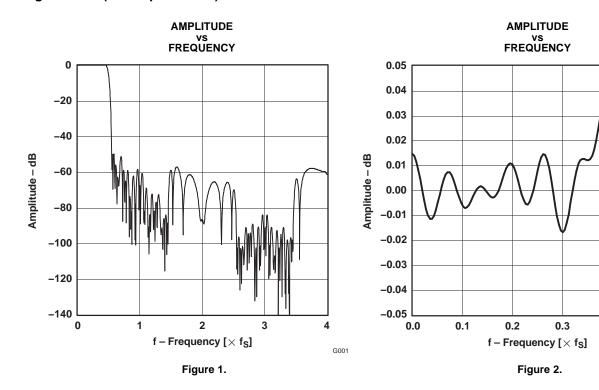


TYPICAL PERFORMANCE CURVES

All specifications at T_A = 25°C, V_{CC1} = V_{CC2} = 2.4 V, f_S = 44.1 kHz, system clock = 256 f_S and 24-bit data, R_L = 10 k Ω , unless otherwise noted.

DIGITAL FILTER

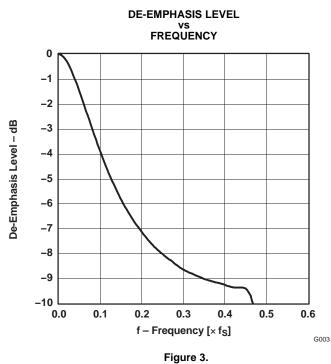
Digital Filter (De-Emphasis Off)

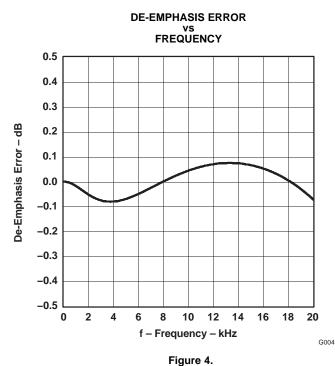


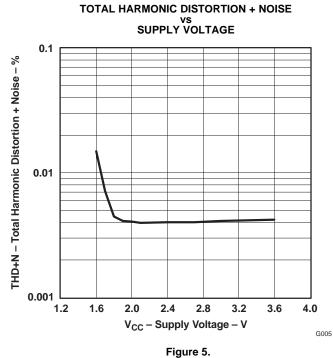


All specifications at $T_A = 25$ °C, $V_{CC1} = V_{CC2} = 2.4$ V, $f_S = 44.1$ kHz, system clock = 256 f_S and 24-bit data, $R_L = 10$ k Ω , unless otherwise noted.

De-Emphasis Curves







DYNAMIC RANGE vs SUPPLY VOLTAGE 104 102

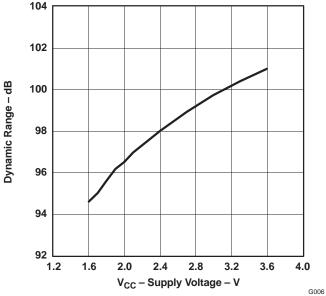


Figure 6.



All specifications at $T_A = 25$ °C, $V_{CC1} = V_{CC2} = 2.4$ V, $f_S = 44.1$ kHz, system clock = 256 f_S and 24-bit data, $R_L = 10$ k Ω , unless otherwise noted.

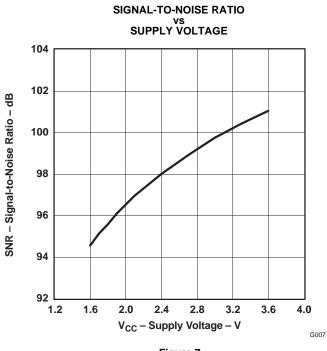


Figure 7.

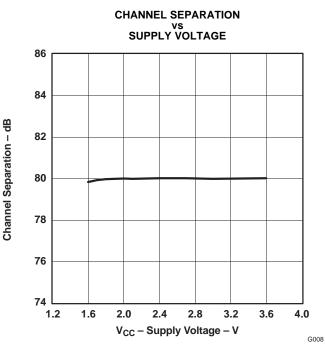
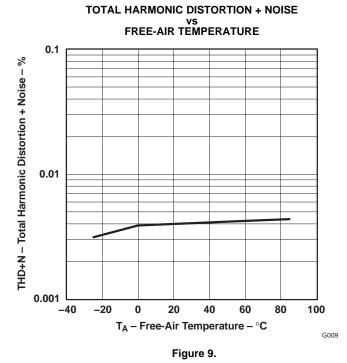
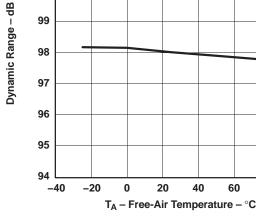


Figure 8.

DYNAMIC RANGE

vs FREE-AIR TEMPERATURE





102

101

100

Figure 10.

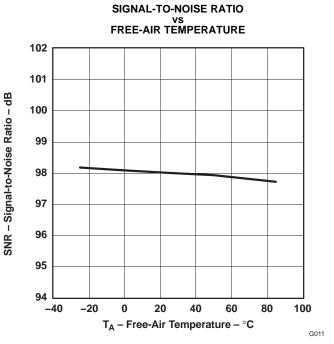
80

100

G010



All specifications at $T_A = 25$ °C, $V_{CC1} = V_{CC2} = 2.4$ V, $f_S = 44.1$ kHz, system clock = 256 f_S and 24-bit data, $R_L = 10$ k Ω , unless otherwise noted.



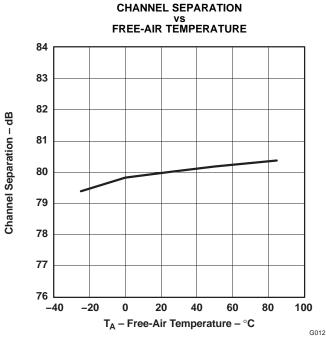
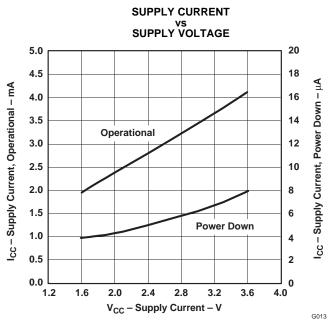


Figure 11.





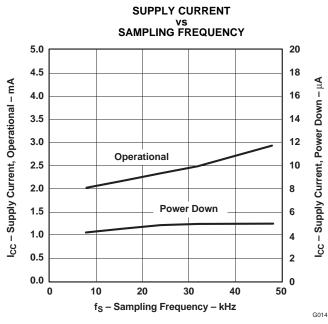
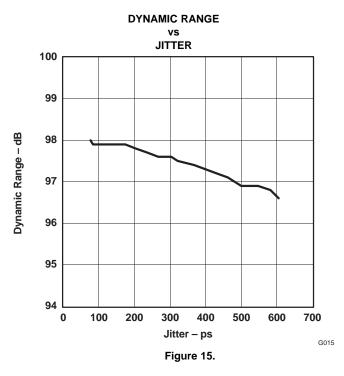


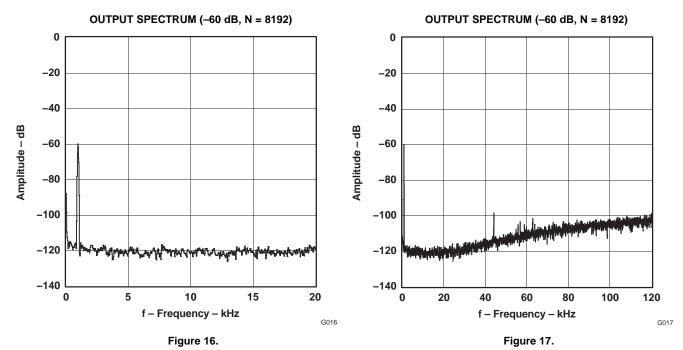
Figure 13.

Figure 14.



All specifications at $T_A = 25$ °C, $V_{CC1} = V_{CC2} = 2.4$ V, $f_S = 44.1$ kHz, system clock = 256 f_S and 24-bit data, $R_L = 10$ k Ω , unless otherwise noted.







DETAILED DESCRIPTION

System Clock, Reset, and Functions

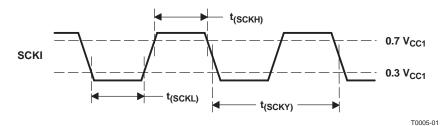
System Clock Input

The PCM1772 and PCM1773 devices require a system clock for operating the digital interpolation filters and multilevel Δ - Σ modulators. The system clock is applied at terminal 16 (SCKI). Table 1 shows examples of system clock frequencies for common audio sampling rates.

Figure 18 shows the timing requirements for the system clock input. For optimal performance, it is important to use a clock source with low phase jitter and noise.

Table 1. System Clock Frequency for Common Audio Sampling Frequencies

| SAMPLING FREQUENCY, LRCK | SYSTEM CLOCK FREQUENCY, SCKI (MHz) | | | | |
|--------------------------|------------------------------------|--------------------|--------------------|--------------------|--|
| | 128 f _S | 192 f _S | 256 f _S | 384 f _S | |
| 48 kHz | 6.144 | 9.216 | 12.288 | 18.432 | |
| 44.1 kHz | 5.6448 | 8.4672 | 11.2896 | 16.9344 | |
| 32 kHz | 4.096 | 6.144 | 8.192 | 12.288 | |
| 24 kHz | 3.072 | 4.608 | 6.144 | 9.216 | |
| 22.05 kHz | 2.8224 | 4.2336 | 5.6448 | 8.4672 | |
| 16 kHz | 2.048 | 3.072 | 4.096 | 6.144 | |
| 12 kHz | 1.536 | 2.304 | 3.072 | 4.608 | |
| 11.025 kHz | 1.4112 | 2.1168 | 2.8224 | 4.2336 | |
| 8 kHz | 1.024 | 1.536 | 2.048 | 3.072 | |



| SYMBOL | PARAMETER | MIN | UNIT |
|---------------------|--|-----|------|
| t _(SCKH) | System clock pulse duration, HIGH | 7 | ns |
| t _(SCKL) | System clock pulse duration, LOW | 7 | ns |
| t _(SCKY) | System clock pulse cycle time ⁽¹⁾ | 52 | ns |

(1) $1/(128 f_S)$, $1/(192 f_S)$, $1/(256 f_S)$ or $1/(384 f_S)$

Figure 18. System Clock Timing



Power On/Off and Reset

The PCM1772/73 always must have the \overline{PD} pin set from LOW to HIGH once after power-supply voltages V_{CC1} and V_{CC2} have reached the specified voltage range and stable clocks SCKI, BCK, and LRCK are being supplied for the power-on sequence. A minimum time of 1 ms after both the clock and power-supply requirements are met is required before the \overline{PD} pin changes from LOW to HIGH, as shown in Figure 19. Subsequent to the \overline{PD} LOW-to-HIGH transition, the internal logic state is held in reset for 1024 system clock cycles prior to the start of the power-on sequence. During the power-on sequence, $V_{OUT}L$ and $V_{OUT}R$ increase gradually from ground level, reaching an output level that corresponds to the input data after a period of 9334/f_S. When powering off, the \overline{PD} pin is set from HIGH to LOW first. Then $V_{OUT}L$ and $V_{OUT}R$ decrease gradually to ground level over a period of 9334/f_S, as shown in Figure 20, after which power can be removed without creating pop noise. When powering on or off, adhering to the timing requirements of Figure 19 and Figure 20 ensures that pop noise does not occur. If the timing requirements are not met, pop noise might occur.

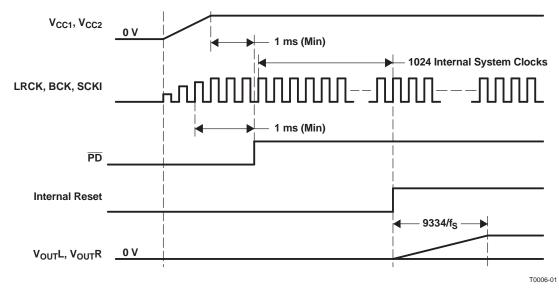


Figure 19. Power-On Sequence

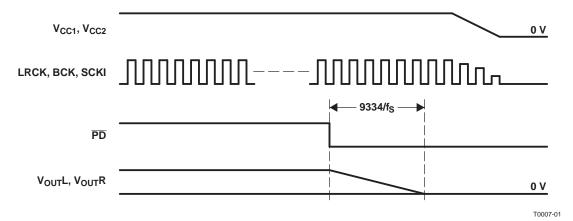


Figure 20. Power-Off Sequence



Power-Up/-Down Sequence and Reset

The PCM1772 device has two kinds of power-up/-down methods: the \overline{PD} terminal through hardware control and PWRD (register 4, B0) through software control. The PCM1773 device has only the \overline{PD} terminal through hardware control for the power-up/-down sequence. The power-up or power-down sequence operates the same as the power-on or power-off sequence. When powering up or down using the \overline{PD} terminal, all digital circuits are reset. When powering up or down using PWRD, all digital circuits are reset except for maintaining the logic states of the registers. Figure 21 shows the power-up/power-down sequence.

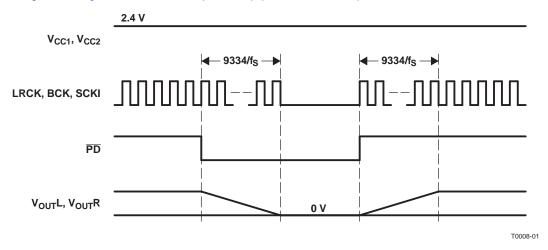


Figure 21. Power-Down and Power-Up Sequences



Audio Serial Interface

The audio serial interface for the PCM1772 and PCM1773 devices consists of a 3-wire synchronous serial port. It includes terminals 1 (LRCK), 2 (DATA), and 3 (BCK). BCK is the serial audio bit clock, and it clocks the serial data present on DATA into the audio interface serial shift register. Serial data is clocked into the PCM1772 and PCM1773 devices on the rising edge of BCK. LRCK is the serial audio left/right word clock. It latches serial data into the serial audio interface internal registers.

Both LRCK and BCK of the PCM1772 device support the slave and master modes, which are set by FMT (register 3). LRCK and BCK are outputs during the master mode and inputs during the slave mode.

In slave mode, BCK and LRCK are synchronous to the audio system clock, SCKI. Ideally, it is recommended that LRCK and BCK be derived from SCKI. LRCK is operated at the sampling frequency, f_S. BCK can be operated at 32, 48, and 64 times the sampling frequency.

In master mode, BCK and LRCK are derived from the system clock, and these terminals are outputs. The BCK and LRCK are synchronous to SCKI. LRCK is operated at the sampling frequency, f_S. BCK can be operated at 64 times the sampling frequency.

The PCM1772 and PCM1773 devices operate under LRCK, synchronized with the system clock. The PCM1772 and PCM1773 devices do not need a specific phase relationship between LRCK and the system clock, but do require the synchronization of LRCK and the system clock. If the relationship between the system clock and LRCK changes more than ±3 BCK during one sample period, internal operation of the PCM1772 and PCM1773 devices halts within 1/f_S, and the analog output is kept in last data until resynchronization between system clock and LRCK is completed.

Audio Data Formats and Timing

The PCM1772 device supports industry-standard audio data formats, including standard, I²S, and left justified. The PCM1773 device supports the I²S and left-justified data formats. Table 2 lists the main features of the audio data interface. Figure 22 shows the data formats. Data formats are selected using the format bits, FMT[2:0] of control register 3 in case of the PCM1772 device, and are selected using the FMT terminal in case of the PCM1773 device. The default data format is 24-bit, left-justified, slave mode. All formats require binary 2s complement, MSB-first audio data. Figure 23 shows a detailed timing diagram for the serial audio interface in slave mode. Figure 24 shows a detailed timing diagram for the serial audio interface in master mode.

Table 2. Audio Data Interface

| AUDIO-DATA INTERFA | CHARACTERISTIC | |
|-----------------------------|--------------------------|--|
| Audia data interfera farmat | PCM1772 | Standard, I ² S, left-justified |
| Audio data interface format | PCM1773 | I ² S, left-justified |
| Audio data bit length | · | 16-, 20-, 24-bit, selectable |
| Audio data format | MSB first, 2s complement | |



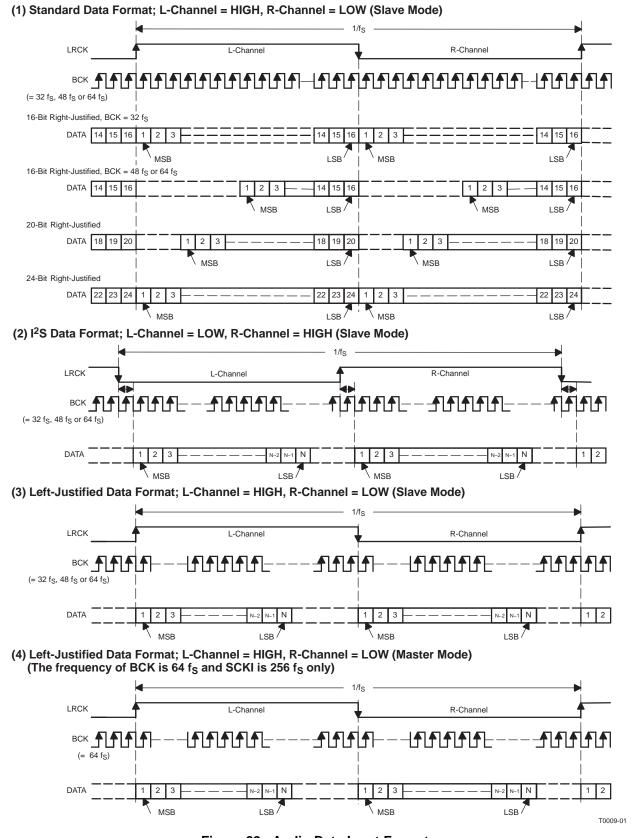
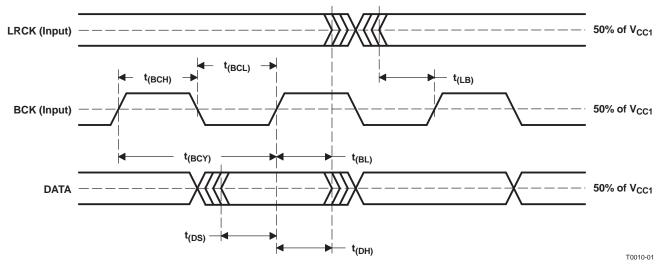


Figure 22. Audio Data Input Formats



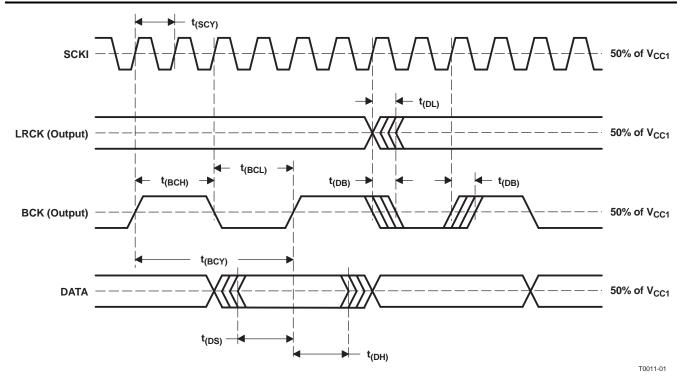


| PARAMETERS | SYMBOL | MIN | MAX | UNIT |
|------------------------------|--------------------|---------------------------------------|-----|------|
| BCK pulse cycle time | t _(BCY) | 1/(64 f _S) ⁽¹⁾ | | |
| BCK high-level time | t _(BCH) | 35 | | ns |
| BCK low-level time | t _(BCL) | 35 | | ns |
| BCK rising edge to LRCK edge | t _(BL) | 10 | | ns |
| LRCK edge to BCK rising edge | t _(LB) | 10 | | ns |
| DATA setup time | t _(DS) | 10 | | ns |
| DATA hold time | t _(DH) | 10 | | ns |

⁽¹⁾ f_S is the sampling frequency.

Figure 23. Audio Interface Timing (Slave Mode)





| PARAMETERS | SYMBOL | MIN | MAX | UNIT |
|---------------------------------|--------------------|--|-----|------|
| SCKI pulse cycle time | t _(SCY) | 1/(256 f _S) ⁽¹⁾ | | |
| LRCK edge from SCKI rising edge | t _(DL) | 0 | 40 | ns |
| BCK edge from SCKI rising edge | t _(DB) | 0 | 40 | ns |
| BCK pulse cycle time | t _(BCY) | 1/(64 f _S) ⁽¹⁾ | | |
| BCK high-level time | t _(BCH) | 146 | | ns |
| BCK low-level time | t _(BCL) | 146 | | ns |
| DATA setup time | t _(DS) | 10 | | ns |
| DATA hold time | t _(DH) | 10 | | ns |

⁽¹⁾ f_S is up to 48 kHz. f_S is the sampling frequency.

Figure 24. Audio Interface Timing (Master Mode)



Hardware Control (PCM1773)

The digital functions of the PCM1773 device are capable of hardware control. Table 3 shows selectable formats, Table 4 shows de-emphasis control, and Table 5 shows analog mixing control.

Table 3. Data Format Select

| FMT | DATA FORMAT |
|------|--|
| Low | 16- to 24-bit, left-justified format |
| High | 16- to 24-bit, I ² S format |

Table 4. De-Emphasis Control

| DEMP | DE-EMPHASIS FUNCTION | | | | | | | |
|------|--------------------------|--|--|--|--|--|--|--|
| Low | 44.1-kHz de-emphasis OFF | | | | | | | |
| High | 44.1-kHz de-emphasis ON | | | | | | | |

Table 5. Analog Mixing Control

| AMIX | ANALOG MIXING | | | | | | | |
|------|-------------------|--|--|--|--|--|--|--|
| Low | Analog mixing OFF | | | | | | | |
| High | Analog mixing ON | | | | | | | |



Software Control (PCM1772)

The PCM1772 device has many programmable functions that can be controlled in the software control mode. The functions are controlled by programming the internal registers using MS, MC, and MD.

The software control interface is a 3-wire serial port that operates asynchronously to the serial audio interface. The serial control interface is used to program the on-chip mode registers. MD is the serial data input, used to program the mode registers. MC is the serial bit clock, used to shift data into the control port. MS is the mode control port select signal.

Register Write Operation (PCM1772)

All write operations for the serial control port use 16-bit data words. Figure 25 shows the control data word format. The most significant bit must be 0. Seven bits, labeled IDX[6:0], set the register index (or address) for the write operation. The eight least significant bits, D[7:0], contain the data to be written to the register specified by IDX[6:0].

Figure 26 shows the functional timing diagram for writing to the serial control port. To write data into the mode register, data is clocked into an internal shift register on the rising edge of the MC clock. Serial data can change on the falling edge of the MC clock and must be stable on the rising edge of the MC clock. The $\overline{\text{MS}}$ signal must be low during the write mode, and the rising edge of the $\overline{\text{MS}}$ signal must be aligned with the falling edge of the last MC clock pulse in the 16-bit frame. The MC clock can run continuously between transactions while the $\overline{\text{MS}}$ signal is low.

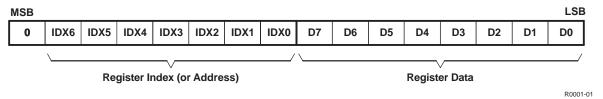


Figure 25. Control Data Word Format for MD

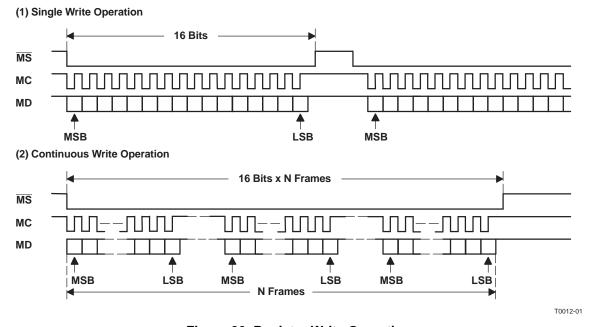
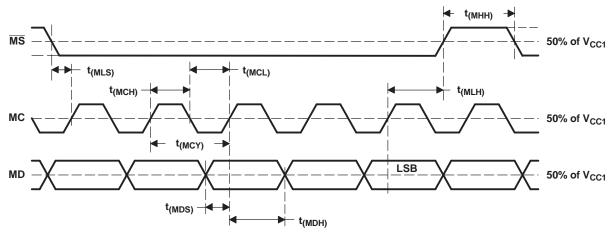


Figure 26. Register Write Operation



Control Interface Timing Requirements (PCM1772)

Figure 27 shows a detailed timing diagram for the serial control interface. These timing parameters are critical for proper control port operation.



T0013-01

| PARAMETERS | SYMBOL | MIN | TYP | MAX | UNIT |
|-----------------------------------|--------------------|--------|-----|-----|------|
| MC pulse cycle time | t _(MCY) | 100(1) | | | ns |
| MC low-level time | t _(MCL) | 50 | | | ns |
| MC high-level time | t _(MCH) | 50 | | | ns |
| MS high-level time | t _(MHH) | (2) | | | ns |
| MS falling edge to MC rising edge | t _(MLS) | 20 | | | ns |
| MS hold time | t _(MLH) | 20 | | | ns |
| MD hold time | t _(MDH) | 15 | | | ns |
| MD setup time | t _(MDS) | 20 | | | ns |

⁽¹⁾ When MC runs continuously between transactions, MC pulse cycle time is specified as $3/(128 f_S)$, where f_S is the sampling rate.

Figure 27. Control Interface Timing

⁽²⁾ $3/(128f_S)$ s (minimum), where f_S is sampling rate



Mode Control Registers (PCM1772)

User-Programmable Mode Controls

The PCM1772 device has a number of user-programmable functions that can be accessed via mode control registers. The registers are programmed using the serial control interface, as discussed in the *Software Control (PCM1772)* section. Table 6 lists the available mode control functions, along with their reset default conditions and associated register index.

Register Map

Table 7 shows the mode control register map. Each register includes an index (or address) indicated by the IDX[6:0] bits.

Table 6. User-Programmable Mode Controls

| FUNCTION | RESET DEFAULT | REGISTER NO. | BIT(S) |
|--|---------------------------------|--------------|--------------------|
| Soft mute control, L/R independently | Disabled | 01 | MUTL, MUTR |
| Digital attenuation level setting, 0 dB to -62 dB in 1-dB steps, L/R independently | 0 dB | 01, 02 | ATL[5:0], ATR[5:0] |
| Oversampling rate control (128 f _S , 192 f _S , 256 f _S , 384 f _S) | 128 f _S oversampling | 03 | OVER |
| Polarity control for analog output for R-channel DAC | Not inverted | 03 | RINV |
| Analog mixing control for analog in, AIN (terminal 14) | Disabled | 03 | AMIX |
| 44.1-kHz de-emphasis control | Disabled | 03 | DEM |
| Audio data format select | 24-bit, left-justified format | 03 | FMT[2:0] |
| Zero cross attenuation | Disabled | 04 | ZCAT |
| Power-down control | Disabled | 04 | PWRD |

Table 7. Mode Control Register Map

| Register | IDX [6:0] (B14- B8) | B15 | B14 | B13 | B12 | B11 | B10 | В9 | B8 | В7 | В6 | B5 | В4 | В3 | B2 | B1 | В0 |
|-------------|------------------------------|-----|------|------|------|------|------|------|------|--------------------|--------------------|--------------------|------|--------------------|--------------------|--------------------|------|
| Register 01 | 01h | 0 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | MUTR | MUTL | ATL5 | ATL4 | ATL3 | ATL2 | ATL1 | ATL0 |
| Register 02 | 02h | 0 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | RSV ⁽¹⁾ | RSV ⁽¹⁾ | ATR5 | ATR4 | ATR3 | ATR2 | ATR1 | ATR0 |
| Register 03 | 03h | 0 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | OVER | RSV ⁽¹⁾ | RINV | AMIX | DEM | FMT2 | FMT1 | FMT0 |
| Register 04 | 04h | 0 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | RSV ⁽¹⁾ | RSV ⁽¹⁾ | RSV ⁽¹⁾ | ZCAT | RSV ⁽¹⁾ | RSV ⁽¹⁾ | RSV ⁽¹⁾ | PWRD |

⁽¹⁾ RSV: Reserved for test operation. It must be set to 0 during regular operation.



Register Definitions

Register 01

| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | В6 | B5 | B4 | B 3 | B2 | B1 | B0 |
|-----|------|------|------|------|------|------|------|------|------|------|------|------------|------|------|------|
| 0 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | MUTR | MUTL | ATL5 | ATL4 | ATL3 | ATL2 | ATL1 | ATL0 |

IDX[6:0]: 000 0001b

MUTx: Soft Mute Control

Where, x = L or R, corresponding to the line output $V_{OUT}L$ or $V_{OUT}R$.

Default Value: 0

| MUTL, MUTR = 0 | Mute disabled (default) |
|----------------|-------------------------|
| MUTL, MUTR = 1 | Mute enabled |

The mute bits, MUTL and MUTR, enable or disable the soft mute function for the corresponding line outputs, $V_{OUT}L$ and $V_{OUT}R$. The soft mute function is incorporated into the digital attenuators. When mute is disabled (MUTx = 0), the attenuator and DAC operate normally. When mute is enabled by setting MUTx = 1, the digital attenuator for the corresponding output is decreased from the current setting to infinite attenuation, one attenuator step (1 dB) at a time. This provides pop-free muting of the line output.

By setting MUTx = 0, the attenuator is increased one step at a time to the previously programmed attenuation level.

ATL[5:0]: Digital Attenuation Level Setting for Line Output, Vout

Default value: 11 1111b

Line output, $V_{OUT}L$, includes a digital attenuation function. The attenuation level can be set from 0 dB to -62 dB, in 1-dB steps. Changes in attenuator levels are made by incrementing or decrementing by one step (1 dB) for every $8/f_S$ time internal until the programmed attenuator setting is reached. Alternatively, the attenuation level can be set to infinite attenuation (or mute).

The following table shows attenuation levels for various settings:

| ATL[5:0] | ATTENUATION LEVEL SETTING |
|----------|--------------------------------|
| 11 1111b | 0 dB, no attenuation (default) |
| 11 1110b | -1 dB |
| 11 1101b | -2 dB |
| : | : |
| 00 0010b | -61 dB |
| 00 0001b | −62 dB |
| 00 0000b | Mute |

Register 02

| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B 3 | B2 | B1 | B0 |
|-----|------|------|------|------|------|------|------|-----|-----|------|------|------------|------|------|------|
| 0 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | RSV | RSV | ATR5 | ATR4 | ATR3 | ATR2 | ATR1 | ATR0 |

IDX[6:0]: 000 0010b

ATR[5:0]: Digital Attenuation Level Setting for Line Output, Vout

Default Value: 11 1111b

Line output, $V_{OUT}R$, includes a digital attenuation function. The attenuation level can be set from 0 dB to -62 dB, in 1-dB steps. Changes in attenuator levels are made by incrementing or decrementing by one step (1 dB) for every $8/f_S$ time internal until the programmed attenuator setting is reached. Alternatively, the attenuation level can be set to infinite attenuation (or mute).

To set the attenuation levels for ATR[5:0], see the table for ATL[5:0], register 01.



Register 03

| ı | B15 | B14 | B13 | B12 | B11 | B10 | В9 | B8 | B7 | В6 | B5 | B4 | В3 | B2 | B1 | B0 |
|---|-----|------|------|------|------|------|------|------|------|-----|------|------|-----|------|------|------|
| | 0 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | OVER | RSV | RINV | AMIX | DEM | FMT2 | FMT1 | FMT0 |

IDX[6:0]: 000 0011b

OVER: Oversampling Control

Default Value: 0

| OVER = 0 | 128f _S oversampling |
|----------|--|
| OVER = 1 | 192f _S , 256f _S , 384f _S oversampling |

The OVER bit controls the oversampling rate of the Δ - Σ D/A converters. When it operates at a low sampling rate, less than 24 kHz, this function is recommended.

RINV: Polarity Control for Line Output, V_{OUT}R

Default Value: 0

| RINV = 0 | Not inverted |
|----------|-----------------|
| RINV = 1 | Inverted output |

The RINV bits allow the user to control the polarity of the line output, V_{OUT}R. This function can be used to connect the monaural speaker with BTL connection method. This bit is recommended to be 0 during the power-up/-down sequence for minimizing audible pop noise.

AMIX: Analog Mixing Control for External Analog Signal, AIN

Default Value: 0

| AMIX = 0 | Disabled (not mixed) |
|----------|------------------------------------|
| AMIX = 1 | Enabled (mixing to the DAC output) |

AMIX bit allows the user to mix analog input (AIN) with line outputs (V_{OUT}L/V_{OUT}R) internally.

DEM: 44.1-kHz De-Emphasis Control

Default Value: 0

| DEM = 0 | Disabled |
|---------|----------|
| DEM = 1 | Enabled |

The DEM bit enables or disables the digital de-emphasis filter for 44.1-kHz sampling rate.

FMT[2:0]: Audio Interface Data Format

Default Value: 000

The FMT[2:0] bits select the data format for the serial audio interface. The following table shows the available format options.

| FMT[2:0] | Audio Data Format Selection |
|----------|---|
| 000 | 16- to 24-bit, left-justified format (default) |
| 001 | 16- to 24-bit, I ² S format |
| 010 | 24-bit right-justified data |
| 011 | 20-bit right-justified data |
| 100 | 16-bit right-justified data |
| 101 | 16- to 24-bit, left-justified format, master mode |
| 110 | Reserved |
| 111 | Reserved |



Register 04

| B15 | B14 | B13 | B12 | B11 | B10 | В9 | B8 | B7 | В6 | B5 | B4 | В3 | B2 | B1 | В0 | |
|-----|------|------|------|------|------|------|------|-----|-----|-----|------|-----|-----|-----|------|--|
| 0 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | RSV | RSV | RSV | ZCAT | RSV | RSV | RSV | PWRD | |

IDX[6:0]: 000 0100b

ZCAT: Zero Cross Attenuation

Default Value: 0

| ZCAT = 0 | Normal attenuation (default) |
|----------|------------------------------|
| ZCAT = 1 | Zero cross attenuation |

This bit enables changing the signal level on zero crossing during attenuation control or muting. If the signal does not cross BPZ beyond $512/f_S$ (11.6 ms at the 44.1-kHz sampling rate), the signal level is changed similarly to normal attenuation control. This function is independently monitored for each channel; moreover, change of signal level is alternated between both channels. Figure 28 shows an example of zero cross attenuation.

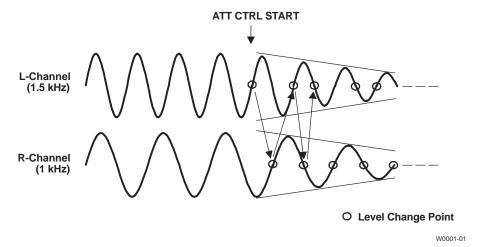


Figure 28. Example of Zero Cross Attenuation

PWRD: Power Down Control

Default Value: 0

| PWRD = 0 | Normal operation (default) |
|----------|----------------------------|
| PWRD = 1 | Power-down state |

This bit is used to enter into low-power mode. Note that PWRD has no reset function.

When this bit is set to 1, the PCM1772 device enters low-power mode, and all digital circuits are reset except the register states, which remain unchanged.



Analog In/Out

Line Output (Stereo)

The PCM1772 and PCM1773 devices have two independent lineout amplifiers, and each amplifier output is provided at the corresponding $V_{OUT}L$ or $V_{OUT}R$ terminal. The capability of line output is designed for driving a 10-k Ω minimum load.

Monaural Output (BTL Mode/Monaural Speaker)

When the user needs monaural output, the PCM1772 device can provide it. The PCM1772 device has RINV bit on control register 03. Because this bit allows the user to invert the polarity of the line output for the right channel, the user can create a monaural output by summing the line output for left and right channels through the external power amplifier or headphone amplifier. The RINV bit is recommended to be 0 during power-up/-down sequence for minimizing audible pop noise.

Analog Input

The PCM1772 and PCM1773 devices have an analog input, AIN (terminal 10). The AMIX bit (PCM1772) or the AMIX terminal (PCM1773) allows the user to mix AIN with the line outputs ($V_{OUT}L$ and $V_{OUT}R$) internally. When in MIXING mode, an ac-coupling capacitor is needed for AIN. But if AIN is not used, AIN must be open and the AMIX bit (PCM1772) must be disabled or the AMIX terminal (PCM1773) must be low.

Because AIN does not have an internal low-pass filter, it is recommended that the bandwidth of the input signal into AIN is limited to less than 100 kHz. The source of signals connected to AIN must be connected by low impedance.

Although the maximum input voltage on AIN is designed to be as large as 0.584 V_{CC2} [peak-to-peak], the user must attenuate the input voltage on AIN and control the digital input data so that each line output ($V_{OUT}L$ and $V_{OUT}R$) does not exceed 0.75 V_{CC2} [peak-to-peak] during mixing mode.

V_{COM} Output

One unbuffered common-mode voltage output terminal, V_{COM} , is brought out for decoupling purposes. This terminal is nominally biased to a dc voltage level equal to 0.5 V_{CC2} and connected to a 10- μ F capacitor. In the case of a capacitor smaller than 10 μ F, pop noise can be generated during the power-on/-off or power-up/-down sequences.



APPLICATION INFORMATION

Connection Diagrams

Figure 29 shows the basic connection diagram with the necessary power supply bypassing and decoupling components. It is recommended that the component values shown in Figure 29 be used for all designs.

The use of series resistors (22 Ω to 100 Ω) is recommended for the SCKI, LRCK, BCK, and DATA inputs. The series resistor combines with the stray PCB and device input capacitance to form a low-pass filter that reduces high-frequency noise emissions and helps to dampen glitches and ringing present on the clock and data lines.

Power Supplies and Grounding

The PCM1772 and PCM1773 devices require a 2.4-V typical analog supply for V_{CC1} and V_{CC2} . These 2.4-V supplies power the DAC, analog output filter, and other circuits. For best performance, these 2.4-V supplies must be derived from the analog supply using a linear regulator, as shown in Figure 29.

Figure 29 shows the proper power supply bypassing. The $10-\mu\text{F}$ capacitors must be tantalum or aluminum electrolytic, while the $0.1-\mu\text{F}$ capacitors are ceramic (X7R type is recommended for surface-mount applications).

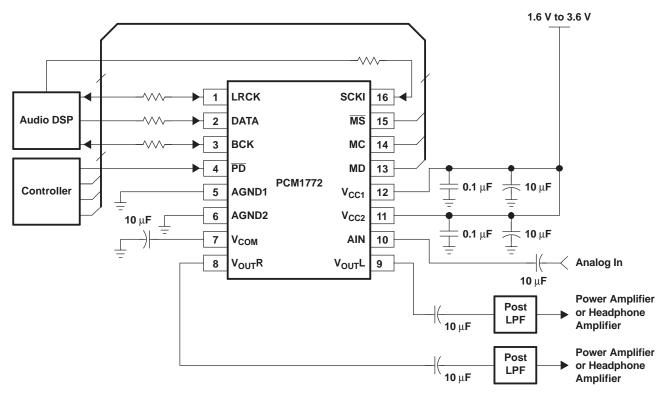


Figure 29. Basic Connection Diagram

S0007-01



Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from F Revision (November 2005) to G Revision | Page |
|--|------------------|
| Changed signal name from MCKI to SCKI | 28 |
| Corrected errors, added recommended parts, and changed incorrect symbols | 28 |
| Changes from E Revision (April 2005) to F Revision | Page |
| Changed dynamic performance for full-scale output voltage of line output from 0.75 Vcc2 | 2 to 0.77 Vcc2 3 |
| Changes from D Revision (May 2004) to E Revision | Page |
| Changed data sheet to new format | |
| Changed value for power-supply voltage | 2 |
| • Removed package/ordering information, reformatted, and appended at end of data sheet | t 2 |
| Added new Recommended Operating Conditions table to data sheet | 2 |
| Changed page layout for terminal function tables | 5 |
| Changed page layout of Figure 13 and Figure 14 | |
| • In Figure 22, added arrows to all rising edges of BCK for data formats (2), (3), and (4) | 17 |
| In Figure 29, changed signal direction on SCKI pin | |

PACKAGE OPTION ADDENDUM

www.ti.com 3-Aug-2009

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | e Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|-----------------|--------------------|------|----------------|---------------------------|------------------|------------------------------|
| PCM1772PW | ACTIVE | TSSOP | PW | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| PCM1772PWG4 | ACTIVE | TSSOP | PW | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| PCM1772PWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| PCM1772PWRG4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| PCM1772RGA | ACTIVE | VQFN | RGA | 20 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| PCM1772RGAG4 | ACTIVE | VQFN | RGA | 20 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| PCM1772RGAR | ACTIVE | VQFN | RGA | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| PCM1772RGARG4 | ACTIVE | VQFN | RGA | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| PCM1773PW | ACTIVE | TSSOP | PW | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| PCM1773PWG4 | ACTIVE | TSSOP | PW | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| PCM1773PWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| PCM1773PWRG4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| PCM1773RGA | ACTIVE | VQFN | RGA | 20 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| PCM1773RGAG4 | ACTIVE | VQFN | RGA | 20 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| PCM1773RGAR | ACTIVE | VQFN | RGA | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| PCM1773RGARG4 | ACTIVE | VQFN | RGA | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.



PACKAGE OPTION ADDENDUM

www.ti.com 3-Aug-2009

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

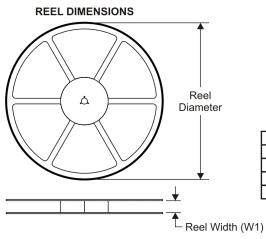
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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





| | Dimension designed to accommodate the component width |
|----|---|
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| All difficults are norminal | | | | | | | | | | | | |
|-----------------------------|-----------------|--------------------|----|------|--------------------------|--------------------------|------------|------------|------------|------------|-----------|------------------|
| Device | Package Type | Package Drawing | | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
| PCM1772PWR | TSSOP | PW | 16 | 2000 | 330.0 | 17.4 | 6.8 | 5.4 | 1.6 | 8.0 | 16.0 | Q1 |
| PCM1772RGAR | VQFN | RGA | 20 | 2000 | 330.0 | 13.4 | 4.4 | 4.4 | 1.3 | 8.0 | 12.0 | Q1 |
| PCM1773PWR | TSSOP | PW | 16 | 2000 | 330.0 | 17.4 | 6.8 | 5.4 | 1.6 | 8.0 | 16.0 | Q1 |
| PCM1773RGAR | VQFN | RGA | 20 | 2000 | 330.0 | 13.4 | 4.4 | 4.4 | 1.3 | 8.0 | 12.0 | Q1 |

www.ti.com 31-Jul-2009



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| PCM1772PWR | TSSOP | PW | 16 | 2000 | 346.0 | 346.0 | 33.0 |
| PCM1772RGAR | VQFN | RGA | 20 | 2000 | 346.0 | 346.0 | 29.0 |
| PCM1773PWR | TSSOP | PW | 16 | 2000 | 346.0 | 346.0 | 33.0 |
| PCM1773RGAR | VQFN | RGA | 20 | 2000 | 346.0 | 346.0 | 29.0 |

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



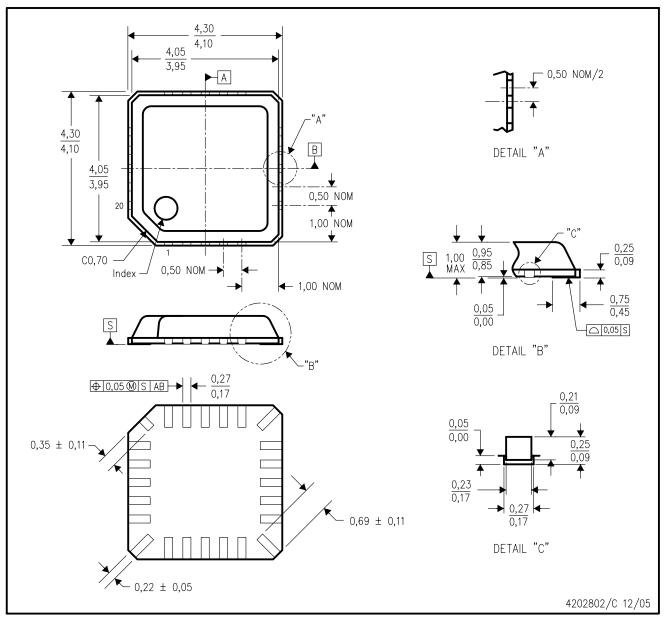
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



RGA (S-PQFP-N20)

PLASTIC QUAD FLATPACK



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. These dimensions include package bend.
- D. Falls within EIAJ: EDR-7324.



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