



STEREO DIGITAL AUDIO LIP-SYNC DELAY

FEATURES

- Digital Audio Format: 16-24-bit I²S
- Single Serial Input Port
- Delay Time: 170 ms/ch at fs = 48 kHz
- Delay Resolution: 256 samples
- Delay Memory Cleared on Power-Up or After Delay Changes
 - Eliminates Erroneous Data From Being Output
- 3.3 V Operation With 5 V Tolerant I/O
- Supports Audio Bit Clock Rates of 32 to 64 fs with fs = 32 kHz-192 kHz
- No External Crystal or Oscillator Required
 - All Internal Clocks Generated From the Audio Clock
- Surface Mount 4mm × 4mm, 16-pin QFN Package

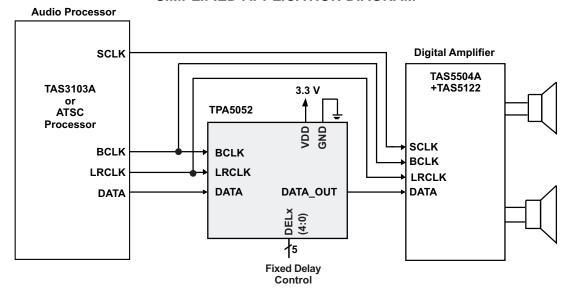
APPLICATIONS

- High Definition TV Lip-Sync Delay
- Flat Panel TV Lip-Sync Delay
- Home Theater Rear-Channel Effects
- Wireless Speaker Front-Channel Synchronization
- Camcorders

DESCRIPTION

The TPA5052 accepts a single serial audio input, buffers the data for a selectable period of time, and outputs the delayed audio data on a single serial output. In systems with complex video processing algorithms, one device allows delay of up to 170 ms/ch (fs = 48 kHz) to synchronize the audio stream to the video stream. If more delay is needed, the devices can be connected in series.

SIMPLIFIED APPLICATION DIAGRAM





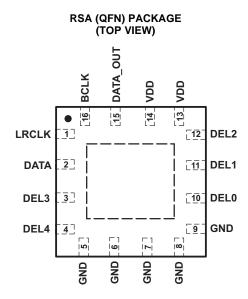
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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PIN DESCRIPTIONS

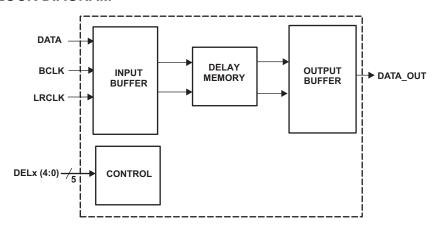


TERMINAL FUNCTIONS

TERMINAL I/O			DECODIDATION
NAME	NO.	1/0	DESCRIPTION
DEL0	10	I	Delay select pin – LSB. 5V tolerant input.
DEL1	11	I	Delay select pin. 5V tolerant input.
DEL2	12	I	Delay select pin. 5V tolerant input.
DEL3	3	1	Delay select pin. 5V tolerant input.
DEL4	4	1	Delay select pin - MSB. 5V tolerant input.
BCLK	16	I	Audio data bit clock input for serial input. 5V tolerant input.
DATA	2	I	Audio serial data input for serial input. 5V tolerant input.
DATA_OUT	15	0	Delayed audio serial data output.
GND	5–9	Р	Ground – All ground terminals must be tied to GND for proper operation
LRCLK	1	1	Left and Right serial audio sampling rate clock (fs). 5V tolerant input.
VDD	13, 14	Р	Power supply interface. Both pins must be tied to power supply.
Thermal Pad		-	Connect to ground. Must be soldered down in all applications to properly secure device on the PCB.



FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature (unless otherwise noted) (1)

			VALUE	UNIT
V_{DD}	Supply voltage		-0.3 to 3.6	V
V_{I}	Input voltage	DATA, LRCLK, BCLK, DEL[4:0]	-0.3 to 5.5	V
	Continuous total	power dissipation	See Dissipation Rating Table	
T _A	Operating free-a	ir temperature range	-40 to 85	°C
T_{J}	Operating junction	on temperature range	-40 to 125	°C
T _{stg}	Storage tempera	ture range	-65 to 125	°C
	Lead temperatur	e 1,6 mm (1/16 inch) from case for 10 seconds	260	°C

⁽¹⁾ Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operations of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS(1)

PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING
RSA	2.5 W	25 mW/°C	1.375 W	1 W

⁽¹⁾ This data was taken using 1 oz trace and copper pad that is soldered directly to a JEDEC standard high-k PCB. The thermal pad must be soldered to a thermal land on the printed-circuit board. See TI Technical Briefs SCBA017D and SLUA271 for more information about using the QFN thermal pad.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{DD}	Supply voltage	VDD	3	3.6	V
V_{IH}	High-level input voltage	DATA, LRCLK, BCLK, DEL[4:0]	2		V
V_{IL}	Low-level input voltage	DATA, LRCLK, BCLK, DEL[4:0]		0.8	V
T_A	Operating free-air tempera	ture	-40	85	°C



DC CHARACTERISTICS

 $T_A = 25^{\circ}C$, $V_{DD} = 3 \text{ V}$ (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{DD}	Supply current	V_{DD} = 3.3 V, fs = 48 kHz, BCLK = 32 × fs		1.8	3	mA
I _{OH}	High-level output current	DATA_OUT = 2.6 V	5		13	mA
I _{OL}	Low-level output current	DATA_OUT = 0.4 V	5		13	mA
	High lovel input ourrest	DATA, LRCLK, BCLK, V _I = 5.5V, VDD = 3V			20	^
IH	High-level input current	DEL[4:0], V _I = 3.6V, VDD = 3.6V			5	μΑ
I _{IL}	Low-level input current	DATA, LRCLK, BCLK, DEL[4:0], V _I = 0V, VDD = 3.6V			1	μΑ

Serial Audio Input Ports

over recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{SCLKIN}	Frequency, BCLK $32 \times fs$, $48 \times fs$, $64 \times fs$		1.024		12.288	MHz
t _{su1}	Setup time, LRCLK to BCLK rising edge		10			ns
t _{h1}	Hold time, LRCLK from BCLK rising edge		10			ns
t _{su2}	Setup time, DATA to BCLK rising edge		10			ns
t _{h2}	Hold time, DATA from BCLK rising edge		10			ns
	LRCLK frequency		32	48	192	kHz
	BCLK duty cycle			50%		
	LRCLK duty cycle			50%		
	BCLK rising edges between LRCLK rising edges	LRCLK duty cycle = 50%	32		64	BCLK edges

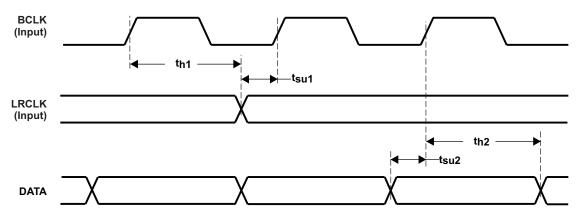


Figure 1. Serial Data Interface Timing



APPLICATION INFORMATION

AUDIO SERIAL INTERFACE

The audio serial interface for the TPA5052 consists of a 3-wire synchronous serial port. It includes LRCLK, BCLK, and DATA. BCLK is the serial audio bit clock, and it is used to clock the serial data present on DATA into the serial shift register of the audio interface. Serial data is clocked into the TPA5052 on the rising edge of BCLK. LRCLK is the serial audio left/right word clock. It is used to latch serial data into the internal registers of the serial audio interface. LRCLK is operated at the sampling frequency, fs. BCLK can be operated at 32 to 64 times the sampling frequency for I²S formats. A system clock is not necessary for the operation of the TPA5052.

I2S TIMING

The I²S data format diagram is shown in Figure 2.

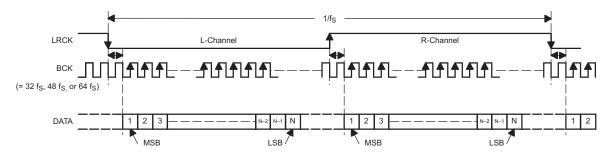


Figure 2. I²S Data Format; L-Channel = LOW, R-Channel = HIGH

GENERAL DELAY OPERATION

The delay of the TPA5052 is set using the 5 delay pins (DEL4, DEL3, DEL2, DEL1, DEL0). The minimum delay is 255 samples, and occurs when all five pins are at logic 0. The maximum delay is 8191 samples, and occurs when all five pins are at logic 1. The delay can be increased by changing the values on each pin from a 0 to a 1. See Table 1. Delay pin DEL4 is the MSB, and DEL0 is the LSB.

The delay is calculated with the following forumula:

Audio Delay (in samples) = $4096 \times (DEL4) + 2048 \times (DEL3) + 1024 \times (DEL2) + 512 \times (DEL1) + 256 \times (DEL0) + 255$

Audio Delay (ms) = Audio Delay (in samples) x (1/fs)

Both channels have the same amount of delay. They cannot be controlled individually.

DEL4	DEL3	DEL2	DEL1	DEL0	Delay in Samples
0	0	0	0	0	255
0	0	0	0	1	511
0	0	0	1	0	767
0	0	0	1	1	1023
\	\	\	\	\	\
1	1	1	1	1	8191

Table 1. Delay Settings



TPA5052 Operation

Only a single decoupling capacitor (0.1 μ F–1 μ F) is required across VDD and GND. The DELx terminals can be directly connected to VDD or GND. Table 1 describes the delay settings selectable via the DELx terminals. A schematic implementation of the TPA5052 is shown in Figure 3.

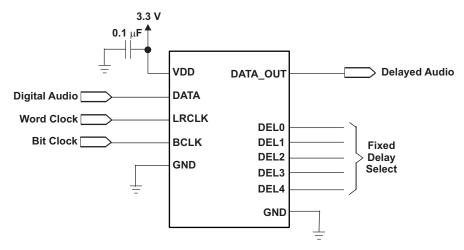


Figure 3. TPA5052 Schematic

COMPLETE UPDATE

To avoid pops and clicks in the audio stream when the delay is changed, the TPA5052 holds each channel in an internal mute mode until all the set number of samples have passed. For example, if the delay is set to 511 samples, the TPA5052 holds each channel in mute until all 511 samples of audio data have passed.



APPLICATION EXAMPLES

Connecting Two Devices in Series to Increase the Delay

It is sometimes desirable to increase the delay time beyond the limit which one device provides. In such cases, the TPA5052 device can be placed in a series to increase the delay. See Figure 4 for an example.

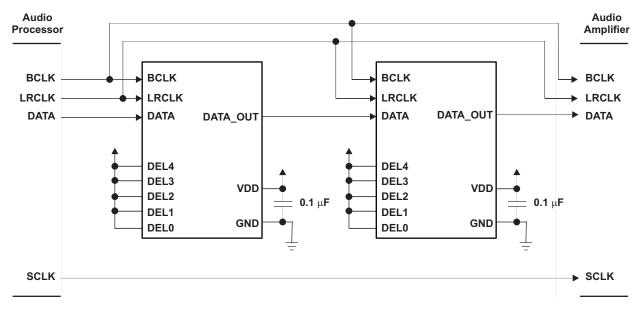
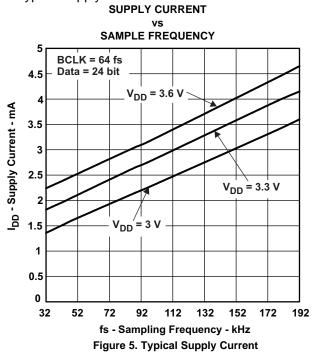


Figure 4. Two Devices in Series

DEVICE CURRENT CONSUMPTION

The TPA5052 draws different amounts of supply current depending upon the conditions under which it is operated. As V_{DD} increases, so too does I_{DD} . Likewise, as V_{DD} decreases, I_{DD} decreases. The same is true of the sampling frequency, fs. An increase in fs causes an increase in I_{DD} . Figure 5 illustrates the relationship between operating condition and typical supply current.







com 6-Dec-2006

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TPA5052RSAR	ACTIVE	QFN	RSA	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPA5052RSARG4	ACTIVE	QFN	RSA	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPA5052RSAT	ACTIVE	QFN	RSA	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPA5052RSATG4	ACTIVE	QFN	RSA	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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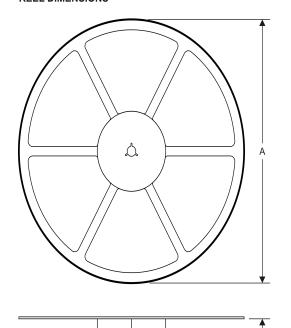
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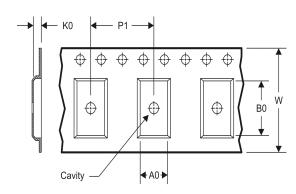
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TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

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Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA5052RSAR	QFN	RSA	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPA5052RSAT	QFN	RSA	16	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

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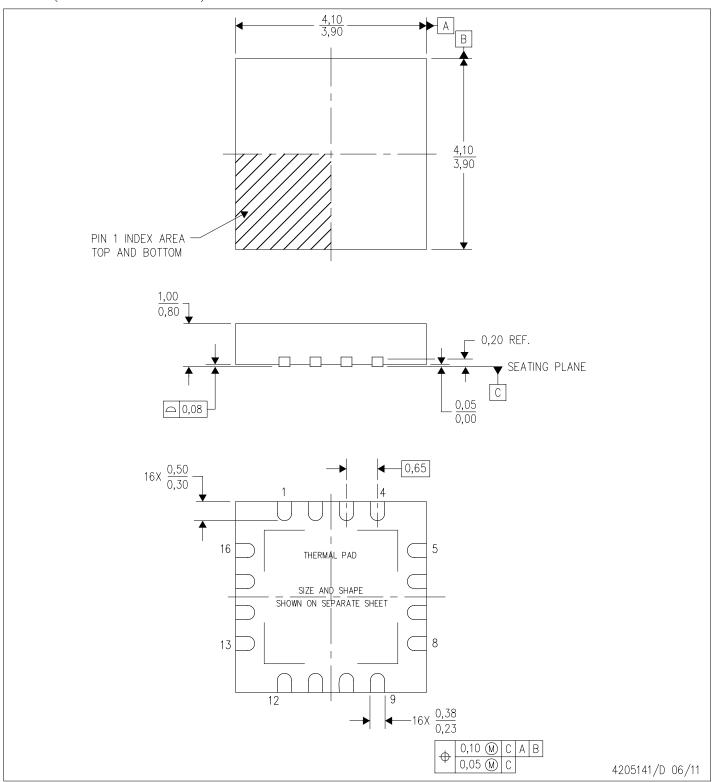


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA5052RSAR	QFN	RSA	16	3000	346.0	346.0	29.0
TPA5052RSAT	QFN	RSA	16	250	210.0	185.0	35.0

RSA (S-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.

- B. This drawing is subject to change without notice.
- C. Quad Flatpack, No—leads (QFN) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO-220.



RSA (S-PVQFN-N16)

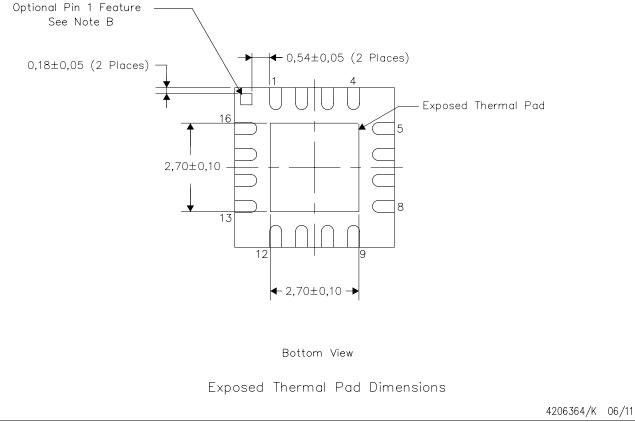
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No—Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



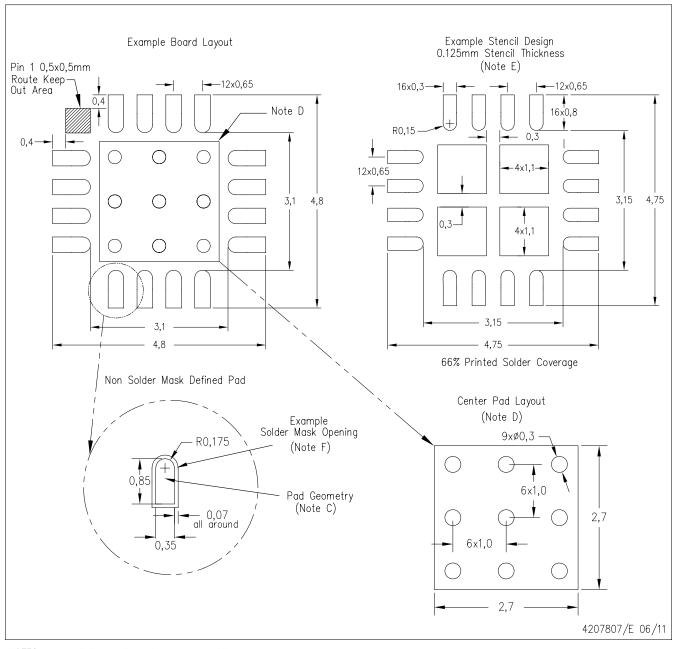
NOTES:

- A. All linear dimensions are in millimeters
- B. The Pin 1 Identification mark is an optional feature that may be present on some devices In addition, this Pin 1 feature if present is electrically connected to the center thermal pad and therefore should be considered when routing the board layout.



RSA (S-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com https://www.ti.com.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for solder mask tolerances.



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