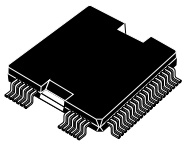
TDA7570

250W PWM high efficiency power audio amplifier

Features

- Output power 2 x 70W / 1 x 250W @ THD<1%
- PWM output
- ±30V supply voltage (Max)
- Stand-by
- Mute
- Protections against short circuit across the load
- Chip thermal protection
- External temperature sensor possibility
- Thermal warning pins
- Adjustable clip detector pin



HiQUAD64

Description

The TDA7570 is a switchmode power audio amplifier with differential inputs and PWM output.

The maximum output current and voltage swing are depending by the output circuitry (power supply, external power transistors and sensing resistors). The device can work as a stereo single-ended channels or a mono bridge power amplifier.

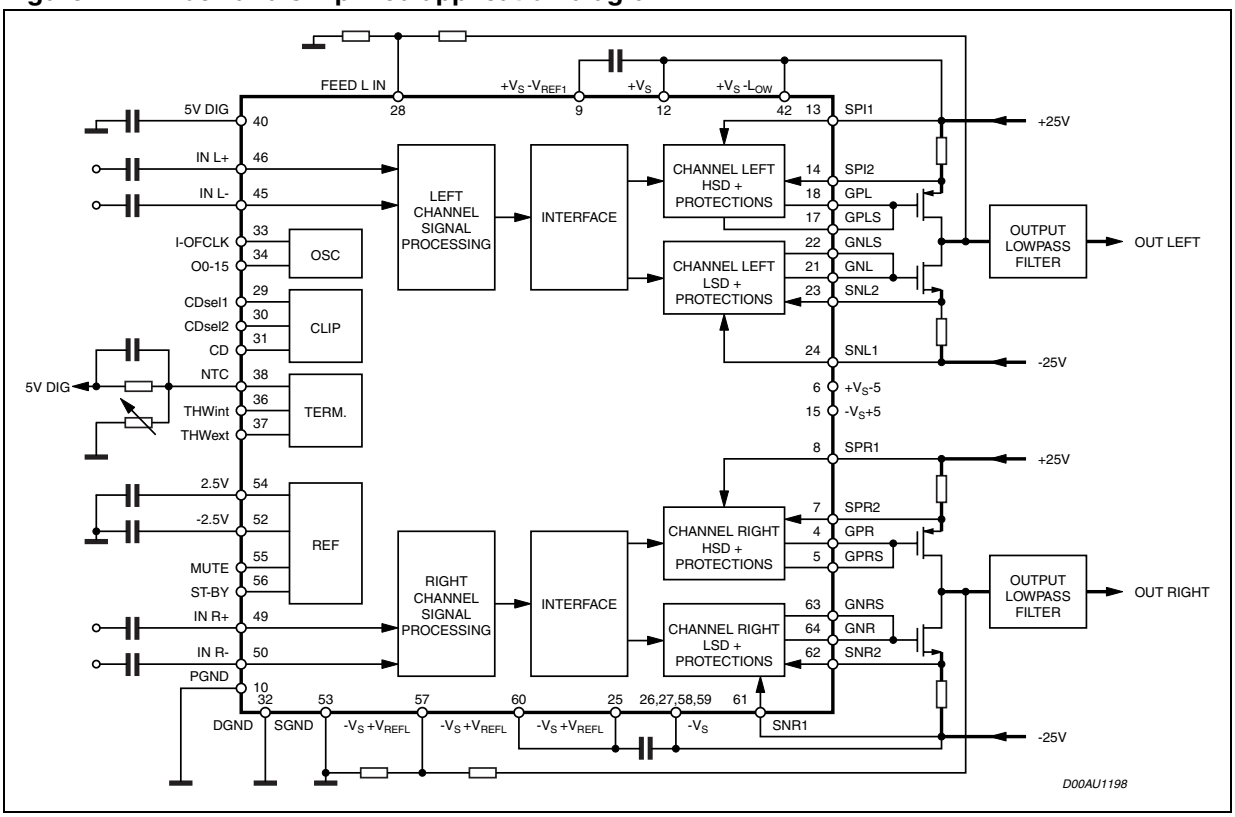
Table 1. Device summary

Order code	Package	Packing
TDA7570	HiQUAD64	Tray

Contents

1 Block and simplified application diagram

Figure 1. Block and simplified application diagram



2 Pin description

Figure 2. Pins connection diagram

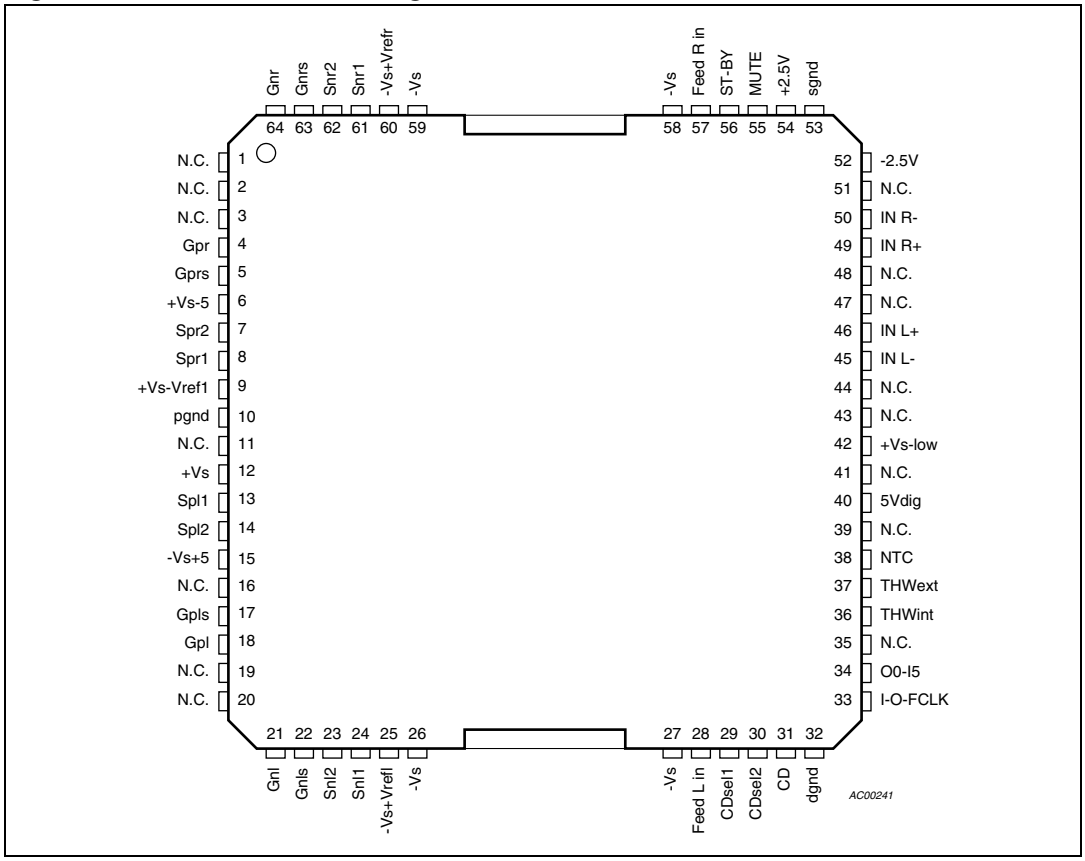


Table 2. Pins description

Pin number	Name	Function	Voltage limit (low)	Voltage limit (high)
1	N.C.	Not connected		
2	N.C.	Not connected		
3	N.C.	Not connected		
4	Gpr	Gate PMOS, right channel	+Vs-12V	30V
5	Gprs	Sense gate PMOS, right channel	+Vs-12V	30V
6	+Vs-5		+Vs-6	
7	Spr2	Sensing 2 PMOS, right channel		30V
8	Spr1	Sensing 1 PMOS, right channel		30V
9	+Vs-Vref1	Supply drivers PMOS	+Vs-12V	30V
10	pgnd	Power ground	0 (ref.)	
11	N.C.	Not connected		

Table 2. Pins description (continued)

Pin number	Name	Function	Voltage limit (low)	Voltage limit (high)
12	+Vs	Positive power supply		30V
13	Spl1	Sensing 1 PMOS, left channel		30V
14	Spl2	Sensing 2 PMOS, left channel		30V
15	-Vs+5			-Vs+6
16	N.C.	Not connected		
17	Gpls	Sense gate PMOS, left channel	+Vs-12V	30V
18	Gpl	Gate PMOS, left channel	+Vs-12V	30V
19	N.C.	Not connected		
20	N.C.	Not connected		
21	Gnl	Gate NMOS, left channel	-30V	-Vs+12V
22	Gnls	Gate NMOS, left channel	-30V	-Vs+12V
23	Snl2	Sensing 2 NMOS, left channel	-30V	
24	Snl1	Sensing 1 NMOS, left Channel	-30V	
25	-Vs+Vrefl	Supply drivers NMOS. left channel	-30V	-Vs+12V
26	-Vs	Negative power supply	-30V	
27	-Vs	Negative power supply	-30V	
28	Feed L in	Feedback network left channel	-5V	5V
29	CDsel1	Clip detector selection 1		5.5V
30	CD sel2	Clip detector selection 2		5.5V
31	CD	Clip detector output		5.5V
32	dgnd	Digital ground	0 (ref)	
33	I-O-FCLK	Clock frequency input/output pin		5.5V
34	O0-I5	Input/output FCLK selection 0 = Output; 1 = Input		5.5V
35	N.C.	Not connected		
36	THWint	Internal thermal warning output		5.5V
37	THWext	External thermal warning output		5.5V
38	NTC	Sensing resistors network		5.5V
39	N.C.	Not connected		
40	5Vdig	Digital 5V supply output		5.5V
41				
42	+Vs-low	Positive voltage supply low power		30V
43	N.C.	Not connected		
44	N.C.	Not connected		

Table 2. Pins description (continued)

Pin number	Name	Function	Voltage limit (low)	Voltage limit (high)
45	IN L-	Left channel negative input	-3V	3V
46	IN L+	Left channel positive input	-3V	3V
47	N.C.	Not connected		
48	N.C.	Not connected		
49	IN R+	Right channel positive input	-3V	3V
50	IN R-	Right channel negative input	-3V	3V
51	N.C.	Not connected		
52	-2.5V	Signal -2.5V supply output	-2.75V	
53	sgnd	Signal ground	0 (ref)	
54	+2.5V	Signal 2.5V supply output		2.75V
55	MUTE	Mute input		5.5V
56	ST-BY	Stand by input		6V
57	Feed R in	Feedback network right channel	-5	5V
58	-Vs	Negative voltage supply	-30V	
59	-Vs	Negative voltage supply	-30V	
60	-Vs+Vrefr	Supply drivers NMOS. Right channel	-30V	-Vs+12V
61	Snr1	Sensing 2 NMOS, right channel	-30V	
62	Snr2	Sensing 1 NMOS, right channel	-30V	
63	Gnrs	Sense gate NMOS, right channel	-30V	-Vs+12V
64	Gnr	Gate NMOS, right channel	-30V	-Vs+12V

3 Electrical specifications

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
$\pm V_s$	Operating supply voltage	±30	V
P_{tot}	Power dissipation T_{case} = 85°C	21	W
T_j	Junction temperature, operating range	-40 to 150	°C
T_{stg}	Storage temperature, operating range	-55 to 150	°C

3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}case}$	Thermal resistance junction to case	3	°C/W

3.3 Electrical characteristics

Table 5. Electrical characteristics

(V_S = ±25V, R_L = 4Ω, f = 100Hz, T_j = 25°C, Gain = 28dB, application circuit shown in *Figure 3*, 2x65/1x130W system, unless otherwise specified.)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$\pm V_S$	Operating supply voltage		±12		±30	V
I_q	Quiescent supply current	$V_{st\text{-}by}$ = 5V, $F_{switching}$ = 352.8kHz				
		from $+V_S$	20	25	35	mA
		from $+V_S$ -low	5.4	7	9	mA
		from $-V_S$	20	25	35	mA
$I_{st\text{-}by}$	Quiescent supply current	$V_{st\text{-}by}$ = 0 from $+V_S$	0.35	0.5	0.65	mA
		$V_{st\text{-}by}$ = 0 from $-V_S$	-0.2	-0.3	-0.4	mA
V_{os}	Output offset voltage	Output-GND (single-ended)			350	mV
		Output L - Output R (bridge)			120	mV
P_o	Output Power	Single-ended, @ THD = 1% 2 x 70W system		70		W
		Bridge, @ THD = 1% 1 x 250W system		250		W
P_d	Power dissipation of the TDA7570	Quiescent condition		1.5	1.75	W

Table 5. Electrical characteristics (continued)

(V_S = ±25V, R_L = 4Ω, f = 100Hz, T_j = 25°C, Gain = 28dB, application circuit shown in *Figure 3*, 2x65/1x130W system, unless otherwise specified.)

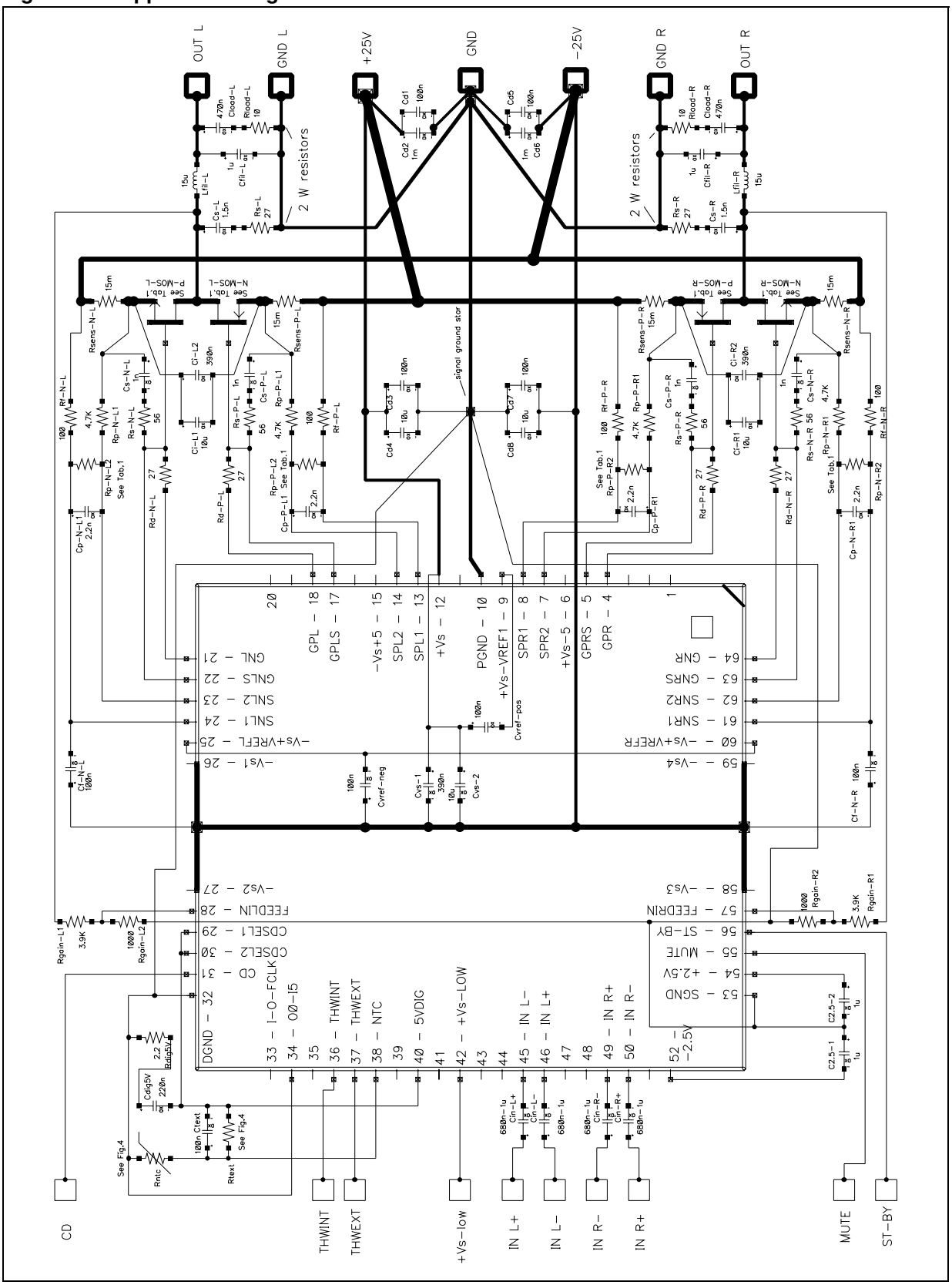
Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
P_{dt}	Power dissipation of the external power transistors (total)	@ P_{out} = 25W, bridge configuration		10		W
THD	Total harmonic distortion	@ P_{out} = 10 W, single ended		0.1		%
		@ P_{out} = 40 W, bridge		0.03	0.1	%
G	Gain	single-ended	27	28	29	dB
G	Gain	Bridge	33	34	35	dB
E_n	Output noise Single_Ended	"A" weighted		200		µV
E	Output noise bridge	"A" weighted		150		µV
ΔG_e	Delta gain error between channels	f = 1kHz, after output filter of TBD order, 20kHz butterworth			0.5	dB
R_i	Input resistance	Single-ended	7	10	13	KΩ
R_i	Input resistance	Bridge	3.5	5	6.5	KΩ
V_{gspth}	Threshold voltage of the Pchannel V_{gs} sensor (VSpx1 - VGpxs)		2.5	3	3.5	V
V_{gsnth}	Threshold voltage of the Pchannel V_{gs} sensor (VGnxs - VSnx1)		2.5	3	3.5	V
c_t	Crosstalk	f = 1kHz, V_o = 2Vrms	50	60		dB
A_m	Mute attenuation	V_o = 2Vrms	70	80		dB
SVR	Supply voltage rejection	f = 100Hz, V_r = 0.5V	50	60		dB
F_{SW}	Switching frequency		250	310	360	KHz
V_{il}	Logic inputs low level voltage				1.5	V
V_{ih}	Logic inputs high level voltage		2.3			V
CLIP DETECTOR						
Vcd	Clip detector pin max operating voltage (open drain)				5.5	V
CDl	Clip detector pin leakage current	CD off			1	µA
CDs	Clip detector pin saturation voltage	CD on, 1mA			1	V
CDi	Clip detector THD intervention	CDsel1=0, CDsel2=0 (near clipping detection)			0.5	%
		CDsel1=0, CDsel2=1		1		%
		CDsel1=1, CDsel2=0		5		%
		CDsel1=1, CDsel2=1		8		%

Table 5. Electrical characteristics (continued)

(V_S = ±25V, R_L = 4Ω, f = 100Hz, T_j = 25°C, Gain = 28dB, application circuit shown in *Figure 3*, 2x65/1x130W system, unless otherwise specified.)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
PROTECTIONS						
T_{hwc}	Chip thermal warning intervention			150		°C
T_{sdc}	Thermal shut-down chip			160		°C
T_{sdch}	Thermal shut-down chip hysteresis			10		°C
T_{hws}	External thermal warning intervention		5Vdig x 0.45	5Vdig x 0.48	5Vdig x 0.51	V
T_{sds}	External thermal shut-down intervention		5Vdig x 0.37	5Vdig x 0.4	5Vdig x 0.43	V
T_{sdsh}	External thermal shut-down hysteresis		5Vdig x 0.037	5Vdig x 0.04	5Vdig x 0.043	V
V_{pp}	Protection intervention voltage Pchannel (Vspx1-Vspx2)		85	100	120	mV
V_{pn}	Protection intervention voltage Nchannel (Vsnx2-Vsnx1)		85	100	120	mV
I_{spx1}	Current input pins 7, 13		150	200	260	µA
I_{snx1}	Current output pins 24, 61		-150	-200	-260	µA
DRIVERS						
V_{hgp}	High level output voltage (Gpl, Gpr)			$+V_s$-10		V
V_{lgp}	Low level output voltage (Gpl, Gpr)			$+V_s$		V
V_{hgn}	High level output voltage (Gnl, Gnr)			$-V_s$		V
V_{lgn}	Low level output voltage (Gnl, Gnr)			$-V_s$+10		V
I_{hgp}	High level output sink current (Gpl, Gpr, peak)			2.2		A
I_{lgp}	Low level output source current (Gpl, Gpr, peak)			2.7		A
I_{hgn}	High level output sink current (Gnl, Gnr, peak)			2.5		A
I_{lgn}	Low level output source current (Gnl, Gnr, peak)			1.7		A
INTERNAL POWER SUPPLY						
5Vdig	5Vdig pin output voltage	Reference: dgnd pin	4.3	4.8	5.3	V
2.5V	2.5V pin output voltage	Reference: sgnd pin	2.15	2.4	2.65	V
-2.5V	-2.5V pin output voltage	Reference: sgnd pin	-2.15	-2.4	-2.65	V
Vref1	Vref1 pin output voltage	Reference: + Vs pin	8.6	9.6	10.6	V
Vrefl/Vrefr	Vrefl, Vrefr pin output voltage	Reference: - Vs pin	-8.6	-9.6	-10.6	V

Figure 3. Application diagrams



3.4 Notes on the electrical schematic shown in *Figure 3*

3.4.1 Main characteristics

- 2 channels single-ended or 1 channel bridge PWM amplifier
- Power output: see *Table 5*
- Gain single-ended = 28 dB
- Gain bridge = 34dB
- Clip detector settled at THD=10%
- Internal master oscillator

The schematic is depicted showing the suggested structure of the printed circuit board tracks (star points, high current path, components placement).

To avoid malfunctioning due to the parasitic inductance, short connections lengths are recommended.

Table 6. Component characteristics

Component (See schematic of *Figure 4*)	Minimum load: 2 x 4 Ohm single-ended or 8 Ohm bridge (2 x 65W / 1 x 130W)	Minimum load: 2 x 2 Ohm single-ended or 4Ohm bridge (2 x 125W / 1 x 250W))
P-MOS-L P-MOS-R	STP12PF06	2 x STP12PF06 in parallel
N-MOS-L N-MOS-R	STP14NF06	2 x STP14NF06 in parallel
Rp-N-L2 RP-P-L2 Rp-N-R2 Rp-P-R2	Not present	4.7K

4 Functions, pins and components description

4.1 Components with critical placement and type:

- Ci-L1, Ci-L2, Ci-R1, Ci-R2 must be placed as near as possible to the sources of the respective power MOS. If 2 power MOS in parallel are needed, can be useful to place a couple of capacitors for each couple of power MOS. These capacitors are needed to absorb the high di/dt current present during the Pchannel/Nchannel and Nchannel/Pchannel transition that can cause high peak voltages on the power supply wiring connection due to their parasitic inductance.
- The capacitors placed between +Vs to GND and to -Vs are distributed along the power lines. With P.C. board with very short connections, some of these capacitors can be avoided (Cvs-1, Cvs-2, Cd3, Cd4, Cd5, Cd6).
- The current sensing resistors Rsens-N-L, Rsens-P-L, Rsens-P-R and Rsens-N-R must be not inductive components, as example, made by a costant an wire.

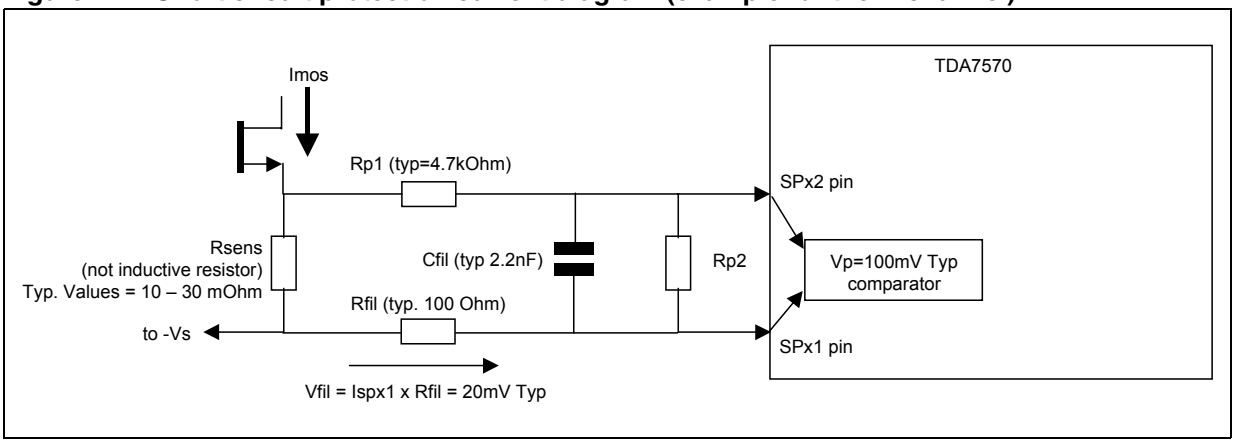
4.2 Input capacitors

- The value of the input capacitors (Cin-L+, Cin-L-, Cin-R+, Cin-R- depends on the desired -3dB high pass cutoff frequency, following the formula:

$$F(3dB) = \frac{1}{6.28 \cdot 10000 \cdot C_{in}}$$

4.3 Short circuit protection current calculation

Figure 4. Short circuit protection current diagram (example for the N-channel)



$$I_{lim} = \frac{1}{Rsens}\left(\frac{Vpx \cdot (Rp1 + Rp2)}{Rp2} + Vfil\right)$$

$$I_{lim} = \frac{1}{Rsens}(Vpx + Vfil) \quad \leftarrow \text{if Rp2 is not used}$$

4.4 External thermal protection network

Example of external thermal protection circuitry

- Components:
  - type: B57621 C621/100k/+
  - R_{text} = 10K
- Results (simulations):
  - External thermal warning temperature intervention: 90 °C
  - External thermal shut down temperature intervention: 100 °C
  - External thermal shut down hysteresis: 6 °C

4.5 Gate driving network

The main purpose of the 27 Ohm resistors Rd-N-L, Rd-P-L, Rd-N-R and Rd-P-R are the following:

- 1) Dumping of the L-C equivalent circuit done by the parasitic inductance and capacitance present in the circuit
- 2) Reduction of the dv/dt of the Vgs and then reduction of the di/dt of the drain current of the power MOS.

The R-C snubber network done by:

- Rs-N-L, Cs-N-L
- Rs-P-L, Cs-P-L
- Rs-N-R, Cs-N-R
- Rs-P-R, Cs-P-R

Are in the direction to increase the dumping (point 1) and reduce the dv/dt (point 2.

The value of these components is also depending on the layout structure. With a reduction of the parasitic inductance present in the P.C. board layout, in the region around the power transistors, the value of these components can be reduced, giving advantage in terms of THD, mainly at mid-high power levels, due to the reduction of the "dead zone".

The minimum suggested value of Rd-x-x is around 10Ω, while, is some cases, Rs-x-x and Cs-x-x can be removed.

4.6 External connections

- **CD, THWEXT, THWINT**
  These pins, if used, it must be connected to a pull-up resistor (>10kΩ) connected to a supply voltage referred to the receiver device (as example, a μP). Max 10V.
- **MUTE** - To have a soft mute-play and play-mute transition, an R-C network can be applied (as example 47kΩ, 1μF)
- **ST-BY** - To avoid pop noise due to multiple ST-BY parasitic pulses, an R-C network can be added (as example 47kΩ, 0.1μF)
- **+V_s-low** - This pin supply the low voltage circuits. It can be connected to the +Vs or to a reference voltage comprising between 12V to +Vs.

A connection to +Vs through a 100Ω resistor, together a 1μF capacitor placed from +Vs-low and GND is possible too.

- **NL+, INL-, INR+, INR-** Input pins. The sign is referred to the input of the differential-to-singleended amplifier. Because the power stage is an inverting stage, the output of the amplifier is with opposite sign with respect these pins. For bridge operation, the connection INL+ must be shorted to the INR- and the connection INL- must be shorted to INR+

5 Package informations

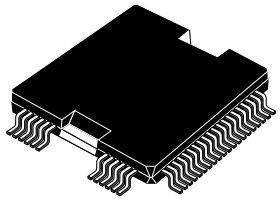
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 5. HiQUAD-64 mechanical data and package dimensions

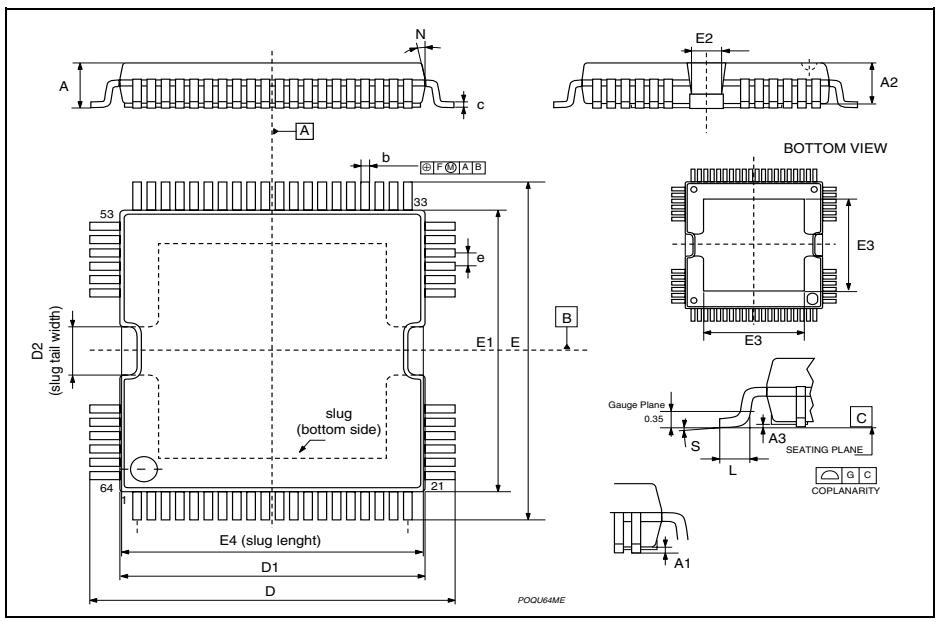
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.15			0.124
A1	0		0.25	0		0.010
A2	2.50		2.90	0.10		0.114
A3	0		0.10	0		0.004
b	0.22		0.38	0.008		0.015
c	0.23		0.32	0.009		0.012
D	17.00		17.40	0.669		0.685
D1 (1)	13.90	14.00	14.10	0.547	0.551	0.555
D2	2.65	2.80	2.95	0.104	0.110	0.116
E	17.00		17.40	0.669		0.685
E1 (1)	13.90	14.00	14.10	0.547	0.551	0.555
e		0.65			0.025	
E2	2.35		2.65	0.092		0.104
E3	9.30	9.50	9.70	0.366	0.374	0.382
E4	13.30	13.50	13.70	0.523	0.531	0.539
F		0.10			0.004	
G		0.12			0.005	
L	0.80		1.10	0.031		0.043
N	10°(max.)					
S	0°(min.), 7°(max.)					

(1): "D1" and "E1" do not include mold flash or protusions
- Mold flash or protusions shall not exceed 0.15mm(0.006inch) per side

OUTLINE AND MECHANICAL DATA



HiQUAD-64



6 Revision history

Table 7. Document revision history

Date	Revision	Changes
29-Aug-2007	1	Initial release.