

# SINGLE CHIP RDS DEMODULATOR + FILTER

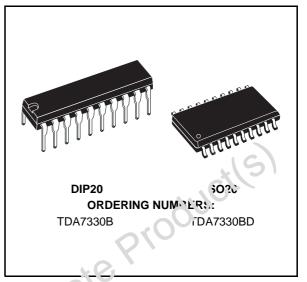
- HIGH PERFORMANCE, 57KHz BANDPASS FILTER (8th ORDER)
- FILTER ADJUSTMENT FREE AND WITHOUT EXTERNAL COMPONENTS
- PURELY DIGITAL RDS DEMODULATION WITHOUT EXTERNAL COMPONENTS
- ARI (SK INDICATION) AND RDS SIGNAL QUALITY OUTPUT
- 4.332MHz CRYSTAL OSCILLATOR (8.664MHz OPTIONAL)
- LOW NOISE MIXED BIPOLAR/CMOS TECH-NOLOGY

# DESCRIPTION

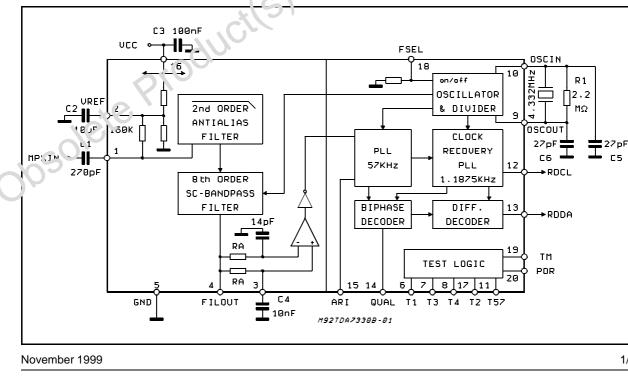
The TDA7330B is a RDS demodulator. It recovers the additional inaudible RDS information which is transmitted by FM radio broadcasting stations.

The output data signal (RDDA) and clock signal (RDCL) can be further processed by a suitable RDS decoder (microprocessor).

The device operates in accordance with the EBU (European Broadcasting Union) specifications. The IC includes a 2nd order antialiasing input fil-



ter, a 57 KHz switched capacitor band pass filter, a smcounny filter and cross detector, a bit rate clock recovery circuit, a 57 KHz PLL, BI-PHASE CSK decoder, differential decoding circuit, ARI inducation and RDS signal quality output.



# **BLOCK DIAGRAM**

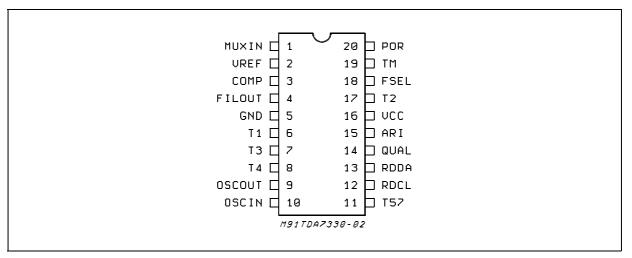
# **ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply Voltage	7	V
T <sub>op</sub>	Operating Temperature Range	-40 to 85	°C
T <sub>stg</sub>	Storage Temperature	-40 to 150	°C

# THERMAL DATA

Symbol	Description	DIP20	SO20	Unit
R <sub>th j-case</sub>	Thermal Resistance Junction-case Typ.	100	200	°C/W

# **PIN CONNECTION** (Top view)



# **PIN FUNCTION**

Nr.	Name	Description
1	MUXIN	RDS input signal.
2	V <sub>ref</sub>	Reference voltage
2 3	COMP	Not inverting comparator input (smoothing filter)
4	FIL OUT	Filter Output
4 5 6 7	GND	Ground
6	T1	Testing output pin (not to be used)
7	T3	Testing output pin (not to be used)
8 9	T4	Testing output pin (not to be used)
9	OSC OUT	Oscillator output
10	OSC IN	Oscillator Input
11	T57	Testing output pin: 57KHz clock output
12	RDCL	RDS clock output (1187.5Hz)
13	RDDA	RDS data output
14	QUAL	Output for signal quality indication (High = good)
15	ARI	Output for ARI indication (High when RDS + ARI signals are present)
		(High when only ARI is present)
		(Low when only RDS is present)
		(indefined when no signal is present)
16	V <sub>CC</sub>	Supply Voltage
17	T2	Testing output pin (not to be used)
18	FSEL	Frequency selector pin: open = 4.332MHz, closed to Vcc = 8.664MHz
19	TM	Test mode pin (open = normal RUN)
		(closed to $V_{CC}$ = Test mode)
20	POR	Reset Input for testing (active high)

# **ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 5V$ , Tamb = 25°C; $R_g = 600\Omega$ ; fosc = 4.332MHz; $V_{IN} = 20mVrms$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Тур.	Max.	Unit
SUPPLY						
V <sub>CC</sub>	Supply Voltage		4.5	5	5.5	V
Is	Supply Current			9		mA
R <sub>POR</sub>	POR Pull Down Resistor	pin 20		40		KΩ
POR <sub>ON</sub>	POR Threshold			2.5		V

# FILTER(measured an pin 4 FILOUT)

Fc	Center Frequency		56.5	57	57.5	KHz
BW	3dB Bandwidth		2.5	3	3.5	KHz
G	Gain	f = 57KHz	18	20	22	dB
A	Attenuation	$\Delta f = \pm 4$ KHz f = 38KHz; V <sub>i</sub> = 500mVrms f = 67KHz; V <sub>i</sub> = 250mVrms	18 50 35	22 80 50		dB dB dB
∆Ph	Phase non linearity	A (see note1) B (see note1) C (see note1)		0.5 1 2	5 7.5 10	DEG DEG DEG
Ri	Input Impedance		100	160	200	KΩ
S/N	Signal to Noise Ratio	V <sub>i</sub> = 3mVrms	30	40		dB
Vi	Maximum Input Signal Capability	$f = 19KHz; T3 \le -40dB$ (see note2) f = 57KHz (RDS + ARI)			1 50	Vrms mVrms
RL	Load Impedance	Pin 4	100			KΩ

# CROSS DETECTOR

Î	RA	Resistance pin 3-4		15	21	28	KΩ

# OSCILLATOR

Fosc	Oscillator Frequency	$F_{SEL}$ = Open (*) $F_{SEL}$ = Closed to V <sub>CC</sub> (**)		4.332 8.664		MHz MHz
VCLL	Clock Input level LOW (pin 10)				1	V
VCLH	Clock Input Level HIGH (pin 10)		4			V
	Output Amplitude (pin 9)			4.5		V <sub>PP</sub>

(\*) FSEL pin has an internal 40K $\Omega$  pull down resistor A 4.332MHz QUARTZ must be used (\*\*) A 8.664MHz QUARTZ must be used. **DEMODULATOR** 

### Δfo Max Oscillator Deviation FSEL = Open <u>+</u> 1.2 KHz S<sub>RDS</sub> **RDS** Detection Sensitivity 1 mVrms 3 SARI **ARI Detection Sensitivity** mVrms **RDS Lockup Time** 100 Tlock ms VOH Output HIGH Voltage $I_L = 0.5 mA$ ; pins 12, 13, 14, 15 4 V $I_L = 0.5 mA$ ; pins 12, 13, 14, 15 V Vol Output LOW Voltage 1 Data Rate for RDS RDCL pin 1187.5 Hz f<sub>RDS</sub> **RDDA Transition versus RDCL** (see figure 2) 4.3 t<sub>D</sub> μsec

## Note(1):

The phase non linearity is defined as:  $\Delta Ph = |-2 \phi f2 + \phi f1 + \phi f3|$ 

where  $\phi$ fx is the input-output phase difference at the frequency fx (x = 1,2,3)

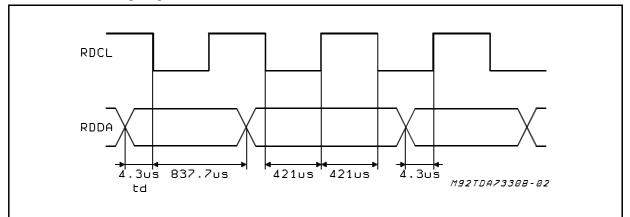
57

Measure	f1 (KHz)	f2 (KHz)	f3 (KHz)	$\Delta \mathbf{Ph} \ \mathbf{max}$
А	56.5	57	57.5	<5°
В	56	57	58	<7.5°
С	55.5	57	58.5	<10°

# ELECTRICAL CHARACTERISTICS (continued)

Note(2): The 3th harmonic (57KHz) must be less than -40dB in respect to the input signal 19KHz plus gain.

# Figure 2: RDS timing diagram



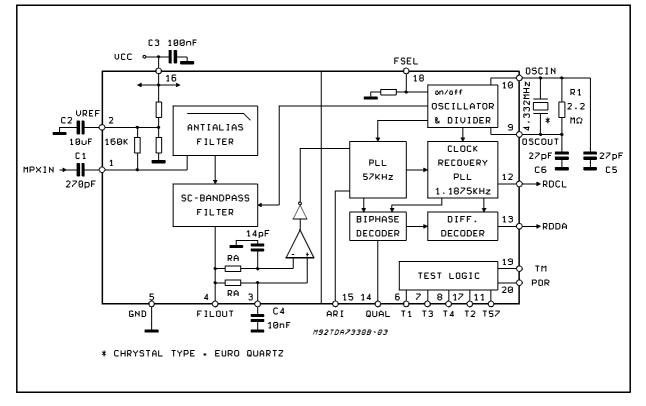
# **OUTPUT TIMING**

The generated 1187.5Hz output clock (RDCL line) is synchronized to the incoming data. According to the internal PLL lock condition this

data change can results on the falling or on the rising clock edge.

Whichever clock edge is used by the decoder (rising or falling edge) the data will remain valid for 416.7  $\mu$ sec after the clock transition.

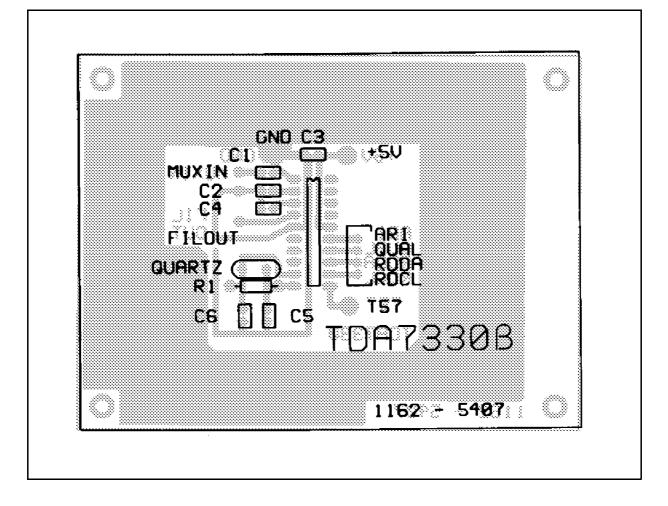
Figure 3: Test Circuit



# **APPLICATION SUGGESTION**

- A good DC decoupling between V<sub>CC</sub> and GROUND is necessary: a 100nF ceramic capacitor, with low resistance and low inductance at high frequency, directly connected on pin 16 (V<sub>CC</sub>)and 5 (GND) is recommended.
- A small series inductance (100μH) or resistor (27Ω) may be used for supply line filtering.
- The Layout path pin2 C2 pin5 must be as short as possible.
- If the supply line, after the power on has a soft and disturbed (spikes) slope, a capacitor of 100nF, between POR and V<sub>CC</sub>, is racommended.
- The various testing pins have no sense for the customer.

Figure 4: P.C. board and component layout of fig. 3 (1:1 scale)



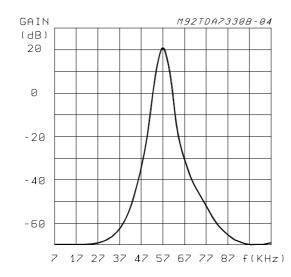
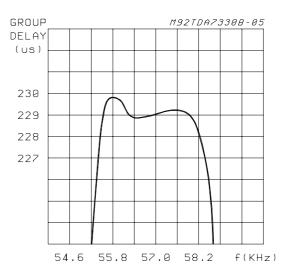


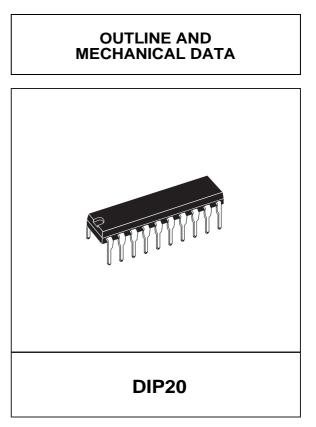
Figure 5: Gain vs. Frequency

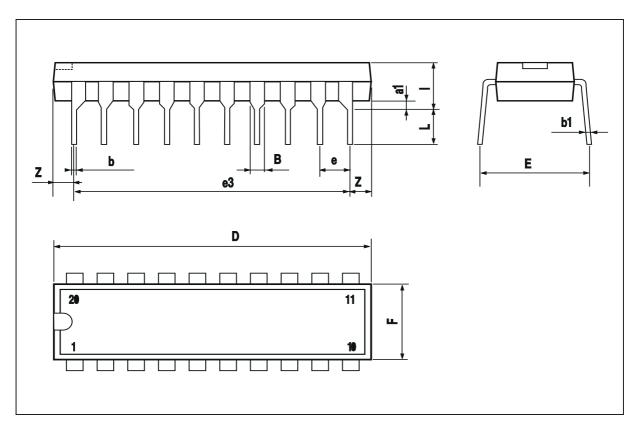
Figure 6: Group Delay vs. Frequency





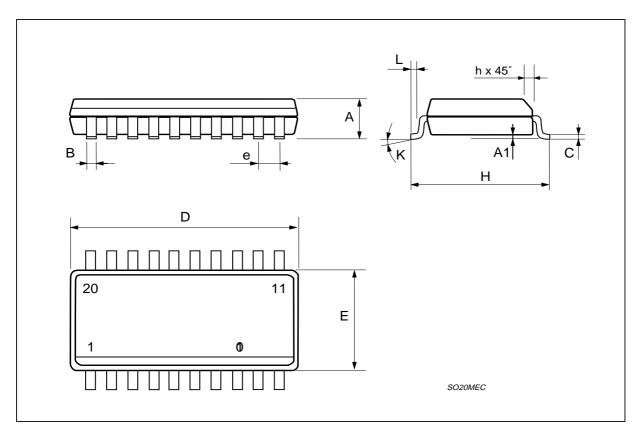
DIM.		mm		inch			
2	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
a1	0.254			0.010			
В	1.39		1.65	0.055		0.065	
b		0.45			0.018		
b1		0.25			0.010		
D			25.4			1.000	
E		8.5			0.335		
е		2.54			0.100		
e3		22.86			0.900		
F			7.1			0.280	
I			3.93			0.155	
L		3.3			0.130		
Z			1.34			0.053	





DIM.		mm			inch					
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
А	2.35		2.65	0.093		0.104				
A1	0.1		0.3	0.004		0.012				
В	0.33		0.51	0.013		0.020				
с	0.23		0.32	0.009		0.013				
D	12.6		13	0.496		0.512				
E	7.4		7.6	0.291		0.299				
е		1.27			0.050					
н	10		10.65	0.394		0.419				
h	0.25		0.75	0.010		0.030				
L	0.4		1.27	0.016		0.050				
к		0° (min.)8° (max.)								

# **ΔΟΥΤΕΙΝΕ ΑΝΟ** ΜΕCHANICAL DATA



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