- Advanced Multibus Architecture With Three Separate 16-Bit Data Memory Buses and One Program Memory Bus
- 40-Bit Arithmetic Logic Unit (ALU) Including a 40-Bit Barrel Shifter and Two Independent 40-Bit Accumulators
- 17- × 17-Bit Parallel Multiplier Coupled to a 40-Bit Dedicated Adder for Non-Pipelined Single-Cycle Multiply/Accumulate (MAC) Operation
- Compare, Select, and Store Unit (CSSU) for the Add/Compare Selection of the Viterbi Operator
- Exponent Encoder to Compute an Exponent Value of a 40-Bit Accumulator Value in a Single Cycle
- Two Address Generators With Eight Auxiliary Registers and Two Auxiliary Register Arithmetic Units (ARAUs)
- Data Bus With a Bus Holder Feature
- Address Bus With a Bus Holder Feature
- Extended Addressing Mode for 8M × 16-Bit Maximum Addressable External Program Space
- 192K × 16-Bit Maximum Addressable Memory Space (64K Words Program, 64K Words Data, and 64K Words I/O)
- On-Chip ROM with Some Configurable to Program/Data Memory
- Dual-Access On-Chip RAM
- Single-Access On-Chip RAM
- Single-Instruction Repeat and Block-Repeat Operations for Program Code
- Block-Memory-Move Instructions for Better Program and Data Management
- Instructions With a 32-Bit Long Word Operand
- Instructions With Two- or Three-Operand Reads

- Arithmetic Instructions With Parallel Store and Parallel Load
- Conditional Store Instructions
- Fast Return From Interrupt
- On-Chip Peripherals
 - Software-Programmable Wait-State Generator and Programmable Bank Switching
 - On-Chip Phase-Locked Loop (PLL) Clock Generator With Internal Oscillator or External Clock Source
 - Time-Division Multiplexed (TDM) Serial Port
 - Buffered Serial Port (BSP)
 - 8-Bit Parallel Host Port Interface (HPI)
 - One 16-Bit Timer
 - External-Input/Output (XIO) Off Control to Disable the External Data Bus,
 Address Bus and Control Signals
- Power Consumption Control With IDLE1, IDLE2, and IDLE3 Instructions With Power-Down Modes
- CLKOUT Off Control to Disable CLKOUT
- On-Chip Scan-Based Emulation Logic, IEEE Std 1149.1[†] (JTAG) Boundary Scan Logic
- 12.5-ns Single-Cycle Fixed-Point Instruction Execution Time (80 MIPS) for 3.3-V Power Supply)
- 10-ns Single-Cycle Fixed-Point Instruction Execution Time (100 MIPS) for 3.3-V Power Supply (2.5-V Core)
- 8.3-ns Single-Cycle Fixed-Point Instruction Execution Time (120 MIPS) for 3.3-V Power Supply (2.5-V Core)
- Available in a 144-Pin Plastic Thin Quad Flatpack (TQFP) (PGE Suffix) and a 144-Pin Ball Grid Array (BGA) (GGU Suffix)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor's and disclaimers thereto appears at the end of this data sheet.

† IEEE Standard 1149.1-1990 Standard-Test-Access Port and Boundary Scan Architecture. All trademarks are the property of their respective owners.



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REVISION HISTORY

This data sheet revision history highlights the technical changes made to the SPRS078F device-specific data sheet to make it an SPRS078G revision.

Scope: Applicable updates to the C5x device family, specifically relating to the C549 device, have been incorporated. Updated the device-specific information supporting the VC549, 8.3-ns, 120 MIPS device, which is now in the production data (PD) state of development.

PAGE(S) NO.	ADDITIONS/CHANGES/DELETIONS
1	Features: Deleted "(Product Preview Data)" from the "8.3-ns Single-Cycle Fixed-Point Instruction Execution Time (120 MIPS) for 3.3-V Power Supply (2.5-V Core)" feature Deleted NOTE about data for the 8.3-ns, 120 MIPS device being Product Preview data
11	$^{\circ}$ 549 Signal Descriptions table, IEEE1149.1 TEST PINS: Added "This pin should be pulled high with a separate 4.7-k Ω resistor" to the EMU0 pin DESCRIPTION Added "This pin should be pulled high with a separate 4.7-k Ω resistor" to the EMU1/OFF pin DESCRIPTION
13	Electrical Characteristics Over Recommended Operating Case Temperature Range table: I _{DD} , Supply current, standby, IDLE3 (VC549-120 only): Deleted the TYP value of "170" μA Added the TYP value of "5" mA for "25°C" TEST CONDITIONS Added the TYP value of "50" mA for "100°C" TEST CONDITIONS
42	Serial Port Receive Timing section: Timing Requirements Over Recommended Operating Conditions for Serial Port Receive table: Changed the MIN value of "th(FSR), Hold time, FSR after CLKR falling edge" from "4" to "6" ns Changed the MIN value of "t _{SU(DR)} , Setup time, DR before CLKR falling edge" from "6" to "4" ns
59	Mechanical Data section: Deleted the "PGE (S-PQFP-G144)" and GGU "(S-PBGA-N144)" mechanical data package diagrams; now an automated merge process Added lead-in sentences for the thermal resistance characteristics table(s) and the "merged" mechanical data packages



TMS320VC549 FIXED-POINT DIGITAL SIGNAL PROCESSOR

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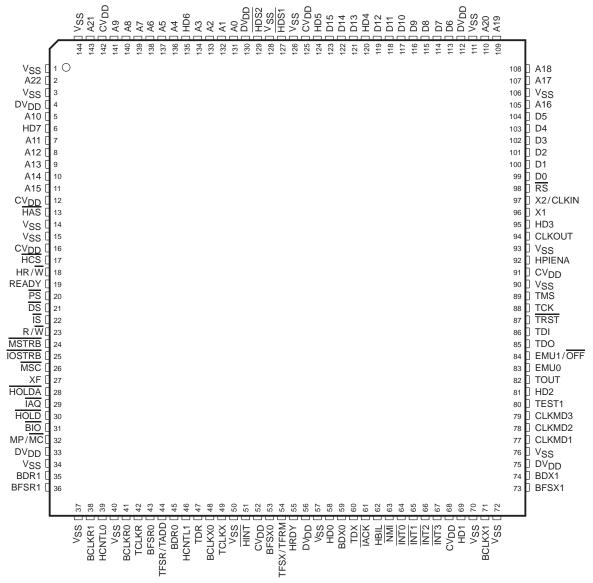
description

The TMS320VC549 fixed-point, digital signal processor (DSP) (hereafter referred to as the 549) is based on an advanced modified Harvard architecture that has one program memory bus and three data memory buses. The processor also provides an arithmetic logic unit (ALU) that has a high degree of parallelism, application-specific hardware logic, on-chip memory, and additional on-chip peripherals. The 549 also utilizes a highly specialized instruction set, which is the basis of its operational flexibility and speed.

Separate program and data spaces allow simultaneous access to program instructions and data, providing the high degree of parallelism. Two reads and one write operation can be performed in a single cycle. Instructions with parallel store and application-specific instructions can fully utilize this architecture. In addition, data can be transferred between data and program spaces. Such parallelism supports a powerful set of arithmetic, logic, and bit-manipulation operations that can all be performed in a single machine cycle. In addition, the 549 includes the control mechanisms to manage interrupts, repeated operations, and function calls.

This data sheet contains the pin layouts, signal descriptions, and electrical specifications for the TMS320VC549 DSP. For additional information, see the *TMS320C54x*, *TMS320LC54x*, *TMS320VC54x* Fixed-Point Digital Signal Processors data sheet (literature number SPRS039). The SPRS039 is considered a family functional overview and should be used in conjunction with this data sheet.

PGE PACKAGE†‡ (TOP VIEW)

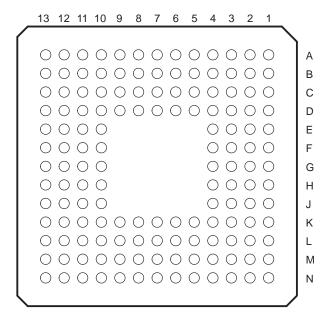


[†] NC = No connection

For the 144-pin TQFP, the letter B in front of CLKRn, FSRn, DRn, CLKXn, FSXn, and DXn pin names denotes buffered serial port (BSP), where n = 0 or 1 port. The letter T in front of CLKR, FSR, DR, CLKX, FSX, and DX pin names denotes time-division multiplexed (TDM) serial port.

[‡] DV_{DD} is the power supply for the I/O pins while CV_{DD} is the power supply for the core CPU, and V_{SS} is the ground for both the I/O pins and the core CPU.

GGU PACKAGE (BOTTOM VIEW)



The pin assignments table to follow lists each signal quadrant and BGA ball pin number for the 144-pin BGA package.

The Signal Descriptions table lists each terminal name, function, and operating mode(s).

Pin Assignments for the 144-Pin GGU Package[†]

SIGNAL QUADRANT 1	BGA BALL#	SIGNAL QUADRANT 2	BGA BALL#	SIGNAL QUADRANT 3	BGA BALL#	SIGNAL QUADRANT 4	BGA BALL#
V _{SS}	A1	BFSX1	N13	V _{SS}	N1	A19	A13
A22	B1	BDX1	M13	BCLKR1	N2	A20	A12
VSS	C2	DV _{DD}	L12	HCNTL0	M3	V _{SS}	B11
DV_DD	C1	Vss	L13	Vss	N3	DV_DD	A11
A10	D4	CLKMD1	K10	BCLKR0	K4	D6	D10
HD7	D3	CLKMD2	K11	TCLKR	L4	D7	C10
A11	D2	CLKMD3	K12	BFSR0	M4	D8	B10
A12	D1	TEST1	K13	TFSR/TADD	N4	D9	A10
A13	E4	HD2	J10	BDR0	K5	D10	D9
A14	E3	TOUT	J11	HCNTL1	L5	D11	C9
A15	E2	EMU0	J12	TDR	M5	D12	В9
CV _{DD}	E1	EMU1/OFF	J13	BCLKX0	N5	HD4	A9
HAS	F4	TDO	H10	TCLKX	K6	D13	D8
V _{SS}	F3	TDI	H11	V _{SS}	L6	D14	C8
Vss	F2	TRST	H12	HINT	M6	D15	B8
CV _{DD}	F1	TCK	H13	CVDD	N6	HD5	A8
HCS	G2	TMS	G12	BFSX0	M7	CV _{DD}	B7
HR/W	G1	Vss	G13	TFSX/TFRM	N7	Vss	A7
READY	G3	CV _{DD}	G11	HRDY	L7	HDS1	C7
PS	G4	HPIENA	G10	DV _{DD}	K7	Vss	D7
DS	H1	V _{SS}	F13	V _{SS}	N8	HDS2	A6
ĪS	H2	CLKOUT	F12	HD0	M8	DV_DD	В6
R/W	Н3	HD3	F11	BDX0	L8	A0	C6
MSTRB	H4	X1	F10	TDX	K8	A1	D6
IOSTRB	J1	X2/CLKIN	E13	IACK	N9	A2	A5
MSC	J2	RS	E12	HBIL	M9	А3	B5
XF	J3	D0	E11	NMI	L9	HD6	C5
HOLDA	J4	D1	E10	ĪNT0	K9	A4	D5
ĪAQ	K1	D2	D13	ĪNT1	N10	A5	A4
HOLD	K2	D3	D12	ĪNT2	M10	A6	B4
BIO	K3	D4	D11	ĪNT3	L10	A7	C4
MP/MC	L1	D5	C13	CV _{DD}	N11	A8	A3
DV _{DD}	L2	A16	C12	HD1	M11	A9	В3
V _{SS}	L3	V _{SS}	C11	V _{SS}	L11	CV _{DD}	C3
BDR1	M1	A17	B13	BCLKX1	N12	A21	A2
BFSR1	M2	A18	B12	VSS	M12	V _{SS}	B2

[†]DV_{DD} is the power supply for the I/O pins while CV_{DD} is the power supply for the core CPU, and V_{SS} is the ground for both the I/O pins and the core CPU.



Signal Descriptions

N	TERMIN.	AL TYPEŤ	DESCRIPTION				
	DATA SIGNALS						
A22 A21 A20 A19 A18 A17 A16 A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	(MSB)	O/Z	Parallel port address bus A22 (MSB) through A0 (LSB). The sixteen LSBs (A15–A0) are multiplexed to address external data/program memory or I/O. A15–A0 are placed in the high-impedance state in the hold mode. A15–A0 also go into the high-impedance state when EMU1/OFF is low. The seven MSBs (A22 to A16) are used for extended program memory addressing. The address bus have a feature called bus holder that eliminates passive components and the power dissipation associated with it. The bus holders keep the address bus at the previous logic level when the bus goes into a high-impedance state. The bus holders on the address bus are always enabled.				
D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0	(MSB)	I/O/Z	Parallel port data bus D15 (MSB) through D0 (LSB). D15–D0 are multiplexed to transfer data between the core CPU and external data/program memory or I/O devices. D15–D0 are placed in the high-impedance state when not output or when RS or HOLD is asserted. D15–D0 also go into the high-impedance state when EMU1/OFF is low. The data bus has a feature called bus holder that eliminates passive components and the power dissipation associated with it. The bus holders keep the data bus at the previous logic level when the bus goes into a high-impedance state. These bus holders are enabled or disabled by the BH bit in the bank switching control register (BSCR).				
	INITIALIZATION, INTERRUPT AND RESET OPERATIONS						
IACK		O/Z	Interrupt acknowledge signal. IACK indicates the receipt of an interrupt and that the program counter is fetching the interrupt vector location designated by A15–0. IACK also goes into the high-impedance state when EMU1/OFF is low.				
INTO INT1 INT2 INT3		I	External user interrupt inputs. INT0-INT3 are prioritized and are maskable by the interrupt mask register and the interrupt mode bit. INT0 -INT3 can be polled and reset by the interrupt flag register.				

[†] I = Input, O = Output, Z = High impedance



TERMINAL .		DESCRIPTION
NAME	TYPET	DESCRIPTION
		INITIALIZATION, INTERRUPT AND RESET OPERATIONS (CONTINUED)
NMI	I	Nonmaskable interrupt. NMI is an external interrupt that cannot be masked by way of the INTM or the IMR. When NMI is activated, the processor traps to the appropriate vector location.
RS	I	Reset input. $\overline{\text{RS}}$ causes the DSP to terminate execution and forces the program counter to $\overline{\text{OFF80h}}$. When $\overline{\text{RS}}$ is brought to a high level, execution begins at location OFF80h of the program memory. $\overline{\text{RS}}$ affects various registers and status bits.
MP/MC	I	Microprocessor/microcomputer mode-select pin. If active-low at reset (microcomputer mode), MP/MC causes the internal program ROM to be mapped into the upper program memory space. In the microprocessor mode, off-chip memory and its corresponding addresses (instead of internal program ROM) are accessed by the DSP.
CNT	I	I/O level select. With CMOS-compatible I/O interface levels, CNT is pulled to a high level.
		MULTIPROCESSING SIGNALS
BIO	I	Branch control input. A branch can be conditionally executed when $\overline{\text{BIO}}$ is active. If low, the processor executes the conditional instruction. The $\overline{\text{BIO}}$ condition is sampled during the decode phase of the pipeline for the XC instruction, and all other instructions sample $\overline{\text{BIO}}$ during the read phase of the pipeline.
XF	O/Z	External flag output (latched software-programmable signal). XF is set high by the SSBX XF instruction, set low by RSBX XF instruction or by loading the ST1 status register. XF is used for signaling other processors in multiprocessor configurations or as a general-purpose output pin. XF goes into the high-impedance state when OFF is low, and is set high at reset.
		MEMORY CONTROL SIGNALS
DS PS IS	O/Z	Data, program, and I/O space select signals. DS, PS, and IS are always high unless driven low for communicating to a particular external space. Active period corresponds to valid address information. Placed into a high-impedance state in hold mode. DS, PS, and IS also go into the high-impedance state when EMU1/OFF is low.
MSTRB	O/Z	Memory strobe signal. MSTRB is always high unless low-level asserted to indicate an external bus access to data or program memory. Placed in high-impedance state in hold mode. MSTRB also goes into the high-impedance state when OFF is low.
READY	I	Data-ready input. READY indicates that an external device is prepared for a bus transaction to be completed. If the device is not ready (READY is low), the processor waits one cycle and checks READY again. Note that the processor performs ready-detection if at least two software wait states are programmed. The READY signal is not sampled until the completion of the software wait states.
R/W	O/Z	Read/write signal. $R\overline{W}$ indicates transfer direction during communication to an external device and is normally high (in read mode), unless asserted low when the DSP performs a write operation. Placed in the high-impedance state in hold mode, $R\overline{W}$ also goes into the high-impedance state when EMU1/ \overline{OFF} is low.
IOSTRB	O/Z	I/O strobe signal. IOSTRB is always high unless low level asserted to indicate an external bus access to an I/O device. Placed in high-impedance state in hold mode. IOSTRB also goes into the high-impedance state when EMU1/OFF is low.
HOLD	I	Hold input. HOLD is asserted to request control of the address, data, and control lines. When acknowledged, these lines go into high-impedance state.
HOLDA	O/Z	Hold acknowledge signal. HOLDA indicates to the external circuitry that the processor is in a hold state and that the address, data, and control lines are in a high-impedance state, allowing them to be available to the external circuitry. HOLDA also goes into the high-impedance state when EMU1/OFF is low.
MSC	O/Z	Microstate complete signal. Goes low on CLKOUT falling at the start of the first software wait state. Remains low until one CLKOUT cycle before the last programmed software wait state. If connected to the READY line, MSC forces one external wait state after the last internal wait state has been completed. MSC also goes into the high-impedance state when EM1/OFF is low.

[†] I = Input, O = Output, Z = High impedance



TERMINAL		DESCRIPTION
NAME	TYPET	DESCRIPTION
		MEMORY CONTROL SIGNALS (CONTINUED)
ĪĀQ	O/Z	Instruction acquisition signal. \overline{IAQ} is asserted (active low) when there is an instruction address on the address bus and goes into the high-impedance state when EMU1/ \overline{OFF} is low.
		OSCILLATOR/TIMER SIGNALS
CLKOUT	O/Z	Master clock output signal. CLKOUT cycles at the machine-cycle rate of the CPU. The internal machine cycle is bounded by the falling edges of this signal. CLKOUT also goes into the high-impedance state when EMU1/OFF is low.
CLKMD1 CLKMD2 CLKMD3	I	Clock mode external/internal input signals. CLKMD1, CLKMD2, and CLKMD3 allow you to select and configure different clock modes, such as crystal, external clock, and various PLL factors. Refer to PLL section for a detailed functional description of these pins.
X2/CLKIN	I	Input pin to internal oscillator from the crystal. If the internal (crystal) oscillator is not being used, a clock can become input to the device using this pin. The internal machine cycle time is determined by the clock operating-mode pins (CLKMD1, CLKMD2 and CLKMD3).
X1	0	Output pin from the internal oscillator for the crystal. If the internal oscillator is not used, X1 should be left unconnected. X1 does not go into the high-impedance state when EMU1/OFF is low.
TOUT	O/Z	Timer output. TOUT signals a pulse when the on-chip timer counts down past zero. The pulse is a CLKOUT-cycle wide. TOUT also goes into the high-impedance state when EMU1/OFF is low.
		BUFFERED SERIAL PORT 0 AND BUFFERED SERIAL PORT 1 SIGNALS
BCLKR0 BCLKR1	1	Receive clocks. External clock signal for clocking data from the data-receive (DR) pin into the buffered serial port receive shift registers (RSRs). Must be present during buffered serial port transfers. If the buffered serial port is not being used, BCLKR0 and BCLKR1 can be sampled as an input by way of IN0 bit of the SPC register.
BCLKX0 BCLKX1	I/O/Z	Transmit clock. Clock signal for clocking data from the serial port transmit shift register (XSR) to the data transmit (DX) pin. BCLKX can be an input if MCM in the serial port control register is cleared to 0. It also can be driven by the device at 1/(CLKDV + 1) where CLKDV range is 0–31 CLKOUT frequency when MCM is set to 1. If the buffered serial port is not used, BCLKX can be sampled as an input by way of IN1 of the SPC register. BCLKX0 and BCLKX1 go into the high-impedance state when OFF is low.
BDR0 BDR1	I	Buffered serial-data-receive input. Serial data is received in the RSR by BDR0/BDR1.
BDX0 BDX1	O/Z	Buffered serial-port-transmit output. Serial data is transmitted from the XSR by way of BDX. BDX0 and BDX1 are placed in the high-impedance state when not transmitting and when EMU1/OFF is low.
BFSR0 BFSR1	I	Frame synchronization pulse for receive input. The falling edge of the BFSR pulse initiates the data-receive process, beginning the clocking of the RSR.
BFSX0 BFSX1	I/O/Z	Frame synchronization pulse for transmit input/output. The falling edge of the BFSX pulse initiates the data-transmit process, beginning the clocking of the XSR. Following reset, the default operating condition of BFSX is an input. BFSX0 and BFSX1 can be selected by software to be an output when TXM in the serial control register is set to 1. This pin goes into the high-impedance state when EMU1/OFF is low.
		SERIAL PORT 0 AND SERIAL PORT 1 SIGNALS
CLKR0 CLKR1	I	Receive clocks. External clock signal for clocking data from the data receive (DR) pin into the serial port receive shift register (RSR). Must be present during serial port transfers. If the serial port is not being used, CLKR0 and CLKR1 can be sampled as an input via IN0 bit of the SPC register.
CLKX0 CLKX1	I/O/Z	Transmit clock. Clock signal for clocking data from the serial port transmit shift register (XSR) to the data transmit (DX) pin. CLKX can be an input if MCM in the serial port control register is cleared to 0. It also can be driven by the device at 1/4 CLKOUT frequency when MCM is set to 1. If the serial port is not used, CLKX can be sampled as an input via IN1 of the SPC register. CLKX0 and CLKX1 go into the high-impedance state when EMU1/OFF is low.
DR0 DR1	I	Serial-data-receive input. Serial data is received in the RSR by DR.

 $[\]dagger$ I = Input, O = Output, Z = High impedance



TERMINAL NAME TYPET		DESCRIPTION				
	SERIAL PORT 0 AND SERIAL PORT 1 SIGNALS (CONTINUED)					
DX0 DX1	O/Z	Serial port transmit output. Serial data is transmitted from the XSR via DX. DX0 and DX1 are placed in the high-impedance state when not transmitting and when EMU1/OFF is low.				
FSR0 FSR1	I	Frame synchronization pulse for receive input. The falling edge of the FSR pulse initiates the data-receive process, beginning the clocking of the RSR.				
FSX0 FSX1	I/O/Z	Frame synchronization pulse for transmit input/output. The falling edge of the FSX pulse initiates the data transmit process, beginning the clocking of the XSR. Following reset, the default operating condition of FSX is an input. FSX0 and FSX1 can be selected by software to be an output when TXM in the serial control register is set to 1. This pin goes into the high-impedance state when EMU1/OFF is low.				
		TDM SERIAL PORT SIGNALS				
TCLKR	1	TDM receive clock input				
TDR	I	TDM serial data-receive input				
TFSR/TADD	I/O	TDM receive frame synchronization or TDM address				
TCLKX	I/O/Z	TDM transmit clock				
TDX	O/Z	TDM serial data-transmit output				
TFSX/TFRM	I/O/Z	TDM transmit frame synchronization				
		HOST PORT INTERFACE SIGNALS				
HD0-HD7	I/O/Z	Parallel bidirectional data bus. HD0–HD7 are placed in the high-impedance state when not outputting data. The signals go into the high-impedance state when EMU1/OFF is low. These pins each have bus holders similar to those on the address/data bus, but which are always enabled.				
HCNTL0 HCNTL1	I	Control inputs				
HBIL	1	Byte-identification input				
HCS	I	Chip-select input				
HDS1 HDS2	I	Data strobe inputs				
HAS	1	Address strobe input				
HR/W	I	Read/write input				
HRDY	O/Z	Ready output. This signal goes into the high-impedance state when EMU1/OFF is low.				
HINT	O/Z	Interrupt output. When the DSP is in reset, this signal is driven high. The signal goes into the high-impedance state when EMU1/OFF is low.				
HPIENA	I	HPI module select input. This signal must be tied to a logic 1 state to have HPI selected. If this input is left open or connected to ground, the HPI module will not be selected, internal pullup for the HPI input pins are enabled, and the HPI data bus has keepers set. This input is provided with an internal pull-down resistor which is active only when RS is low. HPIENA is sampled when RS goes high and ignored until RS goes low again. Refer to the Electrical Characteristics section for the input current requirements for this pin.				
	SUPPLY PINS					
CV _{DD}	Supply	+V _{DD} . CV _{DD} is the dedicated power supply for the core CPU.				
DV_DD	Supply	+V _{DD} . DV _{DD} is the dedicated power supply for I/O pins.				
VSS	Supply	Ground. VSS is the dedicated power ground for the device.				

[†] I = Input, O = Output, Z = High impedance



TERN NAME	IINAL TYPE [†]	DESCRIPTION
		IEEE1149.1 TEST PINS
TCK	I	IEEE standard 1149.1 test clock. Pin with internal pullup device. This is normally a free-running clock signal with a 50% duty cycle. The changes on the test-access port (TAP) of input signals TMS and TDI are clocked into the TAP controller, instruction register, or selected test data register on the rising edge of TCK. Changes at the TAP output signal (TDO) occur on the falling edge of TCK.
TDI	I	IEEE standard 1149.1 test data input. Pin with internal pullup device. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK.
TDO	O/Z	IEEE standard 1149.1 test data output. The contents of the selected register (instruction or data) is shifted out of TDO on the falling edge of TCK. TDO is in the high-impedance state except when the scanning of data is in progress. TDO also goes into the high-impedance state when EMU1/OFF is low.
TMS	1	IEEE standard 1149.1 test mode select. Pin with internal pullup device. This serial control input is clocked into the TAP controller on the rising edge of TCK.
TRST	1	IEEE standard 1149.1 test reset. TRST, when high, gives the IEEE standard 1149.1 scan system control of the operations of the device. If TRST is not connected or driven low, the device operates in its functional mode, and the IEEE standard 1149.1 signals are ignored. Pin with internal pulldown device.
EMU0	I/O/Z	Emulator interrupt 0 pin. When $\overline{\text{TRST}}$ is driven low, EMU0 must be high for the activation of the EMU1/ $\overline{\text{OFF}}$ condition. When $\overline{\text{TRST}}$ is driven high, EMU0 is used as an interrupt to or from the emulator system and is defined as input/output by way of IEEE standard 1149.1 scan system. This pin should be pulled high with a separate 4.7-k Ω resistor.
EMU1/OFF	I/O/Z	Emulator interrupt 1 pin/disable all outputs. When TRST is driven high, EMU1/OFF is used as an interrupt to or from the emulator system and is defined as input/output by way of IEEE standard 1149.1 scan system. When TRST is driven low, EMU1/OFF is configured as OFF. The EMU1/OFF signal, when active low, puts all output drivers into the high-impedance state. This pin should be pulled high with a separate 4.7-kΩ resistor. Note that OFF is used exclusively for testing and emulation purposes (not for multiprocessing applications). Therefore, for the OFF condition, the following conditions apply: TRST = low, EMU0 = high EMU1/OFF = low
		DEVICE TEST PIN
TEST1	I	Test1 – Reserved for internal use only. This pin must not be connected (NC).

 $[\]dagger$ I = Input, O = Output, Z = High impedance

TMS320VC549 FIXED-POINT DIGITAL SIGNAL PROCESSOR

SPRS078G - SEPTEMBER 1998 - REVISED OCTOBER 2004

absolute maximum ratings over specified temperature range (unless otherwise noted)†

Supply voltage I/O range, DV _{DD} ‡	0.3 V to 4.6 V
Supply voltage core range, CV _{DD} [‡]	. -0.3 V to 3.75 V
Input voltage range	
Output voltage range	\dots -0.3 V to 4.6 V
Operating case temperature range, T _C	. -40° C to 100° C
Storage temperature range, T _{stg}	55°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			MIN	NOM	MAX	UNIT
DV_{DD}	Device supply voltage, I/O [†]		3	3.3	3.6	V
CV _{DD}	Device supply voltage, core†		2.4	2.5	2.75	V
VSS	Supply voltage, GND			0		V
VIH	High-level input voltage, I/O	Schmitt trigger inputs, $DV_{DD} = 3.3 \pm 0.3 \text{ V}^{\ddagger}$	2.5		DV _{DD} + 0.3	V
		All other inputs	2		DV _{DD} + 0.3	
VIL	Low-level input voltage		-0.3		0.8	V
ІОН	High-level output current				-300	μΑ
l _{OL}	Low-level output current				1.5	mA
TC	Operating case temperature		-40		100	°C

Texas Instrument DSPs do not require specific power sequencing between the core supply and the I/O supply. However, systems should be designed to ensure that neither supply is powered up for extended periods of time if the other supply is below the proper operating voltage. Excessive exposure to these conditions can adversely affect the long term reliability of the devices. System-level concerns such as bus contention may require supply sequencing to be implemented. In this case, the core supply should be powered up at the same time as, or prior to (and powered down after), the I/O buffers. For additional power sequencing information, see the *Power Supply Sequencing Solutions for Dual Supply Voltage DSPs* application report (literature number SLVA073).

See Figure 1 for 3.3-V device test load circuit values.



[‡] All voltage values are with respect to VSS.

[‡] On the VC549 devices, the following pins have schmitt trigger inputs: RS, INTn, NMI, X2/CLKIN, CLKMDn, TCK, HAS, HCS, HDSn, BCLKRn, TCLKR, BCLKXn, and TCLKX

electrical characteristics over recommended operating case temperature range (unless otherwise noted)

	PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT	
Vон	High-level	high-level output voltage‡ V _{DD} = 3.3 ± 0.3 V, I _{OH} = MAX		2.4			V		
VOL	Low-level	output voltage [‡]	I _{OL} = MAX				0.4	V	
	Input current in	A[22:0]	V _{DD} = MAX☆		-150		250	4	
l IZ	high impedan ce	All other pins	$V_{DD} = MAX$, $V_{I} = V_{SS}$ to V_{DD}	$V_{DD} = MAX, V_I = V_{SS}$ to V_{DD}			10	μΑ	
		TRST	With internal pulldown		-10		800		
	Input	HPIENA	With internal pulldown, $\overline{RS} = 0$		-10		400	μΑ	
١.	current	TMS, TCK, TDI, HPI	With internal pullups		-400		10		
li l	$(V_I = V_{SS})$	D[15:0], HD[7:0]	Bus holders enabled, V _{DD} = MAX☆		-150		250		
	to V _{DD})	X2/CLKIN	Oscillator enabled		-40		40		
		All other input-only pins			-10		10		
IDDC	Supply cur	rent, core CPU	$CV_{DD} = 2.5 \text{ V}, f_X = 40 \text{ MHz}, \ T_C = 25^{\circ}\text{C}$			20¶		mA	
I _{DDP}	Supply cui	rent, pins	$DV_{DD} = 3.3 \text{ V}, f_X = 40 \text{ MHz}, \ T_C = 25^{\circ}\text{C}$			12#		mA	
		IDLE2	PLL × 1 mode, 40 MHz input			2		mA	
lDD	Supply current,		Divide-by-two mode, CLKIN stopped (VC549-80 and VC549-100)			15		μΑ	
	standby IDLE3 Divide-by-two mode, CLKIN sto	Divide-by-two mode, CLKIN stopped	25°C		5				
		(VC549-120 only) 100°C	100°C		50		mA .		
Ci	C _i Input capacitance			•		10		pF	
Co	Output cap	pacitance				10		pF	

[†] All values are typical unless otherwise specified.

[‡] All input and output voltage levels except RS, INTO – INT3, NMI, CNT, X2/CLKIN, CLKMD0 – CLKMD3 are LVTTL-compatible.

[§] Clock mode: PLL × 1 with external source

This value was obtained with 50% usage of MAC and 50% usage of NOP instructions. Actual operating current varies with program being executed.

[#] This value was obtained with single-cycle external writes, CLKOFF = 0 and load = 15 pF. For more details on how this calculation is performed, refer to the *Calculation of TMS320LC54x Power Dissipation* application report (literature number SPRA164).

^{||} HPI input signals except for HPIENA.

 $[\]star V_{IL}(MIN) \leq V_{I} \leq V_{IL}(MAX)$ or $V_{IH}(MIN) \leq V_{I} \leq V_{IH}(MAX)$

PARAMETER MEASUREMENT INFORMATION

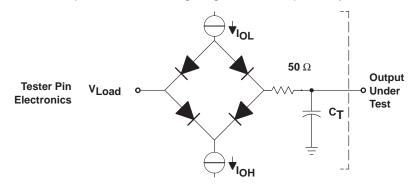
timing parameter symbology

Timing parameter symbols used are created in accordance with JEDEC Standard 100-A. To shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

Lowercase	subscripts and their meanings:	Letters and	symbols and their meanings:
а	access time	Н	High
С	cycle time (period)	L	Low
d	delay time	V	Valid
dis	disable time	Z	High impedance
en	enable time		
f	fall time		
h	hold time		
r	rise time		
su	setup time		
t	transition time		
V	valid time		
W	pulse duration (width)		
Χ	Unknown, changing, or don't care level		

signal transition reference points

All timing references are made at a voltage of 1.5 volts, except rise and fall times which are referenced at the 10% and 90% points of the specified low and high logic levels, respectively.



Where: I_{OL} = 1.5 mA (all outputs) I_{OH} = 300 μ A (all outputs)

 $V_{Load} = 1.5 V$

C_T = 40 pF typical load circuit capacitance.

Figure 1. 3.3-V Test Load Circuit

internal oscillator with external crystal

The internal oscillator is enabled by selecting the appropriate clock mode at reset (this is device dependent – see PLL section) and connecting a crystal or ceramic resonator across X1 and X2/CLKIN. The CPU clock frequency is one-half the crystal oscillation frequency following reset. After reset, the clock mode of the devices with the software PLL can also be changed to divide-by-four.

The crystal should be in fundamental mode operation and parallel resonant with an effective series resistance of 30ohms and power dissipation of 1 mW. The connection of the required circuit, consisting of the crystal and two load capacitors, is shown in Figure 2. The load capacitors, C₁ and C₂, should be chosen such that the equation below is satisfied. C_L in the equation is the load specified for the crystal.

$$C_{L} = \frac{C_{1}C_{2}}{(C_{1} + C_{2})}$$

recommended operating conditions (see Figure 2)

		549-80			549-100			549-120			
				MAX	MIN	NOM	MAX	MIN	NOM	MAX	UNIT
f _X	Input clock frequency	10†		20‡	10†		20‡	10†		20‡	MHz

[†] This device utilizes a fully static design and therefore can operate with t_{C(CI)} approaching ∞. The device is characterized at frequencies approaching 0 Hz.

[‡] It is recommended that the PLL clocking option be used for maximum frequency operation.

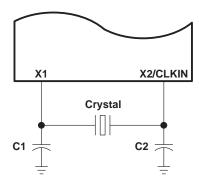


Figure 2. Internal Divide-by-Two Clock Option With External Crystal

TMS320VC549 FIXED-POINT DIGITAL SIGNAL PROCESSOR

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divide-by-two/divide-by-four clock option - PLL disabled

The frequency of the reference clock provided at the X2/CLKIN pin can be divided by a factor of two or four to generate the internal machine cycle.

When an external clock source is used, the frequency injected must conform to specifications listed in the timing requirements table.

switching characteristics over recommended operating conditions for divide-by-two/divide-by-four clock option – PLL disabled [H = $0.5t_{\rm C(CO)}$] (see Figure 2 and Figure 3, and the recommended operating conditions table)

	DADAMETED		549-80		549-100			549-120			UNIT
	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNII
t _C (CO)	Cycle time, CLKOUT	12.5‡	2t _{c(CI)}	†	10‡	2t _{c(CI)}	†	8.33‡	2t _{c(CI)}	†	ns
td(CIH-CO)	Delay time, X2/CLKIN high to CLKOUT high/low	3	6	10	3	6	10	3	6	10	ns
t _f (CO)	Fall time, CLKOUT†		2			2			2		ns
t _r (CO)	Rise time, CLKOUT [†]		2			2			2		ns
tw(COL)	Pulse duration, CLKOUT low†	H-3	H-1	Н	H-2	H-1	Н	H-2	H–1	Н	ns
tw(COH)	Pulse duration, CLKOUT high [†]	H-3	H-1	Н	H-2	H-1	Н	H-2	H-1	Н	ns

[†] This device utilizes a fully static design and therefore can operate with t_{C(CI)} approaching ∞. The device is characterized at frequencies approaching 0 Hz.

[‡] It is recommended that the PLL clocking option be used for maximum frequency operation.

divide-by-two/divide-by-four clock option - PLL disabled (continued)

timing requirements for divide-by-two/divide-by-four clock option – PLL disabled (see Figure 3)

		549-80		549-100		549-120		
		MIN	MAX	MIN	MAX	MIN	MAX	UNIT
t _C (CI)	Cycle time, X2/CLKIN	20‡	†	20‡	†	20‡	†	ns
t _f (CI)	Fall time, X2/CLKIN		8		8		8	ns
tr(CI)	Rise time, X2/CLKIN		8		8		8	ns
tw(CIL)	Pulse duration, X2/CLKIN low	5	†	5	†	5	†	ns
tw(CIH)	Pulse duration, X2/CLKIN high	5	†	5	†	5	†	ns

[†] This device utilizes a fully static design and therefore can operate with $t_{C(CI)}$ approaching ∞ . The device is characterized at frequencies approaching 0 Hz.

[‡] It is recommended that the PLL clocking option be used for maximum frequency operation.

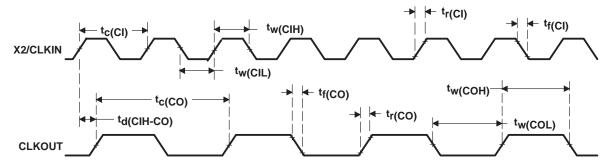


Figure 3. External Divide-by-Two Clock Timing

TMS320VC549 FIXED-POINT DIGITAL SIGNAL PROCESSOR

SPRS078G - SEPTEMBER 1998 - REVISED OCTOBER 2004

multiply-by-N clock option - PLL enabled

The frequency of the reference clock provided at the X2/CLKIN pin can be multiplied by a factor of N to generate the internal machine cycle.

When an external clock source is used, the frequency injected must conform to specifications listed in the timing requirements table.

switching characteristics over recommended operating conditions for multiply-by-N clock option – PLL enabled [H = $0.5t_{c(CO)}$] (see Figure 2 and Figure 4, and the recommended operating conditions table)

			549-80		549-100				UNIT		
	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNII
t _{c(CO)}	Cycle time, CLKOUT	12.5	tc(CI)/N		10	tc(CI)/N		8.33	tc(CI)/N		ns
td(CIH-CO)	Delay time, X2/CLKIN high/low to CLKOUT high/low	3	6	10	3	6	10	3	6	10	ns
t _f (CO)	Fall time, CLKOUT		2			2			2		ns
t _r (CO)	Rise time, CLKOUT		2			2			2		ns
tw(COL)	Pulse duration, CLKOUT low	H-3	H-1	Н	H-2	H-1	Н	H-2	H-1	Н	ns
tw(COH)	Pulse duration, CLKOUT high	H-3	H-1	Н	H-2	H-1	Н	H-2	H-1	Н	ns
tp	Transitory phase, PLL lock-up time			29			35			45	μS

multiply-by-N clock option - PLL enabled (continued)

timing requirements for multiply-by-N clock option – PLL enabled (see Figure 4)

			549	-80	549- 549-	UNIT	
			MIN	MAX	MIN	MAX	
		Integer PLL multiplier N (N = 1–15)	20†	200	20†	200	
t _C (CI)	Cycle time, X2/CLKIN	PLL multiplier N = x.5	20†	100	20†	100	ns
, ,		PLL multiplier N = x.25, x.75	20†	50	20†	50	
t _f (CI)	Fall time, X2/CLKIN	·		8		8	ns
t _{r(CI)}	Rise time, X2/CLKIN			8		8	ns
tw(CIL)	Pulse duration, X2/CLKIN low		5		5		ns
tw(CIH)	Pulse duration, X2/CLKIN high		5		5		ns

[†] Note that for all values of $t_{C(CI)}$, the minimum $t_{C(CO)}$ period must not be exceeded.

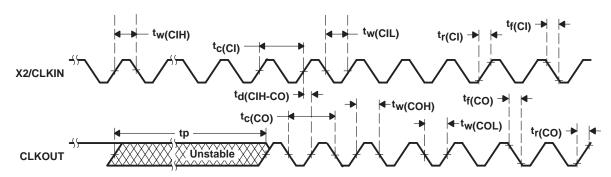


Figure 4. External Multiply-by-One Clock Timing

TMS320VC549 FIXED-POINT DIGITAL SIGNAL PROCESSOR

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memory and parallel I/O interface timing

$\underline{switching}$ characteristics over recommended operating conditions for a memory read (MSTRB = 0)†‡ (see Figure 5)

	PARAMETER			549-100		549-	LINIT	
	PARAMETER				MAX	MIN	MAX	UNIT
td(CLKL-A)	Delay time, address valid from CLKOUT low§	- 1	5	- 1	4	- 1	4	ns
td(CLKH-A)	Delay time, address valid from CLKOUT high (transition) \P	- 1	5	- 1	4	- 1	4	ns
td(CLKL-MSL)	Delay time, MSTRB low from CLKOUT low	- 1	5	- 1	4	- 1	3	ns
td(CLKL-MSH)	Delay time, MSTRB high from CLKOUT low	- 1	5	- 1	5	- 1	3	ns
th(CLKL-A)R	Hold time, address valid after CLKOUT low§	- 1	5	- 1	4	- 1	4	ns
th(CLKH-A)R	Hold time, address valid after CLKOUT high¶	- 1	5	-1	4	-1	4	ns

[†] Address, PS, and DS timings are all included in timings referenced as address.

[‡] See Table 1, Table 2, and Table 3 for address bus timing variation with load capacitance.

 $[\]$ In the case of a memory read preceded by a memory read

[¶] In the case of a memory read preceded by a memory write

timing requirements for a memory read ($\overline{\text{MSTRB}}$ = 0) [H = 0.5 t_{c(CO)}]^{†‡} (see Figure 5)

		549-80		549-100		549-120		
		MIN	MAX	MIN	MAX	MIN	MAX	UNIT
ta(A)M	Access time, read data access from address valid		2H-9		2H-8		2H-8	ns
ta(MSTRBL)	Access time, read data access from MSTRB low		2H-8		2H-7		2H-7	ns
t _{su(D)R}	Setup time, read data before CLKOUT low	5		5		5		ns
th(D)R	Hold time, read data after CLKOUT low	0		0		0		ns
th(A-D)R	Hold time, read data after address invalid	0	·	0		0	·	ns
th(D)MSTRBH	Hold time, read data after MSTRB high	0		0		0		ns

[†] Address, PS, and DS timings are all included in timings referenced as address. ‡ See Table 1, Table 2, and Table 3 for address bus timing variation with load capacitance.

memory and parallel I/O interface timing (continued)

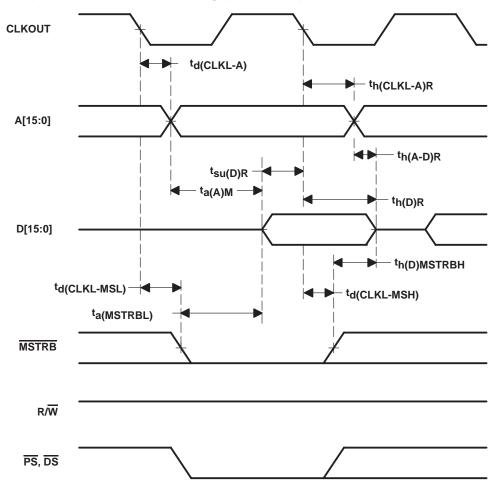


Figure 5. Memory Read ($\overline{MSTRB} = 0$)

switching characteristics over recommended operating conditions for a memory write (MSTRB = 0) [H = 0.5 $t_{c(CO)}$]^{†‡} (see Figure 6)

		549	-80	549-	100	549-120		UNIT
	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
t _d (CLKH-A)	Delay time, address valid from CLKOUT high§	- 1	5	- 1	4	- 1	4	ns
td(CLKL-A)	Delay time, address valid from CLKOUT low¶	- 1	5	- 1	4	- 1	4	ns
^t d(CLKL-MSL)	Delay time, MSTRB low from CLKOUT low	- 1	5	- 1	4	- 1	3	ns
td(CLKL-D)W	Delay time, data valid from CLKOUT low	0	7	0	7	0	5	ns
^t d(CLKL-MSH)	Delay time, MSTRB high from CLKOUT low	- 1	5	– 1	5	- 1	3	ns
^t d(CLKH-RWL)	Delay time, R/\overline{W} low from CLKOUT high	0	5	0	4	- 1	4	ns
td(CLKH-RWH)	Delay time, R/\overline{W} high from CLKOUT high	- 1	5	– 1	4	- 1	4	ns
td(RWL-MSTRBL)	Delay time, MSTRB low after R/W low	H – 2	H + 3	H – 2	H + 2	H – 2	H + 2	ns
^t h(A)W	Hold time, address valid after CLKOUT high§	- 1	5	- 1	4	- 1	4	ns
th(D)MSH	Hold time, write data valid after MSTRB high	H-4	H+4¶	H-3	H+3¶	H-3	H+3¶	ns
t _{w(SL)MS}	Pulse duration, MSTRB low	2H-5		2H-4		2H-4		ns
t _{su(A)W}	Setup time, address valid before MSTRB low	2H-5		2H-4		2H-4		ns
t _{su(D)MSH}	Setup time, write data valid before MSTRB high	2H-7	2H+7¶	2H-5	2H+5¶	2H-4	2H+4¶	ns

 $^{^{\}dagger}$ Address, $\overline{\text{PS}}$, and $\overline{\text{DS}}$ timings are all included in timings referenced as address.

[‡] See Table 1, Table 2, and Table 3 for address bus timing variation with load capacitance.

[§] In the case of a memory write preceded by a memory write.

¶ In the case of a memory write preceded by an I/O cycle.

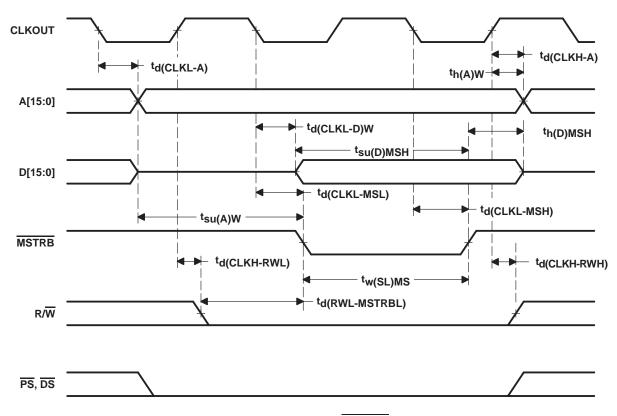


Figure 6. Memory Write ($\overline{MSTRB} = 0$)



memory and parallel I/O interface timing (continued)

switching characteristics over recommended operating conditions for a parallel I/O port read ($\overline{IOSTRB} = 0$)^{†‡} (see Figure 7)

	PARAMETER			549-100		549-12	20	LINUT
PARAMETER		MIN	MAX	MIN	MAX	MIN	MAX	UNIT
td(CLKL-A)	Delay time, address valid from CLKOUT low	- 1	5	– 1	4	– 1	4	ns
^t d(CLKH-ISTRBL)	Delay time, IOSTRB low from CLKOUT high	0	5	0	4	0	4	ns
^t d(CLKH-ISTRBH)	Delay time, IOSTRB high from CLKOUT high	- 1	5	– 1	4	– 1	4	ns
t _{h(A)IOR}	Hold time, address after CLKOUT low	- 1	5	- 1	4	- 1	4	ns

[†] Address and $\overline{\text{IS}}$ timings are included in timings referenced as address.

[‡] See Table 1, Table 2, and Table 3 for address bus timing variation with load capacitance.

timing requirements for a parallel I/O port read ($\overline{IOSTRB} = 0$) [H = 0.5 t_{c(CO)}]^{†‡} (see Figure 7)

		549-80		549-100		549-120		
		MIN	MAX	MIN	MAX	MIN	MAX	UNIT
t _{a(A)IO}	Access time, read data access from address valid		3H-9		3H-8		3H-8	ns
ta(ISTRBL)IO	Access time, read data access from OSTRB low		2H-9		2H-8		2H-7	ns
t _{su(D)IOR}	Setup time, read data before CLKOUT high	4		4		4		ns
th(D)IOR	Hold time, read data after CLKOUT high	0		0		0		ns
th(ISTRBH-D)R	Hold time, read data after IOSTRB high	0		0		0		ns

[†] Address and IS timings are included in timings referenced as address.

[‡] See Table 1, Table 2, and Table 3 for address bus timing variation with load capacitance.

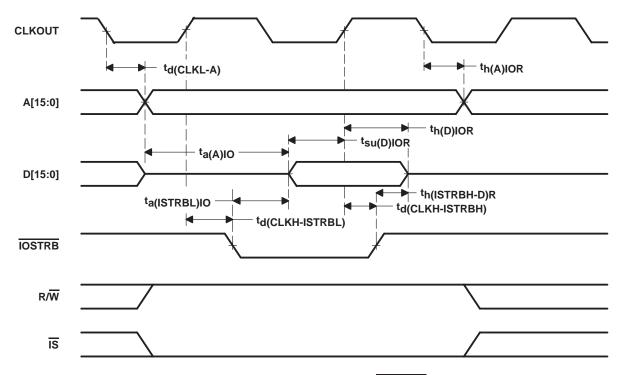


Figure 7. Parallel I/O Port Read (IOSTRB = 0)

switching characteristics over recommended operating conditions for a parallel I/O port write $(\overline{\text{IOSTRB}} = 0) [H = 0.5 t_{\text{C(CO)}}] (\text{see Figure 8})^{\dagger}$

	DADAMETER	549-	-80	549-	100	549-120		UNIT
	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNII
td(CLKL-A)	Delay time, address valid from CLKOUT low [‡]	- 1	5	- 1	4	- 1	4	ns
td(CLKH-ISTRBL)	Delay time, IOSTRB low from CLKOUT high	0	5	0	4	0	4	ns
td(CLKH-D)IOW	Delay time, write data valid from CLKOUT high	H-5	H+7	H-5	H+7	H-5	H+6	ns
td(CLKH-ISTRBH)	Delay time, IOSTRB high from CLKOUT high	- 1	5	- 1	4	- 1	4	ns
td(CLKL-RWL)	Delay time, R/W low from CLKOUT low	0	5	0	4	0	4	ns
td(CLKL-RWH)	Delay time, R/W high from CLKOUT low	0	5	0	4	0	4	ns
th(A)IOW	Hold time, address valid from CLKOUT low‡	- 1	5	- 1	4	- 1	4	ns
th(D)IOW	Hold time, write data after IOSTRB high	H-4	H+4	H-3	H+3	H-3	H+3	ns
t _{su(D)IOSTRBH}	Setup time, write data before IOSTRB high	H-5	H+1	H-5	H+1	H-5	Н	ns
t _{su(A)IOSTRBL}	Setup time, address valid before IOSTRB low	H-5	H+5	H-3	H+3	H-3	H+3	ns

[†] See Table 1, Table 2, and Table 3 for address bus timing variation with load capacitance. ‡ Address and TS timings are included in timings referenced as address.

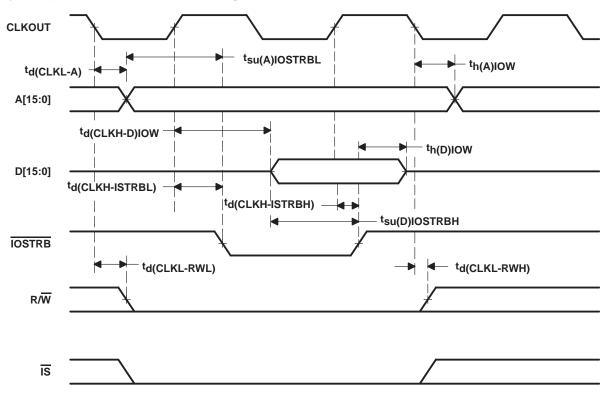


Figure 8. Parallel I/O Port Write (IOSTRB = 0)

I/O timing variation with load capacitance: SPICE simulation results

Condition: Temperature : 125° C

Capacitance : 0-100pF : 2.7/3.0/3.3 V

Voltage Model : Weak/Nominal/Strong

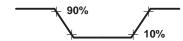


Figure 9. Rise and Fall Time Diagram

I/O timing variation with load capacitance: SPICE simulation results (continued)

Table 1. Timing Variation With Load Capacitance: [2.7 V] 10% – 90%

	WE	AK	NOM	INAL	STR	ONG
	RISE	FALL	RISE	FALL	RISE	FALL
0 pF	0.476 ns	0.457 ns	0.429 ns	0.391 ns	0.382 ns	0.323 ns
10 pF	1.511 ns	1.278 ns	1.386 ns	1.148 ns	1.215 ns	1.049 ns
20 pF	2.551 ns	2.133 ns	2.350 ns	1.956 ns	2.074 ns	1.779 ns
30 pF	3.614 ns	3.011 ns	3.327 ns	2.762 ns	2.929 ns	2.512 ns
40 pF	4.664 ns	3.899 ns	4.394 ns	3.566 ns	3.798 ns	3.264 ns
50 pF	5.752 ns	4.786 ns	5.273 ns	4.395 ns	4.655 ns	4.010 ns
60 pF	6.789 ns	5.656 ns	6.273 ns	5.206 ns	5.515 ns	4.750 ns
70 pF	7.817 ns	6.598 ns	7.241 ns	6.000 ns	6.442 ns	5.487 ns
80 pF	8.897 ns	7.531 ns	8.278 ns	6.928 ns	7.262 ns	6.317 ns
90 pF	10.021 ns	8.332 ns	9.152 ns	7.735 ns	8.130 ns	7.066 ns
100 pF	11.072 ns	9.299 ns	10.208 ns	8.537 ns	8.997 ns	7.754 ns

Table 2. Timing Variation With Load Capacitance: [3 V] 10% - 90%

	WEAK		NOMINAL		STRONG		
	RISE	FALL	RISE	FALL	RISE	FALL	
0 pF	0.436 ns	0.387 ns	0.398 ns	0.350 ns	0.345 ns	0.290 ns	
10 pF	1.349 ns	1.185 ns	1.240 ns	1.064 ns	1.092 ns	0.964 ns	
20 pF	2.273 ns	1.966 ns	2.098 ns	1.794 ns	1.861 ns	1.634 ns	
30 pF	3.226 ns	2.765 ns	2.974 ns	2.539 ns	2.637 ns	2.324 ns	
40 pF	4.168 ns	3.573 ns	3.849 ns	3.292 ns	3.406 ns	3.013 ns	
50 pF	5.110 ns	4.377 ns	4.732 ns	4.052 ns	4.194 ns	3.710 ns	
60 pF	6.033 ns	5.230 ns	5.660 ns	4.811 ns	5.005 ns	4.401 ns	
70 pF	7.077 ns	5.997 ns	6.524 ns	5.601 ns	5.746 ns	5.117 ns	
80 pF	8.020 ns	6.899 ns	7.416 ns	6.336 ns	6.559 ns	5.861 ns	
90 pF	8.917 ns	7.709 ns	8.218 ns	7.124 ns	7.323 ns	6.498 ns	
100 pF	9.885 ns	8.541 ns	9.141 ns	7.830 ns	8.101 ns	7.238 ns	

I/O timing variation with load capacitance: SPICE simulation results (continued)

Table 3. Timing Variation With Load Capacitance: [3.3 V] 10% - 90% [3 V] 10% - 90%

	WI	EAK	NOMINAL		STRONG	
	RISE	FALL	RISE	FALL	RISE	FALL
0 pF	0.404 ns	0.361 ns	0.371 ns	0.310 ns	0.321 ns	0.284 ns
10 pF	1.227 ns	1.081 ns	1.133 ns	1.001 ns	1.000 ns	0.892 ns
20 pF	2.070 ns	1.822 ns	1.915 ns	1.675 ns	1.704 ns	1.530 ns
30 pF	2.931 ns	2.567 ns	2.719 ns	2.367 ns	2.414 ns	2.169 ns
40 pF	3.777 ns	3.322 ns	3.515 ns	3.072 ns	3.120 ns	2.823 ns
50 pF	4.646 ns	4.091 ns	4.319 ns	3.779 ns	3.842 ns	3.466 ns
60 pF	5.487 ns	4.859 ns	5.145 ns	4.503 ns	4.571 ns	4.142 ns
70 pF	6.405 ns	5.608 ns	5.980 ns	5.234 ns	5.301 ns	4.767 ns
80 pF	7.284 ns	6.463 ns	6.723 ns	5.873 ns	5.941 ns	5.446 ns
90 pF	8.159 ns	7.097 ns	7.560 ns	6.692 ns	6.740 ns	6.146 ns
100 pF	8.994 ns	7.935 ns	8.300 ns	7.307 ns	7.431 ns	6.822 ns

ready timing for externally generated wait states

timing requirements for externally generated wait states [H = 0.5 $t_{c(CO)}$][†] (see Figure 10, Figure 11, Figure 12, and Figure 13)

		549-80		549-100		549-120		LINUT
		MIN	MAX	MIN	MAX	MIN	MAX	UNIT
t _{su(RDY)}	Setup time, READY before CLKOUT low	6		5		5		ns
t _{h(RDY)}	Hold time, READY after CLKOUT low	0		0		0		ns
t _V (RDY)MSTRB	Valid time, READY after MSTRB low‡		4H-10		4H-8		4H-8	ns
th(RDY)MSTRB	Hold time, READY after MSTRB low [‡]	4H		4H		4H		ns
t _V (RDY)IOSTRB	Valid time, READY after IOSTRB low [‡]		5H-10		5H-8		5H-8	ns
th(RDY)IOSTRB	Hold time, READY after IOSTRB low‡	5H		5H		5H		ns
t _V (MSCL)	Valid time, MSC low after CLKOUT low	0	5	0	4	0	4	ns
t _V (MSCH)	Valid time, MSC high after CLKOUT low	0	5	0	4	0	4	ns

[†] The hardware wait states can be used only in conjunction with the software wait states to extend the bus cycles. To generate wait states by READY, at least two software wait states must be programmed. READY is not sampled until the completion of the internal software wait states.

[‡]These timings are included for reference only. The critical timings for READY are those referenced to CLKOUT.

ready timing for externally generated wait states (continued)

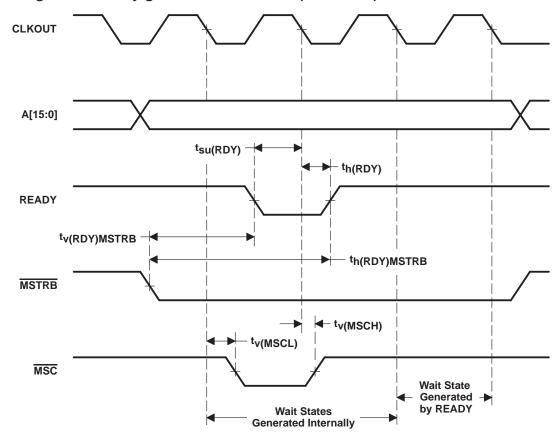


Figure 10. Memory Read With Externally Generated Wait States



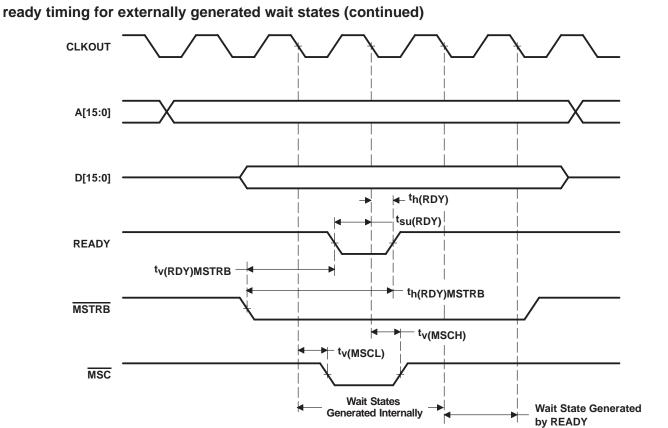


Figure 11. Memory Write With Externally Generated Wait States

ready timing for externally generated wait states (continued)

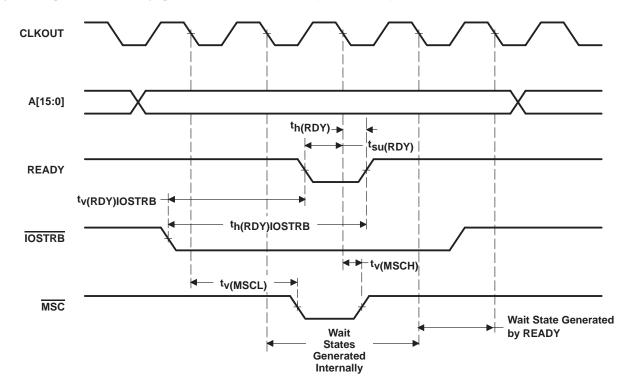


Figure 12. I/O Read With Externally Generated Wait States



ready timing for externally generated wait states (continued)

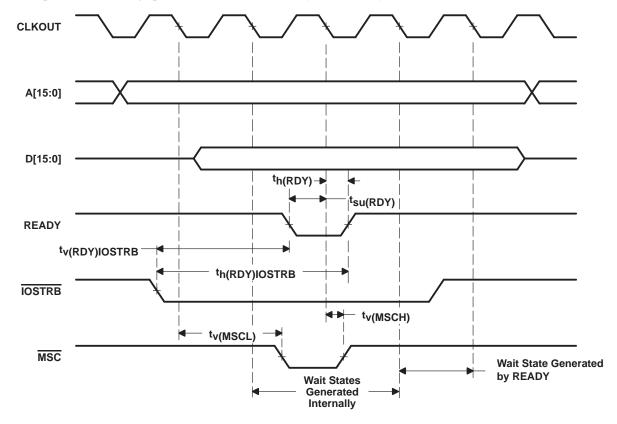


Figure 13. I/O Write With Externally Generated Wait States

TMS320VC549 FIXED-POINT DIGITAL SIGNAL PROCESSOR

SPRS078G - SEPTEMBER 1998 - REVISED OCTOBER 2004

HOLD and **HOLDA** timing

switching characteristics over recommended operating conditions for memory control signals and HOLDA [H = 0.5 $t_{c(CO)}$] (see Figure 14)

	PARAMETER	549	549-80 549-100 549-120	
		MIN	MAX]
^t dis(CLKL-A)	Disable time, CLKOUT low to address, PS, DS, IS high impedance		5	ns
tdis(CLKL-RW)	Disable time, CLKOUT low to R/W high impedance		5	ns
^t dis(CLKL-S)	Disable time, CLKOUT low to MSTRB, IOSTRB high impedance		5	ns
ten(CLKL-A)	Enable time, CLKOUT low to address, PS, DS, IS		2H+5	ns
ten(CLKL-RW)	Enable time, CLKOUT low to R/\overline{W} enabled		2H+5	ns
ten(CLKL-S)	Enable time, CLKOUT low to MSTRB, IOSTRB enabled	2	2H+5	ns
^t v(HOLDA)	Valid time, HOLDA low after CLKOUT low	0	5	ns
	Valid time, HOLDA high after CLKOUT low	0	5	ns
tw(HOLDA)	Pulse duration, HOLDA low duration	2H-3		ns

timing requirements for $\overline{\text{HOLD}}$ [H = 0.5 $t_{\text{c(CO)}}$] (see Figure 14)

		549-80 549-100 549-120	UNIT
		MIN MAX	
tw(HOLD)	Pulse duration, HOLD low duration	4H+10	ns
t _{su(HOLD)}	Setup time, HOLD before CLKOUT low	10	ns

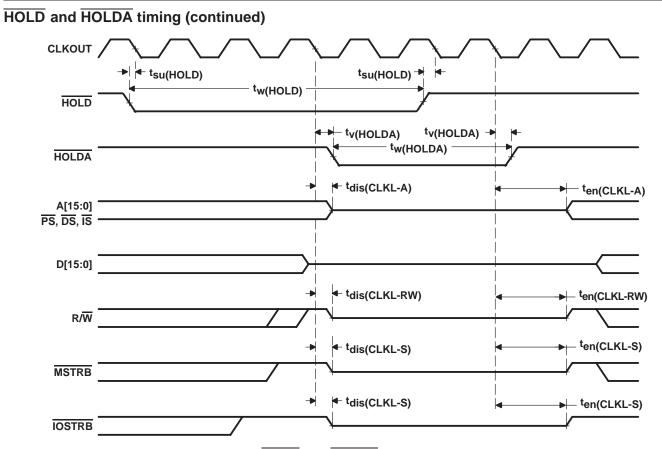


Figure 14. $\overline{\text{HOLD}}$ and $\overline{\text{HOLDA}}$ Timing (HM = 1)

reset, BIO, interrupt, and MP/MC timings

timing requirements over recommended operating conditions for reset, interrupt, $\overline{\text{BIO}}$, and $\overline{\text{MP/MC}}$ [H = 0.5 t_{C(CO)}] (see Figure 15, Figure 16, and Figure 17)

		549-	80	549-	100	549-	120	
		MIN	MAX	MIN	MAX	MIN	MAX	UNIT
^t h(RS)	Hold time, RS after CLKOUT low	0		0		0		ns
^t h(BIO)	Hold time, BIO after CLKOUT low	0		0		0		ns
^t h(INT)	Hold time, INTn, NMI, after CLKOUT low†	0		0		0		ns
th(MPMC)	Hold time, MP/MC after CLKOUT low	0		0		0		ns
^t w(RSL)	Pulse duration, RS lowद	4H+7		4H+5		4H+5		ns
tw(BIO)S	Pulse duration, BIO low, synchronous	2H+7		2H+5		2H+5		ns
tw(BIO)A	Pulse duration, BIO low, asynchronous	4H		4H		4H		ns
tw(INTH)S	Pulse duration, INTn, NMI high (synchronous)	2H+7		2H+7		2H+7		ns
^t w(INTH)A	Pulse duration, INTn, NMI high (asynchronous)	4H		4H		4H		ns
tw(INTL)S	Pulse duration, INTn, NMI low (synchronous)	2H+7		2H+7		2H+7		ns
^t w(INTL)A	Pulse duration, INTn, NMI low (asynchronous)	4H		4H		4H		ns
tw(INTL)WKP	Pulse duration, INTn, NMI low for IDLE2/IDLE3 wakeup	10		8		8		ns
t _{su(RS)}	Setup time, RS before X2/CLKIN low§	5		5		5		ns
t _{su(BIO)}	Setup time, BIO before CLKOUT low	10	2H	9	2H	8	2H	ns
t _{su(INT)}	Setup time, INTn, NMI, RS before CLKOUT low	10	2H	9	2H	8	2H	ns
tsu(MPMC)	Setup time, MP/MC before CLKOUT low	10		8		8		ns

[†] The external interrupts (INT0 – INT3, NMI) are synchronized to the core CPU by way of a two flip-flop synchronizer which samples these inputs with consecutive falling edges of CLKOUT. The input to the interrupt pins is required to represent a 1–0–0 sequence at the timing that is corresponding to three CLKOUTs sampling sequence.

[‡] If the PLL mode is selected, then at power-on sequence, or at wakeup from IDLE3, RS must be held low for at least 50 μs to assure synchronization and lock-in of the PLL.

[§] Divide-by-two mode

[¶] Note that $\overline{\mathsf{RS}}$ may cause a change in clock frequency, therefore changing the value of H (see the PLL section).

reset, BIO, interrupt, and MP/MC timings (continued)

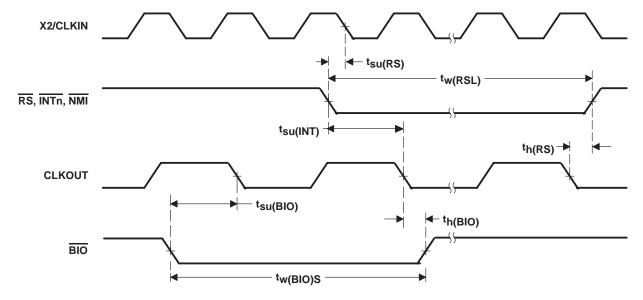


Figure 15. Reset and BIO Timings

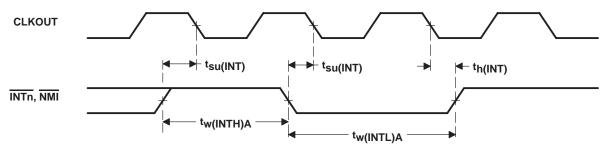


Figure 16. Interrupt Timing

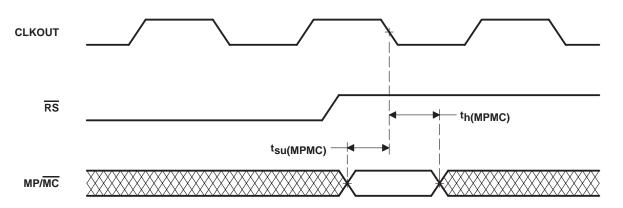


Figure 17. MP/MC Timing

instruction acquisition (IAQ), interrupt acknowledge (IACK), external flag (XF), and TOUT timing

switching characteristics over recommended operating conditions for $\overline{\text{IAQ}}$ and $\overline{\text{IACK}}$ [H = 0.5 $t_{\text{c(CO)}}$] (see Figure 18)

	PARAMETER	549-80 549-100		549-120		UNIT
		MIN	MAX	MIN	MAX	
td(CLKL-IAQL)	Delay time, IAQ low from CLKOUT low	- 1	5	- 1	4	ns
td(CLKL-IAQH)	Delay time, IAQ high from CLKOUT low	- 1	5	- 1	4	ns
t _d (A)IAQ	Delay time, address valid before IAQ low		4		4	ns
td(CLKL-IACKL)	Delay time, IACK low from CLKOUT low	0	5	0	4	ns
td(CLKL-IACKH)	Delay time , IACK high from CLKOUT low	0	5	0	4	ns
td(A)IACK	Delay time, address valid before IACK low		3		3	ns
th(A)IAQ	Hold time, address valid after IAQ high	- 3		- 3		ns
th(A)IACK	Hold time, address valid after IACK high	- 3		- 3		ns
tw(IAQL)	Pulse duration, IAQ low	2H-3		2H-3		ns
tw(IACKL)	Pulse duration, IACK low	2H-3		2H-3		ns

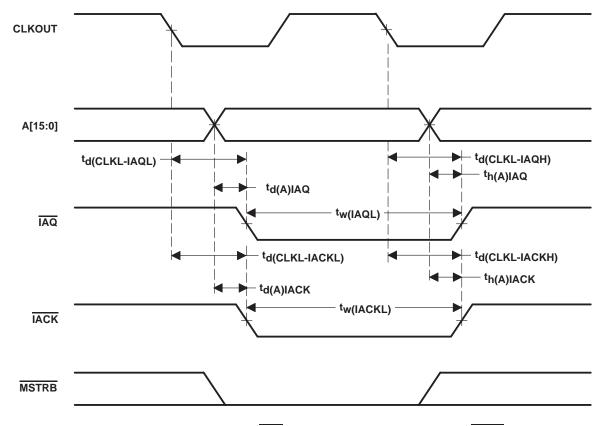


Figure 18. Instruction Acquisition (IAQ) and Interrupt Acknowledge (IACK) Timing

instruction acquisition (IAQ), interrupt acknowledge (IACK), external flag (XF), and TOUT timing (continued)

switching characteristics over recommended operating conditions for external flag (XF) and TOUT [H = 0.5 $t_{c(CO)}$] (see Figure 19 and Figure 20)

PARAMETER		549-80 549-100		549-120		UNIT
		MIN	MAX	MIN	MAX	
	Delay time, XF high after CLKOUT low	0	5	0	4	
^t d(XF)	Delay time, XF low after CLKOUT low	0	5	0	4	ns
td(TOUTH)	Delay time, TOUT high after CLKOUT low	0	5	– 1	4	ns
td(TOUTL)	Delay time, TOUT low after CLKOUT low	-1	5	– 1	4	ns
tw(TOUT)	Pulse duration, TOUT	2H-3		2H-3		ns

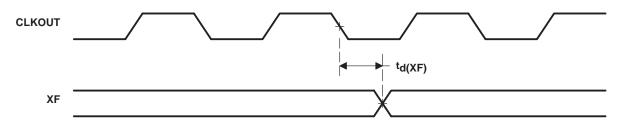


Figure 19. External Flag (XF) Timing

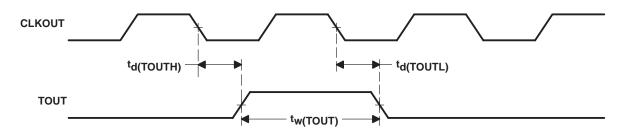


Figure 20. TOUT Timing

serial port receive timing

timing requirements over recommended operating conditions for serial port receive [H = $0.5 t_{c(CO)}$] (see Figure 21)

		549-80 549-100 549-120		549-100		UNIT
		MIN	MAX			
t _C (SCK)	Cycle time, serial port clock	6H	†	ns		
t _f (SCK)	Fall time, serial port clock		6	ns		
tr(SCK)	Rise time, serial port clock		6	ns		
tw(SCK)	Pulse duration, serial port clock low/high	ЗН		ns		
t _{su(FSR)}	Setup time, FSR before CLKR falling edge	4		ns		
th(FSR)	Hold time, FSR after CLKR falling edge	6		ns		
th(DR)	Hold time, DR after CLKR falling edge	6		ns		
t _{su(DR)}	Setup time, DR before CLKR falling edge	4		ns		

[†] The serial port design is fully static and, therefore, can operate with t_C(SCK) approaching ∞. It is characterized approaching an input frequency of 0 Hz but tested at a much higher frequency to minimize test time.

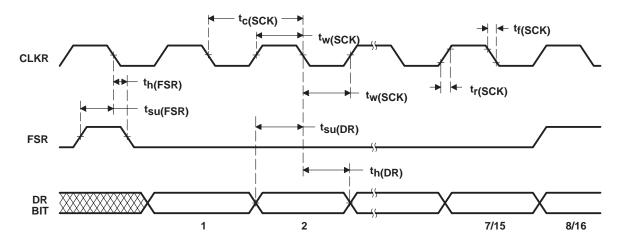


Figure 21. Serial Port Receive Timing

serial port transmit timing

switching characteristics over recommended operating conditions for serial port transmit with external clocks and frames (see Figure 22)

	PARAMETER		549-80 549-100 549-120		
		MIN	MAX		
t _d (DX)	Delay time, DX valid after CLKX rising		25	ns	
th(DX)	Hold time, DX valid after CLKX rising	- 5		ns	
tdis(DX)	Disable time, DX after CLKX rising		40	ns	

timing requirements over recommended operating conditions for serial port transmit with external clocks and frames $[H = 0.5t_{c(CO)}]$ (see Figure 22)

		549-80 549-100 549-120		UNIT
		MIN	MAX	
t _c (SCK)	Cycle time, serial port clock	6H	†	ns
th(FSX)	Hold time, FSX after CLKX falling edge (see Note 1)	6		ns
th(FSX)H	Hold time, FSX after CLKX rising edge (see Note 1)		2H-3 [‡]	ns
td(FSX)	Delay time, FSX after CLKX rising edge		2H-3	ns
tf(SCK)	Fall time, serial port clock		6	ns
tr(SCK)	Rise time, serial port clock		6	ns
tw(SCK)	Pulse duration, serial port clock low/high	3H		ns

[†] The serial port design is fully static and, therefore, can operate with t_C(SCK) approaching ∞. It is characterized approaching an input frequency of 0 Hz but tested at a much higher frequency to minimize test time.

NOTE 1: Internal clock with external FSX and vice versa are also allowable. However, FSX timings to CLKX always are defined depending on the source of FSX, and CLKX timings always are dependent upon the source of CLKX. Specifically, the relationship of FSX to CLKX is independent of the source of CLKX.

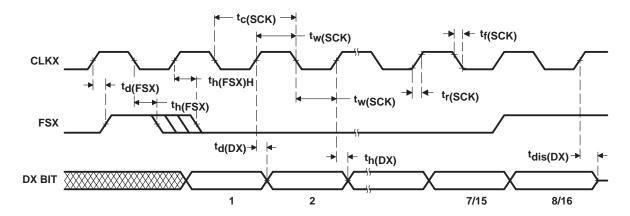


Figure 22. Serial Port Transmit Timing With External Clocks and Frames

[‡] If the FSX pulse does not meet this specification, the first bit of serial data is driven on DX until the falling edge of FSX. After the falling edge of FSX, data is shifted out on DX pin. The transmit buffer-empty interrupt is generated when the th(FSX) and th(FSX)H specification is met.

serial port transmit timing (continued)

switching characteristics over recommended operating conditions for serial port transmit with internal clocks and frames [H = $0.5t_{c(CO)}$] (see Figure 23)

PARAMETER		549-80 549-100 549-120			UNIT
		MIN	TYP	MAX	
t _C (SCK)	Cycle time, serial port clock		8H		ns
td(FSX)	Delay time, CLKX rising to FSX			7	ns
t _d (DX)	Delay time, CLKX rising to DX			7	ns
tdis(DX)	Disable time, CLKX rising to DX			20	ns
th(DX)	Hold time, DX valid after CLKX rising edge	-2			ns
t _f (SCK)	Fall time, serial port clock			3	ns
tr(SCK)	Rise time, serial port clock			3	ns
tw(SCK)	Pulse duration, serial port clock low/high	4H-4			ns

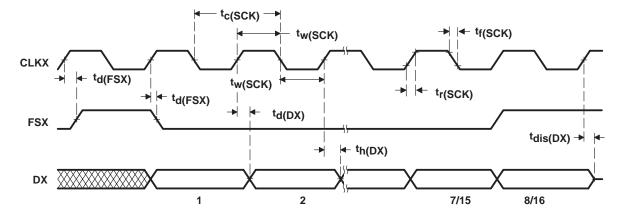


Figure 23. Serial Port Transmit Timing With Internal Clocks and Frames

buffered serial port receive timing

timing requirements over recommended operating conditions (see Figure 24)

		54 54 54	UNIT	
		MIN	MAX	
t _c (SCK)	Cycle time, serial port clock	20	†	ns
t _f (SCK)	Fall time, serial port clock		4	ns
tr(SCK)	Rise time, serial port clock		4	ns
tw(SCK)	Pulse duration, serial port clock low/high	6		ns
t _{su(BFSR)}	Setup time, BFSR before BCLKR falling edge (see Note 2)	2		ns
th(BFSR)	Hold time, BFSR after BCLKR falling edge (see Note 2)	7	tc(SCK)-2 [‡]	ns
t _{su(BDR)}	Setup time, BDR before BCLKR falling edge	0		ns
th(BDR)	Hold time, BDR after BCLKR falling edge	7		ns

[†] The serial port design is fully static and therefore can operate with t_{C(SCK)} approaching infinity. It is characterized approaching an input frequency of 0 Hz but tested at a much higher frequency to minimize test time.

NOTE 2: Timings for BCLKR and BFSR are given with polarity bits (BCLKP and BFSP) set to 0.

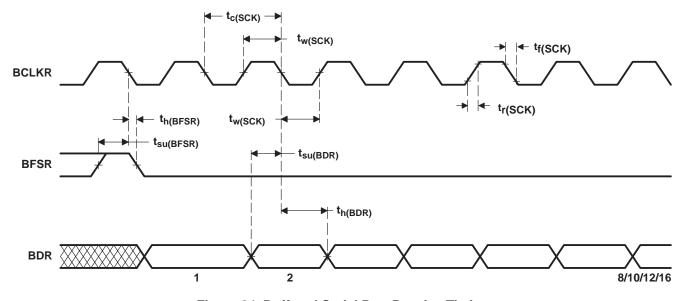


Figure 24. Buffered Serial Port Receive Timing

[‡] First bit is read when BFSR is sampled low by BCLKR clock.

buffered serial port transmit timing of external frames

switching characteristics over recommended operating conditions (see Figure 25)

	PARAMETER		549-80 549-100 549-120		
		MIN	MAX		
t _d (BDX)	Delay time, BDX valid after BCLKX rising		18	ns	
tdis(BDX)	Disable time, BDX after BCLKX rising	4	6	ns	
tdis(BDX)pcm	Disable time, PCM mode, BDX after BCLKX rising		6	ns	
ten(BDX)pcm	Enable time, PCM mode, BDX after BCLKX rising	8		ns	
th(BDX)	Hold time, BDX valid after BCLKX rising	2		ns	

timing requirements over recommended operating conditions (see Figure 25)

			549-80 549-100 549-120	
		IIM	N MAX	
t _c (SCK)	Cycle time, serial port clock	20) †	ns
tf(SCK)	Fall time, serial port clock		4	ns
tr(SCK)	Rise time, serial port clock		4	ns
tw(SCK)	Pulse duration, serial port clock low/high	(6	ns
th(BFSX)	Hold time, BFSX after CLKX falling edge (see Notes 3 and 4)	(6 t _{c(SCK)-6} ‡	ns
t _{su(BFSX)}	Setup time, FSX before CLKX falling edge (see Notes 3 and 4)	(6	ns

[†] The serial port design is fully static and therefore can operate with t_C(SCK) approaching infinity. It is characterized approaching an input frequency of 0 Hz but tested at a much higher frequency to minimize test time.

4. Timings for BCLKX and BFSX are given with polarity bits (BCLKP and BFSP) set to 0.

[‡] If BFSX does not meet this specification, the first bit of the serial data is driven on BDX until BFSX goes low (sampled on falling edge of BCLKX). After falling edge of the BFSX, data will be shifted out on the BDX pin.

NOTES: 3. Internal clock with external BFSX and vice versa are also allowable. However, BFSX timings to BCLKX always are defined depending on the source of BFSX, and BCLKX timings always are dependent upon the source of BCLKX.

buffered serial port transmit timing of external frames (continued)

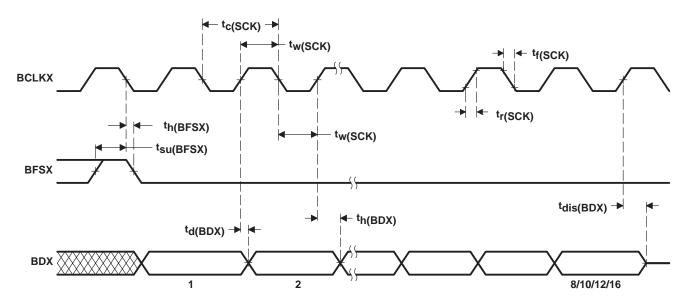


Figure 25. Buffered Serial Port Transmit Timing of External Clocks and External Frames

buffered serial port transmit timing of internal frame and internal clock

switching characteristics over recommended operating conditions [H = 0.5tc(CO)] (see Figure 26)

	PARAMETER		549-80 549-100 549-120		
		MIN	MAX		
t _c (SCK)	Cycle time, serial port clock, internal clock	20	62H	ns	
t _d (BFSX)	Delay time, BFSX after BCLKX rising edge (see Notes 3 and 4)		7	ns	
^t d(BDX)	Delay time, BDX valid after BCLKX rising edge		7	ns	
tdis(BDX)	Disable time, BDX after BCLKX rising edge	0	5	ns	
tdis(BDX)pcm	Disable time, PCM mode, BDX after BCLKX rising edge		5	ns	
ten(BDX)pcm	Enable time, PCM mode, BDX after BCLKX rising edge	7		ns	
th(BDX)	Hold time, BDX valid after BCLKX rising edge	0		ns	
t _f (SCK)	Fall time, serial port clock		3.5	ns	
tr(SCK)	Rise time, serial port clock		3.5	ns	
tw(SCK)	Pulse duration, serial port clock low/high	6		ns	

NOTES: 3. Internal clock with external BFSX and vice versa are also allowable. However, BFSX timings to BCLKX always are defined depending on the source of BFSX, and BCLKX timings always are dependent upon the source of BCLKX.

4. Timings for BCLKX and BFSX are given with polarity bits (BCLKP and BFSP) set to 0.

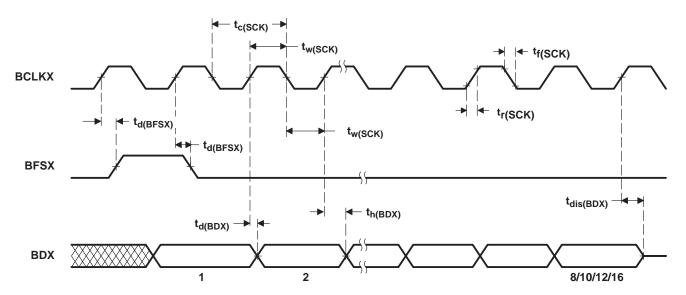


Figure 26. Buffered Serial Port Transmit Timing of Internal Clocks and Internal Frames

serial-port receive timing in TDM mode

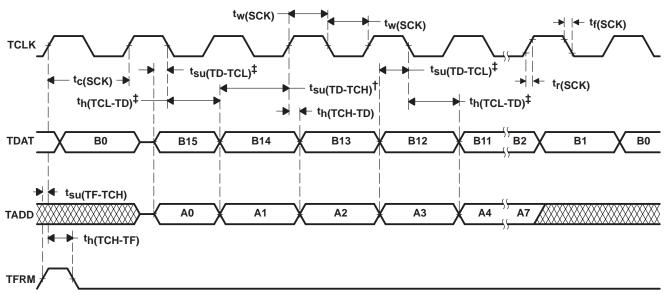
timing requirements over recommended ranges of supply voltage and operating free-air temperature [H = $0.5t_{c(CO)}$] (see Figure 27)

		549-80 549-100 549-120		UNIT
		MIN	MAX	
t _C (SCK)	Cycle time, serial-port clock	16H	†	ns
tf(SCK)	Fall time, serial-port clock		6	ns
tr(SCK)	Rise time, serial-port clock		6	ns
tw(SCK)	Pulse duration, serial-port clock low/high	8H		ns
tsu(TD-TCH)	Setup time, TDAT/TADD before TCLK rising edge	10		ns
th(TCH-TD)	Hold time, TDAT/TADD after TCLK rising edge	1		ns
t _{su(TF-TCH)}	Setup time, TFRM before TCLK rising edge‡	10		ns
th(TCH-TF)	Hold time, TFRM after TCLK rising edge‡	10		ns

[†] The serial-port design is fully static and, therefore, can operate with t_{C(SCK)} approaching infinity. It is characterized approaching an input frequency of 0 Hz but tested at a much higher frequency to minimize test time.

[‡]TFRM timing and waveforms shown in Figure 27 are for external TFRM. TFRM can also be configured as internal. The TFRM internal case is illustrated in the transmit timing diagram in Figure 28.

serial-port receive timing in TDM mode (continued)



[†] All devices except 542/543

Figure 27. Serial-Port Receive Timing in TDM Mode



^{‡542/543} only

serial-port transmit timing in TDM mode

switching characteristics over recommended operating conditions [H = $0.5t_{c(CO)}$] (see Figure 28)

	549 549- 549-	UNIT		
		MIN	MAX	
th(TCH-TDV)	Hold time, TDAT/TADD valid after TCLK rising edge, TCLK external	1		ns
th(TCH-TDV)	Hold time, TDAT/TADD valid after TCLK rising edge, TCLK internal	1		ns
	Delay time, TFRM valid after TCLK rising edge, TCLK ext [†]	H – 3 3H+22		
^t d(TCH-TFV)	Delay time, TFRM valid after TCLK rising edge, TCLK int [†]	H – 3	3H+12	ns
^t d(TC-TDV)	Delay time, TCLK to valid TDAT/TADD, TCLK ext		25	
	Delay time, TCLK to valid TDAT/TADD, TCLK int		18	ns

[†] TFRM timing and waveforms shown in Figure 28 are for internal TFRM. TFRM can also be configured as external. The TFRM external case is illustrated in the receive timing diagram in Figure 27.

serial-port transmit timing in TDM mode (continued)

timing requirements over recommended ranges of supply voltage and operating free-air temperature [H = $0.5t_{c(CO)}$] (see Figure 28)

		549-10	549-80 549-100 549-120	
		MIN	MAX	
t _c (SCK)	Cycle time, serial-port clock	16H [†]	‡	ns
tf(SCK)	Fall time, serial-port clock		6	ns
tr(SCK)	Rise time, serial-port clock		6	ns
tw(SCK)	Pulse duration, serial-port clock low/high	8H†		ns

[†] When SCK is generated internally, this value is typical.

[‡] The serial-port design is fully static and, therefore, can operate with t_C(SCK) approaching ∞. It is characterized approaching an input frequency of 0 Hz but tested as a much higher frequency to minimize test time.

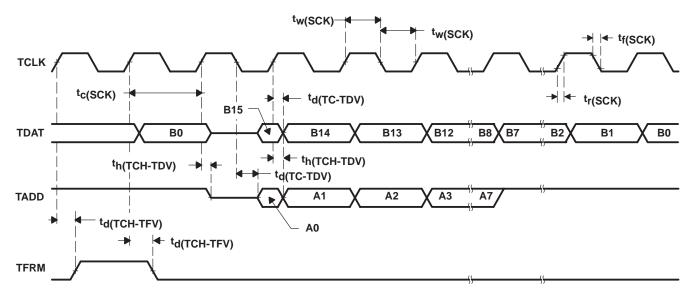


Figure 28. Serial-Port Transmit Timing in TDM Mode

host port interface timing

switching characteristics over recommended operating conditions $[H = 0.5t_{c(CO)}]$ (see Notes 5 and 6) (see Figure 29 through Figure 32)

	PARAMETER	!	UNIT		
			MIN	MAX	
td(DSL-HDV)	Delay time, DS low to HD driven	5	12	ns	
[†] d(HEL-HDV1)		Case 1: Shared-access mode if $t_W(DSH) < 7H$		7H+20-t _{w(DSH)}	
	Delay time, HDS falling to HD valid for first byte of a non-subsequent read: → max 20 ns ^{†‡}	Case 2: Shared-access mode if tw(DSH) > 7H		20	
		Case 3: Host-only mode if t _w (DSH) < 20 ns		^{40-t} w(DSH)	ns
		Case 4: Host-only mode if t _w (DSH) > 20 ns		20	
td(DSL-HDV2)	Delay time, DS low to HD valid, second byte		5‡	20	ns
td(DSH-HYH)	Delay time, DS high to HRDY high		10H+10	ns	
tsu(HDV-HYH)	Setup time, HD valid before HRDY rising edge	3H-10		ns	
th(DSH-HDV)R	Hold time, HD valid after DS rising edge, read	0	12	ns	
td(COH-HYH)	Delay time, CLKOUT rising edge to HRDY hig		10	ns	
td(DSH-HYL)	Delay time, HDS or HCS high to HRDY low		12	ns	
td(COH-HTX)	Delay time, CLKOUT rising edge to HINT char		15	ns	

[†] Host-only mode timings apply for read accesses to HPIC or HPIA, write accesses to BOB, and resetting DSPINT or HINT to 0 in shared-access mode. HRDY does not go low for these accesses.

NOTES: 5. SAM = shared-access mode, HOM = host-only mode HAD stands for HCNTRL0, HCNTRL1, and HR/W. HDS refers to either HDS1 or HDS2.

DS refers to the logical OR of HCS and HDS.

6. On host read accesses to the HPI, the setup time of HD before $\overline{\text{DS}}$ rising edge depends on the host waveforms and cannot be specified here.



[‡] Shared-access mode timings will be met automatically if HRDY is used.

host port interface timing (continued)

timing requirements over recommended operating conditions [H = $0.5t_{c(CO)}$] (see Note 7) (see Figure 29 through Figure 32)

			549-80 549-100		549-120		UNIT		
			MIN	MAX	MIN	MIN MAX			
t _{su} (HBV-DSL)	Setup time, HAD/HBIL	valid before DS or HAS falling edge	10		10		ns		
th(DSL-HBV)	Hold time, HAD/HBIL v	ralid after DS or HAS falling edge	5		5		ns		
tsu(HSL-DSL)	Setup time, HAS low be	efore DS falling edge	12		12		ns		
tw(DSL)	Pulse duration, DS low		30		30		ns		
tw(DSH)	Pulse duration, DS high	1	10		10		ns		
	Cycle time, DS rising	Case 1: HOM access timings (see Access Timing Without HRDY)	50		40				
t _C (DSH-DSH)	edge to next DS rising edge		10H		10H		ns		
t _{su(HDV-DSH)}	Setup time, HD valid be	12		12		ns			
td(DSH-HSL) [‡]	Delay time, DS high to	10H		10H		ns			
th(DSH – HDV)W	Hold time, HD valid after	3		3		ns			

[†] A host not using HRDY should meet this timing requirement all the time unless a software handshake is used to change the access rate according to the HPI mode.

 $\underline{\mathsf{HAD}}$ stands for $\underline{\mathsf{HCNTRL0}}$, $\underline{\mathsf{HCNTRL1}}$, and $\underline{\mathsf{HR}}/\overline{\mathsf{W}}$.

HDS refers to either HDS1 or HDS2.

DS refers to the logical OR of HCS and HDS.



[‡] Must only be met if HAS is going low when not accessing the HPI (as would be the case where multiple devices are being driven by one host). NOTE 7: SAM = shared-access mode, HOM = host-only mode

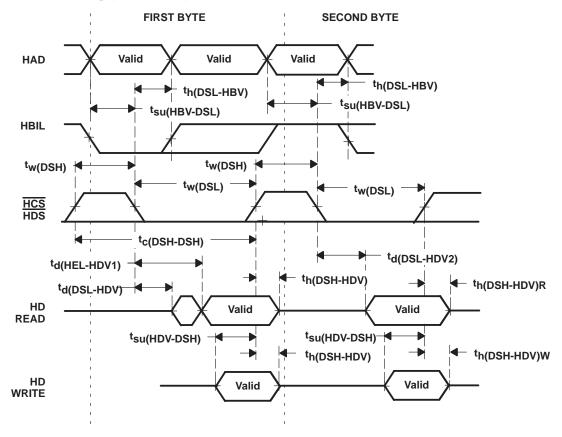


Figure 29. Read/Write Access Timings Without HRDY or HAS

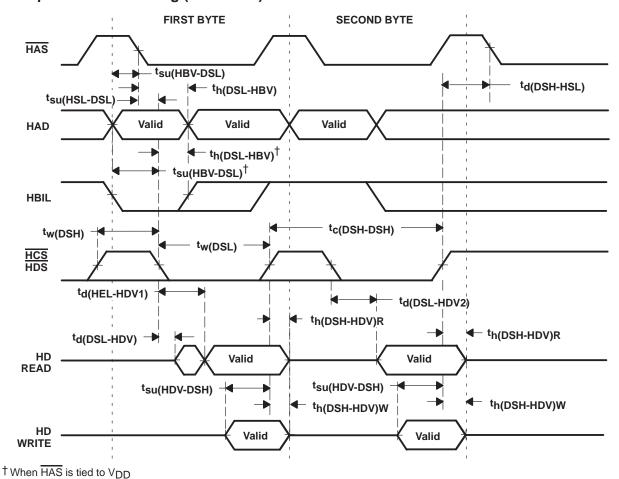


Figure 30. Read/Write Access Timings Using HAS Without HRDY

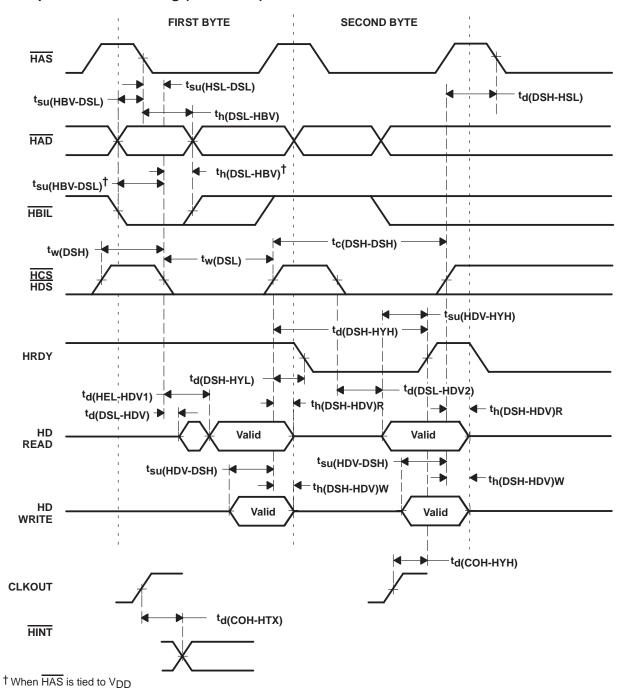


Figure 31. Read/Write Access Timing With HRDY

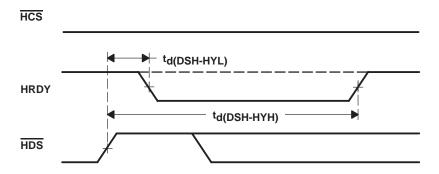


Figure 32. HRDY Signal When $\overline{\text{HCS}}$ is Always Low

MECHANICAL DATA

The following tables show the thermal resistance characteristics for the PGE (PQFP) and GGU (PBGA) mechanical packages.

Thermal Resistance Characteristics for PGE

PARAMETER	°C/W			
$R_{\Theta JA}$	56			
R _⊖ JC	5			

Thermal Resistance Characteristics for GGU

PARAMETER	°C/W
R_{\ThetaJA}	38
R _O JC	5

The following mechanical package diagram(s) reflect the most up-to-date mechanical data released for these designated device(s).

2-Apr-2012

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
TMS320VC549GGU-100	ACTIVE	BGA MICROSTAR	GGU	144	160	TBD	SNPB	Level-3-220C-168 HR	
TMS320VC549GGU-120	OBSOLETE	BGA MICROSTAR	GGU	144		TBD	Call TI	Call TI	
TMS320VC549GGU-80	ACTIVE	BGA MICROSTAR	GGU	144	160	TBD	SNPB	Level-3-220C-168 HR	
TMS320VC549GGUR-80	ACTIVE	BGA MICROSTAR	GGU	144	1000	TBD	SNPB	Level-3-220C-168 HR	
TMS320VC549GGUR100	OBSOLETE	BGA MICROSTAR	GGU	144		TBD	Call TI	Call TI	
TMS320VC549PGE-100	ACTIVE	LQFP	PGE	144	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TMS320VC549PGE-120	ACTIVE	LQFP	PGE	144	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TMS320VC549PGE-80	ACTIVE	LQFP	PGE	144	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TMS320VC549PGE100W	OBSOLETE	LQFP	PGE	144		TBD	Call TI	Call TI	
TMS320VC549PGER-80	OBSOLETE	LQFP	PGE	144		TBD	Call TI	Call TI	
TMS320VC549PGER100	ACTIVE	LQFP	PGE	144	500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TMS320VC549ZGU-100	OBSOLETE	BGA MICROSTAR	ZGU	144		TBD	Call TI	Call TI	
TMS320VC549ZGU-120	ACTIVE	BGA MICROSTAR	ZGU	144	160	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	
TMS32VC549PGE100G4	ACTIVE	LQFP	PGE	144	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.



PACKAGE OPTION ADDENDUM

2-Apr-2012

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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GGU (S-PBGA-N144)

PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice

C. MicroStar BGA™ configuration

MicroStar BGA is a trademark of Texas Instruments Incorporated.



PGE (S-PQFP-G144)

PLASTIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-026

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