



SLLS668C-FEBRUARY 2006-REVISED JULY 2008

5-V FULL-DUPLEX RS-485/RS-422 DRIVER AND BALANCED RECEIVER

FEATURES

- Designed for INTERBUS Applications
- Balanced Receiver Thresholds
- 1/2 Unit-Load (up to 64 nodes on the bus)
- Bus-Pin ESD Protection 15 kV HBM
- Bus-Fault Protection of –7V to 12V
- Thermal Shutdown Protection
- Power-Up/Down Glitch-free Bus Inputs and Outputs
- Designed for RS-422 and RS-485 Networks

APPLICATIONS

- Digital Motor Control
- Utility Meters
- Chassis-to-Chassis Interconnections
- Electronic Security Stations
- Industrial, Process, and Building Automation
- Point-of-Sale (POS) Terminals and Networks
- DTE/DCE Interfaces

DESCRIPTION

The SN65HVD179 is a differential line driver and differential-input line receiver that operates with a 5-V power supply. Each driver and receiver has separate input and output pins for full-duplex bus communication designs. They are designed for balanced transmission lines and interoperation with ANSI TIA/EIA-485A, TIA/EIA-422-B, ITU-T v.11, and ISO 8482:1993 standard-compliant devices.

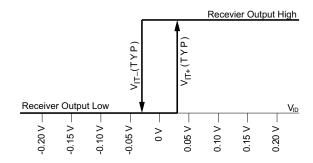
The differential bus driver and receiver are monolithic, integrated circuits designed for full-duplex bi-directional data communication on multipoint bus-transmission lines at signaling rates⁽¹⁾ up to 25 Mbps. The SN65HVD179 is fully enabled with no external enabling pins.

The 1/2 unit load receiver has a high receiver input resistance. This results in lower bus leakage currents over the common-mode voltage range, and reduces the total amount of current that a 485 driver is forced to source or sink when transmitting.

The balanced differential receiver input threshold makes the SN65HVD179 fully compatible with fieldbus requirements that define an external failsafe structure.

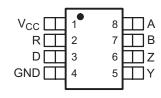
 The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

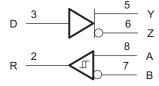
BALANCED RECEIVER INPUT THRESHOLDS



SN65HVD179

D PACKAGE (TOP VIEW)







Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE OPTIONS

SIGNALING RATE	UNIT LOADS	BASE PART NUMBER	SOIC MARKING
25 Mbps	1/2	SN65HVD179	SN65HVD179

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1) (2)

		UNIT
V _{CC}	Supply voltage range	–0.3 V to 6 V
V_A , V_B , V_Y , V_Z	Voltage range at any bus terminal (A, B, Y, Z)	–9 V to 14 V
V _{TRANS}	Voltage input, transient pulse through 100 Ω. See Figure 8 (A, B, Y, Z) (3)	-50 to 50 V
VI	Voltage input range (D, DE, RE)	–0.5 V to 7 V
P _{CONT}	Continuous total power dissipation	Internally limited (4)
Io	Output current (receiver output only, R)	11 mA

⁽¹⁾ Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			1	MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage			4.5		5.5	V
V _I or V _{IC}	Voltage at any bus terminal	(separately or common mode)	_	-7 ⁽¹⁾		12	V
1/t _{UI}	Signaling rate					25	Mbps
R _L	Differential load resistance			54	60		Ω
V _{IH}	High-level input voltage	D		2		V_{CC}	
V _{IL}	Low-level input voltage	D		0		8.0	V
V _{ID}	Differential input voltage			-12		12	
	Lligh lovel output ourrent	Driver		-60			A
ІОН	High-level output current	Receiver		-8			mA
	Low lovel output ourrent	Driver				60	A
I _{OL}	Low-level output current	Receiver				8	mA
TJ	Junction temperature (2)			-40		150	°C

The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

ELECTROSTATIC DISCHARGE PROTECTION

PARAMETER	TEST CONDITIONS	MIN TYP ⁽¹⁾	MAX	UNIT
Human body model	Bus terminals and GND	±16		
Human body model ⁽²⁾	All pins	±4		kV
Charged-device-model (3)	All pins	±1		

All typical values at 25°C and with a 5-V supply. Tested in accordance with JEDEC Standard 22, Test Method A114-A.

Tested in accordance with JEDEC Standard 22, Test Method C101.

Submit Documentation Feedback

All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

This tests survivability only and the output state of the receiver is not specified.

The Thermal shutdown of this device internally limits the continuous total power dissipation. Thermal shutdown typically occurs when the junction temperature reaches 165°C.

See thermal characteristics table for information regarding this specification.

www.ti.com

DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

	PARAMETER		TEST C	CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{I(K)}	Input clamp voltage		I _I = -18 mA	-1.5				
			I _O = 0		4		V_{CC}	
IV/ I	Steady-state differential	output voltage	$R_L = 54 \Omega$, See Fig	ure 1 (RS-485)	1.7	2.6		
$ V_{OD(SS)} $	Steady-State differential	output voltage	$R_L = 100 \Omega$, See Fi	gure 1 (RS-422)	2.4	3.2		V
			$V_{\text{test}} = -7 \text{ V to } 12 \text{ V}$, See Figure 2	1.6			
$\Delta V_{OD(SS)} $	Change in magnitude of differential output voltage		$R_L = 54 \Omega$, See Fig	ure 1 and Figure 2	-0.2		0.2	
V _{OD(RING)}	Differential Output Voltagundershoot	ge overshoot and	$R_L = 54 \Omega, C_L = 50$ Figure 3 for definition	pF, See Figure 5 and on			10% ⁽²⁾	
V _{OC(PP)}	Peak-to-peak common-r	node output voltage			0.5			
V _{OC(SS)}	Steady-state common-m	node output voltage	See Figure 4		2.2		3.3	V
$\Delta V_{OC(SS)}$	Change in steady-state output voltage	common-mode	Coo riguro r		-0.1		0.1	·
$I_{Z(Z)}$ or	I limb immediance atota a		$V_{CC} = 0 \text{ V}, V_Z \text{ or } V_Y$ Other input at 0 V	_/ = 12 V,			90	^
$I_{Y(Z)}$	High-impedance state or	utput current	$V_{CC} = 0 \text{ V}, V_Z \text{ or } V_Y$ Other input at 0 V	$V_{CC} = 0 \text{ V}, V_{Z} \text{ or } V_{Y} = -7 \text{ V},$ Other input at 0 V				μΑ
I _{Z(S)} or	Chart Circuit autout aure	0::		Other input	-250		250	mA
I _{Y(S)}	Short Circuit output curre	ent	V_Z or $V_Y = 12 \text{ V}$ at 0 V		-250		250	mA
I _I	Input current	$V_{I} = 0, V_{I} = 2$			0		100	μΑ
C _(OD)	Differential output capac	citance				16		pF

DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

	PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t _{PLH}	Propagation delay time, low-to-high-level output		4	0	12	no
t_{PHL}	Propagation delay time, high-to-low-level output	$R_L = 54 \Omega, C_L = 50 pF,$	4	0	12	ns
t _r	Differential output signal rise time	See Figure 5	2	6	10	no
t _f	Differential output signal fall time		3	6	12	ns
t _{sk(p)}	Pulse skew (t _{PHL} - t _{PLH})			1.4		ns
t _{sk(pp)} (2)	Part-to-part skew			1		ns

Copyright © 2006-2008, Texas Instruments Incorporated

Submit Documentation Feedback

⁽¹⁾ All typical values are at 25°C and with a 5-V supply.
(2) 10% of the peak-to-peak Differential Output voltage swing, per TIA/EIA-485.

Under some conditions of short-circuit to negative voltages, output currents exceeding the ANSI TIA/EIA-485-A maximum current of 250 mA may occur. Continuous exposure may affect device reliability.

All typical values are at 25°C and with a 5-V supply. $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.



RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

	PARAMETER	TEST COND	ITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{IT+}	Positive-going differential input threshold voltage	$I_O = -8 \text{ mA}$	I _O = -8 mA			0.2	V
V _{IT-}	Negative-going differential input threshold voltage	I _O = 8 mA	I _O = 8 mA				V
V _{hys}	Hysteresis voltage (V _{IT+} – V _{IT-})				50		mV
V	Output voltage	V_{ID} = 200 mV, I_{O} = -8 mA, See Figure 6		4.0			V
Vo	Output voltage	$V_{ID} = -200 \text{ mV}, I_{O} = 8 \text{ mA}, Se$	ee Figure 6			0.3	V
		V_A or $V_B = 12 V$			0.20	0.3	
11	Due input compant	V_A or $V_B = 12 \text{ V}$, $V_{CC} = 0 \text{ V}$	Other input		0.24	0.4	A
I _A or I _B	Bus input current	$V_A \text{ or } V_B = -7 \text{ V}$ at 0 V		-0.35	-0.19		mA
		V_A or $V_B = -7$ V, $V_{CC} = 0$ V		-0.25	-0.14		
I _{CC}	Supply current	D at 0 V or V _{CC} and No Load				2.7	mA

⁽¹⁾ All typical values are at 25°C and with a 5-V supply.

RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

	PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t _{PLH}	Propagation delay time, low-to-high-level output			24	40	
t _{PHL}	Propagation delay time, high-to-low-level output	$V_{l} = 0 \text{ V to } 3 \text{ V, } C_{L} = 15 \text{ pF,}$ See Figure 7		24	40	ns
t _{sk(p)}	Pulse skew (t _{PHL} - t _{PLH})	Goo i igaio i			5	
$t_{sk(pp)}^{(2)}$	Part-to-part skew			5		ns
t _r	Output signal rise time	C - 15 pF See Figure 7		2	4	ns
t _f	Output signal fall time	C _L = 15 pF, See Figure 7		2	4	ns

Submit Documentation Feedback

 ⁽¹⁾ All typical values are at 25°C and with a 5-V supply
 (2) t_{sk(pp)} is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

www.ti.com

THERMAL CHARACTERISTICS

over operating free-air temperature range unless otherwise noted (1)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
0	Junction-to-ambient thermal resistance ⁽²⁾	Low-K board ⁽³⁾ , No airflow		230.8		°C/W
θ_{JA}	Junction-to-ambient thermal resistance	High-K board ⁽⁴⁾ , No airflow		135.1		C/VV
θ_{JB}	Junction-to-board thermal resistance	High-K board		44.4		°C/W
θ_{JC}	Junction-to-case thermal resistance	No board		43.5		°C/W
P_D	Device power dissipation	R_L = 60 Ω , C_L = 50 pF, Input to D a 50% duty cycle square wave at indicated signaling rate			420	mW
_	Ambient eintemperature	Low-K board, No airflow	-40		55	°C
T _A	Ambient air temperature	High-K board, No airflow	-40		85	C
T_{JSD}	Thermal shutdown junction temperature			165		°C

- (1) See Application Information section for an explanation of these parameters.
- (2) The intent of θ_{JA} specification is solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment.
- (3) In accordance with the Low-K thermal metric definitions of EIA/JESD51-3.
- (4) In accordance with the High-K thermal metric definitions of EIA/JESD51-7.

PARAMETER MEASUREMENT INFORMATION

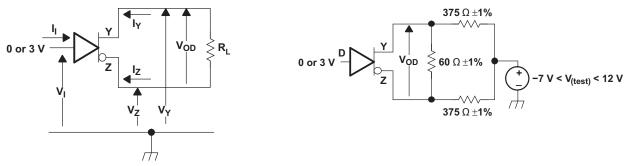


Figure 1. Driver V_{OD} Test Circuit: Voltage and Current Definitions

Figure 2. Driver V_{OD} With Common-Mode Loading Test

VOD(RING) is measured at four points on the output waveform, corresponding to overshoot and undershoot from the VOD(H) and VOD(L) steady state values.

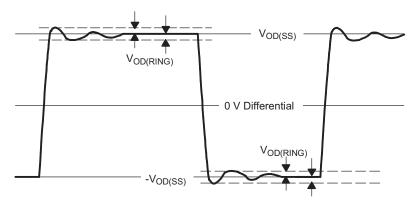
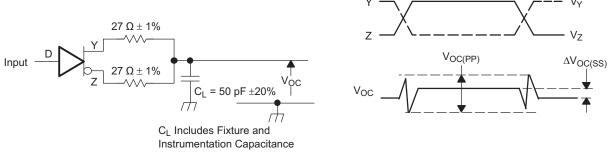


Figure 3. V_{OD(RING)} Waveform and Definitions

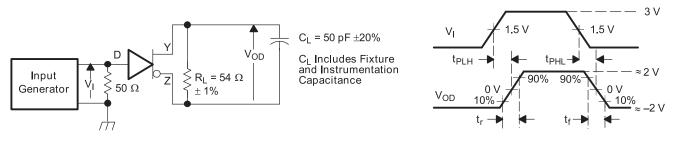


PARAMETER MEASUREMENT INFORMATION (continued)



Input: PRR = 500 kHz, 50% Duty Cycle,t $_r$ <6ns, t_f <6ns, Z_O = 50 Ω

Figure 4. Test Circuit and Definitions for the Driver Common-Mode Output Voltage



Generator: PRR = 500 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_0 = 50 Ω

Figure 5. Driver Switching Test Circuit and Voltage Waveforms

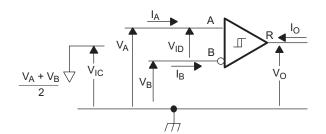


Figure 6. Receiver Voltage and Current Definitions

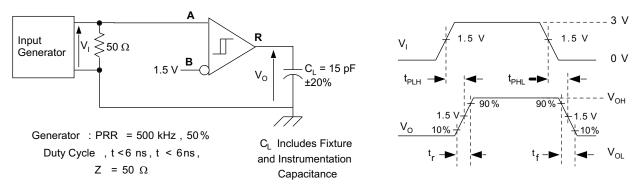


Figure 7. Receiver Switching Test Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION (continued)

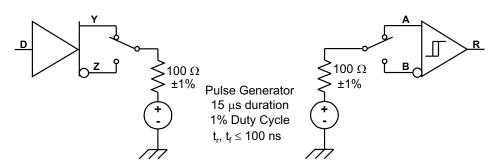


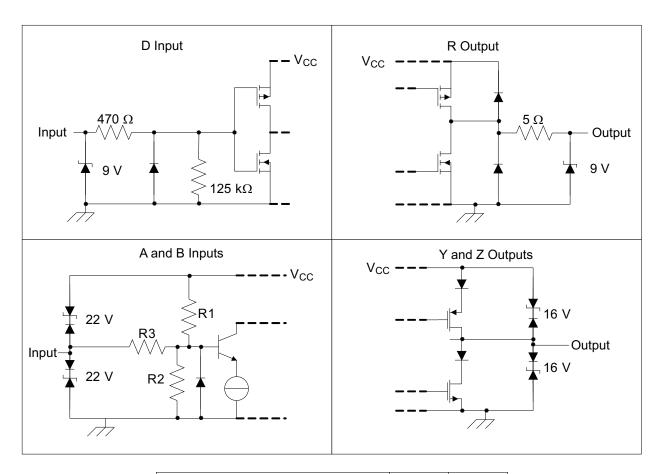
Figure 8. Test Circuit, Transient Overvoltage Test

FUNCTION TABLES

DRIVER			RECEIVER			
INPUT	OUT	PUTS	DIFFERENTIAL INPUTS	OUTPUTS		
D	Y	Z	$V_{ID} = V_A - V_B$	R		
Н	Н	L	V _{ID} ≤ -0.2 V	L		
L	L	Н	$-0.2 \text{ V} < \text{V}_{\text{ID}} < 0.2 \text{ V}$?		
Open	L	Н	0.2 V ≤ V _{ID}	Н		



EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



	R1/R2	R3
SN65HVD179	9 kΩ	45 kΩ



TYPICAL CHARACTERISTICS

RMS SUPPLY CURRENT vs SIGNALING RATE

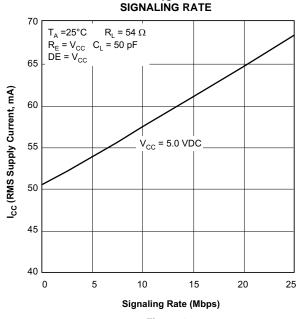


Figure 9.

BUS INPUT CURRENT VS INPUT VOLTAGE

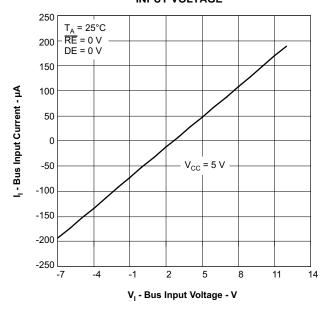


Figure 10.

DRIVER LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

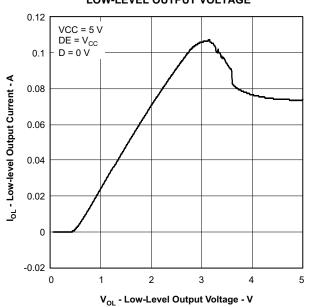
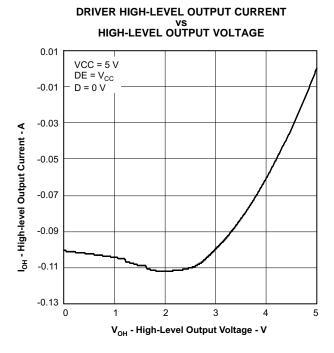


Figure 11.



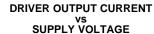
TYPICAL CHARACTERISTICS (continued)



DRIVER DIFFERENTIAL OUTPUT VOLTAGE VS FREE-AIR TEMPERATURE 2.9 V_{cc} = 5 V DE at V_{cc} D at V_{cc} D at V_{cc} 2.7 2.8 T_A - Free-Air Temperature - °C

Figure 12.

Figure 13.



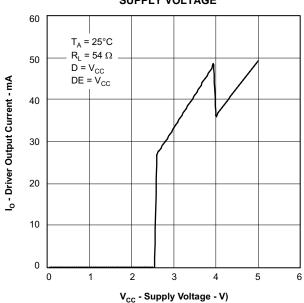


Figure 14.



APPLICATION INFORMATION

THERMAL CHARACTERISTICS OF IC PACKAGES

 θ_{JA} (Junction-to-Ambient Thermal Resistance) is defined as the difference in junction temperature to ambient temperature divided by the operating power.

 θ_{JA} is not a constant and is a strong function of:

- the PCB design (50% variation)
- altitude (20% variation)
- device power (5% variation)

 θ_{JA} can be used to compare the thermal performance of packages if the specific test conditions are defined and used. Standardized testing includes specification of PCB construction, test chamber volume, sensor locations, and the thermal characteristics of holding fixtures. θ_{JA} is often misused when it is used to calculate junction temperatures for other installations.

TI uses two test PCBs as defined by JEDEC specifications. The low-K board gives *average* in-use condition thermal performance, and it consists of a single copper trace layer 25 mm long and 2-oz thick. The high-K board gives best *case* in-use condition, and it consists of two 1-oz buried power planes with a single copper trace layer 25 mm long and 2-oz thick. A 4% to 50% difference in θ_{JA} can be measured between these two test cards

 θ_{JC} (Junction-to-Case Thermal Resistance) is defined as difference in junction temperature to case divided by the operating power. It is measured by putting the mounted package up against a copper block cold plate to force heat to flow from die, through the mold compound into the copper block.

 θ_{JC} is a useful thermal characteristic when a heatsink applied to package. It is *not* a useful characteristic to predict junction temperature because it provides pessimistic numbers if the case temperature is measured in a nonstandard system and junction temperatures are backed out. It can be used with θ_{JB} in 1-dimensional thermal simulation of a package system.

 θ_{JB} (Junction-to-Board Thermal Resistance) is defined as the difference in the junction temperature and the PCB temperature at the center of the package (closest to the die) when the PCB is clamped in a cold-plate structure. θ_{JB} is only defined for the high-K test card.

 θ_{JB} provides an overall thermal resistance between the die and the PCB. It includes a bit of the PCB thermal resistance (especially for BGA's with thermal balls) and can be used for simple 1-dimensional network analysis of package system, see Figure 15.

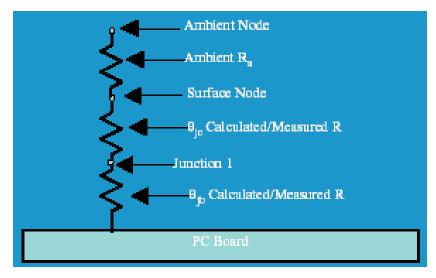


Figure 15. Thermal Resistance





om 21-Aug-2008

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN65HVD179D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD179DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD179DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD179DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

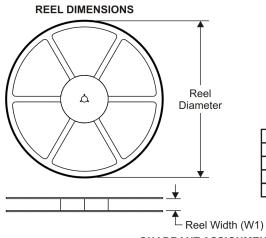
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

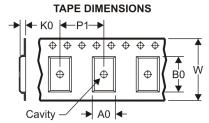
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

tti.com 15-Jul-2008

TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device		Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD179DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1





*All dimensions are nominal

	Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
I	SN65HVD179DR	SOIC	D	8	2500	346.0	346.0	29.0

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.



D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Audio	www.ti.com/audio	Communications and Telecom	www.ti.com/communications
Amplifiers	amplifier.ti.com	Computers and Peripherals	www.ti.com/computers
Data Converters	dataconverter.ti.com	Consumer Electronics	www.ti.com/consumer-apps
DLP® Products	www.dlp.com	Energy and Lighting	www.ti.com/energy
DSP	dsp.ti.com	Industrial	www.ti.com/industrial
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Security	www.ti.com/security
Logic	logic.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Power Mgmt	power.ti.com	Transportation and Automotive	www.ti.com/automotive
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com	Wireless	www.ti.com/wireless-apps
RF/IF and ZigBee® Solutions	www.ti.com/lprf		

TI E2E Community Home Page

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2011, Texas Instruments Incorporated

e2e.ti.com