

70-V Fault-Protected RS-485 Transceiver With Cable Invert

FEATURES

www.ti.com

- Bus-Pin Fault Protection to > ±70 V
- Cable Invert Function Allows Correction for Reversed Bus Pins
- Common-Mode Voltage Range (–20 V to 25 V) More Than Doubles TIA/EIA 485 Requirement
- Bus I/O Protection
 - ±16 kV JEDEC HBM Protection
- Reduced Unit Load for Up to 256 Nodes

- Failsafe Receiver for Open-Circuit, Short-Circuit and Idle-Bus Conditions
- Low Power Consumption
 I_{CC} 5 mA Quiescent During Operation
- Power-Up, Power-Down Glitch-Free Operation

APPLICATIONS

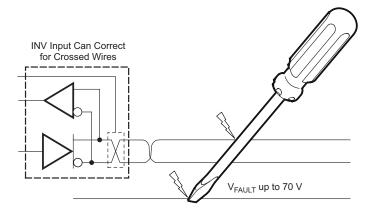
Designed for RS-485 and RS-422 Networks

DESCRIPTION

These devices are designed to survive overvoltage faults such as direct shorts to power supplies, mis-wiring faults, connector failures, cable crushes, and tool mis-applications. They are also robust to ESD events, with high levels of protection to human-body model specifications.

These devices combine a differential driver and a differential receiver, which operate from a single power supply. The driver differential outputs and the receiver differential inputs are connected internally to for a bus port suitable for half-duplex (two-wire bus) communication. A cable invert pin (INV) allows active correction of mis-wires that may occur during installation. Upon detecting communication errors, the user can apply a logic HIGH to the INV pin, effectively inverting the polarity of the differential bus port, thereby correcting for the reversed bus wires.

These devices feature a wide common-mode voltage range, making them suitable for multi-point applications over long cable runs. These devices are characterized from –40°C to 105°C.



PRODUCT SELECTION GUIDE

PART NUMBER	DUPLEX	SIGNALING RATE	NODES	CABLE LENGTH
SN65HVD1794	Half	115 kbps	Up to 256	1500 m
SN65HVD1795 PREVIEW	Half	1 Mbps	Up to 256	150 m
SN65HVD1796 PREVIEW	Half	10 Mbps	Up to 64	50 m

For similar features with 3.3 V supply operation, see the SN65HVD1781 (SLLS877).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SN65HVD1794, SN65HVD1795 SN65HVD1796



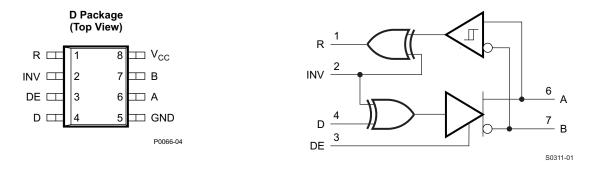
www.ti.com

SLLS935-AUGUST 2008



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DEVICE INFORMATION





INPUT	ENABLE	INVERT	OUT	PUTS	
D	DE	INV	Α	В	
Н	Н	L	Н	L	Actively drive normal bus High
L	Н	L	L	Н	Actively drive normal bus Low
Н	Н	Н	L H		Actively drive inverted bus High (drive normal bus Low)
L	Н	Н	Н	L	Actively drive inverrted bus Low (drive normal bus High)
Х	L	Х	Z	Z	Driver disabled
Х	OPEN	Х	Z	Z	Driver disabled by default
OPEN	Н	L	Н	L	Actively drive bus High by default
OPEN	Н	Н	L H		Actively drive bus Low by default (inverted cable)

DRIVER FUNCTION TABLE

RECEIVER FUNCTION TABLE

DIFFERENTIAL INPUT	INVERT	OUTPUT	
$V_{ID} = V_A - V_B$	INV	R	
V -V	L or OPEN	Н	Receive valid bus High
$V_{IT+} < V_{ID}$	Н	L	Receive inverted bus Low
$V_{IT-} < V_{ID} < V_{IT+}$	х	?	Indeterminate bus state
V -V	L or OPEN	L	Receive valid bus Low
$V_{ID} < V_{IT-}$	Н	Н	Receive inverted bus High
Open circuit hue	L or OPEN	Н	Fail-safe high output
Open-circuit bus	Н	L	Failsafe inverted output
Short-circuit bus	L or OPEN	Н	Fail-safe high output
Short-circuit bus	Н	L	Failsafe inverted output
Idle (terminated) bus	L or OPEN	Н	Fail-safe high output
Idle (terminated) bus	h	L	Failsafe inverted output

2

Copyright © 2008, Texas Instruments Incorporated



SLLS935-AUGUST 2008

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

		VALUE	UNIT
V_{CC}	Supply voltage	–0.5 to 7	V
	Voltage range at A and B pins	-70 to 70	V
	Input voltage range at any logic pin	-0.3 to V _{CC} + 0.3	V
	Voltage input range, transient pulse, A and B, through 100 Ω	-100 to 100	V
	Receiver output current	-24 to 24	mA
TJ	Junction temperature	170	°C
	Continuous total power dissipation	See Dissipation Rating Table	
	IEC 60749-26 ESD (human-body model), bus terminals and GND	±16	kV
	JEDEC Standard 22, Test Method A114 (human-body model), bus terminals and GND	±16	kV
	JEDEC Standard 22, Test Method A114 (human-body model), all pins	±4	kV
	JEDEC Standard 22, Test Method C101 (charged-device model), all pins	±2	kV
	JEDEC Standard 22, Test Method A115 (machine model), all pins	±400	V

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

PACKAGE DISSIPATION RATINGS

PACKAGE	JEDEC THERMAL MODEL	T _A < 25°C RATING	DERATING FACTOR ABOVE T _A = 25°C	T _A = 85°C RATING	T _A = 105°C RATING
	High-K	905 mW	7.25 mW/°C	470 mW	325 mW
SOIC (D) 8-pin	Low-K	516 mW	4.1 mW/°C	268 mW	186 mW
PDIP (P) 8-pin	High-K	2119 mW	16.9 mW/°C	1100 mW	763 mW
	Low-K	976 mW	7.8 mW/°C	508 mW	352 mW

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage		4.5	5	5.5	V
VI	Input voltage at	Input voltage at any bus terminal (separately or common mode) ⁽¹⁾			25	V
VIH	High-level input	voltage (driver, driver enable, and invert inputs)	2		V _{CC}	V
V _{IL}	Low-level input	voltage (driver, driver enable, and invert inputs)	0		0.8	V
V _{ID}	Differential input	voltage	-25		25	V
	Output current, driver		-60		60	mA
I _O	Output current, receiver				8	mA
RL	Differential load	resistance	54	60		Ω
CL	Differential load	capacitance		50		pF
		HVD1794			115	kbps
1/t _{UI}	Signaling rate	HVD1795			1	N.d
		HVD1796			10	Mbps
T _A	Operating free-air temperature (See application section for thermal information)		-40		105	°C
TJ	Junction temper	unction temperature				°C

(1) By convention, the least positive (most negative) limit is designated as minimum in this data sheet.



SLLS935-AUGUST 2008

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CO	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V _{od}	Driver differential output voltage magnitude	RS-485 with common-mode load, $V_{CC} > 4.75$ V, see Figure 2	$T_A \le 85^\circ$ $T_A \le 10^\circ$		1.5 1.4			V
		$R_{L} = 54 \Omega, 4.75 V \le V$	 _{CC} ≤ 5.25	V	1.5	2		
		R _L = 100 Ω, 4.75 V ≤ V	V _{CC} ≤ 5.2	5 V	2	2.5		
Δ V _{OD}	Change in magnitude of driver differential output voltage	R _L = 54 Ω			-0.2	0	0.2	V
V _{OC(SS)}	Steady-state common-mode output voltage				1	V _{CC} /2	3	V
ΔV _{OC}	Change in differential driver output common-mode voltage				-100	0	100	mV
V _{OC(PP)}	Peak-to-peak driver common-mode output voltage	Center of two 27-Ω loa Figure 3	ad resisto	rs, See		500		mV
C _{OD}	Differential output capacitance				23		pF	
V _{IT+}	Positive-going receiver differential input voltage threshold					-100	-10	mV
V _{IT-}	Negative-going receiver differential input voltage threshold	$V_{CM} = -20 V \text{ to } 25 V$			-200	-150		mV
V _{HYS}	Receiver differential input voltage threshold hysteresis $(V_{IT+} - V_{IT-})$				30	50		mV
V _{OH}	Receiver high-level output voltage	I _{OH} = -8 mA			2.4	V _{CC} - 0.3		V
\/	Paggiver low lovel output veltage	L _ 9 m 4	T _A ≤ 85°	°C		0.2	0.4	V
V _{OL}	Receiver low-level output voltage	I _{OL} = 8 mA	T _A ≤ 105	5°C		0.2	0.5	v
I	Driver input, driver enable, and invert input current				-100		100	μA
l _{os}	Driver short-circuit output current				-250		250	mA
			94, 95	V _I = 12 V		75	125	
I,	Bus input current (disabled driver)	V_{CC} = 4.5 to 5.5 V or	54, 55	$V_I = -7 V$	-100	-40		μA
.1		V_{CC} = 0 V, DE at 0 V	96	V _I = 12 V			500	μΛ
				$V_I = -7 V$	-400			
Icc	Supply current (quiescent)	Driver enabled	DE = 5∖	DE = 5V		4	6	mA
		Driver disabled	DE = GI	ND		2	4	
	Supply current (dynamic)	See TYPICAL CHARA	CTERIS	FICS section				



SLLS935-AUGUST 2008

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST CONDITION	IS	MIN	TYP	MAX	UNIT
DRIVER (H)	/D1794)						
t _r , t _f	Driver differential output rise/fall time			0.4	1.7	2.6	μs
t _{PHL} , t _{PLH}	Driver propagation delay	$R_{\rm L} = 54 \ \Omega, C_{\rm L} = 50 \ pF, See F$	Figure 4		0.8	2	μs
t _{SK(P)}	Driver differential output pulse skew, $ t_{PHL} - t_{PLH} $		igure 4		20	250	ns
t _{PHZ} , t _{PLZ}	Driver disable time	See Figure 5 and Figure 6			0.1	5	μs
t _{PZH} , t _{PZL}	Driver enable time				0.2	3	μs
DRIVER (H)	/D1795)						
t _r , t _f	Driver differential output rise/fall time			50		300	ns
t _{PHL} , t _{PLH}	Driver propagation delay	R _L = 54 Ω, C _L = 50 pF, See I	Figure 4			200	ns
t _{SK(P)}	Driver differential output pulse skew, t _{PHL} – t _{PLH}	$1 = 14 \Omega, C_1 = 10 \text{ pr}, 366 \text{ Figure 4}$				25	ns
t _{PHZ} , t _{PLZ}	Driver disable time	See Figure 5 and Figure 6	See Figure 5 and Figure 6			3	μs
t _{PZH} , t _{PZL}	Driver enable time					500	ns
DRIVER (H)	/D1796)						
t _r , t _f	Driver differential output rise/fall time			3		30	ns
t _{PHL} , t _{PLH}	Driver propagation delay	R _I = 54 Ω, C _I = 50 pF, See F				50	ns
t _{SK(P)}	Driver differential output pulse skew, t _{PHL} – t _{PLH}		igure 4			10	ns
t _{PHZ} , t _{PLZ}	Driver disable time	See Figure 5 and Figure 6				3	μs
t _{PZH} , t _{PZL}	Driver enable time		_			500	ns
RECEIVER	(ALL DEVICES UNLESS OTHERWISE NOT	ED)					
t _r , t _f	Receiver output rise/fall time				4	15	ns
			94, 95		100	200	
t _{PHL} , t _{PLH}	Receiver propagation delay time	$C_L = 15 \text{ pF}$, See Figure 7	96			70	ns
	Receiver output pulse skew,		94, 95		6	20	
t _{SK(P)}	t _{PHL} - t _{PLH}		96			5	ns

5

Product Folder Link(s): SN65HVD1794, SN65HVD1795 SN65HVD1796

SN65HVD1794, SN65HVD1795 SN65HVD1796

SLLS935-AUGUST 2008

THERMAL INFORMATION

Texas

INSTRUMENTS

www.ti.com

PARAMETER		TEST CONDITIONS	VALUE	UNIT	
	SOIC-8	JEDEC high-K model	138		
		JEDIC low-K model	242	0 0 0 0 0	
$R_{\theta JA}$ Junction-to-ambient thermal resistance (no airflow) DIP-8	JEDEC high-K model	59	°C/W	
	DIP-6	JEDIC low-K model	128		
D lunction to board thermal resistance	SOIC-8		62	°C/W	
$R_{\theta JB}$ Junction-to-board thermal resistance	DIP-8		39	°C/VV	
D lunction to cope thermal registerion	SOIC-8		61	°C/W	
$R_{\theta JC}$ Junction-to-case thermal resistance	DIP-8		61	°C/W	
	94	$ \begin{array}{l} V_{CC} = 5.5 \; V, \; T_{J} = 150^\circ C, \; R_{L} = 300 \; \Omega, \\ C_{L} = 50 \; pF \; (driver), \; C_{L} = 15 \; pF \; (receiver) \\ \text{5-V supply, unterminated}^{(1)} \end{array} $	290		
	94	$V_{CC} = 5.5 \text{ V}, \text{ T}_{\text{J}} = 150^{\circ}\text{C}, \text{ R}_{\text{L}} = 100 \Omega,$			
P _D Power dissipation	95	$C_{L} = 50 \text{ pF} (\text{driver}), C_{L} = 15 \text{ pF} (\text{receiver})$ 5-V supply, RS-422 load ⁽¹⁾	320	mW	
	96			11100	
	94	$V_{CC} = 5.5 \text{ V}, \text{ T}_{\text{J}} = 150^{\circ}\text{C}, \text{ R}_{\text{L}} = 54 \Omega,$	400		
	95	C _L = 50 pF (driver), C _L = 15 pF (receiver) 5-V supply, RS-485 load ⁽¹⁾			
	96				
T _{SD} Thermal-shutdown junction temperature			170	°C	

(1) Driver enabled, 50% duty cycle square-wave signal at signaling rate: 115 kbps for HVD1794, 1 Mbps for HVD1795, 10 Mbps for HVD1796

PARAMETER MEASUREMENT INFORMATION

Input generator rate is 100 kbps, 50% duty cycle, rise and fall times less than 6 nsec, output impedance 50 Ω.

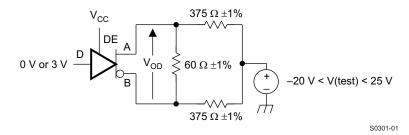


Figure 2. Measurement of Driver Differential Output Voltage With Common-Mode Load

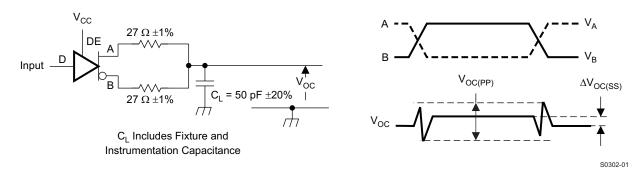


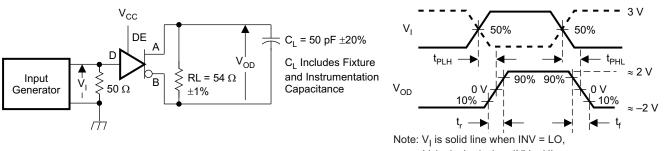
Figure 3. Measurement of Driver Differential and Common-Mode Output With RS-485 Load



SN65HVD1794, SN65HVD1795 SN65HVD1796

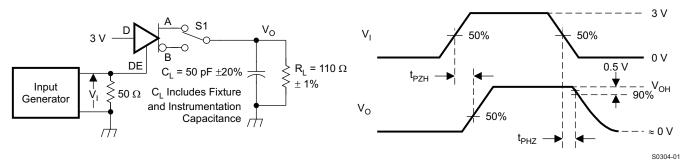
SLLS935-AUGUST 2008

PARAMETER MEASUREMENT INFORMATION (continued)



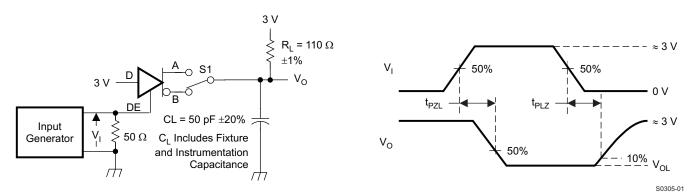
V_I is dashed when INV = HI

Figure 4. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays



NOTE: D at 3 V to test non-inverting output, D at 0 V to test inverting output.

Figure 5. Measurement of Driver Enable and Disable Times With Active High Output and Pulldown Load



NOTE: D at 0 V to test non-inverting output, D at 3 V to test inverting output.

Figure 6. Measurement of Driver Enable and Disable Times With Active-Low Output and Pullup Load

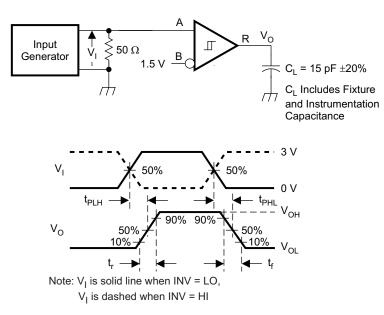
SN65HVD1794, SN65HVD1795 SN65HVD1796

TEXAS INSTRUMENTS

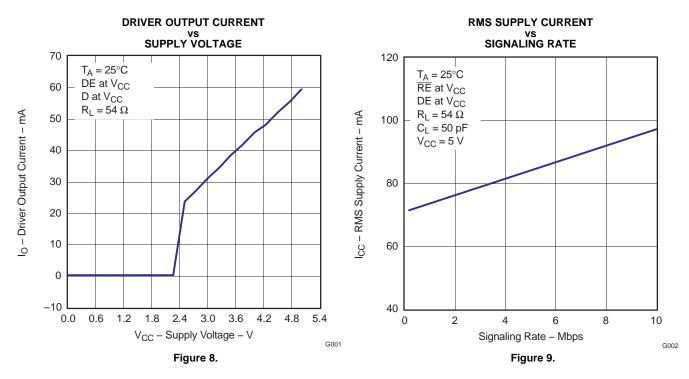
www.ti.com

SLLS935-AUGUST 2008

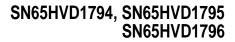








TYPICAL CHARACTERISTICS

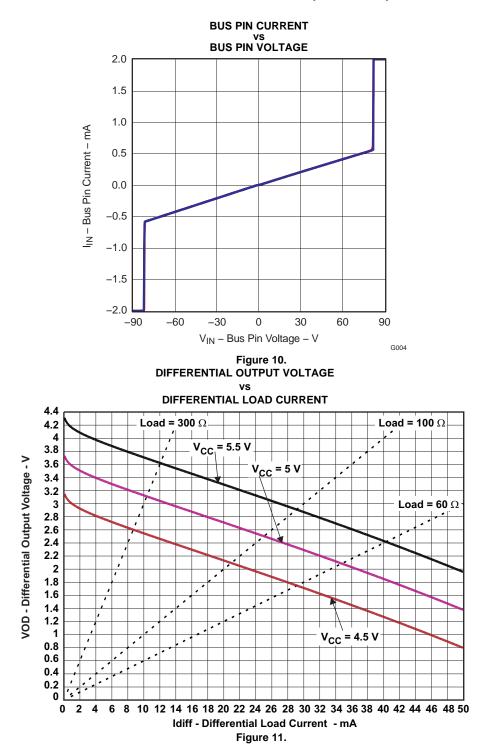


www.ti.com

FEXAS

INSTRUMENTS

TYPICAL CHARACTERISTICS (continued)



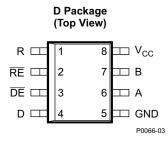
Product Folder Link(s): SN65HVD1794, SN65HVD1795 SN65HVD1796



ADDITIONAL OPTIONS

The SN65HVD17xx family also has options for J1708 applications, for always-enabled full-duplex versions (industry-standard SN65LBC179 footprint) and for inverting-polarity versions, which allow users to correct a reversal of the bus wires without re-wiring. Contact your local Texas Instruments representative for information on these options.

PART NUMBER		SN65HVD17xx			
FOOTPRINT/FUNCTION	SLOW	MEDIUM	FAST		
Half-duplex (176 pinout)	85	86	87		
Full-duplex no enables (179 pinout)	88	89	90		
Full-duplex with enables (180 pinout)	91	92	93		
Half-duplex with cable invert	94	95	96		
Full-duplex with cable invert and enables	97	98	99		
J1708	08	09	10		



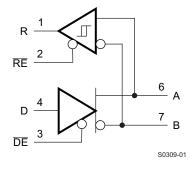


Figure 12. SN65HVD1708E Transceiver for J1708 Applications



Figure 13. SN65HVD17xx Always-Enabled Driver Receiver

Product Folder Link(s): SN65HVD1794, SN65HVD1795 SN65HVD1796

Submit Documentation Feedback



APPLICATION INFORMATION

Hot-Plugging

These devices are designed to operate in "hot swap" or "hot pluggable" applications. Key features for hot-pluggable applications are power-up, power-down glitch free operation, default disabled input/output pins, and receiver failsafe. As shown in Figure 8, an internal Power-On Reset circuit keeps the driver outputs in a high-impedance state until the supply voltage has reached a level at which the device will reliably operate. This ensures that no spurious transitions (glitches) will occur on the bus pin outputs as the power supply turns on or turns off.

As shown in the device **FUNCTION TABLE**, the *ENABLE* inputs have the feature of default disable on both the driver enable and receiver enable. This ensures that the device will neither drive the bus nor report data on the R pin until the associated controller actively drives the enable pins.

Likewise, the receiver output is "failsafe" to open-circuit, short-circuit, or idle (terminated only) bus conditions. This eliminates false transitions on the receiver output until a valid RS-485 signal is applied to the receiver input pins.

Cable Invert

For many RS-485 applications, wiring of data cables takes place during equipment installation, and the possibility of miss-wiring is a significant issue. When the twisted-pair wires are reversed due to installation mistakes, normal RS-485 communication is not possible. The Cable Invert (INV) pin allows designers to compensate for this installation mistake. Under normal circumstances, the INV pin can be set to logic LOW, and the transceiver operates with normal polarity. If, after initial network start-up, a node cannot communicate properly, the local controller can set the INV pin high, which will invert the polarity of the A and B differential bus pins. This will compensate for a reversal of the bus wires, allowing proper communication.

Receiver Failsafe

The differential receiver is "failsafe" to invalid bus states caused by open bus conditions such as a disconnected connector, shorted bus conditions such as cable damage shorting the twisted-pair together or idle bus conditions that occur when no driver is actively driving a valid RS-485 bus state on the network. In any of these cases, the differential receiver outputs a failsafe state, so that small noise signals do not cause spurious transitions at the receiver output. When INV is logic Low or Open (normal operation), the receiver output will be failsafe High. When INV is logic High to correct for a twisted-pair reversal, the receiver output will be failsafe Low under those fault conditions.

TEXAS INSTRUMENTS www.ti.com

TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



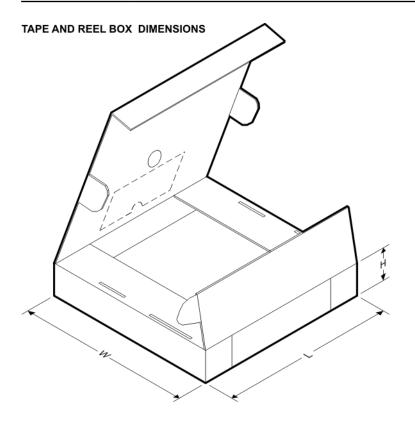
*All dimensions are nominal	

Device		Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD1794DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1



PACKAGE MATERIALS INFORMATION

27-Nov-2008



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD1794DR	SOIC	D	8	2500	346.0	346.0	29.0

P(R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-001 variation BA.



D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.



LAND PATTERN DATA



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Audio	www.ti.com/audio	Communications and Telecom	www.ti.com/communications
Amplifiers	amplifier.ti.com	Computers and Peripherals	www.ti.com/computers
Data Converters	dataconverter.ti.com	Consumer Electronics	www.ti.com/consumer-apps
DLP® Products	www.dlp.com	Energy and Lighting	www.ti.com/energy
DSP	dsp.ti.com	Industrial	www.ti.com/industrial
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Security	www.ti.com/security
Logic	logic.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Power Mgmt	power.ti.com	Transportation and Automotive	www.ti.com/automotive
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com	Wireless	www.ti.com/wireless-apps
RF/IF and ZigBee® Solutions	www.ti.com/lprf		

TI E2E Community Home Page

e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2011, Texas Instruments Incorporated