



SN65HVD10, SN65HVD10Q, SN75HVD10 SN65HVD11, SN65HVD11Q, SN75HVD11 SN65HVD12, SN75HVD12

SLLS505K - FEBRUARY 2002 - REVISED SEPTEMBER 2011

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3.3-V RS-485 TRANSCEIVERS

Check for Samples: SN65HVD10, SN65HVD10Q, SN75HVD10, SN65HVD11, SN65HVD11Q, SN75HVD11, SN65HVD12, SN75HVD12

FEATURES

- Operates With a 3.3-V Supply
- Bus-Pin ESD Protection Exceeds 16 kV HBM
- 1/8 Unit-Load Option Available (Up to 256 Nodes on the Bus)
- Optional Driver Output Transition Times for Signaling Rates ⁽¹⁾ of 1 Mbps, 10 Mbps, and 32 Mbps
- Meets or Exceeds the Requirements of ANSI TIA/EIA-485-A
- Bus-Pin Short Circuit Protection From –7 V to 12 V
- Low-Current Standby Mode . . . 1 µA Typical
- Open-Circuit, Idle-Bus, and Shorted-Bus Failsafe Receiver
- Thermal Shutdown Protection
- Glitch-Free Power-Up and Power-Down Protection for Hot-Plugging Applications
- SN75176 Footprint

APPLICATIONS

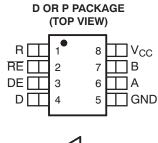
- Digital Motor Control
- Utility Meters
- Chassis-to-Chassis Interconnects
- Electronic Security Stations
- Industrial Process Control
- Building Automation
- Point-of-Sale (POS) Terminals and Networks

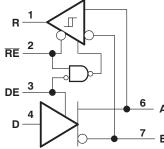
(1) The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

DESCRIPTION

The SN65HVD10, SN75HVD10, SN65HVD11, SN65HVD12, SN75HVD11, and SN75HVD12 combine a 3-state differential line driver and differential input line receiver that operate with a single 3.3-V power supply. They are designed for balanced transmission lines and meet or exceed ANSI standard TIA/EIA-485-A and ISO 8482:1993. These differential bus transceivers are monolithic integrated circuits designed for bidirectional data communication on multipoint bus-transmission lines. The drivers and receivers have active-high and active-low enables respectively, that can be externally connected together to function as direction control. Very low device standby supply current can be achieved by disabling the driver and the receiver.

The driver differential outputs and receiver differential inputs connect internally to form a differential input/output (I/O) bus port that is designed to offer minimum loading to the bus whenever the driver is disabled or $V_{CC} = 0$. These parts feature wide positive and negative common-mode voltage ranges, making them suitable for party-line applications.







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STRUMENTS



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

SIGNALING	UNIT LOADS	т	PACKAGE		SOIC MARKING
RATE	UNIT LUADS	T _A	SOIC ⁽¹⁾	PDIP	SOIC MARKING
32 Mbps	1/2		SN65HVD10D	SN65HVD10P	VP10
10 Mbps	1/8	–40°C to 85°C	SN65HVD11D	SN65HVD11P	VP11
1 Mbps	1/8		SN65HVD12D	SN65HVD12P	VP12
32 Mbps	1/2		SN75HVD10D	SN75HVD10P	VN10
10 Mbps	1/8	−0°C to 70°C	SN75HVD11D	SN75HVD11P	VN11
1 Mbps	1/8		SN75HVD12D	SN75HVD12P	VN12
32 Mbps	1/2	–40°C to 125°C	SN65HVD10QD	SN65HVD10QP	VP10Q
10 Mbps	1/8	-40 C (0 125 C	SN65HVD11QD	SN65HVD11QP	VP11Q

⁽¹⁾ The D package is available taped and reeled. Add an R suffix to the part number (i.e., SN75HVD11DR).

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted (1) (2)

				UNIT
V _{CC}	Supply voltage ran	nge		–0.3 V to 6 V
	Voltage range at A	A or B		–9 V to 14 V
	Input voltage range	e at D, DE, R or RE		–0.5 V to V _{CC} + 0.5 V
	Voltage input rang	e, transient pulse, A and B, throug	gh 100 Ω, see Figure 11	–50 V to 50 V
lo	Receiver output cu	urrent		–11 mA to 11 mA
		11	A, B, and GND	±16 kV
	Electrostatic discharge	Human body model ⁽³⁾	All pins	±4 kV
	uiscriarge	Charged-device model (4)	All pins charge	±1 kV
	Continuous total p	ower dissipation		See Dissipation Rating Table
	Electrical Fast Tra	nsient/Burst ⁽⁵⁾	A, B, and GND	±4 kV
TJ	Junction temperate	ure		170°C

⁽¹⁾ Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- (2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
- (3) Tested in accordance with JEDEC Standard 22, Test Method A114-A and IEC 60749-26.
- (4) Tested in accordance with JEDEC Standard 22, Test Method C101.
- (5) Tested in accordance with IEC 61000-4-4.

PACKAGE DISSIPATION RATINGS

PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR ⁽¹⁾ ABOVE T _A = 25°C	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING	T _A = 125°C POWER RATING
D ⁽²⁾	597 mW	4.97 mW/°C	373 mW	298 mW	100 mW
D ⁽³⁾	990 mW	8.26 mW/°C	620 mW	496 mW	165 mW
Р	1290 mW	10.75 mW/°C	806 mW	645 mW	215 mW

- (1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.
- (2) Tested in accordance with the Low-K thermal metric definitions of EIA/JESD51-3.
- (3) Tested in accordance with the High-K thermal metric definitions of EIA/JESD51-7.



RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range unless otherwise noted

			MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage		3		3.6	
V _I or V _{IC}	Voltage at any bus terminal (separately	or common mode)	-7 ⁽¹⁾		12	
V_{IH}	High-level input voltage	D, DE, RE	2		V_{CC}	V
V _{IL}	Low-level input voltage	D, DE, RE	0		0.8	
V _{ID}	Differential input voltage	Figure 7	-12		12	
	LP-sh level system to a second	Driver	-60			4
I _{OH}	I _{OH} High-level output current	Receiver	-8			mA
		Driver			60	
I _{OL}	Low-level output current	Receiver			8	mA
R _L	Differential load resistance		54	60		Ω
C _L	Differential load capacitance			50		pF
		HVD10			32	
	Signaling rate	HVD11			10	Mbps
		HVD12			1	
T _J ⁽²⁾	Junction temperature				145	°C

⁽¹⁾ The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT	
V_{IK}	Input clamp voltage		$I_1 = -18 \text{ mA}$		-1.5			V
			$I_{O} = 0$		2		V _{CC}	
V _{OD}	Differential output voltage (2)		$R_L = 54 \Omega$, See	Figure 1	1.5			V
			$V_{\text{test}} = -7 \text{ V to } 1$	2 V, See Figure 2	1.5			
$\Delta V_{OD} $	Change in magnitude of differential voltage	output	See Figure 1 an	d Figure 2	-0.2		0.2	V
V _{OC(PP)}	Peak-to-peak common-mode output	voltage				400		mV
V _{OC(SS)}	Steady-state common-mode output	voltage	See Figure 3		1.4		2.5	V
$\Delta V_{OC(SS)}$	Change in steady-state common-movoltage	ode output	- Occ riguic o		-0.0 5		0.05	V
l _{OZ}	High-impedance output current		See receiver inp	out currents				
	lonut ourront	D			-100		0	
I _I	Input current	DE			0		100	μΑ
Ios	Short-circuit output current		-7 V ≤ V _O ≤ 12	V	-250		250	mA
C _(OD)	Differential output capacitance		$V_{OD} = 0.4 \sin (4)$	E6πt) + 0.5 V, DE at 0 V		16		pF
			RE at V _{CC} , D & DE at V _{CC} , No load	Receiver disabled and driver enabled		9	15.5	mA
Icc	Supply current		RE at V _{CC} , D at V _{CC} , DE at 0 V, No load	Receiver disabled and driver disabled (standby)		1	5	μA
			RE at 0 V, D & DE at V _{CC} , No load	Receiver enabled and driver enabled		9	15.5	mA

⁽¹⁾ All typical values are at 25°C and with a 3.3-V supply.

⁽²⁾ See thermal characteristics table for information regarding this specification.

⁽²⁾ For $T_A > 85$ °C, V_{CC} is ±5%.



DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

	PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT	
		HVD10		5	8.5	16		
t _{PLH}	Propagation delay time, low-to-high-level output	HVD11		18	25	40	ns	
		HVD12		135	200	300		
		HVD10		5	8.5	16		
t _{PHL}	Propagation delay time, high-to-low-level output	HVD11		18	25	40	ns	
		HVD12		135	200	300		
		HVD10		3	4.5	10		
t _r	Differential output signal rise time	HVD11	$R_L = 54 \Omega$, $C_L = 50 pF$, See Figure 4	10	20	30	ns	
		HVD12	See Figure 4	100	170	300		
		HVD10		3	4.5	10		
t _f	Differential output signal fall time	HVD11		10	20	30	ns	
		HVD12		100	170	300		
		HVD10				1.5		
t _{sk(p)}	Pulse skew (t _{PHL} - t _{PLH})	HVD11				2.5	ns	
SK(P)	WITE FEID	HVD12				7		
		HVD10				6		
t _{sk(pp)} (2)	Part-to-part skew	HVD11				11	ns	
σκ(ρρ)	•	HVD12			100			
		HVD10				31		
t _{PZH}	Propagation delay time,	HVD11				55	ns	
1 211	high-impedance-to-high-level output	HVD12	$R_1 = 110 \Omega$, \overline{RE} at 0 V,			300		
		HVD10	See Figure 5			25		
t _{PHZ}	Propagation delay time,	HVD11				55	ns	
TIL	high-level-to-high-impedance output	HVD12				300		
		HVD10				26		
t _{PZL}	Propagation delay time,	HVD11				55	ns	
-F Z.L	high-impedance-to-low-level output	HVD12	$R_1 = 110 \Omega$, \overline{RE} at 0 V,			300		
		HVD10	See Figure 6			26		
t _{PLZ}	Propagation delay time,	HVD11				75	ns	
TLL	low-level-to-high-impedance output	HVD12				400		
t _{PZH}	Propagation delay time, standby-to-high-level outp	-1	$R_L = 110 \Omega$, \overline{RE} at 3 V, See Figure 5			6	μs	
t _{PZL}	Propagation delay time, standby-to-low-level output	ıt	$R_L = 110 \Omega$, \overline{RE} at 3 V, See Figure 6			6	μs	

⁽¹⁾ All typical values are at 25°C and with a 3.3-V supply.

 ⁽²⁾ t_{sk(pp)} is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.



RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

	PARAMETER	Т	EST CONDITIO	NS	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{IT+}	Positive-going input threshold voltage	$I_O = -8 \text{ mA}$					-0.01	
V _{IT}	Negative-going input threshold voltage	I _O = 8 mA			-0.2			V
V_{hys}	Hysteresis voltage (V _{IT+} - V _{IT-})					35		mV
V _{IK}	Enable-input clamp voltage	$I_I = -18 \text{ mA}$			-1.5			V
V_{OH}	High-level output voltage	$V_{ID} = 200 \text{ mV},$	$I_{OH} = -8 \text{ mA},$	See Figure 7	2.4			V
V_{OL}	Low-level output voltage	$V_{ID} = -200 \text{ mV},$	$I_{OL} = 8 \text{ mA},$	See Figure 7			0.4	V
I_{OZ}	High-impedance-state output current	$V_O = 0$ or V_{CC}	$\overline{\text{RE}}$ at V_{CC}		-1		1	μΑ
		V_A or $V_B = 12 V$				0.05	0.11	
		V_A or $V_B = 12 V$,	$V_{CC} = 0 V$	HVD11, HVD12,		0.06	0.13	mΛ
		V_A or $V_B = -7 V$		Other input at 0 V	-0.1	-0.05		mA
	Pue input current	V_A or $V_B = -7 V$,	$V_{CC} = 0 V$		-0.05	-0.04		
I _I	Bus input current	V_A or $V_B = 12 V$				0.2	0.5	
		V_A or $V_B = 12 V$,	V _{CC} = 0 V	HVD10,		0.25	0.5	Л
		V_A or $V_B = -7 V$		Other input at 0 V	-0.4	-0.2		mA
		V_A or $V_B = -7 V$,	$V_{CC} = 0 V$		-0.4	-0.15		
I _{IH}	High-level input current, RE	V _{IH} = 2 V			-30		0	μΑ
I _{IL}	Low-level input current, RE	V _{IL} = 0.8 V			-30		0	μΑ
C _{ID}	Differential input capacitance	$V_{ID} = 0.4 \sin (4E6^{\circ})$	πt) + 0.5 V, DE a	at 0 V		15		pF
		RE at 0 V, D & DE at 0 V, No load	Receiver enab	led and driver		4	8	mA
I _{CC}	Supply current	RE at V _{CC} , D at V _{CC} , DE at 0 V, No load	Receiver disab			1	5	μA
		RE at 0 V, D & DE at V _{CC} , No load	Receiver enabled	led and driver		9	15.5	mA

⁽¹⁾ All typical values are at 25°C and with a 3.3-V supply.



RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

	PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t _{PLH}	Propagation delay time, low-to-high-level output	HVD10		12.5	20	25	
t _{PHL}	Propagation delay time, high-to-low-level output	HVD10		12.5	20	25	ns
t _{PLH}	Propagation delay time, low-to-high-level output	HVD11 HVD12	$V_{ID} = -1.5 \text{ V to } 1.5 \text{ V},$	30	55	70	ns
t _{PHL}	Propagation delay time, high-to-low-level output	HVD11 HVD12	C _L = 15 pF, See Figure 8	30	55	70	ns
		HVD10				1.5	
t _{sk(p)}	Pulse skew (t _{PHL} - t _{PLH})	HVD11				4	ns
		HVD12				4	
		HVD10				8	
t _{sk(pp)} (2)	Part-to-part skew	HVD11				15	ns
		HVD12				15	
t _r	Output signal rise time		C _L = 15 pF,	1	2	5	20
t _f	Output signal fall time		See Figure 8	1	2	5	ns
t _{PZH} ⁽¹⁾	Output enable time to high level					15	
t _{PZL} ⁽¹⁾	Output enable time to low level		C _I = 15 pF, DE at 3 V,			15	
t _{PHZ}	Output disable time from high level		See Figure 9			20	ns
t _{PLZ}	Output disable time from low level					15	
t _{PZH} (2)	Propagation delay time, standby-to-high-level out	put	$C_L = 15 \text{ pF, DE at 0,}$			6	
t _{PZL} (2)	Propagation delay time, standby-to-low-level outp	ut	See Figure 10			6	μs

⁽¹⁾ All typical values are at 25°C and with a 3.3-V supply

THERMAL CHARACTERISTICS

over operating free-air temperature range unless otherwise noted (1)

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
0	Junction-to-ambient thermal	High-K board ⁽³⁾ , No airflow	D pkg		121		
θ_{JA}	resistance (2)	No airflow ⁽⁴⁾	P pkg		93		
0	Junction-to-board thermal	High-K board	D pkg		67		°C/W
θ_{JB}	resistance	See (4)	P pkg		57		C/VV
0	Junction-to-case thermal		D pkg		41		
θ_{JC}	resistance		P pkg		55		
		R ₁ = 60 O C ₁ = 50 pF	HVD10 (32 Mbps)		198	250	
P_D	Device power dissipation	R_L = 60 Ω , C_L = 50 pF, DE at V_{CC} , \overline{RE} at 0 V, Input to D a 50% duty cycle square	HVD11 (10 Mbps)		141	176	mW
		wave at indicated signaling rate	HVD12 (500 kbps)		133	161	
_	A	High-K board, No airflow	D pkg	-40		116	
T _A	Ambient air temperature	No airflow ⁽⁴⁾	P pkg	-40		123	°C
T_{JSD}	Thermal shutdown junction temp	erature			165		

⁽¹⁾ See Application Information section for an explanation of these parameters.

⁽²⁾ t_{sk(pp)} is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

⁽²⁾ The intent of θ_{JA} specification is solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment.

⁽³⁾ JSD51-7, High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages.

⁽⁴⁾ JESD51-10, Test Boards for Through-Hole Perimeter Leaded Package Thermal Measurements.



PARAMETER MEASUREMENT INFORMATION

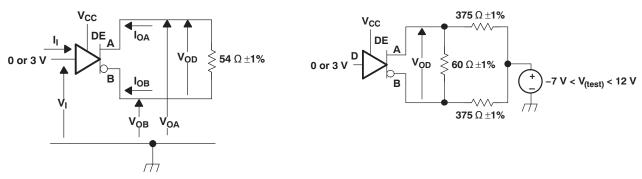
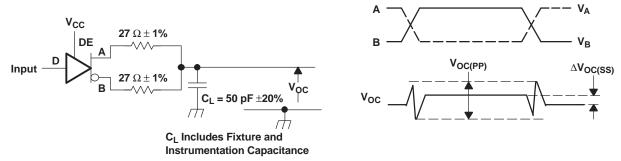


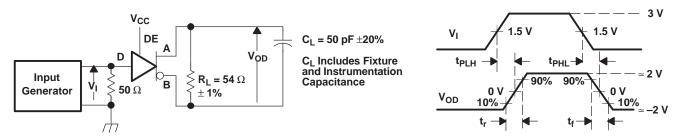
Figure 1. Driver V_{OD} Test Circuit and Voltage and Current Definitions

Figure 2. Driver V_{OD} With Common-Mode Loading Test Circuit



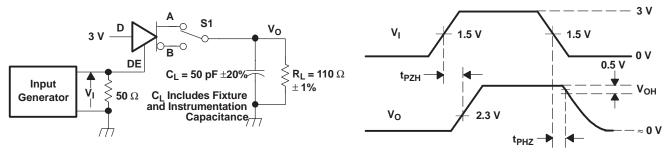
Input: PRR = 500 kHz, 50% Duty Cycle, t_r <6ns, t_f <6ns, Z_O = 50 Ω

Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage



Generator: PRR = 500 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_0 = 50 Ω

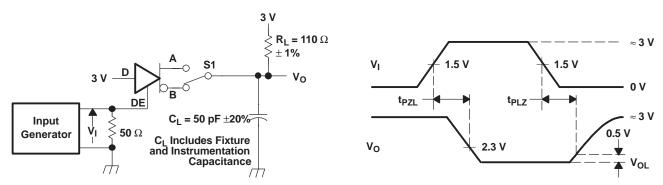
Figure 4. Driver Switching Test Circuit and Voltage Waveforms



Generator: PRR = 500 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_o = 50 Ω

Figure 5. Driver High-Level Enable and Disable Time Test Circuit and Voltage Waveforms





Generator: PRR = 500 kHz, 50% Duty Cycle, t_{r} <6 ns, t_{f} <6 ns, Z_{o} = 50 Ω

Figure 6. Driver Low-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms

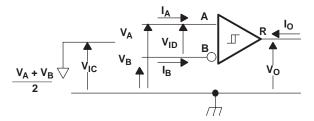
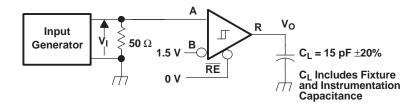


Figure 7. Receiver Voltage and Current Definitions



Generator: PRR = 500 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_o = 50 Ω

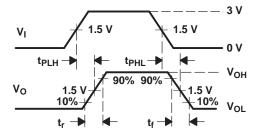
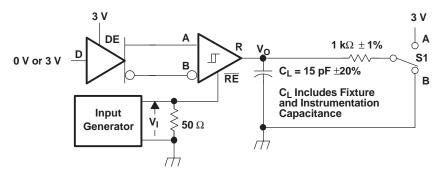


Figure 8. Receiver Switching Test Circuit and Voltage Waveforms





Generator: PRR = 500 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_o = 50 Ω

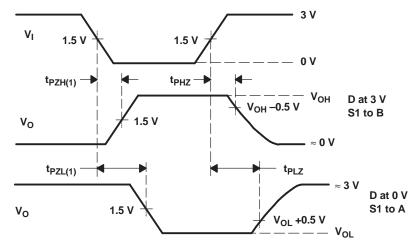
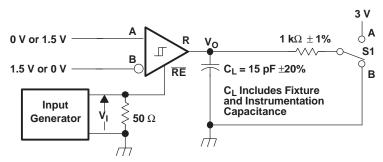


Figure 9. Receiver Enable and Disable Time Test Circuit and Voltage Waveforms With Drivers Enabled





Generator: PRR = 100 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_o = 50 Ω

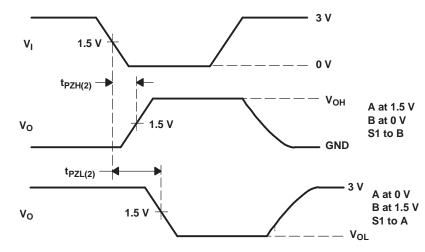
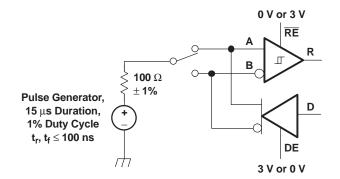


Figure 10. Receiver Enable Time From Standby (Driver Disabled)



NOTE: This test is conducted to test survivability only. Data stability at the R output is not specified.

Figure 11. Test Circuit, Transient Over Voltage Test



FUNCTION TABLES

Table 1. DRIVER⁽¹⁾

		OUTI	PUTS
INPUT D	ENABLE DE	Α	В
Н	Н	Н	L
L	Н	L	Н
Х	L	Z	Z
Open	Н	Н	L

⁽¹⁾ H = high level; L = low level; Z = high impedance; X = irrelevant; ? = indeterminate

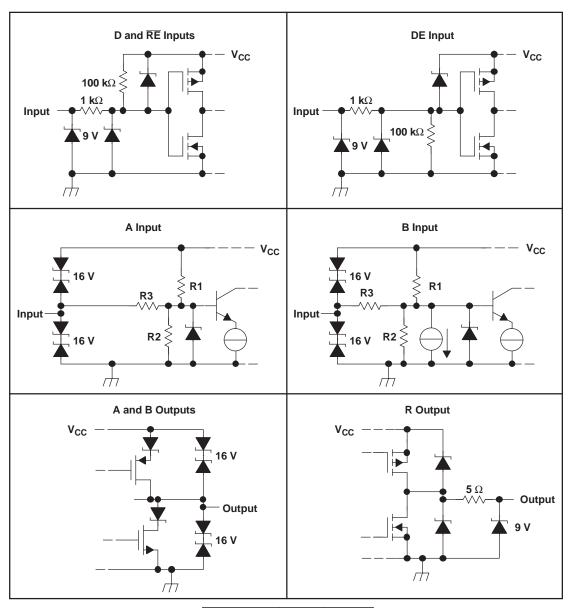
Table 2. RECEIVER (1)

DIFFERENTIAL INPUTS $V_{ID} = V_A - V_B$	ENABLE RE	OUTPUT R
V _{ID} ≤ -0.2 V	L	L
-0.2 V < V _{ID} < -0.01 V	L	?
-0.01 V ≤ V _{ID}	L	Н
X	Н	Z
Open Circuit	L	Н
Short circuit	L	Н

⁽¹⁾ H = high level; L = low level; Z = high impedance; X = irrelevant; ? = indeterminate



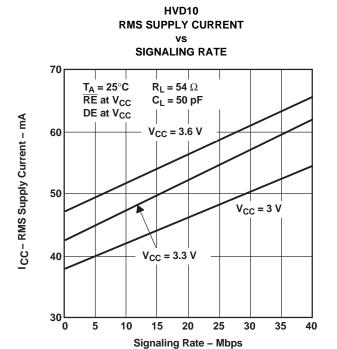
EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



	R1/R2	R3
SN65HVD10	9 k Ω	45 k Ω
SN65HVD11	36 k Ω	180 k Ω
SN65HVD12	36 k Ω	180 k Ω

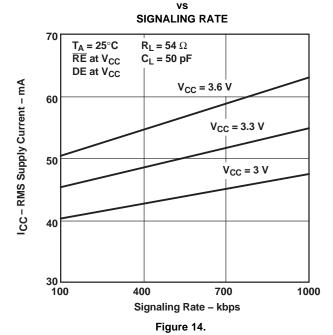


TYPICAL CHARACTERISTICS



HVD12 RMS SUPPLY CURRENT

Figure 12.



HVD11 RMS SUPPLY CURRENT vs SIGNALING RATE

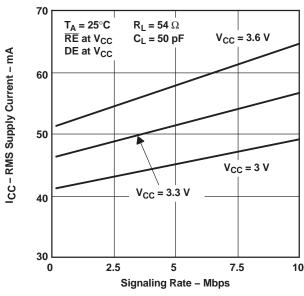


Figure 13.

HVD10 BUS INPUT CURRENT vs BUS INPUT VOLTAGE

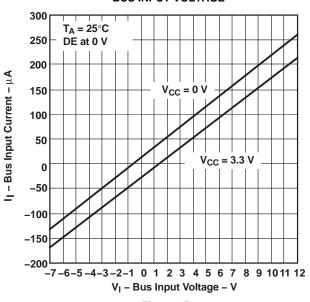
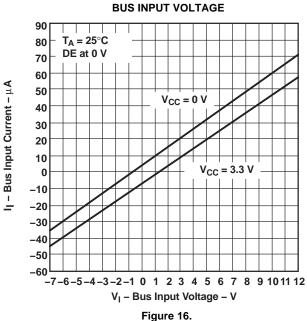


Figure 15.



TYPICAL CHARACTERISTICS (continued)

HVD11 OR HVD12 BUS INPUT CURRENT vs



HIGH-LEVEL OUTPUT CURRENT

DRIVER HIGH-LEVEL OUTPUT VOLTAGE

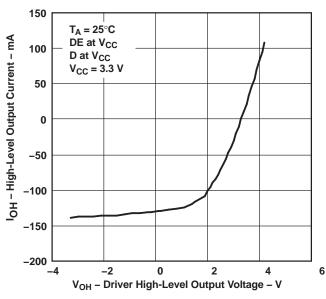
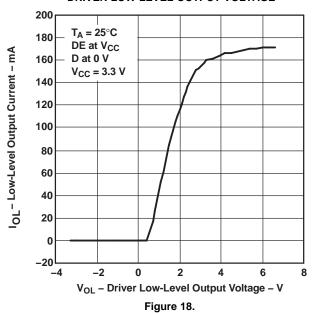


Figure 17.

LOW-LEVEL OUTPUT CURRENT

DRIVER LOW-LEVEL OUTPUT VOLTAGE



DRIVER DIFFERENTIAL OUTPUT

FREE-AIR TEMPERATURE

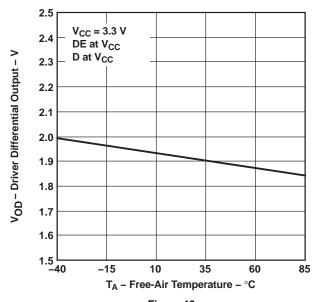


Figure 19.



TYPICAL CHARACTERISTICS (continued)

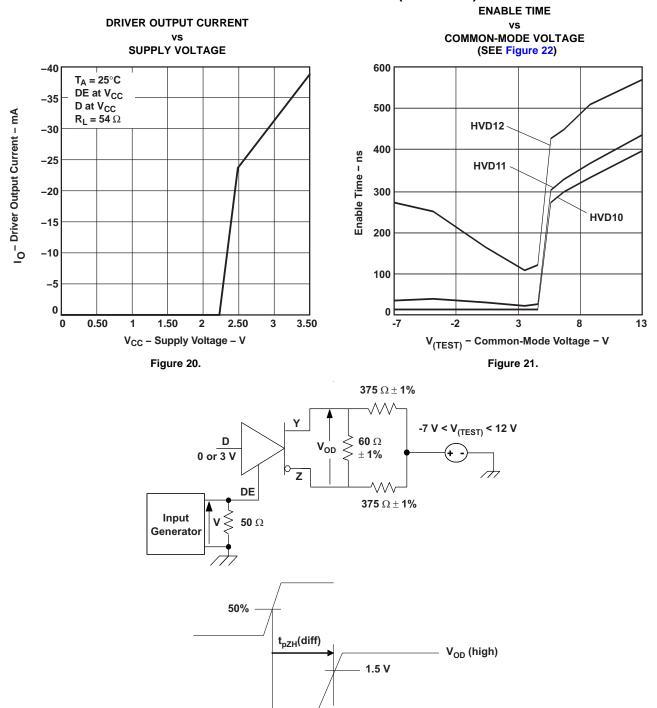


Figure 22. Driver Enable Time From DE to V_{OD}

-1.5 V

V_{OD} (low)

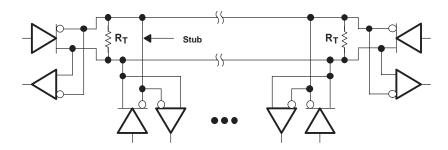
The time $t_{PZL}(x)$ is the measure from DE to $V_{OD}(x)$. V_{OD} is valid when it is greater than 1.5 V.

 $t_{pZL}(diff)$

0 V



APPLICATION INFORMATION



Device	Number of Devices on Bus
HVD10	64
HVD11	256
HVD12	256

NOTE: The line should be terminated at both ends with its characteristic impedance (R_T = Z_O). Stub lengths off the main line should be kept as short as possible.

Figure 23. Typical Application Circuit

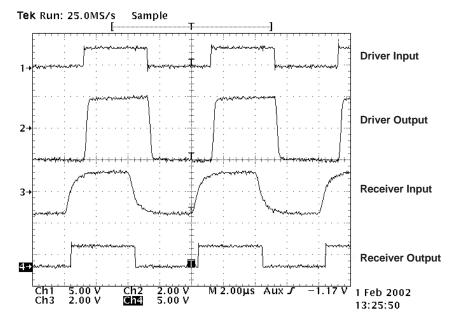


Figure 24. HVD12 Input and Output Through 2000 Feet of Cable

An example application for the HVD12 is illustrated in Figure 23. Two HVD12 transceivers are used to communicate data through a 2000 foot (600 m) length of Commscope 5524 category 5e+ twisted pair cable. The bus is terminated at each end by a $100-\Omega$ resistor, matching the cable characteristic impedance. Figure 24 illustrates operation at a signaling rate of 250 kbps.

LOW-POWER STANDBY MODE

When both the driver and receiver are disabled (DE low and RE high) the device is in standby mode. If the enable inputs are in this state for less than 60 ns, the device does not enter standby mode. This guards against inadvertently entering standby mode during driver/receiver enabling. Only when the enable inputs are held in this state for 300 ns or more, the device is assured to be in standby mode. In this low-power standby mode, most internal circuitry is powered down, and the supply current is typically less than 1 nA. When either the driver or the receiver is re-enabled, the internal circuitry becomes active.



THERMAL CHARACTERISTICS OF IC PACKAGES

 θ_{JA} (Junction-to-Ambient Thermal Resistance) is defined as the difference in junction temperature to ambient temperature divided by the operating power.

 θ_{JA} is *not* a constant and is a strong function of:

- the PCB design (50% variation)
- altitude (20% variation)
- device power (5% variation)

 θ_{JA} can be used to compare the thermal performance of packages if the specific test conditions are defined and used. Standardized testing includes specification of PCB construction, test chamber volume, sensor locations, and the thermal characteristics of holding fixtures. θ_{JA} is often misused when it is used to calculate junction temperatures for other installations.

TI uses two test PCBs as defined by JEDEC specifications. The low-k board gives *average* in-use condition thermal performance, and it consists of a single copper trace layer 25 mm long and 2-oz thick. The high-k board gives best *case* in-use condition, and it consists of two 1-oz buried power planes with a single copper trace layer 25 mm long and 2-oz thick. A 4% to 50% difference in θ_{IA} can be measured between these two test cards.

 θ_{JC} (Junction-to-Case Thermal Resistance) is defined as difference in junction temperature to case divided by the operating power. It is measured by putting the mounted package up against a copper block cold plate to force heat to flow from die, through the mold compound into the copper block.

 θ_{JC} is a useful thermal characteristic when a heatsink is applied to package. It is *not* a useful characteristic to predict junction temperature because it provides pessimistic numbers if the case temperature is measured in a nonstandard system and junction temperatures are backed out. It can be used with θ_{JB} in 1-dimensional thermal simulation of a package system.

 θ_{JB} (Junction-to-Board Thermal Resistance) is defined as the difference in the junction temperature and the PCB temperature at the center of the package (closest to the die) when the PCB is clamped in a cold-plate structure. θ_{JB} is only defined for the high-k test card.

 θ_{JB} provides an overall thermal resistance between the die and the PCB. It includes a bit of the PCB thermal resistance (especially for BGAs with thermal balls) and can be used for simple 1-dimensional network analysis of package system, see Figure 25.

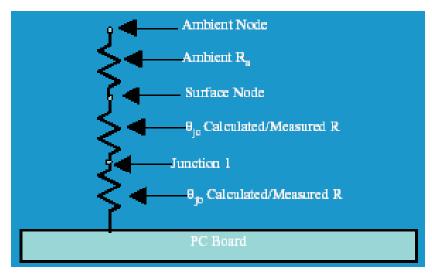
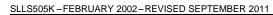


Figure 25. Thermal Resistance





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REVISION HISTORY

Ch	nanges from Revision J (February 2009) to Revision K	Pa	ge
•	Added new section 'LOW-POWER STANDBY MODE', in the Application Information section		16



2-Sep-2011

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN65HVD10D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65HVD10DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65HVD10DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65HVD10DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65HVD10P	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN65HVD10PE4	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN65HVD10QD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65HVD10QDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65HVD10QDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65HVD10QDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65HVD11D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65HVD11DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65HVD11DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65HVD11DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65HVD11P	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN65HVD11PE4	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN65HVD11QD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65HVD11QDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	



2-Sep-2011

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN65HVD11QDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65HVD11QDRG4	ACTIVE	SOIC	D	8		TBD	Call TI	Call TI	
SN65HVD12D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65HVD12DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65HVD12DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65HVD12DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65HVD12P	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN65HVD12PE4	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN75HVD10D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN75HVD10DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN75HVD10DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN75HVD10DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN75HVD10P	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN75HVD10PE4	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN75HVD11D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN75HVD11DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN75HVD11DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN75HVD11DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN75HVD12D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN75HVD12DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	



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PACKAGE OPTION ADDENDUM

2-Sep-2011

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN75HVD12DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN75HVD12DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN75HVD12P	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN75HVD12PE4	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN65HVD10, SN65HVD11, SN65HVD12:

Enhanced Product: SN65HVD10-EP, SN65HVD12-EP





2-Sep-2011

NOTE: Qualified Version Definitions:

• Enhanced Product - Supports Defense, Aerospace and Medical Applications

PACKAGE MATERIALS INFORMATION

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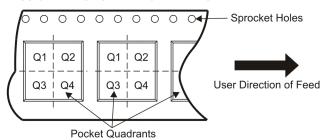
TAPE AND REEL INFORMATION





		Dimension designed to accommodate the component width
		Dimension designed to accommodate the component length
P	〈 0	Dimension designed to accommodate the component thickness
		Overall width of the carrier tape
П	P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD10DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD10QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD11DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD11QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD12DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75HVD10DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75HVD11DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75HVD12DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD10DR	SOIC	D	8	2500	340.5	338.1	20.6
SN65HVD10QDR	SOIC	D	8	2500	340.5	338.1	20.6
SN65HVD11DR	SOIC	D	8	2500	340.5	338.1	20.6
SN65HVD11QDR	SOIC	D	8	2500	340.5	338.1	20.6
SN65HVD12DR	SOIC	D	8	2500	340.5	338.1	20.6
SN75HVD10DR	SOIC	D	8	2500	340.5	338.1	20.6
SN75HVD11DR	SOIC	D	8	2500	340.5	338.1	20.6
SN75HVD12DR	SOIC	D	8	2500	340.5	338.1	20.6

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-001 variation BA.



D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



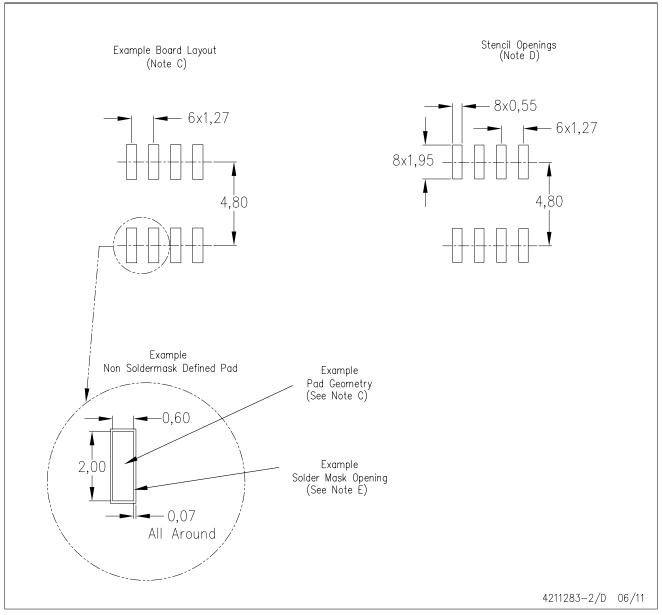
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.



D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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