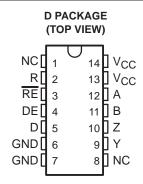
- Qualified for Automotive Applications
- Designed for High-Speed Multipoint Data Transmission Over Long Cables
- Operate With Pulse Durations as Low as 30 ns
- Low Supply Current . . . 5 mA Max
- Meet or Exceed the Requirements of ANSI Standard RS-485 and ISO 8482:1987(E)
- 3-State Outputs for Party-Line Buses
- Common-Mode Voltage Range of -7 V to 12 V
- Thermal Shutdown Protection Prevents Driver Damage From Bus Contention
- Positive and Negative Output Current Limiting
- Pin Compatible With the SN75ALS180

description

The SN65LBC180 differential driver and receiver pair is a monolithic integrated circuit designed for bidirectional data communication over long cables that take on the characteristics of transmission lines. It is a balanced, or differential, voltage mode device that meets or exceeds the requirements of industry standards ANSI RS-485 and ISO 8482:1987(E). The device is designed using TI's proprietary LinBiCMOS[™] with the low power consumption of CMOS and the precision and robustness of bipolar transistors in the same circuit.

The SN65LBC180 combines a differential line driver and receiver with 3-state outputs and operates from a single 5-V supply. The driver and receiver have active-high and active-low enables, respectively, which can be externally connected to function as a direction control. The driver differential outputs and the receiver differential inputs are connected to separate terminals for full-duplex operation and are designed to present minimum loading to the bus whether disabled or powered off ($V_{CC} = 0$). This part features a wide common-mode voltage range making it suitable for point-to-point or multipoint data-bus applications.



SGLS251A - JULY 2004 - REVISED JUNE 2008

NC-No internal connection

Function Tables

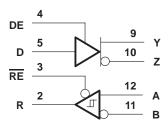
	DRIVER		
INPUT	ENABLE	OUT	PUTS
D	DE	Y	Z
Н	Н	Н	L
L	Н	L	Н
Х	L	Z	Z

RECEIVER

DIFFERENTIAL INPUTS A-B	ENABLE RE	OUTPUT R
$V_{ID} \ge 0.2 V$	L	Н
-0.2 V < V _{ID} < 0.2 V	L	?
$V_{ID} \leq -0.2 V$	L	L
X	Н	Z
Open circuit	L	Н

H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

logic diagram (positive logic)





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LinBiCMOS is a trademark of Texas Instruments Incorporated

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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SGLS251A - JULY 2004 - REVISED JUNE 2008

description/ordering information (continued)

ORDERING INFORMATION[†]

TA	PACKAGE [‡]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – D	Tape and reel	SN65LBC180IDRQ1	LBC180Q1

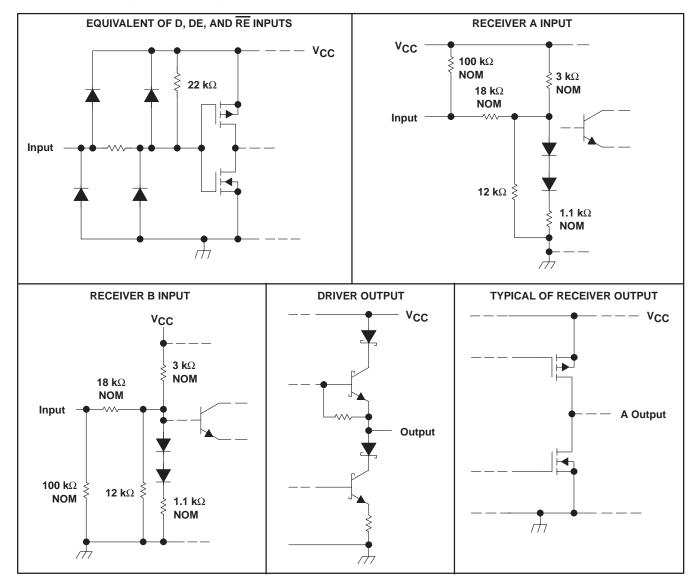
[†] For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at http://www.ti.com.

[‡]Package drawings, thermal data, and symbolization are available at http://www.ti.com/packaging.

The devices also provide positive and negative output-current limiting and thermal shutdown for protection from line fault conditions. The line driver shuts down at a junction temperature of approximately 172°C.



SGLS251A - JULY 2004 - REVISED JUNE 2008



schematics of inputs and outputs



SGLS251A - JULY 2004 - REVISED JUNE 2008

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Continuous total power dissipation (see Note 2) Internally limited Total power dissipation	Total power dissipation	
Storage temperature 1,6 mm (1/16 inch) from case for 10 seconds -65° C to -65° C to 260° C	Storage temperature range, T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.

2. The maximum operating junction temperature is internally limited. Use the dissipation rating table to operate below this temperature.

DISSIPATION RATING TABLE										
PACKAGE	$T_A \le 25^{\circ}C$ POWER RATING	DERATING FACTOR ABOVE T _A = 25°C	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING						
D	950 mW	7.6 mW/°C	608 mW	494 mW						

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V _{CC}		4.75	5	5.25	V
High-level input voltage, VIH	D, DE, and RE	2			V
Low-level input voltage, VIL	D, DE, and RE			0.8	V
Differential input voltage, V _{ID}		-6‡		6	V
Voltage at any bus terminal (separately or common mode), VO, VI, or VIC	A, B, Y, or Z	_7‡		12	V
1 Park land and and an entry 1	Y or Z			-60	
High-level output current, IOH	R			-8	mA
	Y or Z			60	
Low-level output current, IOL	R			8	mA
Operating free-air temperature, T _A		-40		85	°C

⁺ The algebraic convention where the least positive (more negative) limit is designated minimum, is used in this data sheet for the differential input voltage, voltage at any bus terminal, operating temperature, input threshold voltage, and common-mode output voltage.



SGLS251A - JULY 2004 - REVISED JUNE 2008

DRIVER SECTION

electrical characteristics over recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST CC	NDITIONS	MIN	TYP†	MAX	UNIT
VIK	Input clamp voltage	I _I = –18 mA				-1.5	V
	Differential output voltage magnitude	RL = 54 Ω,	See Figure 1	1.1	2.5	5	N
Vod	(see Note 3)	RL = 60 Ω,	See Figure 2	1.1	2	5	V
Δ V _{OD}	Change in magnitude of differential output voltage (see Note 4)	See Figures 1 and 2				±0.2	V
V _{OC}	Common-mode output voltage			1	2.5	3	V
A VOC	Change in magnitude of common-mode output voltage (see Note 4)	R _L = 54 Ω, See Figure 1				±0.2	V
IO	Output current with power off	$V_{CC} = 0,$	$V_{O} = -7 V$ to 12 V			±100	μΑ
IOZ	High-impedance-state output current	$V_{O} = -7 V$ to 12 V				±100	μΑ
IIН	High-level input current	VI = 2.4 V				-100	μΑ
١ _{IL}	Low-level input current	V ₁ = 0.4 V				-100	μΑ
IOS	Short-circuit output current	$-7 \text{ V} \le \text{V}_0 \le 12 \text{ V}$				±250	mA
	Supply ourrent	Receiver disabled	Outputs enabled			5	~^^
ICC	Supply current	Receiver disabled	Outputs disabled			3	mA

[†] All typical values are at V_{CC} = 5 V and T_A = 25°C. NOTES: 3. The minimum V_{OD} specification of the SN65LBC180 may not fully comply with ANSI RS-485 at operating temperatures below 0°C. System designers should take the possibly lower output signal into account in determining the maximum signal-transmission distance.

4. $\Delta |V_{OD}|$ and $\Delta |V_{OC}|$ are the changes in the steady-state magnitude of V_{OD} and V_{OC} , respectively, that occur when the input is changed from a high level to a low level.

switching characteristics, $V_{CC} = 5 V$, $T_A = 25^{\circ}C$

	PARAMETER	TEST CO	ONDITIONS	MIN	TYP	MAX	UNIT
td(OD)	Differential output delay time	540		7	12	18	ns
^t t(OD)	Differential output transition time	$R_L = 54 \Omega$,	See Figure 3	5	10	20	ns
^t PZH	Output enable time to high level	RL = 110 Ω,	See Figure 4			35	ns
^t PZL	Output enable time to low level	R _L = 110 Ω,	See Figure 5			35	ns
^t PHZ	Output disable time from high level	R _L = 110 Ω,	See Figure 4			50	ns
^t PLZ	Output disable time from low level	R _L = 110 Ω,	See Figure 5			35	ns



SGLS251A - JULY 2004 - REVISED JUNE 2008

RECEIVER SECTION

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	I _O = -8 mA				0.2	V
V_{IT-}	Negative-going input threshold voltage	I _O = 8 mA		-0.2			V
V _{hys}	Hysteresis voltage (VIT + - VIT -)				45		mV
VIK	Enable-input clamp voltage	II = -18 mA				-1.5	V
VOH	High-level output voltage	V _{ID} = 200 mV,	IOH = -8 mA	3.5	4.5		V
VOL	Low-level output voltage	$V_{ID} = -200 \text{ mV},$	I _{OL} = 8 mA		0.3	0.5	V
IOZ	High-impedance-state output current	$V_{O} = 0 V \text{ to } V_{CC}$				±20	μA
IIH	High-level enable-input current	V _{IH} = 2.4 V				-50	μA
۱ _{IL}	Low-level enable-input current	V _{IL} = 0.4 V				-100	μA
		V _I = 12 V, Other input at 0 V	V _{CC} = 5 V,		0.7	1	
	Bus input current	V _I = 12 V, Other input at 0 V	V _{CC} = 0 V,		0.8	1	
1ı		$V_{I} = -7 V$, Other input at 0 V	V _{CC} = 5 V,		-0.5	-0.8	mA
		$V_I = -7 V$, Other input at 0 V	V _{CC} = 0 V,		-0.5	-0.8	
	Currely current	Driver dischlad	Outputs enabled			5	
ICC	CC Supply current Driver disabled		Outputs disabled			3	mA

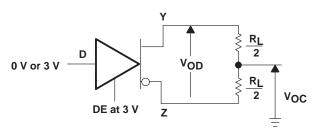
switching characteristics, V_{CC} = 5 V, T_A = 25°C

	PARAMETER	TEST CONDIT	TIONS	MIN	TYP	MAX	UNIT
^t PHL	Propagation delay time, high- to low-level output			11	22	33	ns
^t PLH	Propagation delay time, low- to high-level output			11	22	33	ns
^t sk(p)	Pulse skew ($V_{\text{ID}} = -1.5 \text{ V} \text{ to } 1.5 \text{ V},$ See Figure 6			3	6	ns
tt	Transition time				5	8	ns
^t PZH	Output enable time to high level					35	ns
t _{PZL}	Output enable time to low level	See Figure 7				30	ns
^t PHZ	Output disable time from high level	See Figure 7				35	ns
^t PLZ	Output disable time from low level				30	ns	



SGLS251A - JULY 2004 - REVISED JUNE 2008

PARAMETER MEASUREMENT INFORMATION





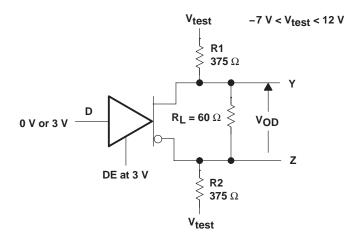
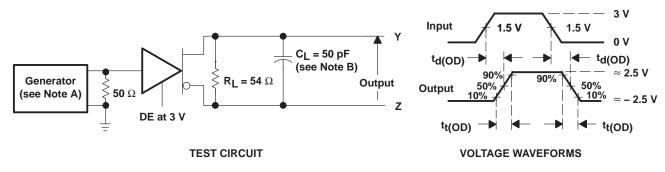


Figure 2. Driver V_{OD} Test Circuit



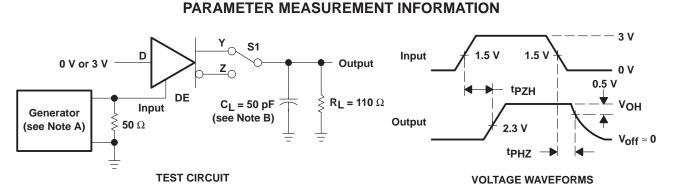
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR > 1 MHz, 50% duty cycle, $t_f \le 6$ ns, $t_f \le 6$ ns, $Z_O = 50 \Omega$.

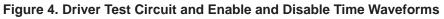
B. CL includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Differential Output Delay and Transition Time Voltage Waveforms



SGLS251A - JULY 2004 - REVISED JUNE 2008





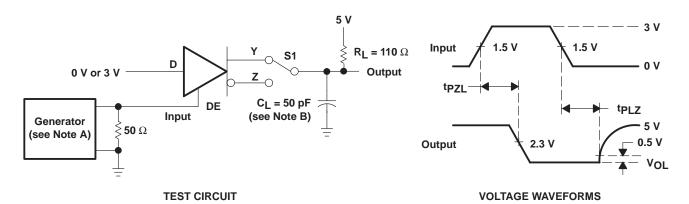
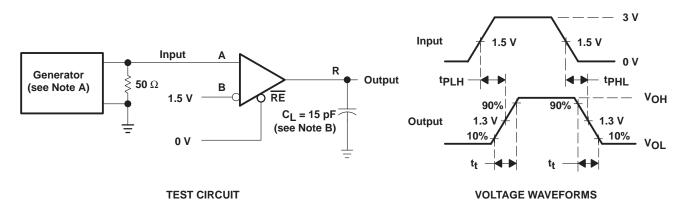


Figure 5. Driver Test Circuit and Enable and Disable Time Voltage Waveforms

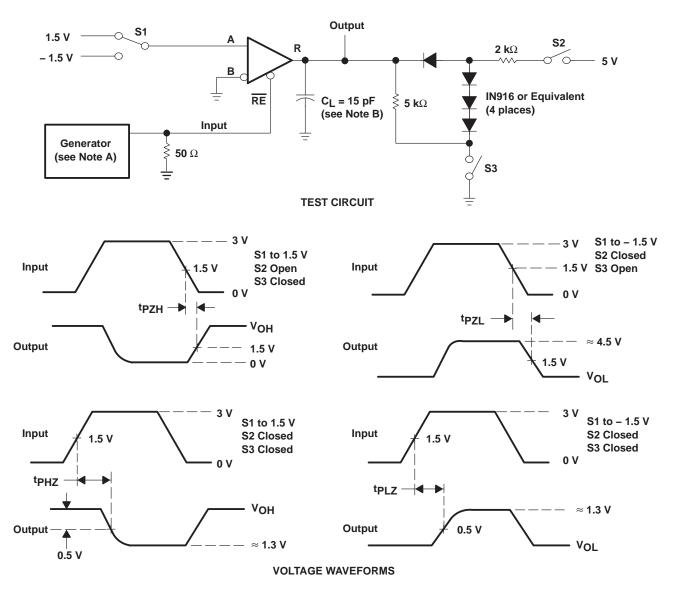


- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, t_f \leq 6 ns, t_f \leq 6 ns, Z_Q = 50 Ω .
 - B. CL includes probe and jig capacitance.

Figure 6. Receiver Test Circuit and Propagation Delay Time Voltage Waveforms



SGLS251A - JULY 2004 - REVISED JUNE 2008



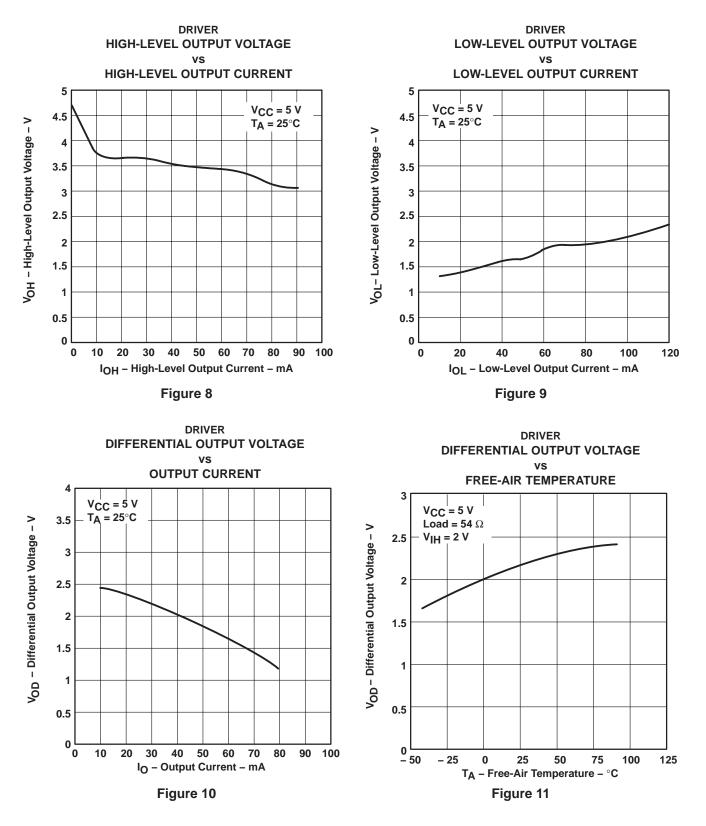
PARAMETER MEASUREMENT INFORMATION

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, t_f \leq 6 ns, t_f \leq 6 ns, Z_O = 50 Ω .
 - B. C_{L} includes probe and jig capacitance.

Figure 7. Receiver Output Enable and Disable Times

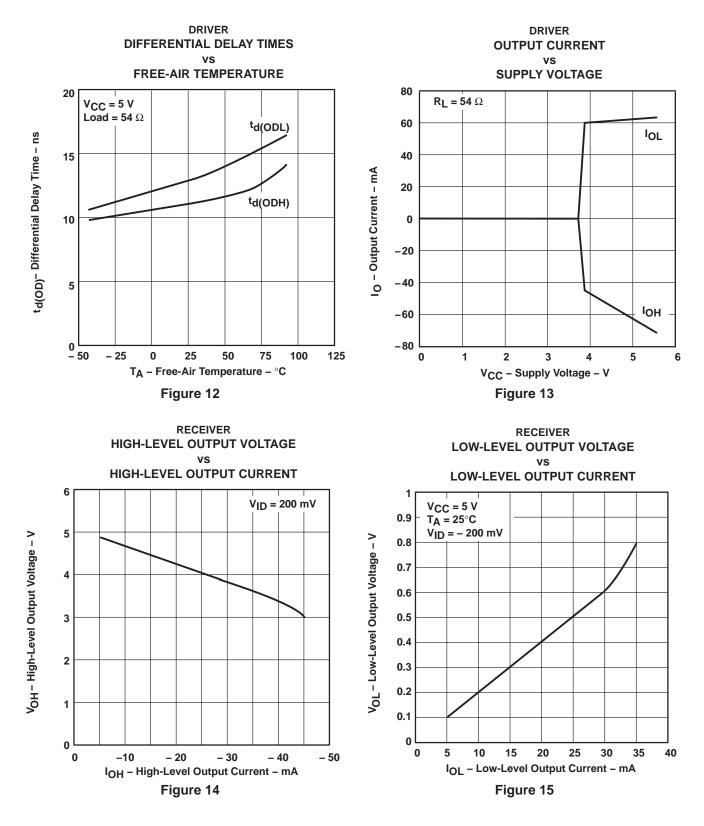


SGLS251A - JULY 2004 - REVISED JUNE 2008



TYPICAL CHARACTERISTICS

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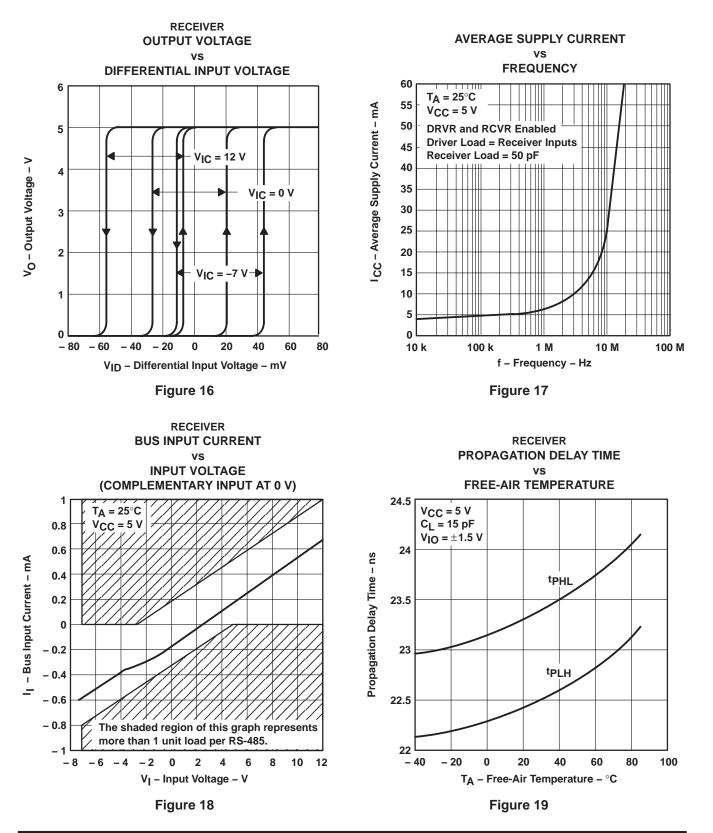


TYPICAL CHARACTERISTICS



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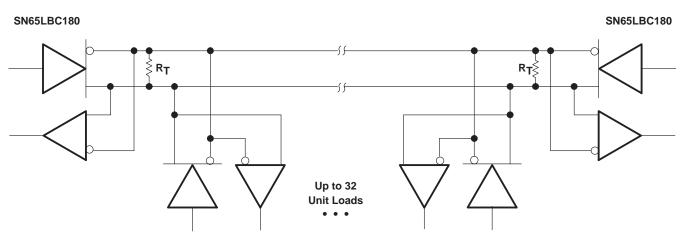






SGLS251A - JULY 2004 - REVISED JUNE 2008

APPLICATION INFORMATION



NOTE A: The line should be terminated at both ends in its characteristic impedance (R_T = Z_O). Stub lengths off the main line should be kept as short as possible. One SN65LBC180 typically represents less than one unit load.

Figure 20. Typical Application Circuit





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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN65LBC180IDRG4Q1	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65LBC180IDRQ1	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN65LBC180-Q1 :

Catalog: SN65LBC180





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27-Apr-2012

• Catalog - TI's standard catalog product

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.



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