SN75ALS171, SN75ALS171A TRIPLE DIFFERENTIAL BUS TRANSCEIVERS

DW OR J PACKAGE (TOP VIEW)

SLLS056D - AUGUST 1987 - REVISED SEPTEMBER 1995

- Three Bidirectional Transceivers
- Driver Meets or Exceeds the Requirements of ANSI EIA/TIA-422-B and RS-485 and ITU Recommendation V.11
- Two Skew Limits Available
- Designed to Operate Up to 20 Million Data Transfers per Second (FAST-20 SCSI)
- High-Speed Advanced Low-Power Schottky Circuitry
- Low Pulse Skew . . . 5 ns Max
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- Features Independent Driver Enables and Combined Receiver Enables
- Wide Positive and Negative Input/Output Bus Voltages Ranges
- Driver Output Capacity . . . ±60 mA
- Thermal Shutdown Protection
- Driver Positive- and Negative-Current Limiting
- Receiver Input Impedances . . . 12 kΩ Min
- Receiver Input Sensitivity . . . ±300 mV Max
- Receiver Input Hysteresis . . . 60 mV Typ
- Operates From a Single 5-V Supply
- Glitch-Free Power-Up and Power-Down Protection

2R [6 15 2B 2DE [7 14] 2A 2D [8 13] 3B 3R [9 12] 3A 3DE [10 11] 3D

description

The SN75ALS171 and the SN75ALS171A triple differential bus transceivers are monolithic integrated circuits designed for bidirectional data communication on multipoint bus transmission lines. They are designed for balanced transmission lines, and each driver meets ANSI Standards EIA/TIA-422-B and RS-485 and both the drivers and receivers meet ITU Recommendation V.11. The SN75ALS171A is designed for FAST-20 SCSI and can transmit or receive data pulses as short as 30 ns with a maximum skew of 5 ns.

The SN75ALS171 and the SN75ALS171A operate from a single 5-V power supply. The drivers and receivers have individual active-high and active-low enables, respectively, which can be externally connected together to function as a direction control. The driver differential output and the receiver differential input pairs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus when the driver is disabled or V_{CC} is at 0 V. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

The SN75ALS171 and the SN75ALS171A are characterized for operation from 0°C to 70°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



Function Tables

EACH DRIVER

INPUT	ENA	BLES	OUTPUTS		
D	DE	CDE	Α	В	
Н	Н	Н	Н	L	
L	Н	Н	L	Н	
Х	L	Χ	Z	Z	
Х	Х	L	Z	Z	

EACH RECEIVER

DIFFERENTIAL INPUTS A-B	ENABLE RE	OUTPUT R
V _{ID} ≥ 0.3 V	L	Н
$-0.3 \text{ V} < \text{V}_{\text{ID}} < 0.3 \text{ V}$	L	?
V _{ID} ≤ −0.3 V	L	L
X	Н	Z
Open	L	Н

H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

AVAILABLE OPTIONS

SKEW LIMIT	PART NUMBER						
10 ns	SN75ALS171DW	SN75ALS171J					
5 ns	SN75ALS171ADW						

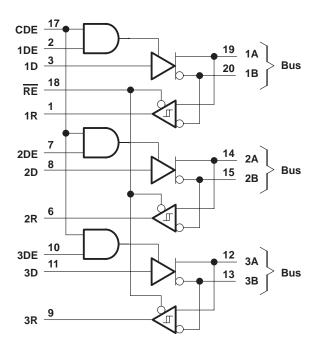


logic symbol†

CDE G5 1DE 5EN1 2DE 5EN2 10 3DE 5EN3 18 RE EN4 19 \triangleright 1▽ 1D 20 1▽ 1B 1 1R ▽ 4 ┚ 2▽ \triangleright 2A 2D 2▽ 2B 1 ▽ 4 2R П 12 3▽ \triangleright 3A 3D 13 3▽ 3B 3R ╜

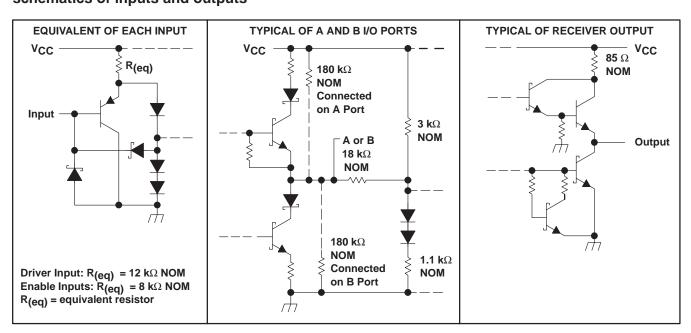
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and

logic diagram (positive logic)



schematics of inputs and outputs

IEC Publication 617-12.



SN75ALS171, SN75ALS171A TRIPLE DIFFÉRENTIAL BUS TRANSCEIVERS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC} (see Note 1)	7 V
Voltage range at any bus terminal	–7 V to 12 V
Enable input voltage, V _I	7 V
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T _A	0°C to 70°C
Storage temperature range, T _{stq}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package .	300°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_{\mbox{\scriptsize A}} \le 25^{\circ}\mbox{\scriptsize C}$ POWER RATING	DERATING FACTOR ABOVE T _A = 25°C	T _A = 70°C POWER RATING		
DW	1125 mW	9.0 mW/°C	720 mW		
J	1025 mW	8.2 mW/°C	656 mW		

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V _{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), V _I or V _{IC}		-7		12	V
High-level input voltage, VIH	D, CDE, DE, and RE	2			V
Low-level input voltage, V _{IL}	D, CDE, DE, and RE			0.8	V
Differential input voltage, V _{ID} (see Note 2)			±12	V	
High level output ourrent leve	Driver			-60	mA
High-level output current, IOH	Receiver			-400	μΑ
Lour lovel outbut outroot lo	Driver Receiver			60	A
Low-level output current, IOL				8	mA
Operating free-air temperature, T _A				70	°C

NOTE 2: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.



NOTE 1: All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CO	MIN	TYP‡	MAX	UNIT	
٧ıĸ	Input clamp voltage	I _I = -18 mA				-1.5	V
VO	Output voltage	IO = 0		0		6	V
Vон	High-level output voltage	V _{CC} = 4.75 V, V _{IL} = 0.8 V,	$V_{IH} = 2 V$, $I_{OH} = -55 \text{ mA}$	2.7			V
VOL	Low-level output voltage	V _{CC} = 4.75 V, V _{IL} = 0.8 V,	V _{IH} = 2 V, I _{OL} = 55 mA			1.7	٧
VOD1	Differential output voltage	IO = 0		1.5		6	V
IV _{OD2} I	Differential output voltage	$R_L = 100 \Omega$,	See Figure 1	1/2 V _{OD1} or 2§	2.5	5	V
		$R_L = 54 \Omega$,	See Figure 1	1.5	2.5	5	
V _{OD3}	Differential output voltage	$V_{test} = -7 V to 12 V$,	See Figure 2	1.5		5	V
Δ VOD	Change in magnitude of differential output voltage¶					±0.2	V
Voc	Common-mode output voltage	$R_L = 54 \Omega \text{ or } 100 \Omega,$	See Figure 1			3 -1	٧
Δ V _{OC}	Change in magnitude of common-mode output voltage¶					±0.2	V
Ю	Output current	Output disabled, See Note 3	$V_{O} = 12 \text{ V}$ $V_{O} = -7 \text{ V}$			1 -0.8	mA
lін	High-level enable-input current	D and DE CDE	V _{IH} = 2.7 V			20 60	
IιΓ	Low-level enable-input current	D and DE	V _{IL} = 0.4 V			-100 -900	μΑ
		V _O = -6 V		+		-300 -250	
		V _O = 0				-150	
los	Short-circuit output current	Vo = Vcc				250	mA
		V _O = 8 V		 	-	250	
	Owner to a company		Outputs enabled	<u> </u>	69	90	A
ICC	Supply current	No load	Outputs disabled	1	57	78	mA

The power-off measurement in ANSI Standard EIA/TIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.



[‡] All typical values are at $V_{CC} = 5 \text{ V}$ and $T_A = 25^{\circ}\text{C}$.

[§] The minimum V_{OD2} with 100-W load is either 1/2 V_{OD2} or 2 V, whichever is greater.

[¶] Δ|V_{OD}| and Δ|V_{OC}| are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

NOTE 3: This applies for both power on and off; refer to EIA Standard RS-485 for exact conditions. The EIA/TIA-422-B limit does not apply for a combined driver and receiver terminal.

SN75ALS171, SN75ALS171A TRIPLE DIFFERENTIAL BUS TRANSCEIVERS

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP [†]	MAX	UNIT
		ALS171	R _L = 54 Ω,	See Figure 3,	3		13	
		ALS171A	$C_{L} = 50 \text{ pF}$		6		11	
td(OD)	Differential output delay time	ALS171	$R_{L1} = R_{L3} = 165 \Omega$, $C_{L} = 60 pF$,	V _{TERM} = 5 V, See Figure 6	3		13	ns
		ALS171A	$R_{L2} = 75 \Omega$	See Figure 0	6		11	
*	Dules shout		R_L = 54 Ω, See Figure 3	C _L = 50 pF,		1	5	ns
tsk(p)	Pulse skew [‡]		$R_{L1} = R_{L3} = 165 \Omega$, $C_{L} = 60 pF$,	$R_{L2} = 75 \Omega$, See Figure 6		1	5	ns
	Skew limit§	ALS171	R _L = 54 Ω,	C _L = 50 pF,			10	
• • • • •		ALS171A	See Figure 3				5	ns
tsk(lim)		ALS171	$R_{L1} = R_{L3} = 165 \Omega$,	$R_{L2} = 75 \Omega$,			10	115
		ALS171A	$C_L = 60 \text{ pF},$	See Figure 6			5	
	Differential-output transition time		$R_L = 54 \Omega$, See Figure 3	C _L = 50 pF,	3	8	13	
^t t(OD)			$R_{L1} = R_{L3} = 165 \Omega$, $C_{L} = 60 \text{ pF}$, See Figure 6	$R_{L2} = 75 \Omega,$ VTERM = 5 V,	3	8	13	ns
^t PZH	Output enable time to high level		$R_L = 110 \Omega$,	See Figure 4		30	50	ns
tPZL	Output enable time to low level		$R_L = 110 \Omega$,	See Figure 5		30	50	ns
^t PHZ	Output disable time from high level		$R_L = 110 \Omega$,	See Figure 4	3	8	13	ns
^t PLZ	Output disable time from low level		$R_L = 110 \Omega$,	See Figure 5	3	8	13	ns
tPDE	DE Differential-output enable time		$R_{L1} = R_{L3} = 165 \Omega,$ $C_{L} = 60 \text{ pF},$	$R_{L2} = 75 \Omega$,	8	30	45	ns
tPDZ				See Figure 7	5	10	45	ns

[†] All typical values are at $V_{CC} = 5 \text{ V}$ and $T_A = 25^{\circ}\text{C}$.

SYMBOL EQUIVALENTS

DATA-SHEET PARAMETER	EIA/TIA-422-B	RS-485
Vo	V _{oa} , V _{ob}	V _{oa} , V _{ob}
V _{OD1}	Vo	Vo
V _{OD2}	$V_t (R_L = 100 \Omega)$	$V_t (R_L = 54 \Omega)$
V _{OD3}		V _t (Test Termination Measurement 2)
V _{test}		V _{tst}
Δ V _{OD}	$ V_t - \overline{V}_t $	$ \vee_{t} - \overline{\vee}_{t} $
Voc	V _{os}	V _{os}
Δ V _{OC}	$ V_{OS} - \overline{V}_{OS} $	$ V_{OS} - \overline{V}_{OS} $
los	I _{sa} , I _{sb}	
lo	$ I_{xa} , I_{xb} $	I _{ia} , I _{ib}



[‡] Pulse skew is defined as the |t_{d(ODL)}| of each channel. § Skew limit is the maximum difference in propagation delay times between any two channels of one device and between any two devices. This parameter is applicable at one V_{CC} and operating temperature within the recommended operating conditions.

RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CO	TEST CONDITIONS			MAX	UNIT
V _{IT+}	Positive-going input threshold voltage	V _O = 2.7 V,	$I_0 = -0.4 \text{ mA}$			0.3	V
VIT-	Negative-going input threshold voltage	V _O = 0.5 V,	IO = 8 mA	-0.3‡			V
V _{hys}	Hysteresis voltage (V _{IT+} - V _{IT-})				60		mV
VIK	Enable-input clamp voltage	I _I = -18 mA				-1.5	V
VOH	High-level output voltage	V _{ID} = 300 mV, See Figure 8	$I_{OH} = -400 \mu A$,	2.7			V
VOL	Low-level output voltage	V _{ID} = -300 mV, See Figure 8	$I_{OL} = 8 \text{ mA},$			0.45	V
loz	High-impedance-state output current	$V_0 = 0.4 \text{ V to } 2.4 \text{ V}$				±20	μΑ
1.	Line input current	Other input = 0 V,	V _I = 12 V			1	A
''	Line input current	See Note 4	V _I = -7 V			-0.8	mA
ΙΗ	High-level enable-input current	V _{IH} = 2.7 V				60	μΑ
I _{IL}	Low-level enable-input current	V _{IL} = 0.4 V				-300	μΑ
rį	Input resistance			12			kΩ
los	Short-circuit output current	$V_{ID} = 300 \text{ mV},$	V _O = 0	-15		-85	mA
laa	Committee on the committee of the committ	No load	Outputs enabled		69	90	
lcc	Supply current	INO IOAU	Outputs disabled		57	78	mA

 $[\]overline{\dagger}$ All typical values are at V_{CC} = 5 V and T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature range

	PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT	
	Programatical delegations from the binds found and and	ALS171	$V_{ID} = -1.5 \text{ V to } 1.5 \text{ V},$	9		19	20
^t PLH	Propagation delay time, low- to high-level output	ALS171A	$C_L = 15 \text{ pF},$	11		16	ns
	Propagation delay time, high- to low-level output	ALS171	$T_A = 25^{\circ}C$,	9		19	no
^t PHL	Propagation delay time, high- to low-level output	ALS171A	See Figure 9	11		16	ns
t _{sk(p)}	k(p) Pulse skew§		$V_{ID} = -1.5 \text{ V to } 1.5 \text{ V},$		2	5	ns
	OL 15 M	ALS171 $C_L = 15 \text{ pF},$				10	
tsk(lim)	Skew limit¶	ALS171A	See Figure 9			5	ns
^t PZH	Output enable time to high level		C _L = 15 pF,		7	14	ns
t _{PZL} Output enable time to low level		See Figure 10		7	14	ns	
tPHZ			C _L = 15 pF,		20	35	ns
tpLZ Output disable time from low level		See Figure 10		8	17	ns	

[†] All typical values are at $V_{CC} = 5 \text{ V}$ and $T_A = 25^{\circ}\text{C}$.



[‡] The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

NOTE 4: This applies for both power on and off; refer to EIA Standard RS-485 for exact conditions.

[§] Pulse skew is defined as the |tpLH-tpHL| of each channel.

[¶] Skew limit is the maximum difference in propagation delay times between any two channels of one device and between any two devices. This parameter is applicable at one V_{CC} and operating temperature within the recommended operating conditions.

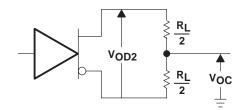


Figure 1. Driver V_{OD} and V_{OC}

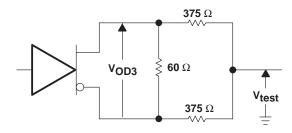
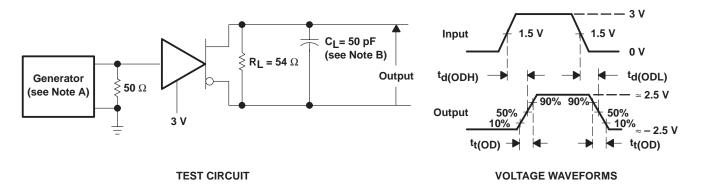
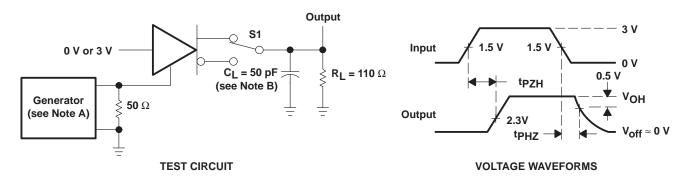


Figure 2. Driver V_{OD3}



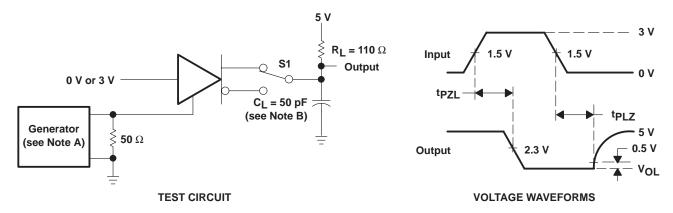
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_{\tilde{f}} \leq$ 6 ns, $t_{\tilde{f}} \leq$ 7 ns, $t_{\tilde{f}} \leq$ 8 ns, $t_{\tilde{f}} \leq$ 9 ns, $t_{$

Figure 3. Driver Test Circuit and Voltage Waveforms



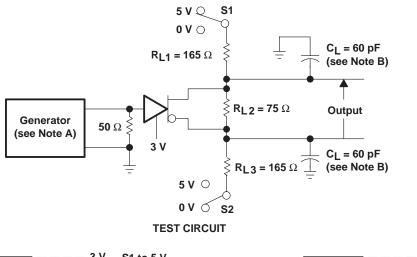
- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_f \leq$ 6 ns, $t_f \leq$ 8 ns, $t_f \leq$ 8 ns, $t_f \leq$ 9 ns, t_f
 - B. C_L includes probe and jig capacitance.

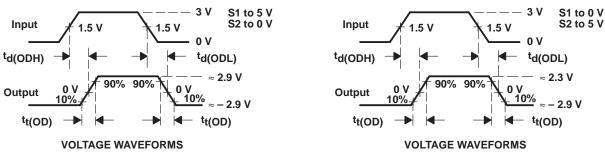
Figure 4. Driver Test Circuit and Voltage Waveforms



- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_f \leq$ 6 ns, $t_f \leq$ 8 ns, $t_f \leq$ 8 ns, $t_f \leq$ 9 ns, t_f
 - B. CL includes probe and jig capacitance.

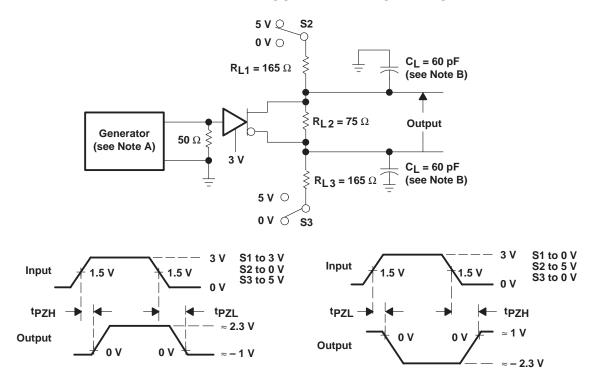
Figure 5. Driver Test Circuit and Voltage Waveforms





NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_f \leq$ 6 ns, $t_f \leq$ 8 ns, $t_f \leq$ 8 ns, $t_f \leq$ 9 ns, t_f

Figure 6. Driver Test Circuit and Voltage Waveforms With Double-Differential-SCSI Termination for the Load



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_f \leq$ 6 ns, $t_f \leq$ 7 ns, $t_f \leq$ 8 ns, $t_f \leq$ 8 ns, $t_f \leq$ 8 ns, $t_f \leq$ 8 ns, $t_f \leq$ 9 ns, t_f

Figure 7. Driver Differential-Enable and Disable Times With a Double-SCSI Termination

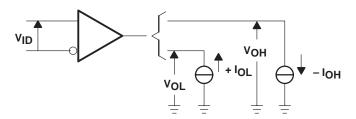
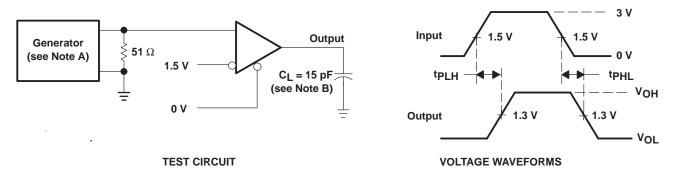
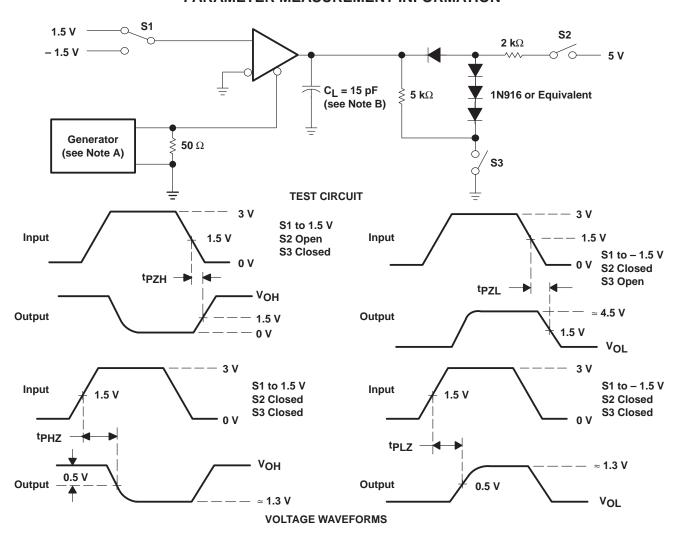


Figure 8. Receiver VOH and VOL



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_{\Gamma} \leq$ 6 ns, $t_{\Gamma} \leq$ 7 ns, $t_{\Gamma} \leq$ 8 ns, $t_{\Gamma} \leq$ 8 ns, $t_{\Gamma} \leq$ 9 ns, $t_$

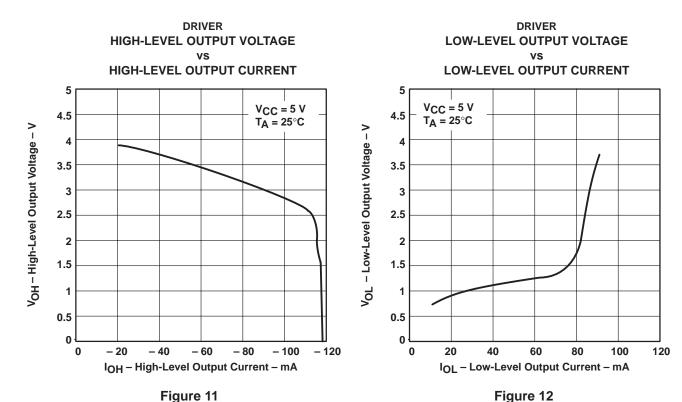
Figure 9. Receiver Test Circuit and Voltage Waveforms



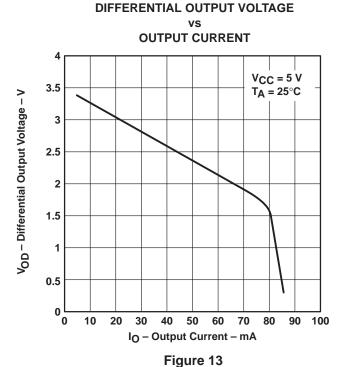
- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_{\Gamma} \leq$ 6 ns, $t_{f} \leq$ 6 ns, $t_{O} = 50 \ \Omega$.
 - B. C_L includes probe and jig capacitance.

Figure 10. Receiver Test Circuit and Voltage Waveforms

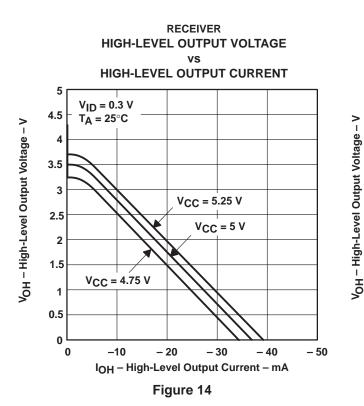
TYPICAL CHARACTERISTICS



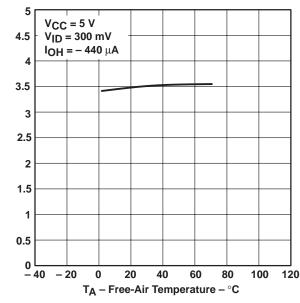
DRIVER



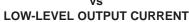
TYPICAL CHARACTERISTICS

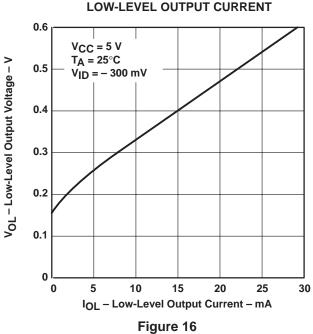


RECEIVER HIGH-LEVEL OUTPUT VOLTAGE FREE-AIR TEMPERATURE



RECEIVER LOW-LEVEL OUTPUT VOLTAGE





RECEIVER LOW-LEVEL OUTPUT VOLTAGE

Figure 15

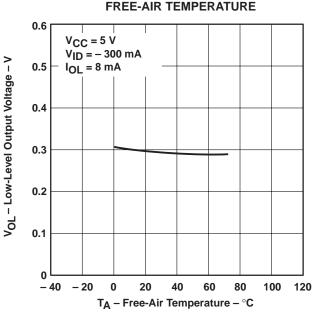
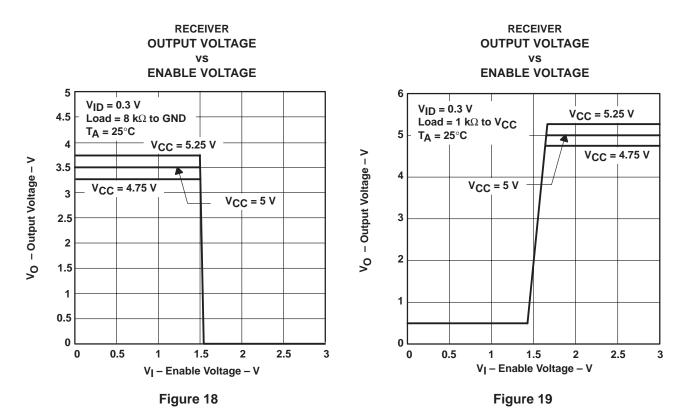
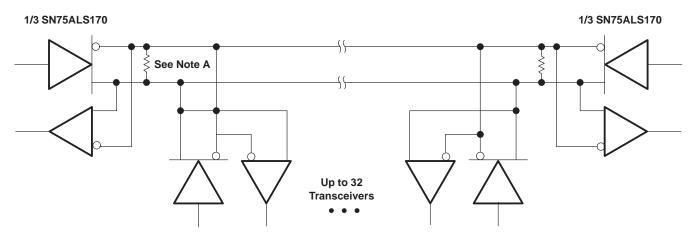


Figure 17

TYPICAL CHARACTERISTICS



APPLICATION INFORMATION



NOTE A: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

Figure 20. Typical Application Circuit

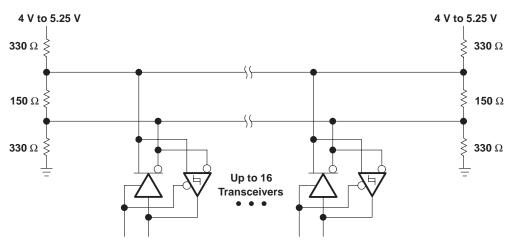


Figure 21. Typical Differential SCSI Application Circuit

APPLICATION INFORMATION

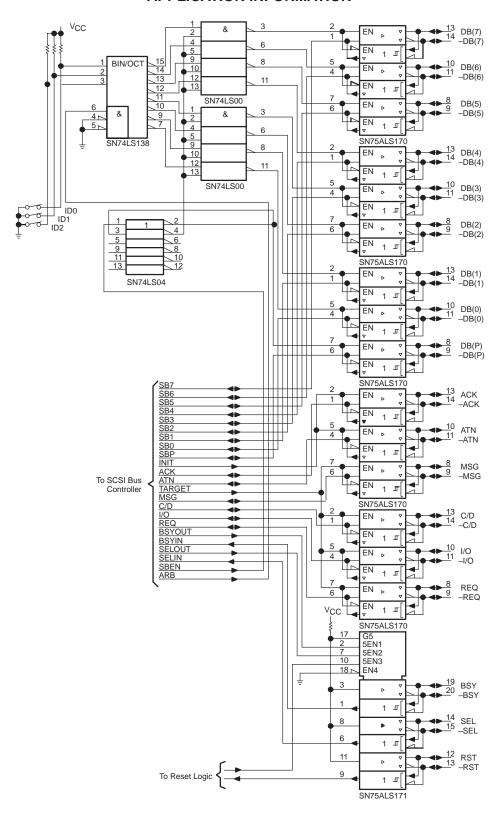


Figure 22. Typical Differential SCSI Bus Interface Implementation







com 10-May-2007

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN75ALS171ADW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS171ADWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS171ADWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS171ADWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS171ADWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS171ADWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS171DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS171DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS171DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS171DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS171DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS171DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS171J	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE OPTION ADDENDUM

10-May-2007

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TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device		Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75ALS171ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.1	2.65	12.0	24.0	Q1
SN75ALS171DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.1	2.65	12.0	24.0	Q1





*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75ALS171ADWR	SOIC	DW	20	2000	346.0	346.0	41.0
SN75ALS171DWR	SOIC	DW	20	2000	346.0	346.0	41.0

14 LEADS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



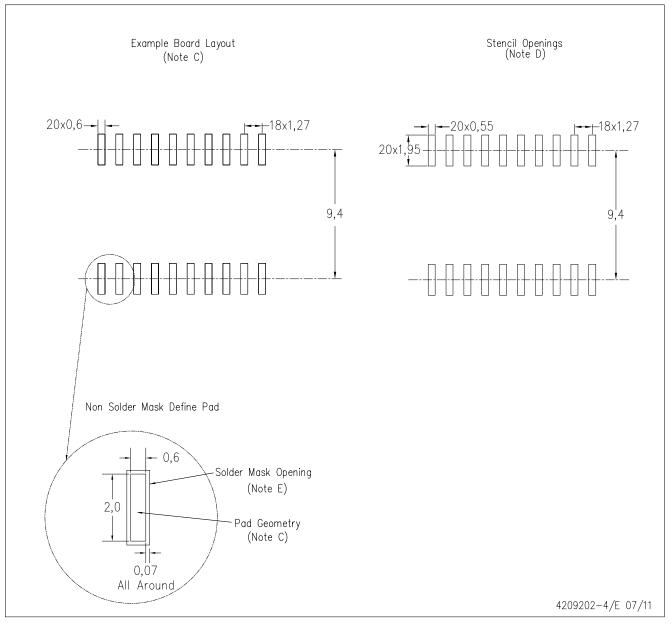
NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.



DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC—7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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