

VERY LOW POWER, NEGATIVE RAIL INPUT, RAIL-TO-RAIL OUTPUT, FULLY DIFFERENTIAL AMPLIFIER

Check for Samples: THS4521-HT

FEATURES

- Fully Differential Architecture
- Bandwidth: 40.7 MHz (210°C)
- Slew Rate: 353.5 V/µs (210°C)
- HD₂: -96 dBc at 1 kHz (1 V_{RMS}, R_L = 1 kΩ) (210°C)
- HD₃: -91.5 dBc at 1 kHz (1 V_{RMS}, R_L = 1 kΩ) (210°C)
- Input Voltage Noise: 19.95 nV/\(\sqrt{Hz}\) (f = 100 kHz)
- Open-Loop Gain: 90 dB (typ) (210°C)
- NRI—Negative Rail Input
- RRO—Rail-to-Rail Output
- Output Common-Mode Control (with Low Offset and Drift)
- Power Supply:
 - Voltage: 2.5 V (±1.25 V) to 3.3 V (±1.65 V)
 - Current: 1.4 mA/ch (3.3 V)
- Power-Down Capability: 10 µA (typ) (210°C)

APPLICATIONS

- Down-Hole Drilling
- High Temperature Environments

SUPPORTS EXTREME TEMPERATURE APPLICATIONS

- Controlled Baseline
- One Assembly/Test Site
- One Fabrication Site
- Available in Extreme (-55°C/210°C) Temperature Range⁽¹⁾
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability
- Texas Instruments high temperature products utilize highly optimized silicon (die) solutions with design and process enhancements to maximize performance over extended temperatures.
- (1) Custom temperature ranges available

DESCRIPTION

The THS4521 is a very low-power, fully differential op amp with rail-to-rail output and an input common-mode range that includes the negative rail. This amplifier is designed for low-power data acquisition systems and high-density applications where power dissipation is a critical parameter, and provides exceptional performance in audio applications.

The THS4521 features accurate output common-mode control that allows for dc-coupling when driving analog-todigital converters (ADCs). This control, coupled with an input common-mode range below the negative rail as well as rail-to-rail output, allows for easy interfacing between single-ended, ground-referenced signal sources. Additionally, this device is ideally suited for driving both successive-approximation register (SAR) and deltasigma ($\Delta\Sigma$) ADCs using only a single 2.5-V to 3.3-V and ground power supply.

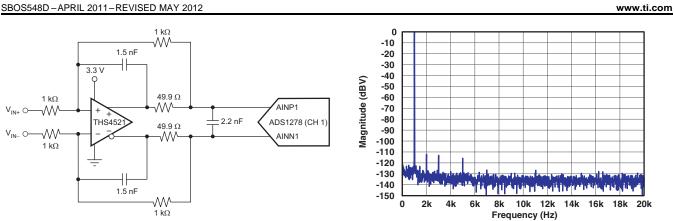
The THS4521 is characterized for operation from -55°C to 210°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



SBOS548D-APRIL 2011-REVISED MAY 2012





DIE THICKNESS

11 mils.

BACKSIDE FINISH

Silicon with backgrind

SBOS548D-APRIL 2011-REVISED MAY 2012

BOND PAD

THICKNESS

1380 nm



www.ti.com

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

BOND PAD

METALLIZATION COMPOSITION

Al-Cu (0.5%)

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

<		922 μm>	
			\uparrow
	12	11 10 9 8	
76.8 µm			mu 809 —
		6	
	1	2 3 4 5	
0.0			
 0.0		75.8 μm	

BARE DIE INFORMATION

BACKSIDE

POTENTIAL

Floating

Table 1. Bond Pad Coordinates in Microns

DISCRIPTION	PAD NUMBER	X min	Y min	X max	Y max
V _{IN-}	1	80.7	3.7	165.7	88.7
V _{OCM}	2	310.6	3.7	395.6	88.7
V _{S+}	3	405.6	3.7	490.6	88.7
V _{S+}	4	500.6	3.7	585.6	88.7
V _{S+}	5	595.6	3.7	680.6	88.7
V _{OUT+}	6	679.6	137.55	764.6	222.55
V _{OUT-}	7	679.6	434.7	764.6	519.7
V _{S-}	8	595.6	568.6	680.6	653.6
V _{S-}	9	500.6	568.6	585.6	653.6
V _{S-}	10	405.6	568.6	490.6	653.6
PD	11	310.6	568.6	395.6	653.6
V _{IN+}	12	80.7	568.6	165.7	653.6

THS4521-HT

www.ti.com

SBOS548D-APRIL 2011-REVISED MAY 2012

ORDERING INFORMATION⁽¹⁾

T _A PACKAGE ⁽²⁾ ORDERABLE PART NUMBER TOP-SIDE MARKING								
-55°C to175°C	D	THS4521HD	THS4521					
	KGD (bare die)	THS4521SKGD1	NA					
–55°C to 210°C	HKJ	THS4521SHKJ	THS4521SHKJ					
	HKQ	THS4521SHKQ	THS4521SHKQ					

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Over operating free-air temperature range (unless otherwise noted).

				UNIT
Supply Vo	bltage, V_{S-} to V_{S+}	3.6	V	
Input/Out	out Voltage, V _I (V _{IN±} , V _{OUT±} , V _{OCM} pins)		$(V_{S-}) - 0.7$ to $(V_{S+}) + 0.7V$	V
Differentia	al Input Voltage, V _{ID}		1	V
Output Cu	urrent, I _O		100	mA
Input Curi	rent, I _I (V _{IN±} , V _{OCM} pins)	10	mA	
Continuou	us Power Dissipation	See Thermal Characteristic	c Specifications	
Maximum	Junction Temperature, T_J (continuous operation, long-to	erm reliability) ⁽²⁾	217	°C
Operating	Free air Tomporatura Banga T	D package	-40 to 175	°C
Operating	Free-air Temperature Range, T _A	KGD, HKJ, HKQ packages	-55 to 210	C
Storage T	emperature Range, T _{STG}		-65 to 210	°C
Human Body Model (HBM)			1300	V
ESD Rating:	Charge Device Model (CDM)	1000	V	
. tating.	Machine Model (MM)	50	V	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Refer to Figure 1 for expected life time.

THERMAL CHARACTERISTICS FOR D PACKAGE

over operating free-air temperature range (unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT
θ _{JC} ⁽¹⁾ Junction-to-case thermal resistance			72.5	°C/W
θ _{JA} Junction-to-ambient thermal resistance			118.5	°C/W

(1) Taken as per JESD51.

THERMAL CHARACTERISTICS FOR HKJ OR HKQ PACKAGE

over operating free-air temperature range (unless otherwise noted)

	PARAME	MIN	TYP	MAX	UNIT	
0	lunction to cope thermal registeres	to ceramic side of case			5.7	°C/W
$\theta^{\rm JC}$	Junction-to-case thermal resistance	to top of case lid (metal side of case)			13.7	°C/vv



ELECTRICAL CHARACTERISTICS: $V_{S+} - V_{S-} = 3.3 V$

At $V_{S+} = 3.3 \text{ V}$, $V_{S-} = 0 \text{ V}$, $V_{OCM} = \text{open}$, $V_{OUT} = 2 \text{ V}_{PP}$ (differential), $R_L = 1 \text{ k}\Omega$ differential, G = 1 V/V, single-ended input, differential output, input and output referenced to midsupply, unless otherwise noted.

		-55	°C to 125	°C		175°C		-55	°C to 210	°C		TEST
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	ТҮР	MAX	MIN	ТҮР	MAX	UNIT	LEVEL ⁽¹⁾
AC PERFORMANCE												
Small-Signal Bandwidth	$V_{OUT} = 100 \text{ mV}_{PP},$ G = 1		104.3			40.7			40.7		MHz	С
	$V_{OUT} = 100 \text{ mV}_{PP},$ G = 2		42			12.5			12.5		MHz	С
	$V_{OUT} = 100 \text{ mV}_{PP},$ G = 5		12.2			3.15			3.15		MHz	С
	$V_{OUT} = 100 \text{ mV}_{PP},$ G = 10		8.1			2.2			2.2		MHz	С
Gain Bandwidth Product	$V_{OUT} = 100 \text{ mV}_{PP},$ G = 10		81			22			22		MHz	С
Large-Signal Bandwidth	$V_{OUT} = 2 V_{PP}, G = 1$		84			22			22		MHz	С
Bandwidth for 0.1-dB Flatness	V_{OUT} = 2 V_{PP} , G = 1		18.1			5.4			5.4		MHz	С
Rising Slew Rate (Differential)	V_{OUT} = 2-V Step, G = 1, R _L = 200 Ω		377.5			353.5			353.5		V/µs	С
Falling Slew Rate (Differential)	V_{OUT} = 2-V Step, G = 1, R _L = 200 Ω		422.5			392.5			392.5		V/µs	С
Overshoot	V_{OUT} = 2-V Step, G = 1, R _L = 200 Ω		6.75			8.85			8.85		%	С
Undershoot	V_{OUT} = 2-V Step, G = 1, R _L = 200 Ω		7.85			11.45			11.45		%	С
Rise Time	V_{OUT} = 2-V Step, G = 1, R _L = 200 Ω		13.5			15.9			15.9		ns	С
Fall Time	V_{OUT} = 2-V Step, G = 1, R _L = 200 Ω		11.4			14.6			14.6		ns	С
Settling Time to 1%	V_{OUT} = 2-V Step, G = 1, R _L = 200 Ω		18.5			23.5			23.5		ns	С
HARMONIC DISTORTIO	N					-			-		-	
2nd harmonic	$ \begin{array}{l} f=1 \ \text{kHz}, \\ V_{\text{OUT}}=1 \ V_{\text{RMS}}, \\ G=1^{(2)}, \\ \text{differential input} \end{array} $		-115			-96			-96		dBc	С
	$\label{eq:f_f_f} \begin{array}{l} f = 1 \mbox{ MHz}, \\ V_{OUT} = 2 \mbox{ V}_{PP}, \mbox{ G} = 1 \end{array}$		-77			-68.5			-68.5		dBc	С
3rd harmonic			-116			-91.5			-91.5		dBc	С
	$\label{eq:f} \begin{array}{l} f=1 \mbox{ MHz}, \\ V_{OUT}=2 \mbox{ V}_{PP}, \mbox{ G}=1 \end{array}$		-80.5			-68.5			-68.5		dBc	С
Second-Order Intermodulation Distortion	Two-tone, $f_1 = 2 \text{ kHz}$, $f_2 = 500 \text{ Hz}$, $V_{OUT} = 1 \text{ V}_{RMS}$ envelope		-91.5			-79.5			-79.5		dBc	С
Third-Order Intermodulation Distortion	Two-tone, $f_1 = 2 \text{ kHz}$, $f_2 = 500 \text{ Hz}$, $V_{OUT} = 1 \text{ V}_{RMS}$ envelope		-95.5			-79.5			-79.5		dBc	С
Input Voltage Noise	f > 10 kHz		9.05			19.95			19.95		nV/√Hz	С
Input Current Noise	f > 100 kHz		1.8			2.45			2.45		pA/√Hz	С
Overdrive Recovery Time	Overdrive = ± 0.5 V		116.5			126			126		ns	С
Output Balance Error	$V_{OUT} = 100 \text{ mV},$ f ≤ 2 MHz (differential input)		-51.5			-45.5			-45.5		dB	С
Closed-Loop Output Impedance	f = 1 MHz (differential)		0.3								Ω	С

Test levels: (A) 100% tested. (B) Limits set by characterization and simulation. (C) Typical value only for information.
 Not directly measureable; calculated using noise gain of 101.



SBOS548D-APRIL 2011-REVISED MAY 2012

ELECTRICAL CHARACTERISTICS: $V_{s_{+}} - V_{s_{-}} = 3.3 V$ (continued)

At $V_{S+} = 3.3 \text{ V}$, $V_{S-} = 0 \text{ V}$, $V_{OCM} = \text{open}$, $V_{OUT} = 2 \text{ V}_{PP}$ (differential), $R_L = 1 \text{ k}\Omega$ differential, G = 1 V/V, single-ended input, differential output, input and output referenced to midsupply, unless otherwise noted.

		-55	°C to 125	°C		175°C		-55	°C to 210	°C		TEST
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT	LEVEL ⁽¹⁾
DC PERFORMANCE				•								
Open-Loop Voltage Gain (A _{OL})			102			81.9			90		dB	А
Input-Referred Offset Voltage			±0.1	±5		±0.13			±0.43	±11.5	mV	А
Input offset voltage drift ⁽³⁾			±1	±28		±10			±2	±50	µV/°C	В
Input Bias Current			±0.75	±3.3		±0.75	±4.5		±0.78	±4.5	μA	А
Input bias current drift ⁽³⁾			±3.3	±14		±4.7			±4.8	±17	nA/°C	В
Input Offset Current			±0.3	±1.7		±0.5	±3.2		±0.5	±3.5	μA	А
Input offset current drift ⁽³⁾			±1.1	±8		±3.6			±1.26	±9	nA/°C	В
INPUT				•								
Common-Mode Input Voltage Low			-0.1	0		-0.1			-0.1	0	V	А
Common-Mode Input Voltage High		1.8	1.9			1.9		1.8	1.9		V	А
Common-Mode Rejection Ratio (CMRR)		80	105			95		74	98		dB	А
Input Resistance			154∥3. 2			12.3∥4 6			12.3∥4 6		kΩ∥pF	С
OUTPUT		1			1			1		I.		
Output Voltage Low			0.09	0.25		0.3			0.09	0.31	V	А
Output Voltage High		2.95	3.11			3.11		2.85	3.05		V	А
Output Current Drive (for linear operation)	$R_L = 50 \ \Omega$		±35 ⁽⁴⁾			±33 ⁽⁴⁾			±33 ⁽⁴⁾		mA	С
POWER SUPPLY												
Specified Operating Voltage		2.5		3.6	2.5		3.6	2.5		3.6	V	А
Quiescent Operating Current, per channel		0.85	1	1.3	0.9	1.16	1.4	0.9	1.1	1.4	mA	A
Power-Supply Rejection Ratio (±PSRR)		66	85		62.5	74		60	80		dB	А
POWER DOWN												
Enable Voltage Threshold	Assured <i>on</i> above 2.2 V		1	2.2		1	2.2		1	2.2	V	A
Disable Voltage Threshold	Assured off below 0.7 V	0.7	1.6		0.7	1.6		0.7	1.6		V	A
Disable Pin Bias Current			1			1			1		μA	С
Power Down Quiescent Current			2			10			10		μA	С
Turn-On Time Delay	Time to V_{OUT} = 90% of final value, V_{IN} = 2 V, R_L = 200 Ω		86.5			99			99		ns	С
Turn-Off Time Delay	Time to V _{OUT} = 10% of original value, V _{IN} = 2 V, R _L = 200 Ω		136			145			144.5		ns	С
VOLTAGE CONTR	OL				. <u></u>							
Small-Signal Bandwidth			21			13			13		MHz	С

(3) Input Offset Voltage Drift, Input Bias Current Drift and Input Offset Current Drift are average values calculated by taking data at -55°C and 125°C, computing the difference and dividing by 180. High temperature drift data is an average value calculated by taking data at -55°C and 210°C, computing the difference and dividing by 265.

(4) Continuous operation with high current loads at elevated temperature may affect product reliability. Refer to operating lifetime chart (Figure 1).



THS4521-HT

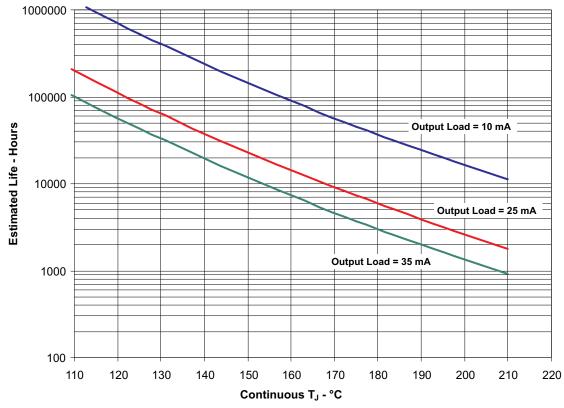
SBOS548D-APRIL 2011-REVISED MAY 2012

www.ti.com

ELECTRICAL CHARACTERISTICS: V_{S+} – V_{S-} = 3.3 V (continued)

At $V_{S+} = 3.3 \text{ V}$, $V_{S-} = 0 \text{ V}$, $V_{OCM} = \text{open}$, $V_{OUT} = 2 \text{ V}_{PP}$ (differential), $R_L = 1 \text{ k}\Omega$ differential, G = 1 V/V, single-ended input, differential output, input and output referenced to midsupply, unless otherwise noted.

		-55	°C to 125	°C		175°C		-55	°C to 210	°C		TEST
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT	LEVEL ⁽¹⁾
Slew Rate			49			39			39		V/µs	С
Gain		0.97	0.99	1.02	0.97	1	1.03	0.97	1	1.03	V/V	А
Common-Mode Offset Voltage from V _{OCM} Input	Measured at V _{OUT} with V _{OCM} input driven, V _{OCM} = 1.65 V ± 0.5 V		±0.2	±4		±0.7			±0.7	±10	mV	A
Input Bias Current	V _{OCM} = 1.65 V ±0.5 V		±0.9	±2.73		±0.27	±2.75		±0.91	±2.75	μA	А
V _{OCM} Voltage Range		1.01	0.8 to 2.5	2.3		0.8 to 2.5		1.09	0.8 to 2.5	2.3	V	А
Input Impedance			114∥3. 6			148∥3. 7			148∥3. 7		kΩ∥pF	С
Default Output Common-Mode Voltage Offset from $(V_{S+}-V_{S-})/2$	Measured at V_{OUT} with V_{OCM} input open		±0.3	±5		±0.6	±10		±0.6	±10	mV	A



- (1) See data sheet for absolute maximum and minimum recommended operating conditions.
- (2) Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).
- (3) The predicted operating lifetime vs. junction temperature is based on reliability modeling using electromigration as the dominant failure mechanism affecting device wearout for the specific device process and design characteristics.
- (4) Device is qualified to ensure reliable operation for 1000 hours at maximum rated temperature. This includes, but is not limited to temperature bake, temperature cycle, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits. For plastic package only.

Figure 1. THS4521SHKJ/SHKQ/SKGD1 Operating Life Derating Chart

TEXAS INSTRUMENTS

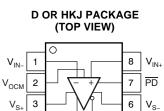
SBOS548D-APRIL 2011-REVISED MAY 2012

V_{OUT+}

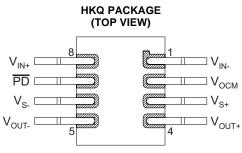
4

www.ti.com

DEVICE INFORMATION



5 V_{OUT-}



HKQ as formed or HKJ mounted dead bug

TERMINAL FUNCTIONS

PIN NO.	NAME	DESCRIPTION
1	V _{IN}	Inverting amplifier input
2	V _{OCM}	Common-mode voltage input
3	V _{S+}	Amplifier positive power-supply input
4	V _{OUT+}	Noninverting amplifier output
5	V _{OUT-}	Inverting amplifier output
6	V _{S-}	Amplifier negative power-supply input. Note that V_{S-} is tied together on multi-channel devices.
7	PD	Power down. \overline{PD} = logic low puts device into low-power mode. \overline{PD} = logic high or open for normal operation.
8	V _{IN+}	Noninverting amplifier input



SBOS548D

SBOS548D-APRIL 2011-REVISED MAY 2012

www.ti.com

TYPICAL CHARACTERISTICS

Table of Graphs⁽¹⁾: $V_{S+} - V_{S-} = 3.3 V$

TITLE	FIGURE
Small-Signal Frequency Response	Figure 2
Large-Signal Frequency Response	Figure 3
Large- and Small-Signal Pulse Response	Figure 4
Slew Rate vs V _{OUT} Step	Figure 5
Overdrive Recovery	Figure 6
10-kHz Output Spectrum on AP Analyzer	Figure 7
Harmonic Distortion vs Frequency	Figure 8
Harmonic Distortion vs Output Voltage at 1 MHz	Figure 9
Harmonic Distortion vs Gain at 1 MHz	Figure 10
Harmonic Distortion vs Load at 1 MHz	Figure 11
Harmonic Distortion vs V _{OCM} at 1 MHz	Figure 12
Two-Tone, Second- and Third-Order Intermodulation Distortion vs Frequency	Figure 13
Single-Ended Output Voltage Swing vs Load Resistance	Figure 14
Main Amplifier Differential Output Impedance vs Frequency	Figure 15
Frequency Response vs C_{LOAD} (R_{LOAD} = 1 k Ω)	Figure 16
$R_O vs C_{LOAD} (R_{LOAD} = 1 k\Omega)$	Figure 17
Rejection Ratio vs Frequency	Figure 18
Turn-on Time	Figure 19
Turn-off Time	Figure 20
Input-Referred Voltage Noise and Current Noise Spectral Density	Figure 21
Main Amplifier Differential Open-Loop Gain and Phase	Figure 22
Output Balance Error vs Frequency	Figure 23
V _{OCM} Small-Signal Frequency Response	Figure 24
V _{OCM} Large-Signal Frequency Response	Figure 25
V _{OCM} Input Impedance vs Frequency	Figure 26

(1) Graphs are plotted for room temperature only and are given only for reference.

1.5

1.0

0.5

0

-0.5

-1.0

-1.5

0

20

40

Time (ns)

Figure 4.

60

Differential V_{OUT} (V)

V_{S+} = 3.3 V

G = 1 V/V

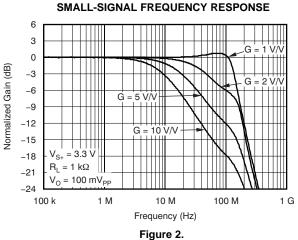
 $R_F = 1 k\Omega$ R_L = 200 Ω

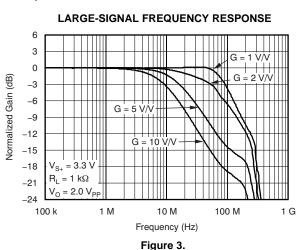


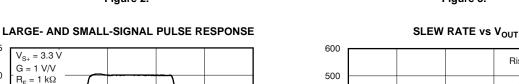
www.ti.com

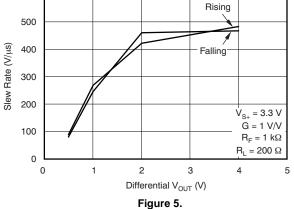
TYPICAL CHARACTERISTICS: $V_{s+} - V_{s-} = 3.3 V$

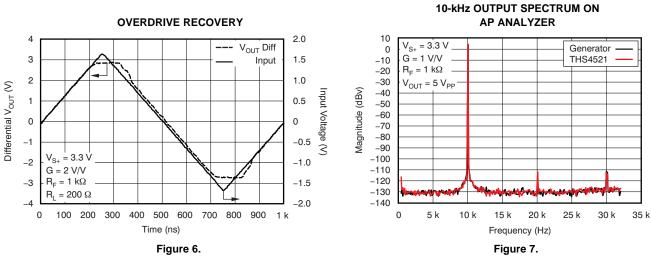
At V_{S+} = +3.3 V, V_{S-} = 0 V, V_{OCM} = open, V_{OUT} = 2 V_{PP} (differential), R_L = 1 k Ω differential, G = 1 V/V, single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted. Graphs are plotted for room temperature only and are given only for reference.











0.5-V Step

2-V Step

100

80



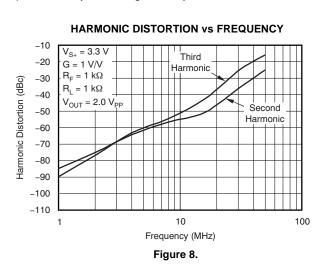
THS4521-HT

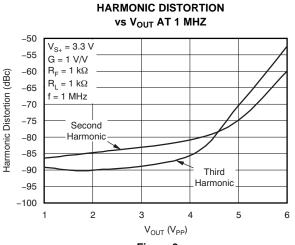
SBOS548D - APRIL 2011 - REVISED MAY 2012

www.ti.com

TYPICAL CHARACTERISTICS: $V_{s_{+}} - V_{s_{-}} = 3.3 V$ (continued)

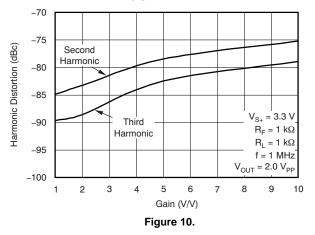
At $V_{S+} = +3.3 \text{ V}$, $V_{S-} = 0 \text{ V}$, $V_{OCM} = \text{open}$, $V_{OUT} = 2 \text{ V}_{PP}$ (differential), $R_L = 1 \text{ k}\Omega$ differential, G = 1 V/V, single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted. Graphs are plotted for room temperature only and are given only for reference.



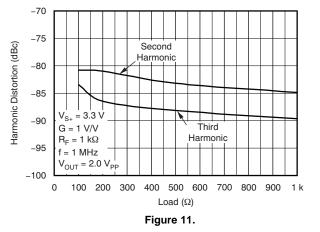




HARMONIC DISTORTION vs GAIN AT 1 MHZ



HARMONIC DISTORTION vs LOAD AT 1 MHZ

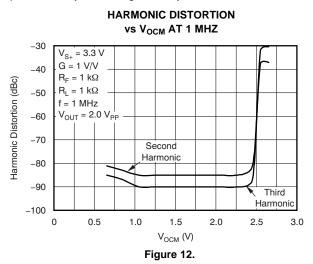


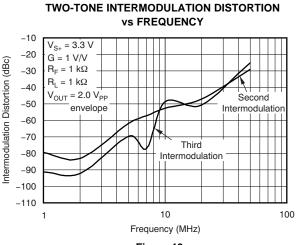


SBOS548D-APRIL 2011-REVISED MAY 2012

TYPICAL CHARACTERISTICS: $V_{s_{+}} - V_{s_{-}} = 3.3 V$ (continued)

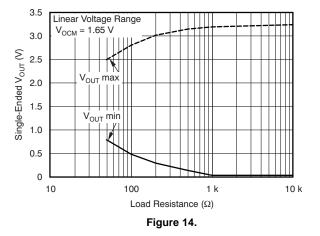
At $V_{S+} = +3.3 \text{ V}$, $V_{S-} = 0 \text{ V}$, $V_{OCM} = \text{open}$, $V_{OUT} = 2 \text{ V}_{PP}$ (differential), $R_L = 1 \text{ k}\Omega$ differential, G = 1 V/V, single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted. Graphs are plotted for room temperature only and are given only for reference.



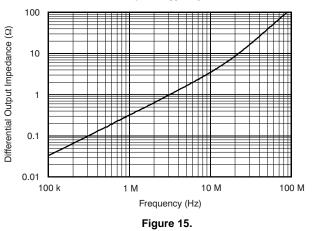




SINGLE-ENDED OUTPUT VOLTAGE SWING vs LOAD RESISTANCE



MAIN AMPLIFIER DIFFERENTIAL OUTPUT IMPEDANCE vs FREQUENCY



TEXAS INSTRUMENTS

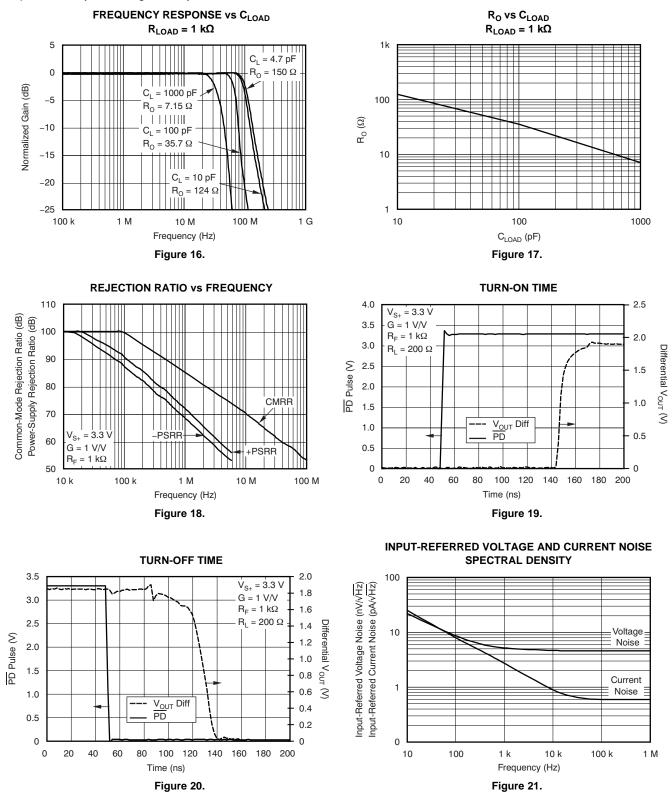
THS4521-HT

SBOS548D - APRIL 2011 - REVISED MAY 2012

www.ti.com

TYPICAL CHARACTERISTICS: $V_{s_{+}} - V_{s_{-}} = 3.3 V$ (continued)

At $V_{S+} = +3.3 \text{ V}$, $V_{S-} = 0 \text{ V}$, $V_{OCM} = \text{open}$, $V_{OUT} = 2 \text{ V}_{PP}$ (differential), $R_L = 1 \text{ k}\Omega$ differential, G = 1 V/V, single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted. Graphs are plotted for room temperature only and are given only for reference.



Copyright © 2011–2012, Texas Instruments Incorporated

13

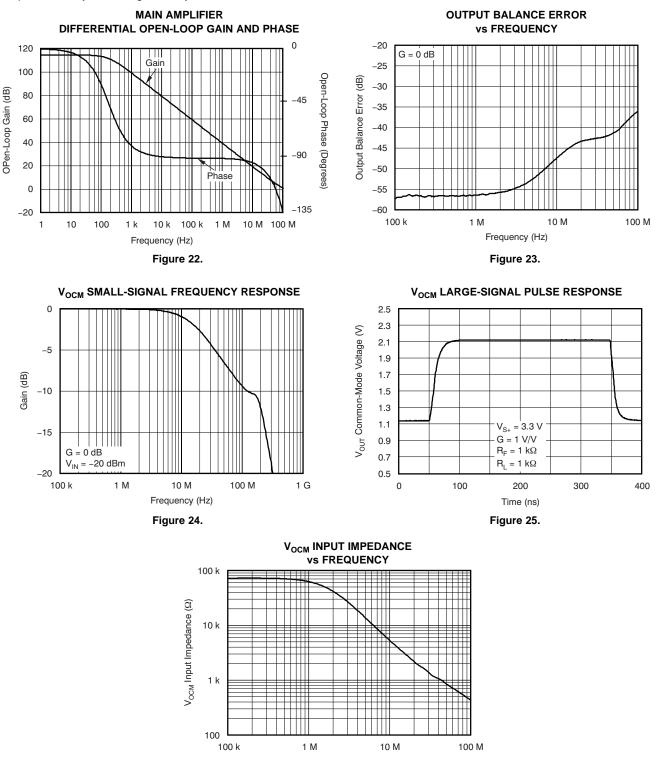
SBOS548D-APRIL 2011-REVISED MAY 2012



www.ti.com

TYPICAL CHARACTERISTICS: $V_{s_{+}} - V_{s_{-}} = 3.3 V$ (continued)

At $V_{S+} = +3.3 \text{ V}$, $V_{S-} = 0 \text{ V}$, $V_{OCM} = \text{open}$, $V_{OUT} = 2 \text{ V}_{PP}$ (differential), $R_L = 1 \text{ k}\Omega$ differential, G = 1 V/V, single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted. Graphs are plotted for room temperature only and are given only for reference.



Frequency (Hz) Figure 26.



SBOS548D - APRIL 2011 - REVISED MAY 2012

TEST CIRCUITS

Overview

The THS4521 is tested with the test circuits shown in this section; all circuits are built using the available THS4521 evaluation module (EVM). For simplicity, power-supply decoupling is not shown; see the layout in the Applications section for recommendations. Depending on the test conditions, component values change in accordance with Table 2 and Table 3, or as otherwise noted. In some cases the signal generators used are ac-coupled and in others they dc-coupled 50- Ω sources. To balance the amplifier when ac-coupled, a 0.22- μ F capacitor and 49.9- Ω resistor to ground are inserted across RIT on the alternate input; when dc-coupled, only the 49.9-Ω resistor to ground is added across R_{IT}. A split power supply is used to ease the interface to common test equipment, but the amplifier can be operated in a single-supply configuration as described in the Applications section with no impact on performance. Also, for most of the tests, except as noted, the devices are tested with single-ended inputs and a transformer on the output to convert the differential output to single-ended because common lab test equipment has single-ended inputs and outputs. Similar or better performance can be expected with differential inputs and outputs.

As a result of the voltage divider on the output formed by the load component values, the amplifier output is attenuated. The **Atten** column in Table 3 shows the attenuation expected from the resistor divider. When using a transformer at the output (as shown in Figure 28), the signal sees slightly more loss because of transformer and line loss; these numbers are approximate.

Table 2. Gain Component Values for Single-Ended Input⁽¹⁾

Gain	R _F	R _G	R _{IT}
1 V/V	1 kΩ	1 kΩ	52.3 Ω
2 V/V	1 kΩ	487 Ω	53.6 Ω
5 V/V	1 kΩ	187 Ω	59.0 Ω
10 V/V	1 kΩ	86.6 Ω	69.8 Ω

1. Gain setting includes $50-\Omega$ source impedance. Components are chosen to achieve gain and 50-

Ω input termination.
Table 3. Load Component Values For 1:1
Differential to Single-Ended Output Transformer ⁽¹⁾

RL	Ro	R _{ot}	Atten
100 Ω	24.9 Ω	Open	6 dB
200 Ω	86.6 Ω	69.8 Ω	16.8 dB
499 Ω	237 Ω	56.2 Ω	25.5 dB
1 kΩ	487 Ω	52.3 Ω	31.8 dB

1. Total load includes $50-\Omega$ termination by the test equipment. Components are chosen to achieve load and $50-\Omega$ line termination through a 1:1 transformer.

Frequency Response

The circuit shown in Figure 27 is used to measure the frequency response of the circuit.

An HP network analyzer is used as the signal source and the measurement device. The output impedance of the HP network analyzer is is dc-coupled and is 50 Ω . R_{IT} and R_G are chosen to impedance-match to 50 Ω and maintain the proper gain. To balance the amplifier, a 49.9- Ω resistor to ground is inserted across R_{IT} on the alternate input.

The output is probed using a Tektronix highimpedance differential probe across the $953-\Omega$ resistor and referred to the amplifier output by adding back the 0.42-dB because of the voltage divider on the output.

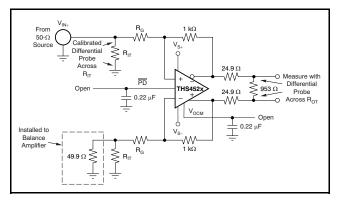


Figure 27. Frequency Response Test Circuit

SBOS548D-APRIL 2011-REVISED MAY 2012

www.ti.com

Distortion

The circuit shown in Figure 28 is used to measure harmonic and intermodulation distortion of the amplifier.

An HP signal generator is used as the signal source and the output is measured with a Rhode and Schwarz spectrum analyzer. The output impedance of the HP signal generator is ac-coupled and is 50 Ω . R_{IT} and R_G are chosen to impedance match to 50 Ω and maintain the proper gain. To balance the amplifier, a 0.22-µF capacitor and 49.9- Ω resistor to ground are inserted across R_{IT} on the alternate input.

A low-pass filter is inserted in series with the input to reduce harmonics generated at the signal source. The level of the fundamental is measured and then a high-pass filter is inserted at the output to reduce the fundamental so it does not generate distortion in the input of the spectrum analyzer.

The transformer used in the output to convert the signal from differential to single-ended is an ADT1–1WT. It limits the frequency response of the circuit so that measurements cannot be made below approximately 1 MHz.

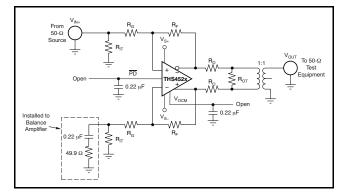


Figure 28. Distortion Test Circuit

Slew Rate, Transient Response, Settling Time, Output Impedance, Overdrive, Output Voltage, and Turn-On/Turn-Off Time

The circuit shown in Figure 29 is used to measure slew rate, transient response, settling time, output impedance, overdrive recovery, output voltage swing, and ampliifer turn-on/turn-off time. Turn-on and turn-off time are measured with the same circuit modified for 50- Ω input impedance on the PD input by replacing the 0.22- μ F capacitor with a 49.9- Ω resistor. For output impedance, the signal is injected at V_{OUT} with V_{IN} open; the drop across the 2x 49.9- Ω resistors is then used to calculate the impedance seen looking into the amplifier output.

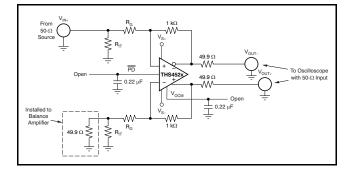


Figure 29. Slew Rate, Transient Response, Settling Time, Output Impedance, Overdrive Recovery, V_{OUT} Swing, and Turn-On/Turn-Off Test Circuit



SBOS548D - APRIL 2011 - REVISED MAY 2012

www.ti.com

Common-Mode and Power-Supply Rejection

The circuit shown in Figure 30 is used to measure the CMRR. The signal from the network analyzer is applied common-mode to the input. Figure 31 is used to measure the PSRR of V_{S+} and V_{S-}. The power supply under test is applied to the network analyzer dc offset input. For both CMRR and PSRR, the output is probed using a Tektronix high-impedance differential probe across the 953- Ω resistor and referred to the amplifier output by adding back the 0.42-dB as a result of the voltage divider on the output. For these tests, the resistors are matched for best results.

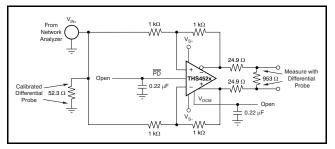


Figure 30. CMRR Test Circuit

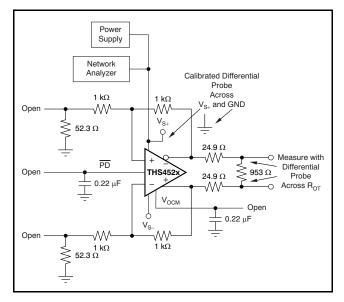


Figure 31. PSRR Test Circuit

V_{OCM} Input

The circuit illustrated in Figure 32 is used to measure the frequency response and input impedance of the V_{OCM} input. Frequency response is measured using a Tektronix high-impedance differential probe, with $R_{CM} = 0~\Omega$ at the common point of V_{OUT+} and V_{OUT-} , formed at the summing junction of the two matched 499- Ω resistors, with respect to ground. The input impedance is measured using a Tektronix high-impedance differential probe at the V_{OCM} input with $R_{CM} = 10~k\Omega$ and the drop across the 10-k Ω resistor is used to calculate the impedance seen looking into the amplifier V_{OCM} input.

The circuit shown in Figure 33 measures the transient response and slew rate of the V_{OCM} input. A 1-V step input is applied to the V_{OCM} input and the output is measured using a 50- Ω oscilloscope input referenced back to the amplifier output.

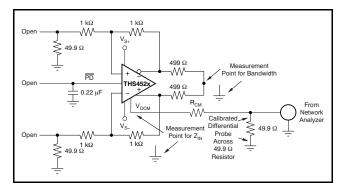


Figure 32. V_{OCM} Input Test Circuit

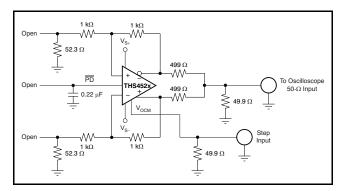


Figure 33. V_{OCM} Transient Response and Slew Rate Test Circuit

TEXAS INSTRUMENTS

SBOS548D-APRIL 2011-REVISED MAY 2012

www.ti.com

APPLICATION INFORMATION

The following circuits show application information for the THS4521. For simplicity, power-supply decoupling capacitors are not shown in these diagrams; the **EVM** see and Lavout *Recommendations* section for suggested guidelines. For more details on the use and operation of fully differential op amps, refer to the Application Report Fully-Differential Amplifiers (SLOA054), available for download from the TI web site at www.ti.com.

Differential Input to Differential Output Amplifier

The THS4521 is fully-differential operational amplifiers that can be used to amplify differential input signals to differential output signals. Figure 34 shows a basic block diagram of the circuit (V_{OCM} and PD inputs not shown). The gain of the circuit is set by R_F divided by R_G .

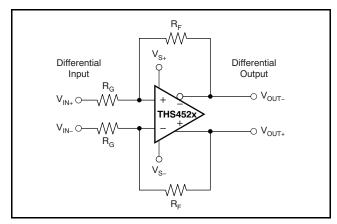


Figure 34. Differential Input to Differential Output Amplifier

Single-Ended Input to Differential Output Amplifier

The THS4521 can also amplify and convert singleended input signals to differential output signals. Figure 35 illustrates a basic block diagram of the circuit (V_{OCM} and \overline{PD} inputs not shown). The gain of the circuit is again set by R_F divided by R_G .

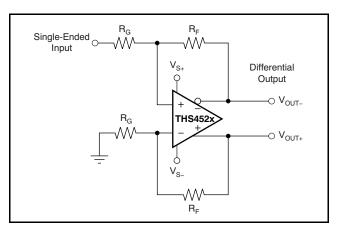


Figure 35. Single-Ended Input to Differential Output Amplifier

Input Common-Mode Voltage Range

The input common-mode voltage of a fully-differential op amp is the voltage at the + and - input pins of the device.

It is important to not violate the input common-mode voltage range (V_{ICR}) of the op amp. Assuming the op amp is in linear operation, the voltage across the input pins is only a few millivolts at most. Therefore, finding the voltage at one input pin determines the input common-mode voltage of the op amp.

Treating the negative input as a summing node, the voltage is given by Equation 1:

$$\left[V_{OUT+} \times \frac{R_{G}}{R_{G} + R_{F}}\right] + \left[V_{IN-} \times \frac{R_{F}}{R_{G} + R_{F}}\right]$$
(1)

To determine the V_{ICR} of the op amp, the voltage at the negative input is evaluated at the extremes of V_{OUT+} . As the gain of the op amp increases, the input common-mode voltage becomes closer and closer to the input common-mode voltage of the source.

Setting the Output Common-Mode Voltage

The output common-model voltage is set by the voltage at the V_{OCM} pin. The internal common-mode control circuit maintains the output common-mode voltage within 5-mV offset (typ) from the set voltage. If left unconnected, the common-mode set point is set to midsupply by internal circuitry, which may be overdriven from an external source.

Copyright © 2011–2012, Texas Instruments Incorporated



SBOS548D - APRIL 2011 - REVISED MAY 2012

www.ti.com

Figure 36 represents the V_{OCM} input. The internal V_{OCM} circuit has typically 23 MHz of –3 dB bandwidth, which is required for best performance, but it is intended to be a dc bias input pin. A 0.22-µF bypass capacitor is recommended on this pin to reduce noise. The external current required to overdrive the internal resistor divider is given approximately by the formula in Equation 2:

$$I_{EXT} = \frac{2V_{OCM} - (V_{S+} - V_{S-})}{50 \text{ k}\Omega}$$

where:

• V_{OCM} is the voltage applied to the V_{OCM} pin (2)

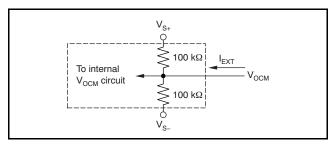


Figure 36. V_{OCM} Input Circuit

Typical Performance Variation with Supply Voltage

The THS4521 provides excellent performance across the specified power-supply range of 2.5 V to 3.3 V with only minor variations. The input and output voltage compliance ranges track with the power supply in nearly a 1:1 correlation. Other changes can be observed in slew rate, output current drive, openloop gain, bandwidth, and distortion.

Single-Supply Operation

To facilitate testing with common lab equipment, the THS4521EVM allows for split-supply operation; most of the characterization data presented in this data sheet is measured using split-supply power inputs. The device can easily be used with a single-supply power input without degrading performance.

Figure 37 shows a dc-coupled single-supply circuit with single-ended inputs. This circuit can also be applied to differential input sources.

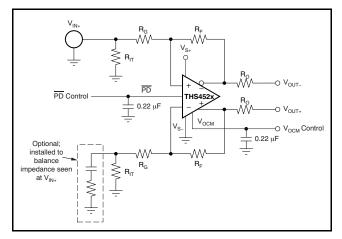


Figure 37. THS4521 DC-Coupled Single-Supply with Single-Ended Inputs

The input common-mode voltage range of the THS4521 is designed to include the negative supply voltage. In the circuit shown in Figure 37, the signal source is referenced to ground. V_{OCM} is set by an external control source or, if left unconnected, the internal circuit defaults to midsupply. Together with the input impedance of the amplifier circuit, R_{IT} provides input termination, which is also referenced to ground.

Note that R_{IT} and optional matching components are added to the alternate input to balance the impedance at signal input.



Low-Power Applications and the Effects of Resistor Values on Bandwidth

For low-power operation, it may be necessary to increase the gain setting resistors values to limit current consumption and not load the source. Using larger value resistors lowers the bandwidth of the THS4521 as a result of the interactions between the resistors, the device parasitic capacitance, and printed circuit board (PCB) parasitic capacitance.

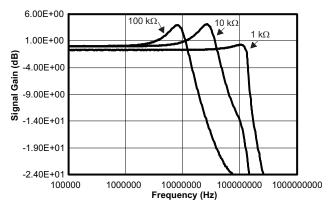


Figure 38. THS4521 Frequency Response with Various Gain Setting and Load Resistor Values

Driving Capacitive Loads

The THS4521 is designed for a nominal capacitive load of 1 pF on each output to ground. When driving capacitive loads greater than 1 pF, it is recommended to use small resistors (R₀) in series with the output, placed as close to the device as possible. Without R_o, capacitance on the output interacts with the output impedance of the amplifier and causes phase shift in the loop gain of the amplifier that reduces the phase margin. This reduction in phase margin results peaking; frequency response overshoot. in undershoot, and/or ringing when a step or squarewave signal is applied; and may lead to instability or oscillation. Inserting Ro isolates the phase shift from the loop gain path and restores the phase margin, but it also limits bandwidth.



SBOS548D-APRIL 2011-REVISED MAY 2012

LAYOUT RECOMMENDATIONS

It is recommended to follow the layout of the external components near to the amplifier, ground plane construction, and power routing as closely as possible. Follow these general guidelines:

- 1. Signal routing should be direct and as short as possible into and out of the op amp circuit.
- 2. The feedback path should be short and direct.
- 3. Ground or power planes should be removed from directly under the amplifier input and output pins.
- 4. An output resistor is recommended in each output lead, placed as near to the output pins as possible.
- 5. Two 0.1-µF power-supply decoupling capacitors should be placed as near to the power-supply pins as possible.
- 6. Two 10-μF power-supply decoupling capacitors should be placed within 1 inch of the device and can be shared among multple analog devices.
- A 0.22-µF capacitor should be placed between the V_{OCM} input pin and ground near to the pin. This capacitor limits noise coupled into the pin.
- 8. The PD pin uses TTL logic levels; a bypass capacitor is not necessary if actively driven, but can be used for robustness in noisy environments whether driven or not.



PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
THS4521HD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
THS4521SHKJ	ACTIVE	CFP	HKJ	8	1	TBD	Call TI	N / A for Pkg Type	
THS4521SHKQ	ACTIVE	CFP	HKQ	8	25	TBD	AU	N / A for Pkg Type	
THS4521SKGD1	ACTIVE	XCEPT	KGD	0	360	TBD	Call TI	N / A for Pkg Type	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF THS4521-HT :

• Catalog: THS4521





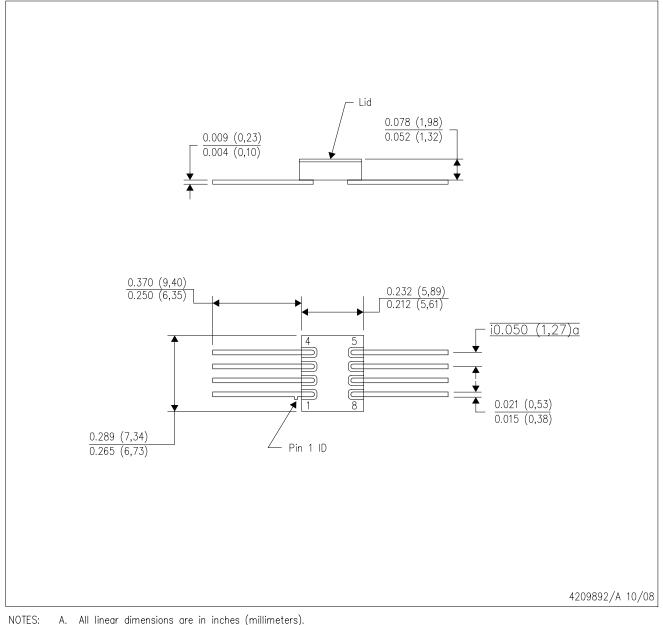
28-May-2012

NOTE: Qualified Version Definitions:

• Catalog - TI's standard catalog product

HKJ (R-CDFP-F8)

CERAMIC DUAL FLATPACK

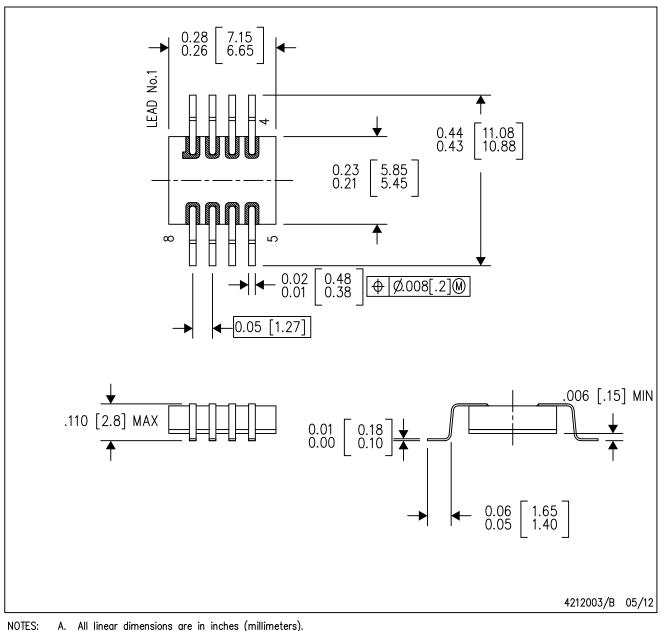


- All linear dimensions are in inches (millimeters).
 - В. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid. D. The terminals will be gold plated.



HKQ (R-CDFP-G8)

CERAMIC GULL WING



- A. All linear dimensions are in inches (millimeters). This drawing is subject to change without notice.
 - Β. C. This package can be hermetically sealed with a metal lid.

 - D. The terminals will be gold plated.E. Lid is not connected to any lead.



D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.



LAND PATTERN DATA



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Mobile Processors	www.ti.com/omap		
Wireless Connectivity	www.ti.com/wirelessconnectivity		
	TI 505 0		

TI E2E Community Home Page

e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2012, Texas Instruments Incorporated