



High Common-Mode Voltage Difference Amplifier

FEATURES

Common-Mode Voltage Range: ±275 V

Minimum CMRR: 90 dB from -40°C to +125°C

DC Specifications:

Maximum Offset Voltage: 1100 μV

Maximum Offset Voltage Drift: 15 µV/°C

- Maximum Gain Error: 0.02%

Maximum Gain Error Drift: 10 ppm/°C

Maximum Gain Nonlinearity: 0.001% FSR

AC Performance:

- Bandwidth: 500 kHz

Typical Slew Rate: 5 V/µs

Wide Supply Range: ±2.0 V to ±18 V

- Maximum Quiescent Current: 900 µA

Output Swing on ±15-V Supplies: ±13.5 V

Input Protection:

Common-Mode: ±500 VDifferential: ±500 V

APPLICATIONS

High-Voltage Current Sensing

Battery Cell Voltage Monitoring

Power-Supply Current Monitoring

Motor Controls

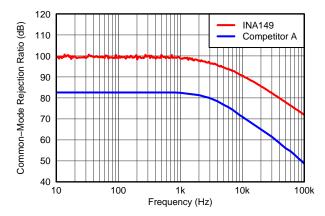
Replacement for Isolation Circuits

DESCRIPTION

The INA149 is a precision unity-gain difference amplifier with a very high input common-mode voltage range. It is a single, monolithic device that consists of a precision op amp and an integrated thin-film resistor network. The INA149 can accurately measure small differential voltages in the presence of common-mode signals up to ±275 V. The INA149 inputs are protected from momentary common-mode or differential overloads of up to 500 V.

In many applications, where galvanic isolation in not required, the INA149 can replace isolation amplifiers. This ability can eliminate costly isolated input side power supplies and the associated ripple, noise, and quiescent current. The excellent 0.0005% nonlinearity and 500-kHz bandwidth of the INA149 are superior to those of conventional isolation amplifiers.

The INA149 is pin-compatible with the INA117 and INA148 type high common-mode voltage amplifiers and offers improved performance over both devices. The INA149 is available in the SOIC-8 package with operation specified over the extended industrial temperature range of –40°C to +125°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.





This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING		
INA149	SOIC-8	D	INA149AID		

⁽¹⁾ For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		INA149	UNIT	
Supply voltage	(V+) – (V–)	40	V	
Input voltage range	Continuous	300	V	
Common-mode and differential, 10	s	500	V	
Maximum Voltage on REF _A and RE	F _B	(V-) - 0.3 to (V+) + 0.3	V	
Input current on any input pin (2)		10 mA		
Output short-circuit current duration	1	Indefinite		
Operating temperature range		-55 to +150	°C	
Storage temperature range		-65 to +150	°C	
Junction temperature		+150	°C	
	Human body model (HBM)	1500	V	
ESD rating	Charged device model (CDM)	1000	V	
	Machine model (MM)	100	V	

⁽¹⁾ Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

Submit Documentation Feedback

Copyright © 2011, Texas Instruments Incorporated

⁽²⁾ REF_A and REF_B are diode clamped to the power-supply rails. Signals applied to these pins that can swing more than 0.3 V beyond the supply rails should be limited to 10 mA or less.

www.ti.com

ELECTRICAL CHARACTERISTICS: V + = +15 V and V - = -15 V

At T_A = +25°C, R_L = 2 k Ω connected to ground, and V_{CM} = REF_A = REF_B = GND, unless otherwise noted.

		INA149			
PARAMETER	TEST CONDITIONS	MIN TYP MA			UNIT
GAIN		-		"	
Initial	V _{OUT} = ±10.0 V		1		V/V
Gain error	V _{OUT} = ±10.0 V		±0.005	±0.02	%FSR
Gain	vs temperature, $T_A = -40^{\circ}\text{C}$ to +125°C		±1.5	±10	ppm/°C
Nonlinearity			±0.0005	±0.001	%FSR
OFFSET VOLTAGE					
			350	1100	μV
Initial offset	vs temperature, $T_A = -40^{\circ}\text{C}$ to +125°C		3	15	μV/°C
	vs supply (PSRR), V _S = ±2 V to ±18 V	90	120		dB
INPUT				'	
	Differential		800		kΩ
Impedance	Common-mode		200		kΩ
	Differential	-13.5		13.5	V
Voltage range	Common-mode	-275		275	V
	At dc, V _{CM} = ±275 V	90	100		dB
Common-mode rejection	vs temperature, $T_A = -40^{\circ}$ C to +125°C, at dc	90			dB
(CMRR)	At ac, 500 Hz, V _{CM} = 500 V _{PP}	90			dB
	At ac, 1 kHz, V _{CM} = 500 V _{PP}		90		dB
OUTPUT		1		<u> </u>	
Voltage range		-13.5		13.5	V
Short-circuit current			±25		mA
Capacitive load drive	No sustained oscillations		10		nF
OUTPUT NOISE VOLTAGE				'	
0.01 Hz to 10 Hz			20		μV_{PP}
10 kHz			550		nV/√ Hz
DYNAMIC RESPONSE		'		*	
Small-signal bandwidth			500		kHz
Slew rate	V _{OUT} = ±10-V step	1.7	5		V/µs
Full-power bandwidth	$V_{OUT} = 20 V_{PP}$		32		kHz
Settling time	0.01%, V _{OUT} = 10-V step		7		μs
POWER SUPPLY		'		*	
Voltage range		±2		±18	V
	$V_S = \pm 18 \text{ V}, V_{OUT} = 0 \text{ V}$		810	900	μA
Quiescent current	vs temperature, $T_A = -40^{\circ}\text{C}$ to +125°C			1.1	mA
TEMPERATURE RANGE		1		· L	
Specified		-40		+125	°C
Operating		-55		+150	°C
Storage		-65		+150	°C

Copyright © 2011, Texas Instruments Incorporated



ELECTRICAL CHARACTERISTICS: V+ = 5 V and V- = 0 V

At T_A = +25°C, R_L = 2 k Ω connected to 2.5 V, and V_{CM} = REF_A = REF_B = 2.5 V, unless otherwise noted.

		INA149			
PARAMETER	TEST CONDITIONS	MIN TYP	MAX	UNIT	
GAIN			•		
Initial	V _{OUT} = 1.5 V to 3.5 V	1		V/V	
Gain error	V _{OUT} = 1.5 V to 3.5 V	±0.005		%FSR	
Gain	vs temperature, $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	±1.5		ppm/°C	
Nonlinearity		±0.0005		%FSR	
OFFSET VOLTAGE			*		
		350		μV	
Initial offset	vs temperature, $T_A = -40^{\circ}C$ to $+125^{\circ}C$	3		μV/°C	
	vs supply (PSRR), $V_S = 4 \text{ V to 5 V}$	120		dB	
INPUT					
	Differential	800		kΩ	
Impedance	Common-mode	200		kΩ	
	Differential	1.5	3.5	V	
Voltage range	Common-mode	-20	25	V	
	At dc, $V_{CM} = -20 \text{ V}$ to 25 V	100		dB	
	vs temperature, $T_A = -40^{\circ}\text{C}$ to +125°C, at dc	100		dB	
Common-mode rejection	At ac, 500 Hz, V _{CM} = 49 V _{PP}	100		dB	
	At ac, 1 kHz, V _{CM} = 49 V _{PP}	90		dB	
OUTPUT					
Voltage range		1.5	3.5	V	
Short-circuit current		±15		mA	
Capacitive load drive	No sustained oscillations	10		nF	
OUTPUT NOISE VOLTAGE					
0.01 Hz to 10 Hz		20		μV _{PP}	
10 kHz		550		nV/√Hz	
DYNAMIC RESPONSE					
Small-signal bandwidth		500		kHz	
Slew rate	V _{OUT} = 2 V _{PP} step	5		V/µs	
Full-power bandwidth	$V_{OUT} = 2 V_{PP}$	32		kHz	
Settling time	0.01%, V _{OUT} = 2 V _{PP} step	7		μs	
POWER SUPPLY					
Voltage range		5		V	
	V _S = 5 V	810		μA	
Quiescent current	vs temperature, $T_A = -40^{\circ}\text{C}$ to +125°C	1		mA	

www.ti.com

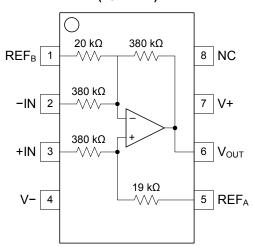
THERMAL INFORMATION

		INA149		
	THERMAL METRIC ⁽¹⁾	D (SOIC)	UNITS	
		8 PINS		
θ_{JA}	Junction-to-ambient thermal resistance	110		
θ_{JCtop}	Junction-to-case (top) thermal resistance	57		
θ_{JB}	Junction-to-board thermal resistance	54	°C // //	
Ψлт	Junction-to-top characterization parameter	11	°C/W	
ΨЈВ	Junction-to-board characterization parameter	53		
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A		

⁽¹⁾ For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

PIN CONFIGURATION

D PACKAGE SOIC-8 (TOP VIEW)



PIN DESCRIPTIONS

NAME	NO.	DESCRIPTION
–IN	2	Inverting input
+IN	3	Noninverting input
NC	8	No internal connection
REFA	5	Reference input
REF _B	1	Reference input
V–	4	Negative power supply
V+	7	Positive power supply ⁽¹⁾
V _{OUT}	6	Output

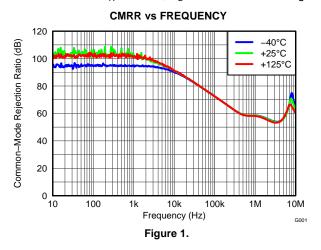
(1) In this document, (V+) – (V–) is referred to as V_S .

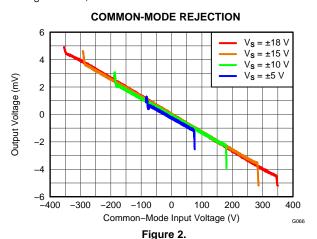
Copyright © 2011, Texas Instruments Incorporated

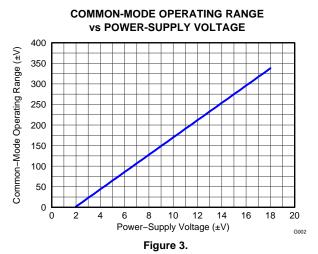


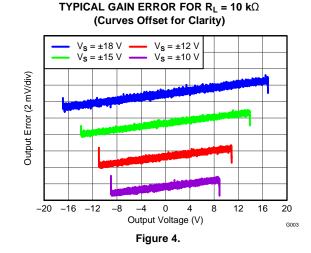
TYPICAL CHARACTERISTICS

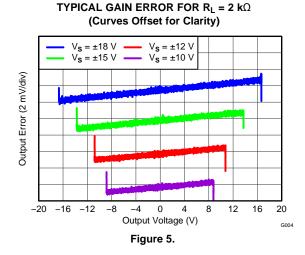
At T_A = +25°C, R_L = 2 k Ω connected to ground, and V_S = ±15 V, unless otherwise noted.

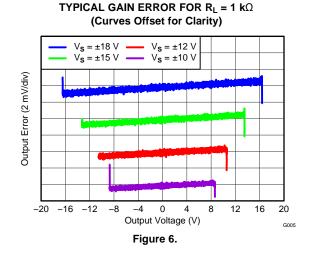














At $T_A = +25$ °C, $R_L = 2 \text{ k}\Omega$ connected to ground, and $V_S = \pm 15 \text{ V}$, unless otherwise noted.

TYPICAL GAIN ERROR FOR LOW SUPPLY VOLTAGES (Curves Offset for Clarity)

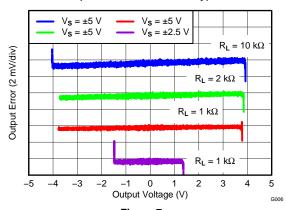


Figure 7.

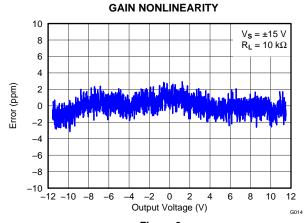


Figure 8.

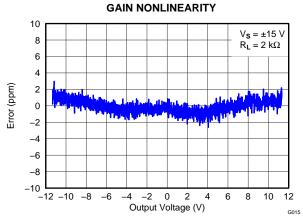
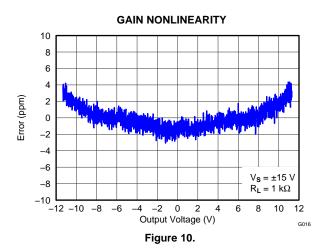


Figure 9.

GAIN NONLINEARITY



OUTPUT VOLTAGE vs LOAD CURRENT

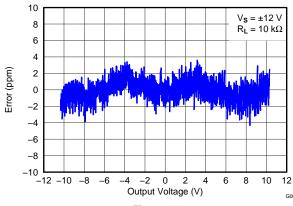
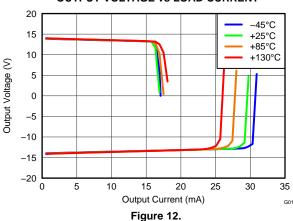


Figure 11.





At $T_A = +25$ °C, $R_L = 2 \text{ k}\Omega$ connected to ground, and $V_S = \pm 15 \text{ V}$, unless otherwise noted.

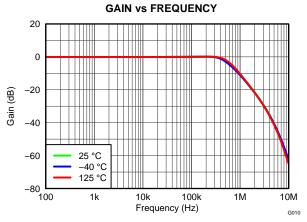


Figure 13.

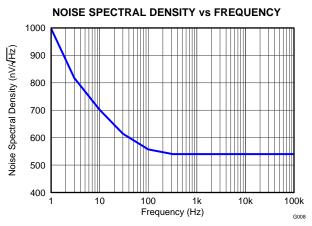


Figure 14.

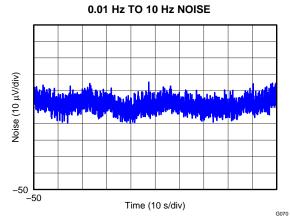
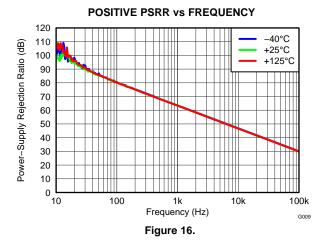
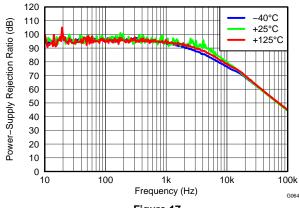


Figure 15.

NEGATIVE PSRR vs FREQUENCY



MAXIMUM POWER DISSIPATION vs TEMPERATURE





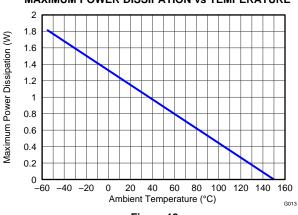


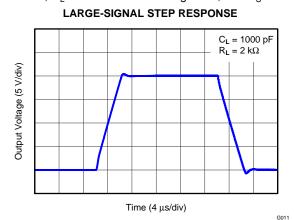
Figure 18.

G012



TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, R_L = 2 k Ω connected to ground, and V_S = ±15 V, unless otherwise noted.

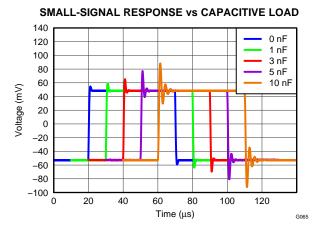


SMALL-SIGNAL STEP RESPONSE



Figure 19.

Figure 20.



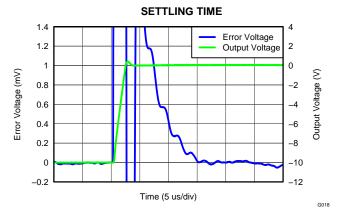
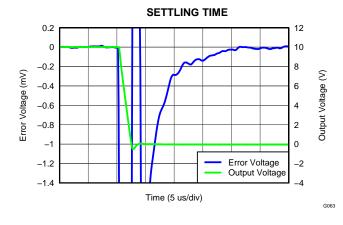


Figure 21.

Figure 22.



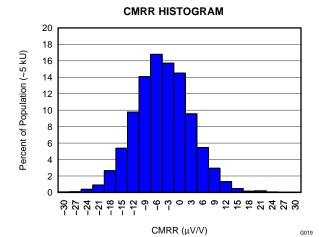
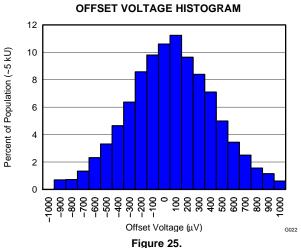


Figure 23.

Figure 24.



At T_A = +25°C, R_L = 2 k Ω connected to ground, and V_S = ±15 V, unless otherwise noted.



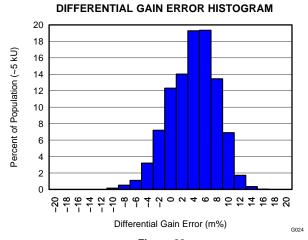
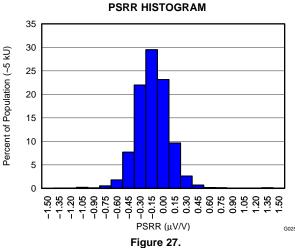
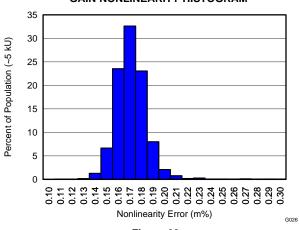


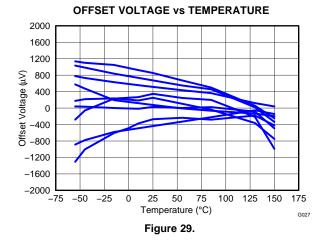
Figure 26.



GAIN NONLINEARITY HISTOGRAM



27. Figure 28.



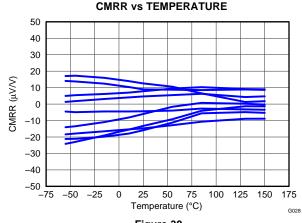
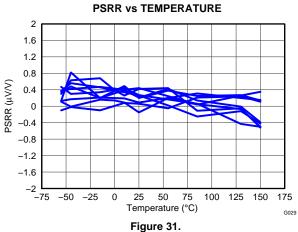
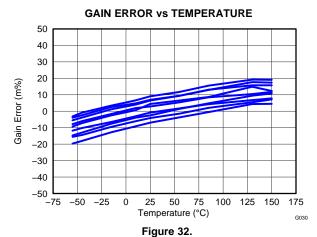


Figure 30.

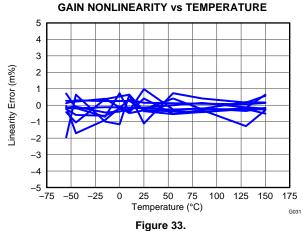


At T_A = +25°C, R_L = 2 k Ω connected to ground, and V_S = ±15 V, unless otherwise noted.

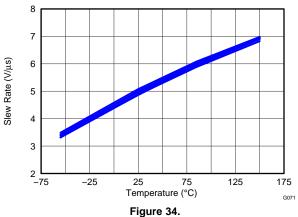




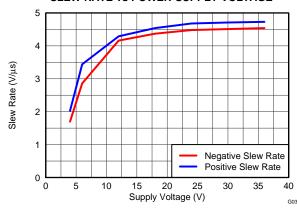




SLEW RATE vs TEMPERATURE



SLEW RATE vs POWER-SUPPLY VOLTAGE



QUIESCENT CURRENT vs TEMPERAUTRE

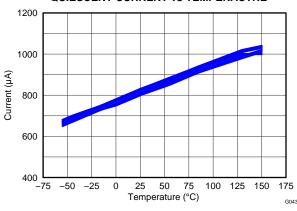
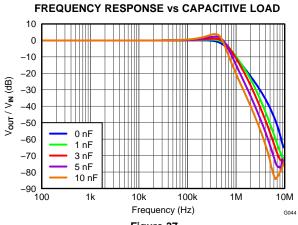


Figure 35.

Figure 36.

At T_A = +25°C, R_L = 2 k Ω connected to ground, and V_S = ±15 V, unless otherwise noted.



QUIESCENT CURRENT vs SUPPLY VOLTAGE

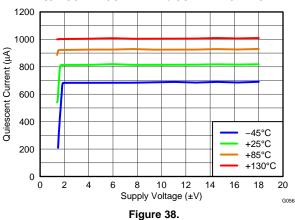
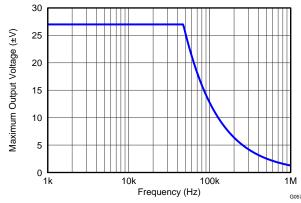


Figure 37.





OVERLOAD RECOVERY

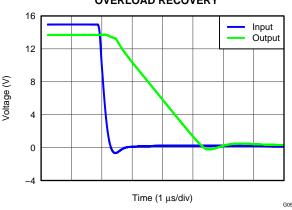


Figure 39.

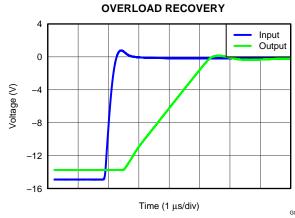


Figure 40.

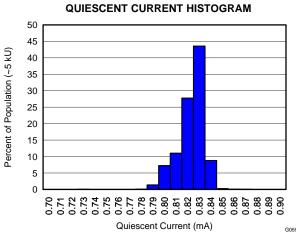


Figure 41.

Figure 42.



APPLICATION INFORMATION

BASIC INFORMATION

Figure 43 shows the basic connections required for dual-supply operation. Applications with noisy or high-impedance power-supply lines may require decoupling capacitors placed close to the device pins. The output voltage is equal to the differential input voltage between pins 2 and 3. The common-mode input voltage is rejected. Figure 44 shows the basic connections required for single-supply operation.

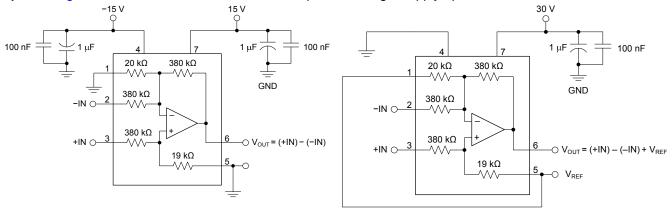


Figure 43. Basic Power and Signal Connections for Figure 44. Basic Power and Signal Connections for **Dual-Supply Operation**

Single-Supply Operation

TRANSFER FUNCTION

Most applications use the INA149 as a simple unity-gain difference amplifier. The transfer function is given in Equation 1:

$$V_{OLIT} = (+IN) - (-IN) \tag{1}$$

Some applications, however, apply voltages to the reference terminals (REF_A and REF_B). The complete transfer function is given in Equation 2:

$$V_{OUT} = (+IN) - (-IN) + 20 \times REF_A - 19 \times REF_B$$
 (2)

COMMON-MODE RANGE

The high common-mode range of the INA149 is achieved by dividing down the input signal with a high precision resistor divider. This resistor divider brings both the positive input and the negative input within the input range of the internal operational amplifier. This input range depends on the supply voltage of the INA149.

Both Figure 2 and Figure 3 can be used to determine the maximum common-mode range for a specific supply voltage. The maximum common-mode range can also be calculated by ensuring that both the positive and the negative input of the internal amplifier are within 1.5 V of the supply voltage.

In case the voltage at the inputs of the internal amplifier exceeds the supply voltage, the internal ESD diodes start conducting current. This current must be limited to 10 mA to make sure not to exceed the absolute maximum ratings for the device.

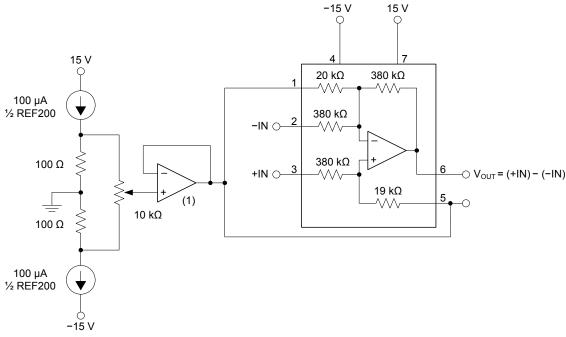


COMMON-MODE REJECTION

Common-mode rejection (CMR) of the INA149 depends on the input resistor network, which is laser-trimmed for accurate ratio matching. To maintain high CMR, it is important to have low source impedance driving the two inputs. A 75- Ω resistance in series with pins 2 or 3 decreases the common-mode rejection ratio (CMRR) from 100 dB (typical) to 74 dB.

Resistance in series with the reference pins also degrades CMR. A 4- Ω resistance in series with pins 1 or 5 decreases CMRR from 100 dB to 74 dB.

Most applications do not require trimming. Figure 45 shows an optional circuit that may be used for trimming offset voltage and common-mode rejection.



(1) The OPA171 (a 36-V, low-power, RRO, general-purpose operational amplifier) can be used for this application.

Figure 45. Offset Voltage Trim Circuit



MEASURING CURRENT

The INA149 can be used to measure a current by sensing the voltage drop across a series resistor, R_S. Figure 46 shows the INA149 used to measure the supply currents of a device under test.

The sense resistor imbalances the input resistor matching of the INA149, thus degrading its CMR. Also, the input impedance of the INA149 loads $R_{\rm S}$, causing gain error in the voltage-to-current conversion. Both of these errors can be easily corrected.

The CMR error can be corrected with the addition of a compensation resistor (R_C), equal to the value of R_S , as shown in Figure 46. If R_S is less than 5 Ω , degradation in the CMR is negligible and R_C can be omitted. If R_S is larger than approximately 1 $k\Omega$, trimming R_C may be required to achive greater than 90-dB CMR. This error is caused by the INA149 input impedance mismatch.

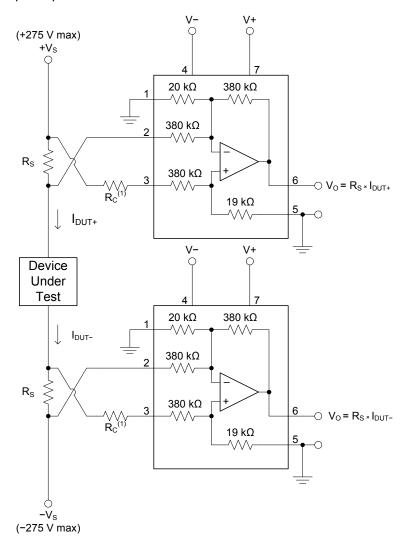


Figure 46. Measuring Supply Currents of a Device Under Test

If R_S is more than approximately 50 Ω , the gain error is greater than the 0.02% specification of the INA149. This gain error can be corrected by slightly increasing the value of R_S . The corrected value (R_S ') can be calculated by R_S ' = $R_S \times 380 \text{ k}\Omega/(380 \text{ k}\Omega - R_S)$

Example: For a 1-V/mA transfer function, the nominal, uncorrected value for R_S would be 1 k Ω . A slightly larger value ($R_S' = 1002.6 \Omega$), compensates for the gain error as a result of loading.

The 380-k Ω term in the equation for R_S' has a tolerance of 25%, thus sense resistors above approximately 400 Ω may require trimming to achive gain accuracy better than 0.02%.

Copyright © 2011, Texas Instruments Incorporated

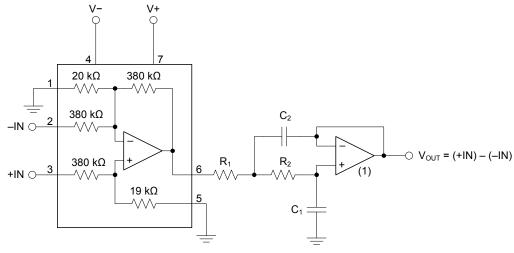


NOISE PERFORMANCE

The wideband noise performane of the INA149 is dominated by the internal resistor network. The thermal or *Johnson noise* of these resistors measures approximately 550 nV/ $\sqrt{\text{Hz}}$. The internal op amp contributes virtually no excess noise at frequencies above 100 Hz.

Many applications may be satisfied with less than the full 500-kHz bandwidth of the INA149. In these cases, the noise can be reduced with a low-pass filter on the output. The two-pole filter shown in Figure 47 limits bandwidth and reduces noise. Because the INA149 has a 1/f noise corner frequency of approximately 100 Hz, a cutoff frequency below 100 Hz does not further reduce noise.

Component values for different filter frequencies are shown in Table 1.



(1) For most applications, the OPA171 can be used as an operational amplifier. For directly driving successive-approximation register (SAR) data converters, the OPA140 is a good choice.

Figure 47. Output Filter for Noise Reduction

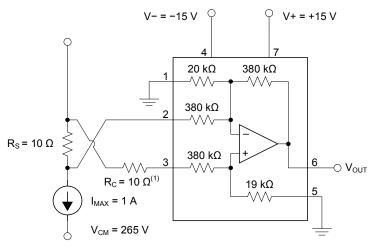
Table 1. Components Values for Different Filter Bandwidths

BUTTERWORTH LOW-PASS (f _{-3 dB})	OUTPUT NOISE (mV _{PP})	R ₁	R ₂	C ₁	C ₂
200 kHz	1.8		No	filter	
100 kHz	1.1	11 kΩ	11.3 kΩ	100 pF	200 pF
10 kHz	0.35	11 kΩ	11.3 kΩ	1 nF	2 nF
1 kHz	0.11	11 kΩ	11.3 kΩ	10 nF	20 nF
100 Hz	0.05	11 kΩ	11.3 kΩ	0.1 μF	0.2 μF



ERROR BUDGET ANALYSIS

The following error budget analysis demonstrates the importance of a high common-mode rejection ratio when measuring small differential signals in the presence of high common-mode voltages. Figure 48 shows a typical current measurement application.



(1) See the *Measuring Current* section for details about R_C.

Figure 48. Typical Current Measurement Application

The maximum current through the shunt resistor (R_S) is 1 A and generates a full-scale voltage drop of 10 V. All error sources in this calculation are shown in relation to this full-scale voltage. The common-mode voltage in this scenario is 265 V and the temperature range is from room temperature (+25°C) to +85°C. Table 2 shows the dominant error sources for the INA149 and a competitor device.

ERROR (ppm of FS) **ERROR INA149 SOURCE INA149 COMPETIOR A COMPETITOR A** Accuracy, $T_A = +25^{\circ}C$ Initial gain error 0.02% FS 0.05% FS 200 500 Offset voltage 1100 µV 1000 μV 110 100 $265 \text{ V/90 dB} = 8380 \,\mu\text{V}$ $265 \text{ V/77 dB} = 37432 \,\mu\text{V}$ Common mode 838 3743 Total acuracy error 1148 4343 Temperature drift 10 ppm/°C × 60°C Gain 10 ppm/°C × 60°C 600 600 10 μV/°C × 60°C 20 μV/°C × 60°C Offset voltage 60 120 660 **Total drift error** 720 **Total error** 1808 5063

Table 2. Error Budget Analysis

If a smaller shunt resistor is used, the full-scale voltage drop is also smaller. A shunt resistor of 1 Ω causes a 1-V voltage drop with a current of 1 A flowing through it. The error of 1808 ppm for a full-scale voltage of 10 V becomes 18080 ppm (1.6%) for a full-scale voltage of only 1 V.

This example demonstrates that the dominate source of error, even over temperature, comes from the CMRR specification of the devices. The common-mode error is 46% of the total error for the INA149 and 74% of the total error for the competitor device.



BATTERY CELL VOLTAGE MONITOR

The INA149 can be used to measure the voltages of single cells in a stacked battery pack. Figure 49 shows an examples for such an application.

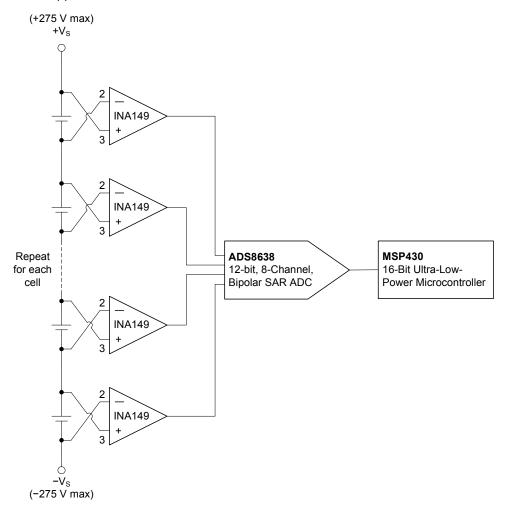


Figure 49. Battery Cell Voltage Monitor

3-Mar-2012

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
INA149AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
INA149AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF INA149:

Enhanced Product: INA149-EP

NOTE: Qualified Version Definitions:





3-Mar-2012

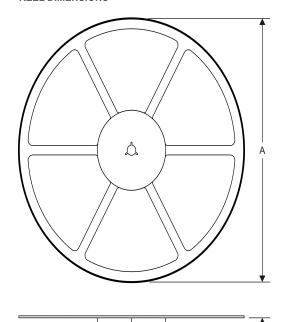
• Enhanced Product - Supports Defense, Aerospace and Medical Applications

PACKAGE MATERIALS INFORMATION

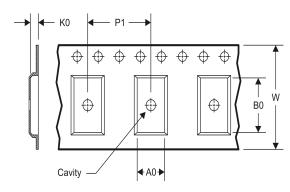
www.ti.com 12-Dec-2011

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA149AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

www.ti.com 12-Dec-2011



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
INA149AIDR	SOIC	D	8	2500	346.0	346.0	29.0	

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.



D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

Applications

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

.ti.com/automotive
.ti.com/communications
.ti.com/computers
.ti.com/consumer-apps
r.ti.com/energy
.ti.com/industrial
v.ti.com/medical
.ti.com/security
.ti.com/space-avionics-defense
v.ti.com/video
ti.

Wireless Connectivity <u>www.ti.com/wirelessconnectivity</u>

OMAP Mobile Processors www.ti.com/omap

Products

TI E2E Community Home Page

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2012, Texas Instruments Incorporated

e2e.ti.com