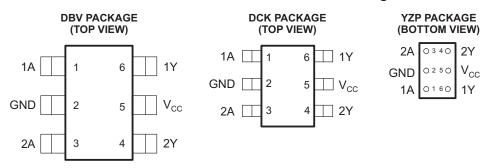


FEATURES

- Available in the Texas Instruments NanoFree™ Package
- Optimized for 1.8-V Operation and Is 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- Sub-1-V Operable
- Unbuffered Outputs
- Max t_{nd} of 1.9 ns at 1.8 V

- Low Power Consumption, 10 μA at 1.8 V
- ±8-mA Output Drive at 1.8 V
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

This dual inverter is operational at 0.8-V to 2.7-V V_{CC}, but is designed specifically for 1.65-V to 1.95-V V_{CC} operation.

The SN74AUC2GU04 contains two inverters with unbuffered outputs and performs the Boolean function $Y = \overline{A}$.

NanoFree[™] package technology is a major breakthrough in IC packaging concepts, using the die as the package.

For more information about AUC Little Logic devices, please refer to the TI application report, *Applications of Texas Instruments AUC Sub-1-V Little Logic Devices*, literature number SCEA027.

T _A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING ⁽²⁾		
-40°C to 85°C	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	SN74AUC2GU04YZPR	UD_		
	SOT (SOT-23) – DBV	Reel of 3000	SN74AUC2GU04DBVR	UU4_		
	SOT (SC-70) – DCK	Reel of 3000	SN74AUC2GU04DCKR	UD_		

ORDERING INFORMATION

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

(2) DBV/DCK: The actual top-side marking has one additional character that designates the assembly/test site. YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoFree is a trademark of Texas Instruments.

SN74AUC2GU04 **DUAL INVERTER GATE**

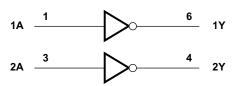
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FUNCTION TABLE (EACH INVERTER)

INPUT A	OUTPUT Y
Н	L
L	Н

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	3.6	V
VI	Input voltage range ⁽²⁾	-0.5	3.6	V	
Vo	Output voltage range ⁽²⁾		-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V ₁ < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
I _O	Continuous output current			±20	mA
	Continuous current through V_{CC} or GND			±100	mA
		DBV package		165	
θ_{JA}	Package thermal impedance ⁽³⁾	DCK package		259	°C/W
		YZP package		123	
T _{stg}	Storage temperature range		-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed. (2)

(3) The package thermal impedance is calculated in accordance with JESD 51-7.

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Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT
V_{CC}	Supply voltage		0.8	2.7	V
VIH	High-level input voltage	I _O = −100 μA	$0.65 imes V_{CC}$		V
V _{IL}	Low-level input voltage	I _O = −100 μA		$0.35 \times V_{CC}$	V
VI	Input voltage		0	3.6	V
Vo	Output voltage		0	V _{CC}	V
		V _{CC} = 0.8 V		-0.7	
		V _{CC} = 1.1 V		-3	
I _{OH}	High-level output current	V _{CC} = 1.4 V		-5	mA
		V _{CC} = 1.65 V		-8	
		$V_{CC} = 2.3 V$		-9	
		V _{CC} = 0.8 V		0.7	
		V _{CC} = 1.1 V		3	
I _{OL}	Low-level output current	V _{CC} = 1.4 V		5	mA
		V _{CC} = 1.65 V		8	
		$V_{CC} = 2.3 V$		9	
$\Delta t/\Delta v$	Input transition rise or fall rate			20	ns/V
T _A	Operating free-air temperature		-40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST	CONDITIONS	V _{cc}	MIN	TYP ⁽¹⁾	MAX	UNIT	
	I _{OH} = −100 μA		0.8 V to 2.7 V	V _{CC} - 0.1			ĺ	
	I _{OH} = -0.7 mA		0.8 V		0.55			
N/	I _{OH} = -3 mA		1.1 V	0.8			v	
V _{OH}	I _{OH} = -5 mA	V _{IL} = GND	1.4 V	1			V	
	I _{OH} = -8 mA		1.65 V	1.2				
	I _{OH} = -9 mA		2.3 V	1.8				
	I _{OL} = 100 μA		0.8 V to 2.7 V			0.2		
	I _{OL} = 0.7 mA		0.8 V		0.25			
N/	I _{OL} = 3 mA		1.1 V			0.3	v	
V _{OL}	$I_{OL} = 5 \text{ mA}$	$V_{IH} = V_{CC}$	1.4 V			0.4	v	
	I _{OL} = 8 mA		1.65 V	0.4		0.45		
	I _{OL} = 9 mA		2.3 V			0.6		
I _I A inputs	$V_{I} = V_{CC}$ or GND		0 to 2.7 V			±5	μΑ	
I _{CC}	$V_I = V_{CC}$ or GND,	I _O = 0	0.8 V to 2.7 V			10	μΑ	
CI	$V_I = V_{CC}$ or GND		2.5 V		2.5		pF	

(1) All typical values are at $T_A = 25^{\circ}C$.

SN74AUC2GU04 DUAL INVERTER GATE

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Switching Characteristics

over recommended operating free-air temperature range, $C_L = 15 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)		V _{CC} = 0.8 V	V_{CC} = 1.2 V ± 0.1 V		V_{CC} = 1.5 V ± 0.1 V		V _{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V \pm 0.2 V		UNIT	
			TYP	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
t _{pd}	А	Y	6.2	0.7	3.1	0.7	2.2	0.6	1.1	1.9	0.5	1.4	ns

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 30 \text{ pF}$ (unless otherwise noted) (see Figure 1)

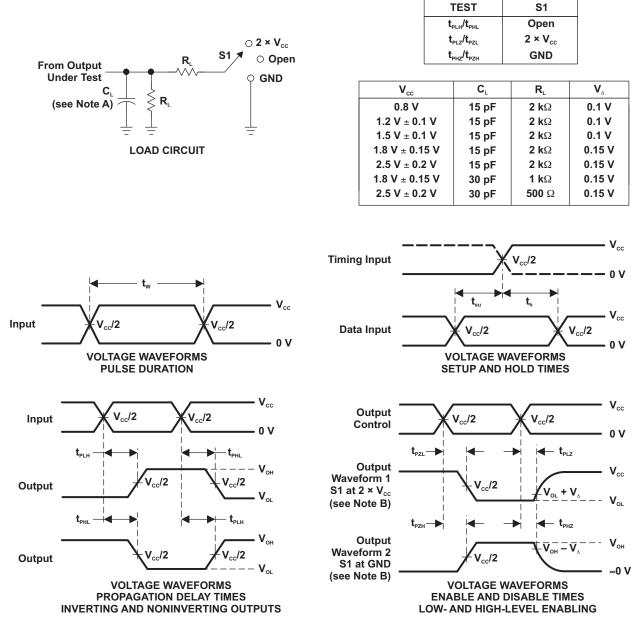
PARAMETER	FROM (INPUT)	TO (OUTPUT)		_c = 1.8 \ 0.15 V	V	V_{CC} = 2.5 V ± 0.2 V		UNIT
		(001101)	MIN	TYP	MAX	MIN	MAX	
t _{pd}	А	Y	0.7	1.6	2.7	0.5	2	ns

Operating Characteristics

 $T_A = 25^{\circ}C$

PARAMETER	TEST CONDITIONS	V _{CC} = 0.8 V TYP	V _{CC} = 1.2 V TYP	V _{CC} = 1.5 V TYP	V _{CC} = 1.8 V TYP	V _{CC} = 2.5 V TYP	UNIT
C _{pd} Power dissipation capacitance	f = 10 MHz	4.5	4.5	4.5	4.5	5.5	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_{L} includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z₀ = 50 Ω,
- slew rate ≥ 1 V/ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. $t_{_{PLZ}}$ and $t_{_{PHZ}}$ are the same as $t_{_{dis}}$.
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHI} are the same as t_{od} .

Figure 1. Load Circuit and Voltage Waveforms



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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
74AUC2GU04DBVRE4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74AUC2GU04DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74AUC2GU04DCKRE4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74AUC2GU04DCKRG4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AUC2GU04DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AUC2GU04DCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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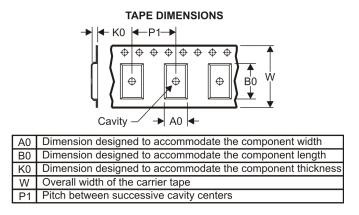
PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUC2GU04DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUC2GU04DCKR	SC70	DCK	6	3000	180.0	8.4	2.25	2.4	1.22	4.0	8.0	Q3

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PACKAGE MATERIALS INFORMATION

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUC2GU04DBVR	SOT-23	DBV	6	3000	202.0	201.0	28.0
SN74AUC2GU04DCKR	SC70	DCK	6	3000	202.0	201.0	28.0

DBV (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- È. Falls within JEDEC MO-178 Variation AB, except minimum lead width.



LAND PATTERN DATA



NOTES:

- A. All linear dimensions are in millimeters.B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



DCK (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES: A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-203 variation AB.



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