

SM320C6713-EP SM320C6713B-EP FLOATING-POINT DIGITAL SIGNAL PROCESSORS

Data Manual



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Contents

| | | |
|-----------|--|-----------|
| 1 | FEATURES | 9 |
| 2 | SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS | 10 |
| 3 | DEVICE INFORMATION | 11 |
| | 3.1 Description | 14 |
| | 3.2 Device Characteristics | 16 |
| | 3.3 Functional Block and CPU (DSP Core) Diagram | 17 |
| 4 | OVERVIEW | 18 |
| | 4.1 CPU (DSP Core) Description | 18 |
| | 4.2 Memory Map Summary | 19 |
| | 4.3 L2 Memory Structure Expanded | 21 |
| | 4.4 Peripheral Register Descriptions | 22 |
| | 4.5 Signal Groups Description | 30 |
| 5 | DEVICE CONFIGURATIONS | 35 |
| | 5.1 Device Configurations at Device Reset | 35 |
| | 5.2 Peripheral Pin Selection at Device Reset | 36 |
| | 5.3 Peripheral Selection/Device Configurations Via the DEVCFG Control Register | 36 |
| | 5.4 Multiplexed Pins | 37 |
| | 5.5 Configuration Examples | 41 |
| | 5.6 Debugging Considerations | 47 |
| 6 | TERMINAL FUNCTIONS | 47 |
| | 6.1 Development Support | 55 |
| | 6.2 Device and Development-Support Tool Nomenclature | 56 |
| | 6.2.1 Device Development Evolutionary Flow | 56 |
| | 6.2.2 Support Tool Development Evolutionary Flow | 56 |
| | 6.3 Ordering Nomenclature | 57 |
| | 6.4 Documentation Support | 57 |
| 7 | REGISTER INFORMATION | 59 |
| | 7.1 CPU Control Status Register (CSR) Description | 59 |
| | 7.2 Cache Configuration (CCFG) Register Description (13B) | 60 |
| | 7.3 Interrupts and Interrupt Selector | 61 |
| | 7.4 External Interrupt Sources | 63 |
| | 7.5 EDMA Module and EDMA Selector | 64 |
| 8 | PLL and PLL Controller | 68 |
| | 8.1 PLL Registers | 69 |
| 9 | MULTICHANNEL AUDIO SERIAL PORT (McASP) PERIPHERALS | 75 |
| | 9.1 McASP Block Diagram | 75 |
| | 9.2 Multichannel Time Division Multiplexed (TDM) Synchronous Transfer Mode | 77 |
| | 9.3 Burst Transfer Mode | 77 |
| | 9.4 Supported Bit Stream Formats for TDM and Burst Transfer Modes | 78 |
| | 9.5 Digital Audio Interface Transmitter (DIT) Transfer Mode (Transmitter Only) | 78 |
| | 9.6 McASP Flexible Clock Generators | 79 |
| | 9.7 McASP Error Handling and Management | 79 |
| | 9.8 McASP Interrupts and EDMA Events | 80 |
| | 9.9 I ² C | 80 |
| 10 | LOGIC AND POWER SUPPLY | 82 |

| | | |
|-----------|---|----------------------------|
| 10.1 | General-Purpose Input/Output (GPIO) | 82 |
| 10.2 | Power-Down Mode Logic | 83 |
| 10.2.1 | Triggering, Wake-Up, and Effects | 83 |
| 10.3 | Power-Supply Sequencing | 84 |
| 10.3.1 | System-Level Design Considerations | 85 |
| 10.3.2 | Power-Supply Design Considerations | 85 |
| 10.4 | Power-Supply Decoupling | 85 |
| 10.5 | IEEE Std 1149.1 JTAG Compatibility Statement | 85 |
| 10.6 | EMIF Device Speed | 86 |
| 10.7 | EMIF Big Endian Mode Correctness (C6713B Only) | 87 |
| 10.8 | Bootmode | 88 |
| 11 | PARAMETRIC INFORMATION | 89 |
| 11.1 | Absolute Maximum Ratings | 89 |
| 11.2 | Recommended Operating Conditions | 89 |
| 11.3 | Electrical Characteristics | 90 |
| 11.4 | Parameter Measurement Information | 91 |
| 11.4.1 | Timing Information | 91 |
| 11.4.2 | Signal Transition Levels | 91 |
| 11.4.3 | AC Transient Rise/Fall Time Specifications | 92 |
| 11.4.4 | Timing Parameters and Board Routing Analysis | 93 |
| 11.5 | Input and Output Clocks | 94 |
| 11.6 | Asynchronous Memory Timing | 97 |
| 11.7 | Synchronous-Burst Memory Timing | 100 |
| 11.8 | Synchronous DRAM Timing | 101 |
| 11.9 | HOLD/HOLDA Timing | 106 |
| 11.10 | BUSREQ Timing | 106 |
| 11.11 | Reset Timing | 107 |
| 11.12 | External Interrupt Timing | 109 |
| 11.13 | Multichannel Audio Serial Port (McASP) Timing | 110 |
| 11.14 | Inter-Integrated Circuits (I ² C) Timing | 113 |
| 11.15 | Host-Port Interface Timing | 115 |
| 11.16 | Multichannel Buffered Serial Port (McBSP) Timing | 119 |
| 11.17 | Timer Timing | 126 |
| 11.18 | General-Purpose Input/Output (GPIO) Port Timing | 127 |
| 11.19 | JTAG Test Port Timing | 128 |
| 12 | MECHANICAL DATA | 129 |
| 12.1 | Mechanical Information | 129 |
| 12.2 | Packaging Information | 129 |

List of Figures

| | | |
|-------|---|---------------------|
| 4-1 | 320C67x™ CPU (DSP Core) Data Paths | 19 |
| 4-2 | L2 Memory Configuration | 21 |
| 4-3 | EDMA Channel Parameter Entries (Six Words) for Each EDMA Event | 25 |
| 4-4 | CPU (DSP Core) and Peripheral Signals | 31 |
| 4-5 | Peripheral Signals | 32 |
| 4-6 | Peripheral Signals | 33 |
| 4-7 | Peripheral Signals | 34 |
| 4-8 | Peripheral Signals | 34 |
| 5-1 | Configuration Example A (Two I2C + Two McASP + GPIO) | 42 |
| 5-2 | Configuration Example B (One I2C + One McBSP + Two McASP + GPIO) | 43 |
| 5-3 | Configuration Example C [2 I2C + 1 McBSP + 1 McASP + 1 McASP (DIT) + GPIO] | 44 |
| 5-4 | Configuration Example D [1 I2C + 2 McBSP + 1 McASP + 1 McASP (DIT) + GPIO + Timers] | 45 |
| 5-5 | Configuration Example E (1 I2C + HPI + 1 McASP)..... | 46 |
| 5-6 | Configuration Example F (One McBSP + HPI + One McASP)..... | 47 |
| 6-1 | TMS320C6000™ DSP Device Nomenclature (Including SM320C6713 and C6713B Devices) | 57 |
| 7-1 | CPU Control Status Register (CPU CSR) | 59 |
| 7-2 | Cache Configuration (CCFG) Register | 61 |
| 8-1 | PLL and Clock Generator Logic..... | 68 |
| 9-1 | McASP0 and McASP1 Configuration..... | 76 |
| 9-2 | I2Cx Module Block Diagram | 81 |
| 10-1 | GPIO Enable (GPEN) Register (Hex Address: 01B0 0000) | 82 |
| 10-2 | GPIO Direction (GPDIR) Register (Hex Address: 01B0 0004) | 82 |
| 10-3 | Power-Down Mode Logic..... | 83 |
| 10-4 | PWRD Field of the CSR | 84 |
| 10-5 | Schottky Diode Diagram..... | 85 |
| 10-6 | 16/8-Bit EMIF Big Endian Mode Correctness Mapping (HD12 = 1) (C6713B Only) | 87 |
| 10-7 | 16/8-Bit EMIF Big Endian Mode Correctness Mapping (HD12 = 0) (C6713B Only) | 88 |
| 11-1 | Test Load Circuit for AC Timing Measurements | 91 |
| 11-2 | Input and Output Voltage Reference Levels for AC Timing Measurements..... | 91 |
| 11-3 | Rise and Fall Transition Time Voltage Reference Levels..... | 91 |
| 11-4 | AC Transient Specification Rise Time | 92 |
| 11-5 | AC Transient Specification Fall Time | 92 |
| 11-6 | Board-Level Input/Output Timings | 94 |
| 11-7 | CLKIN | 94 |
| 11-8 | CLKOUT2 | 94 |
| 11-9 | CLKOUT3 | 95 |
| 11-10 | ECLKIN | 95 |
| 11-11 | ECLKOUT | 96 |
| 11-12 | Asynchronous Memory Read | 99 |
| 11-13 | Asynchronous Memory Write | 99 |
| 11-14 | SBSRAM Read Timing..... | 101 |
| 11-15 | SBSRAM Write Timing..... | 101 |
| 11-16 | SDRAM Read Command (CAS Latency 3) | 103 |
| 11-17 | SDRAM Write Command | 103 |
| 11-18 | SDRAM ACTV Command | 104 |
| 11-19 | SDRAM DCAB Command | 104 |
| 11-20 | SDRAM DEAC Command | 105 |

| | | |
|-------|---|---------------------|
| 11-21 | SDRAM REFR Command | 105 |
| 11-22 | SDRAM MRS Command | 105 |
| 11-23 | HOLD/HOLDA Timing | 106 |
| 11-24 | BUSREQ | 107 |
| 11-25 | Reset Timing | 108 |
| 11-26 | External/NMI Interrupt | 109 |
| 11-27 | McASP Input Timings | 112 |
| 11-28 | McASP Output Timings | 112 |
| 11-29 | I ² C Receive | 113 |
| 11-30 | I ² C Transmit Timings | 114 |
| 11-31 | HPI Read Timing ($\overline{\text{HAS}}$ Not Used, Tied High) | 117 |
| 11-32 | HPI Read Timing ($\overline{\text{HAS}}$ Used) | 117 |
| 11-33 | HPI Write Timing ($\overline{\text{HAS}}$ Not Used, Tied High) | 118 |
| 11-34 | HPI Write Timing ($\overline{\text{HAS}}$ Used)..... | 118 |
| 11-35 | McBSP Timings | 121 |
| 11-36 | FSR Timing When GSYNC = 1 | 121 |
| 11-37 | McBSP Timing as SPI Master or Slave: CLKSTP = 10b, CLKXP = 0 | 122 |
| 11-38 | McBSP as SPI Master or Slave: CLKSTP = 11b, CLKXP = 0 | 123 |
| 11-39 | McBSP as SPI Master or Slave: CLKSTP = 10b, CLKXP = 1 | 124 |
| 11-40 | McBSP as SPI Master or Slave: CLKSTP = 11b, CLKXP = 1 | 125 |
| 11-41 | Timer | 126 |
| 11-42 | GPIO Port Timing | 127 |
| 11-43 | JTAG Test-Port Timing..... | 128 |

List of Tables

| | | |
|------|--|--------------------|
| 3-1 | Terminal Assignments for 272-Ball GDP Package (in Order of Ball No.) | 12 |
| 3-2 | Characteristics of the C6713 and C6713B Processor | 16 |
| 4-1 | 320C6713/13B Memory Map Summary | 20 |
| 4-2 | EMIF Registers | 22 |
| 4-3 | L2 Cache Registers | 23 |
| 4-4 | Interrupt Selector Registers | 23 |
| 4-5 | Device Registers | 24 |
| 4-6 | EDMA Parameter RAM | 24 |
| 4-7 | EDMA Registers | 25 |
| 4-8 | Quick DMA (QDMA) and Pseudo Registers | 25 |
| 4-9 | PLL Controller Registers | 25 |
| 4-10 | McASP0 and McASP1 Registers | 26 |
| 4-11 | I2C0 and I2C1 Registers | 28 |
| 4-12 | HPI Registers | 28 |
| 4-13 | Timer 0 and Timer 1 Registers | 28 |
| 4-14 | McBSP0 and McBSP1 Registers | 28 |
| 4-15 | GPIO Registers | 29 |
| 5-1 | Device Configurations Pins at Device Reset (HD[4:3], HD8, HD12 [13B only], and CLKMODE0) | 35 |
| 5-2 | HPI_EN (HD14 Pin) Peripheral Selection (HPI or McASP1, and Select GPIO Pins) | 36 |
| 5-3 | Device Configuration Register (DEVCFG) [Address Location: 0x019C0200–0x019C02FF] | 36 |
| 5-4 | Device Configuration Register (DEVCFG) Selection Bit Descriptions | 37 |
| 5-5 | Peripheral Pin Selection Matrix | 38 |
| 5-6 | C6713/13B Device Multiplexed/Shared Pins | 38 |
| 6-1 | 320C6713 and C6713B Device Part Numbers (P/Ns) and Ordering Information | 57 |
| 7-1 | CPU CSR Bit Field Description | 60 |
| 7-2 | CCFG Register Bit Field Description | 61 |
| 7-3 | DSP Interrupts | 61 |
| 7-4 | Interrupt Selector | 63 |
| 7-5 | External Interrupt Sources and Peripheral Module Control | 64 |
| 7-6 | EDMA Channels | 65 |
| 7-7 | EDMA Selector | 66 |
| 7-8 | EDMA Event Selector Registers (ESEL0 Register (0x01A0 FF00) | 67 |
| 7-9 | EDMA Event Selector Registers—ESEL1 Register (0x01A0 FF04) | 67 |
| 7-10 | EDMA Event Selector Registers—ESEL3 Register (0x01A0 FF0C) | 67 |
| 7-11 | EDMA Event Selection Registers (ESEL0, ESEL1, and ESEL3) Description | 67 |
| 8-1 | PLL Lock and Reset Times | 69 |
| 8-2 | CLKOUT Signals, Default Settings, and Control | 69 |
| 8-3 | PLL Clock Frequency Ranges | 70 |
| 8-4 | PLL Control/Status Register (PLLCSR) (0x01B7 C100) | 70 |
| 8-5 | PLL Control/Status Register (PLLCSR) Description | 71 |
| 8-6 | PLL Multiplier (PLL M) Control Register (0x01B7 C110) | 71 |
| 8-7 | PLL Multiplier (PLL M) Control Register Description | 72 |
| 8-8 | PLL Wrapper Divider x Registers (PLLDIV0, PLLDIV1, PLLDIV2, and PLLDIV3) (0x01B7 C114, 0x01B7 C118, 0x01B7 C11C, and 0x01B7 C120, respectively) | 72 |
| 8-9 | PLL Wrapper Divider x Registers (Prescaler Divider D0 and Post-Scaler Dividers D1, D2, and D3) Description | 72 |
| 8-10 | Oscillator Divider 1 (OSCDIV1) Register (0x01B7 C124) | 73 |

| | | |
|-------|--|---------------------|
| 8-11 | Oscillator Divider 1 (OSCDIV1) Register Description | 74 |
| 10-1 | Characteristics of the Power-Down Modes | 84 |
| 10-2 | C6713/13B Example Boards and Maximum EMIF Speed | 87 |
| 11-1 | Board-Level Timings Example (see) | 93 |
| 11-2 | Timing Requirements for CLKIN | 94 |
| 11-3 | Switching Characteristics for CLKOUT2 | 94 |
| 11-4 | Switching Characteristics for CLKOUT3 | 95 |
| 11-5 | Timing Requirements for ECLKIN | 95 |
| 11-6 | Switching Characteristics for ECLKOUT | 96 |
| 11-7 | Timing Requirements for Asynchronous Memory Cycles | 97 |
| 11-8 | Switching Characteristics for Asynchronous Memory Cycles | 97 |
| 11-9 | Timing Requirements for Synchronous-Burst SRAM Cycles | 100 |
| 11-10 | Switching Characteristics for Synchronous-Burst SRAM Cycles | 100 |
| 11-11 | Timing Requirements for Synchronous DRAM Cycles | 101 |
| 11-12 | Switching Characteristics for Synchronous DRAM Cycles | 101 |
| 11-13 | Timing Requirements for $\overline{\text{HOLD}}/\overline{\text{HOLDA}}$ Cycles | 106 |
| 11-14 | Switching Characteristics for $\overline{\text{HOLD}}/\overline{\text{HOLDA}}$ Cycles | 106 |
| 11-15 | Switching Characteristics for BUSREQ Cycles | 106 |
| 11-16 | Timing Requirements for $\overline{\text{RESET}}$ | 107 |
| 11-17 | Switching Characteristics For $\overline{\text{RESET}}$ | 107 |
| 11-18 | Timing Requirements for External Interrupts | 109 |
| 11-19 | Timing Requirements for McASP | 110 |
| 11-20 | Switching Characteristics for McASP | 110 |
| 11-21 | Timing Requirements for I ² C | 113 |
| 11-22 | Switching Characteristics for I ² C | 114 |
| 11-23 | Timing Requirements for Host-Port Interface Cycles | 115 |
| 11-24 | Switching Characteristics for Host-Port Interface Cycles | 116 |
| 11-25 | Timing Requirements for McBSP | 119 |
| 11-26 | Switching Characteristics for McBSP | 120 |
| 11-27 | Timing Requirements for FSR When GSYNC = 1 | 121 |
| 11-28 | Timing Requirements for McBSP as SPI Master or Slave: CLKSTP = 10b, CLKXP = 0 | 121 |
| 11-29 | Switching Characteristics for McBSP as SPI Master or Slave: CLKSTP = 10b, CLKXP = 0 | 122 |
| 11-30 | Timing Requirements for McBSP as SPI Master or Slave: CLKSTP = 11b, CLKXP = 0 | 122 |
| 11-31 | Switching Characteristics for McBSP as SPI Master or Slave: CLKSTP = 11b, CLKXP = 0 | 123 |
| 11-32 | Timing Requirements for McBSP as SPI Master or Slave: CLKSTP = 10b, CLKXP = 1 | 124 |
| 11-33 | Switching Characteristics for McBSP as SPI Master or Slave: CLKSTP = 10b, CLKXP = 1 | 124 |
| 11-34 | Timing Requirements for McBSP as SPI Master or Slave: CLKSTP = 11b, CLKXP = 1 | 125 |
| 11-35 | Switching Characteristics for McBSP as SPI Master or Slave: CLKSTP = 11b, CLKXP = 1 | 125 |
| 11-36 | Timing Requirements for Timer Inputs | 126 |
| 11-37 | Switching Characteristics for Timer Inputs | 126 |
| 11-38 | Timing Requirements for GPIO Inputs | 127 |
| 11-39 | Switching Characteristics for GPIO Inputs | 127 |
| 11-40 | Timing Requirements for JTAG Test Port | 128 |

| | | |
|-------|---|---------------------|
| 11-41 | Switching Characteristics for JTAG Test Port | 128 |
| 12-1 | Thermal Resistance Characteristics (S-PBGA Package) for GDP | 129 |

FLOATING-POINT DIGITAL SIGNAL PROCESSORS

 Check for Samples: [SM320C6713-EP](#)

1 FEATURES

- **Highest Performance Floating Point Digital Signal Processors (DSPs): C6713/C6713B**
 - Eight 32 Bit Instructions/Cycle
 - 32/64 Bit Data Word
 - 200 and 300 MHz Clock Rate
 - 5 Instruction Cycle Times
 - 2400/1800 and 1600/1200 MIPS/MFLOPS
 - Rich Peripheral Set, Optimized for Audio
 - Highly Optimized C/C++ Compiler
 - **Advanced Very Long Instruction Word (VLIW) 320C67x™ DSP Core**
 - Eight Independent Functional Units:
 - Two ALUs (Fixed Point)
 - Four ALUs (Floating Point and Fixed Point)
 - Two Multipliers (Floating Point and Fixed Point)
 - Load Store Architecture With 32 32-Bit General Purpose Registers
 - Instruction Packing Reduces Code Size
 - All Instructions Conditional
 - **Instruction Set Features**
 - Native Instructions for IEEE 754
 - Byte Addressable (8/16/32 Bit Data)
 - 8 Bit Overflow Protection
 - Saturation; Bit-Field Extract, Set, Clear; Bit-Counting; Normalization
 - **L1/L2 Memory Architecture**
 - 4K Byte L1P Program Cache (Direct-Mapped)
 - 4K Byte L1D Data Cache (2-Way)
 - 256K Byte L2 Memory Total: 64K-Byte L2 Unified Cache/Mapped RAM, and 192K Byte Additional L2 Mapped RAM
 - **Device Configuration**
 - Boot Mode: HPI, 8/16/32 Bit ROM Boot
 - Endianness: Little Endian, Big Endian
 - **32 Bit External Memory Interface (EMIF)**
 - Glueless Interface to SRAM, EPROM, Flash, SBSRAM, and SDRAM
 - 512M Byte Total Addressable External Memory Space
 - **Enhanced Direct Memory Access (EDMA) Controller (16 Independent Channels)**
 - **16 Bit Host Port Interface (HPI)**
 - **Two Multichannel Audio Serial Ports (McASPs)**
 - Two Independent Clock Zones Each (One TX and One RX)
 - Eight Serial Data Pins Per Port: Individually Assignable to any of the Clock Zones
 - Wide Variety of I²S™ and Similar Bit Stream Formats
 - Integrated Digital Audio Interface Transmitter (DIT)
 - Extensive Error Checking and Recovery
 - **Two Inter-Integrated Circuit Bus (I²C™ Bus) Multi-Master and Slave Interfaces**
 - **Two Multichannel Buffered Serial Ports:**
 - Serial Peripheral Interface (SPI)
 - High Speed TDM Interface
 - AC97 Interface
 - **Two 32 Bit General Purpose Timers**
 - **Dedicated GPIO Module With 16 Pins (External Interrupt Capable)**
 - **Flexible Phase Locked Loop (PLL) Based Clock Generator Module**
 - **IEEE-1149.1 (JTAG)⁽¹⁾ Boundary-Scan Compatible**
 - **272 Ball, Ball Grid Array Package (GDP)**
 - **0.13 μm/6 Level Copper Metal Process**
 - CMOS Technology
 - **3.3 V I/Os, 1.26 V Internal**
- (1) IEEE Standard 1149.1-1990 Standard-Test-Access Port and Boundary Scan Architecture.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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2 SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Available in Military (–55°C/125°C) Temperature Range⁽²⁾**
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**

(2) Custom temperature ranges available

3 DEVICE INFORMATION

GDP 272-BALL BGA PACKAGE (BOTTOM VIEW)

| | | | | | | | | | | | | | | | | | | | | |
|---|---------------------------------|---------------------------------|-------------------|-------------------------|-------------------------|--------------------------|------------------|------------------|------------------|--|---|---|---------------------------|------------------|------------------|------------------|--------------------------|---------------------------|-------------------------|-------------------------|
| Y | V _{SS} | V _{SS} | ED18 | $\overline{\text{BE}}2$ | ARDY | EA2 | DV _{DD} | EA7 | EA9 | ECLKOUT | ECLKIN | CLKOUT2 GP[2] | V _{SS} | EA14 | EA16 | EA18 | DV _{DD} | EA20 | V _{SS} | V _{SS} |
| W | V _{SS} | CV _{DD} | DV _{DD} | ED17 | V _{SS} | $\overline{\text{CE}}2$ | EA4 | EA6 | DV _{DD} | $\overline{\text{AOE}}/$ $\overline{\text{SDRAS}}/$ SSOE | V _{SS} | DV _{DD} | EA11 | EA13 | EA15 | V _{SS} | EA19 | $\overline{\text{CE}}1$ | CV _{DD} | V _{SS} |
| V | ED20 | ED19 | CV _{DD} | ED16 | $\overline{\text{BE}}3$ | $\overline{\text{CE}}3$ | EA3 | EA5 | EA8 | EA10 | $\overline{\text{ARE}}/$ SDCAS/ SSADS | $\overline{\text{AWE}}/$ SDWE/ SSWE | DV _{DD} | EA12 | DV _{DD} | EA17 | $\overline{\text{CE}}0$ | CV _{DD} | DV _{DD} | $\overline{\text{BE}}0$ |
| U | ED22 | ED21 | ED23 | V _{SS} | DV _{DD} | CV _{DD} | DV _{DD} | V _{SS} | V _{SS} | CV _{DD} | CV _{DD} | DV _{DD} | V _{SS} | CV _{DD} | CV _{DD} | DV _{DD} | V _{SS} | EA21 | $\overline{\text{BE}}1$ | V _{SS} |
| T | ED24 | ED25 | DV _{DD} | V _{SS} | | | | | | | | | | | | | V _{SS} | ED13 | ED15 | ED14 |
| R | DV _{DD} | ED27 | ED26 | CV _{DD} | | | | | | | | | | | | | CV _{DD} | DV _{DD} | ED11 | ED12 |
| P | ED28 | ED29 | ED30 | V _{SS} | | | | | | | | | | | | | V _{SS} | ED9 | V _{SS} | ED10 |
| N | SCL0 | SDA0 | ED31 | V _{SS} | | | | | | | | | | | | | V _{SS} | ED6 | ED7 | ED8 |
| M | CLKR1/ AXR0[6] | DR1/ SDA1 | FSR1/ AXR0[7] | V _{SS} | | | | | | | | | | | | | V _{SS} | DV _{DD} | ED4 | ED5 |
| L | FSX1 | DX1 AXR0[5] | CLKX1/ AMUTE0 | CV _{DD} | | | | | | | | | | | | | CV _{DD} | ED2 | ED3 | CV _{DD} |
| K | CV _{DD} | V _{SS} | CLKS0 AHCLKR0 | CV _{DD} | | | | | | | | | | | | | CV _{DD} | ED0 | ED1 | V _{SS} |
| J | DR0/ AXR0[0] | DV _{DD} | FSR0/ AFSR0 | V _{SS} | | | | | | | | | | | | | $\overline{\text{HOLD}}$ | $\overline{\text{HOLDA}}$ | BUS REQ | HINT/ GP[1] |
| H | FSX0/ AFSX0 | DX0/ AXR0[1] | CLKR0/ ACLKR0 | V _{SS} | | | | | | | | | | | | | V _{SS} | DV _{DD} | HRDY/ ACLKR[1] | HHWL/ AFSR[1] |
| G | TOUT0/ AXR0[2] | TINP0/ AXR0[3] | CLKX0/ ACLKX0 | V _{SS} | | | | | | | | | | | | | V _{SS} | HCNTL0/ AXR1[3] | HCNTL1/ AXR1[1] | HRW/ AXR1[0] |
| F | TOUT1/ AXR0[4] | TINP1/ AHCLKX0 | DV _{DD} | CV _{DD} | | | | | | | | | | | | | CV _{DD} | FDS2/ AXR1[5] | V _{SS} | FCS/ AXR1[1] |
| E | CLKS1/ SCL1 | V _{SS} | GP[7] EXT_INT7 | V _{SS} | | | | | | | | | | | | | V _{SS} | FAS/ ACLKX1 | FDS/ AXR1[6] | HD0/ AXR1[4] |
| D | DV _{DD} | GP[6] EXT_INT6 | EMU2 | V _{SS} | CV _{DD} | CV _{DD} | RSV | V _{SS} | EMU0 | CLKOUT3 | CV _{DD} | RSV | V _{SS} | CV _{DD} | CV _{DD} | DV _{DD} | V _{SS} | HD2/ AFSX1 | DV _{DD} | HD1/ AXR1[7] |
| C | GP[5] (EXT_INT5) AMUTEIN0 | GP[4] (EXT_INT4) AMUTEIN1 | CV _{DD} | CLK MODE0 | PLLHV | V _{SS} | CV _{DD} | V _{SS} | V _{SS} | DV _{DD} | EMU4 | RSV | NMI | HD14/ GP[14] | HD12/ GP[12] | HD9/ GP[9] | HD6/ AHCLKR1 | CV _{DD} | HD4/ GP[0] | HD3/ AMUTE1 |
| B | V _{SS} | CV _{DD} | DV _{DD} | V _{SS} | RSV | $\overline{\text{TRST}}$ | TMS | DV _{DD} | EMU1 | EMU3 | RSV | EMU5 | DV _{DD} | HD15/ GP[15] | V _{SS} | HD10/ GP[10] | HD8/ GP[8] | HD5/ AHCLKX1 | CV _{DD} | V _{SS} |
| A | V _{SS} | V _{SS} | CLKIN | CV _{DD} | RSV | TCK | TDI | TD0 | CV _{DD} | CV _{DD} | V _{SS} | RSV | $\overline{\text{RESET}}$ | V _{SS} | HD13/ GP[13] | HD11/ GP[11] | DV _{DD} | HD7/ GP[3] | V _{SS} | V _{SS} |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 |

Shading denotes the GDP package pin functions that drop out on the PYP package.

Table 3-1. Terminal Assignments for 272-Ball GDP Package (in Order of Ball No.)

| BALL NO. | SIGNAL NAME | BALL NO. | SIGNAL NAME |
|----------|---|----------|---------------------------------|
| A1 | V _{SS} | C1 | GP[5](EXT_INT5)/AMUTEIN0 |
| A2 | V _{SS} | C2 | GP[4](EXT_INT4)/AMUTEIN1 |
| A3 | CLKIN | C3 | CV _{DD} |
| A4 | CV _{DD} | C4 | CLKMODE0 |
| A5 | RSV | C5 | PLLHV |
| A6 | TCK | C6 | V _{SS} |
| A7 | TDI | C7 | CV _{DD} |
| A8 | TDO | C8 | V _{SS} |
| A9 | CV _{DD} | C9 | V _{SS} |
| A10 | CV _{DD} | C10 | DV _{DD} |
| A11 | V _{SS} | C11 | EMU4 |
| A12 | RSV (connected directly to CV _{DD}) | C12 | RSV |
| A13 | $\overline{\text{RESET}}$ | C13 | NMI |
| A14 | V _{SS} | C14 | HD14/GP[14] |
| A15 | HD13/GP[13] | C15 | HD12/GP[12] |
| A16 | HD11/GP[11] | C16 | HD9/GP[9] |
| A17 | DV _{DD} | C17 | HD6/AHCLKR1 |
| A18 | HD7/GP[3] | C18 | CV _{DD} |
| A19 | V _{SS} | C19 | HD4/GP[0] |
| A20 | V _{SS} | C20 | HD3/AMUTE1 |
| B1 | V _{SS} | D1 | DV _{DD} |
| B2 | CV _{DD} | D2 | GP[6](EXT_INT6) |
| B3 | DV _{DD} | D3 | EMU2 |
| B4 | V _{SS} | D4 | V _{SS} |
| B5 | RSV | D5 | CV _{DD} |
| B6 | $\overline{\text{TRST}}$ | D6 | CV _{DD} |
| B7 | TMS | D7 | RSV |
| B8 | DV _{DD} | D8 | V _{SS} |
| B9 | EMU1 | D9 | EMU0 |
| B10 | EMU3 | D10 | CLKOUT3 |
| B11 | RSV (connected directly to V _{SS}) | D11 | CV _{DD} |
| B12 | EMU5 | D12 | RSV |
| B13 | DV _{DD} | D13 | V _{SS} |
| B14 | HD15/GP[15] | D14 | CV _{DD} |
| B15 | V _{SS} | D15 | CV _{DD} |
| B16 | HD10/GP[10] | D16 | DV _{DD} |
| B17 | HD8/GP[8] | D17 | V _{SS} |
| B18 | HD5/AHCLKX1 | D18 | HD2/AFSX1 |
| B19 | CV _{DD} | D19 | DV _{DD} |
| B20 | V _{SS} | D20 | HD1/AXR1[7] |
| E1 | CLKS1/SCL1 | J17 | $\overline{\text{HOLD}}$ |
| E2 | V _{SS} | J18 | $\overline{\text{HOLDA}}$ |
| E3 | GP[7](EXP_INT7) | J19 | BUSREQ |
| E4 | V _{SS} | J20 | $\overline{\text{HINT}}$ /GP[1] |
| E17 | V _{SS} | K1 | CV _{DD} |
| E18 | $\overline{\text{HAS}}$ /ACLKX1 | K2 | V _{SS} |
| E19 | $\overline{\text{HDS1}}$ /AXR1[6] | K3 | CLKS0/AHCLKR0 |
| E20 | HD0/AXR1[4] | K4 | CV _{DD} |
| F1 | TOUT1/AXR0[4] | K9 | V _{SS} |
| F2 | TINP1/AHCLKX0 | K10 | V _{SS} |
| F3 | DV _{DD} | K11 | V _{SS} |

Table 3-1. Terminal Assignments for 272-Ball GDP Package (in Order of Ball No.) (continued)

| BALL NO. | SIGNAL NAME | BALL NO. | SIGNAL NAME |
|----------|----------------------------|----------|-------------------|
| F4 | CV _{DD} | K12 | V _{SS} |
| F17 | CV _{DD} | K17 | CV _{DD} |
| F18 | HDS2/AXR1[5] | K18 | ED0 |
| F19 | V _{SS} | K19 | ED1 |
| F20 | HCS/AXR1[2] | K20 | V _{SS} |
| G1 | TOUT0/AXR0[2] | L1 | FSX1 |
| G2 | TINP0/AXR0[3] | L2 | DX1/AXR0[5] |
| G3 | CLKX0/ACLKX0 | L3 | CLKX1/AMUTE0 |
| G4 | V _{SS} | L4 | CV _{DD} |
| G17 | V _{SS} | L9 | V _{SS} |
| G18 | HCNTL0/AXR1[3] | L10 | V _{SS} |
| G19 | HCNTL1/AXR1[1] | L11 | V _{SS} |
| G20 | HR \overline{W} /AXR1[0] | L12 | V _{SS} |
| H1 | FSX0/AFSX0 | L17 | CV _{DD} |
| H2 | DX0/AXR0[1] | L18 | ED2 |
| H3 | CLKR0/ACLKR0 | L19 | ED3 |
| H4 | V _{SS} | L20 | CV _{DD} |
| H17 | V _{SS} | M1 | CLKR1/AXR0[6] |
| H18 | DV _{DD} | M2 | DR1/SDA1 |
| H19 | HRDY/ACLKR1 | M3 | FSR1/AXR0[7] |
| H20 | HHWIL/AFSR1 | M4 | V _{SS} |
| J1 | DR0/AXR0[0] | M9 | V _{SS} |
| J2 | DV _{DD} | M10 | V _{SS} |
| J3 | FSR0/AFSR0 | M11 | V _{SS} |
| J4 | V _{SS} | M12 | V _{SS} |
| J9 | V _{SS} | M17 | V _{SS} |
| J10 | V _{SS} | M18 | DV _{DD} |
| J11 | V _{SS} | M19 | ED4 |
| J12 | V _{SS} | M20 | ED5 |
| N1 | SCL0 | U9 | V _{SS} |
| N2 | SDA0 | U10 | CV _{DD} |
| N3 | ED31 | U11 | CV _{DD} |
| N4 | V _{SS} | U12 | DV _{DD} |
| N17 | V _{SS} | U13 | V _{SS} |
| N18 | ED6 | U14 | CV _{DD} |
| N19 | ED7 | U15 | CV _{DD} |
| N20 | ED8 | U16 | DV _{DD} |
| P1 | ED28 | U17 | V _{SS} |
| P2 | ED29 | U18 | EA21 |
| P3 | ED30 | U19 | \overline{BE} 1 |
| P4 | V _{SS} | U20 | V _{SS} |
| P17 | V _{SS} | V1 | ED20 |
| P18 | ED9 | V2 | ED19 |
| P19 | V _{SS} | V3 | CV _{DD} |
| P20 | ED10 | V4 | ED16 |
| R1 | DV _{DD} | V5 | \overline{BE} 3 |
| R2 | ED27 | V6 | \overline{CE} 3 |
| R3 | ED26 | V7 | EA3 |
| R4 | CV _{DD} | V8 | EA5 |
| R17 | CV _{DD} | V9 | EA8 |
| R18 | DV _{DD} | V10 | EA10 |

Table 3-1. Terminal Assignments for 272-Ball GDP Package (in Order of Ball No.) (continued)

| BALL NO. | SIGNAL NAME | BALL NO. | SIGNAL NAME |
|----------|------------------|----------|------------------|
| R19 | ED11 | V11 | ARE/SDCAS/SSADS |
| R20 | ED12 | V12 | AWE/SDWE/SSWE |
| T1 | ED24 | V13 | DV _{DD} |
| T2 | ED25 | V14 | EA17 |
| T3 | DV _{DD} | V15 | DV _{DD} |
| T4 | V _{SS} | V16 | EA |
| T17 | V _{SS} | V17 | CE0 |
| T18 | ED13 | V18 | CV _{DD} |
| T19 | ED15 | V19 | DV _{DD} |
| T20 | ED14 | V20 | BE0 |
| U1 | ED22 | W1 | V _{SS} |
| U2 | ED21 | W2 | CV _{DD} |
| U3 | ED23 | W3 | DV _{DD} |
| U4 | V _{SS} | W4 | ED17 |
| U5 | DV _{DD} | W5 | V _{SS} |
| U6 | CV _{DD} | W6 | CE2 |
| U7 | DV _{DD} | W7 | EA4 |
| U8 | V _{SS} | W8 | EA6 |
| W9 | DV _{DD} | Y5 | ARDY |
| W10 | AOE/SDRAS/SSOE | Y6 | EA2 |
| W11 | V _{SS} | Y7 | DV _{DD} |
| W12 | DV _{DD} | Y8 | EA7 |
| W13 | EA11 | Y9 | EA9 |
| W14 | EA13 | Y10 | ECLKOUT |
| W15 | EA15 | Y11 | ECLKIN |
| W16 | V _{SS} | Y12 | CLKOUT2/GP[2] |
| W17 | EA19 | Y13 | V _{SS} |
| W18 | CE1 | Y14 | EA14 |
| W19 | CV _{DD} | Y15 | EA16 |
| W20 | V _{SS} | Y16 | EA18 |
| Y1 | V _{SS} | Y17 | DV _{DD} |
| Y2 | V _{SS} | Y18 | EA20 |
| Y3 | ED18 | Y19 | V _{SS} |
| Y4 | BE2 | Y20 | V _{SS} |

3.1 Description

The TMS320C67x™ DSPs (including the SM320C6713 and SM320C6713B devices) compose the floating-point DSP generation in the TMS320C6000™ DSP platform. The C6713 and C6713B devices are based on the high-performance, advanced very-long-instruction-word (VLIW) architecture developed by Texas Instruments (TI), making this DSP an excellent choice for multichannel and multifunction applications. Throughout the remainder of this document, the SM320C6713 and SM320C6713B are referred to as 320C67x or C67x or 13/13B where generic, and where specific, their individual full device part numbers are used or abbreviated as C6713, C6713B, 13, or 13B, and so forth.

Operating at 225 MHz, the C6713/13B delivers up to 1350 million floating-point operations per second (MFLOPS), 1800 million instructions per second (MIPS), and with dual fixed-/floating-point multipliers up to 450 million multiply-accumulate operations per second (MMACS).

Operating at 300 MHz, the C6713B delivers up to 1800 million floating-point operations per second (MFLOPS), 2400 million instructions per second (MIPS), and with dual fixed-/floating-point multipliers up to 600 million multiply-accumulate operations per second (MMACS).

The C6713/13B has a rich peripheral set that includes two multichannel audio serial ports (McASPs), two multichannel buffered serial ports (McBSPs), two inter-integrated circuit (I²C) buses, one dedicated general-purpose input/output (GPIO) module, two general-purpose timers, a host-port interface (HPI), and a glueless external memory interface (EMIF) capable of interfacing to SDRAM, SBSRAM, and asynchronous peripherals.

The two McASP interface modules each support one transmit and one receive clock zone. Each of the McASPs has eight serial data pins that can be individually allocated to any of the two zones. The serial port supports time-division multiplexing on each pin from 2 to 32 time slots. The C6713/13B has sufficient bandwidth to support all 16 serial data pins transmitting a 192-kHz stereo signal. Serial data in each zone may be transmitted and received on multiple serial data pins simultaneously and formatted in a multitude of variations on the Philips Inter-IC Sound (I²S) format.

In addition, the McASP transmitter may be programmed to output multiple S/PDIF, IEC60958, AES-3, and CP-430 encoded data channels simultaneously, with a single RAM containing the full implementation of user data and channel status fields.

The McASP also provides extensive error-checking and recovery features, such as the bad clock detection circuit for each high-frequency master clock, which verifies that the master clock is within a programmed frequency range.

The two I²C ports on the 320C6713/13B allow the DSP to easily control peripheral devices and communicate with a host processor. In addition, the standard multichannel buffered serial port (McBSP) may be used to communicate with serial peripheral interface (SPI™) mode peripheral devices.

The 320C6713/13B device has two boot modes—from the HPI or from external asynchronous ROM. For more detailed information, see the Bootmode section of this data sheet.

The TMS320C67x DSP generation is supported by the TI eXpressDSP™ set of industry benchmark development tools, including a highly optimizing C/C++ Compiler, the Code Composer Studio™ Integrated Development Environment (IDE), JTAG-based emulation and real-time debugging, and the DSP/BIOS™ kernel.

3.2 Device Characteristics

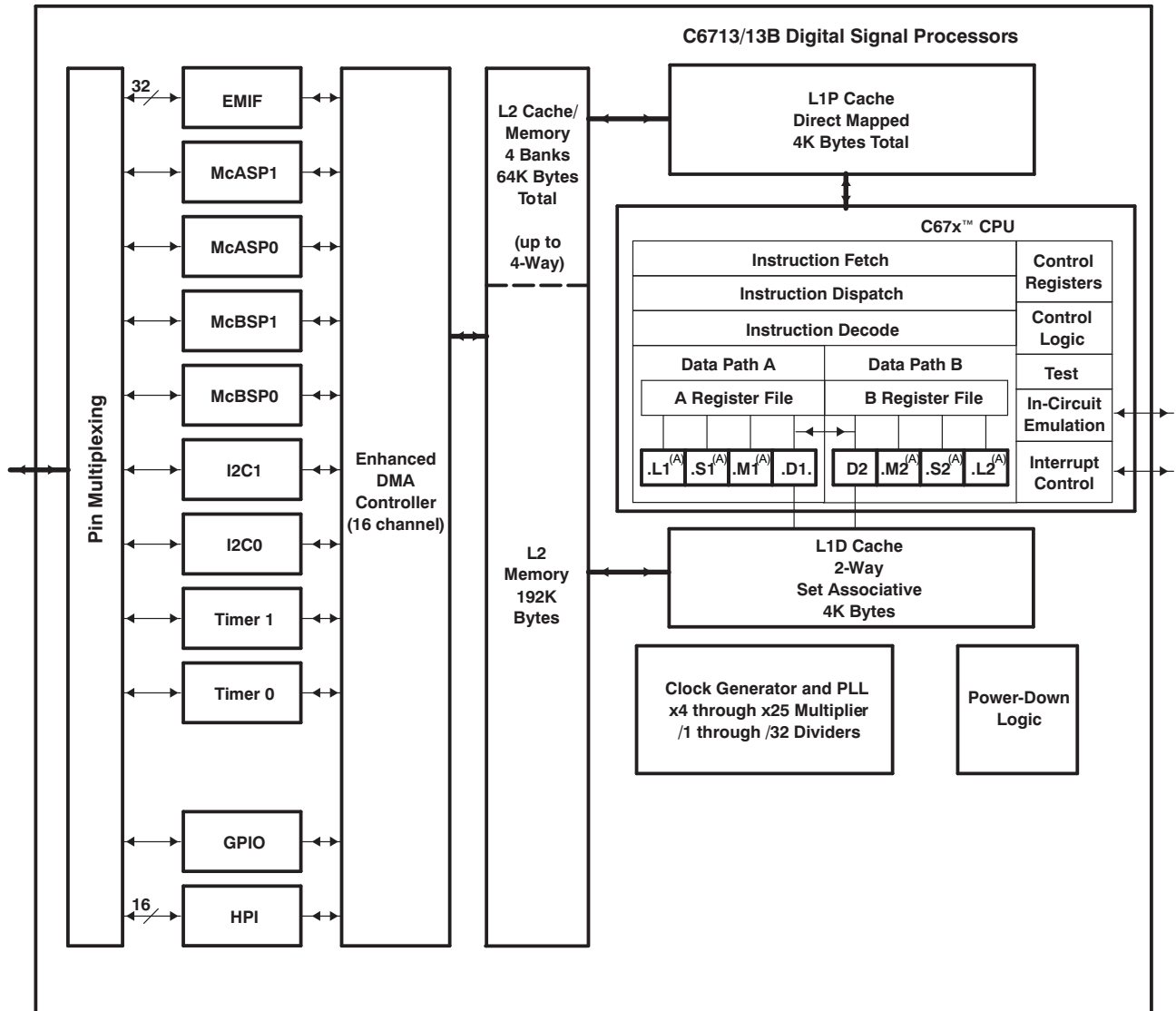
Table 3-2 provides an overview of the C6713/C6713B DSPs. The table shows significant features of each device, including the capacity of on-chip RAM, the peripherals, the execution time, and the package type with pin count. For more details on the C67x™ DSP device part numbers and part numbering, see Table 6-1 and Figure 6-1.

Table 3-2. Characteristics of the C6713 and C6713B Processor

| HARDWARE FEATURES | | INTERNAL CLOCK SOURCE | C6713/C6713B (FLOATING-POINT DSPs) |
|---|---|--------------------------------|---|
| | | | GDP |
| Peripherals Not all peripheral pins are available at the same time. (For more details, see the Device Configurations section.) Peripheral performance is dependent on chip-level configuration. | EMIF | SYSCLK3 or ECLKIN | 1 (32 bit) |
| | EDMA (16 channels) | CPU clock frequency | 1 |
| | HPI (16 bit) | SYSCLK2 | 1 |
| | McASPs | AUXCLK, SYSCLK2 ⁽¹⁾ | 2 |
| | I ² Cs | SYSCLK2 | 2 |
| | McBSPs | SYSCLK2 | 2 |
| | 32-bit timers | ◆ of SYSCLK2 | 2 |
| | GPIO module | SYSCLK2 | 1 |
| On-chip memory | Size (Bytes) | | 264K |
| | Organization | | 4K-Byte (KB) L1 program (L1P) cache 4KB L1 data (L1D) cache 64KB unified L2 cache/mapped RAM 192KB L2 mapped RAM |
| CPU ID+CPU Rev ID | Control Status Register (CSR[31:16]) | | 0x0203 |
| BSDL file | For the C6713/13B BSDL file, contact your field sales representative. | | |
| Frequency | MHz | | 200 |
| Time | ns | | 5 ns |
| Voltage | Core (V) | | 1.26 V (C6713/C6713B) |
| | I/O (V) | | 3.3 V |
| Clock generator options | Prescaler Multiplier Postscaler | | /1, /2, /3, ..., /32 ×4, ×5, ×6, ..., ×25 /1, /2, /3, ..., /32 |
| Package | 27 mm × 27 mm | | 272-ball BGA (GDP) |
| Process technology | µm | | 0.13 |
| Product status ⁽²⁾ Product preview (PP) Advance information (AI) Production data (PD) | | | PD (13) |

- (1) AUXCLK is the McASP internal high-frequency clock source for serial transfers. SYSCLK2 is the McASP system clock used for the clock check (high-frequency) circuit.
- (2) PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice. ADVANCE INFORMATION concerns new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice. PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

3.3 Functional Block and CPU (DSP Core) Diagram



NOTE A: In addition to fixed-point instructions, these functional units execute floating-point instructions.

EMIF interfaces to:
–SDRAM
–SBSRAM
–SRAM
–ROM/flash and I/O devices

McBSPs interface to:
–SPI control port
–High-speed TDM codecs
–AC97 codecs
–Serial EEPROM

McASPs interface to:
–I²S multichannel ADC, DAC, codec, DIR
–DIT: Multiple outputs

4 OVERVIEW

4.1 CPU (DSP Core) Description

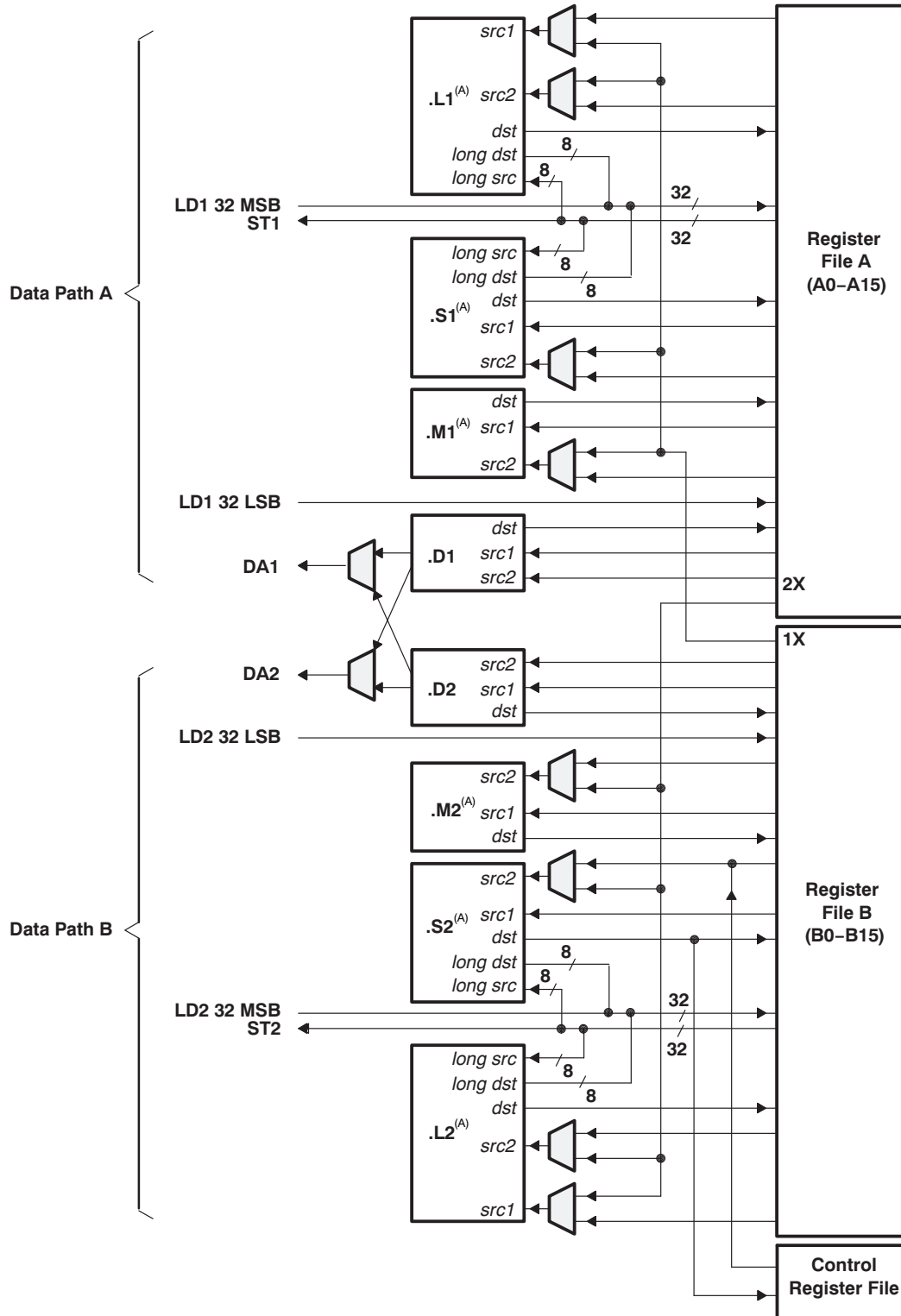
The 320C6713/13B floating-point digital signal processor is based on the C67x CPU. The CPU fetches advanced very-long instruction words (VLIW) (256 bits wide) to supply up to eight 32-bit instructions to the eight functional units during every clock cycle. The VLIW architecture features controls by which all eight units do not have to be supplied with instructions if they are not ready to execute. The first bit of every 32-bit instruction determines if the next instruction belongs to the same execute packet as the previous instruction, or whether it should be executed in the following clock as a part of the next execute packet. Fetch packets are always 256 bits wide; however, the execute packets can vary in size. The variable-length execute packets are a key memory-saving feature, distinguishing the C67x CPU from other VLIW architectures.

The CPU features two sets of functional units. Each set contains four units and a register file. One set contains functional units .L1, .S1, .M1, and .D1. The other set contains units .D2, .M2, .S2, and .L2. The two register files each contain 16 32-bit registers for a total of 32 general-purpose registers. The two sets of functional units, along with two register files, compose sides A and B of the CPU (see the [Functional Block and CPU \(DSP Core\) Diagram](#) and [Figure 4-1](#)). The four functional units on each side of the CPU can freely share the 16 registers belonging to that side. Additionally, each side features a single data bus connected to all the registers on the other side, by which the two sets of functional units can access data from the register files on the opposite side. While register access by functional units on the same side of the CPU as the register file can service all the units in a single clock cycle, register access using the register file across the CPU supports one read and one write per cycle.

The C67x CPU executes all C62x instructions. In addition to C62x fixed-point instructions, the six out of eight functional units (.L1, .S1, .M1, .M2, .S2, and .L2) also execute floating-point instructions. The remaining two functional units (.D1 and .D2) also execute the new LDDW instruction, which loads 64 bits per CPU side for a total of 128 bits per cycle.

Another key feature of the C67x CPU is the load/store architecture, where all instructions operate on registers (as opposed to data in memory). Two sets of data-addressing units (.D1 and .D2) are responsible for all data transfers between the register files and the memory. The data address driven by the .D units allows data addresses generated from one register file to be used to load or store data to or from the other register file. The C67x CPU supports a variety of indirect addressing modes using either linear- or circular-addressing modes with 5- or 15-bit offsets. All instructions are conditional, and most can access any one of the 32 registers. Some registers, however, are singled out to support specific addressing or to hold the condition for conditional instructions (if the condition is not automatically true). The two .M functional units are dedicated for multiplies. The two .S and .L functional units perform a general set of arithmetic, logical, and branch functions with results available every clock cycle.

The processing flow begins when a 256-bit-wide instruction fetch packet is fetched from a program memory. The 32-bit instructions destined for the individual functional units are chained together by 1 bits in the least significant bit (LSB) position of the instructions. The instructions that are chained together for simultaneous execution (up to eight in total) compose an execute packet. A 0 in the LSB of an instruction breaks the chain, effectively placing the instructions that follow it in the next execute packet. If an execute packet crosses the fetch-packet boundary (256 bits wide), the assembler places it in the next fetch packet, while the remainder of the current fetch packet is padded with NOP instructions. The number of execute packets within a fetch packet can vary from one to eight. Execute packets are dispatched to their respective functional units at the rate of one per clock cycle and the next 256-bit fetch packet is not fetched until all the execute packets from the current fetch packet have been dispatched. After decoding, the instructions simultaneously drive all active functional units for a maximum execution rate of eight instructions every clock cycle. While most results are stored in 32-bit registers, they can be subsequently moved to memory as bytes or half-words as well. All load and store instructions are byte, half-word, or word addressable.



A. In addition to fixed-point instructions, these functional units execute floating-point instructions.

Figure 4-1. 320C67x™ CPU (DSP Core) Data Paths

4.2 Memory Map Summary

Table 4-1 shows the memory map address ranges of the C6713/13B devices.

Table 4-1. 320C6713/13B Memory Map Summary

| MEMORY BLOCK DESCRIPTION | BLOCK SIZE (BYTES) | HEX ADDRESS RANGE |
|--|--------------------|---------------------|
| Internal RAM (L2) | 192K | 0000 0000 0002 FFFF |
| Internal RAM/Cache | 64K | 0003 0000 0003 FFFF |
| Reserved | 24M – 256K | 0004 0000 017F FFFF |
| External Memory Interface (EMIF) Registers | 256K | 0180 0000 0183 FFFF |
| L2 Registers | 128K | 0184 0000 0185 FFFF |
| Reserved | 128K | 0186 0000 0187 FFFF |
| HPI Registers | 256K | 0188 0000 018B FFFF |
| McBSP 0 Registers | 256K | 018C 0000 018F FFFF |
| McBSP 1 Registers | 256K | 0190 0000 0193 FFFF |
| Timer 0 Registers | 256K | 0194 0000 0197 FFFF |
| Timer 1 Registers | 256K | 0198 0000 019B FFFF |
| Interrupt Selector Registers | 512 | 019C 0000 019C 01FF |
| Device Configuration Registers | 4 | 019C 0200 019C 0203 |
| Reserved | 256K – 516 | 019C 0204 019F FFFF |
| EDMA RAM and EDMA Registers | 256K | 01A0 0000 01A3 FFFF |
| Reserved | 768K | 01A4 0000 01AF FFFF |
| GPIO Registers | 16K | 01B0 0000 01B0 3FFF |
| Reserved | 240K | 01B0 4000 01B3 FFFF |
| I2C0 Registers | 16K | 01B4 0000 01B4 3FFF |
| I2C1 Registers | 16K | 01B4 4000 01B4 7FFF |
| Reserved | 16K | 01B4 8000 01B4 BFFF |
| McASP0 Registers | 16K | 01B4 C000 01B4 FFFF |
| McASP1 Registers | 16K | 01B5 0000 01B5 3FFF |
| Reserved | 160K | 01B5 4000 01B7 BFFF |
| PLL Registers | 8K | 01B7 C000 01B7 DFFF |
| Reserved | 264K | 01B7 E000 01BB FFFF |
| Emulation Registers | 256K | 01BC 0000 01BF FFFF |
| Reserved | 4M | 01C0 0000 01FF FFFF |
| QDMA Registers | 52 | 0200 0000 0200 0033 |
| Reserved | 16M – 52 | 0200 0034 02FF FFFF |
| Reserved | 720M | 0300 0000 2FFF FFFF |
| McBSP0 Data Port | 64M | 3000 0000 33FF FFFF |
| McBSP1 Data Port | 64M | 3400 0000 37FF FFFF |
| Reserved | 64M | 3800 0000 3BFF FFFF |
| McASP0 Data Port | 1M | 3C00 0000 3C0F FFFF |
| McASP1 Data Port | 1M | 3C10 0000 3C1F FFFF |
| Reserved | 1G + 62M | 3C20 0000 7FFF FFFF |
| EMIF CE0 ⁽¹⁾ | 256M | 8000 0000 8FFF FFFF |
| EMIF CE1 ⁽¹⁾ | 256M | 9000 0000 9FFF FFFF |
| EMIF CE2 ⁽¹⁾ | 256M | A000 0000 AFFF FFFF |
| EMIF CE3 ⁽¹⁾ | 256M | B000 0000 BFFF FFFF |
| Reserved | 1G | C000 0000 FFFF FFFF |

(1) The number of EMIF address pins (EA[21:2]) limits the maximum addressable memory (SDRAM) to 128MB per CE space.

4.3 L2 Memory Structure Expanded

Figure 4-2 shows the detail of the L2 memory structure.

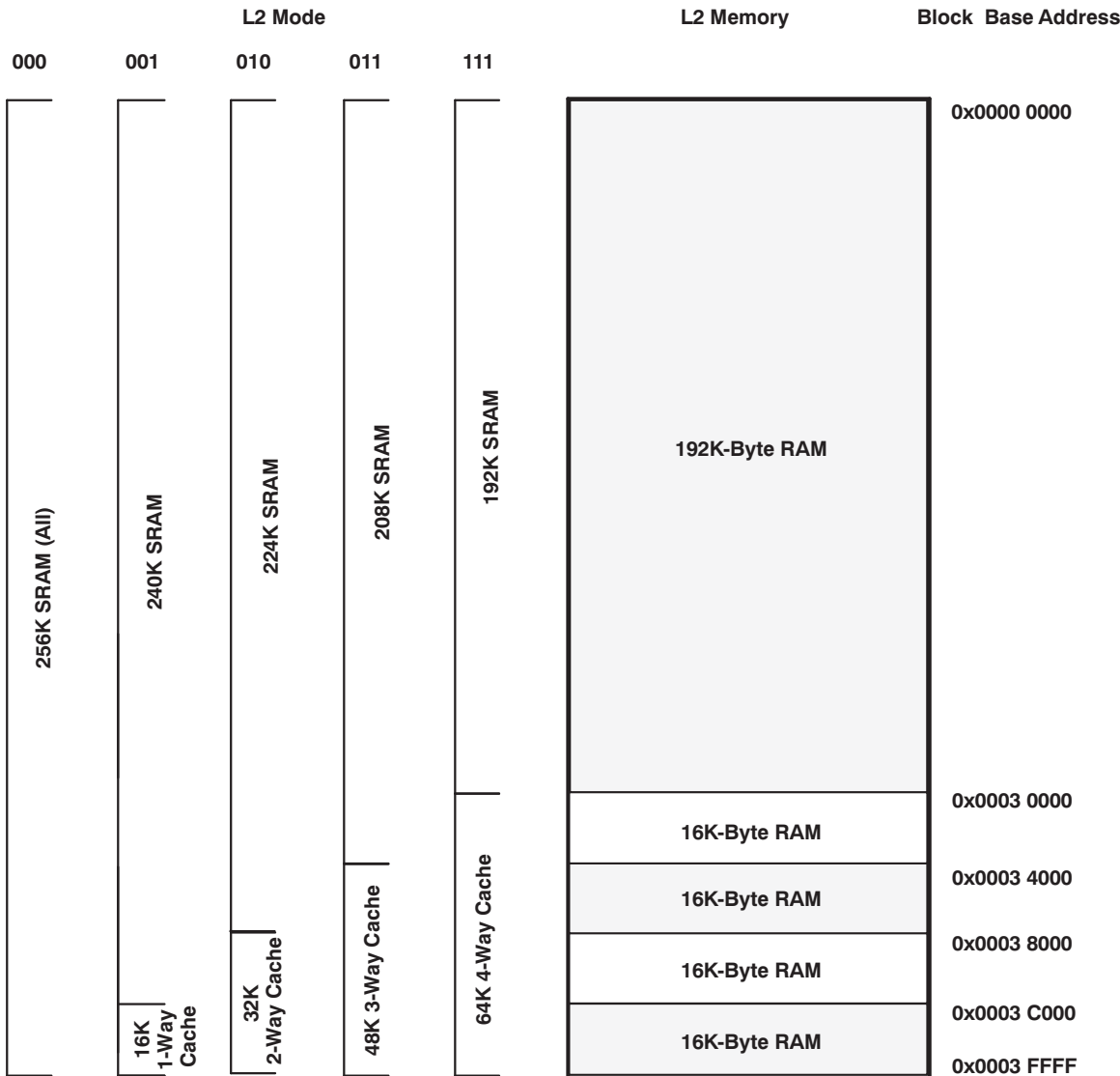


Figure 4-2. L2 Memory Configuration

4.4 Peripheral Register Descriptions

Table 4-2 through Table 4-15 identify the peripheral registers for the C6713/C6713B devices by their register names, acronyms, and hex address or hex address range. For more detailed information on the register contents and bit names and their respective descriptions, see the specific peripheral reference guide listed in the *TMS320C6000 DSP Peripherals Overview Reference Guide* ([literature number SPRU190](#)).

Table 4-2. EMIF Registers

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---------------------|---------|----------------------------|
| 0180 0000 | GBLCTL | EMIF global control |
| 0180 0004 | CECTL1 | EMIF CE1 space control |
| 0180 0008 | CECTL0 | EMIF CE0 space control |
| 0180 000C | — | Reserved |
| 0180 0010 | CECTL2 | EMIF CE2 space control |
| 0180 0014 | CECTL3 | EMIF CE3 space control |
| 0180 0018 | SDCTL | EMIF SDRAM control |
| 0180 001C | SDTIM | EMIF SDRAM refresh control |
| 0180 0020 | SDEXT | EMIF SDRAM extension |
| 0180 0024–0183 FFFF | — | Reserved |

Table 4-3. L2 Cache Registers

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---------------------|----------|--|
| 0184 0000 | CCFG | Cache configuration |
| 0184 4000 | L2WBAR | L2 writeback base address register |
| 0184 4004 | L2WWC | L2 writeback word count |
| 0184 4010 | L2WIBAR | L2 writeback-invalidate base address register |
| 0184 4014 | L2WIWC | L2 writeback-invalidate word count |
| 0184 4020 | L1PIBAR | L1P invalidate base address register |
| 0184 4024 | L1PIWC | L1P invalidate word count |
| 0184 4030 | L1DWIBAR | L1D writeback-invalidate base address register |
| 0184 4034 | L1DWIWC | L1D writeback-invalidate word count |
| 0184 5000 | L2WB | L2 writeback all |
| 0184 5004 | L2WBINV | L2 writeback-invalidate all |
| 0184 8200 | MAR0 | Memory attribute register 0. Controls CE0 range 8000 0000 80FF FFFF |
| 0184 8204 | MAR1 | Memory attribute register 1. Controls CE0 range 8100 0000 81FF FFFF |
| 0184 8208 | MAR2 | Memory attribute register 2. Controls CE0 range 8200 0000 82FF FFFF |
| 0184 820C | MAR3 | Memory attribute register 3. Controls CE0 range 8300 0000 83FF FFFF |
| 0184 8240 | MAR4 | Memory attribute register 4. Controls CE1 range 9000 0000 90FF FFFF |
| 0184 8244 | MAR5 | Memory attribute register 5. Controls CE1 range 9100 0000 91FF FFFF |
| 0184 8248 | MAR6 | Memory attribute register 6. Controls CE1 range 9200 0000 92FF FFFF |
| 0184 824C | MAR7 | Memory attribute register 7. Controls CE1 range 9300 0000 93FF FFFF |
| 0184 8280 | MAR8 | Memory attribute register 8. Controls CE2 range A000 0000 A0FF FFFF |
| 0184 8284 | MAR9 | Memory attribute register 9. Controls CE2 range A100 0000 A1FF FFFF |
| 0184 8288 | MAR10 | Memory attribute register 10. Controls CE2 range A200 0000 A2FF FFFF |
| 0184 828C | MAR11 | Memory attribute register 11. Controls CE2 range A300 0000 A3FF FFFF |
| 0184 82C0 | MAR12 | Memory attribute register 12. Controls CE3 range B000 0000 B0FF FFFF |
| 0184 82C4 | MAR13 | Memory attribute register 13. Controls CE3 range B100 0000 B1FF FFFF |
| 0184 82C8 | MAR14 | Memory attribute register 14. Controls CE3 range B200 0000 B2FF FFFF |
| 0184 82CC | MAR15 | Memory attribute register 15. Controls CE3 range B300 0000 B3FF FFFF |
| 0184 82D0–0185 FFFF | — | Reserved |

Table 4-4. Interrupt Selector Registers

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME | COMMENTS |
|---------------------|---------|-----------------------------|---|
| 019C 0000 | MUXH | Interrupt multiplexer high | Selects which interrupts drive CPU interrupts 10–15 (INT10–INT15) |
| 019C 0004 | MUXL | Interrupt multiplexer low | Selects which interrupts drive CPU interrupts 4–9 (INT04–INT09) |
| 019C 0008 | EXTPOL | External interrupt polarity | Sets the polarity of the external interrupts (EXT_INT4–EXT_INT7) |
| 019C 000C–019F FFFF | — | Reserved | |

Table 4-5. Device Registers

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME | COMMENTS |
|---------------------|---------|-----------------------------|--|
| 019C 0200 | DEVCFG | Device configuration | Allows the user to control peripheral selection. This register also offers the user control of the EMIF input clock source. For more detailed information on the device configuration register, see the Device Configurations section of this data sheet. |
| 019C 0204–019F FFFF | — | Reserved | |
| N/A | CSR | CPU control status register | Identifies which CPU and defines the silicon revision of the CPU. This register also offers the user control of device operation. For more detailed information on the CPU Control Status Register, see the CPU CSR Register description section of this data sheet. |

Table 4-6. EDMA Parameter RAM⁽¹⁾

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|----------------------|---------|---|
| 01A0 0000 01A0 0017 | — | Parameters for Event 0 (6 words) or Reload/Link parameters for other event |
| 01A0 0018 01A0 002F | — | Parameters for Event 1 (6 words) or Reload/Link parameters for other event |
| 01A0 0030 01A0 0047 | — | Parameters for Event 2 (6 words) or Reload/Link parameters for other event |
| 01A0 0048 01A0 005F | — | Parameters for Event 3 (6 words) or Reload/Link parameters for other event |
| 01A0 0060 01A0 0077 | — | Parameters for Event 4 (6 words) or Reload/Link parameters for other event |
| 01A0 0078 01A0 008F | — | Parameters for Event 5 (6 words) or Reload/Link parameters for other event |
| 01A0 0090 01A0 00A7 | — | Parameters for Event 6 (6 words) or Reload/Link parameters for other event |
| 01A0 00A8 01A0 00BF | — | Parameters for Event 7 (6 words) or Reload/Link parameters for other event |
| 01A0 00C0 01A0 00D7 | — | Parameters for Event 8 (6 words) or Reload/Link parameters for other event |
| 01A0 00D8 01A0 00EF | — | Parameters for Event 9 (6 words) or Reload/Link parameters for other event |
| 01A0 00F0 01A0 00107 | — | Parameters for Event 10 (6 words) or Reload/Link parameters for other event |
| 01A0 0108 01A0 011F | — | Parameters for Event 11 (6 words) or Reload/Link parameters for other event |
| 01A0 0120 01A0 0137 | — | Parameters for Event 12 (6 words) or Reload/Link parameters for other event |
| 01A0 0138 01A0 014F | — | Parameters for Event 13 (6 words) or Reload/Link parameters for other event |
| 01A0 0150 01A0 0167 | — | Parameters for Event 14 (6 words) or Reload/Link parameters for other event |
| 01A0 0168 01A0 017F | — | Parameters for Event 15 (6 words) or Reload/Link parameters for other event |
| 01A0 0180 01A0 0197 | — | Reload/link parameters for Event 0–15 |
| 01A0 0198 01A0 01AF | — | Reload/link parameters for Event 0–15 |
| ... | ... | ... |
| 01A0 07E0 01A0 07F7 | — | Reload/link parameters for Event 0–15 |
| 01A0 07F8 01A0 07FF | — | Scratch pad area (two words) |

(1) The C6713/13B device has 85 EDMA parameters total: 16 Event/Reload parameters and 69 Reload-only parameters.

For more details on the EDMA parameter RAM six-word parameter entry structure, see [Figure 4-3](#).

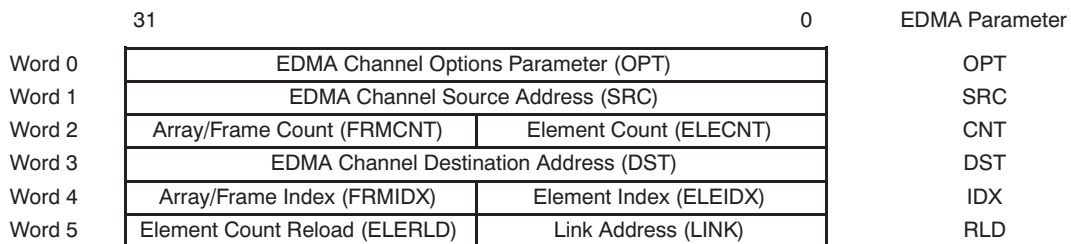


Figure 4-3. EDMA Channel Parameter Entries (Six Words) for Each EDMA Event

Table 4-7. EDMA Registers

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---------------------|---------|------------------------------------|
| 01A0 0800–01A0 FEFC | — | Reserved |
| 01A0 FF00 | ESEL0 | EDMA event selector 0 |
| 01A0 FF04 | ESEL1 | EDMA event selector 1 |
| 01A0 FF08–01A0 FF0B | — | Reserved |
| 01A0 FF0C | ESEL3 | EDMA event selector 3 |
| 01A0 FF1F–01A0 FFDC | — | Reserved |
| 01A0 FFE0 | PQSR | Priority queue status register |
| 01A0 FFE4 | CIPR | Channel interrupt pending register |
| 01A0 FFE8 | CIER | Channel interrupt enable register |
| 01A0 FFEC | CCER | Channel chain enable register |
| 01A0 FFF0 | ER | Event register |
| 01A0 FFF4 | EER | Event enable register |
| 01A0 FFF8 | ECR | Event clear register |
| 01A0 FFFC | ESR | Event set register |
| 01A1 0000–01A3 FFFF | — | Reserved |

Table 4-8. Quick DMA (QDMA) and Pseudo Registers⁽¹⁾

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---------------------|---------|---------------------------------|
| 0200 0000 | QOPT | QDMA options parameter |
| 0200 0004 | QSRC | QDMA source address |
| 0200 0008 | QCNT | QDMA frame count |
| 0200 000C | QDST | QDMA destination address |
| 0200 0010 | QIDX | QDMA index |
| 0200 0014–0200 001C | — | Reserved |
| 0200 0020 | QSOPT | QDMA pseudo options |
| 0200 0024 | QSSRC | QDMA pseudo source address |
| 0200 0028 | QSCNT | QDMA pseudo frame count |
| 0200 002C | QSDST | QDMA pseudo destination address |
| 0200 0030 | QSIDX | QDMA pseudo index |

(1) All the QDMA and Pseudo registers are write accessible only.

Table 4-9. PLL Controller Registers

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---------------------|---------|---|
| 01B7 C000 | PLLPID | Peripheral identification (C6713/13B value: 0x00010801 for PLL Controller) |
| 01B7 C004–01B7 C0FF | — | Reserved |
| 01B7 C100 | PLLCSR | PLL control/status register |
| 01B7 C104–01B7 C10F | — | Reserved |
| 01B7 C110 | PLLM | PLL multiplier control |
| 01B7 C114 | PLLDIV0 | PLL controller divider 0 |
| 01B7 C118 | PLLDIV1 | PLL controller divider 1 |
| 01B7 C11C | PLLDIV2 | PLL controller divider 2 |
| 01B7 C120 | PLLDIV3 | PLL controller divider 3 |
| 01B7 C124 | OSCDIV1 | Oscillator divider 1 |
| 01B7 C128–01B7 DFFF | — | Reserved |

Table 4-10. McASP0 and McASP1 Registers

| HEX ADDRESS RANGE | | ACRONYM | REGISTER NAME AND DESCRIPTION |
|---------------------|---------------------|-------------|--|
| McASP0 | McASP1 | | |
| 3C00 0000–3C00 FFFF | 3C10 0000–3C10 FFFF | RBUF/XBUFx | McASPx receive buffer or McASPx transmit buffer via the peripheral data bus. Used when RSEL or XSEL bits = 0 (these bits are located in the RFMT or XFMT registers, respectively). |
| 01B4 C000 | 01B5 0000 | MCASPPIDx | Peripheral identification [13/13B value: 0x00100101 for McASP0 and for McASP1] |
| 01B4 C004 | 01B5 0004 | PWRDEMUX | Power down and emulation management |
| 01B4 C008 | 01B5 0008 | — | Reserved |
| 01B4 C00C | 01B5 000C | — | Reserved |
| 01B4 C010 | 01B5 0010 | PFUNCx | Pin function |
| 01B4 C014 | 01B5 0014 | PDIRx | Pin direction |
| 01B4 C018 | 01B5 0018 | PDOUTx | Pin data out |
| 01B4 C01C | 01B5 001C | PDIN/PDSETx | Pin data in/data set Read returns: PDIN Writes affect: PDSET |
| 01B4 C020 | 01B5 0020 | PDCLR x | Pin data clear |
| 01B4 C024–01B4 C040 | 01B5 0024–01B5 0040 | — | Reserved |
| 01B4 C044 | 01B5 0044 | GBLCTLx | Global control |
| 01B4 C048 | 01B5 0048 | AMUTEx | Mute control |
| 01B4 C04C | 01B5 004C | DLBCTLx | Digital loopback control |
| 01B4 C050 | 01B5 0050 | DITCTLx | DIT mode control |
| 01B4 C054–01B4 C05C | 01B5 0054–01B5 005C | — | Reserved |
| 01B4 C060 | 01B5 0060 | RGBLCTLx | Alias of GBLCTL containing only Receiver Reset bits; allows transmit to be reset independently from receive |
| 01B4 C064 | 01B5 0064 | RMASKx | Receiver format unit bit mask |
| 01B4 C068 | 01B5 0068 | RFMTx | Receive bit stream format |
| 01B4 C06C | 01B5 006C | AFSRCTLx | Receive frame sync control |
| 01B4 C070 | 01B5 0070 | ACLKRCTLx | Receive clock control |
| 01B4 C074 | 01B5 0074 | AHCLKRCTLx | High-frequency receive clock control |
| 01B4 C078 | 01B5 0078 | RTDMx | Receive TDM slot 0–31 |
| 01B4 C07C | 01B5 007C | RINTCTLx | Receiver interrupt control |
| 01B4 C080 | 01B5 0080 | RSTATx | Status – receiver |
| 01B4 C084 | 01B5 0084 | RSLOTx | Current receive TDM slot |
| 01B4 C088 | 01B5 0088 | RCLKCHKx | Receiver clock check control |
| 01B4 C08C–01B4 C09C | 01B5 008C–01B5 009C | — | Reserved |
| 01B4 C0A0 | 01B5 00A0 | XGBLCTLx | Alias of GBLCTL containing only Transmitter Reset bits; allows transmit to be reset independently from receive |
| 01B4 C0A4 | 01B5 00A4 | XMASKx | Transmit format unit bit mask |
| 01B4 C0A8 | 01B5 00A8 | XFMTx | Transmit bit stream format |
| 01B4 C0AC | 01B5 00AC | AFSXCTLx | Transmit frame sync control |
| 01B4 C0B0 | 01B5 00B0 | ACLKXCTLx | Transmit clock control |
| 01B4 C0B4 | 01B5 00B4 | AHCLKXCTLx | High-frequency Transmit clock control |
| 01B4 C0B8 | 01B5 00B8 | XTDMx | Transmit TDM slot 0–31 |
| 01B4 C0BC | 01B5 00BC | XINTCTLx | Transmit interrupt control |
| 01B4 C0C0 | 01B5 00C0 | XSTATx | Status – transmitter |
| 01B4 C0C4 | 01B5 00C4 | XSLOTx | Current transmit TDM slot |
| 01B4 C0C8 | 01B5 00C8 | XCLKCHKx | Transmit clock check control |
| 01B4 C0D0–01B4 C0FC | 01B5 00CC–01B5 00FC | — | Reserved |
| 01B4 C100 | 01B5 0100 | DITCSRA0x | Left (even TDM slot) channel status register file |
| 01B4 C104 | 01B5 0104 | DITCSRA1x | Left (even TDM slot) channel status register file |
| 01B4 C108 | 01B5 0108 | DITCSRA2x | Left (even TDM slot) channel status register file |
| 01B4 C10C | 01B5 0108 | DITCSRA3x | Left (even TDM slot) channel status register file |
| 01B4 C110 | 01B5 0110 | DITCSRA4x | Left (even TDM slot) channel status register file |

Table 4-10. McASP0 and McASP1 Registers (continued)

| HEX ADDRESS RANGE | | ACRONYM | REGISTER NAME AND DESCRIPTION |
|---------------------|---------------------|-----------|---|
| McASP0 | McASP1 | | |
| 01B4 C114 | 01B5 0114 | DITCSRA5x | Left (even TDM slot) channel status register file |
| 01B4 C118 | 01B5 0118 | DITCSR0x | Right (odd TDM slot) channel status register file |
| 01B4 C11C | 01B5 011C | DITCSR1x | Right (odd TDM slot) channel status register file |
| 01B4 C120 | 01B5 0120 | DITCSR2x | Right (odd TDM slot) channel status register file |
| 01B4 C124 | 01B5 0124 | DITCSR3x | Right (odd TDM slot) channel status register file |
| 01B4 C128 | 01B5 0128 | DITCSR4x | Right (odd TDM slot) channel status register file |
| 01B4 C12C | 01B5 012C | DITCSR5x | Right (odd TDM slot) channel status register file |
| 01B4 C130 | 01B5 0130 | DITUDRA0x | Left (even TDM slot) user data register file |
| 01B4 C134 | 01B5 0134 | DITUDRA1x | Left (even TDM slot) user data register file |
| 01B4 C138 | 01B5 0138 | DITUDRA2x | Left (even TDM slot) user data register file |
| 01B4 C13C | 01B5 013C | DITUDRA3x | Left (even TDM slot) user data register file |
| 01B4 C140 | 01B5 0140 | DITUDRA4x | Left (even TDM slot) user data register file |
| 01B4 C144 | 01B5 0144 | DITUDRA5x | Left (even TDM slot) user data register file |
| 01B4 C148 | 01B5 0148 | DITUDRB0x | Right (odd TDM slot) user data register file |
| 01B4 C14C | 01B5 014C | DITUDRB1x | Right (odd TDM slot) user data register file |
| 01B4 C150 | 01B5 0150 | DITUDRB2x | Right (odd TDM slot) user data register file |
| 01B4 C154 | 01B5 0154 | DITUDRB3x | Right (odd TDM slot) user data register file |
| 01B4 C158 | 01B5 0158 | DITUDRB4x | Right (odd TDM slot) user data register file |
| 01B4 C15C | 01B5 015C | DITUDRB5x | Right (odd TDM slot) user data register file |
| 01B4 C160–01B4 C17C | 01B5 0160–01B5 017C | — | Reserved |
| 01B4 C180 | 01B5 0180 | SRCTL0x | Serializer 0 control |
| 01B4 C184 | 01B5 0184 | SRCTL1x | Serializer 1 control |
| 01B4 C188 | 01B5 0188 | SRCTL2x | Serializer 2 control |
| 01B4 C18C | 01B5 018C | SRCTL3x | Serializer 3 control |
| 01B4 C190 | 01B5 0190 | SRCTL4x | Serializer 4 control |
| 01B4 C194 | 01B5 0194 | SRCTL5x | Serializer 5 control |
| 01B4 C198 | 01B5 0198 | SRCTL6x | Serializer 6 control |
| 01B4 C19C | 01B5 019C | SRCTL7x | Serializer 7 control |
| 01B4 C1A0–01B4 C1FC | 01B5 01A0–01B5 01FC | — | Reserved |
| 01B4 C200 | 01B5 0200 | XBUF0x | Transmit buffer for serializer 0 through configuration bus ⁽¹⁾ |
| 01B4 C204 | 01B5 0204 | XBUF1x | Transmit buffer for serializer 1 through configuration bus ⁽¹⁾ |
| 01B4 C208 | 01B5 0208 | XBUF2x | Transmit buffer for serializer 2 through configuration bus ⁽¹⁾ |
| 01B4 C20C | 01B5 020C | XBUF3x | Transmit buffer for serializer 3 through configuration bus ⁽¹⁾ |
| 01B4 C210 | 01B5 0210 | XBUF4x | Transmit buffer for serializer 4 through configuration bus ⁽¹⁾ |
| 01B4 C214 | 01B5 0214 | XBUF5x | Transmit buffer for serializer 5 through configuration bus ⁽¹⁾ |
| 01B4 C218 | 01B5 0218 | XBUF6x | Transmit buffer for serializer 6 through configuration bus ⁽¹⁾ |
| 01B4 C21C | 01B5 021C | XBUF7x | Transmit buffer for serializer 7 through configuration bus ⁽¹⁾ |
| 01B4 C220–01B4 C27C | 01B5 C220–01B5 027C | — | Reserved |
| 01B4 C280 | 01B5 0280 | RBUF0x | Receive buffer for serializer 0 through configuration bus ⁽²⁾ |
| 01B4 C284 | 01B5 0284 | RBUF1x | Receive buffer for serializer 1 through configuration bus ⁽²⁾ |
| 01B4 C288 | 01B5 0288 | RBUF2x | Receive buffer for serializer 2 through configuration bus ⁽²⁾ |
| 01B4 C28C | 01B5 028C | RBUF3x | Receive buffer for serializer 3 through configuration bus ⁽²⁾ |
| 01B4 C290 | 01B5 0290 | RBUF4x | Receive buffer for serializer 4 through configuration bus ⁽²⁾ |
| 01B4 C294 | 01B5 0294 | RBUF5x | Receive buffer for serializer 5 through configuration bus ⁽²⁾ |
| 01B4 C298 | 01B5 0298 | RBUF6x | Receive buffer for serializer 6 through configuration bus ⁽²⁾ |
| 01B4 C29C | 01B5 029C | RBUF7x | Receive buffer for serializer 7 through configuration bus ⁽²⁾ |
| 01B4 C2A0–01B4 FFFF | 01B5 02A0–01B5 3FFF | — | Reserved |

(1) The transmit buffers for serializers 0–7 are accessible to the CPU via the peripheral bus if the XSEL bit = 1 (XFMT register).

(2) The receive buffers for serializers 0–7 are accessible to the CPU via the peripheral bus if the RSEL bit = 1 (RFMT register).

Table 4-11. I2C0 and I2C1 Registers

| HEX ADDRESS RANGE | | ACRONYM | REGISTER NAME AND DESCRIPTION |
|---------------------|---------------------|----------------------|--|
| I2C0 | I2C1 | | |
| 01B4 0000 | 01B4 4000 | I2COARx | I2Cx own address register |
| 01B4 0004 | 01B4 4004 | I2CIERx | I2Cx interrupt enable register |
| 01B4 0008 | 01B4 4008 | I2CSTRx | I2Cx interrupt status register |
| 01B4 000C | 01B4 400C | I2CCLKLx | I2Cx clock low-time divider |
| 01B4 0010 | 01B4 4010 | I2CCLKHx | I2Cx clock high-time divider |
| 01B4 0014 | 01B4 4014 | I2CCNTx | I2Cx data count |
| 01B4 0018 | 01B4 4018 | I2CDRRx | I2Cx data receive register |
| 01B4 001C | 01B4 401C | I2CSARx | I2Cx slave address register |
| 01B4 0020 | 01B4 4020 | I2CDXRx | I2Cx data transmit register |
| 01B4 0024 | 01B4 4024 | I2CMDRx | I2Cx mode register |
| 01B4 0028 | 01B4 4028 | I2CISRCx | I2Cx interrupt source |
| 01B4 002C | 01B4 402C | — | Reserved |
| 01B4 0030 | 01B4 4030 | I2CPSCx | I2Cx prescaler |
| 01B4 0034 | 01B4 4034 | I2CPID10 I2CPID11 | I2Cx peripheral identification 1 (C6713/13B value: 0x0000 0103) |
| 01B4 0038 | 01B4 4038 | I2CPID20 I2CPID21 | I2Cx peripheral identification 2 (C6713/13B value: 0x0000 0005) |
| 01B4 003C–01B4 3FFF | 01B4 403C–01B4 7FFF | — | Reserved |

Table 4-12. HPI Registers

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME | COMMENTS |
|---------------------|---------|----------------------|---------------------------------|
| — | HPID | HPI data register | Host read/write access only |
| — | HPIA | HPI address register | Host read/write access only |
| 0188 0000 | HPIC | HPI control register | Both Host/CPU read/write access |
| 0188 0004–018B FFFF | — | Reserved | |

Table 4-13. Timer 0 and Timer 1 Registers

| HEX ADDRESS RANGE | | ACRONYM | REGISTER NAME | COMMENTS |
|---------------------|---------------------|---------|--------------------------|---|
| TIMER 0 | TIMER 1 | | | |
| 0194 0000 | 0198 0000 | CTLx | Timer x control register | Determines the operating mode of the timer, monitors the timer status, and controls the function of the TOUT pin. |
| 0194 0004 | 0198 0004 | PRDx | Timer x period register | Contains the number of timer input clock cycles to count. This number controls the TSTAT signal frequency. |
| 0194 0008 | 0198 0008 | CNTx | Timer x counter register | Contains the current value of the incrementing counter. |
| 0194 000C–0197 FFFF | 0198 000C–019B FFFF | — | Reserved | |

Table 4-14. McBSP0 and McBSP1 Registers

| HEX ADDRESS RANGE | | ACRONYM | REGISTER NAME AND DESCRIPTION |
|---------------------|---------------------|---------|---|
| McBSP0 | McBSP1 | | |
| 018C 0000 | 0190 0000 | DRRx | McBSPx data receive register via configuration bus. The CPU and EDMA controller can only read this register; they cannot write to it. |
| 3000 0000–33FF FFFF | 3400 0000–37FF FFFF | DRRx | McBSPx data receive register via peripheral data bus |
| 018C 0004 | 0190 0004 | DXRx | McBSPx data transmit register via configuration bus |
| 3000 0000–33FF FFFF | 3400 0000–37FF FFFF | DXRx | McBSPx data transmit register via peripheral data bus |
| 018C 0008 | 0190 0008 | SPCRx | McBSPx serial port control register |
| 018C 000C | 0190 000C | RCRx | McBSPx receive control register |

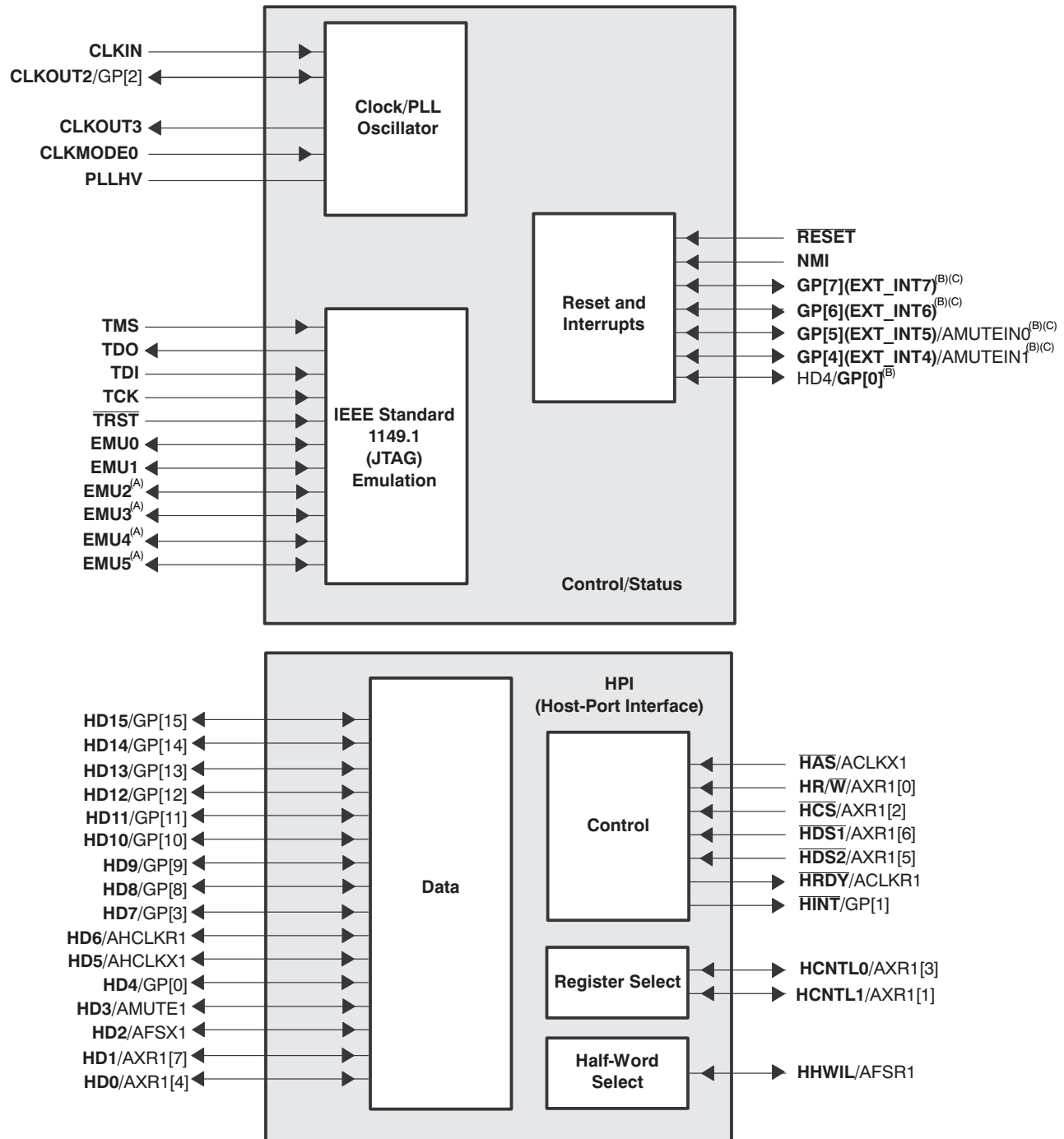
Table 4-14. McBSP0 and McBSP1 Registers (continued)

| HEX ADDRESS RANGE | | ACRONYM | REGISTER NAME AND DESCRIPTION |
|---------------------|---------------------|---------|---|
| McBSP0 | McBSP1 | | |
| 018C 0010 | 0190 0010 | XCRx | McBSPx transmit control register |
| 018C 0014 | 0190 0014 | SRGRx | McBSPx sample rate generator register |
| 018C 0018 | 0190 0018 | MCRx | McBSPx multichannel control register |
| 018C 001C | 0190 001C | RCERx | McBSPx receive channel enable register |
| 018C 0020 | 0190 0020 | XCERx | McBSPx transmit channel enable register |
| 018C 0024 | 0190 0024 | PCRx | McBSPx pin control register |
| 018C 0028–018F FFFF | 0190 0028–0193 FFFF | — | Reserved |

Table 4-15. GPIO Registers

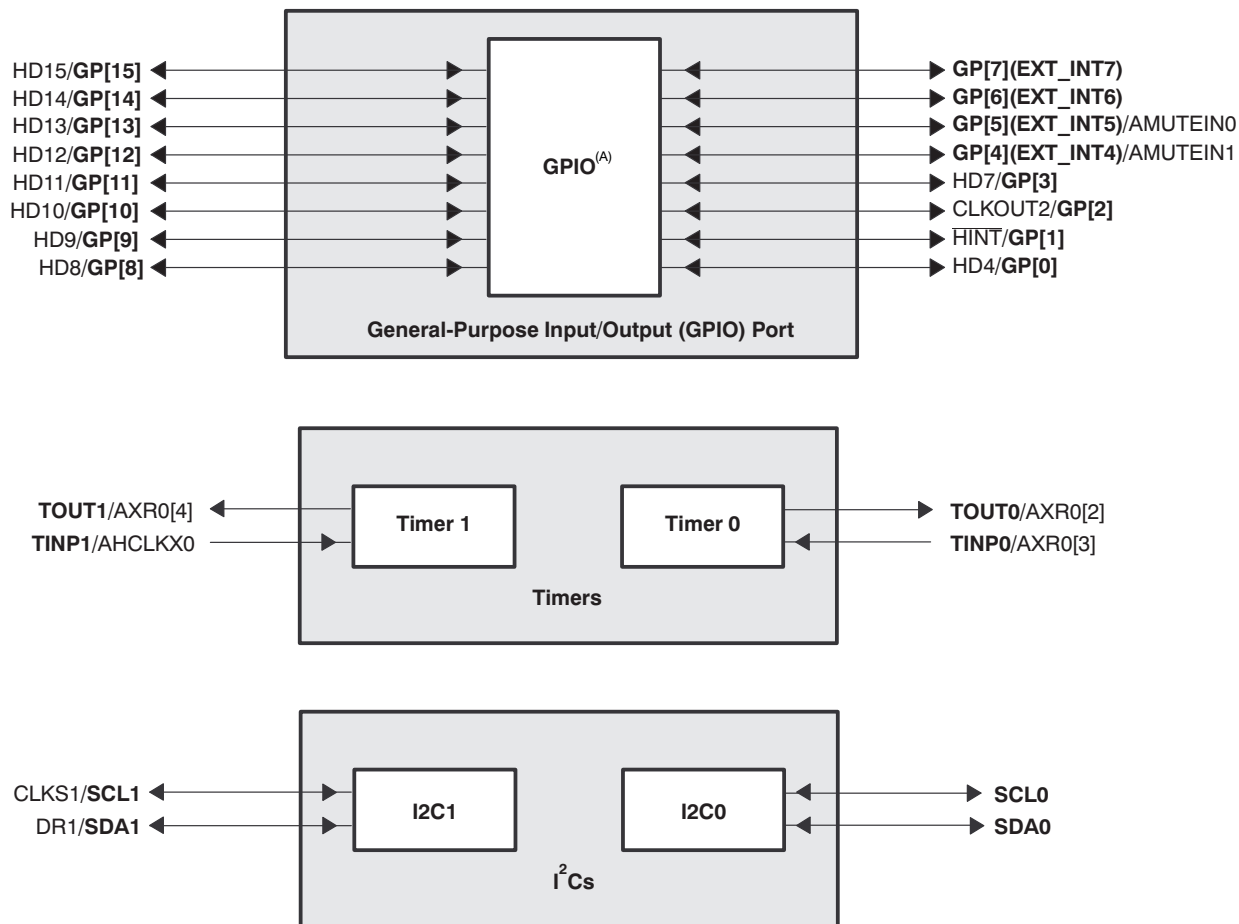
| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---------------------|---------|-------------------------|
| 01B0 0000 | GPEN | GPIO enable |
| 01B0 0004 | GPDIR | GPIO direction |
| 01B0 0008 | GPVAL | GPIO value |
| 01B0 000C | — | Reserved |
| 01B0 0010 | GPDH | GPIO delta high |
| 01B0 0014 | GPHM | GPIO high mask |
| 01B0 0018 | GPDL | GPIO delta low |
| 01B0 001C | GPLM | GPIO low mask |
| 01B0 0020 | GPGC | GPIO global control |
| 01B0 0024 | GPPOL | GPIO interrupt polarity |
| 01B0 0028–01B0 3FFF | — | Reserved |

4.5 Signal Groups Description



- These external pins are applicable to the GDP package only.
- The GP[15:0] pins, through interrupt sharing, are external interrupt capable via GPINT0. For more details, see the external interrupt sources section of this data sheet. For more details on interrupt sharing, see the *TMS320C6000 DSP Interrupt Selector Reference Guide* (literature number [SPRU646](#)).
- All of these pins are external interrupt sources. For more details see the *External Interrupt Sources* section of this data sheet.
- On multiplexed pins, boldface text denotes the active function of the pin for that particular peripheral module.

Figure 4-4. CPU (DSP Core) and Peripheral Signals



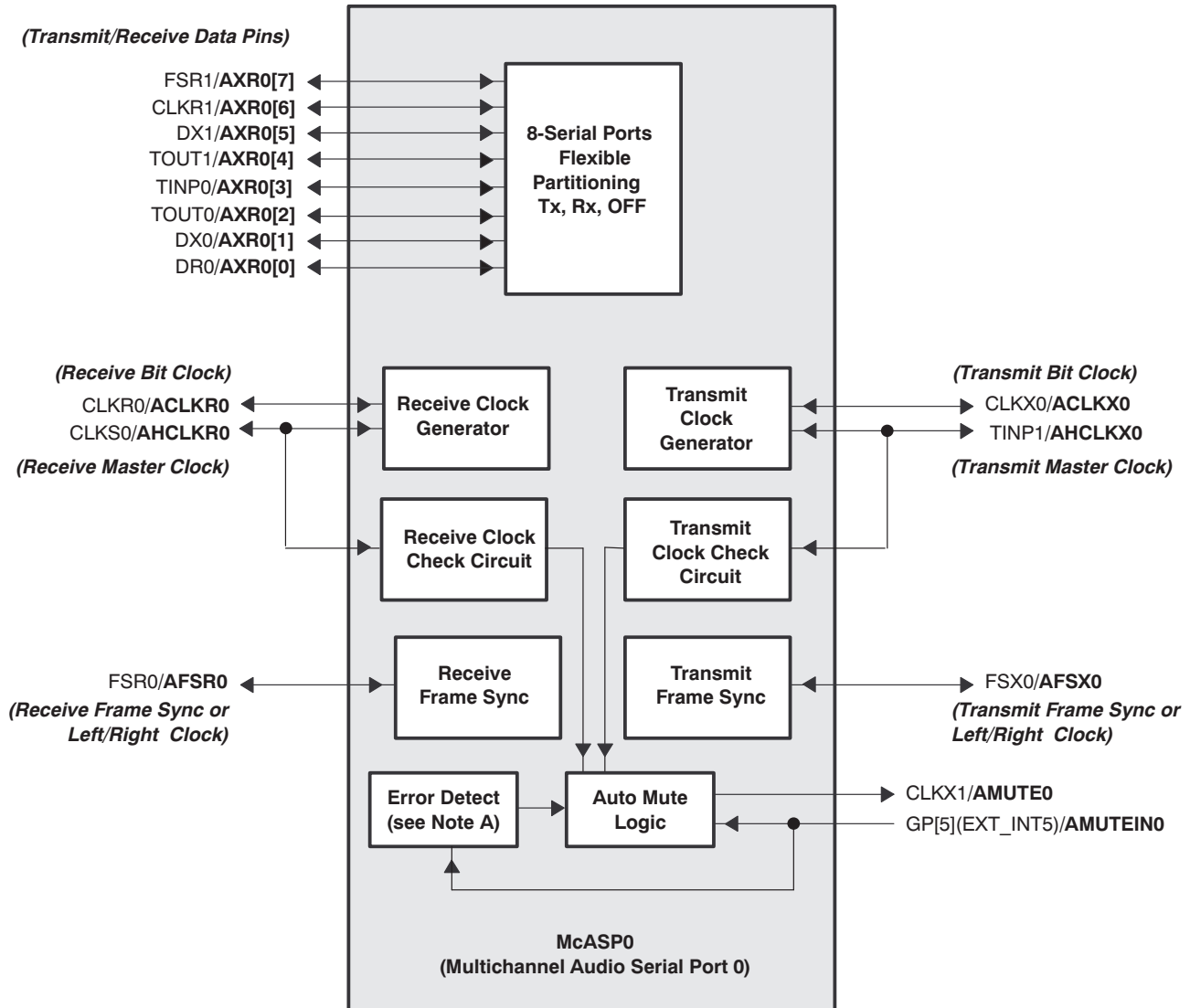
- A. The GP[15:0] pins, through interrupt sharing, are external interrupt capable via GPINT0. GP[15:0] are also external EDMA event source capable. For more details, see the *External Interrupt Sources* and *External EDMA Event Sources* sections of this data sheet.
- B. On multiplexed pins, boldface text denotes the active function of the pin for that particular peripheral module.

Figure 4-5. Peripheral Signals



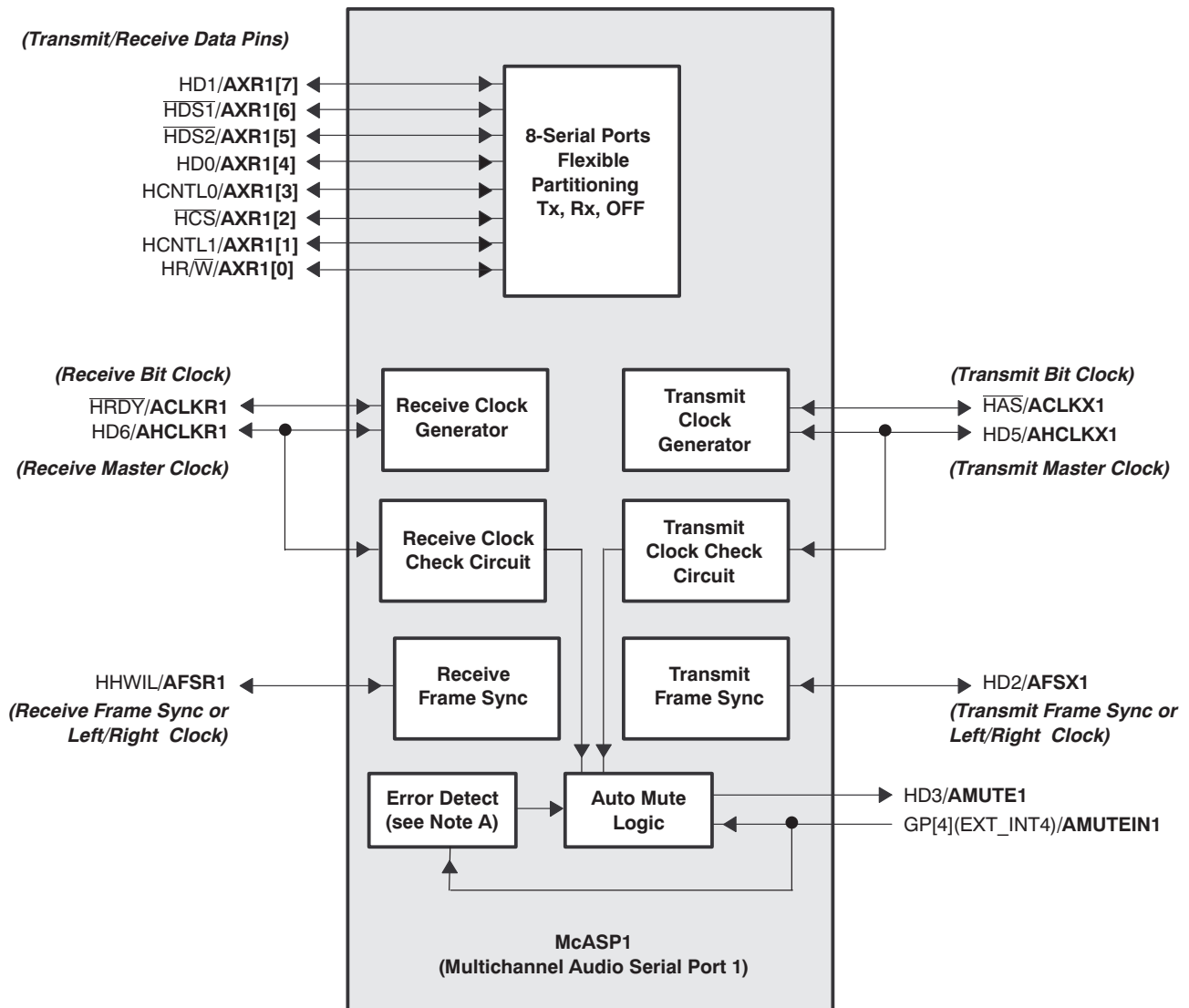
- A. These external pins are applicable to the GDP package only.
- B. On multiplexed pins, boldface text denotes the active function of the pin for that particular peripheral module.

Figure 4-6. Peripheral Signals



- A. The McASP Error Detect function detects underruns, overruns, early/late frame syncs, DMA errors, and external mute input.
- B. On multiplexed pins, boldface text denotes the active function of the pin for that particular peripheral module.
- C. Boldface and italicized text within parentheses denotes the function of the pins in an audio system.

Figure 4-7. Peripheral Signals



- A. The McASP Error Detect function detects underruns, overruns, early/late frame syncs, DMA errors, and external mute input.
- B. On multiplexed pins, boldface text denotes the active function of the pin for that particular peripheral module.
- C. Boldface and italicized text within parentheses denotes the function of the pins in an audio system.

Figure 4-8. Peripheral Signals

5 DEVICE CONFIGURATIONS

On the C6713/13B devices, bootmode and certain device configurations/peripheral selections are determined at device reset, while other device configurations/peripheral selections are software-configurable via the device configurations register (DEVCFG) [address location 0x019C0200] after device reset.

5.1 Device Configurations at Device Reset

Table 5-1 describes the C6713 and C6713B device configuration pins, which are set up via internal or external pullup/pulldown resistors through the HPI data pins (HD[4:3], HD8, HD12 [13B only]), and CLKMODE0 pin. These configuration pins must be in the desired state until reset is released. For proper device operation, do not oppose the HD [13, 11:9, 7, 1, 0] pins with external pullups/pulldowns at reset. For more details on these device configuration pins, see the [Terminal Functions](#) table and the [Debugging Considerations](#) section of this data sheet.

Table 5-1. Device Configurations Pins at Device Reset (HD[4:3], HD8, HD12 [13B only], and CLKMODE0)⁽¹⁾

| CONFIGURATION PIN | GDP | FUNCTIONAL DESCRIPTION |
|--------------------------------------|----------|---|
| HD12 ⁽²⁾ | C15 | <p>EMIF Big Endian mode correctness ($\overline{\text{EMIFBE}}$) [C6713B only] For a C6713BGDP:</p> <ul style="list-style-type: none"> 0 – The EMIF data will always be presented on the ED[7:0] side of the bus, regardless of the endianness mode (Little/Big Endian). 1 – In Little Endian mode (HD8 = 1), the 8-bit or 16-bit EMIF data will be present on the ED[7:0] side of the bus. In Big Endian mode (HD8 = 0), the 8-bit or 16-bit EMIF data will be present on the ED[31:24] side of the bus [default]. <p>For a C6713BPYP, when Big Endian mode is selected (LENDIAN = 0), for proper device operation the EMIFBE pin must be externally pulled low. This enhancement is not supported on the C6713 device. For proper C6713 device operation, do not oppose the internal pullup (IPU) resistor on this pin. This new functionality does not affect systems using the current default value of HD12 = 1. For more detailed information on the big endian mode correctness, see the EMIF Big Endian Mode Correctness [C6713B only] portion of this data sheet.</p> |
| HD8 | B17 | <p>Device Endian mode (LEND)</p> <ul style="list-style-type: none"> 0 – System operates in Big Endian mode 1 – System operates in Little Endian mode (default) |
| HD[4:3] (BOOTMODE) ⁽²⁾ | C19, C20 | <p>Bootmode Configuration pins (BOOTMODE)</p> <ul style="list-style-type: none"> 00 – HPI boot/Emulation boot 01 – $\overline{\text{CE1}}$ width 8-bit, asynchronous external ROM boot with default timings (default mode) 10 – $\overline{\text{CE1}}$ width 16-bit, asynchronous external ROM boot with default timings 11 – $\overline{\text{CE1}}$ width 32-bit, asynchronous external ROM boot with default timings <p>For more detailed information on these bootmode configurations, see the Bootmode section of this data sheet.</p> |
| CLKMODE0 | C4 | <p>Clock generator input clock source select</p> <ul style="list-style-type: none"> 0 – Reserved. Do not use. 1 – CLKIN square wave [default] <p>This pin must be pulled to the correct level even after reset.</p> |

- (1) All other HD pins [HD [15, 13:9, 7:5, 2:0] (for 13) or HD [15, 13, 11:9, 7:5, 2:0] (for 13B)] have pullups/pulldowns (IPUs or IPDs). For proper device operation of the HD [15, 13:9, 7, 1, 0] (for 13) or HD [13, 11:9, 7, 1, 0] (for 13B), **do not** oppose these pins with external pullups/pulldowns at reset; however, the HD[6, 5, 2] (for 13) or HD[15, 6, 5, 2] (for 13B) pins can be opposed and driven during reset.
- (2) IPD = Internal pulldown, IPU = Internal pullup. To oppose the supply rail on these IPD/IPU signal pins, use external pullup or pulldown resistors no greater than 4.4 k Ω and 2.0 k Ω , respectively.

5.2 Peripheral Pin Selection at Device Reset

Some C6713/13B peripherals share the same pins (internally MUXed) and are mutually exclusive (that is, HPI, general-purpose input/output pins GP[15:8, 3, 1, 0], and McASP1).

- HPI, McASP1, and GPIO peripherals

The HPI_EN (HD14 pin) is latched at reset. This pin selects whether the HPI peripheral pins or McASP1 peripheral pins and GP[15:8, 3, 1, 0] pins are functionally enabled (see [Table 5-2](#)).

Table 5-2. HPI_EN (HD14 Pin) Peripheral Selection (HPI or McASP1, and Select GPIO Pins)⁽¹⁾

| PERIPHERAL PIN SELECTION | PERIPHERAL PINS SELECTED | | DESCRIPTION |
|------------------------------|--------------------------|------------------------------|--|
| | HPI | McASP1 and GP[15:8, 3, 1, 0] | |
| HPI_EN (HD14 Pin) [173, C14] | | | |
| 0 | | ✓ | HPI_EN = 0 HPI pins are disabled; McASP1 peripheral pins and GP[15:8, 3, 1, 0] pins are enabled. All multiplexed HPI/McASP1 and HPI/GPIO pins function as McASP1 and GPIO pins, respectively. To use the GPIO pins, the appropriate bits in the GPEN and GPDIR registers need to be configured. |
| 1 | ✓ | | HPI_EN = 1 HPI pins are enabled; McASP1 peripheral pins and GP[15:8, 3, 1, 0] pins are disabled [default]. All multiplexed HPI/McASP1 and HPI/GPIO pins function as HPI pins. |

(1) The HPI_EN (HD[14]) pin **cannot** be controlled via software.

5.3 Peripheral Selection/Device Configurations Via the DEVCFG Control Register

The device configuration register (DEVCFG) allows the user to control the pin availability of the McBSP0, McBSP1, McASP0, I2C1, and timer peripherals. The DEVCFG register also offers the user control of the EMIF input clock source and the timer output pins. For more detailed information on the DEVCFG register control bits, see [Table 5-3](#) and [Table 5-4](#).

Table 5-3. Device Configuration Register (DEVCFG) [Address Location: 0x019C0200–0x019C02FF]

| | | | | | | |
|-------------------------|---|-------|----------|----------|-----------|-----------|
| 31 | | | | | | 16 |
| Reserved ⁽¹⁾ | | | | | | |
| R/W-0 | | | | | | |
| 15 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved ⁽¹⁾ | | EKSRC | TOUT1SEL | TOUT0SEL | MCBSP0DIS | MCBSP1DIS |
| R/W-0 | | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

LEGEND: R = Read, W = Write, --n = value at reset

(1) **Do not** write non-zero values to these bit locations.

Table 5-4. Device Configuration Register (DEVCFG) Selection Bit Descriptions

| BIT NO. | NAME | DESCRIPTION |
|---------|-----------|---|
| 31:5 | Reserved | Reserved. Do not write non-zero values to these bit locations. |
| 4 | EKSRC | EMIF input clock source bit. Determines which clock signal is used as the EMIF input clock. 0 = SYSCLK3 (from the clock generator) is the EMIF input clock source (default). 1 = ECLKIN external pin is the EMIF input clock source. |
| 3 | TOUT1SEL | Timer 1 output (TOUT1) pin function select bit. Selects the pin function of the TOUT1/AXR0[4] external pin independent of the rest of the peripheral selection bits in the DEVCFG register. 0 = The pin functions as a Timer 1 output (TOUT1) pin (default). 1 = The pin functions as the McASP0 transmit/receive data pin 4 (AXR0[4]). The Timer 1 module is still active. |
| 2 | TOUT0SEL | Timer 0 output (TOUT0) pin function select bit. Selects the pin function of the TOUT0/AXR0[2] external pin independent of the rest of the peripheral selection bits in the DEVCFG register. 0 = The pin functions as a Timer 0 output (TOUT0) pin (default). 1 = The pin functions as the McASP0 transmit/receive data pin 2 (AXR0[2]). The Timer 0 module is still active. |
| 1 | MCBSP0DIS | Multichannel Buffered Serial Port 0 (McBSP0) disable bit. Selects whether McBSP0 or the McASP0 multiplexed peripheral pins are enabled or disabled. 0 = McBSP0 peripheral pins are enabled, McASP0 peripheral pins (AHCLKR0, ACLKR0, ACLKX0, AXR0[0], AXR0[1], AFSR0, and AFSX0) are disabled (default). If the McASP0 data pins are available, the McASP0 peripheral is functional for DIT mode only. 1 = McBSP0 peripheral pins are disabled, McASP0 peripheral pins (AHCLKR0, ACLKR0, ACLKX0, AXR0[0], AXR0[1], AFSR0, and AFSX0) are enabled. |
| 0 | MCBSP1DIS | Multichannel Buffered Serial Port 1 (McBSP1) disable bit. Selects whether McBSP1 or I2C1 and McASP0 multiplexed peripheral pins are enabled or disabled. 0 = McBSP1 peripheral pins are enabled, I2C1 peripheral pins (SCL1 and SDA1) and McASP0 peripheral pins (AXR0[7:5] and AMUTE0) are disabled (default) 1 = McBSP1 peripheral pins are disabled, I2C1 peripheral pins (SCL1 and SDA1) and McASP0 peripheral pins (AXR0[7:5] and AMUTE0) are enabled. |

5.4 Multiplexed Pins

Multiplexed (MUXed) pins are pins that are shared by more than one peripheral and are internally multiplexed. Most of these pins are configured by software via the device configuration register (DEVCFG), and the others (specifically, the HPI pins) are configured by external pullup/pulldown resistors only at reset. The MUXed pins that are configured by software can be programmed to switch functionalities at any time. The MUXed pins that are configured by external pullup/pulldown resistors are mutually exclusive; only one peripheral has primary control of the function of these pins after reset. [Table 5-5](#) summarizes the peripheral pins affected by the HPI_EN (HD14 pin) and DEVCFG register. [Table 5-6](#) identifies the multiplexed pins on the C6713/13B devices, shows the default (primary) function and the default settings after reset, and describes the pins, registers, etc., necessary to configure the specific multiplexed functions.

Table 5-5. Peripheral Pin Selection Matrix⁽¹⁾

| SELECTION BITS | | PERIPHERAL PIN AVAILABILITY | | | | | | | | | | |
|--|---------|---|--|-------------------|-------------------|--------|--------|--------------------|--------------------|------|--|---|
| BIT NAME | BIT VAL | MCASP0 ⁽²⁾ | MCASP1 | I ² C0 | I ² C1 | MCBSP0 | MCBSP1 | TIMER0 | TIMER1 | HPI | GPIO PINS | EMIF |
| HPI_EN (boot config pin) | 0 | | AHCLKX1 AHCLKR1 ACLKX1 ACLKR1 AFSX1 AFSR1 AMUTE1 AXR1[0] to AXR1[7] | | | | | | | None | GP[0:1], GP[3], GP[8:15] Plus: GP[2] ctrl'd by GP2EN bit | |
| HPI_EN (boot config pin) | 1 | | None | | | | | | | All | NO GP[0:1], GP[3], GP[8:15] | |
| MCBSP0DIS (DEVCFG bit) | 0 | None | | | | All | | | | | | |
| | 1 | ACLKX0 ACLKR0 AFSX0 AFSR0 AHCLKR0 AXR0[0] AXR0[1] | | | | None | | | | | | |
| MCBSP1DIS (DEVCFG bit) | 0 | NO AMUTE0 AXR0[5] AXR0[6] AXR0[7] | | | None | | All | | | | | |
| | 1 | AMUTE0 AXR0[5] AXR0[6] AXR0[7] | | | All | | None | | | | | |
| TOUT0SEL (DEVCFG bit) | 0 | NO AXR0[2] | | | | | | TOUT0 | | | | |
| | 1 | AXR0[2] | | | | | | NO TOUT0 | | | | |
| TOUT1SEL (DEVCFG bit) | 0 | NO AXR0[4] | | | | | | | TOUT1 | | | |
| | 1 | AXR0[4] | | | | | | | NO TOUT1 | | | |
| HD12 (boot config pin) [13BGDP] ⁽³⁾ | 0 | | | | | | | | | | | ED[7:0]; HD8 = 1/0 |
| | 1 | | | | | | | | | | | ED[7:0] side [HD8 = 1 (Little)] ED[31:24] side [HD8 = 0 (Big)] |

- (1) Gray blocks indicate that the peripheral is not affected by the selection bit.
- (2) The McASP0 pins, AXR0[3] and AHCLKX0, are shared with the timer input pins, TINP0 and TINP1, respectively. See [Table 5-6](#) for more detailed information.
- (3) For more detailed information on endianness correction, see the [EMIF Big Endian Mode Correctness \[C6713B only\]](#) section of this data sheet.

Table 5-6. C6713/13B Device Multiplexed/Shared Pins

| MULTIPLEXED PIN | | DEFAULT FUNCTION | DEFAULT SETTING | DESCRIPTION |
|-----------------|-----|------------------|---|--|
| NAME | GDP | | | |
| CLKOUT2/GP[2] | Y12 | CLKOUT2 | GP2EN = 0 (GPEN register bit) GP[2] function disabled, CLKOUT2 enabled | When the CLKOUT2 pin is enabled, the CLK2EN bit in the EMIF global control register (GBLCTL) controls the CLKOUT2 pin. CLK2EN = 0: CLKOUT2 held high CLK2EN = 1: CLKOUT2 enabled to clock [default]. |

Table 5-6. C6713/13B Device Multiplexed/Shared Pins (continued)

| MULTIPLEXED PIN | | DEFAULT FUNCTION | DEFAULT SETTING | DESCRIPTION |
|------------------------------|-----|------------------------------------|--|---|
| NAME | GDP | | | |
| GP[5](EXT_INT5)/AMUTEIN 0 | C1 | GP[5](EXT_INT5) GP[4](EXT_INT4) | No Function GPxDIR = 0 (input) GP5EN = 0 (disabled) GP4EN = 0 (disabled) [(GPEN register bits) GP[x] function disabled] | To use these software-configurable GPIO pins, the GPxEN bits in the GP Enable Register and the GPxDIR bits in the GP Direction Register must be properly configured. GPxEN = 1: GP[x] pin enabled. GPxDIR = 0: GP[x] pin is an input. GPxDIR = 1: GP[x] pin is an output. To use AMUTEIN0/1 pin function, the GP[5]/GP[4] pins must be configured as an input, the INEN bit set to 1, and the polarity through the INPOL bit selected in the associated McASP AMUTE register. |
| GP[4](EXT_INT4)/AMUTEIN 1 | C2 | | | |
| CLKS0/AHCLKR0 | K3 | McBSP0 pin function | MCBSP0DIS = 0 (DEVCFG register bit) McASP0 pins disabled, McBSP0 pins enabled | By default, McBSP0 peripheral pins are enabled upon reset (McASP0 pins are disabled). To enable the McASP0 peripheral pins, the MCBSP0DIS bit in the DEVCFG register must be set to 1 (disabling the McBSP0 peripheral pins). |
| DR0/AXR0[0] | J1 | | | |
| DX0/AXR0[1] | H2 | | | |
| FSR0/AFSR0 | J3 | | | |
| FSX0/AFSX0 | H1 | | | |
| CLKR0/ACLKR0 | H3 | | | |
| CLKX0/ACLKX0 | G3 | | | |
| CLKS1/SCL1 | E1 | McBSP1 pin function | MCBSP1DIS = 0 (DEVCFG register bit) I2C1 and McASP0 pins disabled, McBSP1 pins enabled | By default, McBSP1 peripheral pins are enabled upon reset (I2C1 and McASP0 pins are disabled). To enable the I2C1 and McASP0 peripheral pins, the MCBSP1DIS bit in the DEVCFG register must be set to 1 (disabling the McBSP1 peripheral pins). |
| DR1/SDA1 | M2 | | | |
| DX1/AXR0[5] | L2 | | | |
| FSR1/AXR0[7] | M3 | | | |
| CLKR1/AXR0[6] | M1 | | | |
| CLKX1/AMUTE0 | L3 | | | |
| HINT/GP[1] | J20 | HPI pin function | HPI_EN (HD14 pin) = 1 (HPI enabled) McASP1 pins and 11 GPIO pins are disabled. | By default, the HPI peripheral pins are enabled at reset. McASP1 peripheral pins and eleven GPIO pins are disabled. To enable the McASP1 peripheral pins and the eleven GPIO pins, an external pulldown resistor must be provided on the HD14 pin setting HPI_EN = 0 at reset. GP enable register and the GPxDIR bits in the GP direction register must be properly configured. To use these software-configurable GPIO pins, the GPxEN bits in the GPxEN = 1: GP[x] pin enabled. GPxDIR = 0: GP[x] pin is an input. GPxDIR = 1: GP[x] pin is an output. McASP1 pin direction is controlled by the PDIR[x] bits in the McASP1PDIR register. |
| HD15/GP[15] | B14 | | | |
| HD14/GP[14] | C14 | | | |
| HD13/GP[13] | A15 | | | |
| HD12/GP[12] | C15 | | | |
| HD11/GP[11] | A16 | | | |
| HD10/GP[10] | B16 | | | |
| HD9/GP[9] | C16 | | | |
| HD8/GP[8] | B17 | | | |
| HD7/GP[3] | A18 | | | |
| HD4/GP[0] | C19 | | | |
| HD1/AXR1[7] | D20 | | | |
| HD0/AXR1[4] | E20 | | | |
| HCNTL1/AXR1[1] | G19 | | | |
| HCNTL0/AXR1[3] | G18 | | | |
| HR \overline{W} /AXR1[0] | G20 | | | |
| HDS1/AXR1[6] | E19 | | | |
| HDS2/AXR1[5] | F18 | | | |
| HCS/AXR1[2] | F20 | | | |
| HD6/AHCLKR1 | C17 | | | |
| HD5/AHCLKX1 | B18 | | | |
| HD3/AMUTE1 | C20 | | | |
| HD2/AFSX1 | D18 | | | |
| HHWIL/AFSR1 | H20 | | | |
| HRDY/ACLKR1 | H19 | | | |
| HAS/ACLKX1 | E18 | | | |

Table 5-6. C6713/13B Device Multiplexed/Shared Pins (continued)

| MULTIPLEXED PIN | | DEFAULT FUNCTION | DEFAULT SETTING | DESCRIPTION |
|-----------------|-----|-------------------------|--|---|
| NAME | GDP | | | |
| TINP0/AXR0[3] | G2 | Timer 0 input function | McASP0PDIR = 0 (input) [specifically AXR0[3] bit] | By default, the Timer 0 input pin is enabled (and a shared input until the McASP0 peripheral forces an output). McASP0PDIR = 0 input, = 1 output |
| TOUT0/AXR0[2] | G1 | Timer 0 output function | TOUT0SEL = 0 (DEVCFG register bit) [TOUT0 pin enabled and McASP0 AXR0[2] pin disabled] | By default, the Timer 0 output pin is enabled. To enable the McASP0 AXR0[2] pin, the TOUT0SEL bit in the DEVCFG register must be set to 1 (disabling the Timer 0 peripheral output pin function). The AXR2 bit in the McASP0PDIR register controls the direction (input/output) of the AXR0[2] pin. McASP0PDIR = 0 input, = 1 output |
| TINP1/AHCLKX0 | F2 | Timer 1 input function | McASP0PDIR = 0 (input) [specifically AHCLKX bit] | By default, the Timer 1 input and McASP0 clock function are enabled as inputs. For the McASP0 clock to function as an output: McASP0PDIR = 1 (specifically the AHCLKX bit). |
| TOUT1/AXR0[4] | F1 | Timer 1 output function | TOUT1SEL = 0 (DEVCFG register bit) [TOUT1 pin enabled and McASP0 AXR0[4] pin disabled] | By default, the Timer 1 output pin is enabled. To enable the McASP0 AXR0[4] pin, the TOUT1SEL bit in the DEVCFG register must be set to 1 (disabling the Timer 1 peripheral output pin function). The AXR4 bit in the McASP0PDIR register controls the direction (input/output) of the AXR0[4] pin. McASP0PDIR = 0 input, = 1 output |

5.5 Configuration Examples

Figure 5-1 through Figure 5-6 illustrate examples of peripheral selections that are configurable on this device.

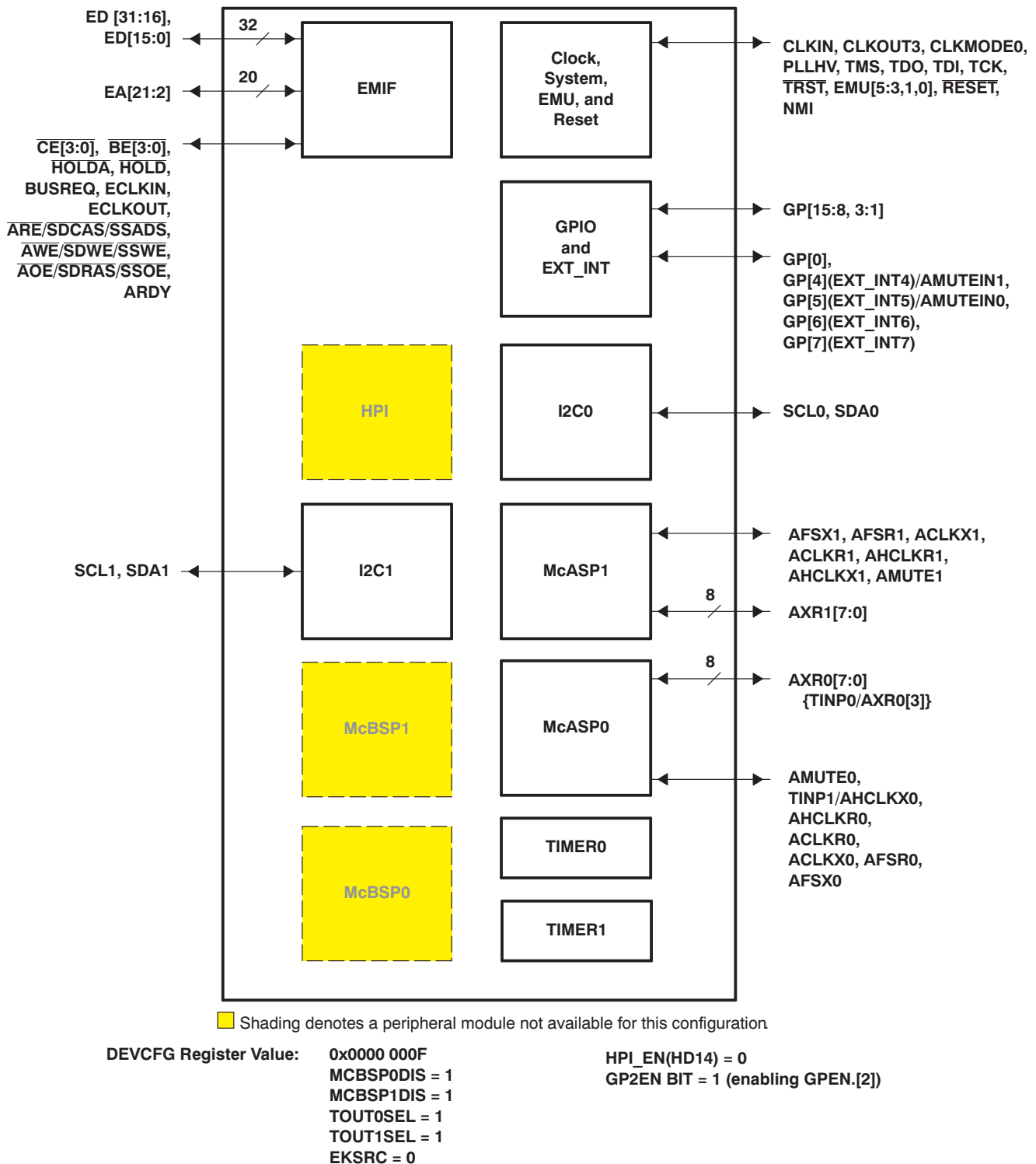
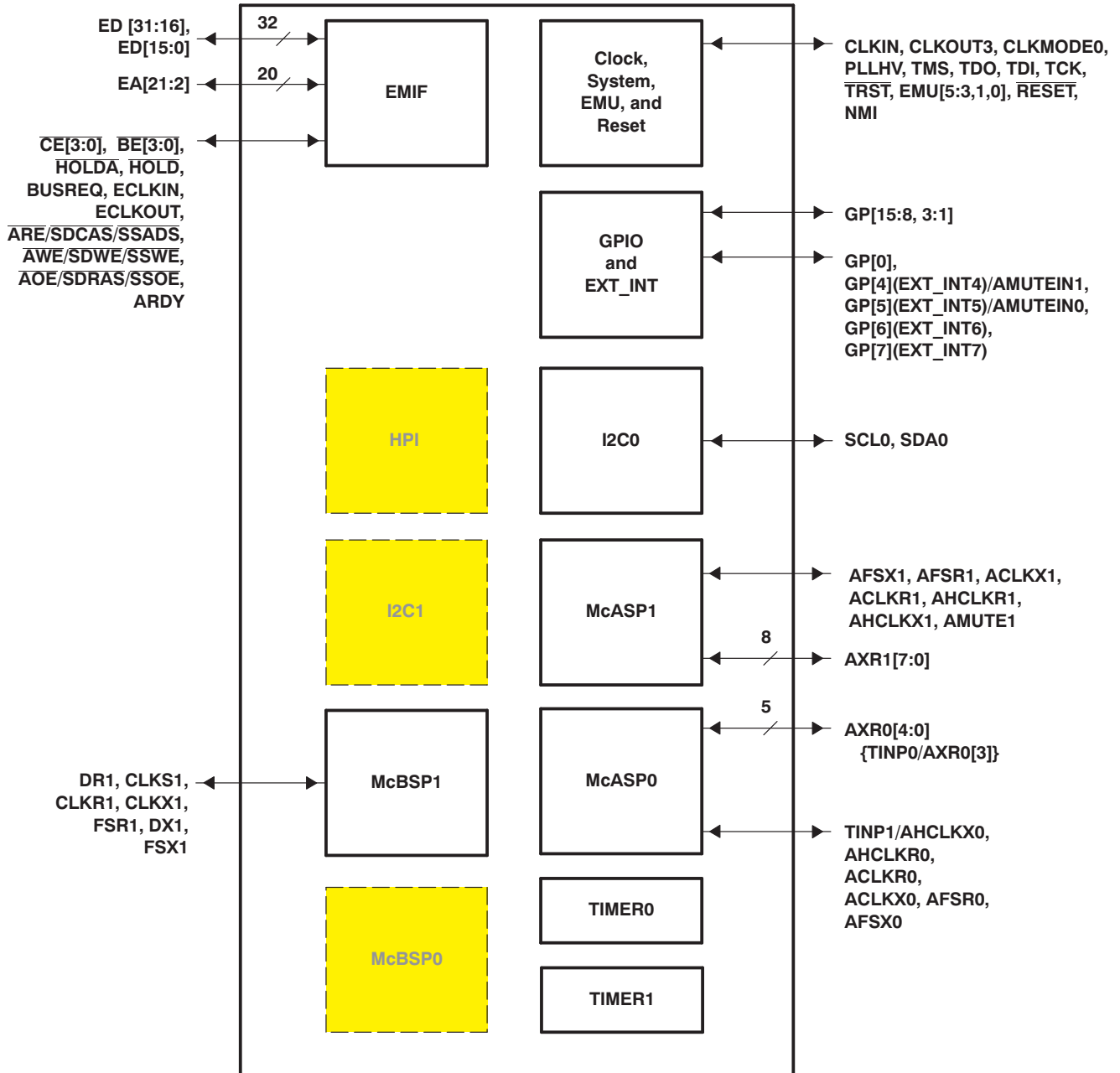


Figure 5-1. Configuration Example A (Two I2C + Two McASP + GPIO)

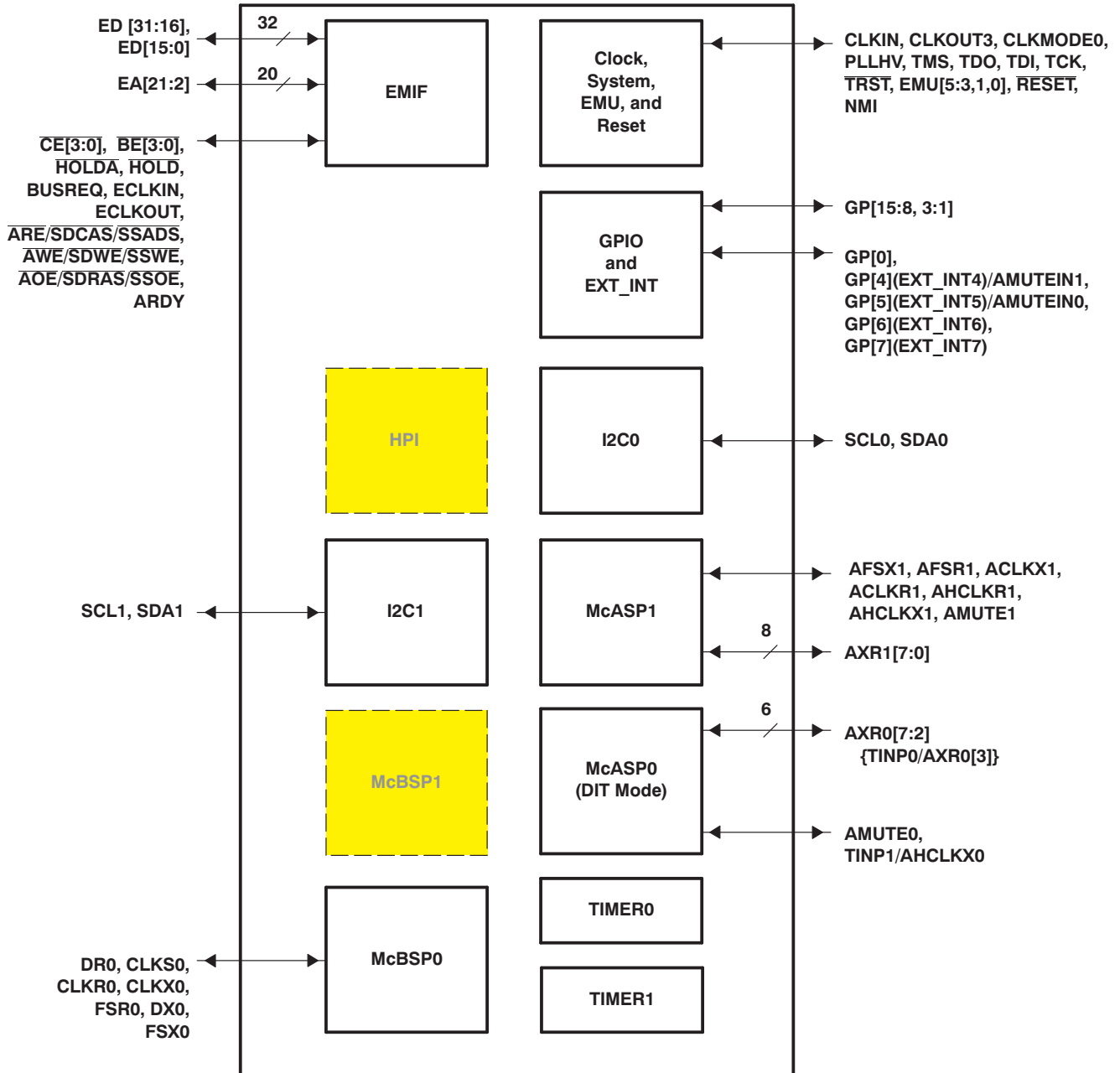


Shading denotes a peripheral module not available for this configuration.

DEVCFG Register Value: 0x0000 000E
 MCBSP0DIS = 1
 MCBSP1DIS = 0
 TOUT0SEL = 1
 TOUT1SEL = 1
 EKSRC = 0

HPI_EN(HD14) = 0
 GP2EN BIT = 1 (enabling GPEN.[2])

Figure 5-2. Configuration Example B (One I2C + One McBSP + Two McASP + GPIO)

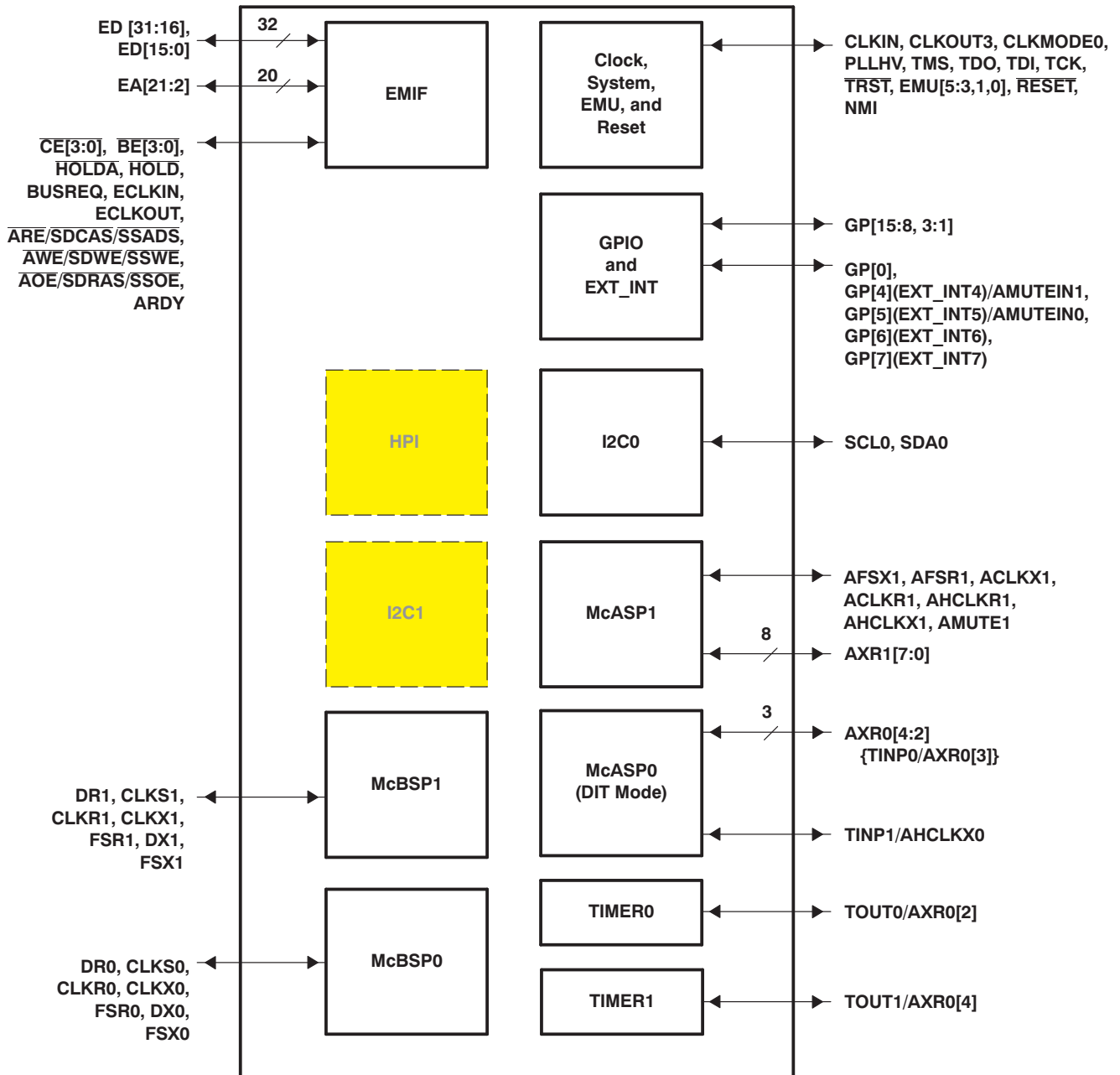


Shading denotes a peripheral module not available for this configuration.

DEVCFG Register Value: 0x0000 000D
 MCBSP0DIS = 0
 MCBSP1DIS = 1
 TOUT0SEL = 1
 TOUT1SEL = 1
 EKSRC = 0

HPI_EN(HD14) = 0
 GP2EN BIT = 1 (enabling GPEN.[2])

Figure 5-3. Configuration Example C [2 I2C + 1 McBSP + 1 McASP + 1 McASP (DIT) + GPIO]

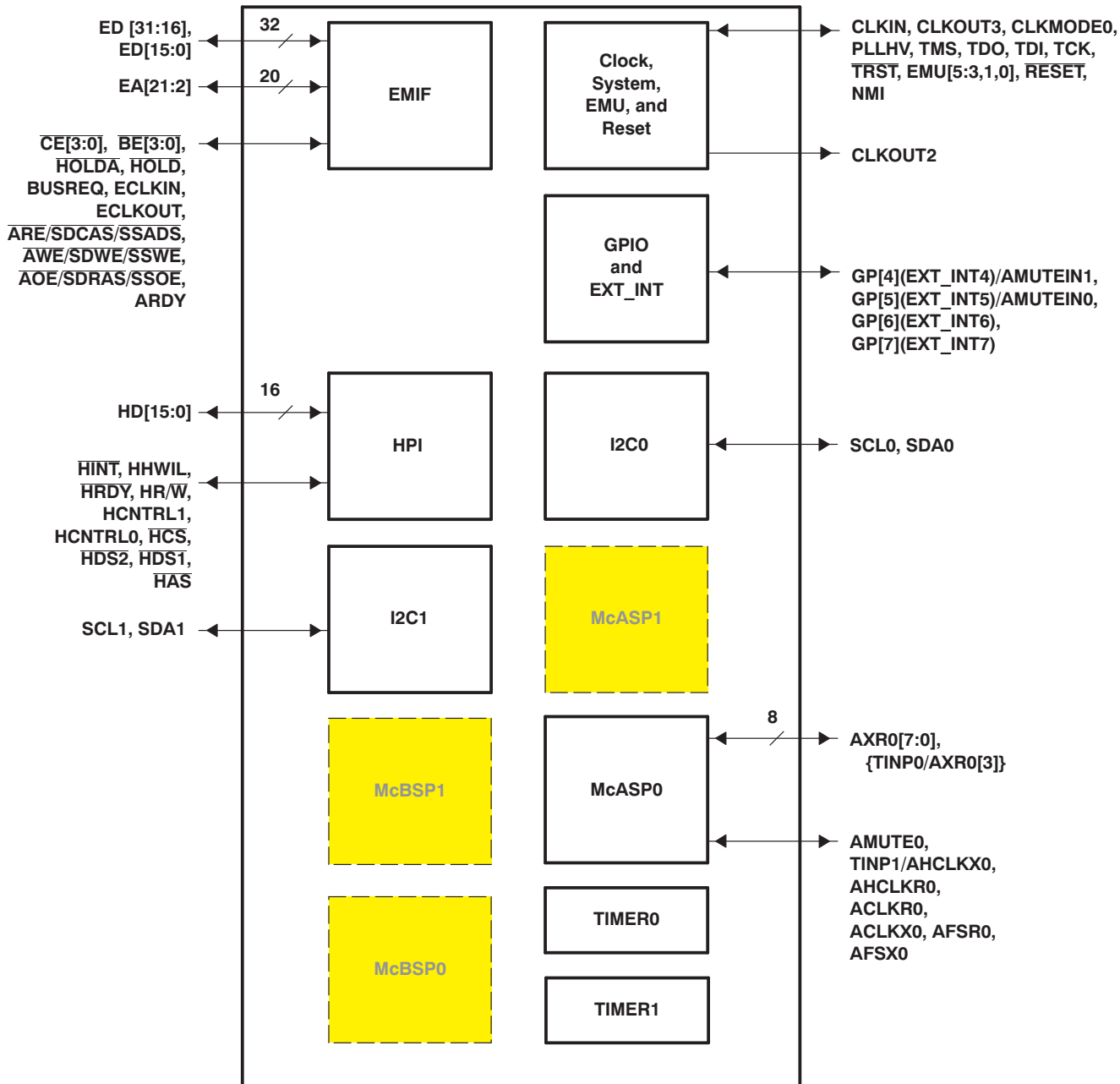


Shading denotes a peripheral module not available for this configuration.

DEVCFG Register Value: 0x0000 000C
 MCBSP0DIS = 0
 MCBSP1DIS = 0
 TOUT0SEL = 1
 TOUT1SEL = 1
 EKSRC = 0

HPI_EN(HD14) = 0
 GP2EN BIT = 1 (enabling GPEN.[2])

Figure 5-4. Configuration Example D [1 I2C + 2 McBSP + 1 McASP + 1 McASP (DIT) + GPIO + Timers]

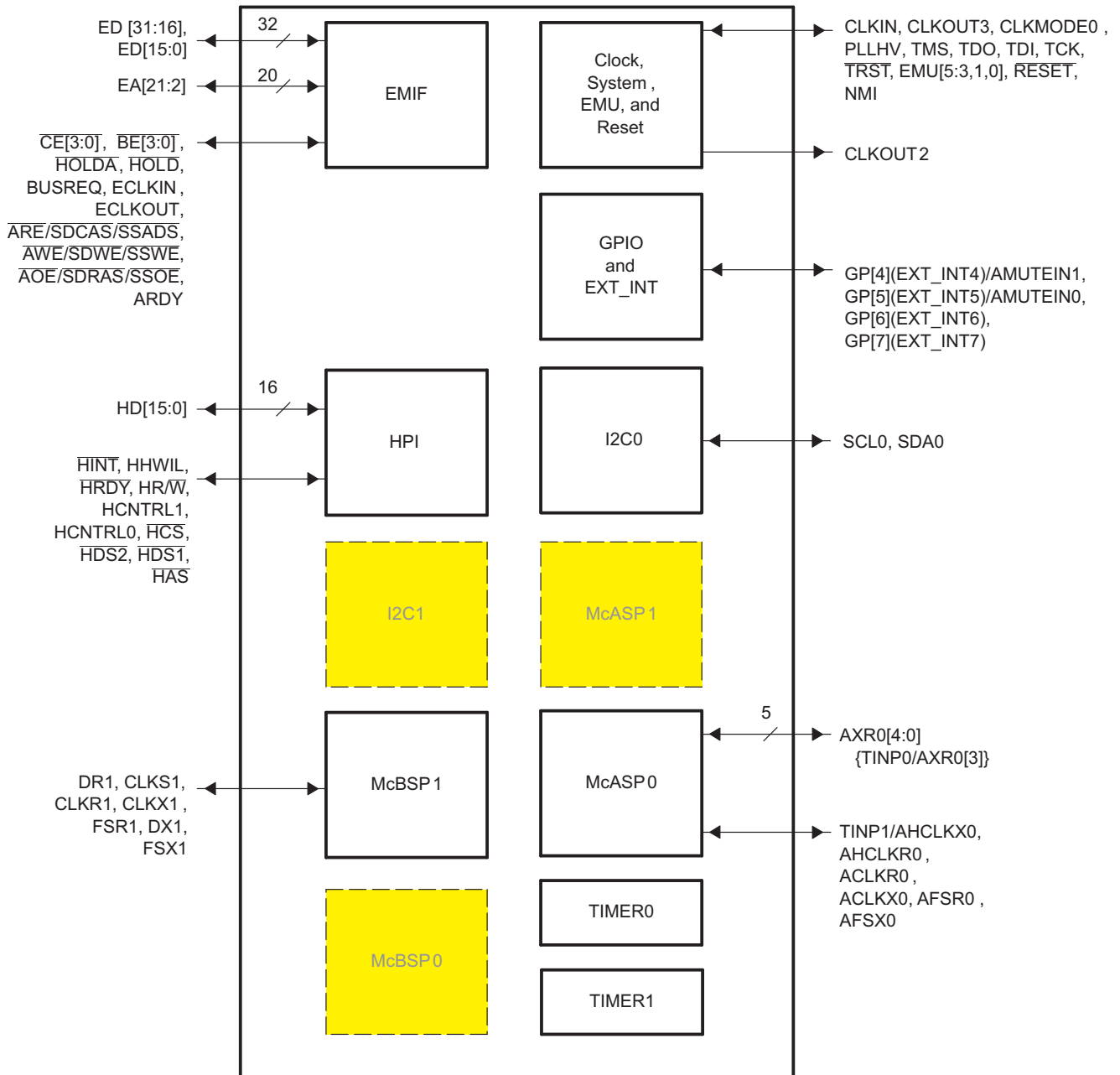


Shading denotes a peripheral module not available for this configuration.

DEVCFG Register Value: 0x0000 000F
 MCBSP0DIS = 1
 MCBSP1DIS = 1
 TOUT0SEL = 1
 TOUT1SEL = 1
 EKSRC = 0

HPI_EN(HD14) = 1
 GP2EN BIT = 0 (enabling GPEN.[2])

Figure 5-5. Configuration Example E (1 I2C + HPI + 1 McASP)



Shading denotes a peripheral module not available for this configuration.

DEVCFG Register V alue: 0x0000 000E
 MCBSP0DIS = 1
 MCBSP1DIS = 0
 TOUT0SEL = 1
 TOUT1SEL = 1
 EKSRC = 0

HPI_EN(HD14) = 1
 GP2EN BIT = 0 (enabling GPEN.[2])

Figure 5-6. Configuration Example F (One McBSP + HPI + One McASP)

5.6 Debugging Considerations

It is recommended that external connections be provided to peripheral selection/device configuration pins, including HD[14, 8, 12 (for 13B only), 4, 3], and CLKMODE0. Although internal pullup resistors exist on these pins, providing external connectivity adds convenience to the user in debugging and flexibility in switching operating modes.

Internal pullup/pulldown resistors also exist on the non-configuration pins on the HPI data bus (HD[15, 13:9, 7:5, 2:0] (for 13) and HD[15, 13, 11:9, 7:5, 2:0] (for 13B)). For proper device operation of the HD[15, 13:9, 7, 1, 0] (for 13) or HD[13, 11:9, 7, 1, 0] (for 13B), do not oppose the internal pullup/pulldown resistors on these non-configuration pins with external pullup/pulldown resistors at reset. If an external controller provides signals to these HD[15, 13:9, 7, 1, 0] (for 13) or HD[13, 11:9, 7, 1, 0] (for 13B) non-configuration pins, these signals must be driven to the default state of the pins at reset, or not be driven at all. For the list of routed out, 3-stated, or not-driven pins recommended for external pullup/pulldown resistors, and internal pullup/pulldown resistors for all devices pins, etc., see [Terminal Functions](#). However, the HD[6, 5, 2] (for 13) or HD[15, 6, 5, 2] (for 13B) non-configuration pins can be opposed and driven during reset.

For the internal pullup/pulldown resistors for all device pins, see the [Terminal Functions](#) table.

6 TERMINAL FUNCTIONS

The [Terminal Functions](#) table identifies the external signal names, the associated pin (ball) numbers along with the mechanical package designator, the pin type (I, O/Z, or I/O/Z), whether the pin has any internal pullup/pulldown resistors and a functional pin description. For more detailed information on device configuration, peripheral selection, multiplexed/shared pins, and debugging considerations, see the [Device Configurations](#) section of this data sheet.

TERMINAL FUNCTIONS

| SIGNAL NAME | PIN NO. | TYPE ⁽¹⁾ | IPD/IPU ⁽²⁾ | DESCRIPTION |
|----------------------------------|----------|---------------------|------------------------|---|
| | GDP | | | |
| CLOCK/PLL CONFIGURATION | | | | |
| CLKIN | A3 | I | IPD | Clock input |
| CLKOUT2/GP[2] | Y12 | O/Z | IPD | Clock output at half of device speed (O/Z) [default] (SYSCLK2 internal signal from the clock generator) or this pin can be programmed as GP[2] pin (I/O/Z). |
| CLKOUT3 | D10 | O | IPD | Clock output programmable by OSCDIV1 register in the PLL controller |
| CLKMODE0 | C4 | I | IPU | Clock generator input clock source select 0: Reserved, do not use 1: CLKIN square wave [default] For proper device operation, this pin must be either left unconnected or externally pulled up with a 1-kΩ resistor. |
| PLLHV | C5 | A ⁽³⁾ | | Analog power (3.3 V) for PLL (PLL filter) |
| JTAG EMULATION | | | | |
| TMS | B7 | I | IPU | JTAG test-port mode select |
| TDO | A8 | O/Z | IPU | JTAG test-port data out |
| TDI | A7 | I | IPU | JTAG test-port data in |
| TCK | A6 | I | IPU | JTAG test-port clock |
| TRST | B6 | I | IPD | JTAG test-port reset. For IEEE Std 1149.1 JTAG compatibility, see the IEEE 1149.1 JTAG Compatibility Statement section of this data sheet. |
| EMU5 | B12 | I/O/Z | IPU | Emulation pin 5. Reserved for future use, leave unconnected. |
| EMU4 | C11 | I/O/Z | IPU | Emulation pin 4. Reserved for future use, leave unconnected. |
| EMU3 | B10 | I/O/Z | IPU | Emulation pin 3. Reserved for future use, leave unconnected. |
| EMU2 | D3 | I/O/Z | IPU | Emulation pin 2. Reserved for future use, leave unconnected. |
| EMU1 EMU0 | B9 D9 | I/O/Z | IPU | Emulation [1:0] • Select the device functional mode of operation Operation: EMU[1:0]: 00 Boundary Scan/Functional Mode (see note) 01 Reserved 10 Reserved 11 Emulation/Functional Mode [default] (see the IEEE 1149.1 JTAG Compatibility Statement of this data sheet) The DSP can be placed in Functional mode when the EMU[1:0] pins are configured for either boundary scan or emulation. Note: When the EMU[1:0] pins are configured for boundary scan mode, the internal pulldown (IPD) on the TRST signal must not be opposed to operate in functional mode. For the boundary scan mode, drive EMU[1:0] and RESET pins low. |
| RESETS AND INTERRUPTS | | | | |
| RESET | A13 | I | — | Device reset. When using boundary scan mode, drive the EMU[1:0] and RESET pins low. |
| NMI | C13 | I | IPD | Nonmaskable interrupt • Edge-driven (rising edge) |
| GP[7](EXT_INT7) | E3 | I/O/Z | IPU | General-purpose input/output pins (I/O/Z), which also function as external interrupts • Edge-driven • Polarity independently selected via the external interrupt polarity register bits (EXTPOL.[3:0]), in addition to the GPIO registers. GP[4] and GP[5] pins also function as AMUTEIN1 McASP1 mute input and AMUTEIN0 McASP0 mute input, respectively, if enabled by the INEN bit in the associated McASP AMUTE register. |
| GP[6](EXT_INT6) | D2 | | | |
| GP[5](EXT_INT5)/ AMUTEIN0 | C1 | | | |
| GP[4](EXT_INT4)/ AMUTEIN1 | C2 | | | |
| HOST-PORT INTERFACE (HPI) | | | | |
| HINT/GP[1] | J20 | O/Z | IPU | Host interrupt (from DSP to host) (O) [default] or this pin can be programmed as a GP[1] pin (I/O/Z) |
| HCNTL1/AXR1[1] | G19 | I | IPU | Host control: Selects between control, address, or data registers (I) [default] or McASP1 data pin 1 (I/O/Z) |
| HCNTL0/AXR1[3] | G18 | I | IPU | Host control: Selects between control, address, or data registers (I) [default] or McASP1 data pin 3 (I/O/Z) |
| HHWIL/AFSR1 | H20 | I | IPU | Host half-word select: First or second half-word (not necessarily high or low order) (I) [default] or McASP1 receive frame sync or left/right clock (LRCLK) (I/O/Z). |
| HR/W/AXR1[0] | G20 | I | IPU | Host read or write select (I) [default] or McASP1 data pin 0 (I/O/Z) |

- (1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground
- (2) IPD = Internal pulldown, IPU = Internal pullup. [These IPD/IPU signal pins feature a 13-kΩ resistor (approximate) for the IPD or 18-kΩ resistor (approximate) for the IPU. An external pullup or pulldown resistor no greater than 4.4 kΩ and 2.0 kΩ, respectively, should be used to pull a signal to the opposite supply rail.]
- (3) A = Analog signal

TERMINAL FUNCTIONS (continued)

| SIGNAL NAME | PIN NO. | TYPE ⁽¹⁾ | IPD/IPU ⁽²⁾ | DESCRIPTION |
|---|---|---------------------|------------------------|--|
| | GDP | | | |
| HD15/GP[15] HD14/GP[14] HD13/GP[13] HD12/GP[12] HD11/GP[11] HD10/GP[10] HD9/GP[9] HD8/GP[8] HD7/GP[3] | B14 C14 A15 C15 A16 B16 C16 B17 A18 | I/O/Z | IPU | <p>Host-port data pins (I/O/Z) [default] or general-purpose input/output pins (I/O/Z)</p> <ul style="list-style-type: none"> Used for transfer of data, address, and control Also controls initialization of DSP modes at reset via pullup/pulldown resistors <ul style="list-style-type: none"> Device Endian mode (HD8) <ul style="list-style-type: none"> 0: Big Endian 1: Little Endian Boot mode (HD[4:3]) <ul style="list-style-type: none"> 00: HPI boot/emulation boot 01: $\overline{CE}1$ width 8-bit, asynchronous external ROM boot with default timings (default mode) 10: $\overline{CE}1$ width 16-bit, asynchronous external ROM boot with default timings 11: $\overline{CE}1$ width 32-bit, asynchronous external ROM boot with default timings <ul style="list-style-type: none"> HPI_EN (HD14) <ul style="list-style-type: none"> 0: HPI disabled, McASP1 enabled 1: HPI enabled, McASP1 disabled (default) <p>Other HD pins (HD [15, 13:9, 7:5, 2:0] have pullups/pulldowns (IPUs/IPDs). For proper device operation, do not oppose these pins with external pullups/pulldowns at reset; however, the HD[15, 6, 5, 2] pins can be opposed and driven at reset. For more details, see the Device Configurations section of this data sheet.</p> |
| HD6/AHCLKR1 | C17 | I/O/Z | IPU | Host-port data pin 6 (I/O/Z) [default] or McASP1 receive high-frequency master clock (I/O/Z) |
| HD5/AHCLKX1 | B18 | I/O/Z | IPU | Host-port data pin 5 (I/O/Z) [default] or McASP1 transmit high-frequency master clock (I/O/Z) |
| HD4/GP[0] | C19 | I/O/Z | IPD | Host-port data pin 4 (I/O/Z) [default] or this pin can be programmed as a GP[0] pin (I/O/Z) |
| HD3/AMUTE1 | C20 | I/O/Z | IPU | Host-port data pin 3 (I/O/Z) [default] or McASP1 mute output (O/Z) |
| HD2/AFSX1 | D18 | I/O/Z | IPU | Host-port data pin 2 (I/O/Z) [default] or McASP1 transmit frame sync or left/right clock (LRCLK) (I/O/Z) |
| HD1/AXR1[7] | D20 | I/O/Z | IPU | Host-port data pin 1 (I/O/Z) [default] or McASP1 data pin 7 (I/O/Z) |
| HD0/AXR1[4] | E20 | I/O/Z | IPU | Host-port data pin 0 (I/O/Z) [default] or McASP1 data pin 4 (I/O/Z) |
| HAS/ACLKX1 | E18 | I | IPU | Host address strobe (I) [default] or McASP1 transmit bit clock (I/O/Z) |
| HCS/AXR1[2] | F20 | I | IPU | Host chip select (I) [default] or McASP1 data pin 2 (I/O/Z) |
| HDS1/AXR1[6] | E19 | I | IPU | Host data strobe 1 (I) [default] or McASP1 data pin 6 (I/O/Z) |
| HDS2/AXR1[5] | F18 | I | IPU | Host data strobe 2 (I) [default] or McASP1 data pin 5 (I/O/Z) |
| HRDY/ACLKR1 | H19 | O/Z | IPD | Host ready (from DSP to host) (O) [default] or McASP1 receive bit clock (I/O/Z) |
| EMIF—COMMON SIGNALS TO ALL TYPES OF MEMORY⁽⁴⁾ | | | | |
| CE3 | V6 | O/Z | IPU | <p>Memory space enables</p> <ul style="list-style-type: none"> Enabled by bits 28 through 31 of the word address Only one asserted during any external data access |
| CE2 | W6 | | | |
| CE1 | W18 | | | |
| CE0 | V17 | | | |
| BE3 | V5 | O/Z | IPU | <p>Byte-enable control</p> <ul style="list-style-type: none"> Decoded from the two lowest bits of the internal address Byte-write enables for most types of memory Can be directly connected to SDRAM read and write mask signal (SDQM) |
| BE2 | Y4 | | | |
| BE1 | U19 | | | |
| BE0 | V20 | | | |
| EMIF—BUS ARBITRATION⁽⁴⁾ | | | | |
| HOLDA | J18 | O/Z | IPU | Hold-request-acknowledge to the host |
| HOLD | J17 | I | IPU | Hold request from the host |
| BUSREQ | J19 | O/Z | IPU | Bus request output |
| EMIF—ASYNCHRONOUS/SYNCHRONOUS MEMORY CONTROL⁽⁴⁾ | | | | |
| ECLKIN | Y11 | I | IPD | External EMIF input clock source |
| ECLKOUT | Y10 | O/Z | IPD | <p>EMIF output clock depends on the EKSRC bit (DEVCFG.[4]) and on EKEN bit (GBLCTL.[5]).</p> <p>EKSRC = 0 ECLKOUT is based on the internal SYSCLK3 signal from the clock generator (default).</p> <p>EKSRC = 1 ECLKOUT is based on the external EMIF input clock source pin (ECLKIN)</p> <p>EKEN = 0 ECLKOUT held low</p> <p>EKEN = 1 ECLKOUT enabled to clock (default)</p> |
| ARE/SDCAS/ SSADS | V11 | O/Z | IPU | Asynchronous memory read enable/SDRAM column-address strobe/SBSRAM address strobe |
| AOE/SDRAS/ SSOE | W10 | O/Z | IPU | Asynchronous memory output enable/SDRAM row-address strobe/SBSRAM output enable |
| AWE/SDWE/ SSWE | V12 | O/Z | IPU | Asynchronous memory write enable/SDRAM write enable/SBSRAM write enable |
| ARDY | Y5 | I | IPU | Asynchronous memory ready input |

(4) To maintain signal integrity for the EMIF signals, serial termination resistors should be inserted into all EMIF output signal lines.

TERMINAL FUNCTIONS (continued)

| SIGNAL NAME | PIN NO. | TYPE ⁽¹⁾ | IPD/IPU ⁽²⁾ | DESCRIPTION | | | | | | | | | | | | |
|-----------------------------------|---------|---------------------|------------------------|--|--------------|------|---------|----|------|--------------|----|------|--------------|---|------|--------------|
| | GDP | | | | | | | | | | | | | | | |
| EMIF—ADDRESS⁽⁴⁾ | | | | | | | | | | | | | | | | |
| EA21 | U18 | O/Z | IPU | <p>External address (word, half-word, and byte address) The EMIF adjusts the address based on memory width:</p> <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Width</th> <th>Pins</th> <th>Address</th> </tr> </thead> <tbody> <tr> <td>32</td> <td>21:2</td> <td>21 through 2</td> </tr> <tr> <td>16</td> <td>21:2</td> <td>20 through 1</td> </tr> <tr> <td>8</td> <td>21:2</td> <td>19 through 0</td> </tr> </tbody> </table> <p>For more details on address width adjustments, see the External Memory Interface (EMIF) chapter of the <i>TMS320C6000 Peripherals Reference Guide</i> (literature number SPRU190)</p> | Width | Pins | Address | 32 | 21:2 | 21 through 2 | 16 | 21:2 | 20 through 1 | 8 | 21:2 | 19 through 0 |
| Width | Pins | | | | Address | | | | | | | | | | | |
| 32 | 21:2 | | | | 21 through 2 | | | | | | | | | | | |
| 16 | 21:2 | | | | 20 through 1 | | | | | | | | | | | |
| 8 | 21:2 | | | | 19 through 0 | | | | | | | | | | | |
| EA20 | Y18 | | | | | | | | | | | | | | | |
| EA19 | W17 | | | | | | | | | | | | | | | |
| EA18 | Y16 | | | | | | | | | | | | | | | |
| EA17 | V16 | | | | | | | | | | | | | | | |
| EA16 | Y15 | | | | | | | | | | | | | | | |
| EA15 | W15 | | | | | | | | | | | | | | | |
| EA14 | Y14 | | | | | | | | | | | | | | | |
| EA13 | W14 | | | | | | | | | | | | | | | |
| EA12 | V14 | | | | | | | | | | | | | | | |
| EA11 | W13 | | | | | | | | | | | | | | | |
| EA10 | V10 | | | | | | | | | | | | | | | |
| EA9 | Y9 | | | | | | | | | | | | | | | |
| EA8 | V9 | | | | | | | | | | | | | | | |
| EA7 | Y8 | | | | | | | | | | | | | | | |
| EA6 | W8 | | | | | | | | | | | | | | | |
| EA5 | V8 | | | | | | | | | | | | | | | |
| EA4 | W7 | | | | | | | | | | | | | | | |
| EA3 | V7 | | | | | | | | | | | | | | | |
| EA2 | Y6 | | | | | | | | | | | | | | | |

TERMINAL FUNCTIONS (continued)

| SIGNAL NAME | PIN NO. GDP | TYPE ⁽¹⁾ | IPD/IPU ⁽²⁾ | DESCRIPTION |
|--|----------------|---------------------|------------------------|--|
| EMIF—DATA⁽⁵⁾ | | | | |
| ED31 | N3 | I/O/Z | IPU | External data pins (ED[31:16] pins applicable to GDP package only) |
| ED30 | P3 | | | |
| ED29 | P2 | | | |
| ED28 | P1 | | | |
| ED27 | R2 | | | |
| ED26 | R3 | | | |
| ED25 | T2 | | | |
| ED24 | T1 | | | |
| ED23 | U3 | | | |
| ED22 | U1 | | | |
| ED21 | U2 | | | |
| ED20 | V1 | | | |
| ED19 | V2 | | | |
| ED18 | Y3 | | | |
| ED17 | W4 | | | |
| ED16 | V4 | | | |
| ED15 | T19 | | | |
| ED14 | T20 | | | |
| ED13 | T18 | | | |
| ED12 | R20 | | | |
| ED11 | R19 | | | |
| ED10 | P20 | | | |
| ED9 | P18 | | | |
| ED8 | N20 | | | |
| ED7 | N19 | | | |
| ED6 | N18 | | | |
| ED5 | M20 | | | |
| ED4 | M19 | | | |
| ED3 | L19 | | | |
| ED2 | L18 | | | |
| ED1 | K19 | | | |
| ED0 | K18 | | | |
| MULTICHANNEL AUDIO SERIAL PORT 1 (McASP1) | | | | |
| GP[4](EXT_INT4)/AMUTEIN1 | C2 | I/O/Z | IPU | General-purpose input/output pin 4 and external interrupt 4 (I/O/Z) [default] or McASP1 mute input (I/O/Z) |
| HD3/AMUTE1 | C20 | I/O/Z | IPU | Host-port data pin 3 (I/O/Z) [default] or McASP1 mute output (O/Z) |
| HRDY/ACLKR1 | H19 | I/O/Z | IPU | Host ready (from DSP to host) (O) [default] or McASP1 receive bit clock (I/O/Z) |
| HD6/AHCLKR1 | C17 | I/O/Z | IPU | Host-port data pin 6 (I/O/Z) [default] or McASP1 receive high-frequency master clock (I/O/Z) |
| HAS/ACLKX1 | E18 | I/O/Z | IPU | Host address strobe (I) [default] or McASP1 transmit bit clock (I/O/Z) |
| HD5/AHCLKX1 | B18 | I/O/Z | IPU | Host-port data pin 5 (I/O/Z) [default] or McASP1 transmit high-frequency master clock (I/O/Z) |
| HHWL/AFSR1 | H20 | I/O/Z | IPU | Host half-word select – first or second half-word (not necessarily high or low order) (I) [default] or McASP1 receive frame sync or left/right clock (LRCLK) (I/O/Z) |
| HD2/AFSX1 | D18 | I/O/Z | IPU | Host-port data pin 2 (I/O/Z) [default] or McASP1 transmit frame sync or left/right clock (LRCLK) (I/O/Z) |
| HD1/AXR1[7] | D20 | I/O/Z | IPU | Host-port data pin 1 (I/O/Z) [default] or McASP1 TX/RX data pin 7 (I/O/Z) |
| HDS1/AXR1[6] | E19 | I/O/Z | IPU | Host data strobe 1 (I) [default] or McASP1 TX/RX data pin 6 (I/O/Z) |
| HDS2/AXR1[5] | F18 | I/O/Z | IPU | Host data strobe 2 (I) [default] or McASP1 TX/RX data pin 5 (I/O/Z) |
| HD0/AXR1[4] | E20 | I/O/Z | IPU | Host-port data pin 0 (I/O/Z) [default] or McASP1 TX/RX data pin 4 (I/O/Z) |
| HCNTL0/AXR1[3] | G18 | I/O/Z | IPU | Host control – selects between control, address, or data registers (I) [default] or McASP1 TX/RX data pin 3 (I/O/Z) |
| HCS/AXR1[2] | F20 | I/O/Z | IPU | Host chip select (I) [default] or McASP1 TX/RX data pin 2 (I/O/Z) |
| HCNTL1/AXR1[1] | G19 | I/O/Z | IPU | Host control – selects between control, address, or data registers (I) [default] or McASP1 TX/RX data pin 1 (I/O/Z) |
| HRW/AXR1[0] | G20 | I/O/Z | IPU | Host read or write select (I) [default] or McASP1 TX/RX data pin 0 (I/O/Z) |

(5) To maintain signal integrity for the EMIF signals, serial termination resistors should be inserted into all EMIF output signal lines.

TERMINAL FUNCTIONS (continued)

| SIGNAL NAME | PIN NO. | TYPE ⁽¹⁾ | IPD/IPU ⁽²⁾ | DESCRIPTION |
|---|---------|---------------------|------------------------|---|
| | GDP | | | |
| MULTICHANNEL AUDIO SERIAL PORT 0 (McASP0) | | | | |
| GP[5](EXT_INT5)/AMUTEIN0 | C1 | I/O/Z | IPU | General-purpose input/output pin 5 and external interrupt 5 (I/O/Z) [default] or McASP0 mute input (I/O/Z) |
| CLKX1/AMUTE0 | L3 | I/O/Z | IPD | McBSP1 transmit clock (I/O/Z) [default] or McASP0 mute output (O/Z) |
| CLKR0/ACLKR0 | H3 | I/O/Z | IPD | McBSP0 receive clock (I/O/Z) [default] or McASP0 receive bit clock (I/O/Z) |
| TINP1/AHCLKX0 | F2 | I/O/Z | IPD | Timer 1 input (I) [default] or McBSP0 transmit high-frequency master clock (I/O/Z) |
| CLKX0/ACLKX0 | G3 | I/O/Z | IPD | McBSP0 transmit clock (I/O/Z) [default] or McASP0 transmit bit clock (I/O/Z) |
| CLKS0/AHCLKR0 | K3 | I/O/Z | IPD | McBSP0 external clock source (as opposed to internal) (I) [default] or McASP0 receive high-frequency master clock (I/O/Z) |
| FSR0/AFSR0 | J3 | I/O/Z | IPD | McBSP0 receive frame sync (I/O/Z) [default] or McASP0 receive frame sync or left/right clock (LRCLK) (I/O/Z) |
| FSX0/AFSX0 | H1 | I/O/Z | IPD | McBSP0 transmit frame sync (I/O/Z) [default] or McASP0 transmit frame sync or left/right clock (LRCLK) (I/O/Z) |
| FSR1/AXR0[7] | M3 | I/O/Z | IPD | McBSP1 receive frame sync (I/O/Z) [default] or McASP0 TX/RX data pin 7 (I/O/Z) |
| CLKR1/AXR0[6] | M1 | I/O/Z | IPD | McBSP1 receive clock (I/O/Z) [default] or McASP0 TX/RX data pin 6 (I/O/Z) |
| DX1/AXR0[5] | L2 | I/O/Z | IPU | McBSP1 transmit data (O/Z) [default] or McASP0 TX/RX data pin 5 (I/O/Z) |
| TOUT1/AXR0[4] | F1 | I/O/Z | IPD | Timer 1 output (O) [default] or McASP0 TX/RX data pin 4 (I/O/Z) |
| TINP0/AXR0[3] | G2 | I/O/Z | IPD | Timer 0 input (I) [default] or McASP0 TX/RX data pin 3 (I/O/Z) |
| TOUT0/AXR0[2] | G1 | I/O/Z | IPD | Timer 0 output (O) [default] or McASP0 TX/RX data pin 2 (I/O/Z) |
| DX0/AXR0[1] | H2 | I/O/Z | IPU | McBSP0 transmit data (O/Z) [default] or McASP0 TX/RX data pin 1 (I/O/Z) |
| DR0/AXR0[0] | J1 | I/O/Z | IPU | McBSP0 receive data (I) [default] or McASP0 TX/RX data pin 0 (I/O/Z) |
| TIMER1 | | | | |
| TOUT1/AXR0[4] | F1 | O | IPD | Timer 1 output (O) [default] or McASP0 TX/RX data pin 4 (I/O/Z) |
| TINP1/AHCLKX0 | F2 | I | IPD | Timer 1 input (I) [default] or McBSP0 transmit high-frequency master clock (I/O/Z). This pin defaults as Timer 1 input (I) and McASP transmit high-frequency master clock input (I). |
| TIMER0 | | | | |
| TOUT0/AXR0[2] | G1 | O | IPD | Timer 0 output (O) [default] or McASP0 TX/RX data pin 2 (I/O/Z) |
| TINP0/AXR0[3] | G2 | I | IPD | Timer 0 input (I) [default] or McASP0 TX/RX data pin 3 (I/O/Z) |
| MULTICHANNEL BUFFERED SERIAL PORT 1 (McBSP1) | | | | |
| CLKS1/SCL1 | E1 | I | — | McBSP1 external clock source (as opposed to internal) (I) [default] or I2C1 clock (I/O/Z). This pin does not have an internal pullup or pulldown. When this pin is used as a McBSP pin, this pin should either be driven externally at all times or be pulled up with a 10-kΩ resistor to a valid logic level. Because it is common for some ICs to 3-state their outputs at times, a 10-kΩ pullup resistor may be desirable even when an external device is driving the pin. |
| CLKR1/AXR0[6] | M1 | I/O/Z | IPD | McBSP1 receive clock (I/O/Z) [default] or McASP0 TX/RX data pin 6 (I/O/Z) |
| CLKX1/AMUTE0 | L3 | I/O/Z | IPD | McBSP1 transmit clock (I/O/Z) [default] or McASP0 mute output (O/Z) |
| DR1/SDA1 | M2 | I | — | McBSP1 receive data (I) [default] or I2C1 data (I/O/Z). This pin does not have an internal pullup or pulldown. When this pin is used as a McBSP pin, this pin should either be driven externally at all times or be pulled up with a 10-kΩ resistor to a valid logic level. Because it is common for some ICs to 3-state their outputs at times, a 10-kΩ pullup resistor may be desirable even when an external device is driving the pin. |
| DX1/AXR0[5] | L2 | O/Z | IPU | McBSP1 transmit data (O/Z) [default] or McASP0 TX/RX data pin 5 (I/O/Z) |
| FSR1/AXR0[7] | M3 | I/O/Z | IPD | McBSP1 receive frame sync (I/O/Z) [default] or McASP0 TX/RX data pin 7 (I/O/Z) |
| FSX1 | L1 | I/O/Z | IPD | McBSP1 transmit frame sync |
| MULTICHANNEL BUFFERED SERIAL PORT 0 (McBSP0) | | | | |
| CLKS0/AHCLKR0 | K3 | I | IPD | McBSP0 external clock source (as opposed to internal) (I) [default] or McASP0 receive high-frequency master clock (I/O/Z) |
| CLKR0/ACLKR0 | H3 | I/O/Z | IPD | McBSP0 receive clock (I/O/Z) [default] or McASP0 receive bit clock (I/O/Z) |
| CLKX0/ACLKX0 | G3 | I/O/Z | IPD | McBSP0 transmit clock (I/O/Z) [default] or McASP0 transmit bit clock (I/O/Z) |
| DR0/AXR0[0] | J1 | I | IPU | McBSP0 receive data (I) [default] or McASP0 TX/RX data pin 0 (I/O/Z) |
| DX0/AXR0[1] | H2 | O/Z | IPU | McBSP0 transmit data (O/Z) [default] or McASP0 TX/RX data pin 1 (I/O/Z) |
| FSR0/AFSR0 | J3 | I/O/Z | IPD | McBSP0 receive frame sync (I/O/Z) [default] or McASP0 receive frame sync or left/right clock (LRCLK) (I/O/Z) |
| FSX0/AFSX0 | H1 | I/O/Z | IPD | McBSP0 transmit frame sync (I/O/Z) [default] or McASP0 transmit frame sync or left/right clock (LRCLK) (I/O/Z) |
| INTER-INTEGRATED CIRCUIT 1 (I2C1) | | | | |
| CLKS1/SCL1 | E1 | I/O/Z | — | McBSP1 external clock source (as opposed to internal) (I) [default] or I2C1 clock (I/O/Z). This pin <i>must</i> be externally pulled up. When this pin is used as an I ² C pin, the value of the pullup resistor depends on the number of devices connected to the I ² C bus. For more details, see the <i>Philips I²C Specification Revision 2.1</i> (January 2000). |
| DR1/SDA1 | M2 | I/O/Z | — | McBSP1 receive data (I) [default] or I2C1 data (I/O/Z). This pin <i>must</i> be externally pulled up. When this pin is used as an I ² C pin, the value of the pullup resistor depends on the number of devices connected to the I ² C bus. For more details, see the <i>Philips I²C Specification Revision 2.1</i> (January 2000). |
| INTER-INTEGRATED CIRCUIT 0 (I2C0) | | | | |
| SCL0 | N1 | I/O/Z | — | I2C0 clock. This pin <i>must</i> be externally pulled up. When this pin is used as an I ² C pin, the value of the pull-up resistor depends on the number of devices connected to the I ² C bus. For more details, see the <i>Philips I²C Specification Revision 2.1</i> (January 2000). |

TERMINAL FUNCTIONS (continued)

| SIGNAL NAME | PIN NO. | TYPE ⁽¹⁾ | IPD/IPU ⁽²⁾ | DESCRIPTION |
|--|---|---------------------|------------------------|--|
| | GDP | | | |
| SDA0 | N2 | I/O/Z | — | I ² C0 data. This pin <i>must</i> be externally pulled up. When this pin is used as an I ² C pin, the value of the pull-up resistor depends on the number of devices connected to the I ² C bus. For more details, see the <i>Philips I²C Specification Revision 2.1</i> (January 2000). |
| GENERAL-PURPOSE INPUT/OUTPUT (GPIO) | | | | |
| HD15/GP[15] | B14 | I/O/Z | IPU | Host-port data pins (I/O/Z) [default] or general-purpose input/output pins (I/O/Z) and some function as boot configuration pins at reset. <ul style="list-style-type: none"> Used for transfer of data, address, and control Also controls initialization of DSP modes at reset via pullup/pulldown resistors |
| HD14/GP[14] | C14 | I/O/Z | IPU | |
| HD13/GP[13] | A15 | I/O/Z | IPU | As general-purpose input/output (GP[x]) functions, these pins are software configurable through registers. The GPxEN bits in the GP Enable register and the GPxDIR bits in the GP Direction register must be properly configured: <p>GPxEN = 1; GP[x] pin is enabled. GPxDIR = 0; GP[x] pin is an input. GPxDIR = 1; GP[x] pin is an output.</p> |
| HD12/GP[12] | C15 | I/O/Z | IPU | |
| HD11/GP[11] | A16 | I/O/Z | IPU | For the functionality description of the Host-port data pins or the boot configuration pins, see the Host-Port Interface (HPI) portion of this table. |
| HD10/GP[10] | B16 | I/O/Z | IPU | |
| HD9/GP[9] | C16 | I/O/Z | IPU | General-purpose input/output pins (I/O/Z) that also function as external interrupts <ul style="list-style-type: none"> Edge-driven Polarity independently selected via the External Interrupt Polarity Register bits (EXTPOL[3:0]) |
| GP[7](EXT_INT7) | E3 | I/O/Z | IPU | |
| GP[6](EXT_INT6) | D2 | I/O/Z | IPU | GP[4] and GP[5] pins also function as AMUTEIN1 McASP1 mute input and AMUTEIN0 McASP0 mute input, respectively, if enabled by the INEN bit in the associated McASP AMUTE register. |
| GP[5](EXT_INT5)/AMUTEIN0 | C1 | I/O/Z | IPU | |
| GP[4](EXT_INT4)/AMUTEIN1 | C2 | I/O/Z | IPU | Host-port data pin 7 (I/O/Z) [default] or general-purpose input/output pin 3 (I/O/Z) |
| HD7/GP[3] | A18 | I/O/Z | IPU | |
| CLKOUT2/GP[2] | Y12 | I/O/Z | IPD | Clock output at half of device speed (O/Z) [default] or this pin can be programmed as GP[2] pin |
| HINT/GP[1] | J20 | O | IPU | Host interrupt (from DSP to host) (O) [default] or this pin can be programmed as a GP[1] pin (I/O/Z) |
| HD4/GP[0] | C19 | I/O/Z | IPD | Host-port data pin 4 (I/O/Z) [default] or this pin can be programmed as a GP[0] pin (I/O/Z) |
| RESERVED FOR TEST | | | | |
| RSV | A5 | O/Z | IPU | Reserved. (Leave unconnected; do not connect to power or ground.) |
| RSV | B5 | A ⁽⁶⁾ | — | Reserved. (Leave unconnected; do not connect to power or ground.) |
| RSV | C12 | O | — | Reserved. (Leave unconnected; do not connect to power or ground.) |
| RSV | D7 | O/Z | IPD | Reserved. (Leave unconnected; do not connect to power or ground.) |
| RSV | D12 | I | — | Reserved. This pin does not have an IPU. For proper C6713 device operation, the D12 pin <i>must</i> be externally pulled down with a 10-kΩ resistor. |
| RSV | A12 | — | — | Reserved. For new designs, it is recommended that this pin be connected directly to CV _{DD} (core power). For old designs, this can be left unconnected. |
| RSV | B11 | — | — | Reserved. For new designs, it is recommended that this pin be connected directly to V _{SS} (ground). For old designs, this pin can be left unconnected. |
| SUPPLY VOLTAGE PINS | | | | |
| DV _{DD} | A17 B3 B8 B13 C10 D1 D16 D19 F3 H18 J2 M18 R1 R18 T3 U5 U7 U12 U16 V13 V15 V19 W3 W9 W12 Y7 Y17 | S | — | 3.3-V supply voltage (see the Power-Supply Decoupling section of this data sheet) |

(6) A = Analog signal

TERMINAL FUNCTIONS (continued)

| SIGNAL NAME | PIN NO. | TYPE ⁽¹⁾ | IPD/IPU ⁽²⁾ | DESCRIPTION |
|------------------|---------|---------------------|------------------------|---|
| | GDP | | | |
| CV _{DD} | A4 | S | — | 1.26-V supply voltage (see the Power-Supply Decoupling section of this data sheet) |
| | A9 | | | |
| | A10 | | | |
| | B2 | | | |
| | B19 | | | |
| | C3 | | | |
| | C7 | | | |
| | C18 | | | |
| | D5 | | | |
| | D6 | | | |
| | D11 | | | |
| | D14 | | | |
| | D15 | | | |
| | F4 | | | |
| | F17 | | | |
| | K1 | | | |
| | K4 | | | |
| | K17 | | | |
| | L4 | | | |
| | L17 | | | |
| L20 | | | | |
| R4 | | | | |
| R17 | | | | |
| U6 | | | | |
| U10 | | | | |
| U11 | | | | |
| U14 | | | | |
| U15 | | | | |
| V3 | | | | |
| V18 | | | | |
| W2 | | | | |
| W19 | | | | |

TERMINAL FUNCTIONS (continued)

| SIGNAL NAME | PIN NO. | TYPE ⁽¹⁾ | IPD/IPU ⁽²⁾ | DESCRIPTION |
|-----------------|---|---------------------|------------------------|---|
| | GDP | | | |
| GROUND PINS | | | | |
| V _{SS} | A1 A2 A11 A14 A19 A20 B1 B4 B15 B20 C6 C8 C9 D4 D8 D13 D17 E2 E4 E17 F19 G4 G17 H4 H17 J4 J9 J10 J11 J12 K2 K9 K10 K11 K12 K20 L9 L10 L11 L12 M4 M9 M10 M11 M12 M17 N4 N17 P4 P17 P19 T4 T17 U4 U8 U9 U13 U17 U20 W1 W5 W11 W16 W20 Y1 Y2 Y13 Y19 Y20 | GND | — | Ground pins ⁽¹⁾ . The center thermal balls (J9–J12, K9–K12, L9–L12, M9–M12) [shaded] are all tied to ground and act as both electrical grounds and thermal relief (thermal dissipation). |

(1) Shaded pin numbers denote the center thermal balls.

6.1 Development Support

TI offers an extensive line of development tools for the TMS320C6000™ DSP platform, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules.

The following products support development of C6000™ DSP-based applications:

Software Development Tools

- Code Composer Studio™ Integrated Development Environment (IDE), including Editor
- C/C++/Assembly Code Generation, and Debug plus additional development tools
- Scalable, Real-Time Foundation Software (DSP/BIOS™), which provides the basic run-time target software needed to support any DSP application.

Hardware Development Tools

- Extended Development System (XDS™) Emulator (supports C6000 DSP multiprocessor system debug)
- EVM (evaluation module)

For a complete listing of development-support tools for the TMS320C6000 DSP platform, visit the Texas Instruments web site at www.ti.com. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

6.2 Device and Development-Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all TMS320™ DSP devices and support tools. Each TMS320 DSP commercial family member has one of three prefixes: SMX, TMP, or SM/SMJ. TI recommends two of three possible prefix designators for support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (SMX/TMDX) through fully qualified production devices/tools (SM/SMJ/TMDS).

6.2.1 Device Development Evolutionary Flow

| | |
|---------------|--|
| SMX | Preproduction device that is not necessarily representative of the final device electrical specifications |
| TMP | Final silicon die that conforms to the device electrical specifications but has not completed quality and reliability verification |
| SM/SMJ | Fully qualified production device |

6.2.2 Support Tool Development Evolutionary Flow

| | |
|-------------|---|
| TMDX | Development-support product that has not yet completed Texas Instruments internal qualification testing |
| TMDS | Fully qualified development-support product |

SMX and TMP devices and TMDX development-support tools are shipped with appropriate disclaimers describing their limitations and intended uses. Experimental devices (SMX) may not be representative of a final product and TI reserves the right to change or discontinue these products without notice.

SM/SMJ devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (SMX or TMP) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, **GDP**), the temperature range (for example, blank is the default commercial temperature range), and the device speed range in megahertz (for example, 20 is 200 MHz).

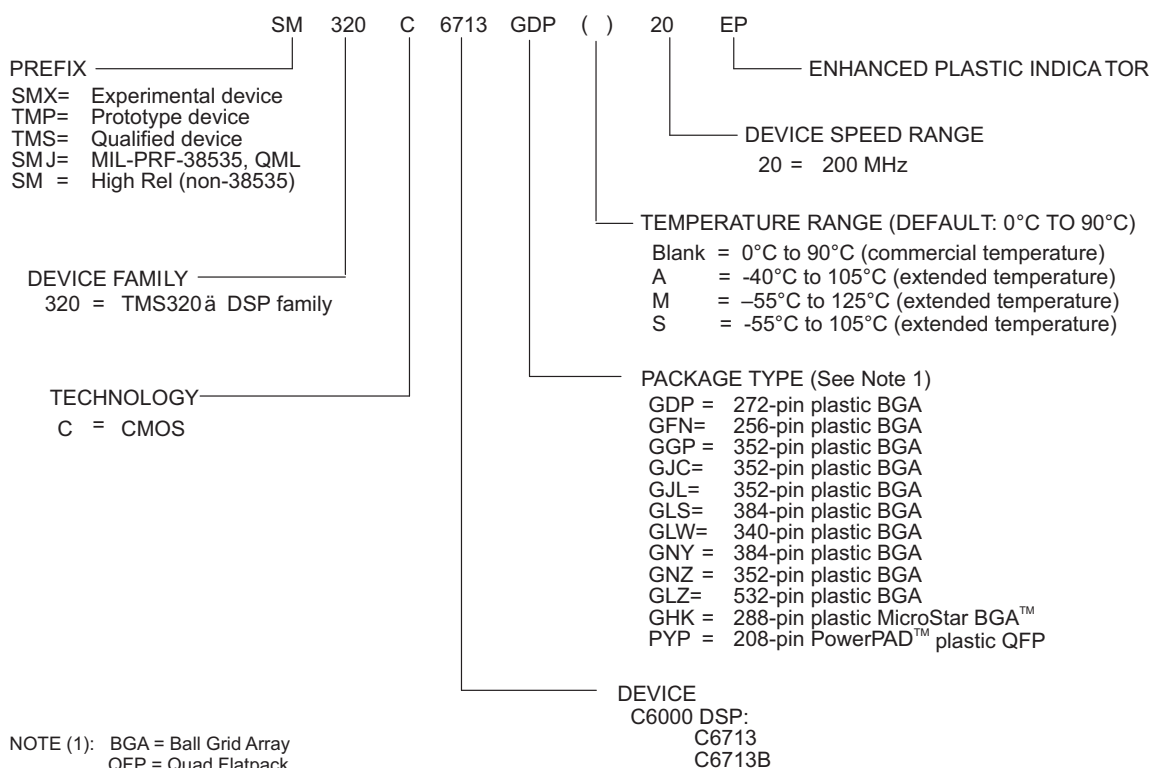
Figure 6-1 provides a legend for reading the complete device name for any TMS320C6000 DSP family member.

Table 6-1. 320C6713 and C6713B Device Part Numbers (P/Ns) and Ordering Information⁽¹⁾

| DEVICE ORDERABLE P/N ⁽²⁾ | DEVICE SPEED | CORE AND I/O VOLTAGE | | OPERATING CASE TEMPERATURE RANGE |
|-------------------------------------|---------------------|-------------------------|------------------------|----------------------------------|
| | | CV _{DD} (CORE) | DV _{DD} (I/O) | |
| C6713B | | | | |
| SM32C6713BGDPA20EP | 200 MHz/1200 MFlops | 1.26 V | 3.3 V | –40°C to 105°C |
| SM32C6713BGDPM30EP | 300 MHz/1800 MFlops | 1.4V | 3.3V | –55°C to 125°C |
| SM32C6713BGDPS20EP | 200 MHz/1200 MFlops | 1.26 V | 3.3 V | –55°C to 105°C |

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
- (2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package

6.3 Ordering Nomenclature



NOTE (1): BGA = Ball Grid Array
QFP = Quad Flatpack

For actual device part numbers (P/Ns) and ordering information, see the Mechanical Data section of this document or the TI website (www.ti.com).

Figure 6-1. TMS320C6000™ DSP Device Nomenclature (Including SM320C6713 and C6713B Devices)

6.4 Documentation Support

Extensive documentation supports all the TMS320 DSP family generations of devices from product announcement through applications development. The types of documentation available include data sheets, such as this document with design specifications complete user's reference guides for all devices and tools, technical briefs, development-support tools, on-line help, and hardware and software applications. The following is a brief, descriptive list of support documentation specific to the C6000 DSP devices, except where noted, all documents are accessible through the TI web site at www.ti.com.

- *TMS320C6000™ CPU and Instruction Set Reference Guide* (literature number [SPRU189](#)) describes the C6000 CPU (DSP core) architecture, instruction set, pipeline, and associated interrupts.

- *TMS320C6000™ DSP Peripherals Overview Reference Guide* [hereafter referred to as the *C6000 PRG Overview*] (literature number [SPRU190](#)) provides an overview and briefly describes the functionality of the peripherals available on the C6000 DSP platform of devices. This document also includes a table listing the peripherals available on the C6000 devices along with literature numbers and hyperlinks to the associated peripheral documents. These C6713/13B peripherals are similar to the peripherals on the TMS320C6711 and TMS320C64x devices; therefore, see the TMS320C6711 (C6711 or C67x) peripheral information and, in some cases (where indicated), see the TMS320C6711 (C6711 or C671x) peripheral information and, in some cases (where indicated), see the C64x information in the *C6000™ PRG Overview* (literature number [SPRU190](#)).
- *TMS320DA6000™ DSP Multichannel Audio Serial Port (McASP) Reference Guide* (literature number [SPRU041](#)) describes the functionality of the McASP peripherals available on the C6713/13B device.
- *TMS320C6000™ DSP Software-Programmable Phase-Locked Loop (PLL) Controller Reference Guide* (literature number [SPRU233](#)) describes the functionality of the PLL peripheral available on the C6713/13B device.
- *TMS320C6000™ DSP Inter-Integrated Circuit (I²C) Module Reference Guide* (literature number [SPRU175](#)) describes the functionality of the I²C peripherals available on the C6713/13B device.
- *The PowerPAD™ Thermally-Enhanced Package Technical Brief* (literature number [SLMA002](#)) focuses on the specifics of integrating a PowerPAD package into the printed circuit board (PCB) design to make optimum use of the thermal efficiencies designed into the PowerPAD package.
- *TMS320C6000™ Technical Brief* (literature number [SPRU197](#)) gives an introduction to the C62x™/C67x™ devices, associated development tools, and third-party support.
- *Migrating from TMS320C6211(B)/C6711(B) to TMS320C6713* application report (literature number [SPRA851](#)) indicates the differences and describes the issues of interest related to the migration from the TI TMS320C6211(B)/C6711(B) GFN package to the TMS320C6713 GDP package.
- *TMS320C6713, TMS320C6713B Digital Signal Processors Silicon Errata* (literature number [SPRZ191](#)) describes the known exceptions to the functional specifications for particular silicon revisions of the TMS320C6713 and TMS320C6713B devices.
- *TMS320C6713/12C/11C Power Consumption Summary* application report (literature number [SPRA889](#)) discusses the power consumption for user applications with the TMS320C6713/13B, TMS320C6712C/12D, and TMS320C6711C/11D DSP devices.
- *Using IBIS Models for Timing Analysis* application report (literature number [SPRA839](#)) describes how to properly use IBIS models to attain accurate timing analysis for a given system.

The tools support documentation is electronically available within the Code Composer Studio Integrated Development Environment (IDE). For a complete listing of C6000 DSP latest documentation, visit the Texas Instruments web site at [www.ti.com](#). Also, see the TI web site for the application report, *How To Begin Development Today With the TMS320C6713 Floating-Point DSP* (literature number [SPRA809](#)), which describes in more detail the similarities/differences between the C6713 and C6711 C6000 DSP devices.

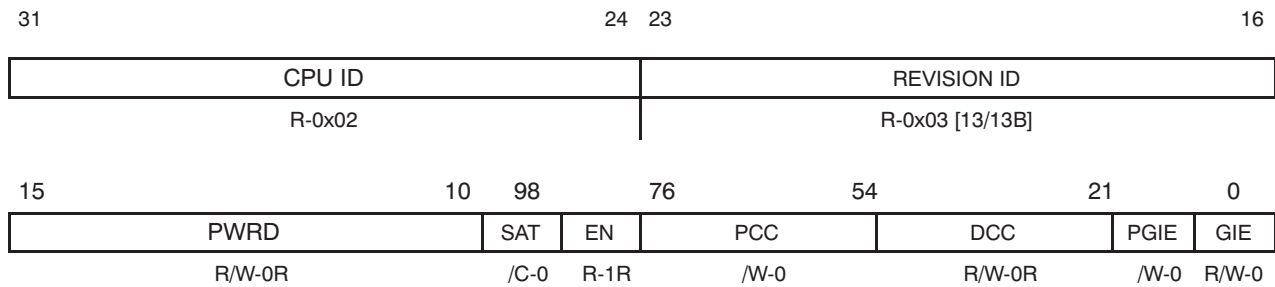
7 REGISTER INFORMATION

This section provides the register information for the device.

7.1 CPU Control Status Register (CSR) Description

The CPU CSR contains the CPU ID and CPU Revision ID (bits 16–31), as well as the status of the device power-down modes [PWRD field (bits 15–10)], program and data cache control modes, the endian bit (EN, bit 8), and the global interrupt enable (GIE, bit 0) and previous GIE (PGIE, bit 1). [Figure 7-1](#) and [Table 7-1](#) identify the bit fields in the CPU CSR.

For more detailed information on the bit fields in the CPU CSR, see the *TMS320C6000 DSP Peripherals Overview Reference Guide* (literature number [SPRU190](#)) and the *TMS320C6000 CPU and Instruction Set Reference Guide* (literature number [SPRU189](#)).



Legend: R = Readable by the MVC instruction, R/W = Readable/Writeable by the MVC instruction; W = Read/write; -n = value after reset, -x = undefined value after reset, C = Clearable by the MVC instruction

Figure 7-1. CPU Control Status Register (CPU CSR)

Table 7-1. CPU CSR Bit Field Description

| Bit NO. | NAME | DESCRIPTION |
|---------|-------------|--|
| 31:24 | CPU ID | CPU ID + REV ID. Read only. Identifies which CPU is used and defines the silicon revision of the CPU. CPU ID + REVISION ID (31:16) are combined for a value of: 0x0203 for C6713/13B |
| 23:16 | REVISION ID | |
| 15:10 | PWRD | Control power-down modes. The values are always read as zero. 000000 = No power down (default) 001001 = PD1, wake up by an enabled interrupt 010001 = PD1, wake up by an enabled or not enabled interrupt 011010 = PD2, wake up by a device reset 011100 = PD3, wake up by a device reset Others = Reserved |
| 9 | SAT | Saturate bit. Set when any unit performs a saturate. This bit can be cleared only by the MVC instruction and can be set only by a functional unit. The set by the a functional unit has priority over a clear (by the MVC instruction) if they occur on the same cycle. The saturate bit is set one full cycle (one delay slot) after a saturate occurs. This bit will not be modified by a conditional instruction whose condition is false. |
| 8 | EN | Endian bit. This bit is read-only. Depicts the device endian mode. 0 = Big Endian mode 1 = Little Endian mode [default] |
| 7:5 | PCC | Program cache control mode. L1D, Level 1 program cache 000/010 = Cache enabled/cache accessed and updated on reads All other PCC values are reserved. |
| 4:2 | DCC | Data cache control mode. L1D, Level 1 data cache 000/010 = Cache enabled/2-way cache All other DCC values are reserved. |
| 1 | PGIE | Previous GIE (global interrupt enable); saves the Global Interrupt Enable (GIE) when an interrupt is taken. Allows for proper nesting of interrupts. 0 = Previous GIE value is 0 (default). 1 = Previous GIE value is 1. |
| 0 | GIE | Global interrupt enable bit. Enables (1) or disables (0) all interrupts except the reset interrupt and NMI (nonmaskable interrupt). 0 = Disables all interrupts (except the reset interrupt and NMI) [default]. 1 = Enables all interrupts (except the reset interrupt and NMI). |

7.2 Cache Configuration (CCFG) Register Description (13B)

The C6713B device includes an enhancement to the CCFG register. A P bit (CCFG.31) allows the programmer to select the priority of accesses to L2 memory originating from the transfer crossbar (TC) over accesses originating from the L1D memory system. An important class of TC accesses is EDMA transfers, which move data to or from the L2 memory. While the EDMA normally has no issue accessing L2 memory because of the high hit rates on the L1D memory system, there are pathological cases where certain CPU behavior could block the EDMA from accessing the L2 memory for long enough to cause a missed deadline when transferring data to a peripheral such as the McASP or McBSP. This can be avoided by setting the P bit to 1 because the EDMA will assume a higher priority than the L1D memory system when accessing L2 memory.

For more detailed information on the P-bit function and for silicon advisories concerning EDMA L2 memory accesses blocked, see the *TMS320C6713, TMS320C6713B Digital Signal Processors Silicon Errata* (literature number [SPRZ191](#)).

| | | | | | | | | | | |
|------------------|----------|--|----|----|--|-----|-----|----------|---|---------|
| 31 | 30 | | 10 | 98 | | 7 | | 32 | 0 | |
| P ⁽¹⁾ | Reserved | | | | | IP | ID | Reserved | | L2MODE |
| R/W-0 | R-x | | | | | W-0 | W-0 | R-0 0000 | | R/W-000 |

Legend: R = Readable; R/W = Readable/Writeable; -n = value after reset, -x = undefined value after reset

A: Unlike the C6713 device, the C6713B device includes a P bit.

A. Unlike the C6713 device, the C6713B device includes a P bit.

Figure 7-2. Cache Configuration (CCFG) Register

Table 7-2. CCFG Register Bit Field Description

| BIT NO. | NAME | DESCRIPTION |
|---------|----------|---|
| 31 | P | L1D requestor priority to L2 bit P = 0: L1D requests to L2 higher priority than TC requests P = 1: TC requests to L2 higher priority than L1D requests |
| 30:10 | Reserved | Reserved. Read only, writes have no effect. |
| 9 | IP | Invalidate L1P bit 0 = Normal L1P operation 1 = All L1P lines are invalidated |
| 8 | ID | Invalidate L1D bit 0 = Normal L1D operation 1 = All L1D lines are invalidated |
| 7:3 | Reserved | Reserved. Read only, writes have no effect. |
| 2:0 | L2MODE | L2 operation mode bits (L2MODE) 000b = L2 cache disabled (All SRAM mode) [256K SRAM] 001b = 1-way cache (16K L2 cache) / [240K SRAM] 010b = 2-way cache (32K L2 cache) / [224K SRAM] 011b = 3-way cache (48K L2 cache) / [208K SRAM] 111b = 4-way cache (64K L2 cache) / [192K SRAM] All others are reserved. |

7.3 Interrupts and Interrupt Selector

The C67x DSP core supports 16 prioritized interrupts, which are listed in [Table 7-3](#). The highest priority interrupt is INT_00 (dedicated to RESET), while the lowest priority is INT_15. The first four interrupts are non-maskable and fixed. The remaining interrupts (4–15) are maskable and default to the interrupt source listed in [Table 7-3](#). However, their interrupt source may be reprogrammed to any one of the sources listed in [Table 7-4](#) (Interrupt Selector). [Table 7-4](#) lists the selector value corresponding to each of the alternate interrupt sources. The selector choice for interrupts 4–15 is made by programming the corresponding fields (listed in [Table 7-3](#)) in the MUXH (address 0x019C0000) and MUXL (address 0x019C0004) registers.

Table 7-3. DSP Interrupts

| DSP INTERRUPT NUMBER | INTERRUPT SELECTOR CONTROL REGISTER | DEFAULT SELECTOR VALUE (BINARY) | DEFAULT INTERRUPT EVENT |
|----------------------|-------------------------------------|---------------------------------|-------------------------|
| INT_00 | — | — | RESET |
| INT_01 | — | — | NMI |
| INT_02 | — | — | Reserved |
| INT_03 | — | — | Reserved |

Table 7-3. DSP Interrupts (continued)

| DSP INTERRUPT NUMBER | INTERRUPT SELECTOR CONTROL REGISTER | DEFAULT SELECTOR VALUE (BINARY) | DEFAULT INTERRUPT EVENT |
|----------------------|-------------------------------------|---------------------------------|-------------------------|
| INT_04 | MUXL[4:0] | 00100 | GPINT4 ⁽¹⁾ |
| INT_05 | MUXL[9:5] | 00101 | GPINT5 ⁽¹⁾ |
| INT_06 | MUXL[14:10] | 00110 | GPINT6 ⁽¹⁾ |
| INT_07 | MUXL[20:16] | 00111 | GPINT7 ⁽¹⁾ |
| INT_08 | MUXL[25:21] | 01000 | EDMAINT |
| INT_09 | MUXL[30:26] | 01001 | EMUDDDMA |
| INT_10 | MUXH[4:0] | 00011 | SDINT |
| INT_11 | MUXH[9:5] | 01010 | EMURTDXR |
| INT_12 | MUXH[14:10] | 01011 | EMURTDXTX |
| INT_13 | MUXH[20:16] | 00000 | DSPINT |
| INT_14 | MUXH[25:21] | 00001 | TINT0 |
| INT_15 | MUXH[30:26] | 00010 | TINT1 |

(1) Interrupt events GPINT4, GPINT5, GPINT6, and GPINT7 are outputs from the GPIO module (GP). They originate from the device pins GP[4](EXT_INT4)/AMUTEIN1, GP[5](EXT_INT5)/AMUTEINO, GP[6](EXT_INT6), and GP[7](EXT_INT7). These pins can be used as edge-sensitive EXT_INTx with polarity controlled by the External Interrupt Polarity Register (EXTPOL.[3:0]). The corresponding pins must first be enabled in the GPIO module by setting the corresponding enable bits in the GP Enable Register (GPEN.[7:4]), and configuring them as inputs in the GP Direction Register (GPDIR.[7:4]). These interrupts can be controlled through the GPIO module in addition to the simple EXPOL.[3:0] bits. For more information on interrupt control via the GPIO module, see the *TMS320C6000™ DSP General-Purpose Input/Output (GPIO) Reference Guide* (literature number [SPRU584](#)).

Table 7-4. Interrupt Selector

| INTERRUPT SELECTOR VALUE (BINARY) | INTERRUPT EVENT | MODULE |
|--------------------------------------|-----------------------|-----------|
| 00000 | DSPINT | HPI |
| 00001 | TINT0 | Timer 0 |
| 00010 | TINT1 | Timer 1 |
| 00011 | SDINT | EMIF |
| 00100 | GPINT4 ⁽¹⁾ | GPIO |
| 00101 | GPINT5 ⁽¹⁾ | GPIO |
| 00110 | GPINT6 ⁽¹⁾ | GPIO |
| 00111 | GPINT7 ⁽¹⁾ | GPIO |
| 01000 | EDMAINT | EDMA |
| 01001 | EMUDDDMA | Emulation |
| 01010 | EMURTDXR | Emulation |
| 01011 | EMURTDXTX | Emulation |
| 01100 | XINT0 | McBSP0 |
| 01101 | RINT0 | McBSP0 |
| 01110 | XINT1 | McBSP1 |
| 01111 | RINT1 | McBSP1 |
| 10000 | GPINT0 | GPIO |
| 10001 | Reserved | — |
| 10010 | Reserved | — |
| 10011 | Reserved | — |
| 10100 | Reserved | — |
| 10101 | Reserved | — |
| 10110 | I2CINT0 | I2C0 |
| 10111 | I2CINT1 | I2C1 |
| 11000 | Reserved | — |
| 11001 | Reserved | — |
| 11010 | Reserved | — |
| 11011 | Reserved | — |
| 11100 | AXINT0 | McASP0 |
| 11101 | ARINT0 | McASP0 |
| 11110 | AXINT1 | McASP1 |
| 11111 | ARINT1 | McASP1 |

(1) Interrupt events GPINT4, GPINT5, GPINT6, and GPINT7 are outputs from the GPIO module (GP). They originate from the device pins GP[4](EXT_INT4)/AMUTEIN1, GP[5](EXT_INT5)/AMUTEIN0, GP[6](EXT_INT6), and GP[7](EXT_INT7). These pins can be used as edge-sensitive EXT_INTx with polarity controlled by the External Interrupt Polarity Register (EXTPOL.[3:0]). The corresponding pins must first be enabled in the GPIO module by setting the corresponding enable bits in the GP Enable Register (GPEN.[7:4]), and configuring them as inputs in the GP Direction Register (GPDIR.[7:4]). These interrupts can be controlled through the GPIO module in addition to the simple EXTPOL.[3:0] bits. For more information on interrupt control via the GPIO module, see the *TMS320C6000™ DSP General-Purpose Input/Output (GPIO) Reference Guide* (literature number [SPRU584](#)).

7.4 External Interrupt Sources

The C6713/13B device supports many external interrupt sources as indicated in [Table 7-5](#). Control of the interrupt source is done by the associated module and is made available by enabling the corresponding binary interrupt selector value (see [Table 7-4](#) shaded rows). Because of pin multiplexing and module usage, not all external interrupt sources are available at the same time.

Table 7-5. External Interrupt Sources and Peripheral Module Control

| PIN NAME | INTERRUPT EVENT | MODULE |
|----------|------------------|--------|
| GP[15] | GPINT0 | GPIO |
| GP[14] | GPINT0 | GPIO |
| GP[13] | GPINT0 | GPIO |
| GP[12] | GPINT0 | GPIO |
| GP[11] | GPINT0 | GPIO |
| GP[10] | GPINT0 | GPIO |
| GP[9] | GPINT0 | GPIO |
| GP[8] | GPINT0 | GPIO |
| GP[7] | GPINT0 or GPINT7 | GPIO |
| GP[6] | GPINT0 or GPINT6 | GPIO |
| GP[5] | GPINT0 or GPINT5 | GPIO |
| GP[4] | GPINT0 or GPINT4 | GPIO |
| GP[3] | GPINT0 | GPIO |
| GP[2] | GPINT0 | GPIO |
| GP[1] | GPINT0 | GPIO |
| GP[0] | GPINT0 | GPIO |

7.5 EDMA Module and EDMA Selector

The C67x EDMA supports up to 16 EDMA channels. Four of the 16 channels (channels 8–11) are reserved for EDMA chaining, leaving 12 EDMA channels available to service peripheral devices.

The EDMA selector registers that control the EDMA channels servicing peripheral devices are located at addresses 0x01A0FF00 (ESEL0), 0x01A0FF04 (ESEL1), and 0x01A0FF0C (ESEL3). These EDMA selector registers control the mapping of the EDMA events to the EDMA channels. Each EDMA event has an assigned EDMA selector code (see [Table 7-7](#)). By loading each EVTSELx register field with an EDMA selector code, users can map any desired EDMA event to any specified EDMA channel. [Table 7-6](#) lists the default EDMA selector value for each EDMA channel.

See [Table 7-8](#) and [Table 7-11](#) for the EDMA Event Selector registers and their associated bit descriptions.

Table 7-6. EDMA Channels

| EDMA CHANNEL | EDMA SELECTOR CONTROL REGISTER | DEFAULT SELECTOR VALUE (BINARY) | DEFAULT EDMA EVENT |
|--------------|--------------------------------|---------------------------------|--------------------|
| 0 | ESEL0[5:0] | 000000 | DSPINT |
| 1 | ESEL0[13:8] | 000001 | TINT0 |
| 2 | ESEL0[21:16] | 000010 | TINT1 |
| 3 | ESEL0[29:24] | 000011 | SDINT |
| 4 | ESEL1[5:0] | 000100 | GPINT4 |
| 5 | ESEL1[13:8] | 000101 | GPINT5 |
| 6 | ESEL1[21:16] | 000110 | GPINT6 |
| 7 | ESEL1[29:24] | 000111 | GPINT7 |
| 8 | — | — | TCC8 (Chaining) |
| 9 | — | — | TCC9 (Chaining) |
| 10 | — | — | TCC10 (Chaining) |
| 11 | — | — | TCC11 (Chaining) |
| 12 | ESEL3[5:0] | 001100 | XEVT0 |
| 13 | ESEL3[13:8] | 001101 | REVT0 |
| 14 | ESEL3[21:16] | 001110 | XEVT1 |
| 15 | ESEL3[29:24] | 001111 | REVT1 |

Table 7-7. EDMA Selector

| EDMA SELECTOR CODE (BINARY) | EDMA EVENT | MODULE |
|-----------------------------|------------|--------|
| 000000 | DSPINT | HPI |
| 000001 | TINT0 | TIMER0 |
| 000010 | TINT1 | TIMER1 |
| 000011 | SDINT | EMIF |
| 000100 | GPINT4 | GPIO |
| 000101 | GPINT5 | GPIO |
| 000110 | GPINT6 | GPIO |
| 000111 | GPINT7 | GPIO |
| 001000 | GPINT0 | GPIO |
| 001001 | GPINT1 | GPIO |
| 001010 | GPINT2 | GPIO |
| 001011 | GPINT3 | GPIO |
| 001100 | XEVT0 | McBSP0 |
| 001101 | REVT0 | McBSP0 |
| 001110 | XEVT1 | McBSP1 |
| 001111 | REVT1 | McBSP1 |
| 010000–011111 | Reserved | |
| 100000 | AXEVTE0 | McASP0 |
| 100001 | AXEVTO0 | McASP0 |
| 100010 | AXEVT0 | McASP0 |
| 100011 | AREVTE0 | McASP0 |
| 100100 | AREVTO0 | McASP0 |
| 100101 | AREVT0 | McASP0 |
| 100110 | AXEVTE1 | McASP1 |
| 100111 | AXEVTO1 | McASP1 |
| 101000 | AXEVT1 | McASP1 |
| 101001 | AREVTE1 | McASP1 |
| 101010 | AREVTO1 | McASP1 |
| 101011 | AREVT1 | McASP1 |
| 101100 | I2CREVT0 | I2C0 |
| 101101 | I2CXEVT0 | I2C0 |
| 101110 | I2CREVT1 | I2C1 |
| 101111 | I2CXEVT1 | I2C1 |
| 110000 | GPINT8 | GPIO |
| 110001 | GPINT9 | GPIO |
| 110010 | GPINT10 | GPIO |
| 110011 | GPINT11 | GPIO |
| 110100 | GPINT12 | GPIO |
| 110101 | GPINT13 | GPIO |
| 110110 | GPINT14 | GPIO |
| 110111 | GPINT15 | GPIO |
| 111000–111111 | Reserved | |

Table 7-8. EDMA Event Selector Registers (ESEL0 Register (0x01A0 FF00))

| | | | | | | | | | | | |
|----------|----|--------------|----|----|----|----------|----|--------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 24 | 23 | 22 | 21 | 20 | 19 | 16 |
| Reserved | | EVTSEL3 | | | | Reserved | | EVTSEL2 | | | |
| R-0 | | R/W-00 0011b | | | | R-0 | | R/W-00 0010b | | | |
| 15 | 14 | 13 | 12 | 11 | 8 | 7 | 6 | 5 | 4 | 3 | 0 |
| Reserved | | EVTSEL1 | | | | Reserved | | EVTSEL0 | | | |
| R-0 | | R/W-00 0001b | | | | R-0 | | R/W-00 0000b | | | |

Legend: R = Read only, R/W = Read/write, -n = value at reset

Table 7-9. EDMA Event Selector Registers—ESEL1 Register (0x01A0 FF04)

| | | | | | | | | | | | |
|----------|----|--------------|----|----|----|----------|----|--------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 24 | 23 | 22 | 21 | 20 | 19 | 16 |
| Reserved | | EVTSEL7 | | | | Reserved | | EVTSEL6 | | | |
| R-0 | | R/W-00 0111b | | | | R-0 | | R/W-00 0110b | | | |
| 15 | 14 | 13 | 12 | 11 | 8 | 7 | 6 | 5 | 4 | 3 | 0 |
| Reserved | | EVTSEL5 | | | | Reserved | | EVTSEL4 | | | |
| R-0 | | R/W-00 0101b | | | | R-0 | | R/W-00 0100b | | | |

Legend: R = Read only, R/W = Read/write, -n = value at reset

Table 7-10. EDMA Event Selector Registers—ESEL3 Register (0x01A0 FF0C)

| | | | | | | | | | | | |
|----------|----|--------------|----|----|----|----------|----|--------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 24 | 23 | 22 | 21 | 20 | 19 | 16 |
| Reserved | | EVTSEL15 | | | | Reserved | | EVTSEL14 | | | |
| R-0 | | R/W-00 1111b | | | | R-0 | | R/W-00 1110b | | | |
| 15 | 14 | 13 | 12 | 11 | 8 | 7 | 6 | 5 | 4 | 3 | 0 |
| Reserved | | EVTSEL13 | | | | Reserved | | EVTSEL12 | | | |
| R-0 | | R/W-00 1101b | | | | R-0 | | R/W-00 1100b | | | |

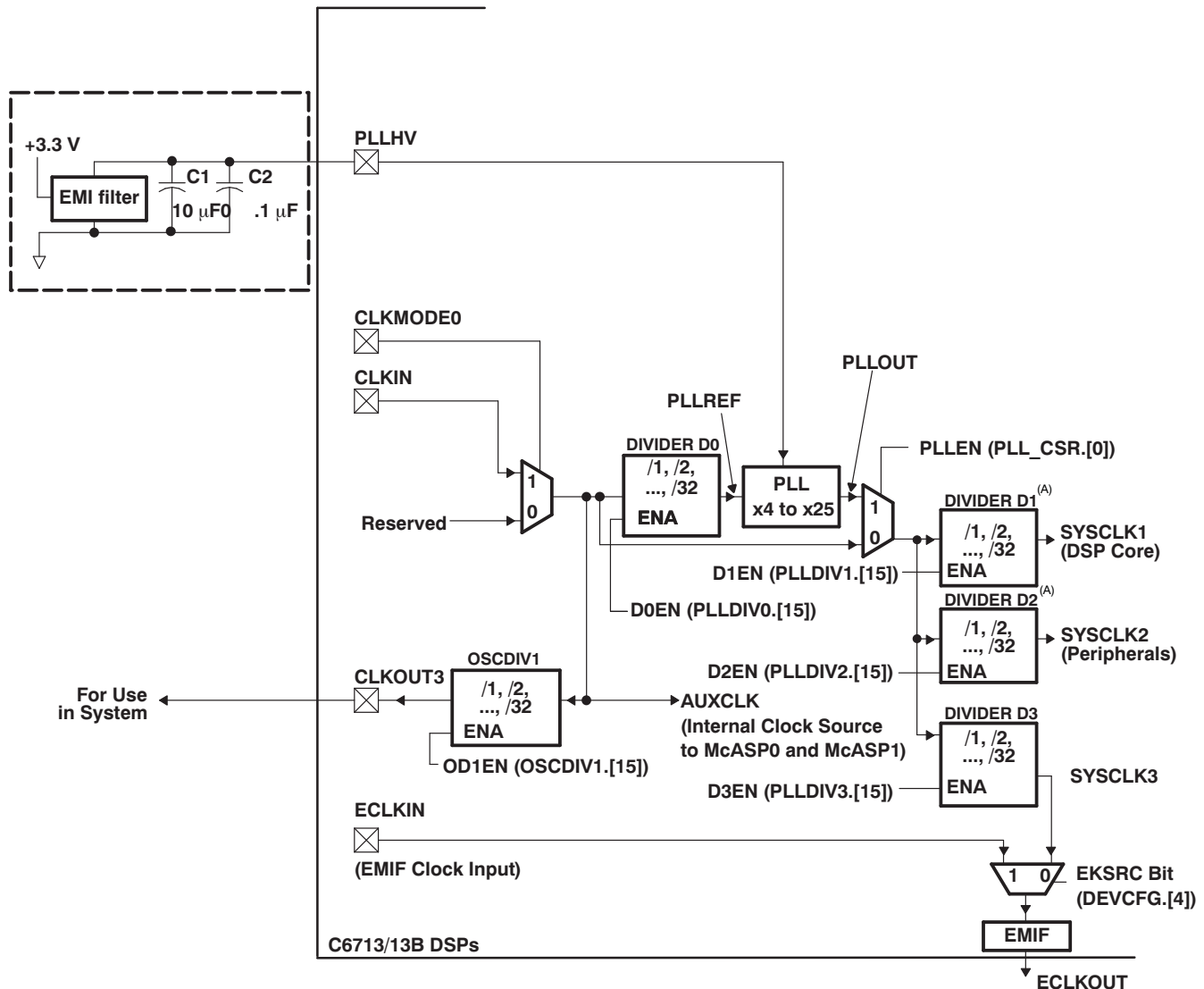
Legend: R = Read only, R/W = Read/write, -n = value at reset

Table 7-11. EDMA Event Selection Registers (ESEL0, ESEL1, and ESEL3) Description

| BIT NO. | NAME | DESCRIPTION |
|--------------------------------|----------|---|
| 31:30 23:22 15:14 7:6 | Reserved | Reserved. Read only, writes have no effect. |
| 29:24 21:16 13:8 5:0 | EVTSELx | EDMA event selection bits for channel x. Allows mapping of the EDMA events to the EDMA channels. The EVTSEL0 through EVTSEL15 bits correspond to channels 0 to 15, respectively. These EVTSELx fields are user selectable. By configuring the EVTSELx fields to the EDMA selector value of the desired EDMA sync event number (see Table 7-7), users can map any EDMA event to the EDMA channel. For example, if EVTSEL15 is programmed to 00 0001b (the EDMA selector code for TINT0), channel 15 is triggered by Timer 0 TINT0 events. |

8 PLL and PLL Controller

The 320C6713/13B includes a PLL and a flexible PLL controller peripheral consisting of a prescaler (D0) and four dividers (OSCDIV1, D1, D2, and D3). The PLL controller is able to generate different clocks for different parts of the system (that is, DSP core, peripheral data bus, external memory interface, McASP, and other peripherals). Figure 8-1 shows the PLL, the PLL controller, and the clock generator logic.



- Dividers D1 and D2 must never be disabled. Never write a '0' to the D1EN or D2EN bits in the PLLDIV1 and PLLDIV2 registers.
- Place all PLL external components (C1, C2, and the EMI filter) as close to the C67x DSP device as possible. For the best performance, TI recommends that all the PLL external components be on a single side of the board without jumpers, switches, or components other than the ones shown.
- For reduced PLL jitter, maximize the spacing between switching signals and the PLL external components (C1, C2, and the EMI filter).
- The 3.3-V supply for the EMI filter must be from the same 3.3-V power plane supplying the I/O voltage, DV_{DD} .
- EMI filter manufacturer TDK part number ACF451832-333, -223, -153, -103. Panasonic part number EXCCET103U.

Figure 8-1. PLL and Clock Generator Logic

8.1 PLL Registers

The PLL reset time is the amount of wait time needed when resetting the PLL (writing PLLRST = 1), for the PLL to properly reset, before bringing the PLL out of reset (writing PLLRST = 0). For the PLL reset time value, see [Table 8-1](#). The PLL lock time is the amount of time from when PLLRST = 0 with PLEN = 0 (PLL out of reset, but still bypassed) to when the PLEN bit can be safely changed to 1 (switching from bypass to the PLL path); see [Table 8-1](#) and [Figure 8-1](#).

Under some operating conditions, the maximum PLL lock time may vary from the specified typical value. For the PLL lock time values, see [Table 8-1](#).

Table 8-1. PLL Lock and Reset Times

| | MIN | TYP | MAX | UNIT |
|----------------|-----|-----|-------|------|
| PLL lock time | | 75 | 187.5 | μs |
| PLL reset time | 125 | | | ns |

[Table 8-2](#) shows the C6713/13B device CLKOUT signals, how and by what register control bits they are derived, and what is the default settings. For more details on the PLL, see the PLL and Clock Generator Logic diagram ([Figure 8-1](#)).

Table 8-2. CLKOUT Signals, Default Settings, and Control

| CLOCK OUTPUT SIGNAL NAME | DEFAULT SETTING (ENABLED or DISABLED) | CONTROL BIT(s) (Register) | DESCRIPTION |
|--------------------------|---------------------------------------|--|---|
| CLKOUT2 | ON (ENABLED) | D2EN = 1 (PLLDIV2.[15]) CK2EN = 1 (EMIF GBLCTL.[3]) | SYSCLK2 selected [default] |
| CLKOUT3 | ON (ENABLED) | OD1EN = 1 (OSCDIV1.[15]) | Derived from CLKIN |
| ECLKOUT | ON (ENABLED); derived from SYSCLK3 | EKSRC = 0 (DEVCFG.[4]) EKEN = 1 (EMIF GBLCTL.[5]) | SYSCLK3 selected [default]. To select ECLKIN source: EKSRC = 1 (DEVCFG.[4]) and EKEN = 1 (EMIF GBLCTL.[5]) |

The input clock (CLKIN) is directly available to the McASP modules as AUXCLK for use as an internal high-frequency clock source. The input clock (CLKIN) may also be divided down by a programmable divider OSCDIV1 (/1, /2, /3, ..., /32) and output on the CLKOUT3 pin for other use in the system.

[Figure 8-1](#) shows that the input clock source may be divided down by divider PLLDIV0 (/1, /2, ..., /32) and then multiplied up by a factor of x4, x5, x6, and so on, up to x25.

Either the input clock (PLEN = 0) or the PLL output (PLEN = 1) then serves as the high-frequency reference clock for the rest of the DSP system. The DSP core clock, the peripheral bus clock, and the EMIF clock may be divided down from this high-frequency clock (each with a unique divider). For example, with a 30-MHz input if the PLL output is configured for 450 MHz, the DSP core may be operated at 225 MHz (/2), while the EMIF may be configured to operate at a rate of 75 MHz (/6). Note that there is a specific minimum and maximum reference clock (PLLREF) and output clock (PLLOUT) for the block labeled PLL in [Figure 8-1](#), as well as for the DSP core, peripheral bus, and EMIF. The clock generator must not be configured to exceed any of these constraints (certain combinations of external clock input, internal dividers, and PLL multiply ratios might not be supported). See [Table 8-3](#) for the PLL clocks input and output frequency ranges.

Table 8-3. PLL Clock Frequency Ranges^{(1) (2)}

| CLOCK SIGNAL | MIN | MAX | UNIT |
|--------------------|-----|-------------------------|------|
| PLLREF (PLLEN = 1) | 12 | 100 | MHz |
| PLLOUT | 140 | 600 | MHz |
| SYCLK1 | — | Device speed (DSP core) | MHz |
| SYCLK3 (EKSRC = 0) | — | 100 | MHz |
| AUXCLK | — | 50 ⁽³⁾ | MHz |

- (1) SYCLK2 rate **must** be exactly half of SYCLK1.
- (2) See also the Electrical Specification (timing requirements and switching characteristics parameters) in the [Input and Output Clocks](#) section of this data sheet.
- (3) When the McASP module is *not* used, the AUXCLK maximum frequency can be any frequency up to the CLKIN maximum frequency.

The EMIF itself may be clocked by an external reference clock via the ECLKIN pin or can be generated on-chip as SYCLK3. SYCLK3 is derived from divider D3 off of PLLOUT (see [Figure 8-1](#)). The EMIF clock selection is programmable via the EKSRC bit in the DEVCFG register.

The settings for the PLL multiplier and each of the dividers in the clock generation block may be reconfigured via software at run time. If either the input to the PLL changes due to D0, CLKMODE0, or CLKIN, or if the PLL multiplier is changed, then software must enter bypass first and stay in bypass until the PLL has had enough time to lock (see electrical specifications). For the programming procedure, see the *TMS320C6000™ DSP Software-Programmable Phase-Locked Loop (PLL) Controller Reference Guide* (literature number [SPRU233](#)).

SYCLK2 is the internal clock source for peripheral bus control. SYCLK2 (Divider D2) **must** be programmed to be half of the SYCLK1 rate. For example, if D1 is configured to divide-by-2 mode (/2), then D2 **must** be programmed to divide-by-4 mode (/4). SYCLK2 is also tied directly to CLKOUT2 pin (see [Figure 8-1](#)).

During the programming transition of Divider D1 and Divider D2 (resulting in SYCLK1 and SYCLK2 output clocks, see [Figure 8-1](#)), the order of programming the PLLDIV1 and PLLDIV2 registers must be observed to ensure that SYCLK2 always runs at half the SYCLK1 rate or slower. For example, if the divider ratios of D1 and D2 are to be changed from /1, /2 (respectively) to /5, /10 (respectively) then, the PLLDIV2 register must be programmed before the PLLDIV1 register. The transition ratios become /1, /2; /1, /10; and then /5, /10. If the divider ratios of D1 and D2 are to be changed from /3, /6 to /1, /2, then the PLLDIV1 register must be programmed before the PLLDIV2 register. The transition ratios, for this case, become /3, /6; /1, /6; and then /1, /2. The final SYCLK2 rate **must** be exactly half of the SYCLK1 rate.

Note that Divider D1 and Divider D2 must **always** be enabled (that is, D1EN and D2EN bits are set to 1 in the PLLDIV1 and PLLDIV2 registers).

The PLL Controller registers should be modified only by the CPU or via emulation. The HPI should **not** be used to directly access the PLL Controller registers.

For detailed information on the clock generator (PLL Controller registers) and the associated software bit descriptions, see [Table 8-4](#) through [Table 8-11](#).

Table 8-4. PLL Control/Status Register (PLLCSR) (0x01B7 C100)

| | | | | | | | | | | | |
|----------|----|----|----|----|--------|----------|------------|--------------|-------------|-------|----|
| 31 | 28 | 27 | 24 | 23 | 20 | 19 | | | | | 16 |
| Reserved | | | | | | | | | | | |
| R-0 | | | | | | | | | | | |
| 15 | 12 | 11 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | | | | Stable | Reserved | PLLRS T | Reserv ed | PLLWRD N | PLLEN | |
| R-0 | | | | | R-x | R-0 | RW-1 | R/W-0 | R/W-0b | RW-0 | |

Legend: R = Read only, R/W = Read/write, -n = value at reset

Table 8-5. PLL Control/Status Register (PLLCSR) Description

| BIT NO. | NAME | DESCRIPTION |
|---------|----------|---|
| 31:7 | Reserved | Reserved. Read only, writes have no effect. |
| 6 | STABLE | Clock input stable. This bit indicates if the clock input has stabilized. 0: Clock input not yet stable. Clock counter is not finished counting (default). 1: Clock input stable |
| 5:4 | Reserved | Reserved. Read only, writes have no effect. |
| 3 | PLLRST | Asserts RESET to PLL 0: PLL reset released 1: PLL reset asserted (default) |
| 2 | Reserved | Reserved. The user <i>must</i> write a 0 to this bit. |
| 1 | PLLPWRDN | Select PLL power down 0: PLL operational (default) 1: PLL placed in power-down state |
| 0 | PLLEN | PLL mode enable 0: Bypass mode (default). PLL disabled Divider D0 and PLL are bypassed. SYSCLK1/SYSCLK2/SYSCLK3 are divided down directly from input reference clock. 1: PLL enabled Divider D0 and PLL are not bypassed. SYSCLK1/SYSCLK2/SYSCLK3 are divided down from PLL output. |

Table 8-6. PLL Multiplier (PLLM) Control Register (0x01B7 C110)

| | | | | | | | |
|----------|----|----|----|----|----|------------|----|
| 31 | 28 | 27 | 24 | 23 | 20 | 19 | 16 |
| Reserved | | | | | | | |
| R-0 | | | | | | | |
| 15 | 12 | 11 | 8 | 7 | 5 | 4 | 0 |
| Reserved | | | | | | PLLM | |
| R-0 | | | | | | R/W-0 0111 | |

Legend: R = Read only, R/W = Read/write, -n = value at reset

Table 8-7. PLL Multiplier (PLLM) Control Register Description

| BIT NO. | NAME | DESCRIPTION |
|---------|----------|--|
| 31:5 | Reserved | Reserved. Read only, writes have no effect. |
| 4:0 | PLLM | PLL multiply mode [default is x7 (0 0111)] 00000 = Reserved 10000 = x16 00001 = Reserved 10001 = x17 00010 = Reserved 10010 = x18 00011 = Reserved 10011 = x19 00100 = x4 10100 = x20 00101 = x5 10101 = x21 00110 = x6 10110 = x22 00111 = x7 10111 = x23 01000 = x8 11000 = x24 01001 = x9 11001 = x25 01010 = x10 11010 = Reserved 01011 = x11 11011 = Reserved 01100 = x12 11100 = Reserved 01101 = x13 11101 = Reserved 01110 = x14 11110 = Reserved 01111 = x15 11111 = Reserved PLLM select values 00000 through 00011 and 11010 through 11111 are <i>not</i> supported. |

Table 8-8. PLL Wrapper Divider x Registers (PLLDIV0, PLLDIV1, PLLDIV2, and PLLDIV3) (0x01B7 C114, 0x01B7 C118, 0x01B7 C11C, and 0x01B7 C120, respectively)

| | | | | | | | |
|----------|----------|----|----|----|----|---------------------------|----|
| 31 | 28 | 27 | 24 | 23 | 20 | 19 | 16 |
| Reserved | | | | | | | |
| R-0 | | | | | | | |
| 15 | 14 | 12 | 11 | 8 | 7 | 5 | 4 |
| DxEN | Reserved | | | | | PLLDIVx | |
| R/W-1 | R-0 | | | | | R/W-x xxxx ⁽¹⁾ | |

Legend: R = Read only, R/W = Read/write, -n = value at reset

(1) Default values for the PLLDIV0, PLLDIV1, PLLDIV2, and PLLDIV3 bits are /1 (0 0000), /1 (0 0000), /2 (0 0001), and /2 (0 0001), respectively.

CAUTION
D1 and D2 should never be disabled. D3 should only be disabled if ECLKIN is used.

Table 8-9. PLL Wrapper Divider x Registers (Prescaler Divider D0 and Post-Scaler Dividers D1, D2, and D3) Description⁽¹⁾

| BIT NO. | NAME | DESCRIPTION |
|---------|----------|--|
| 31:16 | Reserved | Reserved. Read only, writes have no effect. |
| 15 | DxEN | Divider Dx enable (where x denotes 0 through 3). 0: Divider x disabled. No clock output 1: Divider x enabled (default) These divider-enable bits are device specific and must be set to 1 to enable. |

(1) Note that SYSCLK2 *must* run at half the rate of SYSCLK1. Therefore, the divider ratio of D2 must be two times slower than D1. For example, if D1 is set to /2, then D2 must be set to /4.

**Table 8-9. PLL Wrapper Divider x Registers
(Prescaler Divider D0 and Post-Scaler Dividers D1, D2, and D3) Description⁽¹⁾ (continued)**

| BIT NO. | NAME | DESCRIPTION |
|---------|----------|--|
| 14:5 | Reserved | Reserved. Read only, writes have no effect. |
| 4:0 | PLLDIVx | PLL divider ratio (default values for the PLLDIV0, PLLDIV1, PLLDIV2, and PLLDIV3 bits are /1, /1, /2, and /2, respectively). 00000 = /1 10000 = /17 00001 = /2 10001 = /18 00010 = /3 10010 = /19 00011 = /4 10011 = /20 00100 = /5 10100 = /21 00101 = /6 10101 = /22 00110 = /7 10110 = /23 00111 = /8 10111 = /24 01000 = /9 11000 = /25 01001 = /10 11001 = /26 01010 = /11 11010 = /27 01011 = /12 11011 = /28 01100 = /13 11100 = /29 01101 = /14 11101 = /30 01110 = /15 11110 = /31 01111 = /16 11111 = /32 |

Table 8-10. Oscillator Divider 1 (OSCDIV1) Register (0x01B7 C124)

| | | | | | | | |
|----------|----------|----|----|----|----|---------|------|
| 31 | 28 | 27 | 24 | 23 | 20 | 19 | 16 |
| Reserved | | | | | | | |
| R-0 | | | | | | | |
| 15 | 14 | 12 | 11 | 8 | 7 | 5 | 4 |
| OD1EN | Reserved | | | | | OSCDIV1 | |
| R/W-1 | R-0 | | | | | R/W-0 | 0111 |

Legend: R = Read only, R/W = Read/write, -n = value at reset

Table 8-11. Oscillator Divider 1 (OSCDIV1) Register Description

| BIT NO. | NAME | DESCRIPTION |
|---------|----------|---|
| 31:16 | Reserved | Reserved. Read-only; writes have no effect. |
| 15 | OD1EN | Oscillator Divider 1 enable. 0: Oscillator Divider 1 disabled 1: Oscillator Divider 1 enabled (default) |
| 14:5 | Reserved | Reserved. Read only, writes have no effect. |
| 4:0 | OSCDIV1 | Oscillator Divider 1 ratio [default is /8 (0 0111)] <div style="display: flex; justify-content: space-between;"> 0000 = /1 1000 = /17 </div> <div style="display: flex; justify-content: space-between;"> 0001 = /2 1001 = /18 </div> <div style="display: flex; justify-content: space-between;"> 0010 = /3 1010 = /19 </div> <div style="display: flex; justify-content: space-between;"> 0011 = /4 1011 = /20 </div> <div style="display: flex; justify-content: space-between;"> 0100 = /5 1100 = /21 </div> <div style="display: flex; justify-content: space-between;"> 0101 = /6 1101 = /22 </div> <div style="display: flex; justify-content: space-between;"> 0110 = /7 1110 = /23 </div> <div style="display: flex; justify-content: space-between;"> 0111 = /8 1111 = /24 </div> <div style="display: flex; justify-content: space-between;"> 01000 = /9 11000 = /25 </div> <div style="display: flex; justify-content: space-between;"> 01001 = /10 11001 = /26 </div> <div style="display: flex; justify-content: space-between;"> 01010 = /11 11010 = /27 </div> <div style="display: flex; justify-content: space-between;"> 01011 = /12 11011 = /28 </div> <div style="display: flex; justify-content: space-between;"> 01100 = /13 11100 = /29 </div> <div style="display: flex; justify-content: space-between;"> 01101 = /14 11101 = /30 </div> <div style="display: flex; justify-content: space-between;"> 01110 = /15 11110 = /31 </div> <div style="display: flex; justify-content: space-between;"> 01111 = /16 11111 = /32 </div> |

9 MULTICHANNEL AUDIO SERIAL PORT (McASP) PERIPHERALS

The 320C6713/13B device includes two multichannel audio serial port (McASP) interface peripherals (McASP1 and McASP0). The McASP is a serial port optimized for the needs of multichannel audio applications. With two McASP peripherals, the 320C6713/13B device is capable of supporting two completely independent audio zones simultaneously.

Each McASP consists of a transmit and receive section. These sections can operate completely independently with different data formats, separate master clocks, bit clocks, and frame syncs or alternatively, the transmit and receive sections may be synchronized. Each McASP module also includes a pool of 16 shift registers that may be configured to operate as either transmit data, receive data, or general-purpose I/O (GPIO).

The transmit section of the McASP can transmit data in either a time division multiplexed (TDM) synchronous serial format or in a digital audio interface (DIT) format where the bit stream is encoded for S/PDIF, AES-3, IEC-60958, and CP-430 transmission. The receive section of the McASP supports the TDM synchronous serial format.

Each McASP can support one transmit data format (either a TDM format or DIT format) and one receive format at a time. All transmit shift registers use the same format and all receive shift registers use the same format. However, the transmit and receive formats need not be the same.

Both the transmit and receive sections of the McASP also support burst mode, which is useful for non-audio data (for example, passing control information between two DSPs).

The McASP peripherals have additional capability for flexible clock generation, and error detection/handling, as well as error management.

9.1 McASP Block Diagram

[Figure 9-1](#) shows the major blocks along with external signals of the 320C6713/13B McASP1 and McASP0 peripherals, and shows the eight serial data [AXR] pins for each McASP. Each McASP also includes full general-purpose I/O (GPIO) control, so any pins not needed for serial transfers can be used for general-purpose I/O.

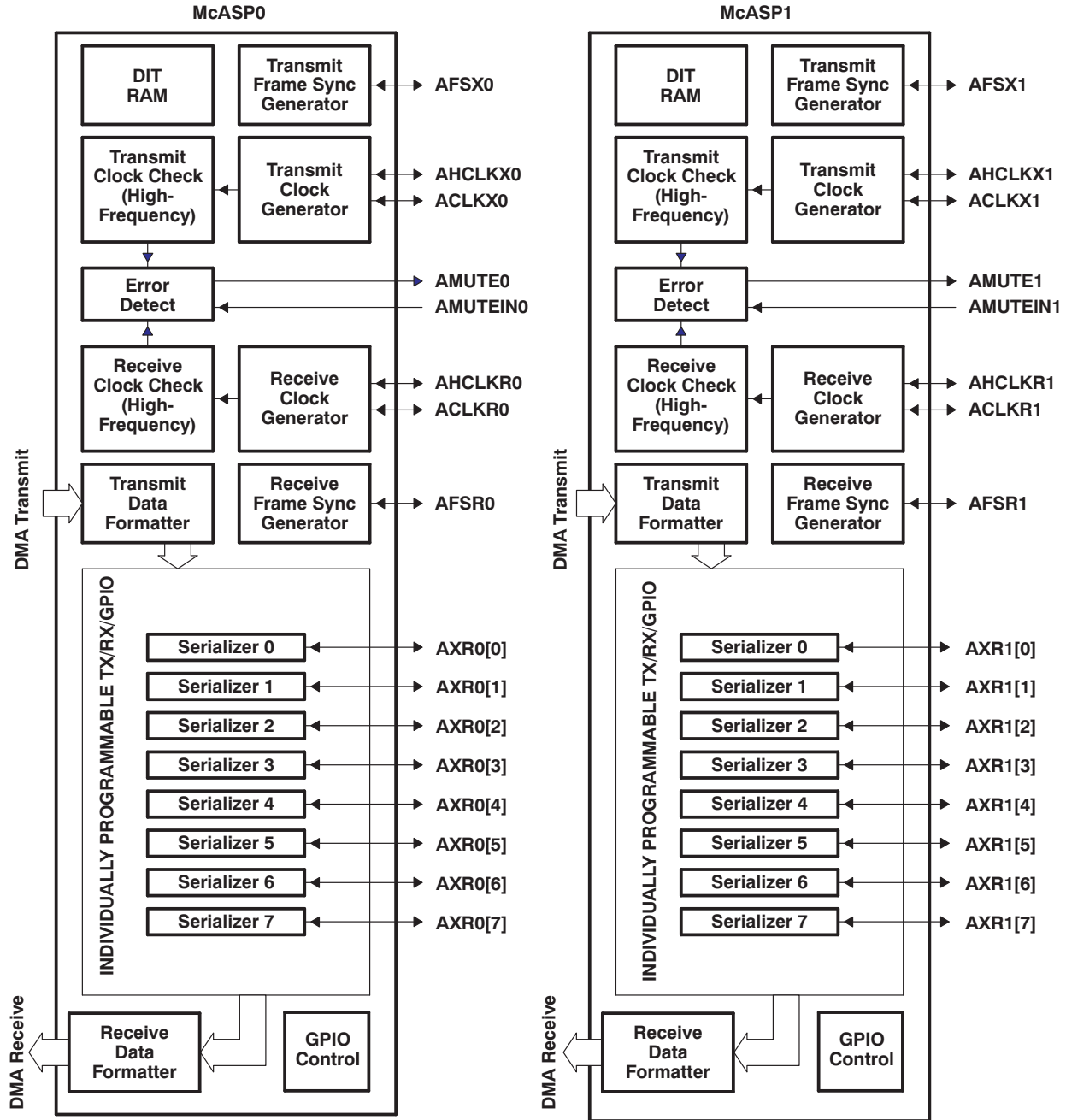


Figure 9-1. McASP0 and McASP1 Configuration

9.2 Multichannel Time Division Multiplexed (TDM) Synchronous Transfer Mode

The McASP supports a multichannel TDM synchronous transfer mode for both transmit and receive. Within this transfer mode, a wide variety of serial data formats are supported, including formats compatible with devices using the Inter-Integrated Sound (IIS) protocol.

TDM synchronous transfer mode is typically used when communicating between integrated circuits, such as between a DSP and one or more ADC, DAC, codec, or S/PDIF receiver devices. In multichannel applications, it is typical to find several devices operating synchronized with each other. For example, to provide six analog outputs, three stereo DAC devices would be driven with the same bit clock and frame sync, but each stereo DAC would use a different McASP serial data pin carrying stereo data (two TDM time slots, left and right).

The TDM synchronous serial transfer mode utilizes several control signals and one or more serial data signals:

- A bit clock signal (ACLKX for transmit, ACKLR for receive)
- A frame sync signal (AFSX for transmit, AFSR for receive)
- An (optional) high-frequency master clock (AHCLKX for transmit, AHCLKR for receive) from which the bit clock is derived
- One or more serial data pins (AXR for transmit and for receive)

Except for the optional high-frequency master clock, all of the signals in the TDM synchronous serial transfer mode protocol are synchronous to the bit clocks (ACLKX and ACKLR).

In the TDM synchronous transfer mode, the McASP continually transmits and receives data periodically (since audio ADCs and DACs operate at a fixed-data rate). The data is organized into frames, and the beginning of a frame is marked by a frame sync pulse on the AFSX, AFSR pin.

In a typical audio system, one frame is transferred per sample period. To support multiple channels, the choices are to either include more time slots per frame (and therefore operate with a higher bit clock) or to keep the bit clock period constant and use additional data pins to transfer the same number of channels. For example, a particular six-channel DAC might require three McASP serial data pins; transferring two channels of data on each serial data pin during each sample period (frame). Another similar DAC may be designed to use only a single McASP serial data pin, but clocked three times faster and transferring six channels of data per sample period. The McASP is flexible enough to support either type of DAC, but a transmitter cannot be configured to do both at the same time.

For multiprocessor applications, the McASP supports any number of time slots per frame (between 2 and 32), and includes the ability to disable transfers during specific time slots.

In addition, to support S/PDIF, AES-3, IEC-60958, and CP-430 receiver chips whose natural block (McASP frame) size is 384 samples; the McASP receiver supports a 384 time slot mode. The advantage to using the 384 time slot mode is that interrupts may be generated synchronous to the S/PDIF, AES-3, IEC-60958, and CP-430 receivers; for example, the last slot interrupt.

9.3 Burst Transfer Mode

The McASP also supports a burst transfer mode, which is useful for non-audio data (for example, passing control information between two DSPs). Burst transfer mode uses a synchronous serial format similar to TDM, except the frame sync is generated for each data word transferred. In addition, frame sync generation is not periodic or time driven as in TDM mode, but rather data driven.

9.4 Supported Bit Stream Formats for TDM and Burst Transfer Modes

The serial data pins support a wide variety of formats. In the TDM and burst synchronous modes, the data may be transmitted/received with the following options:

- Time slots per frame: 1 (burst/data driven), or 2,3...32 (TDM/time driven)
- Time slot size: 8, 12, 16, 20, 24, 28, 32 bits per time slot
- Data size: 8, 12, 16, 20, 24, 28, 32 bits (must be less than or equal to time slot)
- Data alignment within time slot: left or right justified
- Bit order: MSB or LSB first
- Unused bits in time slot: Padded with 0, 1 or extended with value of another bit
- Time slot delay from frame sync: 0-, 1-, or 2-bit delay

The data format can be programmed independently for transmit and receive, and for McASP0 versus McASP1. In addition, the McASP can automatically realign the data as processed natively by the DSP (any format on a nibble boundary) adjusting the data in hardware to any of the supported serial bit stream formats (TDM, burst, and DIT modes). This adjustment reduces the amount of bit manipulation that the DSP must perform and simplifies software architecture.

9.5 Digital Audio Interface Transmitter (DIT) Transfer Mode (Transmitter Only)

The McASP transmit section may also be configured in DIT mode where it outputs data formatted for transmission over an S/PDIF, AES-3, IEC-60958, or CP-430 standard link. These standards encode the serial data such that the equivalent of *clock* and *frame sync* are embedded within the data stream. DIT transfer mode is used as an interconnect between audio components and can transfer multichannel digital audio data over a single optical or coaxial cable.

From an internal DSP standpoint, the McASP operation in DIT transfer mode is similar to the two-time-slot TDM mode, but the data transmitted is output as a bi-phase mark encoded bit stream with preamble, channel status, user data, validity, and parity automatically stuffed into the bit stream by the McASP module. The McASP includes separate validity bits for even/odd subframes and two 384-bit register file modules to hold channel status and user data bits.

DIT mode requires (at a minimum):

- One serial data pin (if the AUXCLK is used as the reference (see [Figure 8-1](#))
OR
- One serial data pin plus either the AHCLKX or ACLKX pin (if an external clock is needed)

If additional serial data pins are used, each McASP may be used to transmit multiple encoded bit streams (one per pin). However, the bit streams will all be synchronized to the same clock and the user data, channel status, and validity information carried by each bit stream will be the same for all bit streams transmitted by the same McASP module.

The McASP can also automatically realign the data as processed by the DSP (any format on a nibble boundary) in DIT mode; reducing the amount of bit manipulation that the DSP must perform and simplifying software architecture.

9.6 McASP Flexible Clock Generators

The McASP transmit and receive clock generators are identical. Each clock generator can accept a high-frequency master clock input (on the AHCLKX and AHCLKR pins).

The transmit and receive bit clocks (on the ACLKX and ACLKR pins) can also be sourced externally or can be sourced internally by dividing down the high-frequency master clock input (programmable factor /1, /2, /3, ... /4096). The polarity of each bit clock is individually programmable.

The frame sync pins are AFSX (transmit) and AFSR (receive). A typical usage for these pins is to carry the left-right clock (LRCLK) signal when transmitting and receiving stereo data. The frame sync signals are individually programmable for either internal or external generation, either bit or slot length, and either rising or falling edge polarity.

Some examples of the things that a system designer can use the McASP clocking flexibility for are:

- Input a high-frequency master clock (for example, 512 f_s of the receiver) and receive with an internally generated bit clock ratio of /8, while transmitting with an internally generated bit clock ratio of /4 or /2. (An example application would be to receive data from a DVD at 48 kHz but output up-sampled or decoded audio at 96 kHz or 192 kHz.)
- Transmit/receive data based on sample rate (for example, 44.1 kHz) using McASP0 while transmitting and receiving at a different sample rate (for example, 48 kHz) on McASP1.
- Use the DSP on-board AUXCLK to supply the system clock when the input source is an A/D converter.

9.7 McASP Error Handling and Management

To support the design of a robust audio system, the McASP module includes error-checking capability for the serial protocol, data underrun, and data overrun. In addition, each McASP includes a timer that continually measures the high-frequency master clock every 32 SYSCLK2 clock cycles. The timer value can be read to get a measurement of the high-frequency master clock frequency and has a min-max range setting that can raise an error flag if the high-frequency master clock goes out of a specified range. The user would read the high-frequency transmit master clock measurement (AHCLKX0 or AHCLKX1) by reading the XCNT field of the XCLKCHK register and the user would read the high-frequency receive master clock measurement (AHCLKR0 or AHCLKR1) by reading the RCNT field of the RCLKCHK register.

Upon the detection of any one or more of the above errors (software selectable) or the assertion of the AMUTE_IN pin, the AMUTE output pin may be asserted to a high or low level (selectable) to immediately mute the audio output. In addition, an interrupt may be generated if enabled based on any one or more of the error sources.

9.8 McASP Interrupts and EDMA Events

The McASP transmitter and receiver sections each generate an event on every time slot. This event can be serviced by an interrupt or by the EDMA controller.

When using interrupts to service the McASP, each shift register buffer has a unique address in the McASP registers space (see [Table 4-1](#)).

When using the EDMA to service the McASP, the McASP DATA Port space, shown in [Table 4-1](#), is accessed. In this case, the address least-significant bits are ignored. Writes to any address in this range access the transmitting buffers in order from lowest (serializer 0) to highest (serializer 15), skipping over disabled and receiving serializers. Likewise, reads from any address in this space access the receiving buffers in the same order but skip over disabled and transmitting buffers.

9.9 I²C

Having two I²C modules on the 320C6713/13B simplifies system architecture, since one module may be used by the DSP to control local peripherals ICs (DACs, ADCs, etc.) while the other may be used to communicate with other controllers in a system or to implement a user interface.

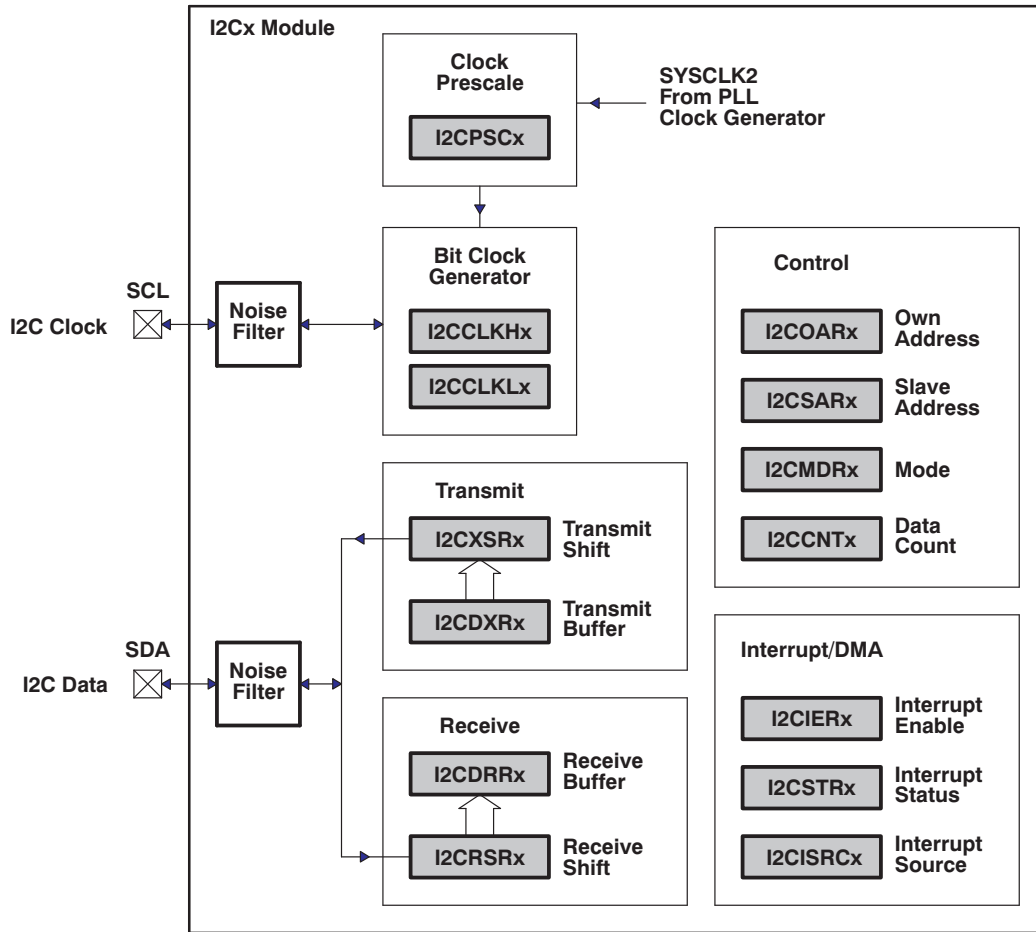
NOTE

I²C ports are compatible with Philips I2C Specification Revision 2.1 (January 2000).

The 320C6713/13B also includes two I²C serial ports for control purposes. Each I²C port supports:

- Fast mode up to 400 Kbps (no fail-safe I/O buffers)
- Noise filter to remove noise 50 ns or less
- 7- and 10-bit device addressing modes
- Master (transmit/receive) and slave (transmit/receive) functionality
- Events: DMA, interrupt, or polling
- Slew-rate limited open-drain output buffers

[Figure 9-2](#) shows a block diagram of the I2Cx module.



NOTE: Shading denotes control/status registers.

Figure 9-2. I2Cx Module Block Diagram

10 LOGIC AND POWER SUPPLY

This section discusses the logic and power-supply configuration of the SM320C6713-EP and SM320C6713B-EP.

10.1 General-Purpose Input/Output (GPIO)

To use the GP[15:0] software-configurable GPIO pins, the GPxEN bits in the GP enable (GPEN) register and the GPxDIR bits in the GP direction (GPDIR) register must be properly configured.

GPxEN = 1 GP[x] pin is enabled.
GPxDIR = 0 GP[x] pin is an input.
GPxDIR = 1 GP[x] pin is an output.

where x represents one of the 15 through 0 GPIO pins.

Figure 10-1 shows the GPIO enable bits in the GPEN register for the C6713/13B device. To use any of the GPx pins as general-purpose input/output functions, the corresponding GPxEN bit must be set to 1 (enabled). Default values are device-specific, so refer to Figure 10-1 for the C6713/13B default configuration.

| | | | | | | | | | | | | | | | | | | | |
|----------|--------|--------|--------|--------|--------|-------|-------|----|--|----|--|----|--|---|--|--|--|--|--|
| 31 | | | | | | | | 24 | | 23 | | 16 | | | | | | | |
| Reserved | | | | | | | | | | | | | | | | | | | |
| R-0 | | | | | | | | | | | | | | | | | | | |
| 15 | | 14 | | 13 | | 12 | | 11 | | 10 | | 9 | | 8 | | | | | |
| GP15EN | GP14EN | GP13EN | GP12EN | GP11EN | GP10EN | GP9EN | GP8EN | | | | | | | | | | | | |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | | | | | | | | | | | | |
| 7 | | 6 | | 5 | | 4 | | 3 | | 2 | | 1 | | 0 | | | | | |
| GP7EN | GP6EN | GP5EN | GP4EN | GP3EN | GP2EN | GP1EN | GP0EN | | | | | | | | | | | | |
| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | | | | | | | | | | | | |

Legend: R/W = Readable/Writeable; -n = value after reset, -x = undefined value after reset

Figure 10-1. GPIO Enable (GPEN) Register (Hex Address: 01B0 0000)

Figure 10-2 shows the GPIO direction bits in the GPIO Direction (GPDIR) register. This register determines if a given GPIO pin is an input or an output providing the corresponding GPxEN bit is enabled (set to 1) in the GPEN register. By default, all the GPIO pins are configured as input pins.

| | | | | | | | | | | | | | | | | | | | |
|----------|---------|---------|---------|---------|---------|--------|--------|----|--|----|--|----|--|---|--|--|--|--|--|
| 31 | | | | | | | | 24 | | 23 | | 16 | | | | | | | |
| Reserved | | | | | | | | | | | | | | | | | | | |
| R-0 | | | | | | | | | | | | | | | | | | | |
| 15 | | 14 | | 13 | | 12 | | 11 | | 10 | | 9 | | 8 | | | | | |
| GP15DIR | GP14DIR | GP13DIR | GP12DIR | GP11DIR | GP10DIR | GP9DIR | GP8DIR | | | | | | | | | | | | |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | | | | | | | | | | | | |
| 7 | | 6 | | 5 | | 4 | | 3 | | 2 | | 1 | | 0 | | | | | |
| GP7DIR | GP6DIR | GP5DIR | GP4DIR | GP3DIR | GP2DIR | GP1DIR | GP0DIR | | | | | | | | | | | | |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | | | | | | | | | | | | |

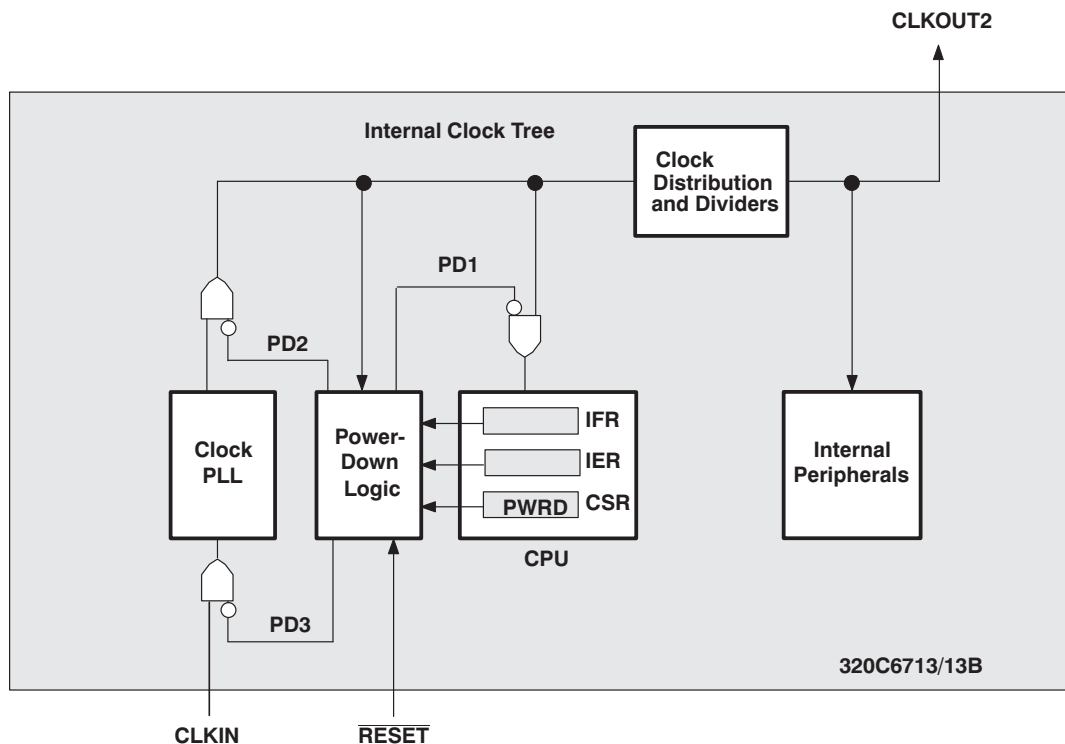
Legend: R/W = Readable/Writeable; -n = value after reset, -x = undefined value after reset

Figure 10-2. GPIO Direction (GPDIR) Register (Hex Address: 01B0 0004)

For more detailed information on general-purpose inputs/outputs (GPIOs), see the *TMS320C6000 DSP General-Purpose Input/Output (GPIO) Reference Guide* (literature number [SPRU584](#)).

10.2 Power-Down Mode Logic

Figure 10-3 shows the power-down mode logic on the C6713/13B.



A. External input clocks, with the exception of CLKIN and CLKOUT3, are not gated by the power-down mode logic.

Figure 10-3. Power-Down Mode Logic

10.2.1 Triggering, Wake-Up, and Effects

The device includes a programmable PLL which allows software control of PLL bypass via the PLEN bit in the PLLCSR register. With this enhanced functionality come some additional considerations when entering power-down modes.

The power-down modes (PD2 and PD3) function by disabling the PLL to stop clocks to the C6713 device. However, if the PLL is bypassed (PLEN = 0), the device will still receive clocks from the external clock input (CLKIN). Therefore, bypassing the PLL makes the power-down modes PD2 and PD3 ineffective.

The PLL needs to be enabled by writing a "1" to PLEN bit (PLLCSR.0) before being able to enter either PD3 (CSR.11) or PD2 (CSR.10) in order for these modes to have an effect.

For the TMS320C6713B device it is recommended to use the PLLPWDN bit (PLLCSR.1) to enter a deep power-down state equivalent to PD3 since the PLLPWDN bit takes full advantage of the PLL power-down feature.

The power-down modes (PD1, PD2 and PD3) and their wake-up methods are programmed by setting the PWRD field (bits 15–10) of the control status register (CSR). The PWRD field of the CSR is shown in [Figure 10-4](#) and described in [Table 10-1](#). When writing to the CSR, all bits of the PWRD field should be set at the same time. Logic 0 should be used when writing to the reserved bit (bit 15) of the PWRD field. The CSR is discussed in detail in the *TMS320C6000 CPU and Instruction Set Reference Guide* (literature number [SPRU189](#)).

| | | | | | | | |
|----------|--------------------------------------|------------------------|-------|-------|-------|----|---|
| 31 | | | | | | 16 | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Reserved | Enable or Non-Enabled Interrupt Wake | Enabled Interrupt Wake | PD3 | PD2 | PD1 | | |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | | |
| 7 | | | | | | 0 | |

Legend: R/W-x = Read/write reset value

Figure 10-4. PWRD Field of the CSR

A delay of up to nine clock cycles may occur after the instruction that sets the PWRD bits in the CSR before the PD mode takes effect. As best practice, NOPs should be padded after the PWRD bits are set in the CSR to account for this delay.

If PD1 mode is terminated by a non-enabled interrupt, the program execution returns to the instruction where PD1 took effect. If PD1 mode is terminated by an enabled interrupt, the interrupt service routine will be executed first, then the program execution returns to the instruction where PD1 took effect. In the case with an enabled interrupt, the GIE bit in the CSR and the NMIE bit in the interrupt enable register (IER) must also be set for the interrupt service routine to execute; otherwise, execution returns to the instruction where PD1 took effect upon PD1 mode termination by an enabled interrupt.

PD2 and PD3 modes can only be aborted by device reset. Table 10-1 summarizes all the power-down modes.

Table 10-1. Characteristics of the Power-Down Modes

| PRWD FIELD (BITS 15–10) | POWER-DOWN MODE | WAKE-UP METHOD | EFFECT ON CHIP OPERATION |
|-------------------------|--------------------|---|--|
| 000000 | No power down | — | — |
| 001001 | PD1 | Wake by an enabled interrupt | CPU halted (except for the interrupt logic) Power-down mode blocks the internal clock inputs at the boundary of the CPU, preventing most of the CPU logic from switching. During PD1, EDMA transactions can proceed between peripherals and internal memory. |
| 010001 | PD1 | Wake by an enabled or non-enabled interrupt | |
| 011010 | PD2 ⁽¹⁾ | Wake by a device reset | Output clock from PLL is halted, stopping the internal clock structure from switching and resulting in the entire chip being halted. All register and internal RAM contents are preserved. All functional I/O freeze in the last state when the PLL clock is turned off. |
| 011100 | PD3 ⁽¹⁾ | Wake by a device reset | Input clock to the PLL stops generating clocks. All register and internal RAM contents are preserved. All functional I/O freeze in the last state when the PLL clock is turned off. Following reset, the PLL needs time to relock, just as it does following power up. Wake-up from PD3 takes longer than wake-up from PD2 because the PLL needs to be relocked, just as it does following power up. It is recommended to use the PLLPWDN bit (PLLCSR.1) as an alternative to PD3. |
| All others | Reserved | — | — |

(1) When entering PD2 and PD3, all functional I/Os remain in the previous state. However, for peripherals that are asynchronous in nature or peripherals with an external clock source, output signals may transition in response to stimulus on the inputs. Under these conditions, peripherals will not operate according to specifications.

10.3 Power-Supply Sequencing

TI DSPs do not require specific power sequencing between the core supply and the I/O supply. However, systems should be designed to ensure that neither supply is powered up for extended periods of time (>1 second) if the other supply is below the proper operating voltage.

10.3.1 System-Level Design Considerations

System-level design considerations, such as bus contention, may require supply sequencing to be implemented. In this case, the core supply should be powered up before, and powered down after, the I/O buffers. This is to ensure that the I/O buffers receive valid inputs from the core before the output buffers are powered up, thus preventing bus contention with other chips on the board.

10.3.2 Power-Supply Design Considerations

A dual-power supply with simultaneous sequencing can be used to eliminate the delay between core and I/O power up. A Schottky diode can also be used to tie the core rail to the I/O rail (see [Figure 10-5](#)).

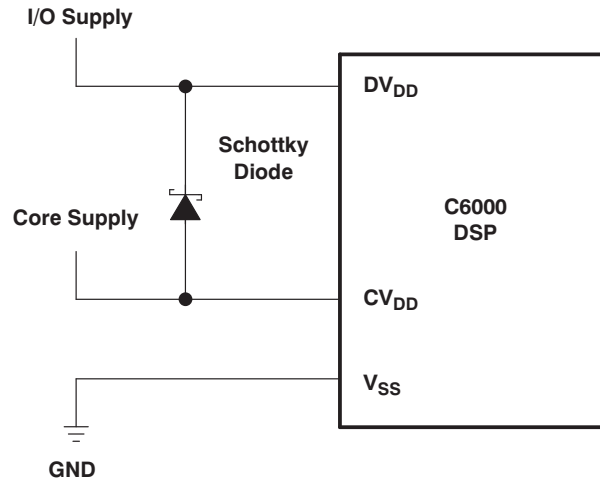


Figure 10-5. Schottky Diode Diagram

Core and I/O supply voltage regulators should be located close to the DSP (or DSP array) to minimize inductance and resistance in the power delivery path. Additionally, when designing for high-performance applications utilizing the C6000 platform of DSPs, the printed circuit board (PCB) should include separate power planes for core, I/O, and ground, all bypassed with high-quality low-ESL/ESR capacitors.

10.4 Power-Supply Decoupling

To properly decouple the supply planes from system noise, place as many capacitors (caps) as possible close to the DSP. Assuming 0603 caps, the user should be able to fit a total of 60 caps—30 for the core supply and 30 for the I/O supply. These caps need to be close (no more than 1.25-cm maximum distance) to the DSP to be effective. Physically smaller caps are better, such as 0402, but the size needs to be evaluated from a yield/manufacturing point-of-view. Parasitic inductance limits the effectiveness of the decoupling capacitors; therefore, physically smaller capacitors should be used while maintaining the largest available capacitance value. As with the selection of any component, verification of capacitor availability over the product's production lifetime needs to be considered.

10.5 IEEE Std 1149.1 JTAG Compatibility Statement

The 320C6713/13B DSP requires that both $\overline{\text{TRST}}$ and $\overline{\text{RESET}}$ resets be asserted upon power up to be properly initialized. While $\overline{\text{RESET}}$ initializes the DSP core, $\overline{\text{TRST}}$ initializes the DSP emulation logic. Both resets are required for proper operation.

NOTE

$\overline{\text{TRST}}$ is synchronous and must be clocked by TCLK; otherwise, BSCAN may not respond as expected after $\overline{\text{TRST}}$ is asserted.

While both $\overline{\text{TRST}}$ and $\overline{\text{RESET}}$ need to be asserted upon power-up, only $\overline{\text{RESET}}$ needs to be released for the DSP to boot properly. $\overline{\text{TRST}}$ may be asserted indefinitely for normal operation, keeping the JTAG port interface and DSP emulation logic in the reset state.

$\overline{\text{TRST}}$ only needs to be released when it is necessary to use a JTAG controller to debug the DSP or exercise the DSP boundary scan functionality.

The TMS320C6713B DSP includes an internal pulldown (IPD) on the $\overline{\text{TRST}}$ pin to ensure that $\overline{\text{TRST}}$ will always be asserted upon power up and the DSP's internal emulation logic will always be properly initialized when this pin is not routed out. JTAG controllers from Texas Instruments actively drive $\overline{\text{TRST}}$ high. However, some third-party JTAG controllers may not drive $\overline{\text{TRST}}$ high but expect the use of an external pullup resistor on $\overline{\text{TRST}}$. When using this type of JTAG controller, assert $\overline{\text{TRST}}$ to initialize the DSP after powerup and externally drive $\overline{\text{TRST}}$ high before attempting any emulation or boundary scan operations.

Following the release of $\overline{\text{RESET}}$, the low-to-high transition of $\overline{\text{TRST}}$ must be “seen” to latch the state of EMU1 and EMU0. The EMU[1:0] pins configure the device for either boundary scan mode or emulation mode. For more detailed information, see the terminal functions section of this data sheet.

NOTE

Note: The DESIGN-WARNING section of the TMS320C6713B BSDL file contains information and constraints regarding proper device operation while in boundary scan mode.

For more detailed information on the C6713B JTAG emulation, see the TMS320C6000 DSP Designing for JTAG Emulation Reference Guide (literature number [SPRU641](#)).

10.6 EMIF Device Speed

The maximum EMIF speed on the C6713/13B device is 100 MHz. TI recommends utilizing I/O buffer information specification (IBIS) to analyze all ac timings to determine if the maximum EMIF speed is achievable for a given board layout. To properly use IBIS models to attain accurate timing analysis for a given system, see the application report *Using IBIS Models for Timing Analysis* (literature number [SPRA839](#)).

For ease of design evaluation, [Table 10-2](#) contains IBIS simulation results showing the maximum EMIF-SDRAM interface speeds for the given example boards (TYPE) and SDRAM speed grades. Timing analysis should be performed to verify that all ac timings are met for the specified board layout. Other configurations are also possible, but again, timing analysis must be done to verify proper ac timings.

To maintain signal integrity, serial termination resistors should be inserted into all EMIF output signal lines (see the [Terminal Functions](#) table for the EMIF output signals).

Table 10-2. C6713/13B Example Boards and Maximum EMIF Speed

| BOARD CONFIGURATION | | | SDRAM SPEED GRADE | MAXIMUM ACHIEVABLE EMIF-SDRAM INTERFACE SPEED |
|----------------------|--|--|----------------------------|--|
| TYPE | EMIF INTERFACE COMPONENTS | BOARD TRACE | | |
| 1-Load Short Traces | One bank of one 32-bit SDRAM | 1- to 3-in traces with proper termination resistors; Trace impedance ~50 Ω | 143-MHz 32-bit SDRAM (-7) | 100 MHz |
| | | | 166-MHz 32-bit SDRAM (-6) | For short traces, SDRAM data output hold time on these SDRAM speed grades cannot meet EMIF input hold time requirement. ⁽¹⁾ |
| | | | 183-MHz 32-bit SDRAM (-55) | |
| | | | 200-MHz 32-bit SDRAM (-5) | |
| 2-Loads Short Traces | One bank of two 16-bit SDRAMs | 1.2 to 3 in from EMIF to each load, with proper termination resistors; Trace impedance ~78 Ω | 125-MHz 16-bit SDRAM (-8E) | 100 MHz |
| | | | 133-MHz 16-bit SDRAM (-75) | 100 MHz |
| | | | 143-MHz 16-bit SDRAM (-7E) | 100 MHz |
| | | | 167-MHz 16-bit SDRAM (-6A) | 100 MHz |
| | | | 167-MHz 16-bit SDRAM (-6) | 100 MHz |
| 3-Loads Short Traces | One bank of two 16-bit SDRAMs One bank of buffer | 1.2 to 3 inches from EMIF to each load, with proper termination resistors; Trace impedance ~78 Ω | 125-MHz 16-bit SDRAM (-8E) | For short traces, EMIF cannot meet SDRAM input hold requirement. ⁽¹⁾ |
| | | | 133-MHz 16-bit SDRAM (-75) | 100 MHz |
| | | | 143-MHz 16-bit SDRAM (-7E) | 100 MHz |
| | | | 167-MHz 16-bit SDRAM (-6A) | 100 MHz |
| | | | 167-MHz 16-bit SDRAM (-6) | For short traces, EMIF cannot meet SDRAM input hold requirement. ⁽¹⁾ |
| 3-Loads Long Traces | One bank of one 32-bit-bit SDRAM, One bank of one 32-bit-bit SDRAM, One bank of buffer | 4 to 7 in from EMIF; Trace impedance ~63 Ω | 143-MHz 32-bit SDRAM (-7) | 83 MHz |
| | | | 166-MHz 32-bit SDRAM (-6) | 83 MHz |
| | | | 183-MHz 32-bit SDRAM (-55) | 83 MHz |
| | | | 200-MHz 32-bit SDRAM (-5) | SDRAM data output hold time cannot meet EMIF input hold requirement. ⁽¹⁾ |

(1) Results are based on IBIS simulations for the given example boards (TYPE). Timing analysis should be performed to determine if timing requirements can be met for the particular system.

10.7 EMIF Big Endian Mode Correctness (C6713B Only)

The HD8 pin device endian mode (LENDIAN) selects the endian mode of operation (Little or Big Endian). For the C6713/13B device Little Endian is the default setting.

The C6713B HD12 pin (EMIF Big Endian Mode Correctness) [EMIFBE] enhancement allows the flexibility to change the EMIF data placement on the EMIF bus.

When using the default setting of HD12 = 1 for the C6713B, the EMIF will present 8-bit or 16-bit data on the ED[7:0] side of the bus if using Little Endian mode (HD8 = 1), and to the ED[31:24] side of the bus if using Big Endian mode. Figure 10-6 shows the mapping of 16-bit and 8-bit C6713B devices.

| EMIF DATA LINES (PINS) WHERE DATA PRESENT | | | |
|---|-----------------|---|--|
| ED[31:24] (BE3) | ED[23:16] (BE2) | ED[15:8] (BE1) | ED[7:0] (BE0) |
| 32-Bit Device in Any Endianness Mode | | | |
| 16-Bit Device in Big Endianness Mode | | 16-Bit Device in Little Endianness Mode | |
| 8-Bit Device in Big Endianness Mode | | | 8-Bit Device in Little Endianness Mode |

Figure 10-6. 16/8-Bit EMIF Big Endian Mode Correctness Mapping (HD12 = 1) (C6713B Only)

When HD12 = 0 for the C6713B, enabling EMIF endianness correction, the EMIF will present 8-bit or 16-bit data on the ED[7:0] side of the bus, regardless of the endianness mode (see Figure 10-7)

| EMIF DATA LINES (PINS) WHERE DATA PRESENT | | | |
|---|--------------------------------|---|------------------------------|
| ED[31:24] ($\overline{BE3}$) | ED[23:16] ($\overline{BE2}$) | ED[15:8] ($\overline{BE1}$) | ED[7:0] ($\overline{BE0}$) |
| 32-Bit Device in Any Endianness Mode | | | |
| | | 16-Bit Device in Any Endianness Mode | |
| | | 8-Bit Device in Any Endianness Mode | |

Figure 10-7. 16/8-Bit EMIF Big Endian Mode Correctness Mapping (HD12 = 0) (C6713B Only)

This new C6713B endianness correction functionality does not affect systems using the default value of HD12 = 1.

This new C6713B feature does not affect systems operating in Little Endian mode.

10.8 Bootmode

The C6713/13B device resets using the active-low signal \overline{RESET} and the internal reset signal. While \overline{RESET} is low, the internal reset is also asserted and the device is held in reset and is initialized to the prescribed reset state. Refer to [Reset Timing](#) for reset timing characteristics and states of device pins during reset. The release of the internal reset signal (see the [Reset phase 3 discussion](#) in the [RESET Timing](#) section of this data sheet) starts the processor running with the prescribed device configuration and boot mode.

The C6713/13B has three types of boot modes:

- Host boot

If host boot is selected, upon release of internal reset, the CPU is internally stalled while the remainder of the device is released. During this period, an external host can initialize the CPU memory space as necessary through the host interface, including internal configuration registers, such as those that control the EMIF or other peripherals. Once the host is finished with all necessary initialization, it must set the DSPINT bit in the HPIC register to complete the boot process. This transition causes the boot configuration logic to bring the CPU out of the stalled state. The CPU then begins execution from address 0. The DSPINT condition is not latched by the CPU, because it occurs while the CPU is still internally stalled. Also, DSPINT brings the CPU out of the stalled state only if the host boot process is selected. All memory may be written to and read by the host. This allows for the host to verify what it sends to the DSP if required. After the CPU is out of the stalled state, the CPU needs to clear the DSPINT; otherwise, no more DSPINTs can be received.
- Emulation boot

Emulation boot mode is a variation of host boot. In this mode, it is not necessary for a host to load code or to set DSPINT to release the CPU from the stalled state. Instead, the emulator will set DSPINT if it has not been previously set so that the CPU can begin executing code from address 0. Before beginning execution, the emulator sets a breakpoint at address 0. This prevents the execution of invalid code by halting the CPU before executing the first instruction. Emulation boot is a good tool in the debug phase of development.
- EMIF boot (using default ROM timings)

Upon the release of internal reset, the 1K-Byte ROM code located in the beginning of CE1 is copied to address 0 by the EDMA using the default ROM timings, while the CPU is internally stalled. The data should be stored in the endian format that the system is using. The boot process also lets you choose the width of the ROM. In this case, the EMIF automatically assembles consecutive 8-bit bytes or 16-bit half-words to form the 32-bit instruction words to be copied. The transfer is automatically done by the EDMA as a single-frame block transfer from the ROM to address 0. After completion of the block transfer, the CPU is released from the stalled state and start running from address 0.

11 PARAMETRIC INFORMATION

11.1 Absolute Maximum Ratings⁽¹⁾

over operating case temperature range (unless otherwise noted)

| | | VALUE | UNIT |
|--|--------------------------|-------------------------|------|
| Supply voltage range, CV_{DD} ⁽²⁾ | | –0.3 to 1.8 | V |
| Supply voltage range, DV_{DD} ⁽²⁾ | | –0.3 to 4 | V |
| Input voltage range | | –0.3 to $DV_{DD} + 0.5$ | V |
| Output voltage range | | –0.3 to $DV_{DD} + 0.5$ | V |
| Operating case temperature range T_C | A version | –40 to 105 | °C |
| | S version | –55 to 105 | |
| | M version ⁽³⁾ | –55 to 125 | |
| Storage temperature range, T_{stg} | | –60 to 150 | °C |

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to V_{SS} .
- (3) Long-term high temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See http://ti.com/ep_quality for additional information on enhanced product packaging.

11.2 Recommended Operating Conditions⁽¹⁾

| | | | MIN | NOM | MAX | UNIT | |
|-------------|---|--|--|------|----------------------|------|----|
| CV_{DD} | Supply voltage, core referenced to V_{SS} | C6713B | 1.20 | 1.26 | 1.32 | V | |
| | | C6713B 300 MHz only | 1.33 | 1.40 | 1.47 | | |
| DV_{DD} | Supply voltage, I/O referenced to V_{SS} | | 3.13 | 3.3 | 3.47 | V | |
| $V_{(C-D)}$ | Maximum supply voltage difference, $CV_{DD} - DV_{DD}$ | | | | 1.32 | V | |
| $V_{(D-C)}$ | Maximum supply voltage difference, $DV_{DD} - CV_{DD}$ | | | | 2.75 | V | |
| V_{IH} | High-level input voltage | All signals except $CLKS1/SCL1$, $DR1/SDA1$, $SCL0$, $SDA0$, and $RESET$ | 2 | | | V | |
| | | $CLKS1/SCL1$, $DR1/SDA1$, $SCL0$, $SDA0$, and $RESET$ | 2 | | | | |
| V_{IL} | Low-level input voltage | All signals except $CLKS1/SCL1$, $DR1/SDA1$, $SCL0$, $SDA0$, and $RESET$ | 0.8 | | | V | |
| | | $CLKS1/SCL1$, $DR1/SDA1$, $SCL0$, $SDA0$, and $RESET$ | | | $0.3 \times DV_{DD}$ | | |
| I_{OH} | High-level output current | C6713 ⁽²⁾ | All signals except $ECLKOUT$, $CLKOUT2$, $CLKOUT3$, $CLKS1/SCL1$, $DR1/SDA1$, $SCL0$, and $SDA0$ | –8 | | | mA |
| | | | $ECLKOUT$, $CLKOUT2$, and $CLKOUT3$ | –16 | | | |
| | | C6713B ⁽²⁾ | All signals except $ECLKOUT$, $CLKOUT2$, $CLKS1/SCL1$, $DR1/SDA1$, $SCL0$, and $SDA0$ | –8 | | | |
| | | | $ECLKOUT$ and $CLKOUT2$ | –16 | | | |
| I_{OL} | Low-level output current | C6713 ⁽²⁾ | All signals except $ECLKOUT$, $CLKOUT2$, $CLKOUT3$, $CLKS1/SCL1$, $DR1/SDA1$, $SCL0$, and $SDA0$ | 8 | | | mA |
| | | | $ECLKOUT$, $CLKOUT2$, and $CLKOUT3$ | 16 | | | |
| | | | $CLKS1/SCL1$, $DR1/SDA1$, $SCL0$, and $SDA0$ | 3 | | | |
| | | C6713B ⁽²⁾ | All signals except $ECLKOUT$, $CLKOUT2$, $CLKS1/SCL1$, $DR1/SDA1$, $SCL0$, and $SDA0$ | 8 | | | |
| | | | $ECLKOUT$ and $CLKOUT2$ | 16 | | | |
| | | | $CLKS1/SCL1$, $DR1/SDA1$, $SCL0$, and $SDA0$ | 3 | | | |
| V_{OS} | Maximum voltage during overshoot (See Figure 11-4) | | | | $4^{(3)}$ | V | |

- (1) The core supply should be powered up before, and powered down after, the I/O supply. Systems should be designed to ensure that neither supply is powered up for an extended period of time if the other supply is below the proper operating voltage.
- (2) Refers to dc (or steady state) currents only; actual switching currents are higher. For more details, see the device-specific IBIS models.
- (3) The absolute maximum ratings should not be exceeded for more than 30% of the cycle period.

Recommended Operating Conditions⁽¹⁾ (continued)

| | | MIN | NOM | MAX | UNIT |
|-----------------|--|-----------|-----|---------------------|------|
| V _{US} | Maximum voltage during undershoot (See Figure 11-5) | | | -0.7 ⁽³⁾ | V |
| T _C | Operating case temperature | A version | | 105 | °C |
| | | S version | -40 | 105 | |
| | | M version | -55 | 125 | |

11.3 Electrical Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating case temperature (unless otherwise noted)

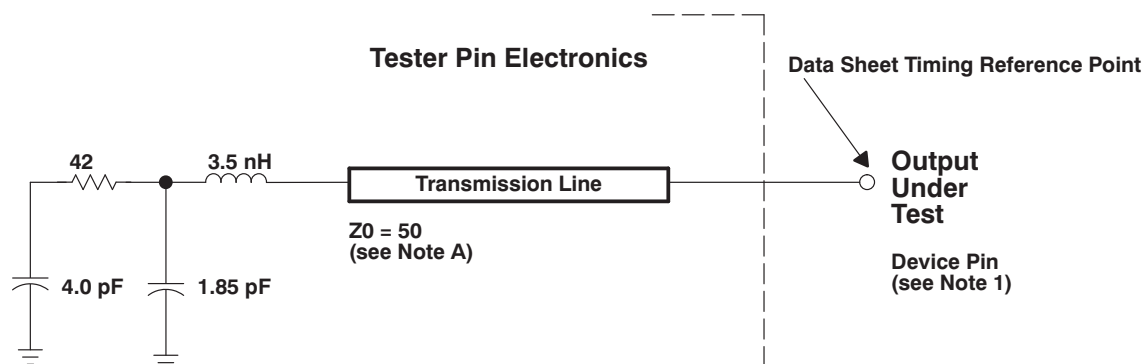
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------|------------------------------------|---|-----|-----|------|------|
| V _{OH} | High-level output voltage | All signals except SCL1, SDA1, SCL0, and SDA0 I _{OH} = MAX | 2.4 | | | V |
| V _{OL} | Low-level output voltage | All signals except SCL1, SDA1, SCL0, and SDA0 I _{OL} = MAX | | | 0.4 | V |
| | | SCL1, SDA1, SCL0, and SDA0 I _{OL} = MAX | | | 0.4 | |
| I _I | Input current | All signals except SCL1, SDA1, SCL0, and SDA0 V _I = V _{SS} to DV _{DD} | | | ±170 | µA |
| | | SCL1, SDA1, SCL0, and SDA0 | | | ±10 | |
| I _{OZ} | Off-state output current | All signals except SCL1, SDA1, SCL0, and SDA0 V _O = DV _{DD} or 0 V | | | ±170 | µA |
| | | SCL1, SDA1, SCL0, and SDA0 | | | ±10 | |
| I _{DD2V} | Core supply current ⁽²⁾ | 13GDPA, CV _{DD} = 1.4 V, CPU clock = 300 MHz | | 945 | | mA |
| | | 13GDPA, CV _{DD} = 1.26 V, CPU clock = 200 MHz | | 560 | | |
| I _{DD3V} | I/O supply current ⁽²⁾ | C6713/13B, DV _{DD} = 3.3 V, EMIF speed = 100 MHz | | 75 | | mA |
| C _I | Input capacitance | | | | 7 | pF |
| C _O | Output capacitance | | | | 7 | pF |

- (1) For test conditions shown as MIN, MAX, or NOM, use the appropriate value specified in the recommended operating conditions table.
 (2) Measured with average activity (50% high/50% low power) at 25°C case temperature and 100-MHz EMIF. This model represents a device performing high-DSP-activity operations 50% of the time, and the remainder performing low-DSP-activity operations. The high/low-DSP-activity models are defined as follows:
- High DSP activity model:
 - CPU: 8 instructions/cycle with 2 LDDW instructions [L1 data memory: 128 bits/cycle via LDDW instructions; L1 program memory: 256 bits/cycle; L2/EMIF EDMA: 50% writes, 50% reads to/from SDRAM (50% bit switching)]
 - McBSP: 2 channels at E1 rate
 - Timers: 2 timers at maximum rate
 - Low DSP activity model:
 - CPU: 2 instructions/cycle with 1 LDH instruction [L1 data memory: 16 bits/cycle; L1 program memory: 256 bits per 4 cycles; L2/EMIF EDMA: None]
 - McBSP: 2 channels at E1 rate
 - Timers: 2 timers at maximum rate

The actual current draw is highly application dependent. For more details on core and I/O activity, refer to the *TMS320C6713/12C/11C Power Consumption Summary* application report (literature number [SPRA889](#)).

11.4 Parameter Measurement Information

11.4.1 Timing Information



NOTE A: The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. A transmission line with a delay of 2 ns or longer can be used to produce the desired transmission line effect. The transmission line is intended as a load only. It is not necessary to add or subtract the transmission line delay (2 ns or longer) from the data-sheet timings.

Input requirements in this data sheet are tested with an input slew rate of <math><4\text{ V per nanosecond}</math> (4 V/ns) at the device pin.

Figure 11-1. Test Load Circuit for AC Timing Measurements

11.4.2 Signal Transition Levels

All input and output timing parameters are referenced to 1.5 V for both 0 and 1 logic levels.

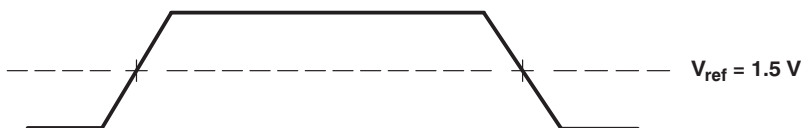


Figure 11-2. Input and Output Voltage Reference Levels for AC Timing Measurements

All rise and fall transition timing parameters are referenced to $V_{IL\text{ MAX}}$ and $V_{IH\text{ MIN}}$ for input clocks, $V_{OL\text{ MAX}}$ and $V_{OH\text{ MIN}}$ for output clocks.

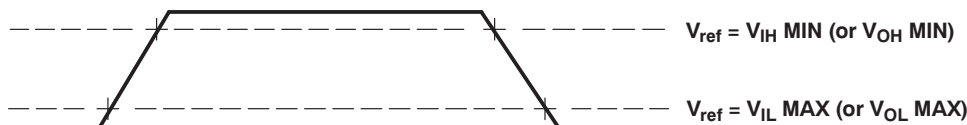
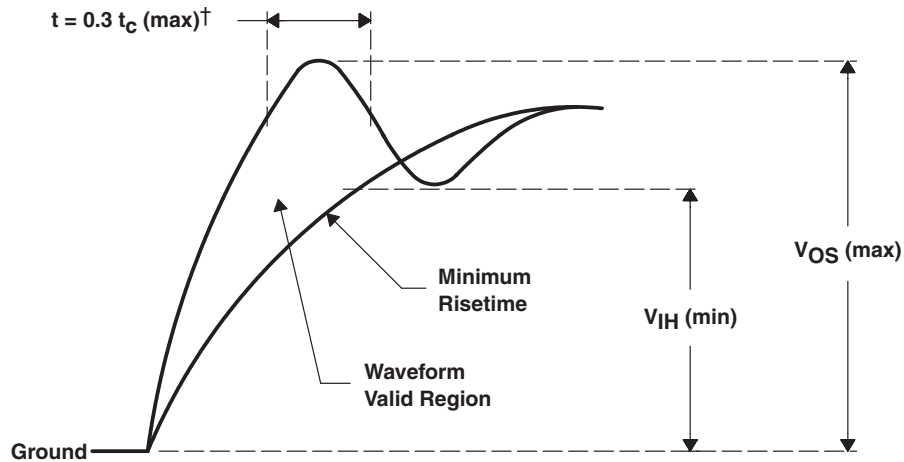


Figure 11-3. Rise and Fall Transition Time Voltage Reference Levels

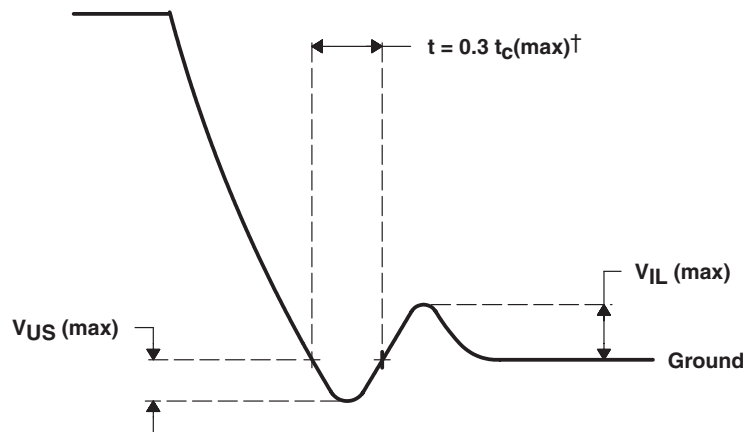
11.4.3 AC Transient Rise/Fall Time Specifications

Figure 11-4 and Figure 11-5 show the AC transient specifications for rise and fall time. For device-specific information on these values, refer to the Recommended Operating Conditions section of this data sheet.



$^\dagger t_C$ = the peripheral cycle time.

Figure 11-4. AC Transient Specification Rise Time



$^\dagger t_C$ = the peripheral cycle time.

Figure 11-5. AC Transient Specification Fall Time

11.4.4 Timing Parameters and Board Routing Analysis

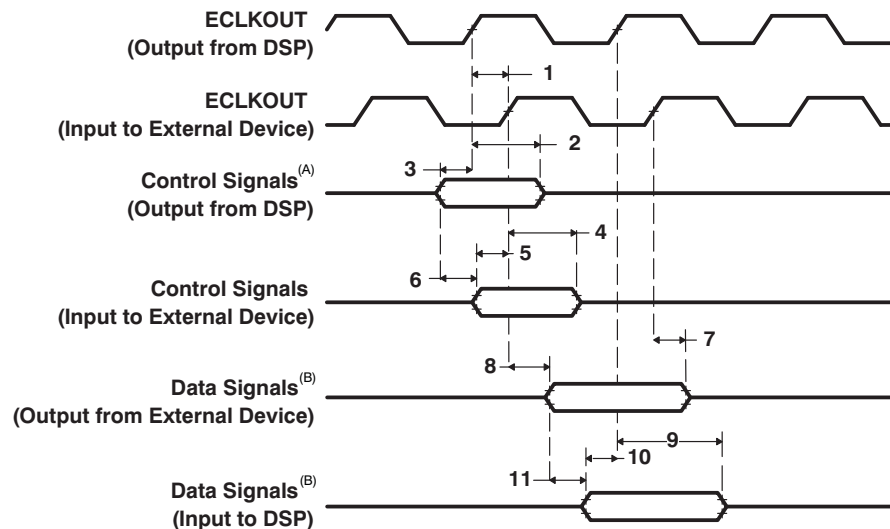
The timing parameter values specified in this data sheet do not include delays by board routings. As a good board design practice, such delays must always be taken into account. Timing values may be adjusted by increasing/decreasing such delays. TI recommends utilizing the available I/O buffer information specification (IBIS) models to analyze the timing characteristics correctly. To properly use IBIS models to attain accurate timing analysis for a given system, see the *Using IBIS Models for Timing Analysis* application report (literature number [SPRA839](#)). If needed, external logic hardware such as buffers may be used to compensate any timing differences.

For inputs, timing is most impacted by the round-trip propagation delay from the DSP to the external device and from the external device to the DSP. This round-trip delay tends to negatively impact the input setup time margin, but also tends to improve the input hold time margins (see [Table 11-1](#) and [Figure 11-6](#)).

[Figure 11-6](#) represents a general transfer between the DSP and an external device. The figure also represents board route delays and how they are perceived by the DSP and the external device.

Table 11-1. Board-Level Timings Example (see [Figure 11-6](#))

| NO. | DESCRIPTION |
|-----|--|
| 1 | Clock route delay |
| 2 | Minimum DSP hold time |
| 3 | Minimum DSP setup time |
| 4 | External device hold time requirement |
| 5 | External device setup time requirement |
| 6 | Control signal route delay |
| 7 | External device hold time |
| 8 | External device access time |
| 9 | DSP hold time requirement |
| 10 | DSP setup time requirement |
| 11 | Data route delay |



NOTES A: Control signals include data for writes.

B: Data signals are generated during reads from an external device.

Figure 11-6. Board-Level Input/Output Timings

11.5 Input and Output Clocks

Table 11-2. Timing Requirements for CLKIN^{(1) (2) (3)}

See [Figure 11-7](#)

| NO. | | | PLL MODE (PLEN = 1) | | BYPASS MODE (PLEN = 0) | | UNIT |
|-----|-----------------|----------------------------|------------------------|-----|---------------------------|------|------|
| | | | MIN | MAX | MIN | MAX | |
| 1 | $t_{c(CLKIN)}$ | Cycle time, CLKIN | GDP-200 | | 5 | 83.3 | ns |
| | | | GDP-300 | | 4 | 83.3 | |
| 2 | $t_{w(CLKINH)}$ | Pulse duration, CLKIN high | 0.4C | | 0.4C | | ns |
| 3 | $t_{w(CLKINL)}$ | Pulse duration, CLKIN low | 0.4C | | 0.4C | | ns |
| 4 | $t_t(CLKIN)$ | Transition time, CLKIN | | | 5 | 5 | ns |

- (1) The reference points for the rise and fall transitions are measured at V_{IL} MAX and V_{IH} MIN.
 (2) C = CLKIN cycle time in nanoseconds (ns). For example, when CLKIN frequency is 40 MHz, use C = 25 ns.
 (3) See the [PLL and PLL Controller](#) section of this data sheet.

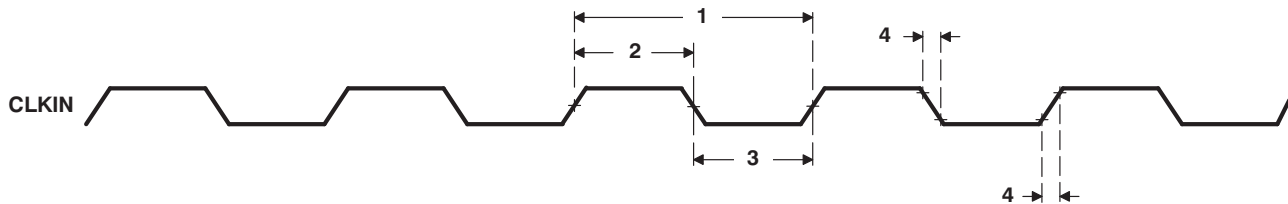


Figure 11-7. CLKIN

Table 11-3. Switching Characteristics for CLKOUT2^{(1) (2)}

over recommended operating conditions (see [Figure 11-8](#))

| NO. | PARAMETER | MIN | MAX | UNIT |
|-----|---|--------------|--------------|------|
| 1 | $t_{c(CKO2)}$ Cycle time, CLKOUT2 | C2 – 0.8 | C2 + 0.8 | ns |
| 2 | $t_{w(CKO2H)}$ Pulse duration, CLKOUT2 high | (C2/2) – 0.8 | (C2/2) + 0.8 | ns |
| 3 | $t_{w(CKO2L)}$ Pulse duration, CLKOUT2 low | (C2/2) – 0.8 | (C2/2) + 0.8 | ns |
| 4 | $t_t(CKO2)$ Transition time, CLKOUT2 | 2 | | ns |

- (1) The reference points for the rise and fall transitions are measured at V_{OL} MAX and V_{OH} MIN.
 (2) C2 = CLKOUT2 period in ns. CLKOUT2 period is determined by the PLL controller output SYSCLK2 period, which **must** be set to CPU period divide-by-2.

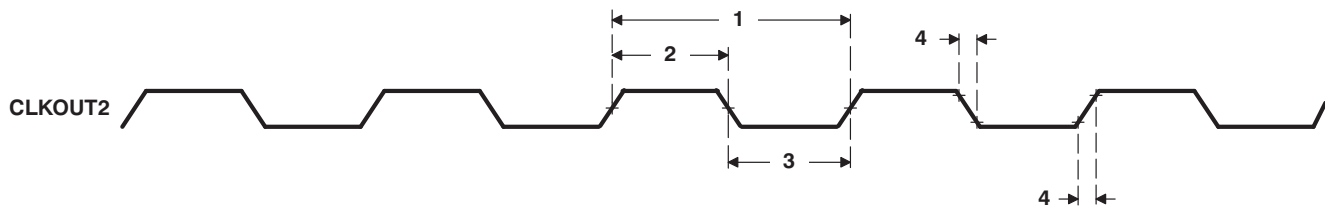


Figure 11-8. CLKOUT2

Table 11-4. Switching Characteristics for CLKOUT3^{(1) (2)}

over recommended operating conditions (see [Figure 11-9](#))

| NO. | PARAMETER | 6713 | | 6713B | | UNIT |
|-----|---|----------------|----------------|----------------|----------------|------|
| | | MIN | MAX | MIN | MAX | |
| 1 | $t_{c(CKO3)}$ Cycle time, CLKOUT3 | $C3 - 0.6$ | $C3 + 0.6$ | $C3 - 0.9$ | $C3 + 0.9$ | ns |
| 2 | $t_{w(CKO3H)}$ Pulse duration, CLKOUT3 high | $(C3/2) - 0.6$ | $(C3/2) + 0.6$ | $(C3/2) - 0.9$ | $(C3/2) + 0.9$ | ns |
| 3 | $t_{w(CKO3L)}$ Pulse duration, CLKOUT3 low | $(C3/2) - 0.6$ | $(C3/2) + 0.6$ | $(C3/2) - 0.9$ | $(C3/2) + 0.9$ | ns |
| 4 | $t_{t(CKO3)}$ Transition time, CLKOUT3 | | 2 | | 3 | ns |
| 5 | $t_{d(CLKINH-CKO3V)}$ Delay time, CLKIN high to CLKOUT3 valid | 1.5 | 6.5 | 1.5 | 7.5 | ns |

(1) The reference points for the rise and fall transitions are measured at V_{OL} MAX and V_{OH} MIN.

(2) C3 = CLKOUT3 period in ns. CLKOUT3 period is a divide-down of the CPU clock, configurable via the RATIO field in the PLLDIV3 register.

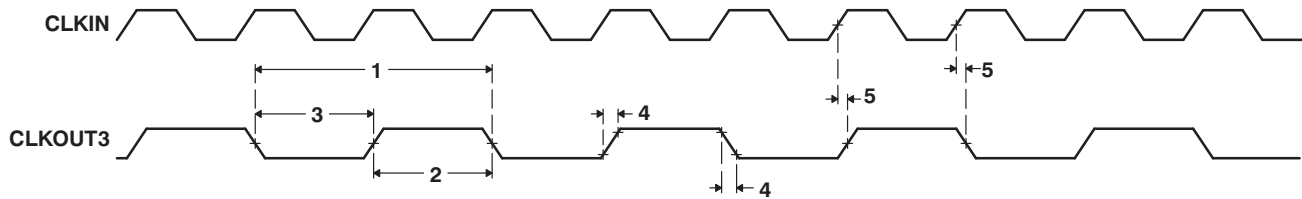


Figure 11-9. CLKOUT3

Table 11-5. Timing Requirements for ECLKIN⁽¹⁾

See [Figure 11-10](#)

| NO. | PARAMETER | MIN | MAX | UNIT |
|-----|---|-----|-----|------|
| 1 | $t_{c(EKI)}$ Cycle time, ECLKIN | 10 | | ns |
| 2 | $t_{w(EKIH)}$ Pulse duration, ECLKIN high | 4.5 | | ns |
| 3 | $t_{w(EKIL)}$ Pulse duration, ECLKIN low | 4.5 | | ns |
| 4 | $t_{t(EKI)}$ Transition time, ECLKIN | | 3 | ns |

(1) The reference points for the rise and fall transitions are measured at V_{IL} MAX and V_{IH} MIN.

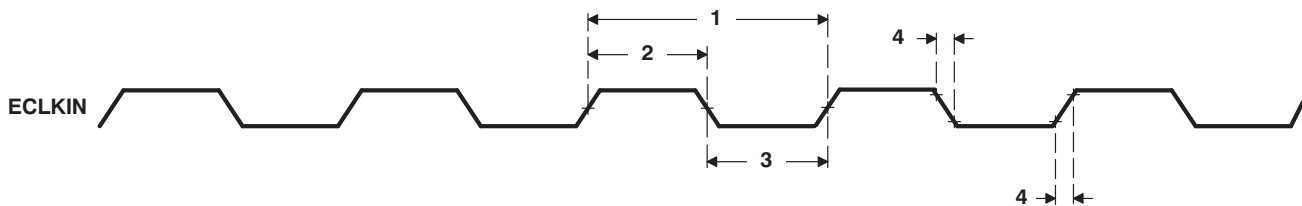


Figure 11-10. ECLKIN

Table 11-6. Switching Characteristics for ECLKOUT^{(1) (2) (3)}

over recommended operating conditions (see [Figure 11-11](#))

| NO. | PARAMETER | | MIN | MAX | UNIT |
|-----|-------------------|---|----------|----------|------|
| 1 | t_c (EKO) | Cycle time, ECLKOUT | E – 0.9 | E + 0.9 | ns |
| 2 | t_w (EKOH) | Pulse duration, ECLKOUT high | EH – 0.9 | EH + 0.9 | ns |
| 3 | t_w (EKOL) | Pulse duration, ECLKOUT low | EL – 0.9 | EL + 0.9 | ns |
| 4 | t_t (EKO) | Transition time, ECLKOUT | | 2 | ns |
| 5 | t_d (EKIH-EKOH) | Delay time, ECLKIN high to ECLKOUT high | 1 | 6.5 | ns |
| 6 | t_d (EKIL-EKOL) | Delay time, ECLKIN low to ECLKOUT low | 1 | 6.5 | ns |

(1) The reference points for the rise and fall transitions are measured at V_{OL} MAX and V_{OH} MIN.

(2) E = ECLKIN period in ns

(3) EH is the high period of ECLKIN in ns and EL is the low period of ECLKIN in ns.

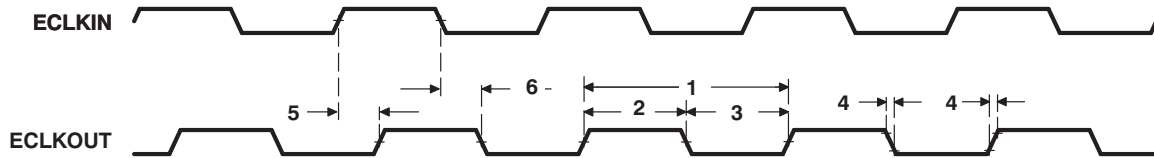


Figure 11-11. ECLKOUT

11.6 Asynchronous Memory Timing

Table 11-7. Timing Requirements for Asynchronous Memory Cycles^{(1) (2) (3)}

See Figure 11-12 and Figure 11-13

| NO. | | MIN | MAX | UNIT |
|-----|---|-----|-----|------|
| 3 | $t_{su(EDV-AREH)}$ Setup time, EDx valid before \overline{ARE} high | 6.5 | | ns |
| 4 | $t_{h(AREH-EDV)}$ Hold time, EDx valid after \overline{ARE} high | 1 | | ns |
| 6 | $t_{su(ARDY-EKOH)}$ Setup time, ARDY valid before ECLKOUT high | 3 | | ns |
| 7 | $t_{h(EKOH-ARDY)}$ ARDY valid after ECLKOUT high | 2.3 | | ns |

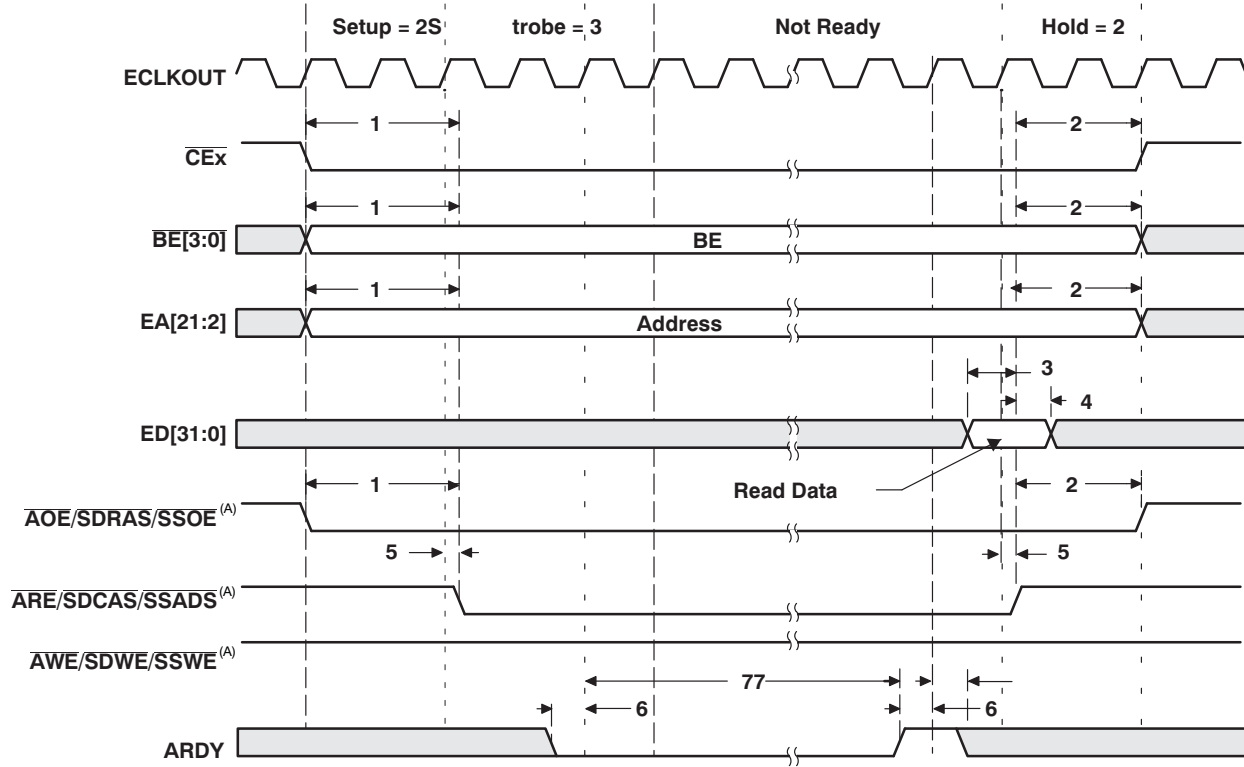
- (1) To ensure data setup time, simply program the strobe width wide enough. ARDY is internally synchronized. The ARDY signal is recognized in the cycle for which the setup and hold time is met. To use ARDY as an asynchronous input, the pulse width of the ARDY signal should be wide enough (for example, pulse width = 2E) to ensure setup and hold time is met.
- (2) RS = Read setup, RST = Read strobe, RH = Read hold, WS = Write setup, WST = Write strobe, WH = Write hold. These parameters are programmed via the EMIF CE space control registers.
- (3) E = ECLKOUT period in ns

Table 11-8. Switching Characteristics for Asynchronous Memory Cycles^{(1) (2) (3)}

over recommended operating condition (see Figure 11-12 and Figure 11-13)

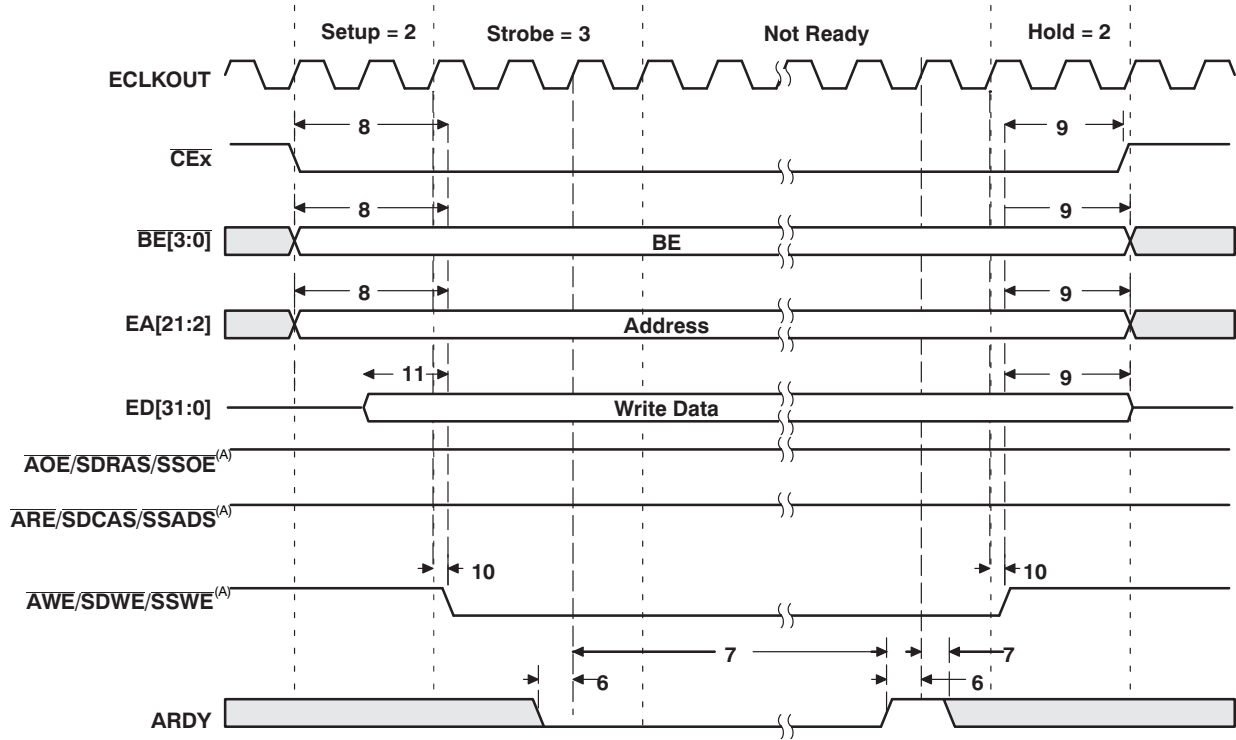
| NO. | PARAMETER | MIN | MAX | UNIT |
|-----|--|------------------|-----|------|
| 1 | $t_{osu(SELV-AREL)}$ Output setup time, select signals valid to \overline{ARE} low | RS*E – 1.7 | | ns |
| 2 | $t_{oh(AREH-SELIV)}$ Output hold time, \overline{ARE} high to select signals invalid | RH*E – 1.7 | | ns |
| 5 | $t_d(EKOH-AREV)$ Delay time, ECLKOUT high to \overline{ARE} valid | 1.5 | 7 | ns |
| 8 | $t_{osu(SELV-AWEL)}$ Output setup time, select signals valid to \overline{AWE} low | WS*E – 1.7 | | ns |
| 9 | $t_{oh(AWEH-SELIV)}$ Output hold time, \overline{AWE} high to select signals and EDx invalid | WH*E – 1.7 | | ns |
| 10 | $t_d(EKOH-AWEV)$ Delay time, ECLKOUT high to \overline{AWE} valid | 1.5 | 7 | ns |
| 11 | $t_{osu(EDV-AWEL)}$ Output setup time, ED valid to \overline{AWE} low | (WS – 1)*E – 1.7 | | ns |

- (1) RS = Read setup, RST = Read strobe, RH = Read hold, WS = Write setup, WST = Write strobe, WH = Write hold. These parameters are programmed via the EMIF CE space control registers.
- (2) E = ECLKOUT period in ns
- (3) Select signals include \overline{CEx} , $\overline{BE}[3:0]$, EA[21:2], and \overline{AOE} .



NOTE A: $\overline{\text{AOE}}/\overline{\text{SDRAS}}/\overline{\text{SSOE}}$, $\overline{\text{ARE}}/\overline{\text{SDCAS}}/\overline{\text{SSADS}}$, and $\overline{\text{AWE}}/\overline{\text{SDWE}}/\overline{\text{SSWE}}$ operate as $\overline{\text{AOE}}$ (identified under select signals), $\overline{\text{ARE}}$, and $\overline{\text{AWE}}$, respectively, during asynchronous memory accesses.

Figure 11-12. Asynchronous Memory Read



NOTE A: $\overline{AOE}/\overline{SDRAS}/\overline{SSOE}$, $\overline{ARE}/\overline{SDCAS}/\overline{SSADS}$, and $\overline{AWE}/\overline{SDWE}/\overline{SSWE}$ operate as \overline{AOE} (identified under select signals), \overline{ARE} , and \overline{AWE} , respectively, during asynchronous memory accesses.

Figure 11-13. Asynchronous Memory Write

11.7 Synchronous-Burst Memory Timing

Table 11-9. Timing Requirements for Synchronous-Burst SRAM Cycles⁽¹⁾

See [Figure 11-14](#)

| NO. | | MIN | MAX | UNIT |
|-----|---|-----|-----|------|
| 6 | $t_{su(EDV-EKOH)}$ Setup time, read EDx valid before ECLKOUT high | 1.5 | | ns |
| 7 | $t_{h(EKOH-EDV)}$ Hold time, read EDx valid after ECLKOUT high | 2.5 | | ns |

(1) The C6713/13B SBSRAM interface takes advantage of the internal burst counter in the SBSRAM. Accesses default to incrementing 4-word bursts, but random bursts and decrementing bursts are done by interrupting bursts in progress. All burst types can sustain continuous data flow.

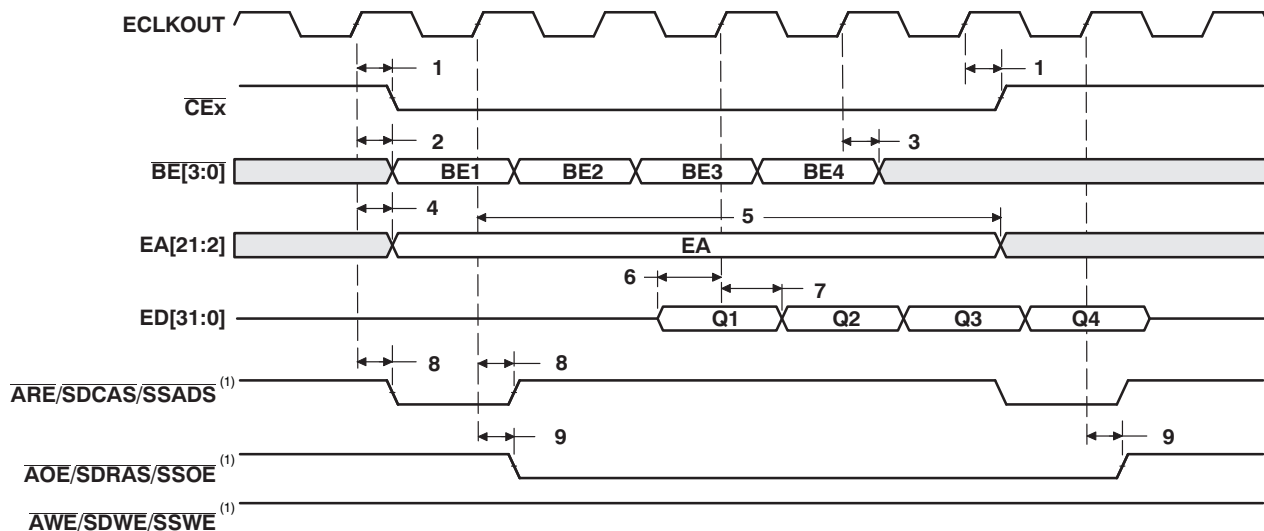
Table 11-10. Switching Characteristics for Synchronous-Burst SRAM Cycles^{(1) (2)}

over recommended operating conditions (see [Figure 11-14](#) and [Figure 11-15](#))

| NO. | PARAMETER | MIN | MAX | UNIT |
|-----|---|-----|-----|------|
| 1 | $t_d(EKOH-CEV)$ Delay time, ECLKOUT high to \overline{CEx} valid | 1.2 | 7 | ns |
| 2 | $t_d(EKOH-BEV)$ Delay time, ECLKOUT high to \overline{BEx} valid | | 7 | ns |
| 3 | $t_d(EKOH-BEIV)$ Delay time, ECLKOUT high to \overline{BEx} invalid | 1.2 | | ns |
| 4 | $t_d(EKOH-EAV)$ Delay time, ECLKOUT high to EAx valid | | 7 | ns |
| 5 | $t_d(EKOH-EAIV)$ Delay time, ECLKOUT high to EAx invalid | 1.2 | | ns |
| 8 | $t_d(EKOH-ADSV)$ Delay time, ECLKOUT high to $\overline{ARE}/\overline{SDCAS}/\overline{SSADS}$ valid | 1.2 | 7 | ns |
| 9 | $t_d(EKOH-OEV)$ Delay time, ECLKOUT high to $\overline{AOE}/\overline{SDRAS}/\overline{SSOE}$ valid | 1.2 | 7 | ns |
| 10 | $t_d(EKOH-EDV)$ Delay time, ECLKOUT high to \overline{EDx} valid | | 7 | ns |
| 11 | $t_d(EKOH-EDIV)$ Delay time, ECLKOUT high to \overline{EDx} invalid | 1.2 | | ns |
| 12 | $t_d(EKOH-WEV)$ Delay time, ECLKOUT high to $\overline{AWE}/\overline{SDWE}/\overline{SSWE}$ valid | 1.2 | 7 | ns |

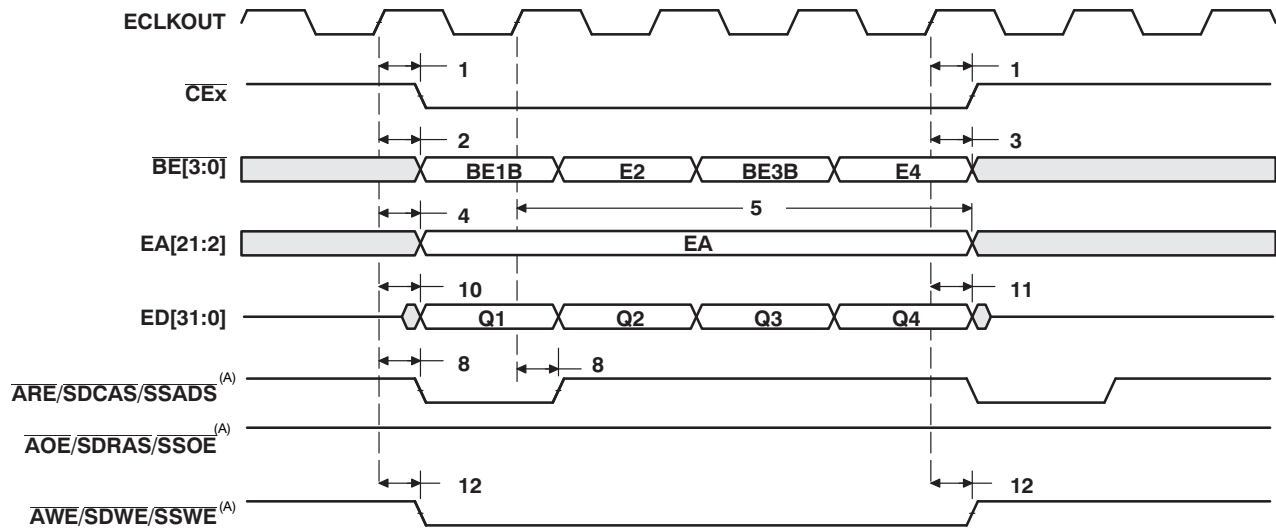
(1) The C6713/13B SBSRAM interface takes advantage of the internal burst counter in the SBSRAM. Accesses default to incrementing 4-word bursts, but random bursts and decrementing bursts are done by interrupting bursts in progress. All burst types can sustain continuous data flow.

(2) $\overline{ARE}/\overline{SDCAS}/\overline{SSADS}$, $\overline{AOE}/\overline{SDRAS}/\overline{SSOE}$, and $\overline{AWE}/\overline{SDWE}/\overline{SSWE}$ operate as \overline{SSADS} , \overline{SSOE} , and \overline{SSWE} , respectively, during SBSRAM accesses.



NOTE (1): $\overline{ARE}/\overline{SDCAS}/\overline{SSADS}$, $\overline{AOE}/\overline{SDRAS}/\overline{SSOE}$, and $\overline{AWE}/\overline{SDWE}/\overline{SSWE}$ operate as \overline{SSADS} , \overline{SSOE} , and \overline{SSWE} , respectively, during SBSRAM accesses.

Figure 11-14. SBSRAM Read Timing



NOTE A: $\overline{\text{ARE}}/\text{SDCAS}/\text{SSADS}$, $\overline{\text{AOE}}/\text{SDRAS}/\text{SSOE}$, and $\overline{\text{AWE}}/\text{SDWE}/\text{SSWE}$ operate as $\overline{\text{SSADS}}$, $\overline{\text{SSOE}}$, and $\overline{\text{SSWE}}$, respectively, during SBSRAM accesses.

Figure 11-15. SBSRAM Write Timing

11.8 Synchronous DRAM Timing

Table 11-11. Timing Requirements for Synchronous DRAM Cycles⁽¹⁾

See Figure 11-16

| NO. | | MIN | MAX | UNIT |
|-----|--|-----|-----|------|
| 6 | $t_{su}(\text{EDV-EKOH})$ Setup time, read EDx valid before ECLKOUT high | 1.5 | | ns |
| 7 | $t_h(\text{EKOH-EDV})$ Hold time, read EDx valid after ECLKOUT high | 2.5 | | ns |

(1) The C6713/13B SDRAM interface takes advantage of the internal burst counter in the SDRAM. Accesses default to incrementing 4-word bursts, but random bursts and decrementing bursts are done by interrupting bursts in progress. All burst types can sustain continuous data flow.

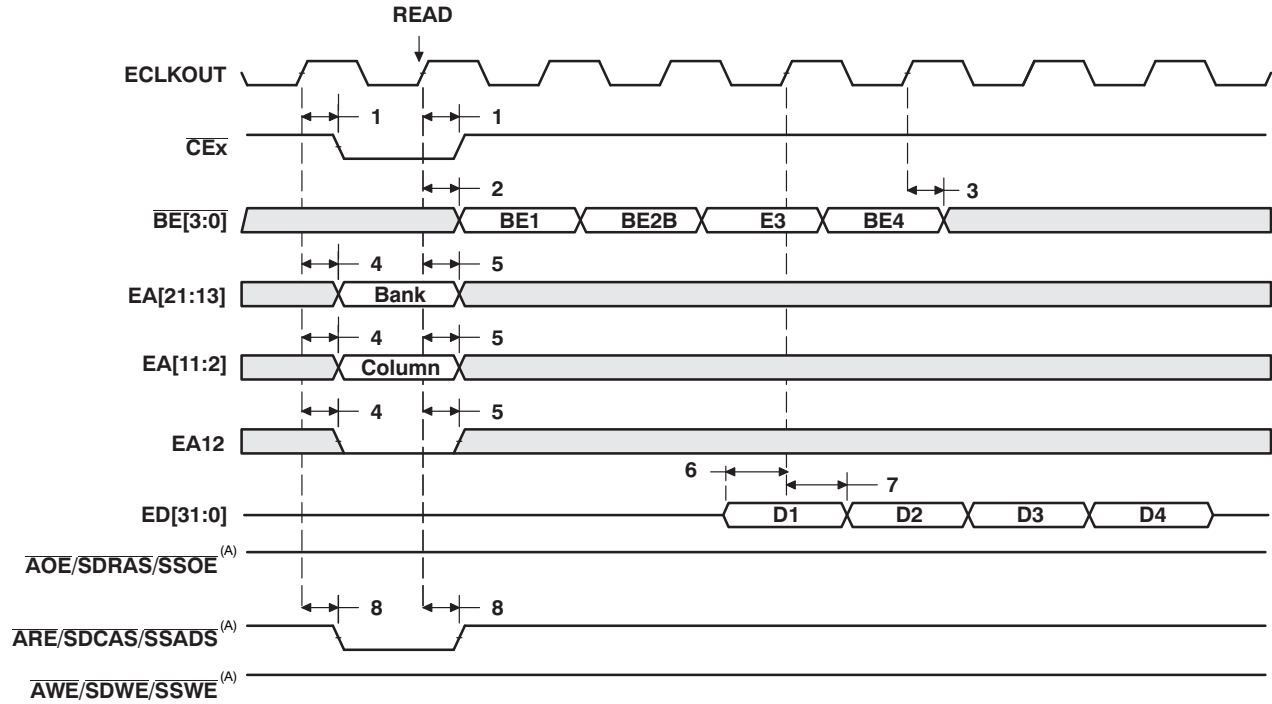
Table 11-12. Switching Characteristics for Synchronous DRAM Cycles^{(1) (2)}

over recommended operating conditions (see Figure 11-16— Figure 11-22)

| NO. | PARAMETER | MIN | MAX | UNIT |
|-----|---|-----|-----|------|
| 1 | $t_d(\text{EKOH-CEV})$ Delay time, ECLKOUT high to $\overline{\text{CE}}_x$ valid | 1.5 | 7 | ns |
| 2 | $t_d(\text{EKOH-BEV})$ Delay time, ECLKOUT high to $\overline{\text{BE}}_x$ valid | | 7 | ns |
| 3 | $t_d(\text{EKOH-BEIV})$ Delay time, ECLKOUT high to $\overline{\text{BE}}_x$ invalid | 1.5 | | ns |
| 4 | $t_d(\text{EKOH-EAV})$ Delay time, ECLKOUT high to EAx valid | | 7 | ns |
| 5 | $t_d(\text{EKOH-EAIV})$ Delay time, ECLKOUT high to EAx invalid | 1.5 | | ns |
| 8 | $t_d(\text{EKOH-CASV})$ Delay time, ECLKOUT high to $\overline{\text{ARE}}/\text{SDCAS}/\text{SSADS}$ valid | 1.5 | 7 | ns |
| 9 | $t_d(\text{EKOH-EDV})$ Delay time, ECLKOUT high to $\overline{\text{ED}}_x$ valid | | 7 | ns |
| 10 | $t_d(\text{EKOH-EDIV})$ Delay time, ECLKOUT high to $\overline{\text{ED}}_x$ invalid | 1.5 | | ns |
| 11 | $t_d(\text{EKOH-WEV})$ Delay time, ECLKOUT high to $\overline{\text{AWE}}/\text{SDWE}/\text{SSWE}$ valid | 1.5 | 7 | ns |
| 12 | $t_d(\text{EKOH-RAV})$ Delay time, ECLKOUT high to $\overline{\text{AOE}}/\text{SDRAS}/\text{SSOE}$ valid | 1.5 | 7 | ns |

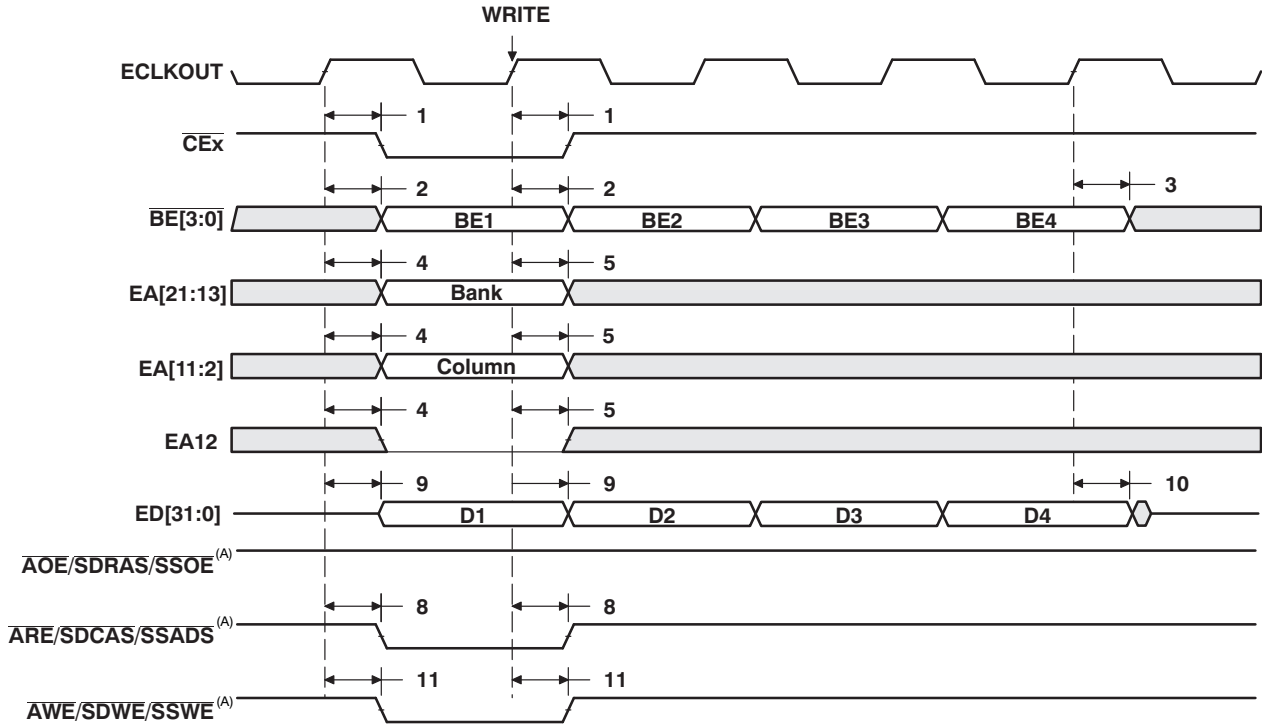
(1) The C6713/13B SDRAM interface takes advantage of the internal burst counter in the SDRAM. Accesses default to incrementing 4-word bursts, but random bursts and decrementing bursts are done by interrupting bursts in progress. All burst types can sustain continuous data flow.

(2) $\overline{\text{ARE}}/\text{SDCAS}/\text{SSADS}$, $\overline{\text{AWE}}/\text{SDWE}/\text{SSWE}$ and $\overline{\text{AOE}}/\text{SDRAS}/\text{SSOE}$ operate as $\overline{\text{SDCAS}}$, $\overline{\text{SWE}}$, and $\overline{\text{SDRAS}}$, respectively, during SDRAM accesses.



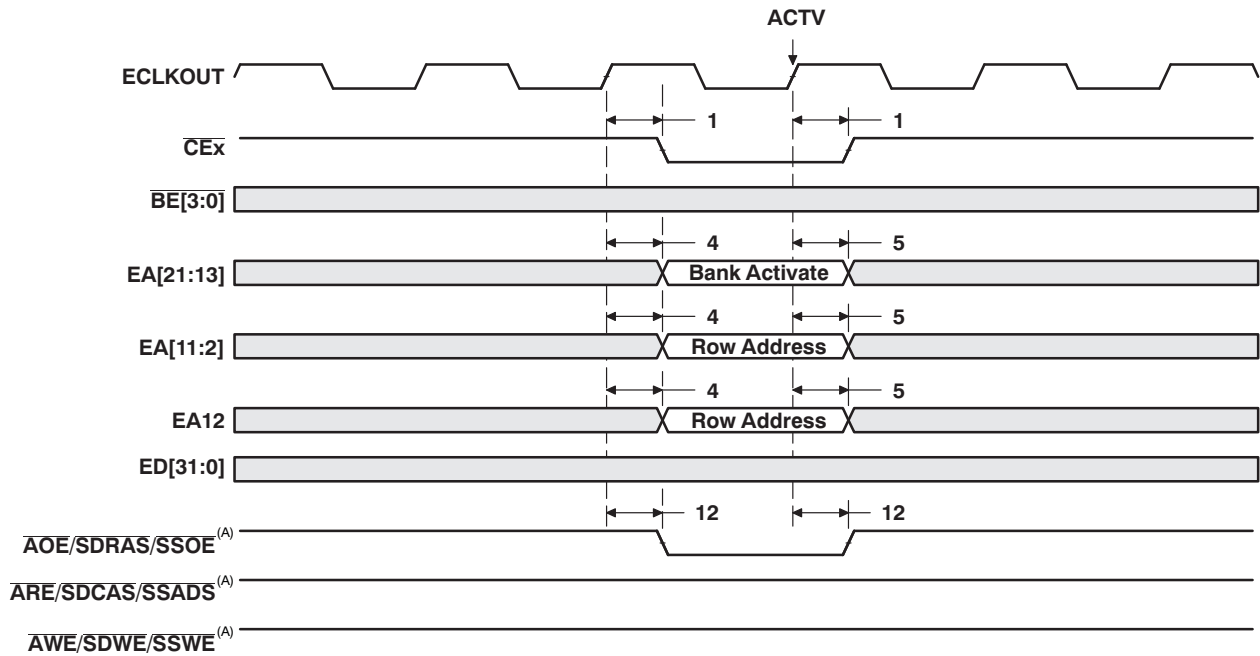
NOTE A: $\overline{\text{ARE}}/\overline{\text{SDCAS}}/\overline{\text{SSADS}}$, $\overline{\text{AWE}}/\overline{\text{SDWE}}/\overline{\text{SSWE}}$, and $\overline{\text{AOE}}/\overline{\text{SDRAS}}/\overline{\text{SSOE}}$ operate as $\overline{\text{SDCAS}}$, $\overline{\text{SDWE}}$, and $\overline{\text{SDRAS}}$, respectively, during SDRAM accesses.

Figure 11-16. SDRAM Read Command (CAS Latency 3)



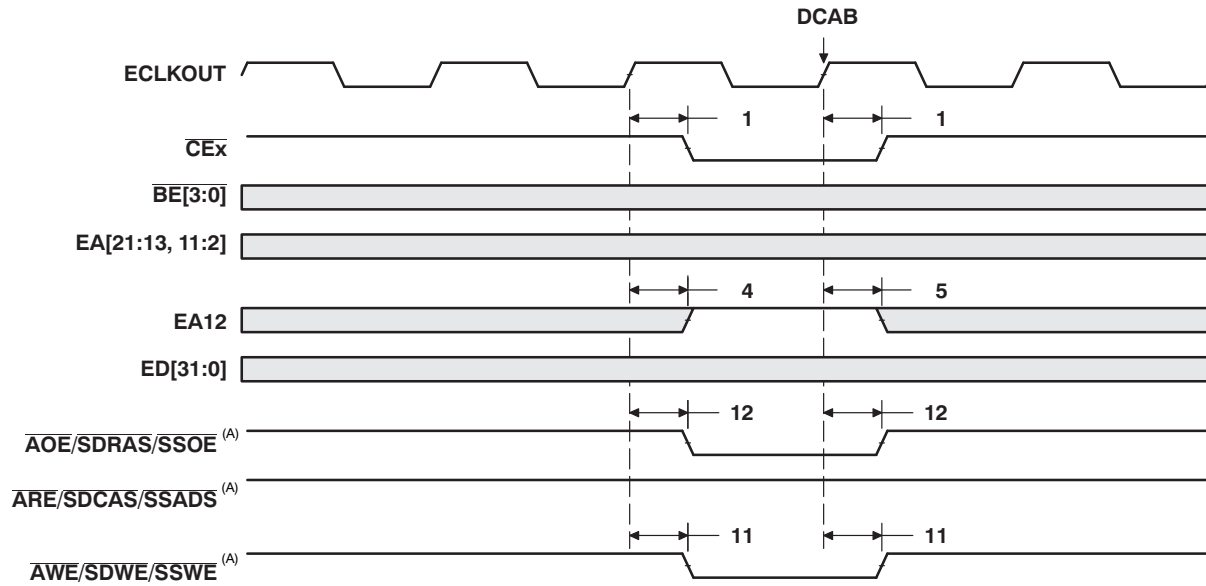
NOTE A: $\overline{\text{ARE}}/\text{SDCAS}/\text{SSADS}$, $\overline{\text{AWE}}/\text{SDWE}/\text{SSWE}$, and $\overline{\text{AOE}}/\text{SDRAS}/\text{SSOE}$ operate as SDCAS , SDWE , and SDRAS , respectively, during SDRAM accesses.

Figure 11-17. SDRAM Write Command



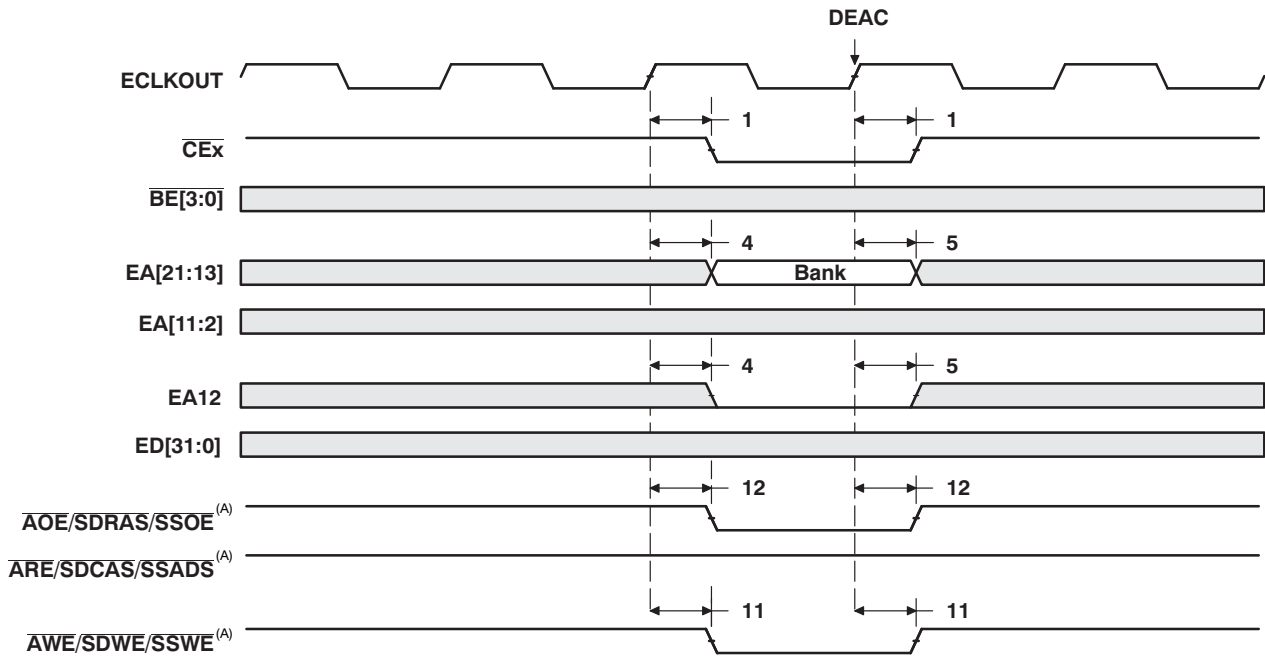
NOTE A: $\overline{\text{ARE}}/\text{SDCAS}/\text{SSADS}$, $\overline{\text{AWE}}/\text{SDWE}/\text{SSWE}$, and $\overline{\text{AOE}}/\text{SDRAS}/\text{SSOE}$ operate as SDCAS , SDWE , and SDRAS , respectively, during SDRAM accesses.

Figure 11-18. SDRAM ACTV Command



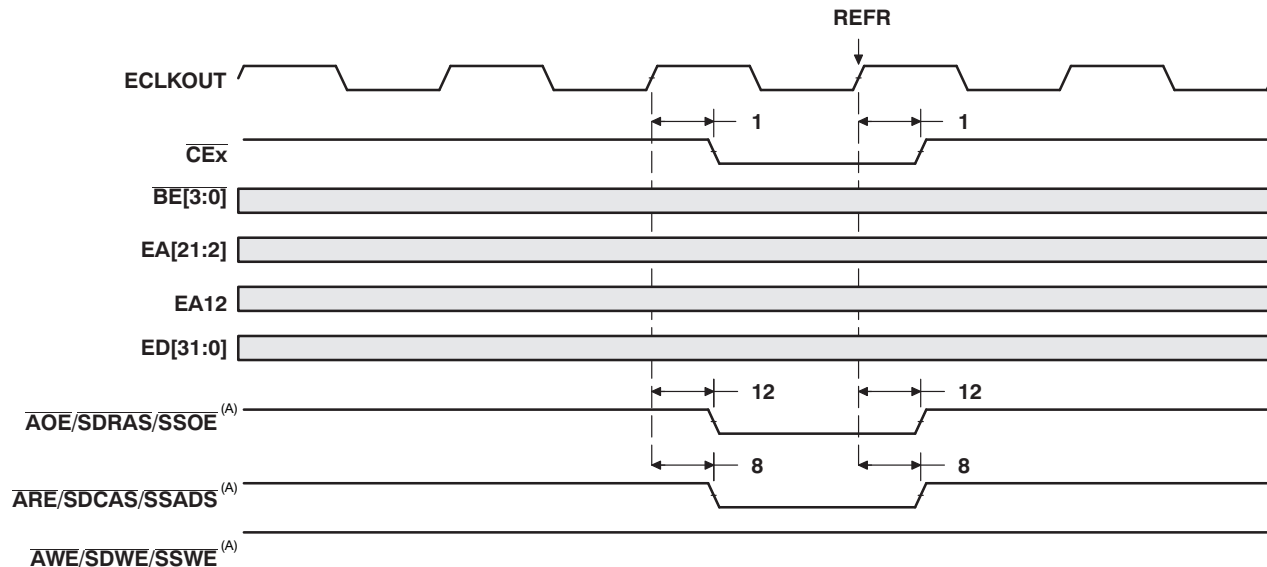
NOTE A: $\overline{\text{ARE}}/\text{SDCAS}/\text{SSADS}$, $\overline{\text{AWE}}/\text{SDWE}/\text{SSWE}$, and $\overline{\text{AOE}}/\text{SDRAS}/\text{SSOE}$ operate as SDCAS , SDWE , and SDRAS , respectively, during SDRAM accesses.

Figure 11-19. SDRAM DCAB Command



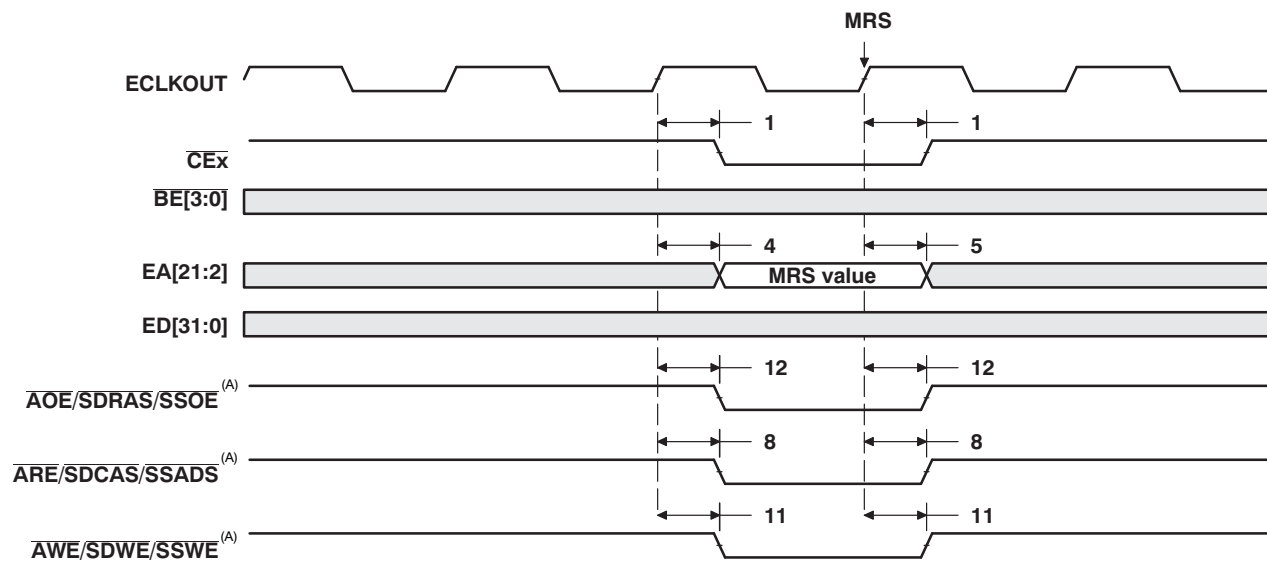
NOTE A: $\overline{\text{ARE}}/\text{SDCAS}/\text{SSADS}$, $\overline{\text{AWE}}/\text{SDWE}/\text{SSWE}$, and $\overline{\text{AOE}}/\text{SDRAS}/\text{SSOE}$ operate as SDCAS , SDWE , and SDRAS , respectively, during SDRAM accesses.

Figure 11-20. SDRAM DEAC Command



NOTE A: $\overline{ARE/SDCAS/SSADS}$, $\overline{AWE/SDWE/SSWE}$, and $\overline{AOE/SDRAS/SSOE}$ operate as \overline{SDCAS} , \overline{SDWE} , and \overline{SDRAS} , respectively, during SDRAM accesses.

Figure 11-21. SDRAM REFR Command



NOTE A: $\overline{ARE/SDCAS/SSADS}$, $\overline{AWE/SDWE/SSWE}$, and $\overline{AOE/SDRAS/SSOE}$ operate as \overline{SDCAS} , \overline{SDWE} , and \overline{SDRAS} , respectively, during SDRAM accesses.

Figure 11-22. SDRAM MRS Command

11.9 HOLD/HOLDA Timing

Table 11-13. Timing Requirements for $\overline{\text{HOLD}}/\overline{\text{HOLDA}}$ Cycles⁽¹⁾

See [Figure 11-23](#)

| NO. | PARAMETER | MIN | MAX | UNIT |
|-----|---|-----|-----|------|
| 3 | $t_{h(\overline{\text{HOLDAL}}-\overline{\text{HOLDL}})}$ Hold time, $\overline{\text{HOLD}}$ low after $\overline{\text{HOLDA}}$ low | E | | ns |

(1) E = ECLKOUT period in ns

Table 11-14. Switching Characteristics for $\overline{\text{HOLD}}/\overline{\text{HOLDA}}$ Cycles^{(1) (2)}

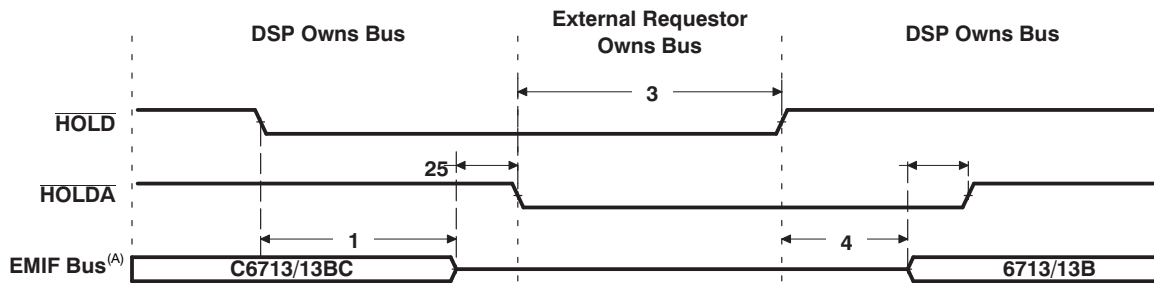
over recommended operating conditions (see [Figure 11-23](#))

| NO. | PARAMETER | 6713 | | 6713B | | UNIT |
|-----|--|------|----------------|-------|----------------|------|
| | | MIN | MAX | MIN | MAX | |
| 1 | $t_{d(\overline{\text{HOLDL}}-\text{EMHZ})}$ Delay time, $\overline{\text{HOLD}}$ low to EMIF Bus high impedance | 2E | ⁽³⁾ | 2E | ⁽³⁾ | ns |
| 2 | $t_{d(\text{EMHZ}-\overline{\text{HOLDAL}})}$ Delay time, EMIF Bus high impedance to $\overline{\text{HOLDA}}$ low | -0.1 | 2E | 0 | 2E | ns |
| 4 | $t_{d(\overline{\text{HOLDH}}-\text{EMLZ})}$ Delay time, $\overline{\text{HOLD}}$ high to EMIF Bus low impedance | 2E | 7E | 2E | 7E | ns |
| 5 | $t_{d(\text{EMLZ}-\overline{\text{HOLDAH}})}$ Delay time, EMIF Bus low impedance to $\overline{\text{HOLDA}}$ high | -1.5 | 2E | 0 | 2E | ns |

(1) E = ECLKOUT period in ns

(2) EMIF bus consists of $\overline{\text{CE}}[3:0]$, $\overline{\text{BE}}[3:0]$, $\overline{\text{ED}}[31:0]$, $\overline{\text{EA}}[21:2]$, $\overline{\text{ARE}}/\overline{\text{SDCAS}}/\overline{\text{SSADS}}$, $\overline{\text{AOE}}/\overline{\text{SDRAS}}/\overline{\text{SSOE}}$, and $\overline{\text{AWE}}/\overline{\text{SDWE}}/\overline{\text{SSWE}}$.

(3) All pending EMIF transactions are allowed to complete before $\overline{\text{HOLDA}}$ is asserted. If no bus transactions are occurring, then the minimum delay time can be achieved. Also, bus hold can be indefinitely delayed by setting $\text{NOHOLD} = 1$.



NOTE A: EMIF bus consists of $\overline{\text{CE}}[3:0]$, $\overline{\text{BE}}[3:0]$, $\overline{\text{ED}}[31:0]$, $\overline{\text{EA}}[21:2]$, $\overline{\text{ARE}}/\overline{\text{SDCAS}}/\overline{\text{SSADS}}$, $\overline{\text{AWE}}/\overline{\text{SDWE}}/\overline{\text{SSWE}}$, and $\overline{\text{AOE}}/\overline{\text{SDRAS}}/\overline{\text{SSOE}}$.

Figure 11-23. $\overline{\text{HOLD}}/\overline{\text{HOLDA}}$ Timing

11.10 BUSREQ Timing

Table 11-15. Switching Characteristics for BUSREQ Cycles

over recommended operating conditions (see [Figure 11-24](#))

| NO. | PARAMETER | MIN | MAX | UNIT |
|-----|--|-----|-----|------|
| 1 | $t_{d(\text{EKOH}-\text{BUSRV})}$ Delay time, ECLKOUT high to BUSREQ valid | 1.5 | 7.2 | ns |

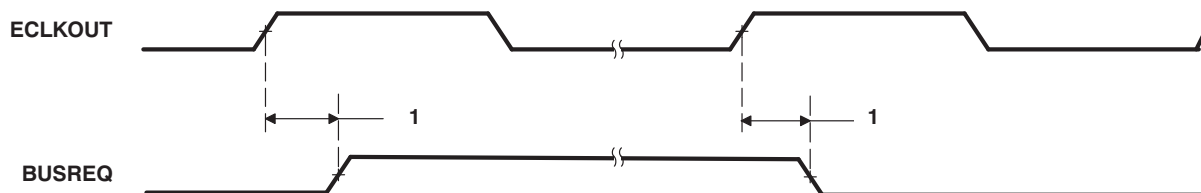


Figure 11-24. BUSREQ

11.11 Reset Timing

Table 11-16. Timing Requirements for $\overline{\text{RESET}}$ (1) (2)

See Figure 11-25

| NO. | | MIN | MAX | UNIT |
|-----|---|-----|-----|------|
| 1 | $t_{w(\text{RST})}$ Pulse duration, $\overline{\text{RESET}}$ | 100 | | ns |
| 13 | $t_{su(\text{HD})}$ Setup time, HD boot configuration bits valid before $\overline{\text{RESET}}$ high ⁽³⁾ | 2P | | ns |
| 14 | $t_{h(\text{HD})}$ Hold time, HD boot configuration bits valid after $\overline{\text{RESET}}$ high ⁽³⁾ | 2P | | ns |

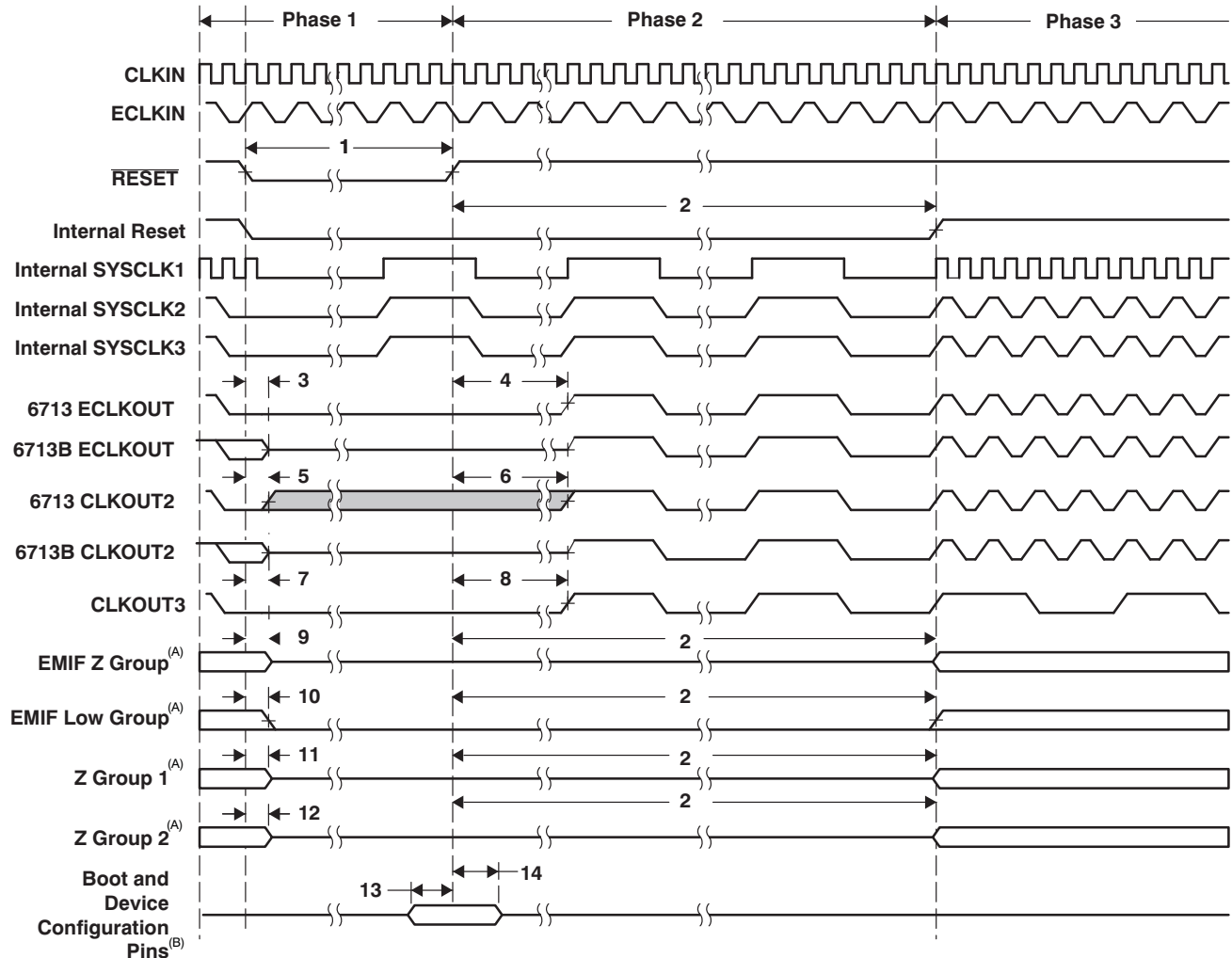
- (1) $P = 1/\text{CPU clock frequency}$ in ns. For example, when running parts at 300 MHz, use $P = 3.3$ ns.
- (2) For the C6713/13B device, the PLL is bypassed immediately after the device comes out of reset. The PLL controller can be programmed to change the PLL mode in software. For more detailed information on the PLL controller, see the *TMS320C6000 DSP Phase-Lock Loop (PLL) Controller Peripheral Reference Guide* (literature number [SPRU233](#)).
- (3) The boot and device configurations bits are latched asynchronously when $\overline{\text{RESET}}$ is transitioning high. The boot and device configurations bits consist of HD[14, 8, 4:3].

Table 11-17. Switching Characteristics For $\overline{\text{RESET}}$ (1)

over recommended operating conditions (see Figure 11-25)

| NO. | PARAMETER | | MIN | MAX | UNIT |
|-----|----------------------------|---|--------------------|-----|------|
| 2 | $t_d(\text{RSTH-ZV})$ | Delay time, external $\overline{\text{RESET}}$ high to internal reset high and all signal groups valid ^{(2) (3)} | 512 x CLKIN period | | ns |
| 3a | $t_d(\text{RSTL-ECKOL})$ | Delay time, $\overline{\text{RESET}}$ low to ECLKOUT low (6713) | 0 | | ns |
| 3b | $t_d(\text{RSTL-ECKOH})$ | Delay time, $\overline{\text{RESET}}$ low to ECLKOUT high impedance (6713B) | 0 | | ns |
| 4 | $t_d(\text{RSTH-ECKOV})$ | Delay time, $\overline{\text{RESET}}$ high to ECLKOUT valid | | 6P | ns |
| 5a | $t_d(\text{RSTL-CKO2IV})$ | Delay time, $\overline{\text{RESET}}$ low to CLKOUT2 invalid (6713) | 0 | | ns |
| 5b | $t_d(\text{RSTL-CKO2IH})$ | Delay time, $\overline{\text{RESET}}$ low to CLKOUT2 high impedance (6713B) | 0 | | ns |
| 6 | $t_d(\text{RSTH-CKO2V})$ | Delay time, $\overline{\text{RESET}}$ high to CLKOUT2 valid | | 6P | ns |
| 7 | $t_d(\text{RSTL-CKO3L})$ | Delay time, $\overline{\text{RESET}}$ low to CLKOUT3 low | 0 | | ns |
| 8 | $t_d(\text{RSTH-CKO3V})$ | Delay time, $\overline{\text{RESET}}$ high to CLKOUT3 valid | | 6P | ns |
| 9 | $t_d(\text{RSTL-EMIFZH})$ | Delay time, $\overline{\text{RESET}}$ low to EMIF Z group high impedance ⁽³⁾ | 0 | | ns |
| 10 | $t_d(\text{RSTL-EMIFLIV})$ | Delay time, $\overline{\text{RESET}}$ low to EMIF low group (BUSREQ) invalid ⁽³⁾ | 0 | | ns |
| 11 | $t_d(\text{RSTL-Z1HZ})$ | Delay time, $\overline{\text{RESET}}$ low to Z group 1 high impedance ⁽³⁾ | 0 | | ns |
| 12 | $t_d(\text{RSTL-Z2HZ})$ | Delay time, $\overline{\text{RESET}}$ low to Z group 2 high impedance ⁽³⁾ | 0 | | ns |

- (1) $P = 1/\text{CPU clock frequency}$ in ns. Note that while internal reset is asserted low, the CPU clock (SYSCLK1) period is equal to the input clock (CLKIN) period multiplied by 8. For example, if the CLKIN period is 20 ns, the CPU clock (SYSCLK1) period is 20 ns x 8 = 160 ns. Therefore, $P = \text{SYSCLK1} = 160$ ns while internal reset is asserted.
- (2) The internal reset is stretched exactly 512 x CLKIN cycles if CLKIN is used (CLKMODE0 = 1). If the input clock (CLKIN) is not stable when $\overline{\text{RESET}}$ is deasserted, the actual delay time may vary.
- (3) EMIF Z group consists of EA[21:2], ED[31:0], CE[3:0], BE[3:0], $\overline{\text{ARE}}/\overline{\text{SDCAS}}/\overline{\text{SSADS}}$, $\overline{\text{AWE}}/\overline{\text{SDWE}}/\overline{\text{SSWE}}$, $\overline{\text{AOE}}/\overline{\text{SDRAS}}/\overline{\text{SSOE}}$, and HOLDA.
EMIF low group consists of BUSREQ.
Z group 1 consists of CLKR0/ACLKR0, CLR1/AXR0[6], CLKX0/ACLKX0, CLKX1/AMUTE0, FSR0/AFSR0, FSR1/AXR0[7], FSX0/AFSX0, FSX1, DX0/AXR0[1], DX1/AXR0[5], TOUT0/AXR0[2], TOUT1/AXR0[4], SDA0, and SCL0.
Z group 2 consists of all other HPI, McASP0/1, GPIO, and I2C1 signals.



NOTES A: EMIF Z group consists of EA[21:2], ED[31:0], CE[3:0], BE[3:0], ARE/SDCAS/SSADS, AWE/SDWE/SSWE, AOE/SDRAS/SSOE, and HOLDA. EMIF low group consists of BUSREQ.

Z group 1 consists of CLKR0/ACLKR0, CLKR1/AXR0[6], CLKX0/ACLKX0, CLKX1/AMUTE0, FSR0/AFSR0, FSR1/AXR0[7], FSX0/AFSX0, FSX1, DX0/AXR0[1], DX1/AXR0[5], TOUT0/AXR0[2], TOUT1/AXR0[4], SDA0, and SCL0.

Z group 2 consists of All other HPI, McASP0/1, GPIO, and I2C1 signals.

B: Boot and device configurations consist of: HD[14, 8, 4:3].

Figure 11-25. Reset Timing

Reset Phase 1: The $\overline{\text{RESET}}$ pin is asserted. During this time, all internal clocks are running at the CLKIN frequency divide-by-8. The CPU is also running at the CLKIN frequency divide-by-8.

Reset Phase 2: The $\overline{\text{RESET}}$ pin is deasserted but the internal reset is stretched. During this time, all internal clocks are running at the CLKIN frequency divide-by-8. The CPU is also running at the CLKIN frequency divide-by-8.

Reset Phase 3: Both the $\overline{\text{RESET}}$ pin and internal reset are deasserted. During this time, all internal clocks are running at their default divide-down frequency of CLKIN. The CPU clock (SYSCLK1) is running at CLKIN frequency. The peripheral clock (SYSCLK2) is running at CLKIN frequency divide-by-2. The EMIF internal clock source (SYSCLK3) is running at CLKIN frequency divide-by-2. SYSCLK3 is reflected on the ECLKOUT pin (when EKSRC bit = 0 [default]). CLKOUT3 is running at CLKIN frequency divide-by-8.

11.12 External Interrupt Timing

Table 11-18. Timing Requirements for External Interrupts⁽¹⁾

See [Figure 11-26](#)

| NO. | | | MIN | MAX | UNIT |
|-----|----------------------|---|-----|-----|------|
| 1 | $t_{w(L\text{OW})}$ | Width of the NMI interrupt pulse low | 2P | | ns |
| | | Width of the EXT_INT interrupt pulse low | 4P | | ns |
| 2 | $t_{w(H\text{IGH})}$ | Width of the NMI interrupt pulse high | 2P | | ns |
| | | Width of the EXT_INT interrupt pulse high | 4P | | ns |

(1) P = 1/CPU clock frequency in ns. For example, when running parts at 300 MHz, use P = 3.3 ns.

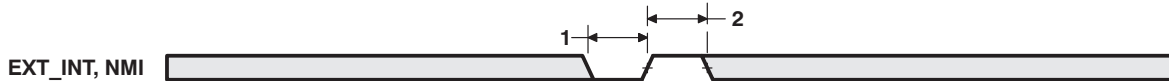


Figure 11-26. External/NMI Interrupt

11.13 Multichannel Audio Serial Port (McASP) Timing

Table 11-19. Timing Requirements for McASP

See [Figure 11-27](#) and [Figure 11-28](#)

| NO. | | | 6713 | | 6713B | | UNIT |
|-----|-----------------------|--|-----------------------------|-----|-------|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| 1 | $t_{c(AHCKRX)}$ | Cycle time, AHCLKR/X | 20 | | 20 | | ns |
| 2 | $t_{w(AHCKRX)}$ | Pulse duration, AHCLKR/X high or low | 7.5 | | 7.5 | | ns |
| 3 | $t_{c(ACKRX)}$ | Cycle time, ACLKR/X | Greater of $2P^{(1)}$ or 33 | | 33 | | ns |
| 4 | $t_{w(ACKRX)}$ | Pulse duration, ACLKR/X high or low | ACLKR/X ext | | 14 | | ns |
| 5 | $t_{su(AFRXC-ACKRX)}$ | Setup time, AFSR/X input valid before ACLKR/X latches data | ACLKR/X int | | 6 | | ns |
| | | | ACLKR/X ext | | 3 | | ns |
| 6 | $t_{h(ACKRX-AFRX)}$ | Hold time, AFSR/X input valid after ACLKR/X latches data | ACLKR/X int | | 0 | | ns |
| | | | ACLKR/X ext | | 3 | | ns |
| 7 | $t_{su(AXR-ACKRX)}$ | Setup time, AXR input valid before ACLKR/X latches data | ACLKR/X int | | 10.2 | | ns |
| | | | ACLKR/X ext | | 6 | | ns |
| 8 | $t_{h(ACKRX-AXR)}$ | Hold time, AXR input valid after ACLKR/X latches data | ACLKR/X int | | 1 | | ns |
| | | | ACLKR/X ext | | 3 | | ns |

(1) P = SYSCLK2 period

Table 11-20. Switching Characteristics for McASP⁽¹⁾

over recommended operating conditions (see [Figure 11-27](#) and [Figure 11-28](#))

| NO. | PARAMETER | | MIN | MAX | UNIT |
|-----|------------------------|---|-----------------------------|-----|--------------|
| 9 | $t_{c(AHCKRX)}$ | Cycle time, AHCLKR/X | 20 | | ns |
| 10 | $t_{w(AHCKRX)}$ | Pulse duration, AHCLKR/X high or low | (AH/2) – 2.5 | | ns |
| 11 | $t_{c(ACKRX)}$ | Cycle time, ACLKR/X | Greater of $2P^{(2)}$ or 33 | | ns |
| 12 | $t_{w(ACKRX)}$ | Pulse duration, ACLKR/X high or low | ACLKR/X int | | (AH/2) – 2.5 |
| 13 | $t_{d(ACKRX-AFRX)}$ | Delay time, ACLKR/X transmit edge to AFSX/R output valid | ACLKR/X int | | –1 |
| | | | ACLKR/X ext | | 5 |
| 14 | $t_{d(ACKX-AXRV)}$ | Delay time, ACLKX transmit edge to AXR output valid | ACLKR/X int | | –1 |
| | | | ACLKR/X ext | | 5 |
| 15 | $t_{dis(ACKRX-AXRHZ)}$ | Disable time, AXR high impedance following last data bit from ACLKR/X transmit edge | ACLKR/X int | | –1 |
| | | | ACLKR/X ext | | 10 |

(1) AH = AHCLKR/X period in ns; A = ACLKR/X period in ns

(2) P = SYSCLK2 period

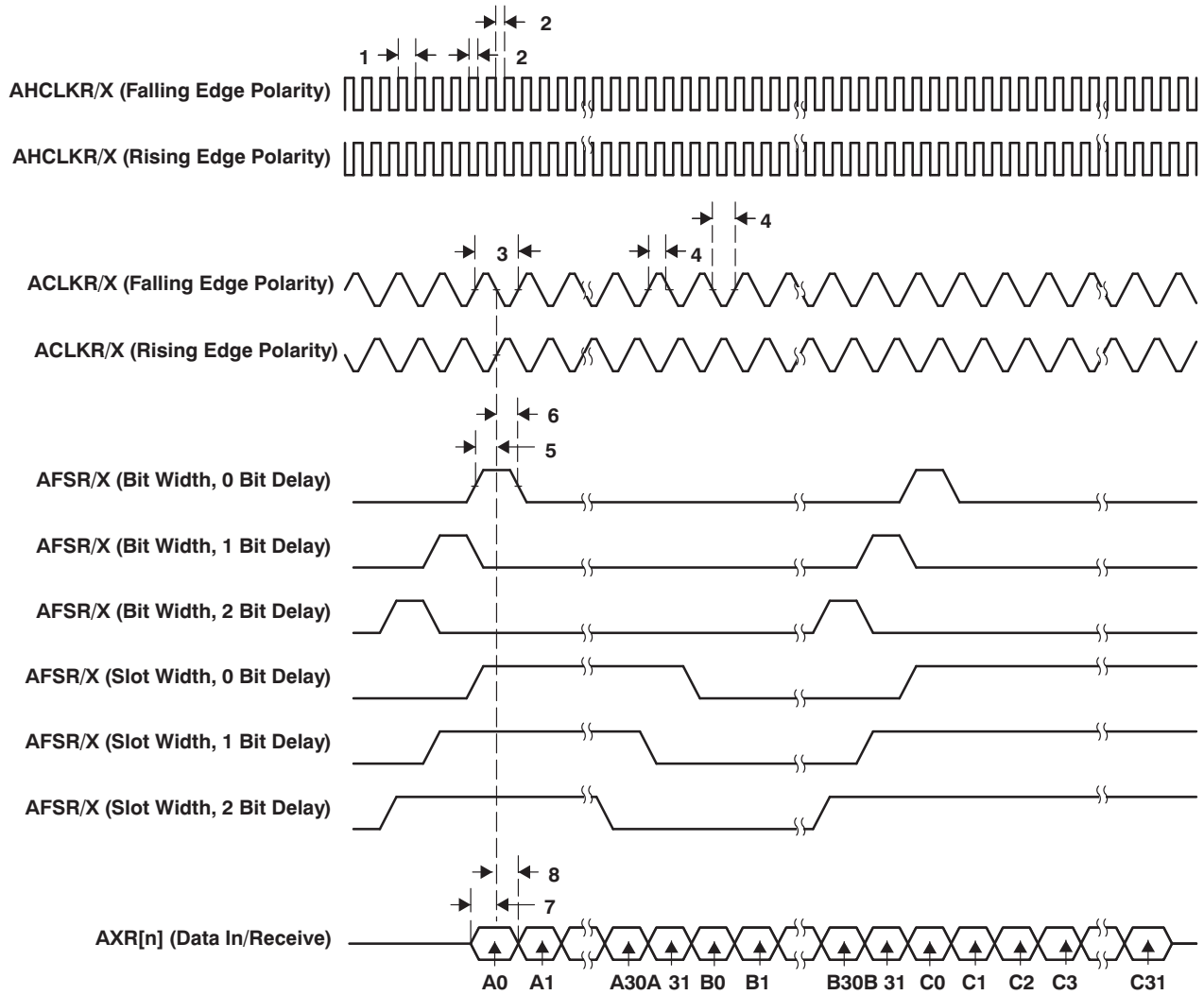


Figure 11-27. McASP Input Timings

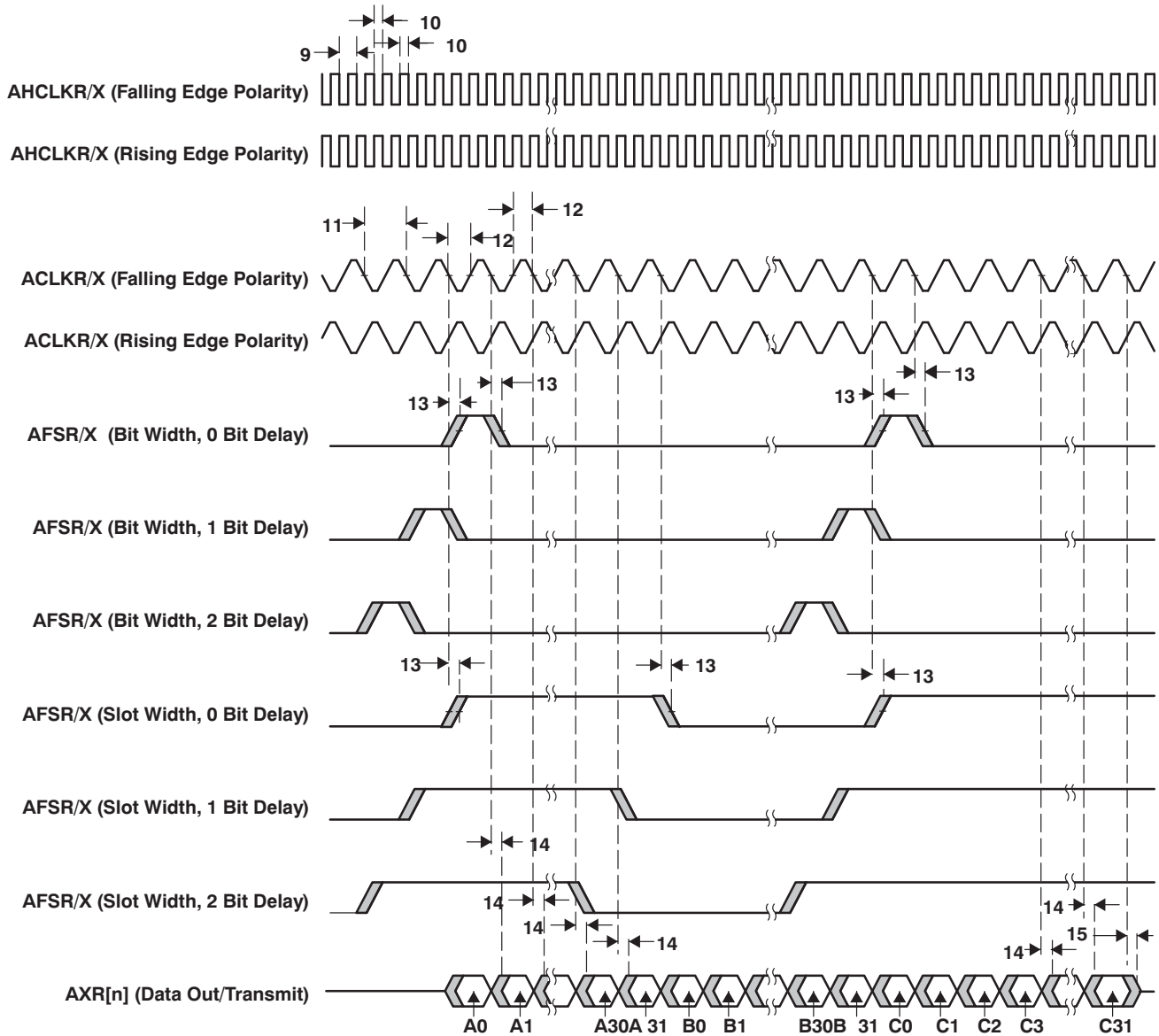


Figure 11-28. McASP Output Timings

11.14 Inter-Integrated Circuits (I²C) Timing

Table 11-21. Timing Requirements for I²C⁽¹⁾

See Figure 11-29

| NO. | | STANDARD MODE | | FAST MODE | | UNIT |
|-----|--|------------------|------|------------------------------|--------------------|---------|
| | | MIN | MAX | MIN | MAX | |
| 1 | $t_{c(SCL)}$ Cycle time, SCL | 10 | | 2.5 | | μ s |
| 2 | $t_{su(SCLH-SDAL)}$ Setup time, SCL high before SDA low (for a repeated START condition) | 4.7 | | 0.6 | | μ s |
| 3 | $t_{h(SCLL-SDAL)}$ Hold time, SCL low after SDA low (for a START and a repeated START condition) | 4 | | 0.6 | | μ s |
| 4 | $t_{w(SCLL)}$ Pulse duration, SCL low | 4.7 | | 1.3 | | μ s |
| 5 | $t_{w(SCLH)}$ Pulse duration, SCL high | 4 | | 0.6 | | μ s |
| 6 | $t_{su(SDAV-SDLH)}$ Setup time, SDA valid before SCL high | 250 | | 100 ⁽²⁾ | | ns |
| 7 | $t_{h(SDA-SDLL)}$ Hold time, SDA valid after SCL low (for I ² C bus devices) | 0 ⁽³⁾ | | 0 ⁽³⁾ | 0.9 ⁽⁴⁾ | μ s |
| 8 | $t_{w(SDAH)}$ Pulse duration, SDA high between STOP and START conditions | 4.7 | | 1.3 | | μ s |
| 9 | $t_{r(SDA)}$ Rise time, SDA | | 1000 | $20 + 0.1C_b$ ⁽⁵⁾ | 300 | ns |
| 10 | $t_{r(SCL)}$ Rise time, SCL | | 1000 | $20 + 0.1C_b$ ⁽⁵⁾ | 300 | ns |
| 11 | $t_{f(SDA)}$ Fall time, SDA | | 300 | $20 + 0.1C_b$ ⁽⁵⁾ | 300 | ns |
| 12 | $t_{f(SCL)}$ Fall time, SCL | | 300 | $20 + 0.1C_b$ ⁽⁵⁾ | 300 | ns |
| 13 | $t_{su(SCLH-SDAH)}$ Setup time, SCL high before SDA high (for STOP condition) | 4 | | 0.6 | | μ s |
| 14 | $t_{w(SP)}$ Pulse duration, spike (must be suppressed) | | | 0 | 50 | ns |
| 15 | C_b ⁽⁵⁾ Capacitive load for each bus line | | 400 | | 400 | pF |

- (1) The I²C pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down.
- (2) A fast-mode I²C-bus device can be used in a standard-mode I²C-bus system, but the requirement $t_{su}(SDA-SCLH) \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r,max} + t_{su}(SDA-SCLH) = 1000 + 250 = 1250$ ns (according to the standard-mode I²C-bus specification) before the SCL line is released.
- (3) A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IH} min of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- (4) The maximum $t_{h(SDA-SCLL)}$ has only to be met if the device does not stretch the low period [$t_{w(SCLL)}$] of the SCL signal.
- (5) C_b = total capacitance of one bus line in pF. If mixed with HS-mode devices, faster fall times are allowed.

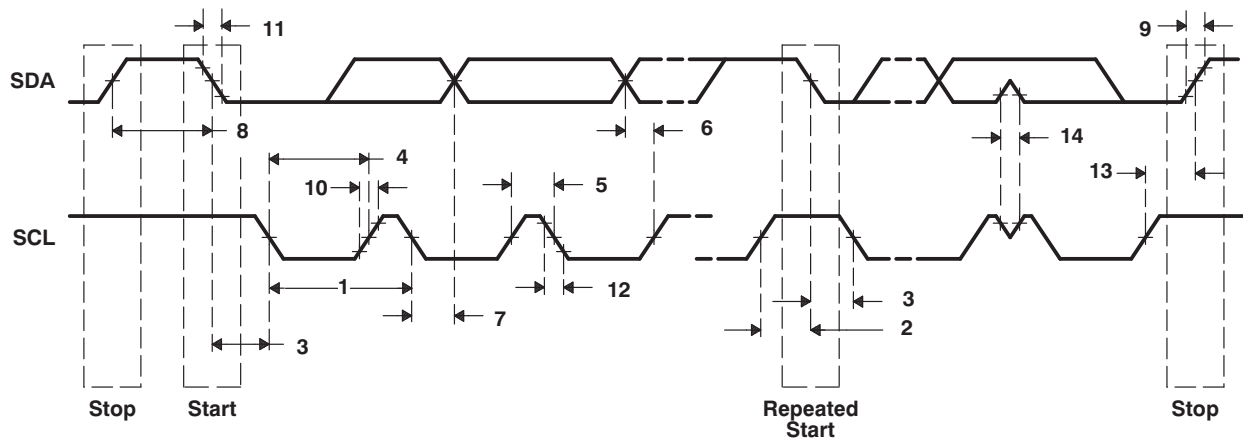


Figure 11-29. I²C Receive

Table 11-22. Switching Characteristics for I²C⁽¹⁾

over recommended operating conditions (see [Figure 11-30](#))

| NO. | PARAMETER | STANDARD MODE | | FAST MODE | | UNIT |
|-----|--|---------------|------|---------------------|-----|---------|
| | | MIN | MAX | MIN | MAX | |
| 16 | $t_{c(SCL)}$ Cycle time, SCL | 10 | | 2.5 | | μ s |
| 17 | $t_{d(SCLH-SDAL)}$ Delay time, SCL high to SDA low (for a repeated START condition) | 4.7 | | 0.6 | | μ s |
| 18 | $t_{d(SDAL-SCLL)}$ Delay time, SDA low to SCL low (for a START and a repeated START condition) | 4 | | 0.6 | | μ s |
| 19 | $t_{w(SCLL)}$ Pulse duration, SCL low | 4.7 | | 1.3 | | μ s |
| 20 | $t_{w(SCLH)}$ Pulse duration, SCL high | 4 | | 0.6 | | μ s |
| 21 | $t_{d(SDAV-SDLH)}$ Delay time, SDA valid to SCL high | 250 | | 100 | | ns |
| 22 | $t_{v(SDLL-SDAV)}$ Valid time, SDA valid after SCL low (for I ² C bus devices) | 0 | | 0 | 0.9 | μ s |
| 23 | $t_{w(SDAH)}$ Pulse duration, SDA high between STOP and START conditions | 4.7 | | 1.3 | | μ s |
| 24 | $t_{r(SDA)}$ Rise time, SDA | | 1000 | $20 + 0.1C_b^{(1)}$ | 300 | ns |
| 25 | $t_{r(SCL)}$ Rise time, SCL | | 1000 | $20 + 0.1C_b^{(1)}$ | 300 | ns |
| 26 | $t_{f(SDA)}$ Fall time, SDA | | 300 | $20 + 0.1C_b^{(1)}$ | 300 | ns |
| 27 | $t_{f(SCL)}$ Fall time, SCL | | 300 | $20 + 0.1C_b^{(1)}$ | 300 | ns |
| 28 | $t_{d(SCLH-SDAH)}$ Delay time, SCL high to SDA high (for STOP condition) | 4 | | 0.6 | | μ s |
| 30 | C_b Capacitance for each I2C pin | | 10 | | 10 | pF |

(1) C_b = total capacitance of one bus line in pF. If mixed with HS-mode devices, faster fall-times are allowed.

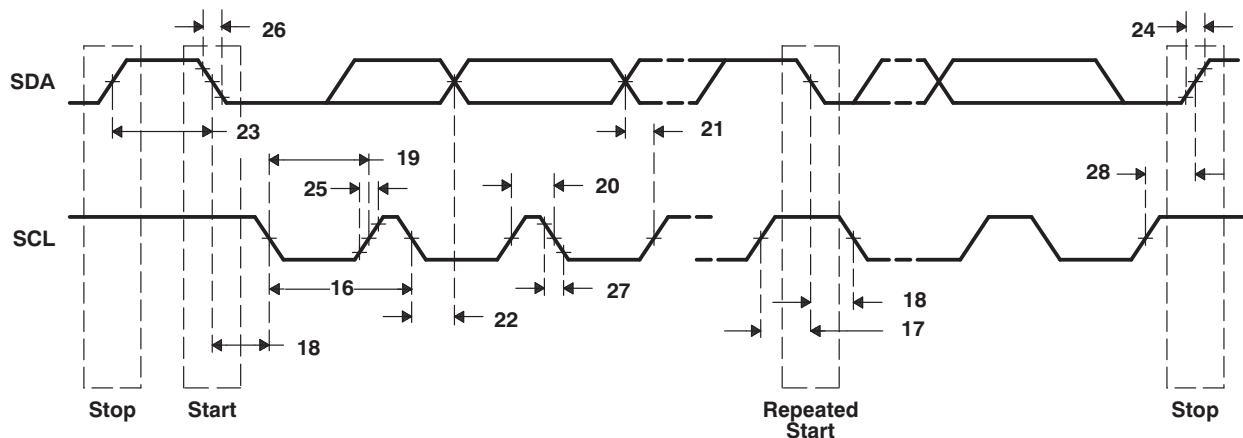


Figure 11-30. I²C Transmit Timings

11.15 Host-Port Interface Timing

Table 11-23. Timing Requirements for Host-Port Interface Cycles^{(1) (2)}

See Figure 11-31—Figure 11-34

| NO. | | 6713 | | 6713B | | UNIT |
|-----|---|-----------|-----|-------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| 1 | $t_{su(SELV-HSTBL)}$ Setup time, select signals valid before $\overline{HSTROBE}$ low ⁽³⁾ | 5 | | 5 | | ns |
| 2 | $t_h(HSTBL-SELV)$ Hold time, select signals valid after $\overline{HSTROBE}$ low ⁽³⁾ | 4 | | 4 | | ns |
| 3 | $t_w(HSTBL)$ Pulse duration, $\overline{HSTROBE}$ low (host read access) | 10P + 5.8 | | 4P | | ns |
| | $t_w(HSTBL)$ Pulse duration, $\overline{HSTROBE}$ low (host write access) | 4P | | 4P | | ns |
| 4 | $t_w(HSTBH)$ Pulse duration, $\overline{HSTROBE}$ high between consecutive accesses | 4P | | 4P | | ns |
| 10 | $t_{su(SELV-HASL)}$ Setup time, select signals valid before \overline{HAS} low ⁽³⁾ | 5 | | 5 | | ns |
| 11 | $t_h(HASL-SELV)$ Hold time, select signals valid after \overline{HAS} low ⁽³⁾ | 3 | | 3 | | ns |
| 12 | $t_{su(HDV-HSTBH)}$ Setup time, host data valid before $\overline{HSTROBE}$ high | 5 | | 5 | | ns |
| 13 | $t_h(HSTBH-HDV)$ Hold time, host data valid after $\overline{HSTROBE}$ high | 3 | | 3 | | ns |
| 14 | $t_h(HRDYL-HSTBL)$ Hold time, $\overline{HSTROBE}$ low after \overline{HRDY} low. $\overline{HSTROBE}$ should not be inactivated until \overline{HRDY} is active (low); otherwise, HPI writes will not complete properly. | 2 | | 2 | | ns |
| 18 | $t_{su(HASL-HSTBL)}$ Setup time, \overline{HAS} low before $\overline{HSTROBE}$ low | 2 | | 2 | | ns |
| 19 | $t_h(HSTBL-HASL)$ Hold time, \overline{HAS} low after $\overline{HSTROBE}$ low | 2 | | 2 | | ns |

(1) $\overline{HSTROBE}$ refers to the following logical operation on \overline{HCS} , $\overline{HDS1}$, and $\overline{HDS2}$: $[\text{NOT}(\overline{HDS1} \text{ XOR } \overline{HDS2})] \text{ OR } \overline{HCS}$.

(2) P = 1/CPU clock frequency in ns. For example, when running parts at 300 MHz, use P = 3.3 ns.

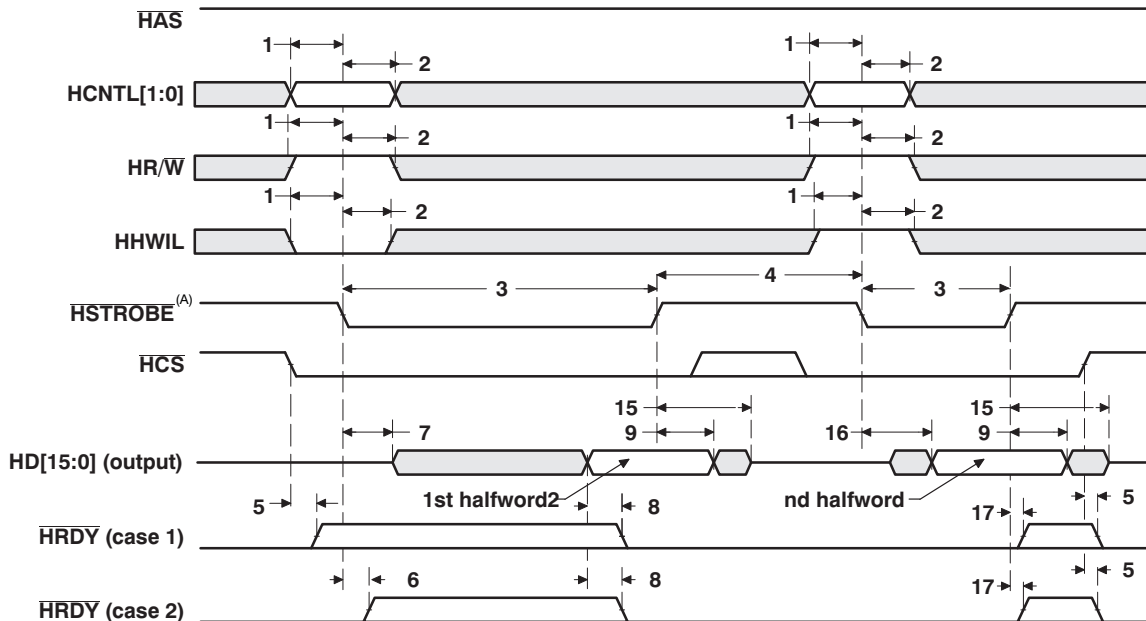
(3) Select signals include $\overline{HCNTL}[1:0]$, $\overline{HR\overline{W}}$, and \overline{HHWIL} .

Table 11-24. Switching Characteristics for Host-Port Interface Cycles^{(1) (2)}

over recommended operating conditions (see [Figure 11-31—Figure 11-34](#))

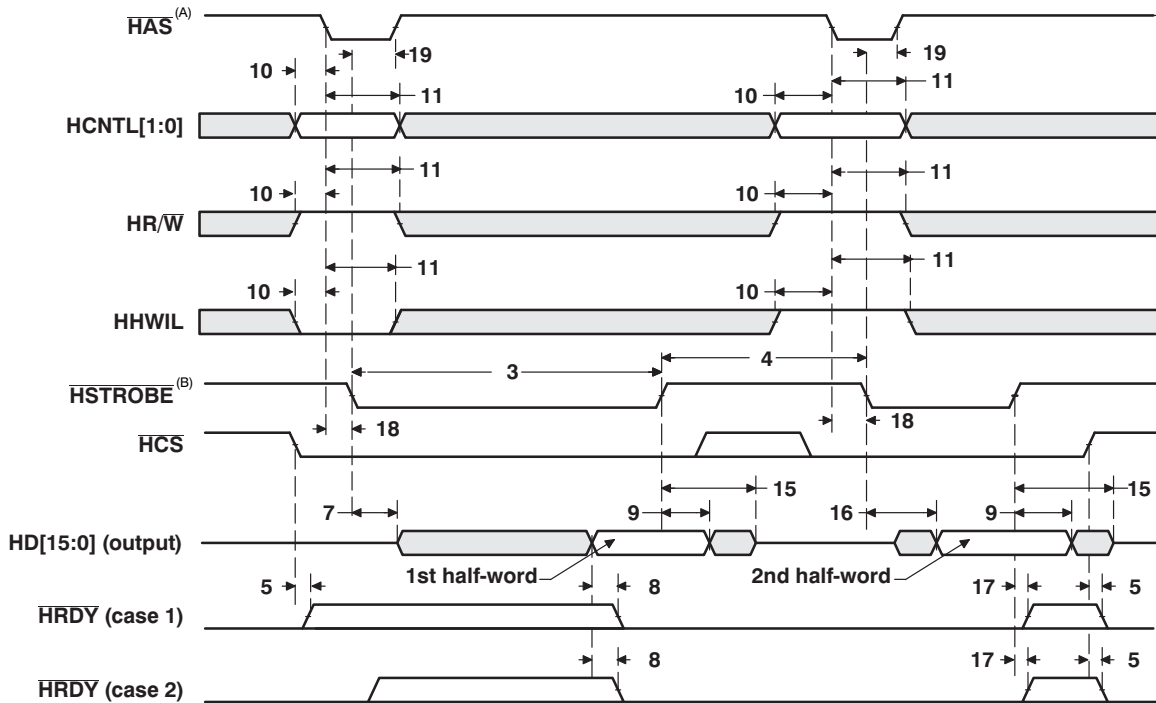
| NO. | PARAMETER | 6713 | | 6713B | | UNIT |
|-----|---|--------|-----------|--------|------|------|
| | | MIN | MAX | MIN | MAX | |
| 5 | $t_{d(HCS-HRDY)}$ Delay time, \overline{HCS} to \overline{HRDY} ⁽³⁾ | 1 | 15 | 1 | 12 | ns |
| 6 | $t_{d(HSTBL-HRDYH)}$ Delay time, $\overline{HSTROBE}$ low to \overline{HRDY} high ⁽⁴⁾ | 3 | 15 | 3 | 12 | ns |
| 7 | $t_{d(HSTBL-HDLZ)}$ Delay time, $\overline{HSTROBE}$ low to HD low impedance for an HPI read | 2 | | 2 | | ns |
| 8 | $t_{d(HDV-HRDYL)}$ Delay time, HD valid to \overline{HRDY} low | 2P – 4 | | 2P – 4 | | ns |
| 9 | $t_{oh(HSTBH-HDV)}$ Output hold time, HD valid after $\overline{HSTROBE}$ high | 3 | 12 | 3 | 12 | ns |
| 15 | $t_{d(HSTBH-HDHZ)}$ Delay time, $\overline{HSTROBE}$ high to HD high impedance | 2 | 12 | 3 | 12 | ns |
| 16 | $t_{d(HSTBL-HDV)}$ Delay time, $\overline{HSTROBE}$ low to HD valid | 3 | 10P + 5.8 | 3 | 12.5 | ns |
| 17 | $t_{d(HSTBH-HRDYH)}$ Delay time, $\overline{HSTROBE}$ high to \overline{HRDY} high ⁽⁵⁾ | 3 | 15 | 3 | 12 | ns |

- (1) $\overline{HSTROBE}$ refers to the following logical operation on \overline{HCS} , $\overline{HDS1}$, and $\overline{HDS2}$: $[\text{NOT}(\overline{HDS1} \text{ XOR } \overline{HDS2})] \text{ OR } \overline{HCS}$.
- (2) $P = 1/\text{CPU clock frequency in ns}$. For example, when running parts at 300 MHz, use $P = 3.3$ ns.
- (3) \overline{HCS} enables \overline{HRDY} , and \overline{HRDY} is always low when \overline{HCS} is high. The case where \overline{HRDY} goes high when \overline{HCS} falls indicates that HPI is busy completing a previous HPID write or READ with autoincrement.
- (4) This parameter is used during an HPID read. At the beginning of the first half-word transfer on the falling edge of $\overline{HSTROBE}$, the HPI sends the request to the EDMA internal address generation hardware, and \overline{HRDY} remains high until the EDMA internal address generation hardware loads the requested data into HPID.
- (5) This parameter is used after the second half-word of an HPID write or autoincrement read. \overline{HRDY} remains low if the access is not an HPID write or autoincrement read. Reading or writing to HPIC or HPIA does not affect the \overline{HRDY} signal.



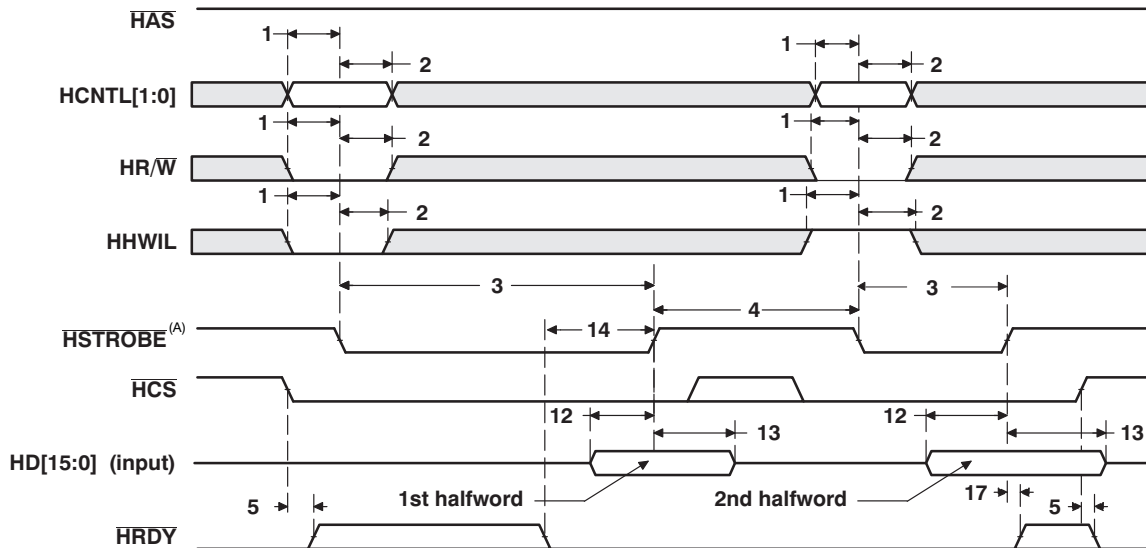
NOTE A: $\overline{HSTROBE}$ refers to the following logical operation on \overline{HCS} , $\overline{HDS1}$, and $\overline{HDS2}$: $[\text{NOT}(\overline{HDS1} \text{ XOR } \overline{HDS2})] \text{ OR } \overline{HCS}$.

Figure 11-31. HPI Read Timing (\overline{HAS} Not Used, Tied High)



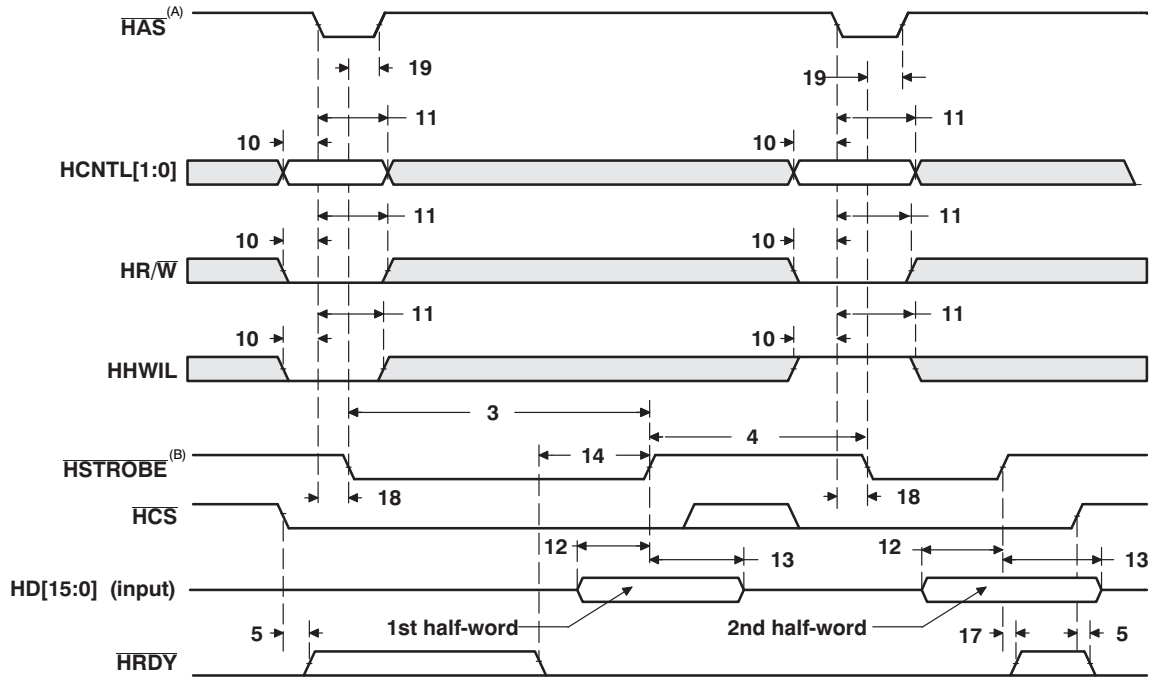
NOTES A: For correct operation, strobe the $\overline{\text{HAS}}$ signal only once per $\overline{\text{HSTROBE}}$ active cycle.
B: $\overline{\text{HSTROBE}}$ refers to the following logical operation on $\overline{\text{HCS}}$, $\overline{\text{HDS1}}$, and $\overline{\text{HDS2}}$: $[\text{NOT}(\overline{\text{HDS1}} \text{ XOR } \overline{\text{HDS2}})] \text{ OR } \overline{\text{HCS}}$.

Figure 11-32. HPI Read Timing ($\overline{\text{HAS}}$ Used)



NOTE A: $\overline{\text{HSTROBE}}$ refers to the following logical operation on $\overline{\text{HCS}}$, $\overline{\text{HDS1}}$, and $\overline{\text{HDS2}}$: $[\text{NOT}(\overline{\text{HDS1}} \text{ XOR } \overline{\text{HDS2}})] \text{ OR } \overline{\text{HCS}}$.

Figure 11-33. HPI Write Timing ($\overline{\text{HAS}}$ Not Used, Tied High)



NOTES A: For correct operation, strobe the HAS signal only once per HSTROBE active cycle.
B: HSTROBE refers to the following logical operation on HCS, HDS1, and HDS2: $\overline{[\text{NOT}(\text{HDS1 XOR HDS2}) \text{ OR HCS}]}$.

Figure 11-34. HPI Write Timing (HAS Used)

11.16 Multichannel Buffered Serial Port (McBSP) Timing

Table 11-25. Timing Requirements for McBSP^{(1) (2)}

See Figure 11-35

| NO. | PARAMETER | | | MIN | MAX | UNIT |
|-----|---------------------------|---|------------|--------------------------------------|-----|------|
| 2 | $t_{c(\text{CKRX})}$ | Cycle time, CLKR/X | CLKR/X ext | $2P^{(3)}$ | | ns |
| 3 | $t_{w(\text{CKRX})}$ | Pulse duration, CLKR/X high or CLKR/X low | CLKR/X ext | $0.5 * t_{c(\text{CKRX})} - 1^{(4)}$ | | ns |
| 5 | $t_{su(\text{FRH-CKRL})}$ | Setup time, external FSR high before CLKR low | CLKR int | 9 | | ns |
| | | | CLKR ext | 1 | | ns |
| 6 | $t_{h(\text{CKRL-FRH})}$ | Hold time, external FSR high after CLKR low | CLKR int | 6 | | ns |
| | | | CLKR ext | 3 | | ns |
| 7 | $t_{su(\text{DRV-CKRL})}$ | Setup time, DR valid before CLKR low | CLKR int | 8 | | ns |
| | | | CLKR ext | 0 | | ns |
| 8 | $t_{h(\text{CKRL-DRV})}$ | Hold time, DR valid after CLKR low | CLKR int | 3 | | ns |
| | | | CLKR ext | 4 | | ns |
| 10 | $t_{su(\text{FXH-CKXL})}$ | Setup time, external FSX high before CLKX low | CLKX int | 9 | | ns |
| | | | CLKX ext | 1 | | ns |
| 11 | $t_{h(\text{CKXL-FXH})}$ | Hold time, external FSX high after CLKX low | CLKX int | 6 | | ns |
| | | | CLKX ext | 3 | | ns |

- (1) CLKRP = CLKXP = FSRP = FSXP = 0. If polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
- (2) $P = 1/\text{CPU clock frequency}$ in ns. For example, when running parts at 300 MHz, use $P = 3.3$ ns.
- (3) The minimum CLKR/X period is twice the CPU cycle time ($2P$) and not faster than 75 Mbps (13.3 ns). This means that the maximum bit rate for communications between the McBSP and other devices is 75 Mbps for 167-MHz and 225-MHz CPU clocks or 50 Mbps for 100-MHz CPU clock; where the McBSP is either the master or the slave. Care must be taken to ensure that the ac timings specified in this data sheet are met. The maximum bit rate for McBSP-to-McBSP communications is 67 Mbps; therefore, the minimum CLKR/X clock cycle is either twice the CPU cycle time ($2P$), or 15 ns (67 MHz), whichever value is larger. For example, when running parts at 150 MHz ($P = 6.7$ ns), use 15 ns as the minimum CLKR/X clock cycle (by setting the appropriate CLKGDV ratio or external clock source). When running parts at 60 MHz ($P = 16.67$ ns), use $2P = 33$ ns (30 MHz) as the minimum CLKR/X clock cycle. The maximum bit rate for McBSP-to-McBSP communications applies when the serial port is a master of the clock and frame syncs (with CLKR connected to CLKX, FSR connected to FSX, CLKXM = FSXM = 1, and CLKRM = FSRM = 0) in data delay 1 or 2 mode (R/XDATDLY = 01b or 10b) and the other device the McBSP communicates to is a slave.
- (4) This parameter applies to the maximum McBSP frequency. Operate serial clocks (CLKR/X) in the reasonable range of 40/60 duty cycle.

Table 11-26. Switching Characteristics for McBSP^{(1) (2)}

over recommended operating conditions (see [Figure 11-35](#))

| NO. | PARAMETER | | 6713 | | 6713B | | UNIT | |
|-----|----------------------|--|-----------------------|----------------------|-----------------------|----------------------|-----------------|----|
| | | | MIN | MAX | MIN | MAX | | |
| 1 | $t_{d(CKSH-CKRXH)}$ | Delay time, CLKS high to CLKR/X high for internal CLKR/X generated from CLKS input | 1.8 | 10 | 1.8 | 10 | ns | |
| 2 | $t_{c(CKRX)}$ | Cycle time, CLKR/X | 2P ^{(3) (4)} | | 2P ^{(3) (4)} | | ns | |
| 3 | $t_{w(CKRX)}$ | Pulse duration, CLKR/X high or CLKR/X low | C – 1 ⁽⁵⁾ | C + 1 ⁽⁵⁾ | C – 1 ⁽⁵⁾ | C + 1 ⁽⁵⁾ | ns | |
| 4 | $t_{d(CKRH-FRV)}$ | Delay time, CLKR high to internal FSR valid | –2 | 3 | –2 | 3 | ns | |
| 9 | $t_{d(CKXH-FXV)}$ | Delay time, CLKX high to internal FSX valid | CLKX int | –2 | 3 | –2 | 3 | ns |
| | | | CLKX ext | 2 | 9 | 2 | 9 | ns |
| 12 | $t_{dis(CKXH-DXHZ)}$ | Disable time, DX high impedance following last data bit from CLKX high | CLKX int | –1 | 4 | –1 | 4 | ns |
| | | | CLKX ext | 1.5 | 10 | 1.5 | 10 | ns |
| 13 | $t_{d(CKXH-DXV)}$ | Delay time, CLKX high to DX valid | CLKX int | $-3.2 + D1^{(6)}$ | $4 + D2^{(6)}$ | $-3.2 + D1^{(6)}$ | $4 + D2^{(6)}$ | ns |
| | | | CLKX ext | $0.5 + D1^{(6)}$ | $10 + D2^{(6)}$ | $0.5 + D1^{(6)}$ | $10 + D2^{(6)}$ | ns |
| 14 | $t_{d(FXH-DXV)}$ | Delay time, FSX high to DX valid ONLY applies when in data delay 0 (XDATDLY = 00b) mode | FSX int | –1.5 | 4.5 | –1 | 7.5 | ns |
| | | | FSX ext | 2 | 9 | 2 | 11.5 | ns |

- (1) CLKRP = CLKXP = FSRP = FSXP = 0. If polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
- (2) Minimum delay times also represent minimum output hold times.
- (3) P = 1/CPU clock frequency in ns. For example, when running parts at 300 MHz, use P = 3.3 ns.
- (4) The minimum CLKR/X period is twice the CPU cycle time (2P) and not faster than 75 Mbps (13.3 ns). This means that the maximum bit rate for communications between the McBSP and other devices is 75 Mbps for 167-MHz and 225-MHz CPU clocks or 50 Mbps for 100-MHz CPU clock; where the McBSP is either the master or the slave. Care must be taken to ensure that the AC timings specified in this data sheet are met. The maximum bit rate for McBSP-to-McBSP communications is 67 Mbps; therefore, the minimum CLKR/X clock cycle is either twice the CPU cycle time (2P), or 15 ns (67 MHz), whichever value is larger. For example, when running parts at 150 MHz (P = 6.7 ns), use 15 ns as the minimum CLKR/X clock cycle (by setting the appropriate CLKGDV ratio or external clock source). When running parts at 60 MHz (P = 16.67 ns), use 2P = 33 ns (30 MHz) as the minimum CLKR/X clock cycle. The maximum bit rate for McBSP-to-McBSP communications applies when the serial port is a master of the clock and frame syncs (with CLKR connected to CLKX, FSR connected to FSX, CLKXM = FSXM = 1, and CLKRM = FSRM = 0) in data delay 1 or 2 mode (R/XDATDLY = 01b or 10b) and the other device the McBSP communicates to is a slave.
- (5) C = H or L
 S = sample rate generator input clock = 2P if CLKSM = 1 (P = 1/CPU clock frequency)
 = sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)
 H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even
 = (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
 L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even
 = (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
 CLKGDV should be set appropriately to ensure the McBSP bit rate does not exceed the maximum limit (see note ⁽⁴⁾ above).
- (6) Extra delay from CLKX high to DX valid applies only to the first data bit of a device, if and only if DXENA = 1 in SPCR. If DXENA = 0, then D1 = D2 = 0. If DXENA = 1, then D1 = 2P, D2 = 4P.

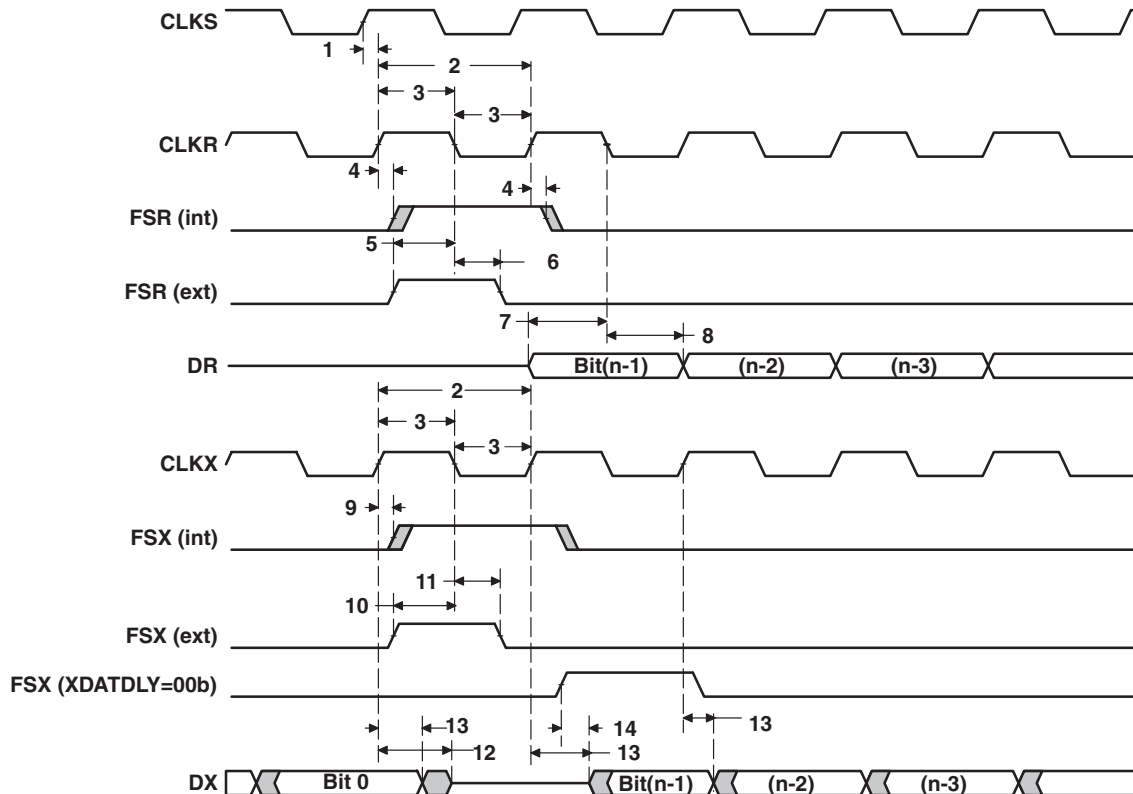


Figure 11-35. McBSP Timings

Table 11-27. Timing Requirements for FSR When GSYNC = 1

See Figure 11-36

| NO. | | MIN | MAX | UNIT |
|-----|--|-----|-----|------|
| 1 | $t_{su}(FRH-CKSH)$ Setup time, FSR high before CLKS high | 4 | | ns |
| 2 | $t_h(CKSH-FRH)$ Hold time, FSR high after CLKS high | 4 | | ns |

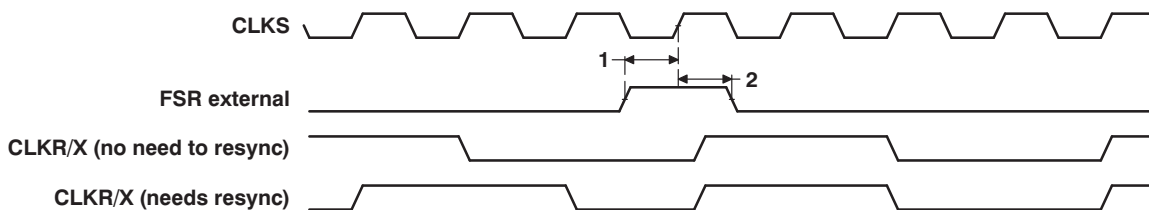


Figure 11-36. FSR Timing When GSYNC = 1

Table 11-28. Timing Requirements for McBSP as SPI Master or Slave:
CLKSTP = 10b, CLKXP = 0⁽¹⁾ ⁽²⁾

See Figure 11-37

| NO. | | MASTER | | SLAVE | | UNIT |
|-----|---|--------|-----|---------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| 4 | $t_{su}(DRV-CKXL)$ Setup time, DR valid before CLKX low | 12 | | 2 – 6P | | ns |
| 5 | $t_h(CKXL-DRV)$ Hold time, DR valid after CLKX low | 4 | | 5 + 12P | | ns |

(1) P = 1/CPU clock frequency in ns. For example, when running parts at 300 MHz, use P = 3.3 ns.

(2) For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

**Table 11-29. Switching Characteristics for McBSP as SPI Master or Slave:
CLKSTP = 10b, CLKXP = 0^{(1) (2)}**

over recommended operating conditions (see Figure 11-37)

| NO. | PARAMETER | 6713 | | | | 6713B | | | | UNIT |
|-----|--|-----------------------|-------|----------|----------|-----------------------|-------|--------|----------|------|
| | | MASTER ⁽³⁾ | | SLAVE | | MASTER ⁽³⁾ | | SLAVE | | |
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| 1 | $t_{h(CKXL-FXL)}$ Hold time, FSX low after CLKX low ⁽⁴⁾ | T - 2 | T + 3 | | | T - 2 | T + 3 | | | ns |
| 2 | $t_{d(FXL-CKXH)}$ Delay time, FSX low to CLKX high ⁽⁵⁾ | L - 2 | L + 3 | | | L - 2 | L + 3 | | | ns |
| 3 | $t_{d(CKXH-DXV)}$ Delay time, CLKX high to DX valid | -3 | 4 | 6P + 2 | 10P + 17 | -3 | 4 | 6P + 2 | 10P + 17 | ns |
| 6 | $t_{dis(CKXL-DXHZ)}$ Disable time, DX high impedance following last data bit from CLKX low | L - 4 | L + 3 | | | L - 2 | L + 3 | | | ns |
| 7 | $t_{dis(FXH-DXHZ)}$ Disable time, DX high impedance following last data bit from FSX high | | | 2P + 1.5 | 6P + 17 | | | 2P + 3 | 6P + 17 | ns |
| 8 | $t_{d(FXL-DXV)}$ Delay time, FSX low to DX valid | | | 4P + 2 | 8P + 17 | | | 4P + 2 | 8P + 17 | ns |

- (1) P = 1/CPU clock frequency in ns. For example, when running parts at 300 MHz, use P = 3.3 ns.
- (2) For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
- (3) S = Sample rate generator input clock = 2P if CLKSM = 1 (P = 1/CPU clock frequency)
= Sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)
T = CLKX period = (1 + CLKGDV) * S
H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
- (4) FSRP = FSXP = 1. As a SPI master, FSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on FSX and FSR is inverted before being used internally.
- (5) CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP. CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP.
- (5) FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).

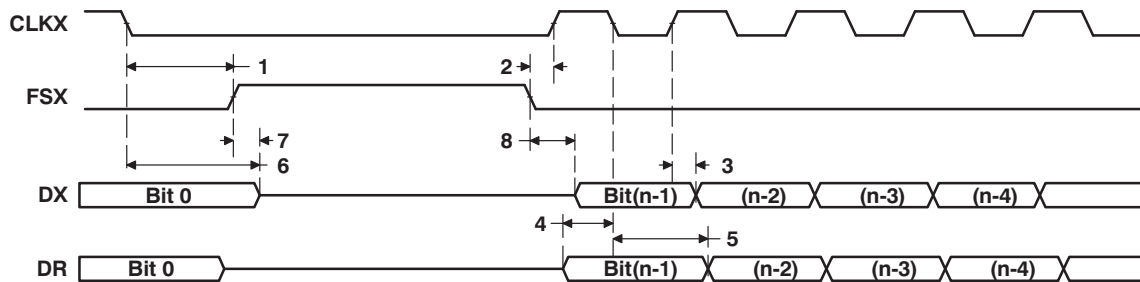


Figure 11-37. McBSP Timing as SPI Master or Slave: CLKSTP = 10b, CLKXP = 0

**Table 11-30. Timing Requirements for McBSP as SPI Master or Slave:
CLKSTP = 11b, CLKXP = 0^{(1) (2)}**

See Figure 11-38

| NO. | PARAMETER | MASTER | | SLAVE | | UNIT |
|-----|--|--------|-----|---------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| 4 | $t_{su(DRV-CKXH)}$ Setup time, DR valid before CLKX high | 12 | | 2 - 6P | | ns |
| 5 | $t_{h(CKXH-DRV)}$ Hold time, DR valid after CLKX high | 4 | | 5 + 12P | | ns |

- (1) P = 1/CPU clock frequency in ns. For example, when running parts at 300 MHz, use P = 3.3 ns.
- (2) For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

**Table 11-31. Switching Characteristics for McBSP as SPI Master or Slave:
CLKSTP = 11b, CLKXP = 0⁽¹⁾ ⁽²⁾**

over recommended operating conditions (see Figure 11-38)

| NO. | PARAMETER | 6713 | | | | 6713B | | | | UNIT | | |
|-----|----------------------|---|-----|-------|-------|-----------------------|----------|-------|---------|--------|----------|----|
| | | MASTER ⁽³⁾ | | SLAVE | | MASTER ⁽³⁾ | | SLAVE | | | | |
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | | | |
| 1 | $t_{h(CKXL-FXL)}$ | Hold time, FSX low after CLKX low ⁽⁴⁾ | | L - 2 | L + 3 | | | L - 2 | L + 3 | | ns | |
| 2 | $t_{d(FXL-CKXH)}$ | Delay time, FSX low to CLKX high ⁽⁵⁾ | | T - 2 | T + 3 | | | T - 2 | T + 3 | | ns | |
| 3 | $t_{d(CKXL-DXV)}$ | Delay time, CLKX low to DX valid | | -3 | 4 | 6P + 2 | 10P + 17 | -3 | 4 | 6P + 2 | 10P + 17 | ns |
| 6 | $t_{dis(CKXL-DXHZ)}$ | Disable time, DX high impedance following last data bit from CLKX low | | -4 | 4 | 6P + 1.5 | 10P + 17 | -2 | 4 | 6P + 3 | 10P + 17 | ns |
| 7 | $t_{d(FXL-DXV)}$ | Delay time, FSX low to DX valid | | H - 2 | H + 4 | 4P + 2 | 8P + 17 | H - 2 | H + 6.5 | 4P + 2 | 8P + 17 | ns |

- (1) P = 1/CPU clock frequency in ns. For example, when running parts at 300 MHz, use P = 3.3 ns.
- (2) For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
- (3) S = Sample rate generator input clock = 2P if CLKSM = 1 (P = 1/CPU clock frequency)
= Sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)
- T = CLKX period = (1 + CLKGDV) * S
- H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
- L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
- (4) FSRP = FSXP = 1. As a SPI master, FSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on FSX and FSR is inverted before being used internally.
- CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP. CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP.
- (5) FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).

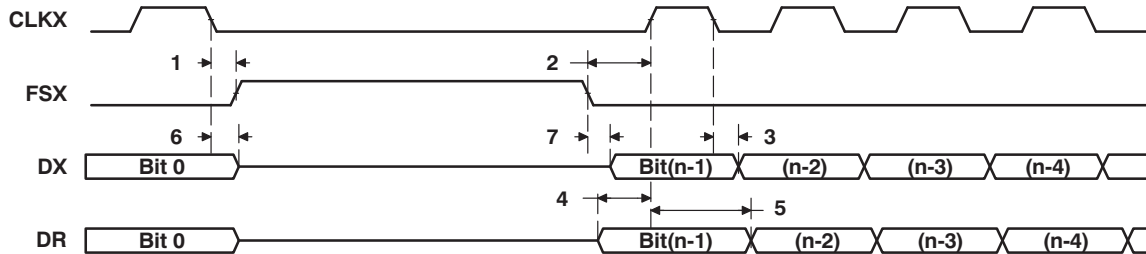


Figure 11-38. McBSP as SPI Master or Slave: CLKSTP = 11b, CLKXP = 0

Table 11-32. Timing Requirements for McBSP as SPI Master or Slave:
CLKSTP = 10b, CLKXP = 1^{(1) (2)}

See Figure 11-39

| NO. | | MASTER | | SLAVE | | UNIT |
|-----|--|--------|-----|---------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| 4 | $t_{su(DRV-CKXH)}$ Setup time, DR valid before CLKX high | 12 | | 2 – 6P | | ns |
| 5 | $t_h(CKXH-DRV)$ Hold time, DR valid after CLKX high | 4 | | 5 + 12P | | ns |

- (1) P = 1/CPU clock frequency in ns. For example, when running parts at 300 MHz, use P = 3.3 ns.
- (2) For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

Table 11-33. Switching Characteristics for McBSP as SPI Master or Slave:
CLKSTP = 10b, CLKXP = 1^{(1) (2)}

over recommended operating conditions (see Figure 11-39)

| NO. | PARAMETER | 6713 | | | | 6713B | | | | UNIT |
|-----|---|-----------------------|-------|----------|----------|-----------------------|-------|--------|----------|------|
| | | MASTER ⁽³⁾ | | SLAVE | | MASTER ⁽³⁾ | | SLAVE | | |
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| 1 | $t_h(CKXH-FXL)$ Hold time, FSX low after CLKX high ⁽⁴⁾ | T – 2 | T + 3 | | | T – 2 | T + 3 | | | ns |
| 2 | $t_d(FXL-CKXL)$ Delay time, FSX low to CLKX low ⁽⁵⁾ | H – 2 | H + 3 | | | H – 2 | H + 3 | | | ns |
| 3 | $t_d(CKXL-DXV)$ Delay time, CLKX low to DX valid | –3 | 4 | 6P + 2 | 10P + 17 | –3 | 4 | 6P + 2 | 10P + 17 | ns |
| 6 | $t_{dis}(CKXH-DXHZ)$ Disable time, DX high impedance following last data bit from CLKX high | H – 3.6 | H + 3 | | | H – 2 | H + 3 | | | ns |
| 7 | $t_{dis}(FXH-DXHZ)$ Disable time, DX high impedance following last data bit from FSX high | | | 2P + 1.5 | 6P + 17 | | | 2P + 3 | 6P + 17 | ns |
| 8 | $t_d(FXL-DXV)$ Delay time, FSX low to DX valid | | | 4P + 2 | 8P + 17 | | | 4P + 2 | 8P + 17 | ns |

- (1) P = 1/CPU clock frequency in ns. For example, when running parts at 300 MHz, use P = 3.3 ns.
- (2) For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
- (3) S = Sample rate generator input clock = 2P if CLKSM = 1 (P = 1/CPU clock frequency)
= Sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)
- T = CLKX period = (1 + CLKGDV) * S
- H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
- L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
- (4) FSRP = FSXP = 1. As a SPI master, FSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on FSX and FSR is inverted before being used internally.
- CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP. CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP.
- (5) FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).

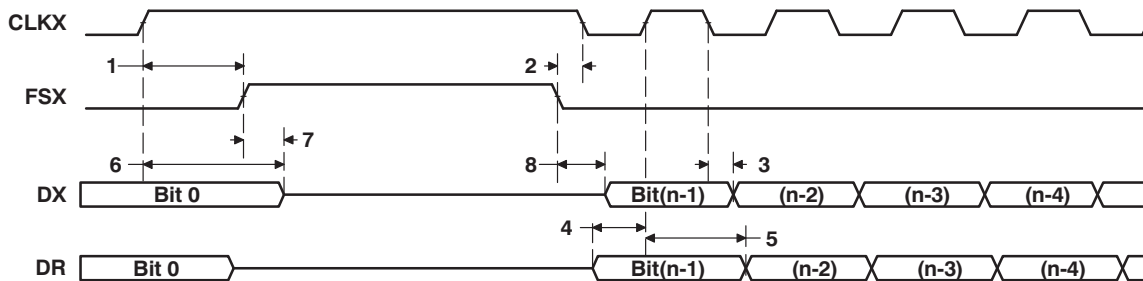


Figure 11-39. McBSP as SPI Master or Slave: CLKSTP = 10b, CLKXP = 1

Table 11-34. Timing Requirements for McBSP as SPI Master or Slave: CLKSTP = 11b, CLKXP = 1⁽¹⁾ (2)

See [Figure 11-40](#)

| NO. | | MASTER | | SLAVE | | UNIT |
|-----|--|--------|-----|---------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| 4 | $t_{su(DRV-CKXH)}$ Setup time, DR valid before CLKX high | 12 | | 2 – 6P | | ns |
| 5 | $t_h(CKXH-DRV)$ Hold time, DR valid after CLKX high | 4 | | 5 + 12P | | ns |

- (1) P = 1/CPU clock frequency in ns. For example, when running parts at 300 MHz, use P = 3.3 ns.
 (2) For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

Table 11-35. Switching Characteristics for McBSP as SPI Master or Slave: CLKSTP = 11b, CLKXP = 1⁽¹⁾ (2)

over recommended operating conditions (see [Figure 11-40](#))

| NO. | PARAMETER | 6713 | | | | 6713B | | | | UNIT |
|-----|---|-----------------------|-------|----------|----------|-----------------------|---------|--------|----------|------|
| | | MASTER ⁽³⁾ | | SLAVE | | MASTER ⁽³⁾ | | SLAVE | | |
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| 1 | $t_h(CKXH-FXL)$ Hold time, FSX low after CLKX high ⁽⁴⁾ | H – 2 | H + 3 | | | H – 2 | T + 3 | | | ns |
| 2 | $t_d(FXL-CKXL)$ Delay time, FSX low to CLKX low ⁽⁵⁾ | T – 2 | T + 3 | | | T – 2 | H + 3 | | | ns |
| 3 | $t_d(CKXH-DXV)$ Delay time, CLKX high to DX valid | –3 | 4 | 6P + 2 | 10P + 17 | –3 | 4 | 6P + 2 | 10P + 17 | ns |
| 6 | $t_{dis}(CKXH-DXHZ)$ Disable time, DX high impedance following last data bit from CLKX high | –3.6 | 4 | 6P + 1.5 | 10P + 17 | –2 | 4 | 6P + 3 | 10P + 17 | ns |
| 7 | $t_d(FXL-DXV)$ Delay time, FSX low to DX valid | L – 2 | L + 4 | 4P + 2 | 8P + 17 | L – 2 | L + 6.5 | 4P + 2 | 8P + 17 | ns |

- (1) P = 1/CPU clock frequency in ns. For example, when running parts at 300 MHz, use P = 3.3 ns.
 (2) For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
 (3) S = Sample rate generator input clock = 2P if CLKSM = 1 (P = 1/CPU clock frequency)
 = Sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)
 T = CLKX period = (1 + CLKGDV) * S
 H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even
 = (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
 L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even
 = (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
 (4) FSRP = FSXP = 1. As a SPI master, FSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on FSX and FSR is inverted before being used internally.
 CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP. CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP.
 (5) FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).

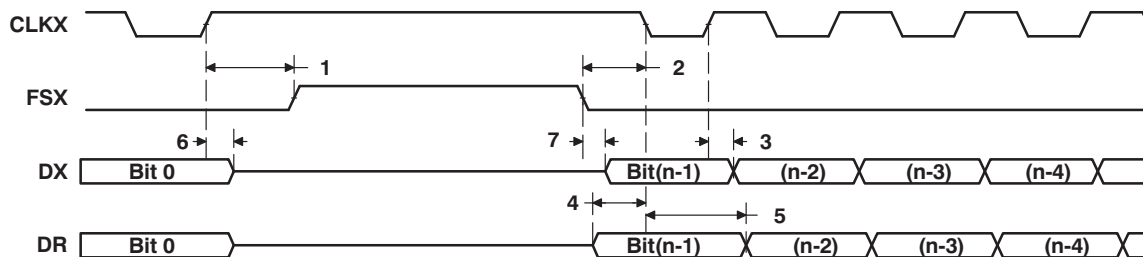


Figure 11-40. McBSP as SPI Master or Slave: CLKSTP = 11b, CLKXP = 1

11.17 Timer Timing

Table 11-36. Timing Requirements for Timer Inputs⁽¹⁾

See [Figure 11-41](#)

| NO. | | MIN | MAX | UNIT |
|-----|--|-----|-----|------|
| 1 | $t_{w(TINPH)}$ Pulse duration, TINP high | 2P | | ns |
| 2 | $t_{w(TINPL)}$ Pulse duration, TINP low | 2P | | ns |

(1) P = 1/CPU clock frequency in ns. For example, when running parts at 300 MHz, use P = 3.3 ns.

Table 11-37. Switching Characteristics for Timer Inputs⁽¹⁾

over recommended operating conditions (see [Figure 11-41](#))

| NO. | PARAMETER | MIN | MAX | UNIT |
|-----|--|--------|-----|------|
| 3 | $t_{w(TOUTH)}$ Pulse duration, TOUT high | 4P – 3 | | ns |
| 4 | $t_{w(TOURL)}$ Pulse duration, TOUT low | 4P – 3 | | ns |

(1) P = 1/CPU clock frequency in ns. For example, when running parts at 300 MHz, use P = 3.3 ns.

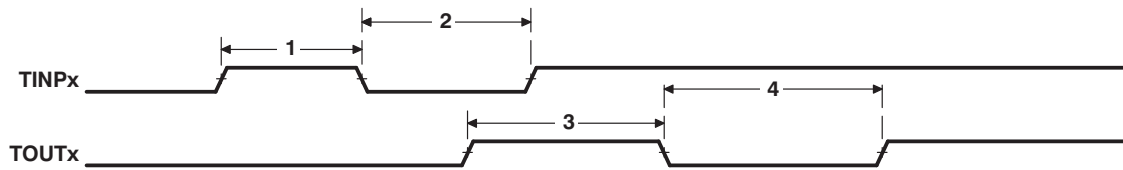


Figure 11-41. Timer

11.18 General-Purpose Input/Output (GPIO) Port Timing

Table 11-38. Timing Requirements for GPIO Inputs^{(1) (2)}

See [Figure 11-42](#)

| NO. | | MIN | MAX | UNIT |
|-----|---|-----|-----|------|
| 1 | $t_{w(GPIH)}$ Pulse duration, GPIx high | 4P | | ns |
| 2 | $t_{w(GPIL)}$ Pulse duration, GPIx low | 4P | | ns |

- (1) $P = 1/\text{CPU clock frequency}$ in ns. For example, when running parts at 300 MHz, use $P = 3.3$ ns.
 (2) The pulse width given is sufficient to generate a CPU interrupt or an EDMA event. However, if a user wants to have the DSP recognize the GPIx changes through software polling of the GPIO register, the GPIx duration must be extended to at least 24P to allow the DSP enough time to access the GPIO register through the CFGBUS.

Table 11-39. Switching Characteristics for GPIO Inputs^{(1) (2)}

over recommended operating conditions (see [Figure 11-42](#))

| NO. | PARAMETER | MIN | MAX | UNIT |
|-----|---|---------|-----|------|
| 3 | $t_{w(GPOH)}$ Pulse duration, GPOx high | 12P – 3 | | ns |
| 4 | $t_{w(GPOL)}$ Pulse duration, GPOx low | 12P – 3 | | ns |

- (1) $P = 1/\text{CPU clock frequency}$ in ns. For example, when running parts at 300 MHz, use $P = 3.3$ ns.
 (2) The number of CFGBUS cycles between two back-to-back CFGBUS writes to the GPIO register is 12 SYSCLK1 cycles; therefore, the minimum GPOx pulse width is 12P.

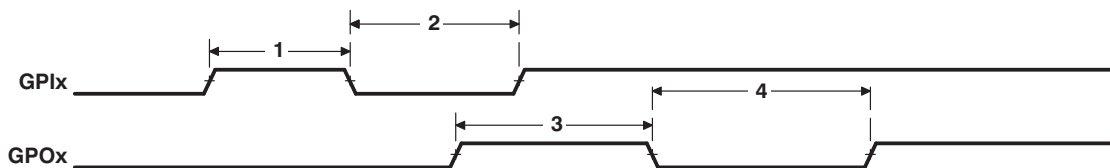


Figure 11-42. GPIO Port Timing

11.19 JTAG Test Port Timing

Table 11-40. Timing Requirements for JTAG Test Port

See [Figure 11-43](#)

| NO. | | MIN | MAX | UNIT |
|-----|--|-----|-----|------|
| 1 | $t_{c(TCK)}$ Cycle time, TCK | 35 | | ns |
| 3 | $t_{su(TDIV-TCKH)}$ Setup time, TDI/TMS/ \overline{TRST} valid before TCK high | 10 | | ns |
| 4 | $t_{h(TCKH-TDIV)}$ Hold time, TDI/TMS/ \overline{TRST} valid after TCK high | 7 | | ns |

Table 11-41. Switching Characteristics for JTAG Test Port

over recommended operating conditions (see [Figure 11-43](#))

| NO. | PARAMETER | MIN | MAX | UNIT |
|-----|---|-----|-----|------|
| 2 | $t_{d(TCKL-TDOV)}$ Delay time, TCK low to TDO valid | 0 | 15 | ns |

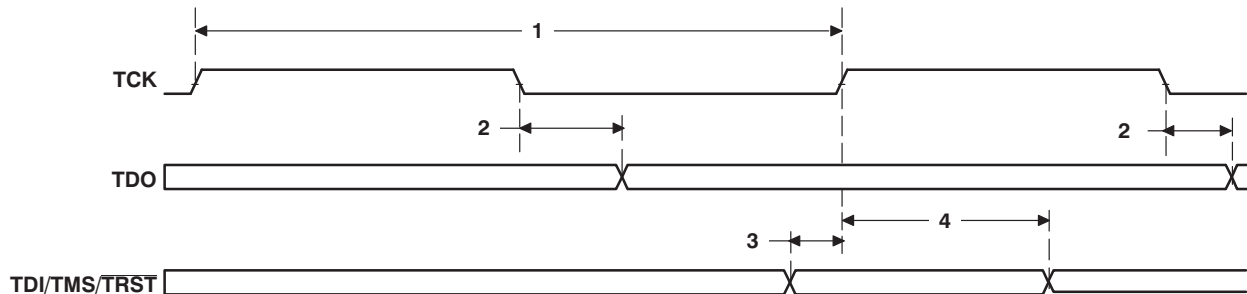


Figure 11-43. JTAG Test-Port Timing

12 MECHANICAL DATA

12.1 Mechanical Information

The following table shows the thermal resistance characteristics for the GDP package.

Table 12-1. Thermal Resistance Characteristics (S-PBGA Package) for GDP

| NO | | | °C/W | Air Flow (m/s) ⁽¹⁾ |
|--|-----------------|-------------------------|------|-------------------------------|
| Two Signals, Two Planes (4-Layer Board) | | | | |
| 1 | R θ_{JC} | Junction-to-case | 9.7 | N/A |
| 2 | Psi $_{JT}$ | Junction-to-package top | 1.5 | 0.0 |
| 3 | R θ_{JB} | Junction-to-board | 19 | N/A |
| 4 | R θ_{JA} | Junction-to-free air | 22 | 0.0 |
| 5 | R θ_{JA} | Junction-to-free air | 21 | 0.5 |
| 6 | R θ_{JA} | Junction-to-free air | 20 | 1.0 |
| 7 | R θ_{JA} | Junction-to-free air | 19 | 2.0 |
| 8 | R θ_{JA} | Junction-to-free air | 18 | 4.0 |
| 9 | Psi $_{JB}$ | Junction-to-board | 16 | 0.0 |

(1) m/s = meters per second

12.2 Packaging Information

For proper device thermal performance, the thermal pad must be soldered to an external ground thermal plane. The following packaging information and addendum reflect the most current released data available for the designated device(s). This data is subject to change without notice and without revision of this document.

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/ Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|--------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|-------------------|------------------------------|--------------------------|
| SM320C6713GDPS20EP | OBSOLETE | BGA | GDP | 272 | | TBD | Call TI | Call TI | |
| SM32C6713BGDPA20EP | ACTIVE | BGA | GDP | 272 | 40 | TBD | Call TI | Level-3-220C-168 HR | |
| SM32C6713BGDPM30EP | ACTIVE | BGA | GDP | 272 | 1 | TBD | SNPB | Level-3-220C-168 HR | |
| SM32C6713BGDPS20EP | ACTIVE | BGA | GDP | 272 | 40 | TBD | Call TI | Level-3-220C-168 HR | |
| V62/04603-02XA | ACTIVE | BGA | GDP | 272 | 40 | TBD | Call TI | Level-3-220C-168 HR | |
| V62/04603-03XA | ACTIVE | BGA | GDP | 272 | 40 | TBD | Call TI | Level-3-220C-168 HR | |
| V62/04603-04XA | ACTIVE | BGA | GDP | 272 | 1 | TBD | SNPB | Level-3-220C-168 HR | |
| V62/4603-04XA | ACTIVE | BGA | GDP | 272 | | TBD | Call TI | Call TI | |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

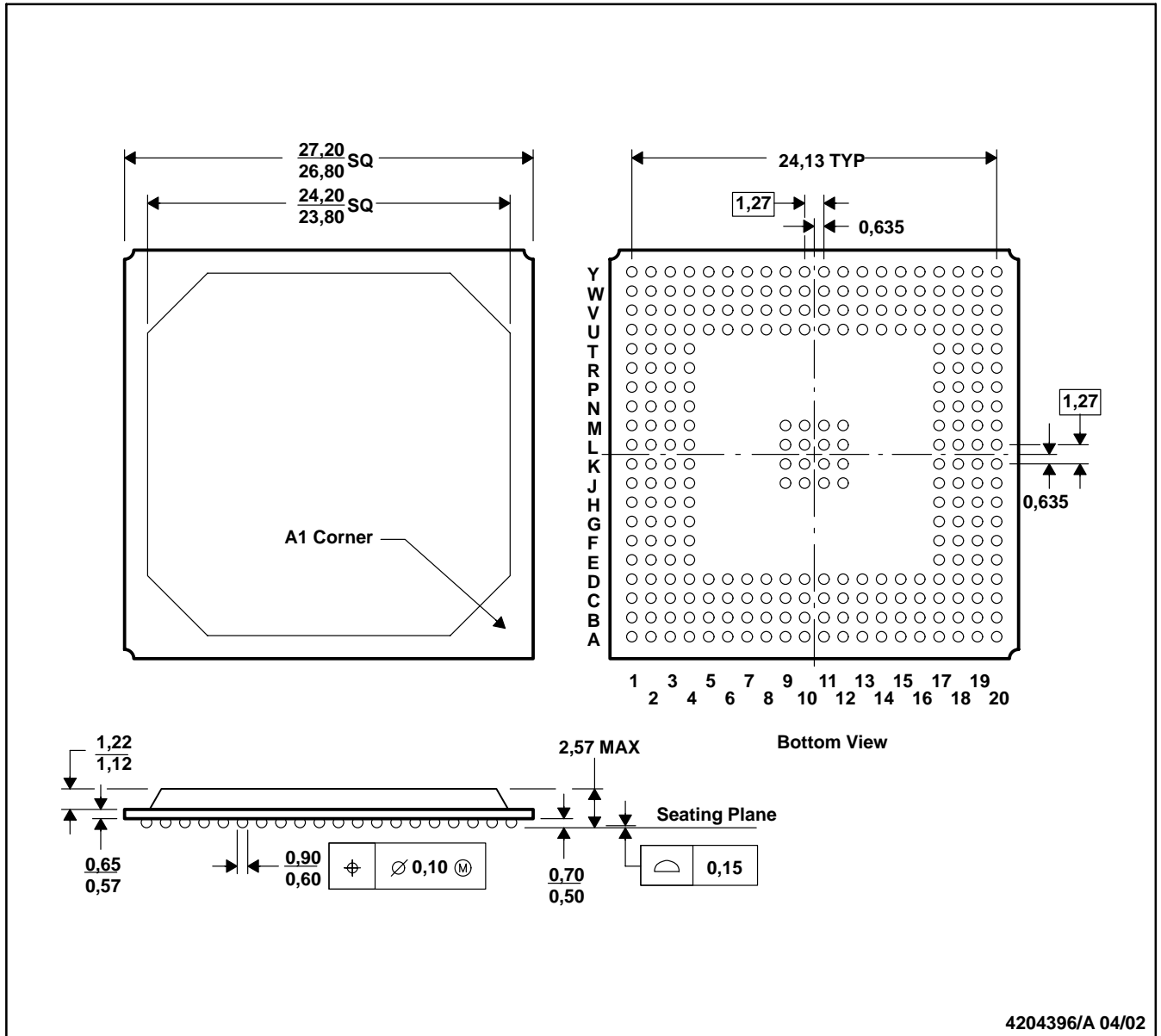
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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GDP (S-PBGA-N272)

PLASTIC BALL GRID ARRAY



4204396/A 04/02

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MO-151

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