

# 12 Output Buffer for 2 DDR and 3 SRAM DIMMS

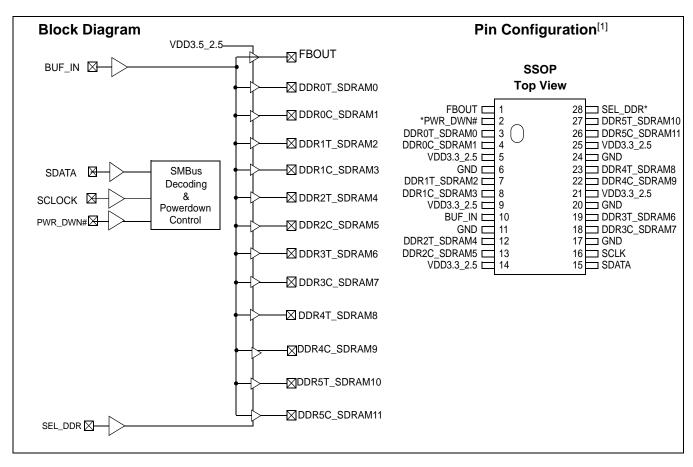
#### **Features**

- One input to 12 output buffer/drivers
- Supports up to 2 DDR DIMMs or 3 SDRAM DIMMS
- · One additional output for feedback
- SMBus interface for individual output control
- Low skew outputs (< 100 ps)
- Supports 266 MHz and 333 MHz DDR SDRAM
- · Dedicated pin for power management support
- Space-saving 28-pin SSOP package

#### **Functional Description**

The W256 is a 3.3V/2.5V buffer designed to distribute high-speed clocks in PC applications. The part has 12 outputs. Designers can configure these outputs to support 3 unbuffered standard SDRAM DIMMs and 2 DDR DIMMs. The W256 can be used in conjunction with the W250-02 or similar clock synthesizer for the VIA Pro 266 chipset.

The W256 also includes an SMBus interface which can enable or disable each output clock. On power-up, all output clocks are enabled (internal pull-up).



#### Note:

1. Internal 100K pull-up resistors present on inputs marked with \*. Design should not rely solely on internal pull-up resistor to set I/O pins HIGH.



# **Pin Summary**

Name	Pins	Description		
SEL_DDR	28	Input to configure for DDR-ONLY mode or STANDARD SDRAM mode.  1 = DDR-ONLY mode.  0 = STANDARD SDRAM mode.  When SEL_DDR is pulled HIGH or configured for DDR-ONLY mode, all the buffers will be configured as DDR outputs.  Connect VDD3.3_2.5 to a 2.5V power supply in DDR-ONLY mode.  When SEL_DDR is pulled LOW or configured for STANDARD SDRAM output, all the buffers will be configured as STANDARD SDRAM outputs.  Connect VDD3.3_2.5 to a 3.3V power supply in STANDARD SDRAM mode.		
SCLK	16	SMBus clock input.		
SDATA	15	SMBus data input.		
BUF_IN	10	<b>Reference input from chipset</b> . 2.5V input for DDR-ONLY mode; 3.3V input for STANDARD SDRAM mode.		
FBOUT	1	Feedback clock for chipset. Output voltage depends on VDD3.3_2.5V.		
PWR_DWN#	2	Active LOW input to enable Power Down mode; all outputs will be pulled LOW.		
DDR[0:5]T_SDRAM [0,2,4,6,8,10]	3, 7, 12, 19, 23, 27	<b>Clock outputs</b> . These outputs provide copies of BUF_IN. Voltage swing depends on VDD3.3_2.5 power supply.		
DDR[0:5]C_SDRAM [1,3,5,7,9, 11]	4, 8, 13, 18, 22, 26	Clock outputs. These outputs provide complementary copies of BUF_IN when SEL_DDR is active. These outputs provide copies of BUF_IN when SEL_DDR inactive. Voltage swing depends on VDD3.3_2.5 power supply.		
VDD3.3_2.5	5, 9, 14, 21, 25	Connect to 2.5V power supply when W256 is configured for DDR-ONLY mode. Connect to 3.3V power supply, when W256 is configured for standard SDRAM mode.		
GND	6, 11, 17, 20, 24	Ground.		



### **Serial Configuration Map**

 The Serial bits will be read by the clock driver in the following order:

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Byte N — Bits 7, 6, 5, 4, 3, 2, 1, 0

- Reserved and unused bits should be programmed to "0".
- SMBus Address for the W256 is:

#### Table 1.

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	0	0	1	

# Byte 6: Outputs Active/Inactive Register (1 = Active, 0 = Inactive), Default = Active

Bit	Pin#	Description	Default
Bit 7	-	Reserved, drive to 0	0
Bit 6	-	Reserved, drive to 0	0
Bit 5	_	Reserved, drive to 0	0
Bit 4	1	FBOUT	1
Bit 3	27, 26	DDR5T_SDRAM10, DDR5C_SDRAM11	1
Bit 2	_	Reserved, drive to 0	1
Bit 1	23, 22	DDR4T_SDRAM8, DDR4C_SDRAM9	1
Bit 0	-	Reserved, drive to 0	1

# Byte 7: Outputs Active/Inactive Register (1 = Active, 0 = Inactive), Default = Active

Bit	Pin#	Description	Default
Bit 7	_	Reserved, drive to 0	1
Bit 6	19, 18	DDR3T_SDRAM6, DDR3C_SDRAM7	1
Bit 5	12, 13	DDR2T_SDRAM4, DDR2C_SDRAM5	1
Bit 4	_	Reserved, drive to 0	1
Bit 3	_	Reserved, drive to 0	1
Bit 2	7, 8	DDR1T_SDRAM2, DDR1C_SDRAM3	1
Bit 1	_	Reserved, drive to 0	1
Bit 0	3, 4	DDR0T_SDRAM0, DDR0C_SDRAM1	1



#### **Maximum Ratings**

Supply Voltage to Ground Potential .......-0.5 to +7.0V DC Input Voltage (except BUF\_IN) ......-0.5V to  $V_{DD}$ +0.5 Storage Temperature ......-65°C to +150°C Static Discharge Voltage ......>2000V (per MIL-STD-883, Method 3015)

### Operating Conditions<sup>[2]</sup>

Parameter	Description	Min.	Тур.	Max.	Unit
V <sub>DD3.3</sub>	Supply Voltage	3.135		3.465	V
V <sub>DD2.5</sub>	Supply Voltage	2.375		2.625	V
T <sub>A</sub>	Operating Temperature (Ambient Temperature)	0		70	°C
C <sub>OUT</sub>	Output Capacitance		6		pF
C <sub>IN</sub>	Input Capacitance		5		pF

#### **Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions	Min.	Тур.	Max.	Unit
V <sub>IL</sub>	Input LOW Voltage	For all pins except SMBus			0.8	V
V <sub>IH</sub>	Input HIGH Voltage		2.0			V
I <sub>IL</sub>	Input LOW Current	V <sub>IN</sub> = 0V			50	μΑ
I <sub>IH</sub>	Input HIGH Current	$V_{IN} = V_{DD}$			50	μΑ
I <sub>OH</sub>	Output HIGH Current	V <sub>DD</sub> = 2.375V V <sub>OUT</sub> = 1V	-18	-32		mA
I <sub>OL</sub>	Output LOW Current	V <sub>DD</sub> = 2.375V V <sub>OUT</sub> = 1.2V	26	35		mA
V <sub>OL</sub>	Output LOW Voltage <sup>[3]</sup>	$I_{OL} = 12 \text{ mA}, V_{DD} = 2.375 \text{V}$			0.6	V
V <sub>OH</sub>	Output HIGH Voltage <sup>[3]</sup>	$I_{OH} = -12 \text{ mA}, V_{DD} = 2.375 \text{ V}$	1.7			V
I <sub>DD</sub>	Supply Current <sup>[3]</sup> (DDR-Only mode)	Unloaded outputs, 133 MHz			400	mA
I <sub>DD</sub>	Supply Current (DDR-Only mode)	Loaded outputs, 133 MHz			500	mA
I <sub>DDS</sub>	Supply Current	PWR_DWN# = 0			100	μΑ
V <sub>OUT</sub>	Output Voltage Swing	See Test Circuity (Refer to Figure 1)	0.7		V <sub>DD</sub> + 0.6	V
V <sub>oc</sub>	Output Crossing Voltage		(V <sub>DD</sub> /2) -0.1	V <sub>DD</sub> /2	(V <sub>DD</sub> /2) +0.1	V
IN <sub>DC</sub>	Input Clock Duty Cycle		48		52	%

#### Notes:

# Switching Characteristics<sup>[4]</sup>

Parameter	Name	Test Conditions	Min.	Тур.	Max.	Unit
_	Operating Frequency		66		180	MHz
_	Duty Cycle <sup>[4,5]</sup> = $t_2 \div t_1$	Measured at 1.4V for 3.3V outputs Measured at VDD/2 for 2.5V outputs.	IN <sub>DC</sub> -5%		IN <sub>DC</sub> +5%	%
t <sub>3</sub>	SDRAM Rising Edge Rate <sup>[4]</sup>	Measured between 0.4V and 2.4V	1.0		2.50	V/ns
t <sub>4</sub>	SDRAM Falling Edge Rate <sup>[4]</sup>	Measured between 2.4V and 0.4V	1.0		2.50	V/ns

<sup>2.</sup> Multiple Supplies: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

<sup>3.</sup> Parameter is guaranteed by design and characterization. Not 100% tested in production.

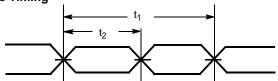


# **Switching Characteristics**<sup>[4]</sup>

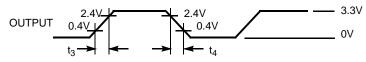
Parameter	Name	Test Conditions	Min.	Тур.	Max.	Unit
t <sub>3d</sub>	DDR Rising Edge Rate <sup>[4]</sup>	Measured between 20% to 80% of output (Refer to Figure 1)	0.5		1.50	V/ns
t <sub>4d</sub>	DDR Falling Edge Rate <sup>[4]</sup>	Measured between 20% to 80% of output (Refer to Figure 1)	0.5		1.50	V/ns
t <sub>5</sub>	Output to Output Skew <sup>[4]</sup>	All outputs equally loaded			100	ps
t <sub>6</sub>	Output t4o Output Skew for SDRAM <sup>[2]</sup>	All outputs equally loaded			150	ps
t <sub>7</sub>	SDRAM Buffer HH Prop. Delay <sup>[4]</sup>	Input edge greater than 1 V/ns	5		10	ns
t <sub>8</sub>	SDRAM Buffer LLProp. Delay <sup>[4]</sup>	Input edge greater than 1 V/ns	5		10	ns

# **Switching Waveforms**

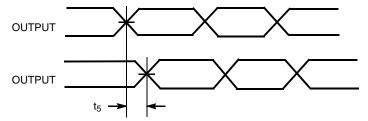
#### **Duty Cycle Timing**



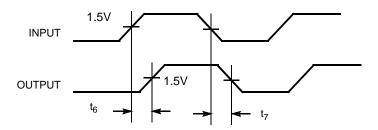
#### All Outputs Rise/Fall Time



# **Output-Output Skew**



#### **SDRAM Buffer HH and LL Propagation Delay**



- All parameters specified with loaded outputs.
   Duty cycle of input clock is 50%. Rising and falling edge rate is greater than 1V/ns.

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Figure 1 shows the differential clock directly terminated by a 120  $\Omega$  resistor.

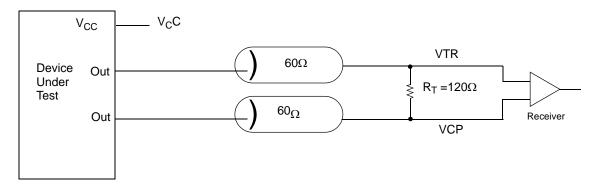
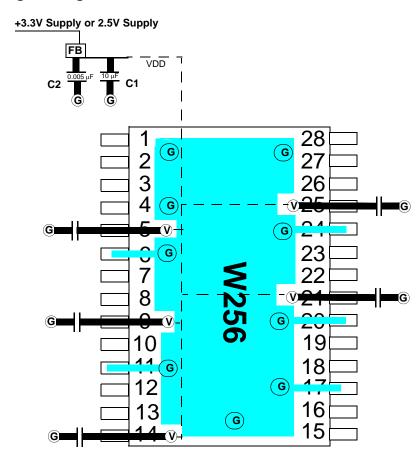


Figure 1. Differential Signal Using Direct Termination Resistor

#### **Layout Example Single Voltage**



FB = Dale ILB1206 - 300 (300 $\Omega$  @ 100 MHz)

Cermaic Caps C1 = 10–22  $\mu F$  C2 = 0.005  $\mu F$ 

G = VIA to GND plane layer V = VIA to respective supply plane layer

Note: Each supply plane or strip should have a ferrite bead and capacitors All bypass caps = 0.1  $\mu F$  ceramic

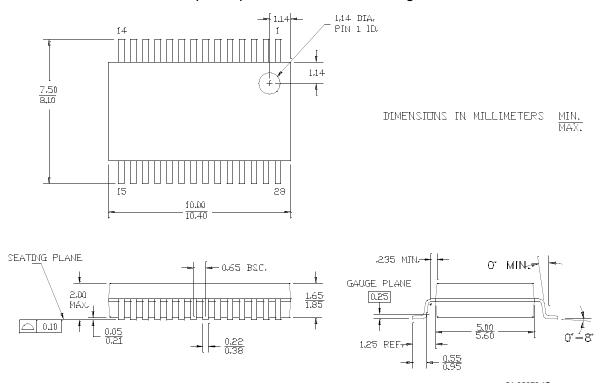


#### **Ordering Information**

Ordering Code	Package Type	Operating Range
W256H	28-pin SSOP	Commercial
W256HT	28-pin SSOP – Tape and Reel	Commercial
Lead Free		
CYW256OXC	28-pin SSOP	Commercial
CYW256OXCT	28-pin SSOP – Tape and Reel	Commercial

#### **Package Drawings and Dimension**

#### 28-Lead (5.3 mm) Shrunk Small Outline Package O28



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