## 12 Output Buffer for 2 DDR and 3 SRAM DIMMS

## Features

- One input to 12 output buffer/drivers
- Supports up to 2 DDR DIMMs or 3 SDRAM DIMMS
- One additional output for feedback
- SMBus interface for individual output control
- Low skew outputs (< 100 ps)
- Supports 266 MHz and 333 MHz DDR SDRAM
- Dedicated pin for power management support
- Space-saving 28-pin SSOP package


## Functional Description

The W 256 is a $3.3 \mathrm{~V} / 2.5 \mathrm{~V}$ buffer designed to distribute high-speed clocks in PC applications. The part has 12 outputs. Designers can configure these outputs to support 3 unbuffered standard SDRAM DIMMs and 2 DDR DIMMs. The W256 can be used in conjunction with the W250-02 or similar clock synthesizer for the VIA Pro 266 chipset.
The W256 also includes an SMBus interface which can enable or disable each output clock. On power-up, all output clocks are enabled (internal pull-up).


Note:

1. Internal 100 K pull-up resistors present on inputs marked with *. Design should not rely solely on internal pull-up resistor to set I/O pins HIGH.

W256
SILICDN LABS

## Pin Summary

$\left.$| Name | Pins | Description |
| :--- | :--- | :--- |
| SEL_DDR | 28 | Input to configure for DDR-ONLY mode or STANDARD SDRAM mode. <br> 1 = DDR-ONLY mode. <br> o = STANDARD SDRAM mode. <br> When SEL_DDR is pulled HIGH or configured for DDR-ONLY mode, all the buffers <br> will be configured as DDR outputs. <br> Connect VDD3.3_2.5 to a 2.5V power supply in DDR-ONLY mode. <br> When SEL_DDR is pulled LOW or configured for STANDARD SDRAM output, all <br> the buffers will be configured as STANDARD SDRAM outputs. <br> Connect VDD3.3_2.5 to a 3.3V power supply in STANDARD SDRAM mode. |
| SCLK | 16 | SMBus clock input. |
| SDATA | 15 | SMBus data input. |
| BUF_IN | 10 | Reference input from chipset. 2.5V input for DDR-ONLY mode; 3.3V input for <br> STANDARD SDRAM mode. |
| FBOUT | Feedback clock for chipset. Output voltage depends on VDD3.3_2.5V. |  |
| PWR_DWN\# | 2 | Active LOW input to enable Power Down mode; all outputs will be pulled LOW. |
| DDR[0:5]T_SDRAM | $3,7,12,19,23,27$ | Clock outputs. These outputs provide copies of BUF_IN. Voltage swing depends <br> on VDD3.3_2.5 power supply. |
| $0,2,4,6,8,10]$ |  |  |$\quad$| Clock outputs. These outputs provide complementary copies of BUF_IN when |
| :--- |
| SEL_DDR is active. These outputs provide copies of BUF_IN when SEL_DDR is |
| inactive. Voltage swing depends on VDD3.3_2.5 power supply. | \right\rvert\, | Connect to 2.5V power supply when W256 is configured for DDR-ONLY mode. |
| :--- |
| Connect to 3.3V power supply, when W256 is configured for standard SDRAM |
| mode. |

## Serial Configuration Map

- The Serial bits will be read by the clock driver in the following order:

Byte 0 - Bits 7, 6, 5, 4, 3, 2, 1, 0
Byte 1 - Bits 7, 6, 5, 4, 3, 2, 1, 0
.-
Byte N - Bits 7, 6, 5, 4, 3, 2, 1, 0

- Reserved and unused bits should be programmed to " 0 ".
- SMBus Address for the W256 is:

Table 1.

| A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/W |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | - |

Byte 6: Outputs Active/Inactive Register (1 = Active, $0=$ Inactive), Default = Active

| Bit | Pin \# | Description | Default |
| :---: | :---: | :--- | :---: |
| Bit 7 | - | Reserved, drive to 0 | 0 |
| Bit 6 | - | Reserved, drive to 0 | 0 |
| Bit 5 | - | Reserved, drive to 0 | 0 |
| Bit 4 | 1 | FBOUT | 1 |
| Bit 3 | 27,26 | DDR5T_SDRAM10, <br> DDR5C_SDRAM11 | 1 |
| Bit 2 | - | Reserved, drive to 0 | 1 |
| Bit 1 | 23,22 | DDR4T_SDRAM8, <br> DDR4C_SDRAM9 | 1 |
| Bit 0 | - | Reserved, drive to 0 | 1 |

Byte 7: Outputs Active/Inactive Register ( 1 = Active, 0 = Inactive), Default = Active

| Bit | Pin \# | Description | Default |
| :---: | :---: | :--- | :---: |
| Bit 7 | - | Reserved, drive to 0 | 1 |
| Bit 6 | 19,18 | DDR3T_SDRAM6, <br> DDR3C_SDRAM7 | 1 |
| Bit 5 | 12,13 | DDR2T_SDRAM4, <br> DDR2C_SDRAM5 | 1 |
| Bit 4 | - | Reserved, drive to 0 | 1 |
| Bit 3 | - | Reserved, drive to 0 | 1 |
| Bit 2 | 7,8 | DDR1T_SDRAM2, <br> DDR1C_SDRAM3 | 1 |
| Bit 1 | - | Reserved, drive to 0 | 1 |
| Bit 0 | 3,4 | DDROT_SDRAM0, <br> DDR0C_SDRAM1 | 1 |

SILICDN LABS

## Maximum Ratings

Supply Voltage to Ground Potential................. -0.5 to +7.0 V
DC Input Voltage (except BUF_IN)............ -0.5 V to $\mathrm{V}_{\mathrm{DD}}+0.5$
Storage Temperature .................................. $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$
Static Discharge Voltage ...........................................>2000V
(per MIL-STD-883, Method 3015)

## Operating Conditions ${ }^{[2]}$

| Parameter | Description | Min. | Typ. | Max. | Unit |
| :--- | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {DD3.3 }}$ | Supply Voltage | 3.135 |  | 3.465 | V |
| $\mathrm{~V}_{\text {DD2.5 }}$ | Supply Voltage | 2.375 |  | 2.625 | V |
| $\mathrm{~T}_{\mathrm{A}}$ | Operating Temperature (Ambient Temperature) | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{C}_{\text {OUT }}$ | Output Capacitance |  | 6 |  | pF |
| $\mathrm{C}_{\mathrm{IN}}$ | Input Capacitance |  | 5 |  | pF |

## Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | Min. | Typ. | Max. | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {IL }}$ | Input LOW Voltage | For all pins except SMBus |  |  | 0.8 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | Input HIGH Voltage |  | 2.0 |  |  | V |
| $I_{\text {IL }}$ | Input LOW Current | $\mathrm{V}_{\text {IN }}=0 \mathrm{~V}$ |  |  | 50 | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\mathrm{IH}}$ | Input HIGH Current | $\mathrm{V}_{\text {IN }}=\mathrm{V}_{\text {DD }}$ |  |  | 50 | $\mu \mathrm{A}$ |
| ${ }^{\mathrm{OH}}$ | Output HIGH Current | $\begin{aligned} & \mathrm{V}_{\mathrm{DD}}=2.375 \mathrm{~V} \\ & \mathrm{~V}_{\text {OUT }}=1 \mathrm{~V} \end{aligned}$ | -18 | -32 |  | mA |
| ${ }_{\text {IOL }}$ | Output LOW Current | $\begin{aligned} & \mathrm{V}_{\mathrm{DD}}=2.375 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{OUT}}=1.2 \mathrm{~V} \end{aligned}$ | 26 | 35 |  | mA |
| $\mathrm{V}_{\mathrm{OL}}$ | Output LOW Voltage ${ }^{[3]}$ | $\mathrm{l}_{\mathrm{OL}}=12 \mathrm{~mA}, \mathrm{~V}_{\mathrm{DD}}=2.375 \mathrm{~V}$ |  |  | 0.6 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | Output HIGH Voltage ${ }^{[3]}$ | $\mathrm{I}_{\mathrm{OH}}=-12 \mathrm{~mA}, \mathrm{~V}_{\mathrm{DD}}=2.375 \mathrm{~V}$ | 1.7 |  |  | V |
| ${ }^{\text {DD }}$ | Supply Current ${ }^{[3]}$ (DDR-Only mode) | Unloaded outputs, 133 MHz |  |  | 400 | mA |
| ${ }^{\text {DD }}$ | Supply Current (DDR-Only mode) | Loaded outputs, 133 MHz |  |  | 500 | mA |
| $\mathrm{I}_{\text {DDS }}$ | Supply Current | PWR_DWN\# = 0 |  |  | 100 | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\text {OUT }}$ | Output Voltage Swing | See Test Circuity (Refer to Figure 1) | 0.7 |  | $\mathrm{V}_{\mathrm{DD}}+0.6$ | V |
| $\mathrm{V}_{\text {OC }}$ | Output Crossing Voltage |  | $\begin{gathered} \hline\left(\mathrm{V}_{\mathrm{DD}} / 2\right) \\ -0.1 \end{gathered}$ | $\mathrm{V}_{\mathrm{DD}} / 2$ | $\begin{gathered} \left(\mathrm{V}_{\mathrm{DD}} / 2\right) \\ +0.1 \end{gathered}$ | V |
| $\mathrm{IN}_{\mathrm{DC}}$ | Input Clock Duty Cycle |  | 48 |  | 52 | \% |

Notes:
2. Multiple Supplies: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.
3. Parameter is guaranteed by design and characterization. Not $100 \%$ tested in production.

## Switching Characteristics ${ }^{[4]}$

| Parameter | Name | Test Conditions | Min. | Typ. | Max. | Unit |
| :--- | :--- | :--- | :---: | :---: | :---: | :---: |
| - | Operating Frequency |  | 66 |  | 180 | MHz |
| - | Duty Cycle ${ }^{[4,5]}=\mathrm{t}_{2} \div \mathrm{t}_{1}$ | Measured at 1.4V for 3.3V outputs <br> Measured at VDD/2 for 2.5 V outputs. | $\mathrm{IN}_{\mathrm{DC}}$ <br> $-5 \%$ |  | $\mathrm{IN}_{\mathrm{DC}}+5 \%$ | $\%$ |
| $\mathrm{t}_{3}$ |  | SDRAM Rising Edge Rate ${ }^{[4]}$ | Measured between 0.4 V and 2.4 V | 1.0 |  | 2.50 |
| $\mathrm{t}_{4}$ | SDRAM Falling Edge Rate ${ }^{[4]}$ | Measured between 2.4 V and 0.4 V | 1.0 |  | 2.50 | $\mathrm{~V} / \mathrm{ns}$ |

## Switching Characteristics ${ }^{[4]}$

| Parameter | Name | Test Conditions | Min. | Typ. | Max. | Unit |
| :--- | :--- | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{t}_{3 \mathrm{~d}}$ | DDR Rising Edge Rate ${ }^{[4]}$ | Measured between 20\% to 80\% of <br> output (Refer to Figure 1) | 0.5 |  | 1.50 | V/ns |
| $\mathrm{t}_{4 \mathrm{~d}}$ | DDR Falling Edge Rate ${ }^{[4]}$ | Measured between 20\% to 80\% of <br> output (Refer to Figure 1) | 0.5 |  | 1.50 | $\mathrm{~V} / \mathrm{ns}$ |
| $\mathrm{t}_{5}$ | Output to Output Skew ${ }^{[4]}$ | All outputs equally loaded |  |  | 100 | ps |
| $\mathrm{t}_{6}$ | Output t4o Output Skew for <br> SDRAM | All outputs equally loaded |  |  | 150 | ps |
| $\mathrm{t}_{7}$ | SDRAM Buffer HH Prop. Delay ${ }^{[4]}$ | Input edge greater than 1 V/ns | 5 |  | 10 | ns |
| $\mathrm{t}_{8}$ | SDRAM Buffer LLProp. Delay ${ }^{[4]}$ | Input edge greater than 1 V/ns | 5 |  | 10 | ns |

## Switching Waveforms

Duty Cycle Timing


## All Outputs Rise/Fall Time

OUTPUT


Output-Output Skew


SDRAM Buffer HH and LL Propagation Delay


## Notes:

4. All parameters specified with loaded outputs.
5. Duty cycle of input clock is $50 \%$. Rising and falling edge rate is greater than $1 \mathrm{~V} / \mathrm{ns}$.

## SILICDN LABS

Figure 1 shows the differential clock directly terminated by a $120 \Omega$ resistor.


Figure 1. Differential Signal Using Direct Termination Resistor

## Layout Example Single Voltage



FB = Dale ILB1206-300 (300 @ @ 100 MHz )
Cermaic Caps C1 $=10-22 \mu \mathrm{~F} \quad \mathrm{C} 2=0.005 \mu \mathrm{~F}$
( $)=$ VIA to GND plane layer (V) =VIA to respective supply plane layer
Note: Each supply plane or strip should have a ferrite bead and capacitors All bypass caps $=0.1 \mu \mathrm{~F}$ ceramic

## Ordering Information

| Ordering Code | Package Type | Operating Range |
| :--- | :--- | :--- |
| W256H | 28 -pin SSOP | Commercial |
| W256HT | 28 -pin SSOP - Tape and Reel | Commercial |
| Lead Free | 28-pin SSOP | Commercial |
| CYW256OXC | 28-pin SSOP - Tape and Reel | Commercial |
| CYW256OXCT |  |  |

## Package Drawings and Dimension

## 28-Lead ( 5.3 mm ) Shrunk Small Outline Package 028



The information in this document is believed to be accurate in all respects at the time of publication but is subject to change without notice. Silicon Laboratories assumes no responsibility for errors and omissions, and disclaims responsibility for any consequences resulting from the use of information included herein. Additionally, Silicon Laboratories assumes no responsibility for the functioning of undescribed features or parameters. Silicon Laboratories reserves the right to make changes without further notice. Silicon Laboratories makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Silicon Laboratories assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. Silicon Laboratories products are not designed, intended, or authorized for use in applications intended to support or sustain life, or for any other application in which the failure of the Silicon Laboratories product could create a situation where personal injury or death may occur. Should Buyer purchase or use Silicon Laboratories products for any such unintended or unauthorized application, Buyer shall indemnify and hold Silicon Laboratories harmless against all claims and damages.

