- Controlled Baseline
 - One Assembly/Test Site, One Fabrication Site
- Enhanced Diminishing Manufacturing Sources (DMS) Support
- Enhanced Product-Change Notification
- Qualification Pedigree[†]
- Low-Price/High-Performance Floating-Point Digital Signal Processors (DSPs): 320C67x™ (SM320C6712, C6712C, C6712D)
 - Eight 32-Bit Instructions/Cycle
 - 100-, 167-MHz Clock Rates
 - 10-, 6-ns Instruction Cycle Times
 - 600, 1000 MFLOPS
- Advanced Very Long Instruction Word (VLIW) C67x™ DSP Core
 - Eight Highly Independent Functional Units:
 - Four ALUs (Floating- and Fixed-Point)
 - Two ALUs (Fixed-Point)
 - Two Multipliers (Floating- and Fixed-Point)
 - Load-Store Architecture With 32 32-Bit General-Purpose Registers
 - Instruction Packing Reduces Code Size
 - All Instructions Conditional
- Instruction Set Features
 - Hardware Support for IEEE
 Single-Precision and Double-Precision
 Instructions
 - Byte-Addressable (8-, 16-, 32-Bit Data)
 - 8-Bit Overflow Protection
 - Saturation
 - Bit-Field Extract, Set, Clear
 - Bit-Counting
 - Normalization
- Device Configuration
 - Boot Mode: 8- and 16-Bit ROM Boot
 - Endianness: Little Endian (12/12C)
 Little Endian, Big Endian (12D)

- L1/L2 Memory Architecture
 - 32K-Bit (4K-Byte) L1P Program Cache (Direct Mapped)
 - 32K-Bit (4K-Byte) L1D Data Cache (2-Way Set-Associative)
 - 512K-Bit (64K-Byte) L2 Unified Mapped RAM/Cache
 - (Flexible Data/Program Allocation)
- Enhanced Direct-Memory-Access (EDMA)
 Controller (16 Independent Channels)
- 16-Bit External Memory Interface (EMIF)
 - Glueless Interface to Asynchronous Memories: SRAM and EPROM
 - Glueless Interface to Synchronous Memories: SDRAM and SBSRAM
 - 256M-Byte Total Addressable External Memory Space
- Two Multichannel Buffered Serial Ports (McBSPs)
 - Direct Interface to T1/E1, MVIP, SCSA Framers
 - ST-Bus-Switching Compatible
 - Up to 256 Channels Each
 - AC97-Compatible
 - Serial-Peripheral-Interface (SPI)
 Compatible (Motorola™)
- Two 32-Bit General-Purpose Timers
- Flexible Phase-Locked-Loop (PLL) Clock Generator [C6712]
- Flexible Software-Configurable PLL-Based Clock Generator Module [C6712C/C6712D]
- A Dedicated General-Purpose Input/Output (GPIO) Module With 5 Pins [12C/12D]
- IEEE-1149.1 (JTAG[‡])
 Boundary-Scan-Compatible
- CMOS Technology
 - 0.13-μm/6-Level Copper Metal Process (C6712C/C6712D)
 - 0.18-um/5-Level Metal Process (C6712)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

320C67x and C67x are trademarks of Texas Instruments. Motorola is a trademark of Motorola, Inc. Other trademarks are the property of their respective owners.

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits. ‡ IEEE Standard 1149.1-1990 Standard-Test-Access Port and Boundary Scan Architecture.

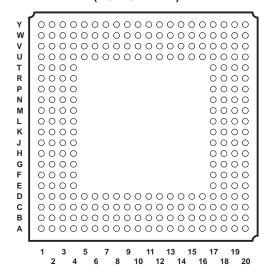


SGUS055 - SEPTEMBER 2004

| GFN BGA package (bottom view) [C6712 only] 3 | EMIF device speed |
|--|---|
| GDP BGA package (bottom view) [C6712C/12D only] 3 | EMIF big endian mode correctness [C6712D only] 60 |
| description 4 | bootmode |
| device characteristics 5 device compatibility 6 functional block and CPU (DSP core) diagram 7 CPU (DSP core) description 8 | absolute maximum ratings over operating case temperature range |
| memory map summary | supply voltage and operating case temperature . 63 |
| peripheral register descriptions | parameter measurement information 64 signal transition levels 65 timing parameters and board routing analysis 65 input and output clocks 67 asynchronous memory timing 72 synchronous-burst memory timing 75 synchronous DRAM timing 77 HOLD/HOLDA timing 83 BUSREQ timing 84 reset timing [C6712] 85 reset timing [C6712C/C6712D] 87 external interrupt timing 89 multichannel buffered serial port timing 90 timer timing 90 general-purpose input/output (GPIO) port timing 104 general-purpose input/output (GPIO) port timing 105 JTAG test-port timing 106 mechanical data [C6712 only] 107 mechanical data [C6712C/C6712D only] 107 mechanical data [C6712C/C6712D only] 108 |

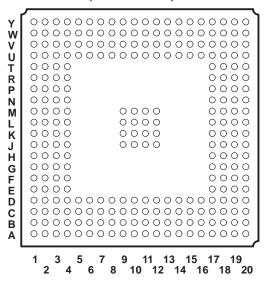
GFN BGA package (bottom view) [C6712 only]

GFN 256-PIN BALL GRID ARRAY (BGA) PACKAGE (BOTTOM VIEW)



GDP BGA package (bottom view) [C6712C/12D only]

GDP 272-PIN BALL GRID ARRAY (BGA) PACKAGE (BOTTOM VIEW)



SGUS055 - SEPTEMBER 2004

description

The 320C67x[™] DSPs (including the SM320C6712-EP, SM320C6712C-EP, SM320C6712D-EP devices[†]) are members of the floating-point DSP family in the TMS320C6000[™] DSP platform. The C6712, C6712C, and C6712D devices are based on the high-performance, advanced very-long-instruction-word (VLIW) architecture developed by Texas Instruments (TI), making these DSPs an excellent choice for multichannel and multifunction applications.

With performance of up to 1000 million floating-point operations per second (MFLOPS) at a clock rate of 167 MHz, the C6712C/C6712D device is the lowest-cost DSP in the C6000™ DSP platform. The C6712C/C6712D DSP possesses the operational flexibility of high-speed controllers and the numerical capability of array processors. This processor has 32 general-purpose registers of 32-bit word length and eight highly independent functional units. The eight functional units provide four floating-/fixed-point ALUs, two fixed-point ALUs, and two floating-/fixed-point multipliers. The C6712C/C6712D can produce two MACs per cycle for a total of 300 MMACS.

With performance of up to 600 million floating-point operations per second (MFLOPS) at a clock rate of 100 MHz, the C6712 device also offers cost-effective solutions to high-performance DSP programming challenges. The C6712 DSP possesses the operational flexibility of high-speed controllers and the numerical capability of array processors. This processor has 32 general-purpose registers of 32-bit word length and eight highly independent functional units. The eight functional units provide four floating-/fixed-point ALUs, two fixed-point ALUs, and two floating-/fixed-point multipliers. The C6712 can produce two multiply-accumulates (MACs) per cycle for a total of 200 million MACs per second (MMACS).

The C6712/C6712D uses a two-level cache-based architecture and has a powerful and diverse set of peripherals. The Level 1 program cache (L1P) is a 32-Kbit direct mapped cache and the Level 1 data cache (L1D) is a 32-Kbit 2-way set-associative cache. The Level 2 memory/cache (L2) consists of a 512-Kbit memory space that is shared between program and data space. L2 memory can be configured as mapped memory, cache, or combinations of the two. The peripheral set includes two multichannel buffered serial ports (McBSPs), two general-purpose timers, and a glueless 16-bit external memory interface (EMIF) capable of interfacing to SDRAM, SBSRAM, and asynchronous peripherals. The C6712C device also includes a dedicated general-purpose input/output (GPIO) peripheral module.

The C6712/C6712D DSPs also have application-specific hardware logic, on-chip memory, and additional on-chip peripherals.

The C6712/C6712D has a complete set of development tools which includes: a new C compiler, an assembly optimizer to simplify programming and scheduling, and a Windows[™] debugger interface for visibility into source code execution.

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† Throughout the remainder of this document, the SM320C6712-EP, SM320C6712C-EP, and SM320C6712D-EP shall be referred to as 320C67x or C67x where generic, and where specific, their individual full device part numbers will be used or abbreviated as C6712, C6712C, C6712D, 12, 12C, or 12D, etc.



device characteristics

Table 1 provides an overview of the C6712/C6712C DSPs. The table shows significant features of each device, including the capacity of on-chip RAM, the peripherals, the execution time, and the package type with pin count. For more details on the C6000™ DSP device part numbers and part numbering, see Table 17 and Figure 5.

Table 1. Characteristics of the C6712, C6712C, and C6712D Processors

| HARDWARE FEATURES | | INTERNAL CLOCK SOURCE | C6712 (FLOATING-POINT DSP) | C6712C/C6712D (FLOATING-POINT DSPs) |
|---|---------------------------------------|--------------------------|---|--|
| | 5145 | ECLKIN | 1 | |
| | EMIF | SYSCLK3 or ECLKIN | | 1 |
| | EDMA | CPU clock frequency | 1 | 1 |
| Destate and | M-DOD- | CPU/2 clock frequency | 2 | _ |
| Peripherals | McBSPs | SYSCLK2 | _ | 2 |
| | 00 B' T | CPU/4 clock frequency | 2 | _ |
| | 32-Bit Timers | 1/2 of SYSCLK2 | _ | 2 |
| | GPIO Module | SYSCLK2 | _ | 1 |
| | Size (Bytes) | | 72K | 72K |
| On-Chip Memory | Organization | | 4K-Byte (4KB) L1 Program (L1P) Cache 4KB L1 Data (L1D) Cache 64KB Unified Mapped RAM/Cache (L2) | |
| CPU ID+ CPU Rev ID | Control Status Register (CSR.[31:16]) | | 0x0202 | 0x0203 |
| Frequency | MHz | | 100 | 167 |
| Cycle Time | ns | | 10 ns (C6712-100) | 6 ns (C6712D-167) 6 ns (C6712C-167) |
| | Core (V) | | 1.8 | 1.20‡ |
| Voltage | I/O (V) | | 3.3 | 3.3 |
| PLL Options | CLKIN frequency | multiplier | Bypass (x1), x4 | - |
| Clock Generator Options | Prescaler Multiplier Postscaler | | _ | /1, /2, /3,, /32 x4, x5, x6,, x25 /1, /2, /3,, /32 |
| BGA Package | 27 x 27 mm | | 256-Pin BGA (GFN) | 272-Pin BGA (GDP) |
| Process Technology | μm | | 0.18 μm | 0.13 μm |
| Product Status Product Preview (PP) Advance Information (AI) Production Data (PD) | | PP† | PP (C6712C) [†] PD (C6712D) [†] | |

[†] PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

ADVANCE INFORMATION concerns new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

[‡]This value is compatible with existing 1.26V designs.

SGUS055 - SEPTEMBER 2004

device compatibility

The 320C6712 and C6211/C6711 devices are pin-compatible; thus, making new system designs easier and providing faster time to market. The following list summarizes the device characteristic differences among the C6211, C6211B, C6711, C6711B, C6711C, C6711D, C6712, C6712C, and C6712D devices:

- The C6211 and C6211B devices have a fixed-point TMS320C62x[™] DSP core (CPU), while the C6711, C6711B, C6711C, C6711D, C6712, C6712C, and C6712D devices have a floating-point C67x™ CPU.
- The C6211, C6211B, C6711, C6711B, C6711C, and C6711D devices have a 32-bit EMIF, while the C6712, C6712C, and C6712D devices have a 16-bit EMIF.
- The C6211, C6211B, C6711, C6711B, C6711C, and C6711D devices feature an HPI, while the C6712, C6712C, and C6712D devices do not.
- The C6712, C6712C, and C6712D devices have dedicated device configuration pins, BOOTMODE, LENDIAN, and EMIFBE (12D only) that specify the boot-load operation and device endianness, respectively, during reset. On the C6211/C6211B and C6711/C6711B/C6711C/C6711D devices, these configuration pins are integrated with the HPI pins.
- The C6211/C6211B device runs at -167 and -150 MHz clock speeds (with a C6211BGFNA extended temperature device that also runs at -150 MHz), while the C6711/C6711B device runs at -150 and -100 MHz (with a C6711BGFNA extended temperature device that also runs at -100 MHz) and the C6711C/C6711D device runs at -200 clock speed (with a C6711CGDPA extended temperature device that also runs at -167 MHz). The C6712 device runs at -100 MHz clock speed and the C6712C/C6712D device runs at -167 MHz clock speed.
- The C6211/C6211B, C6711-100, C6711B and C6712 devices have a core voltage of 1.8 V, the C6711-150 device has a core voltage is 1.9 V, and the C6711C/C6711D and C6712C/C6712D devices operate with a core voltage of 1.20[†] V.
- There are several enhancements and features that are only available on the C6711C/C6711D and C6712C/C6712D devices, such as: the CLKOUT3 signal, a software-programmable PLL and PLL Controller, and a GPIO peripheral module. The C6711D and C6712D devices also have additional enhancements such as: EMIF Big Endian mode correctness EMIFBE and the L1D requestor priority to L2 bit ["P" bit] in the cache configuration (CCFG) register. C6712D supports Big Endian mode.
- The C6712/C6712D is the lowest-cost entry in the TMS320C6000™ platform.

For a more detailed discussion on the similarities/differences among the C6211, C6711, and C6712 devices, see the How to Begin Development Today with the TMS320C6211 DSP, How to Begin Development with the TMS320C6711 DSP, and How to Begin Development With the TMS320C6712 DSP application reports (literature number SPRA474, SPRA522, and SPRA693, respectively).

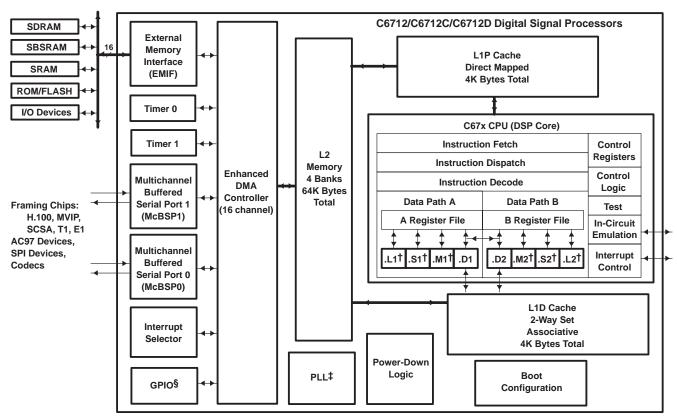
For a more detailed discussion on the migration of a C6211, C6211B, C6711, or C6711B device to a TMS320C6711C device, see the Migrating from TMS320C6211(B)/6711(B) to TMS320C6711C application report (literature number SPRA837).

For a more detailed discussion on the migration of a C6712 device to a TMS320C6712C device, see the Migrating from TMS320C6712 to TMS320C6712C application report (literature number SPRA852).

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functional block and CPU (DSP core) diagram



[†] In addition to fixed-point instructions, these functional units execute floating-point instructions.

[‡] The C6712C/C6712D device has a software-configurable PLL (with x4 through x25 multiplier and /1 through /32 divider) and a PLL Controller which is different from the hardware PLL peripheral on the C6712 device.

[§] Applicable to the C6712C/C6712D device only

SGUS055 - SEPTEMBER 2004

CPU (DSP core) description

The CPU fetches advanced very-long instruction words (VLIW) (256 bits wide) to supply up to eight 32-bit instructions to the eight functional units during every clock cycle. The VLIW architecture features controls by which all eight units do not have to be supplied with instructions if they are not ready to execute. The first bit of every 32-bit instruction determines if the next instruction belongs to the same execute packet as the previous instruction, or whether it should be executed in the following clock as a part of the next execute packet. Fetch packets are always 256 bits wide; however, the execute packets can vary in size. The variable-length execute packets are a key memory-saving feature, distinguishing the C67x CPU from other VLIW architectures.

The CPU features two sets of functional units. Each set contains four units and a register file. One set contains functional units .L1, .S1, .M1, and .D1; the other set contains units .D2, .M2, .S2, and .L2. The two register files each contain 16 32-bit registers for a total of 32 general-purpose registers. The two sets of functional units, along with two register files, compose sides A and B of the CPU [see the functional block and CPU (DSP Core) diagram and Figure 1]. The four functional units on each side of the CPU can freely share the 16 registers belonging to that side. Additionally, each side features a single data bus connected to all the registers on the other side, by which the two sets of functional units can access data from the register files on the opposite side. While register access by functional units on the same side of the CPU as the register file can service all the units in a single clock cycle, register access using the register file across the CPU supports one read and one write per cycle.

The C67x CPU executes all C62x[™] DSP instructions. In addition to C62x[™] fixed-point DSP instructions, the six out of eight functional units (.L1, .M1, .D1, .D2, .M2, and .L2) also execute floating-point instructions. The remaining two functional units (.S1 and .S2) also execute the new LDDW instruction which loads 64 bits per CPU side for a total of 128 bits per cycle.

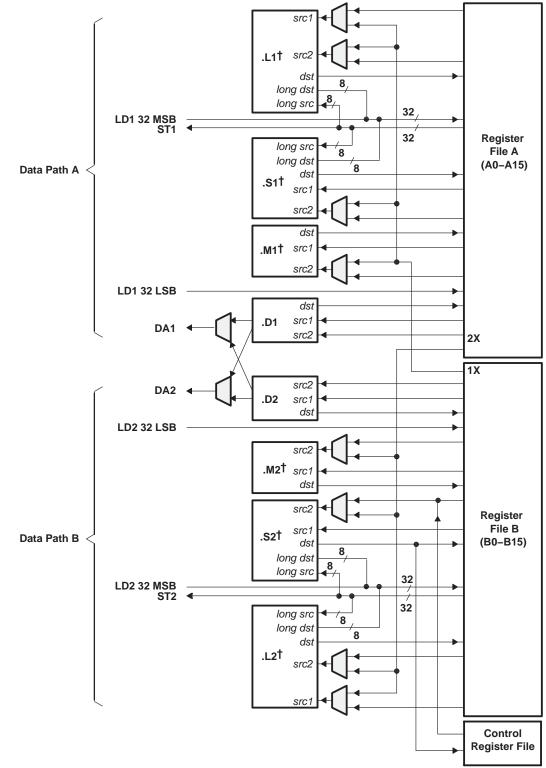
Another key feature of the C67x CPU is the load/store architecture, where all instructions operate on registers (as opposed to data in memory). Two sets of data-addressing units (.D1 and .D2) are responsible for all data transfers between the register files and the memory. The data address driven by the .D units allows data addresses generated from one register file to be used to load or store data to or from the other register file. The C67x CPU supports a variety of indirect addressing modes using either linear- or circular-addressing modes with 5- or 15-bit offsets. All instructions are conditional, and most can access any one of the 32 registers. Some registers, however, are singled out to support specific addressing or to hold the condition for conditional instructions (if the condition is not automatically "true"). The two .M functional units are dedicated for multiplies. The two .S and .L functional units perform a general set of arithmetic, logical, and branch functions with results available every clock cycle.

The processing flow begins when a 256-bit-wide instruction fetch packet is fetched from a program memory. The 32-bit instructions destined for the individual functional units are "linked" together by "1" bits in the least significant bit (LSB) position of the instructions. The instructions that are "chained" together for simultaneous execution (up to eight in total) compose an execute packet. A "0" in the LSB of an instruction breaks the chain, effectively placing the instructions that follow it in the next execute packet. If an execute packet crosses the fetch-packet boundary (256 bits wide), the assembler places it in the next fetch packet, while the remainder of the current fetch packet is padded with NOP instructions. The number of execute packets within a fetch packet can vary from one to eight. Execute packets are dispatched to their respective functional units at the rate of one per clock cycle and the next 256-bit fetch packet is not fetched until all the execute packets from the current fetch packet have been dispatched. After decoding, the instructions simultaneously drive all active functional units for a maximum execution rate of eight instructions every clock cycle. While most results are stored in 32-bit registers, they can be subsequently moved to memory as bytes or half-words as well. All load and store instructions are byte-, half-word, or word-addressable.

C62x is a trademark of Texas Instruments.



CPU (DSP core) description (continued)



[†] In addition to fixed-point instructions, these functional units execute floating-point instructions.

Figure 1. 320C67x[™] CPU (DSP Core) Data Paths



SGUS055 - SEPTEMBER 2004

memory map summary

Table 2 shows the memory map address ranges of the C6712/C6712C/C6712D devices. Internal memory is always located at address 0 and can be used as both program and data memory. The C6712/C6712C/C6712D configuration registers for the common peripherals are located at the same hex address ranges. The external memory address ranges in the C6712/C6712C/C6712D devices begin at the address location 0x8000 0000.

Table 2. 320C6712/C6712C/C6712D Memory Map Summary

| MEMORY BLOCK DESCRIPTION | BLOCK SIZE (BYTES) | HEX ADDRESS RANGE |
|---|--------------------|-----------------------|
| Internal RAM (L2) | 64K | 0000 0000 – 0000 FFFF |
| Reserved | 24M – 64K | 0001 0000 – 017F FFFF |
| External Memory Interface (EMIF) Registers | 256K | 0180 0000 – 0183 FFFF |
| L2 Registers | 256K | 0184 0000 – 0187 FFFF |
| Reserved | 256K | 0188 0000 – 018B FFFF |
| McBSP 0 Registers | 256K | 018C 0000 – 018F FFFF |
| McBSP 1 Registers | 256K | 0190 0000 – 0193 FFFF |
| Timer 0 Registers | 256K | 0194 0000 – 0197 FFFF |
| Timer 1 Registers | 256K | 0198 0000 – 019B FFFF |
| Interrupt Selector Registers | 512 | 019C 0000 - 019C 01FF |
| Device Configuration Registers [C6712C/C6712D only] | 4 | 019C 0200 - 019C 0203 |
| Reserved | 256K – 516 | 019C 0204 – 019F FFFF |
| EDMA RAM and EDMA Registers | 256K | 01A0 0000 – 01A3 FFFF |
| Reserved | 768K | 01A4 0000 – 01AF FFFF |
| GPIO Registers [C6712C/C6712D only] | 16K | 01B0 0000 - 01B0 3FFF |
| Reserved | 480K | 01B0 4000 – 01B7 BFFF |
| PLL Controller Registers [C6712C/C6712D only] | 8K | 01B7 C000 – 01B7 DFFF |
| Reserved | 4M + 520K | 01B7 E000 – 01FF FFFF |
| QDMA Registers | 52 | 0200 0000 – 0200 0033 |
| Reserved | 736M – 52 | 0200 0034 – 2FFF FFFF |
| McBSP 0 Data/Peripheral Data Bus | 64M | 3000 0000 – 33FF FFFF |
| McBSP 1 Data/Peripheral Data Bus | 64M | 3400 0000 – 37FF FFFF |
| Reserved | 64M | 3800 0000 – 3BFF FFFF |
| Reserved | 1G + 64M | 3C00 0000 – 7FFF FFFF |
| EMIF CE0 [†] | 256M | 8000 0000 – 8FFF FFFF |
| EMIF CE1 [†] | 256M | 9000 0000 – 9FFF FFFF |
| EMIF CE2 [†] | 256M | A000 0000 – AFFF FFFF |
| EMIF CE3 [†] | 256M | B000 0000 – BFFF FFFF |
| Reserved | 1G | C000 0000 – FFFF FFFF |

[†] The number of EMIF address pins (EA[21:2]) limits the maximum addressable memory (SDRAM) to 128MB per CE space. To get 256MB of addressable memory, additional general-purpose output pin or external logic is required.

peripheral register descriptions

Table 3 through Table 13 identify the peripheral registers for the C6712/C6712C/C6712D devices by their register names, acronyms, and hex address or hex address range. For more detailed information on the register contents, bit names, and their descriptions, see the specific peripheral reference guide listed in the TMS320C6000 DSP Peripherals Overview Reference Guide (literature number SPRU190).

Table 3. EMIF Registers

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|-----------------------|---------|----------------------------|
| 0180 0000 | GBLCTL | EMIF global control |
| 0180 0004 | CECTL1 | EMIF CE1 space control |
| 0180 0008 | CECTL0 | EMIF CE0 space control |
| 0180 000C | - | Reserved |
| 0180 0010 | CECTL2 | EMIF CE2 space control |
| 0180 0014 | CECTL3 | EMIF CE3 space control |
| 0180 0018 | SDCTL | EMIF SDRAM control |
| 0180 001C | SDTIM | EMIF SDRAM refresh control |
| 0180 0020 | SDEXT | EMIF SDRAM extension |
| 0180 0024 – 0183 FFFF | - | Reserved |

Table 4. L2 Cache Registers

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME | |
|-----------------------|----------|--|--|
| 0184 0000 | CCFG | Cache configuration register | |
| 0184 4000 | L2WBAR | L2 writeback base address register | |
| 0184 4004 | L2WWC | L2 writeback word count register | |
| 0184 4010 | L2WIBAR | L2 writeback-invalidate base address register | |
| 0184 4014 | L2WIWC | L2 writeback-invalidate word count register | |
| 0184 4020 | L1PIBAR | L1P invalidate base address register | |
| 0184 4024 | L1PIWC | L1P invalidate word count register | |
| 0184 4030 | L1DWIBAR | L1D writeback-invalidate base address register | |
| 0184 4034 | L1DWIWC | L1D writeback-invalidate word count register | |
| 0184 5000 | L2WB | L2 writeback all register | |
| 0184 5004 | L2WBINV | L2 writeback-invalidate all register | |
| 0184 8200 | MAR0 | Controls CE0 range 8000 0000 – 80FF FFFF | |
| 0184 8204 | MAR1 | Controls CE0 range 8100 0000 – 81FF FFFF | |
| 0184 8208 | MAR2 | Controls CE0 range 8200 0000 – 82FF FFFF | |
| 0184 820C | MAR3 | Controls CE0 range 8300 0000 – 83FF FFFF | |
| 0184 8240 | MAR4 | Controls CE1 range 9000 0000 – 90FF FFFF | |
| 0184 8244 | MAR5 | Controls CE1 range 9100 0000 – 91FF FFFF | |
| 0184 8248 | MAR6 | Controls CE1 range 9200 0000 – 92FF FFFF | |
| 0184 824C | MAR7 | Controls CE1 range 9300 0000 – 93FF FFFF | |
| 0184 8280 | MAR8 | Controls CE2 range A000 0000 – A0FF FFFF | |
| 0184 8284 | MAR9 | Controls CE2 range A100 0000 – A1FF FFFF | |
| 0184 8288 | MAR10 | Controls CE2 range A200 0000 – A2FF FFFF | |
| 0184 828C | MAR11 | Controls CE2 range A300 0000 – A3FF FFFF | |
| 0184 82C0 | MAR12 | Controls CE3 range B000 0000 – B0FF FFFF | |
| 0184 82C4 | MAR13 | Controls CE3 range B100 0000 – B1FF FFFF | |
| 0184 82C8 | MAR14 | Controls CE3 range B200 0000 – B2FF FFFF | |
| 0184 82CC | MAR15 | Controls CE3 range B300 0000 – B3FF FFFF | |
| 0184 82D0 - 0187 FFFF | _ | Reserved | |

SGUS055 - SEPTEMBER 2004

peripheral register descriptions (continued)

Table 5. Interrupt Selector Registers

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME | COMMENTS |
|-----------------------|---------|-----------------------------|---|
| 019C 0000 | MUXH | Interrupt multiplexer high | Selects which interrupts drive CPU interrupts 10–15 (INT10–INT15) |
| 019C 0004 | MUXL | Interrupt multiplexer low | Selects which interrupts drive CPU interrupts 4–9 (INT04–INT09) |
| 019C 0008 | EXTPOL | External interrupt polarity | Sets the polarity of the external interrupts (EXT_INT4-EXT_INT7) |
| 019C 000C – 019F FFFF | _ | Reserved | |

Table 6. Device Registers

| HEX ADDRESS RANGE | ACRONYM | REGISTER DESCRIPTION | |
|-----------------------|---------|-----------------------------|---|
| 019C 0200 | DEVCFG | Device Configuration | This C6712C/C6712D-only register allows the user control of the EMIF input clock source. For more detailed information on the device configuration register, see the Device Configurations section of this data sheet. |
| 019C 0204 – 019F FFFF | - | Reserved | |
| N/A | CSR | CPU Control Status Register | Identifies which CPU and defines the silicon revision of the CPU. This register also offers the user control of device operation. For more detailed information on the CPU Control Status Register, see the CPU CSR Register Description section of this data sheet. |

Table 7. EDMA Parameter RAM[†]

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|------------------------|---------|---|
| 01A0 0000 – 01A0 0017 | _ | Parameters for Event 0 (6 words) or Reload/Link Parameters for other Event |
| 01A0 0018 - 01A0 002F | _ | Parameters for Event 1 (6 words) or Reload/Link Parameters for other Event |
| 01A0 0030 - 01A0 0047 | 1 | Parameters for Event 2 (6 words) or Reload/Link Parameters for other Event |
| 01A0 0048 - 01A0 005F | _ | Parameters for Event 3 (6 words) or Reload/Link Parameters for other Event |
| 01A0 0060 - 01A0 0077 | _ | Parameters for Event 4 (6 words) or Reload/Link Parameters for other Event |
| 01A0 0078 - 01A0 008F | _ | Parameters for Event 5 (6 words) or Reload/Link Parameters for other Event |
| 01A0 0090 - 01A0 00A7 | - | Parameters for Event 6 (6 words) or Reload/Link Parameters for other Event |
| 01A0 00A8 - 01A0 00BF | _ | Parameters for Event 7 (6 words) or Reload/Link Parameters for other Event |
| 01A0 00C0 - 01A0 00D7 | _ | Parameters for Event 8 (6 words) or Reload/Link Parameters for other Event |
| 01A0 00D8 - 01A0 00EF | _ | Parameters for Event 9 (6 words) or Reload/Link Parameters for other Event |
| 01A0 00F0 - 01A0 00107 | _ | Parameters for Event 10 (6 words) or Reload/Link Parameters for other Event |
| 01A0 0108 - 01A0 011F | _ | Parameters for Event 11 (6 words) or Reload/Link Parameters for other Event |
| 01A0 0120 - 01A0 0137 | _ | Parameters for Event 12 (6 words) or Reload/Link Parameters for other Event |
| 01A0 0138 - 01A0 014F | _ | Parameters for Event 13 (6 words) or Reload/Link Parameters for other Event |
| 01A0 0150 - 01A0 0167 | _ | Parameters for Event 14 (6 words) or Reload/Link Parameters for other Event |
| 01A0 0168 – 01A0 017F | _ | Parameters for Event 15 (6 words) or Reload/Link Parameters for other Event |
| 01A0 0180 – 01A0 0197 | - | Reload/link parameters for Event 0–15 |
| 01A0 0198 – 01A0 01AF | - | Reload/link parameters for Event 0–15 |
| | | |
| 01A0 07E0 - 01A0 07F7 | - | Reload/link parameters for Event 0–15 |
| 01A0 07F8 - 01A0 07FF | _ | Scratch pad area (2 words) |

[†] The C6712/C6712C/C6712D device has 85 EDMA parameters total: 16 Event/Reload parameters and 69 Reload-only parameters.



peripheral register descriptions (continued)

For more details on the EDMA parameter RAM 6-word parameter entry structure, see Figure 2.

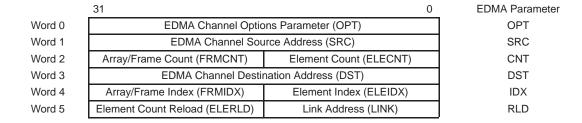


Figure 2. EDMA Channel Parameter Entries (6 Words) for Each EDMA Event

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME | |
|-----------------------|---------|--|--|
| 01A0 0800 - 01A0 FEFC | - | Reserved | |
| 01A0 FF00 | ESEL0 | EDMA event selector 0 [C6712C/C6712D Only] | |
| 01A0 FF04 | ESEL1 | EDMA event selector 1 [C6712C/C6712D Only] | |
| 01A0 FF08 - 01A0 FF0B | - | Reserved | |
| 01A0 FF0C | ESEL3 | EDMA event selector 3 [C6712C/C6712D Only] | |
| 01A0 FF1F - 01A0 FFDC | - | Reserved | |
| 01A0 FFE0 | PQSR | Priority queue status register | |
| 01A0 FFE4 | CIPR | Channel interrupt pending register | |
| 01A0 FFE8 | CIER | Channel interrupt enable register | |
| 01A0 FFEC | CCER | Channel chain enable register | |
| 01A0 FFF0 | ER | Event register | |
| 01A0 FFF4 | EER | Event enable register | |
| 01A0 FFF8 | ECR | Event clear register | |
| 01A0 FFFC | ESR | Event set register | |
| 01A1 0000 – 01A3 FFFF | - | Reserved | |

Table 9. Quick DMA (QDMA) and Pseudo Registers†

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|-----------------------|---------|--|
| 0200 0000 | QOPT | QDMA options parameter register |
| 0200 0004 | QSRC | QDMA source address register |
| 0200 0008 | QCNT | QDMA frame count register |
| 0200 000C | QDST | QDMA destination address register |
| 0200 0010 | QIDX | QDMA index register |
| 0200 0014 - 0200 001C | - | Reserved |
| 0200 0020 | QSOPT | QDMA pseudo options register |
| 0200 0024 | QSSRC | QDMA pseudo source address register |
| 0200 0028 | QSCNT | QDMA pseudo frame count register |
| 0200 002C | QSDST | QDMA pseudo destination address register |
| 0200 0030 | QSIDX | QDMA pseudo index register |

[†] All the QDMA and Pseudo registers are write-accessible only



SGUS055 - SEPTEMBER 2004

peripheral register descriptions (continued)

Table 10. PLL Controller Registers [C6712C/C6712D Only]

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME | |
|-----------------------|---------|--|--|
| 01B7 C000 | PLLPID | Peripheral identification register (PID) | [C6712D value: 0x00010801 for PLL Controller] [C6712C value: 0x00010801 for PLL Controller] |
| 01B7 C004 – 01B7 C0FF | - | Reserved | |
| 01B7 C100 | PLLCSR | PLL control/status register | |
| 01B7 C104 – 01B7 C10F | - | Reserved | |
| 01B7 C110 | PLLM | PLL multiplier control register | |
| 01B7 C114 | PLLDIV0 | PLL controller divider 0 register | |
| 01B7 C118 | PLLDIV1 | PLL controller divider 1 register | |
| 01B7 C11C | PLLDIV2 | PLL controller divider 2 register | |
| 01B7 C120 | PLLDIV3 | PLL controller divider 3 register | |
| 01B7 C124 | OSCDIV1 | Oscillator divider 1 register | |
| 01B7 C128 – 01B7 DFFF | - | Reserved | |

Table 11. GPIO Registers [C6712C/C6712D Only]

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|-----------------------|---------|----------------------------------|
| 01B0 0000 | GPEN | GPIO enable register |
| 01B0 0004 | GPDIR | GPIO direction register |
| 01B0 0008 | GPVAL | GPIO value register |
| 01B0 000C | _ | Reserved |
| 01B0 0010 | GPDH | GPIO delta high register |
| 01B0 0014 | GPHM | GPIO high mask register |
| 01B0 0018 | GPDL | GPIO delta low register |
| 01B0 001C | GPLM | GPIO low mask register |
| 01B0 0020 | GPGC | GPIO global control register |
| 01B0 0024 | GPPOL | GPIO interrupt polarity register |
| 01B0 0028 - 01B0 3FFF | _ | Reserved |

peripheral register descriptions (continued)

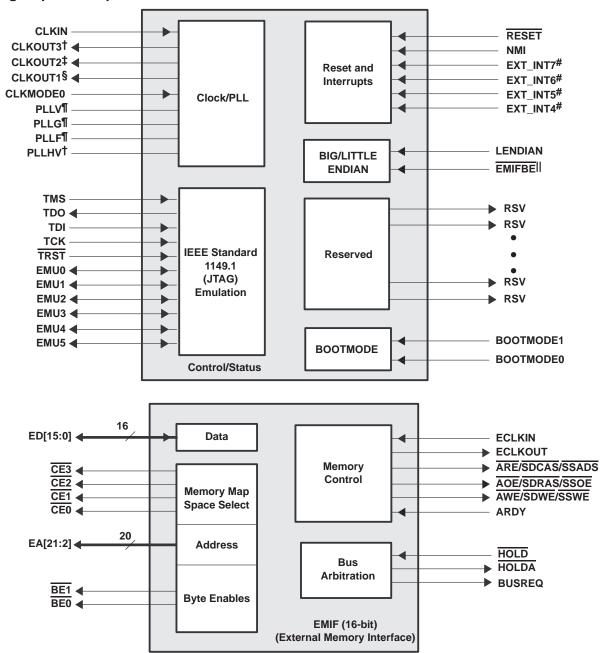
Table 12. Timer 0 and Timer 1 Registers

| HEX ADDRE | ESS RANGE | A CD ONIVA | REGISTER NAME | COMMENTS | | |
|-----------------------|-----------------------|------------|--------------------------|---|--|--|
| TIMER 0 | TIMER 1 | ACRONYM | REGISTER NAME | COMMENTS | | |
| 0194 0000 | 0198 0000 | CTLx | Timer x control register | Determines the operating mode of the timer, monitors the timer status, and controls the function of the TOUT pin. | | |
| 0194 0004 | 0198 0004 | PRDx | Timer x period register | Contains the number of timer input clock cycles to count. This number controls the TSTAT signal frequency. | | |
| 0194 0008 | 0198 0008 | CNTx | Timer x counter register | Contains the current value of the incrementing counter. | | |
| 0194 000C - 0197 FFFF | 0198 000C - 019B FFFF | - | Reserved | - | | |

Table 13. McBSP0 and McBSP1 Registers

| HEX ADDRE | ESS RANGE | ACDONIVA | DECISTED DESCRIPTION | |
|-----------------------|-----------------------|----------|---|--|
| McBSP0 | McBSP1 | ACRONYM | REGISTER DESCRIPTION | |
| 018C 0000 | 0190 0000 | DRRx | McBSPx data receive register via Configuration Bus | |
| | | | The CPU and EDMA controller can only read this register; they cannot write to it. | |
| 3000 0000 – 33FF FFFF | 3400 0000 – 37FF FFFF | DRRx | McBSPx data receive register via Peripheral Data Bus | |
| 018C 0004 | 0190 0004 | DXRx | McBSPx data transmit register via Configuration Bus | |
| 3000 0000 – 33FF FFFF | 3400 0000 – 37FF FFFF | DXRx | McBSPx data transmit register via Peripheral Data Bus | |
| 018C 0008 | 0190 0008 | SPCRx | McBSPx serial port control register | |
| 018C 000C | 0190 000C | RCRx | McBSPx receive control register | |
| 018C 0010 | 0190 0010 | XCRx | McBSPx transmit control register | |
| 018C 0014 | 0190 0014 | SRGRx | McBSPx sample rate generator register | |
| 018C 0018 | 0190 0018 | MCRx | McBSPx multichannel control register | |
| 018C 001C | 0190 001C | RCERx | McBSPx receive channel enable register | |
| 018C 0020 | 0190 0020 | XCERx | McBSPx transmit channel enable register | |
| 018C 0024 | 0190 0024 | PCRx | McBSPx pin control register | |
| 018C 0028 – 018F FFFF | 0190 0028 - 0193 FFFF | _ | Reserved | |

signal groups description



[†] The CLKOUT3 and PLLHV pin functions are applicable to the C6712C/12D device only.

Figure 3. CPU (DSP Core) and Peripheral Signals



[‡] For the C6712C/12D device, the CLKOUT2 pin is multiplexed with the GP[2] pin. Default function is CLKOUT2. To use this pin as GPIO, the GP2EN bit in the GPEN register and the GP2DIR bit in the GPDIR register must be properly configured.

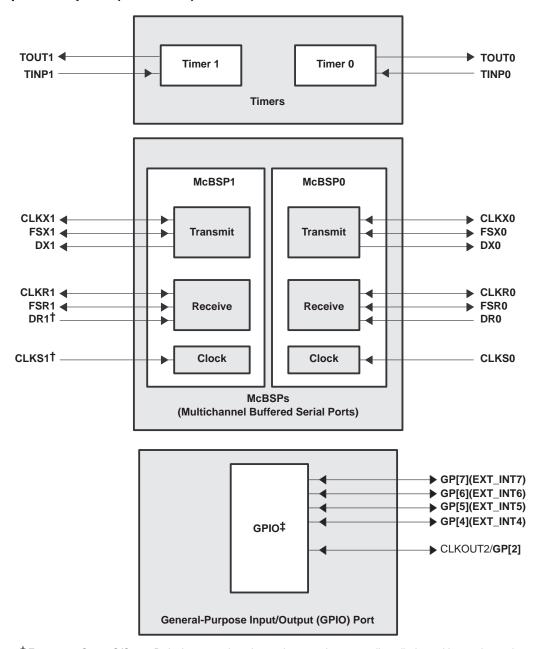
[§] The CLKOUT1 pin function is applicable to the C6712 device only.

These pins apply to the C6712 device only. The C6712C/12D device has a different PLL module and PLL Controller; therefore, the PLLV, PLLG, and PLLF pins are not necessary on the C6712C device.

[#]For the C6712C/12D device, the external interrupts (EXT_INT[7-4]) go through the general-purpose input/output (GPIO) module. When used as interrupt inputs, the GP[7-4] pins must be configured as inputs (via the GPDIR register) and enabled (via the GPEN register) in addition to enabling the interrupts in the interrupt enable register (IER).

This pin functions as the Big Endian mode correctness and is used when Big Endian mode is selected (LENDIAN = 0) [C6712D]

signal groups description (continued)



 $[\]dagger$ For proper C6712C/C6712D device operation, these pins must be externally pulled up with a 10-k Ω resistor.

Figure 4. Peripheral Signals

[‡] Only the C6712C/C6712D device supports the general-purpose input/output (GPIO) port peripheral.

DEVICE CONFIGURATIONS

On the C6712, C6712C, and C6712D devices, bootmode and certain device configurations/peripheral selections are determined at device reset. For the C6712C/C6712D devices only, other device configurations (e.g., EMIF input clock source) are software-configurable via the device configurations register (DEVCFG) [address location 0x019C0200] after device reset.

device configurations at device reset

Table 14 describes the C6712/12C/12D device configuration pins, which are set up via internal or external pullup/pulldown resistors through the LENDIAN, EMIFBE [12D only], BOOTMODE[1:0], and CLKMODE0 pins. These configuration pins must be in the desired state until reset is released. For more details on these device configuration pins, see the Terminal Functions table of this data sheet.

Table 14. Device Configurations Pins at Device Reset (LENDIAN, EMIFBE [12D only], BOOTMODE[1:0], and CLKMODE0)

| | · | |
|----------------------|-------------|--|
| CONFIGURATION PIN | GFN and GDP | FUNCTIONAL DESCRIPTION |
| EMIFBE | C15 | EMIF Big Endian mode correctness (EMIFBE) [C6712D only] C15 – "Reserved" pin for C6712/C6712C devices, the C6712/C6712C devices do <i>not</i> support Big Endian mode. When Big Endian mode is selected (LENDIAN = 0), for proper C6712D device operation the EMIFBE pin <i>must</i> be externally pulled low. This enhancement is <i>not</i> supported on the C6712/12C devices. For proper C6712/C6712C device operation, this pin is "Reserved and <i>must</i> be externally pulled high with a 10-kΩ resistor". This new functionality does <i>not</i> affect systems using the current default value of C15 pin=1. For more detailed information on the Big Endian mode correctness, see the <i>EMIF Big Endian Mode</i> |
| LENDIAN | B17 | Correctness [C6712D Only] portion of this data sheet. Device Endian mode (LEND) 0 — System operates in Big Endian mode. For the C6712D, the EMIFBE pin must be pulled low. For the C6712 and C6712C, Big Endian mode is not supported. 1 — System operates in Little Endian mode (default) |
| BOOTMODE[1:0] | C19, C20 | Bootmode Configuration Pins (BOOTMODE) 00 - Emulation boot 01 - CE1 width 8-bit, Asynchronous external ROM boot with default timings (default mode) 10 - CE1 width 16-bit, Asynchronous external ROM boot with default timings 11 - Reserved, do not use For more detailed information on these bootmode configurations, see the bootmode section of this data sheet. |
| CLKMODE0 | C4 | For the C6712 device, clock mode select 0 - Bypass mode (x1). CPU clock = CLKIN 1 - PLL mode (x4). CPU clock = 4 x CLKIN [default] For the C6712C/C6712D device, clock generator input clock source select 0 - Reserved. Do not use. 1 - CLKIN square wave [default] For proper C6712C/C6712D device operation, this pin must be either left unconnected or externally pulled up with a 1-kΩ resistor. |

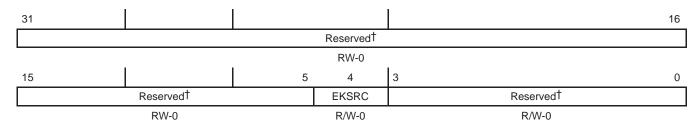


DEVICE CONFIGURATIONS (CONTINUED)

DEVCFG register description [C6712C/C6712D only]

The device configuration register (DEVCFG) allows the user control of the EMIF input clock source for the C6712C/C6712D device only. For more detailed information on the DEVCFG register control bits, see Table 15 and Table 16.

Table 15. Device Configuration Register (DEVCFG) [Address location: 0x019C0200 – 0x019C02FF]



Legend: R/W = Read/Write; -n = value after reset † **Do not** write non-zero values to these bit locations.

Table 16. Device Configuration (DEVCFG) Register Selection Bit Descriptions

| BIT# | NAME | DESCRIPTION | | | | |
|------|----------|---|--|--|--|--|
| 31:5 | Reserved | Reserved. <i>Do not</i> write non-zero values to these bit locations. | | | | |
| 4 | EKSRC | EMIF input clock source bit. Determines which clock signal is used as the EMIF input clock. 0 = SYSCLK3 (from the clock generator) is the EMIF input clock source (default) 1 = ECLKIN external pin is the EMIF input clock source | | | | |
| 3:0 | Reserved | Reserved. Do not write non-zero values to these bit locations. | | | | |

SGUS055 - SEPTEMBER 2004

TERMINAL FUNCTIONS

The terminal functions table identifies the external signal names, the associated pin (ball) numbers along with the mechanical package designator, the pin type (I, O/Z, or I/O/Z), whether the pin has any internal pullup/pulldown resistors and a functional pin description. For more detailed information on device configuration, see the Device Configurations section of this data sheet.

Terminal Functions

| SIGNAL | PIN NO. | | TYPET IPD/ | | | |
|----------|---------|-----|------------|------|--|--|
| NAME | GFN | GDP | TYPET | IPU‡ | DESCRIPTION | |
| | · I | | | | CLOCK/PLL | |
| CLKIN | А3 | А3 | I | IPU | Clock Input | |
| CLKOUT1 | D7 | _ | 0 | IPD | Clock output at device speed [C6712 only] The CLK1EN bit in the EMIF GBLCTL register controls the CLKOUT1 pin. CLK1EN = 0: CLKOUT1 is disabled CLK1EN = 1: CLKOUT1 enabled to clock [default] | |
| | | | | | Clock output at half of device speed [C6712 only] | |
| CLKOUT2 | Y12 | Y12 | O/Z | IPD | For the C6712C/12D device, the CLKOUT2 pin is multiplexed with the GP[2] pin. Clock output at half of device speed (O/Z) [default] (SYSCLK2 internal signal from the clock generator) or this pin can be programmed as GP[2] (I/O/Z). | |
| | | | | | When the CLKOUT2 pin is enabled, the CLK2EN bit in the EMIF global control register (GBLCTL) controls the CLKOUT2 pin (All devices). CLK2EN = 0: CLKOUT2 is disabled CLK2EN = 1: CLKOUT2 enabled to clock [default] | |
| CLKOUT3 | _ | D10 | 0 | IPD | Clock output programmable by OSCDIV1 register in the PLL controller. [12C/12D] | |
| | | | | | Clock mode select [C6712] 0 - Bypass mode (x1). CPU clock = CLKIN 1 - PLL mode (x4). CPU clock = 4 x CLKIN [default] | |
| CLKMODE0 | C4 | C4 | I | IPU | Clock generator input clock source select [C6712C/12D] 0 - Reserved. Do not use. 1 - CLKIN square wave [default] For proper C6712C/12D device operation, this pin must be either left unconnected or externally pulled up with a 1-kΩ resistor. | |
| PLLV§ | A4 | _ | Α¶ | | PLL analog V _{CC} connection for the low-pass filter [C6712 only] | |
| PLLG§ | C6 | _ | Α¶ | | PLL analog GND connection for the low-pass filter [C6712 only] | |
| PLLF | B5 | _ | Α¶ | | PLL low-pass filter connection to external components and a bypass capacitor [C6712 only] | |
| PLLHV | _ | C5 | Α¶ | | Analog power (3.3 V) for PLL [C6712C/C6712D only] | |
| | | | | | JTAG EMULATION | |
| TMS | B7 | B7 | I | IPU | JTAG test-port mode select | |
| TDO | A8 | A8 | O/Z | IPU | JTAG test-port data out | |
| TDI | A7 | A7 | I | IPU | JTAG test-port data in | |
| TCK | A6 | A6 | I | IPU | JTAG test-port clock | |
| TRST | В6 | В6 | I | IPD | JTAG test-port reset. For IEEE 1149.1 JTAG compatibility, see the IEEE 1149.1 JTAG Compatibility Statement section of this data sheet. | |
| EMU5 | B12 | B12 | I/O/Z | IPU | Emulation pin 5. Reserved for future use, leave unconnected. | |
| EMU4 | C11 | C11 | I/O/Z | IPU | Emulation pin 4. Reserved for future use, leave unconnected. | |
| EMU3 | B10 | B10 | I/O/Z | IPU | Emulation pin 3. Reserved for future use, leave unconnected. | |
| EMU2 | D10 | D3 | I/O/Z | IPU | Emulation pin 2. Reserved for future use, leave unconnected. | |

 $[\]dagger$ I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground



[‡] For **C6712**, IPD = Internal pulldown, IPU = Internal pullup. (These IPD/IPU signal pins feature a 30-k Ω IPD or IPU resistor. To pull up a signal to the opposite supply rail, a 1-k Ω resistor should be used.)

For C6712C/12D, IPD = Internal pulldown, IPU = Internal pullup. [These IPD/IPU signal pins feature a 13-k Ω resistor (approximate) for the IPD or 18-k Ω resistor (approximate) for the IPU. An external pullup or pulldown resistor no greater than 4.4 k Ω and 2.0 k Ω , respectively, should be used to pull a signal to the opposite supply rail.]

[§] PLLV and PLLG are not part of external voltage supply or ground. See the clock/PLL section for information on how to connect these pins.

[¶] A = Analog signal (PLL Filter)

SGUS055 - SEPTEMBER 2004

Terminal Functions (Continued)

| SIGNAL | PIN | NO. | | TYPET IPD/ DESCRIPTION | | |
|------------------------|------------|------------|-------|------------------------|---|--|
| NAME | GFN | GDP | TYPET | IPU/ IPU‡ | DESCRIPTION | |
| | | | | JTA | G EMULATION (CONTINUED) | |
| EMU1 EMU0 | B9 D9 | B9 D9 | I/O/Z | IPU | Emulation [1:0] pins [C6712]. For the C6712 device, the EMU0 and EMU1 pins are internally pulled up with 30-kΩ resistors. For Emulation and normal operation, no external pullup/pulldown resistors are necessary. However for the Boundary Scan operation, pull down the EMU1 and EMU0 pins with a dedicated 1-kΩ resistor. Emulation [1:0] pins [C6712C/C6712D]. • Select the device functional mode of operation EMU[1:0] Operation 00 Boundary Scan/Functional Mode (see Note) 01 Reserved 10 Reserved 11 Emulation/Functional Mode [default] (see the IEEE 1149.1 JTAG Compatibility Statement section of this data sheet) The DSP can be placed in Functional mode when the EMU[1:0] pins are configured for either Boundary Scan or Emulation. Note: When the EMU[1:0] pins are configured for Boundary Scan mode, the internal pulldown (IPD) on the TRST signal must not be opposed in order to operate in Functional mode. For the Boundary Scan mode drive EMU[1:0] and RESET pins low [C6712C/12D]. | |
| | | | 1 | | BOOTMODE | |
| BOOTMODE1 BOOTMODE0 | C19 C20 | C19 C20 | I | IPD | Bootmode[1:0] 00 - Emulation boot 01 - CE1 width 8-bit, asynchronous external ROM boot with default timings (default mode) 10 - CE1 width 16-bit, asynchronous external ROM boot with default timings 11 - Reserved, do not use | |
| | | | | LIT | TLE/BIG ENDIAN FORMAT | |
| LENDIAN | B17 | B17 | I | IPU | Device Endian mode 0 - System operates in Big Endian mode. For the C6712D, the EMIFBE pin <i>must</i> be pulled low. For the C6712 and C6712C, Big Endian mode is <i>not</i> supported 1 - System operates in Little Endian mode. | |
| EMIFBE | | C15 | - | IPU | EMIF Big Endian mode correctness (EMIFBE) [C6712D only] "Reserved" pin for C6712/C6712C devices When Big Endian mode is selected (LENDIAN = 0), for proper C6712D device operation the EMIFBE pin <i>must</i> be externally pulled low. This enhancement is <i>not</i> supported on the C6712/12C devices. For proper C6712/C6712C device operation, this pin is "Reserved and <i>must</i> be externally pulled low with a with a 10-kΩ resistor". For more detailed information on the Big Endian mode correctness, see the <i>EMIF Big Endian Mode Correctness</i> [C6712D Only] portion of this data sheet. | |

TI = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground

For **C6712C/12D**, IPD = Internal pulldown, IPU = Internal pullup. [These IPD/IPU signal pins feature a 13-k Ω resistor (approximate) for the IPD or 18-k Ω resistor (approximate) for the IPU. An external pullup or pulldown resistor no greater than 4.4 k Ω and 2.0 k Ω , respectively, should be used to pull a signal to the opposite supply rail.]



[‡] For C6712, IPD = Internal pulldown, IPU = Internal pullup. (These IPD/IPU signal pins feature a 30-k Ω IPD or IPU resistor. To pull up a signal to the opposite supply rail, a 1-k Ω resistor should be used.)

| SIGNAL | PIN | NO. | | IDD/ | T , | | | |
|---|----------|---------|----------|--------------------------|---|--|--|--|
| NAME | GFN | GDP | TYPET | IPD/ IPU‡ | DESCRIPTION | | | |
| | 1 | | | R | ESETS AND INTERRUPTS | | | |
| RESET | A13 | A13 | I | IPU | Device reset. When using Boundary Scan mode on the C6712C/C6712D device, drive the EMU[1:0] and RESET pins low. For the C6712D device, this pin does not have an IPU. | | | |
| NMI | C13 | C13 | I | IPD | Nonmaskable interrupt • Edge-driven (rising edge) Any noise on the NMI pin may trigger an NMI interrupt; therefore, if the NMI pin is not used, it is recommended that the NMI pin be grounded versus relying on the IPD. | | | |
| EXT_INT7 | E3 | E3 | | | External interrupts [C6712] • Edge-driven | | | |
| EXT_INT6 | D2 | D2 | | | Polarity independently selected via the External Interrupt Polarity Register bits (EXTPOL.[3:0]) | | | |
| EXT_INT5 | C1 | C1 | ' | IPU | General-purpose input/output pins (I/O/Z) which also function as external interrupts (default) [C6712C/C6712D only] | | | |
| EXT_INT4 | C2 | C2 | | • P | Edge-driven Polarity independently selected via the External Interrupt Polarity Register bits (EXTPOL.[3:0]), in addition to the GPIO registers. | | | |
| EMIF - CONTROL SIGNALS COMMON TO ALL TYPES OF MEMORY# | | | | | | | | |
| CE3 | V6 | V6 | O/Z | IPU | | | | |
| CE2 | W6 | W6 | O/Z | IPU Memory space enables | | | | |
| CE1 | W18 | W18 | O/Z | IPU | Enabled by bits 28 through 31 of the word address Only one asserted during any external data access | | | |
| CE0 | V17 | V17 | O/Z | IPU | a y a a a a a a a a a a a a a a a a a a | | | |
| BE1 | U19 | U19 | O/Z | IPU | Byte-enable control Decoded from the two lowest bits of the internal address | | | |
| BE0 | V20 | V20 | O/Z | IPU | Byte-write enables for most types of memory Can be directly connected to SDRAM read and write mask signal (SDQM) | | | |
| | | | | E | MIF – BUS ARBITRATION ^{#W} | | | |
| HOLDA | J18 | J18 | 0 | IPU | Hold-request-acknowledge to the host | | | |
| HOLD | J17 | J17 | I | IPU | Hold request from the host | | | |
| BUSREQ | J19 | J19 | 0 | IPU | Bus request output | | | |
| | MIF - AS | YNCHRON | IOUS/SYN | ICHRONO | DUS DRAM/SYNCHRONOUS BURST SRAM MEMORY CONTROL# | | | |
| ECLKIN | Y11 | Y11 | I | IPD | EMIF input clock | | | |
| ECLKOUT | Y10 | Y10 | 0 | IPD | EMIF output clock (based on ECLKIN) [C6712] EMIF output clock depends on the EKSRC bit (DEVCFG.[4]) and on EKEN bit (GBLCTL.[5]). [C6712C/C6712D only] EKSRC = 0 — ECLKOUT is based on the internal SYSCLK3 signal from the clock generator (default). EKSRC = 1 — ECLKOUT is based on the the external EMIF input clock source pin (ECLKIN) | | | |
| | | | | | EKEN = 0 - ECLKOUT held low EKEN = 1 - ECLKOUT enabled to clock (default) | | | |

[†] I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground

[#] To maintain signal integrity for the EMIF signals, serial termination resistors should be inserted into all EMIF output signal lines.



[‡] For **C6712**, IPD = Internal pulldown, IPU = Internal pullup. (These IPD/IPU signal pins feature a 30-k Ω IPD or IPU resistor. To pull up a signal to the opposite supply rail, a 1-k Ω resistor should be used.)

For **C6712C/12D**, IPD = Internal pulldown, IPU = Internal pullup. [These IPD/IPU signal pins feature a 13-k Ω resistor (approximate) for the IPD or 18-k Ω resistor (approximate) for the IPU. An external pullup or pulldown resistor no greater than 4.4 k Ω and 2.0 k Ω , respectively, should be used to pull a signal to the opposite supply rail.]

SGUS055 - SEPTEMBER 2004

| SIGNAL | PIN | NO. | | IPD/ | , , , , , , , , , , , , , , , , , , , |
|---------------------|--------|---------|----------|---------|--|
| NAME | GFN | GDP | TYPET | IPU‡ | DESCRIPTION |
| EMIF – A | SYNCHR | ONOUS/S | YNCHROI | NOUS DR | AM/SYNCHRONOUS BURST SRAM MEMORY CONTROL (CONTINUED)# |
| ARE/SDCAS/ SSADS | V11 | V11 | O/Z | IPU | Asynchronous memory read enable/SDRAM column-address strobe/SBSRAM address strobe |
| AOE/SDRAS/ SSOE | W10 | W10 | O/Z | IPU | Asynchronous memory output enable/SDRAM row-address strobe/SBSRAM output enable |
| AWE/SDWE/ SSWE | V12 | V12 | O/Z | IPU | Asynchronous memory write enable/SDRAM write enable/SBSRAM write enable |
| ARDY | Y5 | Y5 | I | IPU | Asynchronous memory ready input |
| | | | | | EMIF - ADDRESS# |
| EA21 | U18 | U18 | | | |
| EA20 | Y18 | Y18 |] | | |
| EA19 | W17 | W17 |] | | |
| EA18 | Y16 | Y16 | 1 | | |
| EA17 | V16 | V16 |] | | |
| EA16 | Y15 | Y15 |] | | |
| EA15 | W15 | W15 |] | | |
| EA14 | Y14 | Y14 |] | IPU | |
| EA13 | W14 | W14 | 1 | | EMIF external address Note: EMIF address numbering for the C6712, C6712C, and C6712D devices state with EA2 to maintain signal name compatibility with other C671x devices (e.g., |
| EA12 | V14 | V14 |] | | |
| EA11 | W13 | W13 | O/Z | | C6711, C6713) [see the 16-bit EMIF addressing scheme in the TMS320C6000 DSP |
| EA10 | V10 | V10 | 1 | | External Memory Interface (EMIF) Reference Guide (literature number SPRU26 |
| EA9 | Y9 | Y9 | 1 | | |
| EA8 | V9 | V9 | 1 | | |
| EA7 | Y8 | Y8 | 1 | | |
| EA6 | W8 | W8 | 1 | | |
| EA5 | V8 | V8 | 1 | | |
| EA4 | W7 | W7 | 1 | | |
| EA3 | V7 | V7 | 1 | | |
| EA2 | Y6 | Y6 | 1 | | |
| | | | | | EMIF – DATA# |
| ED15 | T19 | T19 | | | |
| ED14 | T20 | T20 |] | | |
| ED13 | T18 | T18 |] | | |
| ED12 | R20 | R20 | 1/6/7 | 15 | Establish data |
| ED11 | R19 | R19 | I/O/Z | IPU | External data |
| ED10 | P20 | P20 | 1 | | |
| ED9 | P18 | P18 |] | | |
| ED8 | N20 | N20 | <u> </u> | | |

[†] I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground

[#] To maintain signal integrity for the EMIF signals, serial termination resistors should be inserted into all EMIF output signal lines.



[‡] For C6712, IPD = Internal pulldown, IPU = Internal pullup. (These IPD/IPU signal pins feature a 30-k Ω IPD or IPU resistor. To pull up a signal to the opposite supply rail, a 1-k Ω resistor should be used.)

For C6712C/12D, IPD = Internal pulldown, IPU = Internal pullup. [These IPD/IPU signal pins feature a 13-k Ω resistor (approximate) for the IPD or 18-k Ω resistor (approximate) for the IPU. An external pullup or pulldown resistor no greater than 4.4 k Ω and 2.0 k Ω , respectively, should be used to pull a signal to the opposite supply rail.]

SGUS055 - SEPTEMBER 2004

| SIGNAL | PIN | NO. | | IPD/ | | | | | |
|--------|-----|-----|----------|---------|---|--|--|--|--|
| NAME | GFN | GDP | TYPET | IPU‡ | DESCRIPTION | | | | |
| | | | | EMIF - | - DATA (CONTINUED)# | | | | |
| ED7 | N19 | N19 | | | | | | | |
| ED6 | N18 | N18 | | | | | | | |
| ED5 | M20 | M20 | | | | | | | |
| ED4 | M19 | M19 | | | | | | | |
| ED3 | L19 | L19 | I/O/Z | IPU | External data | | | | |
| ED2 | L18 | L18 | 1 | | | | | | |
| ED1 | K19 | K19 | 1 | | | | | | |
| ED0 | K18 | K18 | 1 | | | | | | |
| TIMER1 | | | | | | | | | |
| TOUT1 | F1 | F1 | 0 | IPD | Timer 1 or general-purpose output | | | | |
| TINP1 | F2 | F2 | I | IPD | Timer 1 or general-purpose input | | | | |
| | | | | | TIMER0 | | | | |
| TOUT0 | G1 | G1 | 0 | IPD | Timer 0 or general-purpose output | | | | |
| TINP0 | G2 | G2 | I | IPD | Timer 0 or general-purpose input | | | | |
| | | ı | MULTICHA | NNEL BU | JFFERED SERIAL PORT 1 (McBSP1) | | | | |
| CLKS1 | E1 | E1 | ı | IPD | External clock source (as opposed to internal) On the C6712C/12D device, this pin does not have an internal pulldown (IPD). For proper C6712C/12D device operation, the CLKS1 pin should either be driven externally at all times or be pulled up with a 10 -k Ω resistor to a valid logic level. Because it is common for some ICs to 3-state their outputs at times, a 10 -k Ω pullup resistor may be desirable even when an external device is driving the pin. | | | | |
| CLKR1 | M1 | M1 | I/O/Z | IPD | Receive clock | | | | |
| CLKX1 | L3 | L3 | I/O/Z | IPD | Transmit clock | | | | |
| DR1 | M2 | M2 | I | IPU | Receive data On the C6712C/12D device, this pin does not have an internal pullup (IPU). For proper C6712C/12D device operation, the DR1 pin should either be driven externally at all times or be pulled up with a 10-k Ω resistor to a valid logic level. Because it is common for some ICs to 3-state their outputs at times, a 10-k Ω pullup resistor may be desirable even when an external device is driving the pin. | | | | |
| DX1 | L2 | L2 | O/Z | IPU | Transmit data | | | | |
| FSR1 | МЗ | МЗ | I/O/Z | IPD | Receive frame sync | | | | |
| FSX1 | L1 | L1 | I/O/Z | IPD | Transmit frame sync | | | | |

t I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground

[‡] For C6712, IPD = Internal pulldown, IPU = Internal pullup. (These IPD/IPU signal pins feature a 30-k Ω IPD or IPU resistor. To pull up a signal to the opposite supply rail, a 1-k Ω resistor should be used.)

For **C6712C/12D**, IPD = Internal pulldown, IPU = Internal pullup. [These IPD/IPU signal pins feature a 13-k Ω resistor (approximate) for the IPD or 18-k Ω resistor (approximate) for the IPU. An external pullup or pulldown resistor no greater than 4.4 k Ω and 2.0 k Ω , respectively, should be used to pull a signal to the opposite supply rail.]

[#] To maintain signal integrity for the EMIF signals, serial termination resistors should be inserted into all EMIF output signal lines.

SGUS055 - SEPTEMBER 2004

Terminal Functions (Continued)

| SIGNAL | PIN | NO. | | IPD/ | | |
|-----------------|-----|---------|-----------|-----------|---|---|
| NAME | GFN | GDP | TYPET | IPU‡ | DESCRIPTION | |
| | | N | //ULTICHA | NNEL BU | JFFERED SERIAL PORT 0 (McBSP0) | |
| CLKS0 | K3 | K3 | I | IPD | External clock source (as opposed to internal) | |
| CLKR0 | Н3 | НЗ | I/O/Z | IPD | Receive clock | |
| CLKX0 | G3 | G3 | I/O/Z | IPD | Transmit clock | |
| DR0 | J1 | J1 | I | IPU | Receive data | |
| DX0 | H2 | H2 | O/Z | IPU | Transmit data | |
| FSR0 | J3 | J3 | I/O/Z | IPD | Receive frame sync | |
| FSX0 | H1 | H1 | I/O/Z | IPD | Transmit frame sync | |
| | C | SENERAL | -PURPOS | E INPUT/ | DUTPUT (GPIO) MODULE [C6712C/12D ONLY] | |
| CLKOUT2/GP[2] | Y12 | Y12 | I/O/Z | IPD | Clock output at half of device speed [C6712/12D only] For the C6712C/12D device, the CLKOUT2 pin is multiplexed with the GP[2] pin. Clock output at half of device speed (O/Z) [default] (SYSCLK2 internal signal from the clock generator) or this pin can be programmed as GP[2] (I/O/Z). | |
| GP[7](EXT_INT7) | _ | E3 | | | External interrupts [C6712C/12D only] Edge-driven Polarity independently selected via the External Interrupt Polarity Register | |
| GP[6](EXT_INT6) | _ | D2 | 1/0/7 | I/O/Z IPU | bits (EXTPOL.[3:0]) | |
| GP[5](EXT_INT5) | _ | C1 | 1/0/2 | | interrupts [C6712C/12D only] | General-purpose input/output pins (I/O/Z) which also function as external interrupts [C6712C/12D only] • Edge-driven |
| GP[4](EXT_INT4) | _ | C2 | | | Polarity independently selected via the External Interrupt Polarity Register bits (EXTPOL.[3:0]), in addition to the GPIO registers. | |
| | | | | RES | SERVED FOR TEST | |
| RSV | C15 | C15 | | IPU | Reserved (leave unconnected, <i>do not</i> connect to power or ground) [C6712] Reserved. For the C6712C device, it is recommended that this pin be externally pulled <i>low</i> with a 10-kΩ resistor. EMIF Big Endian mode correctness (EMIFBE) [C6712D only]. When Big Endian | |
| | | | | | mode is selected, for proper C6712D device operation, this pin must be externally pulled low. (For more detailed information on Big Endian mode correctness, see the <i>Device Configuration</i> section of this data sheet.) | |
| RSV | C12 | C12 | 0 | IPU | Reserved (leave unconnected, <i>do not</i> connect to power or ground). Only the C6712 device has internal pullup (IPU) on this pin. On the C6712C/12D device, this pin does <i>not</i> have an IPU. | |
| RSV | D12 | D12 | 0 | IPU | Only the C6712 device has internal pullups (IPUs). For the C6712, the D12 pin is reserved (leave unconnected, <i>do not</i> connect to power or ground). On the C6712C/12D device, this pin does <i>not</i> have an IPU. For proper C6712C/12D device operation, the D12 pin <i>must</i> be externally pulled down with a 10-k Ω resistor. | |

TI = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground

For **C6712C**, IPD = Internal pulldown, IPU = Internal pullup. [These IPD/IPU signal pins feature a 13-k Ω resistor (approximate) for the IPD or 18-k Ω resistor (approximate) for the IPU. An external pullup or pulldown resistor no greater than 4.4 k Ω and 2.0 k Ω , respectively, should be used to pull a signal to the opposite supply rail.]



[‡] For **C6712**, IPD = Internal pulldown, IPU = Internal pullup. (These IPD/IPU signal pins feature a 30-k Ω IPD or IPU resistor. To pull up a signal to the opposite supply rail, a 1-k Ω resistor should be used.)

| SIGNAL | PIN | NO. | | IPD/ | |
|--------|-----|-----|-------|----------|---|
| NAME | GFN | GDP | TYPET | IPU | DESCRIPTION |
| RSV | A5 | A5 | 0 | IPU | Reserved (leave unconnected, do not connect to power or ground) |
| RSV | D3 | _ | 0 | | Reserved (leave unconnected, do not connect to power or ground) |
| | | | | | Reserved (leave unconnected, do not connect to power or ground) [C6712 |
| RSV | N2 | N2 | 0 | | Reserved. For proper C6712C/12D device operation, this pin must be |
| | | | | | externally pulled up with a 10-k Ω resistor. |
| RSV | Y20 | _ | 0 | | Reserved (leave unconnected, do not connect to power or ground) |
| RSV | _ | N1 | | | Reserved. For proper C6712C/12D device operation, this pin must be externally pulled up with a 10-k Ω resistor. |
| RSV | _ | B5 | | | Reserved (leave unconnected, do not connect to power or ground) |
| RSV | _ | D7 | | IPD | Reserved (leave unconnected, do not connect to power or ground) |
| RSV | _ | A12 | | | Reserved (leave unconnected, do not connect to power or ground) |
| RSV | | B11 | | | Reserved (leave unconnected, do not connect to power or ground) |
| | | | | ADDITION | IAL RESERVED FOR TEST |
| | A15 | A15 | | | |
| | A16 | A16 |] | | |
| | A18 | A18 | | | |
| | B14 | B14 | | | |
| | B16 | B16 | | | |
| | B18 | B18 | | | |
| | C14 | C14 | | | |
| | C16 | C16 | | | |
| | C17 | C17 | | | |
| | D18 | D18 | | | |
| | D20 | D20 | | | |
| | E18 | E18 | | | |
| RSV | E19 | E19 |] | | Percented (legge unconnected do not connect to negler or arrand) |
| NOV | E20 | E20 |] | | Reserved (leave unconnected, <i>do not</i> connect to power or ground) |
| | F18 | F18 |] | | |
| | F20 | F20 |] | | |
| | G18 | G18 |] | | |
| | G19 | G19 |] | | |
| | G20 | G20 |] | | |
| | H19 | H19 |] | | |
| | H20 | H20 |] | | |
| | J20 | J20 |] | | |
| | N3 | N3 |] | | |
| | P1 | P1 |] | | |
| | P2 | P2 |] | | |
| | P3 | P3 |] | | |

[†] I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground

SGUS055 - SEPTEMBER 2004

| SIGNAL | PIN NO. | | TYPET | IPD/ | DESCRIPTION | | | |
|------------------------------|---------|-----|-------|------|--|--|--|--|
| NAME | GFN | GDP | TYPET | IPU | DESCRIPTION | | | |
| ADDITIONAL RESERVED FOR TEST | | | | | | | | |
| | R2 | R2 | | | | | | |
| | R3 | R3 | | | | | | |
| | T1 | T1 | | | | | | |
| | T2 | T2 | | | | | | |
| | U1 | U1 | | | | | | |
| | U2 | U2 | | | | | | |
| 501/ | U3 | U3 | | | Bearing (for a second of the s | | | |
| RSV | V1 | V1 | | | Reserved (leave unconnected, <i>do not</i> connect to power or ground) | | | |
| | V2 | V2 | | | | | | |
| | V4 | V4 | | | | | | |
| | V5 | V5 | | | | | | |
| | W4 | W4 | | | | | | |
| | Y3 | Y3 | | | | | | |
| | Y4 | Y4 | | ı | | | | |

[†] I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground

| SIGNAL | PIN NO. | | | Terminari unctions (Continueu) | | | | |
|---------------------|-----------|-----------|-------|---|--|--|--|--|
| NAME | GFN | GDP | TYPET | DESCRIPTION | | | | |
| SUPPLY VOLTAGE PINS | | | | | | | | |
| | A17 | A17 | - | | | | | |
| | В3 | В3 | | | | | | |
| | B8 | B8 | | | | | | |
| | B13 | B13 | | | | | | |
| | C5 | _ | | | | | | |
| | C10 | C10 | | | | | | |
| | D1 | D1 | | | | | | |
| | D16 | D16 | | | | | | |
| | D19 | D19 | | | | | | |
| | F3 | F3 | | | | | | |
| | H18 | H18 | | | | | | |
| $^{	extsf{DV}}$ | J2 | J2 | _ | | | | | |
| | M18 | M18 | 4 | | | | | |
| | N1 | | | 3.3-V supply voltage (see the power-supply decoupling portion of this data sheet) | | | | |
| | R1 | R1 | S | | | | | |
| | R18 | R18 | _ | | | | | |
| | T3 | T3 | - | | | | | |
| | U5 | U5 | | | | | | |
| | U7 | U7 | | | | | | |
| | U12 | U12 | | | | | | |
| | U16 | U16 | | | | | | |
| | V13 | V13 | | | | | | |
| | V15 | V15 | | | | | | |
| | V19 | V19 | - | | | | | |
| | W3 | W3 | _ | | | | | |
| | W9 | W9 | | | | | | |
| | W12 Y7 | W12 Y7 | | | | | | |
| | Y17 | Y17 | | | | | | |
| | — — | A4 | | | | | | |
| | A9 | A9 | - | | | | | |
| | A10 | A10 | S | 4 oct V | | | | |
| | A12 | _ | | | | | | |
| | B2 | B2 | | | | | | |
| C∨ _{DD} | B19 | B19 | | 1.20 [‡] -V supply voltage (C6712C/C6712D) 1.8-V supply voltage (C6712) | | | | |
| טטיי ן | C3 | C3 | | (see the power-supply decoupling portion of this data sheet) | | | | |
| | C7 | C7 | | | | | | |
| | C18 | C18 | | | | | | |
| | D5 | D5 | | | | | | |
| | D6 | D6 | | | | | | |

[†] I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground

[‡]This value is compatible with existing 1.26V designs.



SGUS055 - SEPTEMBER 2004

| SIGNAL | PIN | NO. | l . | DESCRIPTION | | | | |
|------------------|---------------------------------|-----|-------|---|--|--|--|--|
| NAME | GFN | GDP | TYPET | | | | | |
| | SUPPLY VOLTAGE PINS (CONTINUED) | | | | | | | |
| | D11 | D11 | | | | | | |
| | D14 | D14 | | | | | | |
| | D15 | D15 | | | | | | |
| | F4 | F4 | | | | | | |
| | F17 | F17 | | | | | | |
| | K1 | K1 | | | | | | |
| | K4 | K4 | | | | | | |
| | K17 | K17 | | | | | | |
| | L4 | L4 | | | | | | |
| | L17 | L17 |] | | | | | |
| CVan | L20 | L20 | | 1.20 [‡] -V supply voltage (C6712C/C6712D) | | | | |
| CV _{DD} | R4 | R4 | S | 1.8-V supply voltage (C6712) (see the power-supply decoupling portion of this data sheet) | | | | |
| | R17 | R17 | | | | | | |
| | U6 | U6 | | | | | | |
| | U10 | U10 | | | | | | |
| | U11 | U11 | | | | | | |
| | U14 | U14 | | | | | | |
| | U15 | U15 | | | | | | |
| | V3 | V3 | | | | | | |
| | V18 | V18 | | | | | | |
| | W2 | W2 | | | | | | |
| | W19 | W19 | | | | | | |
| | | | | GROUND PINS | | | | |
| | A1 | A1 | | | | | | |
| | A2 | A2 | | | | | | |
| | A11 | A11 | | | | | | |
| | A14 | A14 | | | | | | |
| | A19 | A19 | | | | | | |
| | A20 | A20 | | | | | | |
| | B1 | B1 | | | | | | |
| | B4 | B4 | | | | | | |
| Vss | B11 | _ | GND | Ground pins | | | | |
| | B15 | B15 | | | | | | |
| | B20 | B20 | | | | | | |
| | | C6 | | | | | | |
| | C8 | C8 | | | | | | |
| | C9 | C9 | | | | | | |
| | D4 | D4 | | | | | | |
| | D8 | D8 | | | | | | |
| | D13 | D13 | | | | | | |

[†] I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground

[‡] This value is compatible with existing 1.26V designs.



| SIGNAL | PIN NO. | | | Terminal Functions (Continued) | | | | | | |
|-----------------|-------------------------|----------|--|---|--|--|--|--|--|--|
| NAME | GFN | GDP | TYPET | DESCRIPTION | | | | | | |
| | GROUND PINS (CONTINUED) | | | | | | | | | |
| | D17 | D17 | | | | | | | | |
| | E2 | E2 | | | | | | | | |
| | E4 | E4 | | | | | | | | |
| | E17 | E17 | | | | | | | | |
| | F19 | F19 | | | | | | | | |
| | G4 | G4 | | | | | | | | |
| | G17 | G17 | | | | | | | | |
| | H4 | H4 | | | | | | | | |
| | H17 | H17 | | | | | | | | |
| | J4 | J4 | | | | | | | | |
| | | J9 | | | | | | | | |
| | | J10 | | | | | | | | |
| | | J11 | | | | | | | | |
| | | J12 | | | | | | | | |
| | K2 — | K2 K9 | | | | | | | | |
| | | K10 | | | | | | | | |
| | _ | K10 | | | | | | | | |
| | | K12 | | | | | | | | |
| | K20 | K20 | GND | Ground pins | | | | | | |
| V _{SS} | _ | L9 | | The center thermal balls (J9–J12, K9–K12, L9–L12, M9–M12) [shaded] are all tied to ground | | | | | | |
| | | L10 | | and act as both electrical grounds and thermal relief (thermal dissipation). | | | | | | |
| | | L11 | | | | | | | | |
| | _ | L12 | | | | | | | | |
| | M4 | M4 | | | | | | | | |
| | _ | M9 | | | | | | | | |
| | _ | M10 | | | | | | | | |
| | _ | M11 | | | | | | | | |
| | _ | M12 | | | | | | | | |
| | M17 | M17 | | | | | | | | |
| | N4 | N4 | | | | | | | | |
| | N17 | N17 | 74 17 19 74 17 14 18 | | | | | | | |
| | P4 | P4 | | | | | | | | |
| | P17 | P17 | | | | | | | | |
| | P19 | P19 | | | | | | | | |
| | T4 | T4 | | | | | | | | |
| | T17 | T17 | | | | | | | | |
| | U4 | U4 | | | | | | | | |
| | U8 | U8 | | | | | | | | |
| | U9 | U9 | | | | | | | | |

[†] I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground

Shaded pin numbers denote the center thermal balls for the GDP package [C6712C/12D only].



SGUS055 - SEPTEMBER 2004

| SIGNAL | PIN | PIN NO. | | DECORIDATION | | | | |
|-----------------|-------------------------|---------|-------|--------------|--|--|--|--|
| NAME | GFN | GDP | TYPET | DESCRIPTION | | | | |
| | GROUND PINS (CONTINUED) | | | | | | | |
| | U13 | U13 |] | Ground pins | | | | |
| | U17 | U17 | | | | | | |
| | U20 | U20 | | | | | | |
| | W1 | W1 | GND | | | | | |
| | W5 | W5 | | | | | | |
| | W11 | W11 | | | | | | |
| V _{SS} | W16 | W16 | | | | | | |
| | W20 | W20 | | | | | | |
| | Y1 | Y1 | | | | | | |
| | Y2 | Y2 | | | | | | |
| | Y13 | Y13 | | | | | | |
| | Y19 | Y19 | | | | | | |
| | _ | Y20 | | | | | | |

[†] I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground

SGUS055 - SEPTEMBER 2004

development support

TI offers an extensive line of development tools for the TMS320C6000™ DSP platform, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules.

The following products support development of C6000™ DSP-based applications:

Software Development Tools:

Code Composer Studio[™] Integrated Development Environment (IDE): including Editor C/C++/Assembly Code Generation, and Debug plus additional development tools Scalable, Real-Time Foundation Software (DSP/BIOS[™]), which provides the basic run-time target software needed to support any DSP application.

Hardware Development Tools:

Extended Development System (XDS™) Emulator (supports C6000™ DSP multiprocessor system debug) EVM (Evaluation Module)

For a complete listing of development-support tools for the TMS320C6000™ DSP platform, visit the Texas Instruments web site on the Worldwide Web at http://www.ti.com uniform resource locator (URL). For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

Code Composer Studio, DSP/BIOS, and XDS are trademarks of Texas Instruments.



SGUS055 - SEPTEMBER 2004

device and development-support tool nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all TMS320™ DSP devices and support tools. Each TMS320™ DSP commercial family member has one of three prefixes: SMX, TMP, or SM. Texas Instruments recommends two of three possible prefix designators for support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (SMX/TMDX) through fully qualified production devices/tools (SM/TMDS).

Device development evolutionary flow:

SMX Preproduction device that is not necessarily representative of the final device's electrical

specifications

TMP Final silicon die that conforms to the device's electrical specifications but has not completed

quality and reliability verification

SM Fully qualified production device

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification

testing.

TMDS Fully qualified development-support product

SMX and TMP devices and TMDX development-support tools are shipped with appropriate disclaimers describing their limitations and intended uses. Preproduction devices (SMX) may not be representative of a final product and Texas Instruments reserves the right to change or discontinue these products without notice.

SM devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. Tl's standard warranty applies.

Predictions show that preproduction devices (SMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

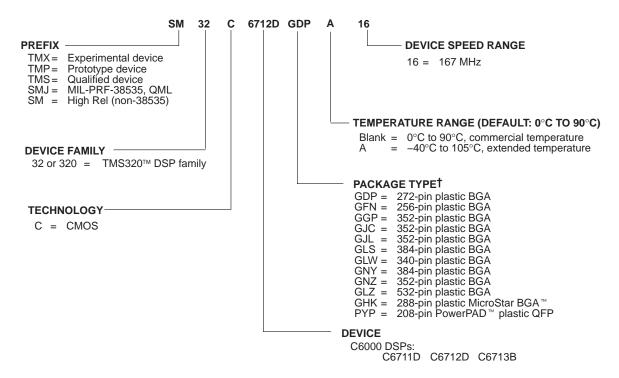
TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, GDP), the temperature range (for example, blank is the default commercial temperature range and A is the extended temperature range), and the device speed range in megahertz (for example, 16 is 167 MHz).

Table 17 identifies the C6712/12C/12D device part numbers (orderables). For more details and for ordering information, see the TI website (www.ti.com). Figure 5 provides a legend for reading the complete device name for any member of the TMS320C6000™ DSP platform.

device and development-support tool nomenclature (continued)

Table 17. 320C6712/C6712C/C6712D Device Part Numbers (P/Ns) and Ordering Information

| DEVICE ORDERABLE P/N | DEVICE SPEED | CV _{DD} (CORE VOLTAGE) | DV _{DD} (I/O VOLTAGE) | OPERATING CASE TEMPERATURE RANGE |
|----------------------|---------------------|------------------------------------|-----------------------------------|--|
| C6712D | | | | |
| SM32C6712DGDPA16EP | 167 MHz/1000 MFLOPS | 1.20 [†] V | 3.3 V | –40°C to 105°C |



†BGA = Ball Grid Array QFP = Quad Flatpack

Figure 5. TMS320C6000™ DSP Platform Device Nomenclature (Including the SM320C6712, SM320C6712C, and SM320C6712D Devices)

MicroStar BGA and PowerPAD are trademarks of Texas Instruments. † This value is compatible with existing 1.26V designs.



SGUS055 - SEPTEMBER 2004

documentation support

Extensive documentation supports all TMS320TM DSP family generations of devices from product announcement through applications development. The types of documentation available include: data sheets, such as this document, with design specifications; complete user's reference guides for all devices and tools; technical briefs; development-support tools; on-line help; and hardware and software applications. The following is a brief, descriptive list of support documentation specific to the C6000TM DSP devices:

The *TMS320C6000 CPU and Instruction Set Reference Guide* (literature number SPRU189) describes the C6000™ DSP core (CPU) architecture, instruction set, pipeline, and associated interrupts.

The *TMS320C6000 DSP Peripherals Overview Reference Guide* [hereafter referred to as the C6000 PRG Overview] (literature number SPRU190) provides an overview and briefly describes the functionality of the peripherals available on the C6000[™] DSP platform of devices. This document also includes a table listing the peripherals available on the C6000 devices along with literature numbers and hyperlinks to the associated peripheral documents. These C6712C/C6712D peripherals, except the PLL, are similar to the peripherals on the TMS320C6712 and TMS320C64x devices; therefore, see the TMS320C6712 (C6711 or C67x) peripheral information, and in some cases, where indicated, see the TMS320C6712 or TMS320C67x[™] or C671x or C67x) peripheral information, and in some cases, where indicated, see the C64x information in the TMS320C6000 DSP Peripherals Overview Reference Guide (literature number SPRU190).

The *TMS320C6000 Technical Brief* (literature number SPRU197) gives an introduction to the C62x[™]/C67x[™] DSP devices, associated development tools, and third-party support.

TMS320C6000 DSP Software-Programmable Phase-Locked Loop (PLL) Controller Reference Guide (literature number SPRU233) describes the functionality of the PLL peripheral available on the C6712C/12D device.

The *Migrating from TMS320C6211(B)/6711(B)* to *TMS320C6711C* application report (literature number SPRA837) describes the differences and issues of interest related to migration from the Texas Instruments TMS320C6211, TMS320C6211B, TMS320C6711, and TMS320C6711B devices, GFN packages, to the TMS320C6711C device, GDP package.

The *Migrating from TMS320C6712 to TMS320C6712C* application report (literature number SPRA852) describes the differences and issues of interest related to migration from the Texas Instruments TMS320C6712 device, GFN package, to the TMS320C6712C device, GDP package.

The TMS320C6712, TMS320C6712C, TMS320C6712D Digital Signal Processors Silicon Errata (C6712 Silicon Revisions 1.0, 1.2, 1.3, C6712C Silicon Revision 1.1, and C6712D Silicon Revision 2.0) [literature number SPRZ182C or later] categorizes and describes the known exceptions to the functional specifications and usage notes for the TMS320C6712, TMS320C6712C, TMS320C6712D DSP devices.

The *TMS320C6713/12C/11C Power Consumption Summary* application report (literature number SPRA889) discusses the power consumption for user applications with the TMS320C6713, TMS320C6712C, and TMS320C6711C DSP devices.

The tools support documentation is electronically available within the Code Composer Studio™ Integrated Development Environment (IDE). For a complete listing of C6000™ DSP latest documentation, visit the Texas Instruments web site on the Worldwide Web at http://www.ti.com uniform resource locator (URL).

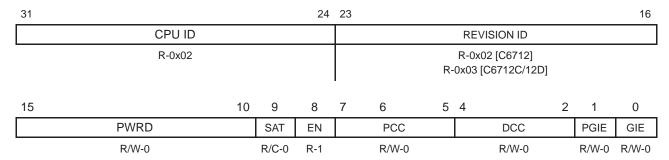
See the Worldwide Web URL for the application report *How To Begin Development with the TMS320C6712 DSP* (literature number SPRA693), which describes in more detail the compatibility and similarities/differences between the C6711 and C6712 devices.



CPU CSR register description

The CPU control status register (CSR) contains the CPU ID and CPU Revision ID (bits 16–31) as well as the status of the device power-down modes [PWRD field (bits 15–10)], program and data cache control modes, the endian bit (EN, bit 8) and the global interrupt enable (GIE, bit 0) and previous GIE (PGIE, bit 1). Figure 6 and Table 18 identify the bit fields in the CPU CSR register.

For more detailed information on the bit fields in the CPU CSR register, see the *TMS320C6000 DSP Peripherals Overview Reference Guide* (literature number SPRU190) and the *TMS320C6000 CPU and Instruction Set Reference Guide* (literature number SPRU189).



Legend: R = Readable by the MVC instruction, R/W = Readable/Writeable by the MVC instruction; W = Read/write; -n = value after reset, -x = undefined value after reset, C = Clearable by the MVC instruction

Figure 6. CPU Control Status Register (CPU CSR)

SGUS055 - SEPTEMBER 2004

CPU CSR register description (continued)

Table 18. CPU CSR Register Bit Field Description

| BIT# | NAME | DESCRIPTION |
|-------|-------------|--|
| 31:24 | CPU ID | CPU ID + REV ID. Read only. Identifies which CPU is used and defines the silicon revision of the CPU. |
| 23:16 | REVISION ID | CPU ID + REVISION ID (31:16) are combined for a value of: 0x0202 for C6712 and 0x0203 for C6712C/C6712D |
| 15:10 | PWRD | Control power-down modes. The values are always read as zero. 000000 = no power-down (default) 001001 = PD1, wake-up by an enabled interrupt 010001 = PD1, wake-up by an enabled or not enabled interrupt 011010 = PD2, wake-up by a device reset 011100 = PD3, wake-up by a device reset Others = Reserved |
| 9 | SAT | Saturate bit. Set when any unit performs a saturate. This bit can be cleared only by the MVC instruction and can be set only by a functional unit. The set by the a functional unit has priority over a clear (by the MVC instruction) if they occur on the same cycle. The saturate bit is set one full cycle (one delay slot) after a saturate occurs. This bit will not be modified by a conditional instruction whose condition is false. |
| 8 | EN | Endian bit. This bit is read-only. Depicts the device endian mode. 0 = Big Endian mode. 1 = Little Endian mode [default]. |
| 7:5 | PCC | Program Cache control mode. L1D, Level 1 Program Cache 000/010 = Cache Enabled / Cache accessed and updated on reads. All other PCC values reserved. |
| 4:2 | DCC | Data Cache control mode. L1D, Level 1 Data Cache 000/010 = Cache Enabled / 2-Way Cache All other DCC values reserved |
| 1 | PGIE | Previous GIE (global interrupt enable); saves the Global Interrupt Enable (GIE) when an interrupt is taken. Allows for proper nesting of interrupts. 0 = Previous GIE value is 0. (default) 1 = Previous GIE value is 1. |
| 0 | GIE | Global interrupt enable bit. Enables (1) or disables (0) all interrupts except the reset interrupt and NMI (nonmaskable interrupt). 0 = Disables all interrupts (except the reset interrupt and NMI) [default] 1 = Enables all interrupts (except the reset interrupt and NMI) |

cache configuration (CCFG) register description (12D)

The C6712D device includes an enhancement to the cache configuration (CCFG) register. A "P" bit (CCFG.31) allows the programmer to select the priority of accesses to L2 memory originating from the transfer crossbar (TC) over accesses originating from the L1D memory system. An important class of TC accesses is EDMA transfers, which move data to or from the L2 memory. While the EDMA normally has no issue accessing L2 memory due to the high hit rates on the L1D memory system, there are pathological cases where certain CPU behavior could block the EDMA from accessing the L2 memory for long enough to cause a missed deadline when transferring data to a peripheral such as the McASP or McBSP. This can be avoided by setting the P bit to "1" because the EDMA will assume a higher priority than the L1D memory system when accessing L2 memory.

For more detailed information on the P-bit function and for silicon advisories concerning EDMA L2 memory accesses blocked, see the *TMS320C6712*, *TMS320C6712C*, *TMS320C6712D Digital Signal Processors Silicon Errata* (literature number SPRZ182C or later).

| 31 | 30 | 10 | 9 | 8 | 7 | 3 | 2 0 |
|-------|----------|----|-----|-----|---------|----|---------|
| P† | Reserved | | ΙP | ID | Reserv | ed | L2MODE |
| R/W-0 | R-x | | W-0 | W-0 | R-0 000 | 00 | R/W-000 |

Legend: R = Readable; R/W = Readable/Writeable; -n = value after reset; -x = undefined value after reset † Unlike the C6712/12C devices, the C6712D device includes a P bit.

Figure 7. Cache Configuration Register (CCFG)

Table 19. CCFG Register Bit Field Description

| BIT# | NAME | DESCRIPTION |
|-------|----------|---|
| 31 | Р | L1D requestor priority to L2 bit. P = 0: L1D requests to L2 higher priority than TC requests P = 1: TC requests to L2 higher priority than L1D requests |
| 30:10 | Reserved | Reserved. Read-only, writes have no effect. |
| 9 | IP | Invalidate L1P bit. 0 = Normal L1P operation 1 = All L1P lines are invalidated |
| 8 | ID | Invalidate L1D bit. 0 = Normal L1D operation 1 = All L1D lines are invalidated |
| 7:3 | Reserved | Reserved. Read-only, writes have no effect. |
| 2:0 | L2MODE | L2 operation mode bits (L2MODE). 000b = L2 Cache disabled (All SRAM mode) [64K SRAM] 001b = 1-way Cache (16K L2 Cache) / [48K SRAM] 010b = 2-way Cache (32K L2 Cache) / [32K SRAM] 011b = 3-way Cache (48K L2 Cache) / [16K SRAM] 111b = 4-way Cache (64K L2 Cache) / [no SRAM] All others Reserved |

SGUS055 - SEPTEMBER 2004

interrupt sources and interrupt selector [C6712 only]

The C67x DSP core on the C6712 supports 16 prioritized interrupts, which are listed in Table 20. The highest-priority interrupt is INT_00 (dedicated to RESET) while the lowest-priority interrupt is INT_15. The first four interrupts (INT_00-INT_03) are non-maskable and fixed. The remaining interrupts (INT_04-INT_15) are maskable and default to the interrupt source specified in Table 20. The interrupt source for interrupts 4–15 can be programmed by modifying the selector value (binary value) in the corresponding fields of the Interrupt Selector Control registers: MUXH (address 0x019C0000) and MUXL (address 0x019C0004).

Table 20. C6712 DSP Interrupts

| DEFAULT INTERRUPT NUMBER | INTERRUPT SELECTOR CONTROL REGISTER | DEFAULT SELECTOR VALUE (BINARY) | INTERRUPT EVENT | INTERRUPT SOURCE |
|--------------------------------|--|--|--------------------|---------------------------------------|
| INT_00 | - | _ | RESET | |
| INT_01 | - | - | NMI | |
| INT_02 | - | - | Reserved | Reserved. Do not use. |
| INT_03 | - | - | Reserved | Reserved. Do not use. |
| INT_04 | MUXL[4:0] | 00100 | EXT_INT4 | External interrupt pin 4 |
| INT_05 | MUXL[9:5] | 00101 | EXT_INT5 | External interrupt pin 5 |
| INT_06 | MUXL[14:10] | 00110 | EXT_INT6 | External interrupt pin 6 |
| INT_07 | MUXL[20:16] | 00111 | EXT_INT7 | External interrupt pin 7 |
| INT_08 | MUXL[25:21] | 01000 | EDMA_INT | EDMA channel (0 through 15) interrupt |
| INT_09 | MUXL[30:26] | 01001 | Reserved | None, but programmable |
| INT_10 | MUXH[4:0] | 00011 | SD_INT | EMIF SDRAM timer interrupt |
| INT_11 | MUXH[9:5] | 01010 | Reserved | None, but programmable |
| INT_12 | MUXH[14:10] | 01011 | Reserved | None, but programmable |
| INT_13 | MUXH[20:16] | 00000 | Reserved | None, but programmable |
| INT_14 | MUXH[25:21] | 00001 | TINT0 | Timer 0 interrupt |
| INT_15 | MUXH[30:26] | 00010 | TINT1 | Timer 1 interrupt |
| _ | - | 01100 | XINT0 | McBSP0 transmit interrupt |
| _ | - | 01101 | RINT0 | McBSP0 receive interrupt |
| _ | _ | 01110 | XINT1 | McBSP1 transmit interrupt |
| _ | - | 01111 | RINT1 | McBSP1 receive interrupt |
| _ | _ | 10000 – 11111 | Reserved | Reserved. Do not use. |

[†] Interrupts INT_00 through INT_03 are non-maskable and fixed.

[‡] Interrupts INT_04 through INT_15 are programmable by modifying the binary selector values in the Interrupt Selector Control registers fields. Table 20 shows the default interrupt sources for interrupts INT_04 through INT_15. For more detailed information on interrupt sources and selection, see the *TMS320C6000 DSP Interrupt Selector Reference Guide* (literature number SPRU646).

interrupt sources and interrupt selector [C6712C/C6712D only]

The C67x DSP core on the C6712C/C6712D supports 16 prioritized interrupts, which are listed in Table 21. The highest priority interrupt is INT_00 (dedicated to RESET) while the lowest priority is INT_15. The first four interrupts are non-maskable and fixed. The remaining interrupts (4–15) are maskable and default to the interrupt source listed in Table 21. However, their interrupt source may be reprogrammed to any one of the sources listed in Table 22 (Interrupt Selector). Table 22 lists the selector value corresponding to each of the alternate interrupt sources. The selector choice for interrupts 4–15 is made by programming the corresponding fields (listed in Table 21) in the MUXH (address 0x019C0000) and MUXL (address 0x019C0004) registers.

Table 21. DSP Interrupts [C6712C/C6712D]

| Table 21. Dor Iliterrupts [Cor 120/Cor 12D] | | | | | | | | | |
|---|--|--|-------------------------------|--|--|--|--|--|--|
| DSP INTERRUPT NUMBER | INTERRUPT SELECTOR CONTROL REGISTER | DEFAULT SELECTOR VALUE (BINARY) | DEFAULT INTERRUPT EVENT | | | | | | |
| INT_00 | _ | ı | RESET | | | | | | |
| INT_01 | - | - | NMI | | | | | | |
| INT_02 | - | - | Reserved | | | | | | |
| INT_03 | - | _ | Reserved | | | | | | |
| INT_04 | MUXL[4:0] | 00100 | GPINT4 [†] | | | | | | |
| INT_05 | MUXL[9:5] | 00101 | GPINT5 [†] | | | | | | |
| INT_06 | MUXL[14:10] | 00110 | GPINT6 [†] | | | | | | |
| INT_07 | MUXL[20:16] | 00111 | GPINT7 [†] | | | | | | |
| INT_08 | MUXL[25:21] | 01000 | EDMAINT | | | | | | |
| INT_09 | MUXL[30:26] | 01001 | EMUDTDMA | | | | | | |
| INT_10 | MUXH[4:0] | 00011 | SDINT | | | | | | |
| INT_11 | MUXH[9:5] | 01010 | EMURTDXRX | | | | | | |
| INT_12 | MUXH[14:10] | 01011 | EMURTDXTX | | | | | | |
| INT_13 | MUXH[20:16] | 00000 | DSPINT | | | | | | |
| INT_14 | MUXH[25:21] | 00001 | TINT0 | | | | | | |
| INT_15 | MUXH[30:26] | 00010 | TINT1 | | | | | | |

Table 22. Interrupt Selector [12C/12D]

| Table 22: Interrupt delector [120/125] | | | | | | | | | |
|--|---------------------|-----------|--|--|--|--|--|--|--|
| INTERRUPT SELECTOR VALUE (BINARY) | INTERRUPT EVENT | MODULE | | | | | | | |
| 00000 | _ | - | | | | | | | |
| 00001 | TINT0 | Timer 0 | | | | | | | |
| 00010 | TINT1 | Timer 1 | | | | | | | |
| 00011 | SDINT | EMIF | | | | | | | |
| 00100 | GPINT4 [†] | GPIO | | | | | | | |
| 00101 | GPINT5 [†] | GPIO | | | | | | | |
| 00110 | GPINT6 [†] | GPIO | | | | | | | |
| 00111 | GPINT7 [†] | GPIO | | | | | | | |
| 01000 | EDMAINT | EDMA | | | | | | | |
| 01001 | EMUDTDMA | Emulation | | | | | | | |
| 01010 | EMURTDXRX | Emulation | | | | | | | |
| 01011 | EMURTDXTX | Emulation | | | | | | | |
| 01100 | XINT0 | McBSP0 | | | | | | | |
| 01101 | RINT0 | McBSP0 | | | | | | | |
| 01110 | XINT1 | McBSP1 | | | | | | | |
| 01111 | RINT1 | McBSP1 | | | | | | | |
| 10000 | GPINT0 | GPIO | | | | | | | |

[†] Interrupt Events GPINT4, GPINT5, GPINT6, and GPINT7 are outputs from the GPIO module (GP). They originate from the device pins GP[4](EXT_INT4), GP[5](EXT_INT5), GP[6](EXT_INT6), and GP[7](EXT_INT7). These pins can be used as edge-sensitive EXT_INTx with polarity controlled by the External Interrupt Polarity Register (EXTPOL.[3:0]). The corresponding pins must first be *enabled* in the GPIO module by setting the corresponding enable bits in the GP Enable Register (GPEN.[7:4]), and configuring them as *inputs* in the GP Direction Register (GPDIR.[7:4]). These interrupts can be controlled through the GPIO module in addition to the simple EXTPOL.[3:0] bits. For more information on interrupt control via the GPIO module, see the *TMS320C6000 DSP General-Purpose Input/Output (GPIO) Reference Guide* (literature number SPRU584). [C6712C/C6712D only].

SGUS055 - SEPTEMBER 2004

EDMA channel synchronization events [C6712 only]

The C67x EDMA on the C6712 device supports up to 16 EDMA channels. Four of the sixteen channels (channels 8–11) are reserved for EDMA chaining, leaving 12 EDMA channels available to service peripheral devices. Table 23 lists the source of synchronization events associated with each of the programmable EDMA channels. For the C6712, the association of an event to a channel is fixed; each of the EDMA channels has one specific event associated with it. For more detailed information on the EDMA module, associated channels, and event-transfer chaining, see the *TMS320C6000 DSP Enhanced Direct Memory Access (EDMA) Controller Reference Guide* (literature number SPRU234).

Table 23. 320C6712 EDMA Channel Synchronization Events

| EDMA CHANNEL | EVENT NAME | EVENT DESCRIPTION |
|-----------------|------------|---|
| 0 | _ | Reserved |
| 1 | TINT0 | Timer 0 interrupt |
| 2 | TINT1 | Timer 1 interrupt |
| 3 | SD_INT | EMIF SDRAM timer interrupt |
| 4 | EXT_INT4 | External interrupt pin 4 |
| 5 | EXT_INT5 | External interrupt pin 5 |
| 6 | EXT_INT6 | External interrupt pin 6 |
| 7 | EXT_INT7 | External interrupt pin 7 |
| 8† | EDMA_TCC8 | EDMA transfer complete code (TCC) 1000b interrupt |
| 9† | EDMA_TCC9 | EDMA TCC 1001b interrupt |
| 10† | EDMA_TCC10 | EDMA TCC 1010b interrupt |
| 11† | EDMA_TCC11 | EDMA TCC 1011b interrupt |
| 12 | XEVT0 | McBSP0 transmit event |
| 13 | REVT0 | McBSP0 receive event |
| 14 | XEVT1 | McBSP1 transmit event |
| 15 | REVT1 | McBSP1 receive event |

[†] EDMA channels 8 through 11 are used for transfer chaining only. For more detailed information on event-transfer chaining, see the TMS320C6000 DSP Enhanced Direct Memory Access (EDMA) Controller Reference Guide (literature number SPRU234).

EDMA module and EDMA selector [12C/12D only]

The C67x EDMA for the C6712C/C6712D device also supports up to 16 EDMA channels. Four of the sixteen channels (channels 8-11) are reserved for EDMA chaining, leaving 12 EDMA channels available to service peripheral devices. On the C6712C/C6712D device, the user, through the EDMA selector registers, can control the EDMA channels servicing peripheral devices.

The EDMA selector registers are located at addresses 0x01A0FF00 (ESEL0), 0x01A0FF04 (ESEL1), and 0x01A0FF0C (ESEL3). These EDMA selector registers control the mapping of the EDMA events to the EDMA channels. Each EDMA event has an assigned EDMA selector code (see Table 25). By loading each EVTSELx register field with an EDMA selector code, users can map any desired EDMA event to any specified EDMA channel. Table 24 lists the default EDMA selector value for each EDMA channel.

See Table 24 and Table 25 for the EDMA Event Selector registers and their associated bit descriptions.

Table 24. EDMA Channels [C6712C/C6712D Only]

| Table 24. EDMA Offamicia [007 120/007 12D Offiy] | | | | | | | | | | |
|--|---|--|--------------------------|--|--|--|--|--|--|--|
| EDMA CHANNEL | EDMA SELECTOR CONTROL REGISTER | DEFAULT SELECTOR VALUE (BINARY) | DEFAULT EDMA EVENT | | | | | | | |
| 0 | ESEL0[5:0] | 000000 | _ | | | | | | | |
| 1 | ESEL0[13:8] | 000001 | TINT0 | | | | | | | |
| 2 | ESEL0[21:16] | 000010 | TINT1 | | | | | | | |
| 3 | ESEL0[29:24] | 000011 | SDINT | | | | | | | |
| 4 | ESEL1[5:0] | 000100 | GPINT4 [†] | | | | | | | |
| 5 | ESEL1[13:8] | 000101 | GPINT5 [†] | | | | | | | |
| 6 | ESEL1[21:16] | 000110 | GPINT6 [†] | | | | | | | |
| 7 | ESEL1[29:24] | 000111 | GPINT7 [†] | | | | | | | |
| 8 | - | - | TCC8 (Chaining) | | | | | | | |
| 9 | - | - | TCC9 (Chaining) | | | | | | | |
| 10 | _ | _ | TCC10 (Chaining) | | | | | | | |
| 11 | - | - | TCC11 (Chaining) | | | | | | | |
| 12 | ESEL3[5:0] | 001000 | XEVT0 | | | | | | | |
| 13 | ESEL3[13:8] | 001001 | REVT0 | | | | | | | |
| 14 | ESEL3[21:16] | 001010 | XEVT1 | | | | | | | |
| 15 | ESEL3[29:24] | 001011 | REVT1 | | | | | | | |

Table 25. EDMA Selector [12C/12D Only]

| | | - 71 | | | |
|-----------------------------------|---------------------|--------|--|--|--|
| EDMA SELECTOR CODE (BINARY) | EDMA EVENT | MODULE | | | |
| 000000 | Reser | ved | | | |
| 000001 | TINT0 | TIMER0 | | | |
| 000010 | TINT1 | TIMER1 | | | |
| 000011 | SDINT | EMIF | | | |
| 000100 | GPINT4 [†] | GPIO | | | |
| 000101 | GPINT5 [†] | GPIO | | | |
| 000110 | GPINT6 [†] | GPIO | | | |
| 000111 | GPINT7 [†] | GPIO | | | |
| 001000 | Reserved | | | | |
| 001001 | Reser | ved | | | |
| 001010 | GPINT2 | GPIO | | | |
| 001011 | Reser | ved | | | |
| 001100 | XEVT0 | McBSP0 | | | |
| 001101 | REVT0 | McBSP0 | | | |
| 001110 | XEVT1 | McBSP1 | | | |
| 001111 | REVT1 McBSP1 | | | | |
| 010000-111111 | Reserved | | | | |

[†] The GPINT[4-7] interrupt events are sourced from the GPIO module via the external interrupt capable GP[4-7] pins [12C/12D only].

SGUS055 - SEPTEMBER 2004

EDMA module and EDMA selector [12C/12D only] (continued)

Table 26. EDMA Event Selector Registers (ESEL0, ESEL1, and ESEL3)

ESEL0 Register (0x01A0 FF00)

| 31 | 30 | 29 | 28 | 27 | 24 | 23 | 22 | 21 | 20 | 19 | 16 |
|------|----------|--------------|---------|--------------|----|------------------|------------------|----|----|--------------|----|
| Rese | rved | | | EVTSEL3 | | Res | erved | | | EVTSEL2 | |
| R- | -0 | R/W-00 0011b | | | | R-0 | | | | R/W-00 0010b | |
| 15 | 14 | 13 | 12 | 11 | 8 | 7 | 6 | 5 | 4 | 3 | 0 |
| Rese | Reserved | | EVTSEL1 | | | Res | Reserved EVTSEL0 | | | | |
| R-0 | | | | R/W-00 0001b | | R-0 R/W-00 0000b | | | | | |

Legend: R = Read only, R/W = Read/Write; -n = value after reset

ESEL1 Register (0x01A0 FF04)

| 31 | 30 | 29 | 28 | 27 | 24 | 23 | 22 | 21 | 20 | 19 | 16 |
|-------|----------|--------------|---------|--------------|----------|-----|---------|--------------|--------------|---------|----|
| Reser | ved | | | EVTSEL7 | | Res | erved | | | EVTSEL6 | |
| R-0 | 0 | R/W-00 0111b | | | R-0 | | | R/W-00 0110b | | | |
| 15 | 14 | 13 | 12 | 11 | 8 | 7 | 6 | 5 | 4 | 3 | 0 |
| Reser | Reserved | | EVTSEL5 | | Reserved | | EVTSEL4 | | | | |
| R-0 | | | | R/W-00 0101b | | R-0 | | | R/W-00 0100b | | |

Legend: R = Read only, R/W = Read/Write; -n = value after reset

ESEL3 Register (0x01A0 FF0C)

| 31 | 30 | 29 | 28 | 27 | 24 | 23 | 22 | 21 | 20 | 19 | 16 | |
|------|----------|--------------|----------|--------------|----|----------|-------|----|--------------|--------------|----|--|
| Rese | rved | | | EVTSEL15 | | Rese | erved | | | EVTSEL14 | | |
| R- | -0 | R/W-00 1111b | | | | R-0 | | | | R/W-00 1110b | | |
| 15 | 14 | 13 | 12 | 11 | 8 | 7 | 6 | 5 | 4 | 3 | 0 | |
| Rese | Reserved | | EVTSEL13 | | | Reserved | | | EVTSEL12 | | | |
| R-0 | | | | R/W-00 1101b | | R-0 | | | R/W-00 1100b | | | |

Legend: R = Read only, R/W = Read/Write; -n = value after reset

Table 27. EDMA Event Selection Registers (ESEL0, ESEL1, and ESEL3) Description

| BIT# | NAME | DESCRIPTION |
|--------------------------------|----------|---|
| 31:30 23:22 15:14 7:6 | Reserved | Reserved. Read-only, writes have no effect. |
| 29:24 21:16 13:8 5:0 | EVTSELx | EDMA event selection bits for channel x. Allows mapping of the EDMA events to the EDMA channels. The EVTSEL0 through EVTSEL15 bits correspond to the channels 0 to 15, respectively. These EVTSELx fields are user–selectable. By configuring the EVTSELx fields to the EDMA selector value of the desired EDMA sync event number (see Table 25), users can map any EDMA event to the EDMA channel. For example, if EVTSEL15 is programmed to 00 0001b (the EDMA selector code for TINT0), then channel 15 is triggered by Timer0 TINT0 events. |

clock PLL [C6712 only]

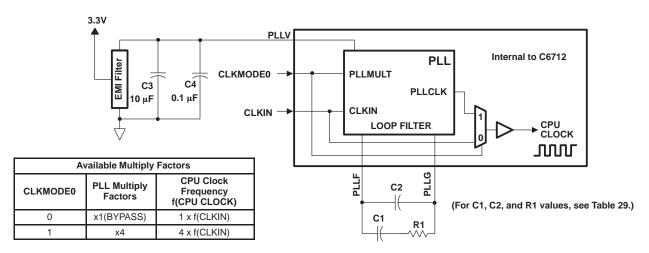
All of the internal C6712 clocks are generated from a single source through the CLKIN pin. This source clock either drives the PLL, which multiplies the source clock in frequency to generate the internal CPU clock, or bypasses the PLL to become the internal CPU clock.

To use the PLL to generate the CPU clock, the external PLL filter circuit must be properly designed. Figure 8 shows the external PLL circuitry for either x1 (PLL bypass) or x4 PLL multiply modes. Figure 9 shows the external PLL circuitry for a system with ONLY x1 (PLL bypass) mode.

To minimize the clock jitter, a single clean power supply should power both the C6712 device and the external clock oscillator circuit. Noise coupling into PLLF will directly impact PLL clock jitter. The minimum CLKIN rise and fall times should also be observed. For the input clock timing requirements, see the *input and output clocks* electricals section. Table 28 lists some examples of compatible CLKIN external clock sources.

COMPATIBLE PARTS FOR PART NUMBER **MANUFACTURER EXTERNAL CLOCK SOURCES (CLKIN)** JITO-2 Fox Electronix STA series, ST4100 series SaRonix Corporation Oscillators SG-636 **Epson America** 342 Corning Frequency Control PLL ICS525-02 Integrated Circuit Systems

Table 28. Compatible CLKIN External Clock Sources [C6712]



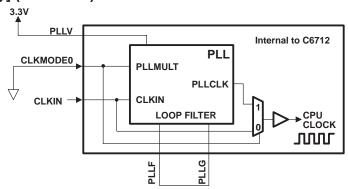
- NOTES: A. Keep the lead length and the number of vias between the PLLF pin, the PLLG pin, and R1, C1, and C2 to a minimum. In addition, place all PLL external components (R1, C1, C2, C3, C4, and the EMI Filter) as close to the C6000™ DSP device as possible. For the best performance, TI recommends that all the PLL external components be on a single side of the board without jumpers, switches, or components other than the ones shown.
 - B. For reduced PLL jitter, maximize the spacing between switching signals and the PLL external components (R1, C1, C2, C3, C4, and the EMI filter).
 - C. The 3.3-V supply for the EMI filter must be from the same 3.3-V power plane supplying the I/O voltage, DV_{DD}.
 - D. EMI filter manufacturer: TDK part number ACF451832-333, 223, 153, 103. Panasonic part number EXCCET103U.

Figure 8. External PLL Circuitry for Either PLL x4 Mode or x1 (Bypass) Mode [C6712]



SGUS055 - SEPTEMBER 2004

clock PLL [C6712 only] (continued)



- NOTES: A. For a system with ONLY PLL x1 (bypass) mode, short the PLLF terminal to the PLLG terminal.
 - B. The 3.3-V supply for the EMI filter must be from the same 3.3-V power plane supplying the I/O voltage, DV_{DD}.

Figure 9. External PLL Circuitry for x1 (Bypass) Mode Only [C6712]

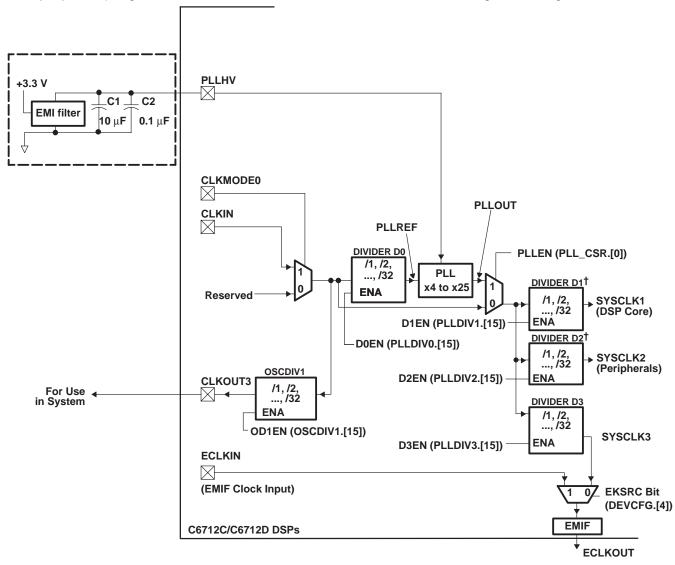
Table 29. C6712 PLL Component Selection Table

| CLKMODE | CLKIN RANGE (MHz) | CPU CLOCK FREQUENCY (CLKOUT1) RANGE (MHz) | CLKOUT2 RANGE (MHz) | R1 [±1%] (Ω) | C1 [±10%] (nF) | C2 [±10%] (pF) | TYPICAL LOCK TIME (μs)† |
|---------|-------------------------|--|---------------------------|-----------------|-------------------|-------------------|-------------------------------|
| x4 | 16.3-37.5 | 65-150 | 32.5-75 | 60.4 | 27 | 560 | 75 |

[†] Under some operating conditions, the maximum PLL lock time may vary as much as 150% from the specified typical value. For example, if the typical lock time is specified as 100 μ s, the maximum value may be as long as 250 μ s.

PLL and PLL controller [C6712C/C6712D only]

The 320C6712C/C6712D includes a PLL and a flexible PLL controller peripheral consisting of a prescaler (D0) and four dividers (OSCDIV1, D1, D2, and D3). The PLL controller is able to generate different clocks for different parts of the system (i.e., DSP core, Peripheral Data Bus, External Memory Interface, McASP, and other peripherals). Figure 10 illustrates the PLL, the PLL controller, and the clock generator logic.



† Dividers D1 and D2 must never be disabled. Never write a "0" to the D1EN or D2EN bits in the PLLDIV1 and PLLDIV2 registers.

- NOTES: A. Place all PLL external components (C1, C2, and the EMI Filter) as close to the C67x[™] DSP device as possible. For the best performance, TI recommends that all the PLL external components be on a single side of the board without jumpers, switches, or components other than the ones shown.
 - B. For reduced PLL jitter, maximize the spacing between switching signals and the PLL external components (C1, C2, and the EMI Filter).
 - C. The 3.3-V supply for the EMI filter must be from the same 3.3-V power plane supplying the I/O voltage, DV_{DD}.
 - D. EMI filter manufacturer TDK part number ACF451832-333, -223, -153, -103. Panasonic part number EXCET103U.

Figure 10. PLL and Clock Generator Logic [C6712C/C6712D Only]



SGUS055 - SEPTEMBER 2004

PLL and PLL controller [C6712C/C6712D only] (continued)

The PLL Reset Time is the amount of wait time needed when resetting the PLL (writing PLLRST=1), in order for the PLL to properly reset, before bringing the PLL out of reset (writing PLLRST = 0). For the PLL Reset Time value, see Table 30. The PLL Lock Time is the amount of time from when PLLRST = 0 with PLLEN = 0 (PLL out of reset, but still bypassed) to when the PLLEN bit can be safely changed to "1" (switching from bypass to the PLL path), see Table 30 and Figure 10.

Under some operating conditions, the maximum PLL Lock Time may vary from the specified typical value. For the PLL Lock Time values, see Table 30.

Table 30. PLL Lock and Reset Times (C6712C/C6712D only)

| | MIN | TYP | MAX | UNIT |
|----------------|-----|-----|-------|------|
| PLL Lock Time | | 75 | 187.5 | μs |
| PLL Reset Time | 125 | | | ns |

Table 31 shows the C6712C/C6712D device's CLKOUT signals, how they are derived and by what register control bits, and the default settings. For more details on the PLL, see the PLL and Clock Generator Logic diagram (Figure 10).

Table 31. CLKOUT Signals, Default Settings, and Control

| CLOCK OUTPUT SIGNAL NAME | | | DESCRIPTION |
|-----------------------------|---------------------------------------|--|--|
| CLKOUT2 | ON (ENABLED) | D2EN = 1 (PLLDIV2.[15]) CK2EN = 1 (EMIF GBLCTL.[3]) | SYSCLK2 selected [default] |
| CLKOUT3 | ON (ENABLED) | OD1EN = 1 (OSCDIV1.[15]) | Derived from CLKIN |
| ECLKOUT | ON (ENABLED); derived from SYSCLK3 | EKSRC = 0 (DEVCFG.[4]) EKEN = 1 (EMIF GBLCTL.[5]) | SYSCLK3 selected [default]. To select ECLKIN as source: EKSRC = 1 (DEVCFG.[4]) and EKEN = 1 (EMIF GBLCTL.[5]) |

This input clock is directly available as an internal high-frequency clock source that may be divided down by a programmable divider OSCDIV1 (/1, /2, /3, ..., /32) and output on the CLKOUT3 pin for other use in the system.

Figure 10 shows that the input clock source may be divided down by divider PLLDIV0 (/1, /2, ..., /32) and then multiplied up by a factor of x4, x5, x6, and so on, up to x25.

Either the input clock (PLLEN = 0) or the PLL output (PLLEN = 1) then serves as the high-frequency reference clock for the rest of the DSP system. The DSP core clock, the peripheral bus clock, and the EMIF clock may be divided down from this high-frequency clock (each with a unique divider) . For example, with a 40-MHz input, if the PLL output is configured for 300 MHz, the DSP core may be operated at 150 MHz (/2) while the EMIF may be configured to operate at a rate of 60 MHz (/5). Note that there is a specific minimum and maximum reference clock (PLLREF) and output clock (PLLOUT) for the block labeled PLL in Figure 10, as well as for the DSP core, peripheral bus, and EMIF. The clock generator must not be configured to exceed any of these constraints (certain combinations of external clock input, internal dividers, and PLL multiply ratios might not be supported). See Table 32 for the PLL clocks input and output frequency ranges.

PLL and PLL controller [C6712C/C6712D only] (continued)

Table 32. PLL Clock Frequency Ranges†‡

| | GDP16 | | | |
|---------------------|-------|-------------------------|------|--|
| CLOCK SIGNAL | MIN | MAX | UNIT | |
| PLLREF (PLLEN = 1) | 12 | 100 | MHz | |
| PLLOUT | 140 | 600 | MHz | |
| SYSCLK1 | - | Device Speed (DSP Core) | MHz | |
| SYSCLK3 (EKSRC = 0) | - | 100 | MHz | |

[†]SYSCLK2 rate *must* be exactly half of SYSCLK1.

The EMIF itself may be clocked by an external reference clock via the ECLKIN pin or can be generated on-chip as SYSCLK3. SYSCLK3 is derived from divider D3 off of PLLOUT (see Figure 10, PLL and Clock Generator Logic). The EMIF clock selection is programmable via the EKSRC bit in the DEVCFG register.

The settings for the PLL multiplier and each of the dividers in the clock generation block may be reconfigured via software at run time. If either the input to the PLL changes due to D0, CLKMODE0, or CLKIN, or if the PLL multiplier is changed, then software must enter bypass first and stay in bypass until the PLL has had enough time to lock (see electrical specifications). For the programming procedure, see the *TMS320C6000 DSP Software-Programmable Phase-Locked Loop (PLL) Controller Reference Guide* (literature number SPRU233).

SYSCLK2 is the internal clock source for peripheral bus control. SYSCLK2 (Divider D2) *must* be programmed to be half of the SYSCLK1 rate. For example, if D1 is configured to divide-by-2 mode (/2), then D2 *must* be programmed to divide-by-4 mode (/4). SYSCLK2 is also tied directly to CLKOUT2 pin (see Figure 10).

During the programming transition of Divider D1 and Divider D2 (resulting in SYSCLK1 and SYSCLK2 output clocks, see Figure 10), the order of programming the PLLDIV1 and PLLDIV2 registers must be observed to ensure that SYSCLK2 always runs at half the SYSCLK1 rate or slower. For example, if the divider ratios of D1 and D2 are to be changed from /1, /2 (respectively) to /5, /10 (respectively) then, the PLLDIV2 register must be programmed before the PLLDIV1 register. The transition ratios become /1, /2; /1, /10; and then /5, /10. If the divider ratios of D1 and D2 are to be changed from /3, /6 to /1, /2 then, the PLLDIV1 register must be programmed before the PLLDIV2 register. The transition ratios, for this case, become /3, /6; /1, /6; and then /1, /2. The final SYSCLK2 rate *must* be exactly half of the SYSCLK1 rate.

Note that Divider D1 and Divider D2 must **always** be enabled (i.e., D1EN and D2EN bits are set to "1" in the PLLDIV1 and PLLDIV2 registers).

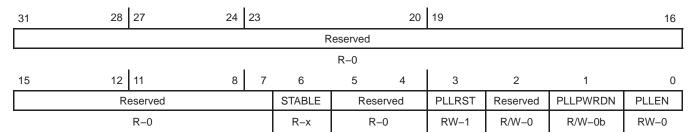
For detailed information on the clock generator (PLL Controller registers) and their associated software bit descriptions, see Table 33 through Table 36.

[‡] Also see the electrical specification (timing requirements and switching characteristics parameters) in the Input and Output Clocks section of this data sheet.

SGUS055 - SEPTEMBER 2004

PLL and PLL controller [C6712C/C6712D only] (continued)

PLLCSR Register (0x01B7 C100)



Legend: R = Read only, R/W = Read/Write; -n = value after reset

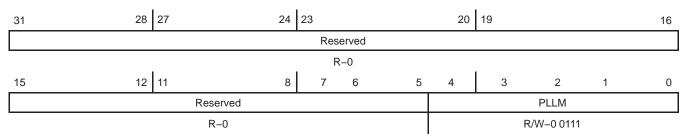
Table 33. PLL Control/Status Register (PLLCSR)

| BIT# | NAME | DESCRIPTION | | | |
|------|----------|---|--|--|--|
| 31:7 | Reserved | Reserved. Read-only, writes have no effect. | | | |
| 6 | STABLE | Clock Input Stable. This bit indicates if the clock input has stabilized. 0 - Clock input not yet stable. Clock counter is not finished counting (default). 1 - Clock input stable. | | | |
| 5:4 | Reserved | Reserved. Read-only, writes have no effect. | | | |
| 3 | PLLRST | Asserts RESET to PLL 0 - PLL Reset Released. 1 - PLL Reset Asserted (default). | | | |
| 2 | Reserved | Reserved. The user <i>must</i> write a "0" to this bit. | | | |
| 1 | PLLPWRDN | Select PLL Power Down 0 - PLL Operational (default). 1 - PLL Placed in Power-Down State. | | | |
| 0 | PLLEN | PLL Mode Enable 0 — Bypass Mode (default). PLL disabled. Divider D0 and PLL are bypassed. SYSCLK1/SYSCLK2/SYSCLK3 are divided down directly from input reference clock. 1 — PLL Enabled. Divider D0 and PLL are not bypassed. SYSCLK1/SYSCLK2/SYSCLK3 are divided down from PLL output. | | | |

SGUS055 - SEPTEMBER 2004

PLL and PLL controller [C6712C/C6712D only] (continued)

PLLM Register (0x01B7 C110)



Legend: R = Read only, R/W = Read/Write; -n = value after reset

Table 34. PLL Multiplier Control Register (PLLM)

| BIT# | NAME | DESCRIPTION | | | | | |
|------|----------|---|--|--|--|--|--|
| 31:5 | Reserved | Reserved. Read-only, writes have no effect. | | | | | |
| 4:0 | PLLM | PLL multiply mode [default is x7 (0 0111)]. 00000 = Reserved 10000 = x16 00001 = Reserved 10001 = x17 00010 = Reserved 10010 = x18 00011 = Reserved 10011 = x19 00100 = x4 | | | | | |

SGUS055 - SEPTEMBER 2004

PLL and PLL controller [C6712C/C6712D only] (continued)

PLLDIV0, PLLDIV1, PLLDIV2, and PLLDIV3 Registers (0x01B7 C114, 0x01B7 C118, 0x01B7 C11C, and 0x01B7 C120, respectively)

| 31 | | 28 27 | 24 | 23 | | 20 | 19 | | | 16 |
|-------|----------|-------|----|----------|---|------------|---------|---|---|----|
| | | | | Reserved | | | | | | |
| ' | | | | R-0 | | | | | | _ |
| 15 | 14 | 12 11 | 8 | 7 | 5 | 4 | 3 | 2 | 1 | 0 |
| DxEN | Reserved | | | | | | PLLDIVx | | | |
| R/W-1 | R-0 | | | | R | /W−x xxxx1 | t | | | |

Legend: R = Read only, R/W = Read/Write; -n = value after reset

CAUTION:

D1 and D2 should never be disabled. D3 should only be disabled if ECLKIN is used.

Table 35. PLL Wrapper Divider x Registers (Prescaler Divider D0 and Post-Scaler Dividers D1, D2, and D3)[‡]

| BIT# | NAME | DESCRIPTION | | | | | |
|-------|----------|---|--|--|--|--|--|
| 31:16 | Reserved | Reserved. Read-only, writes have no effect. | | | | | |
| 15 | DxEN | Divider Dx Enable (where x denotes 0 through 3). 0 — Divider x Disabled. No clock output. 1 — Divider x Enabled (default). These divider-enable bits are device-specific and must be set to 1 to enable. | | | | | |
| 14:5 | Reserved | Reserved. Read-only, writes have no effect. | | | | | |
| 4:0 | PLLDIVx | PLL Divider Ratio [Default values for the PLLDIV0, PLLDIV1, PLLDIV2, and PLLDIV3 bits are /1, /1, /2, and /2, respectively]. 00000 = /1 | | | | | |

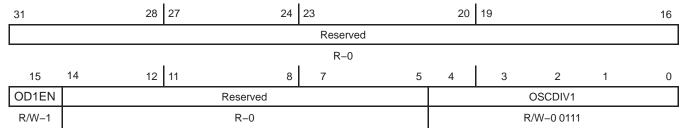
Note that SYSCLK2 *must* run at half the rate of SYSCLK1. Therefore, the divider ratio of D2 must be two times slower than D1. For example, if D1 is set to /2, then D2 *must* be set to /4.

[†] Default values for the PLLDIV0, PLLDIV1, PLLDIV2, and PLLDIV3 bits are /1 (0 0000), /1 (0 0000), /2 (0 0001), and /2 (0 0001), respectively.

SGUS055 - SEPTEMBER 2004

PLL and PLL controller [C6712C/C6712D only] (continued)

OSCDIV1 Register (0x01B7 C124)



Legend: R = Read only, R/W = Read/Write; -n = value after reset

The OSCDIV1 register controls the oscillator divider 1 for CLKOUT3. The CLKOUT3 signal does *not* go through the PLL path.

Table 36. Oscillator Divider 1 Register (OSCDIV1)

| BIT# | NAME | DESCRIPTION | | | | | |
|-------|----------|---|--|--|--|--|--|
| 31:16 | Reserved | Reserved. Read-only, writes have no effect. | | | | | |
| 15 | OD1EN | Oscillator Divider 1 Enable. 0 - Oscillator Divider 1 Disabled. 1 - Oscillator Divider 1 Enabled (default). | | | | | |
| 14:5 | Reserved | Reserved. Read-only, writes have no effect. | | | | | |
| 4:0 | OSCDIV1 | Oscillator Divider 1 Ratio [default is /8 (0 0111)]. 00000 = /1 | | | | | |

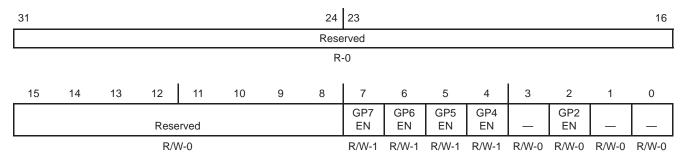
general-purpose input/output (GPIO)

To use the GP[7:4, 2] software-configurable GPIO pins, the GPxEN bits in the GP Enable (GPEN) Register and the GPxDIR bits in the GP Direction (GPDIR) Register must be properly configured.

GPxEN = 1 GP[x] pin is enabled GPxDIR = 0 GP[x] pin is an input GPxDIR = 1 GP[x] pin is an output

where "x" represents one of the 7 through 4, or 2 GPIO pins

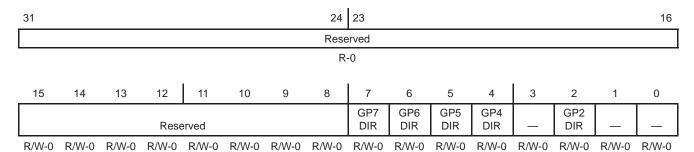
Figure 11 shows the GPIO enable bits in the GPEN register for the C6712C and C6712D devices. To use any of the GPx pins as general-purpose input/output functions, the corresponding GPxEN bit must be set to "1" (enabled). Default values are device-specific, so refer to Figure 11 for the C6712C/C6712D default configuration.



Legend: R/W = Readable/Writeable; -n = value after reset, -x = undefined value after reset

Figure 11. GPIO Enable Register (GPEN) [Hex Address: 01B0 0000]

Figure 12 shows the GPIO direction bits in the GPDIR register. This register determines if a given GPIO pin is an input or an output providing the corresponding GPxEN bit is enabled (set to "1") in the GPEN register. By default, all the GPIO pins are configured as input pins.



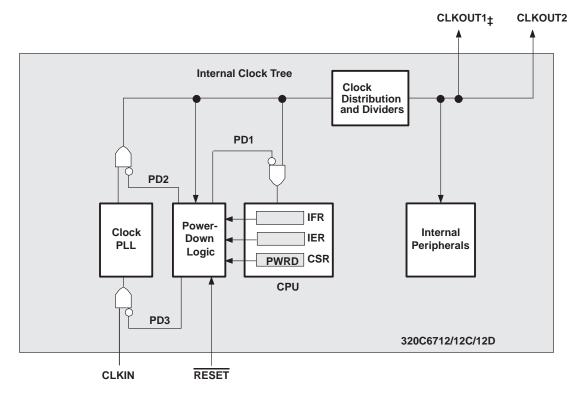
Legend: R/W = Readable/Writeable; -n = value after reset, -x = undefined value after reset

Figure 12. GPIO Direction Register (GPDIR) [Hex Address: 01B0 0004]

For more detailed information on general-purpose inputs/outputs (GPIOs), see the *TMS320C6000 DSP General-Purpose Input/Output (GPIO) Reference Guide* (literature number SPRU584).

power-down mode logic

Figure 13 shows the power-down mode logic on the C6712C/12D.



[†] External input clocks, with the exception of CLKOUT3 [12C/12D only] and CLKIN, are not gated by the power-down mode logic.

Figure 13. Power-Down Mode Logic[†]

triggering, wake-up, and effects

The power-down modes and their wake-up methods are programmed by setting the PWRD field (bits 15–10) of the control status register (CSR). The PWRD field of the CSR is shown in Figure 14 and described in Table 37. When writing to the CSR, all bits of the PWRD field should be set at the same time. Logic 0 should be used when "writing" to the reserved bit (bit 15) of the PWRD field. The CSR is discussed in detail in the *TMS320C6000 CPU* and *Instruction Set Reference Guide* (literature number SPRU189).

[‡]CLKOUT1 is applicable on the C6712 device only.

SGUS055 - SEPTEMBER 2004 31 16 15 14 13 12 11 10 Enable or Enabled PD3 PD2 PD1 Reserved Non-Enabled Interrupt Wake **Interrupt Wake** R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 7 0

Legend: R/W-x = Read/write reset value

NOTE: The shadowed bits are not part of the power-down logic discussion and therefore are not covered here. For information on these other bit fields in the CSR register, see the *TMS320C6000 CPU and Instruction Set Reference Guide* (literature number SPRU189).

Figure 14. PWRD Field of the CSR Register

A delay of up to nine clock cycles may occur after the instruction that sets the PWRD bits in the CSR before the PD mode takes effect. As best practice, NOPs should be padded after the PWRD bits are set in the CSR to account for this delay.

If PD1 mode is terminated by a non-enabled interrupt, the program execution returns to the instruction where PD1 took effect. If PD1 mode is terminated by an enabled interrupt, the interrupt service routine will be executed first, then the program execution returns to the instruction where PD1 took effect. In the case with an enabled, interrupt, the GIE bit in the CSR and the NMIE bit in the interrupt enable register (IER) must also be set in order for the interrupt service routine to execute; otherwise, execution returns to the instruction where PD1 took effect upon PD1 mode termination by an enabled interrupt.

PD2 and PD3 modes can only be aborted by device reset. Table 37 summarizes all the power-down modes.

| Table 27 | Characte | winting a | of 4ho | Power-Down | Madaa |
|----------|----------|------------|--------|------------|-------|
| Table 37 | Characte | eristics (| ot the | Power-Down | Wodes |

| PRWD FIELD (BITS 15–10) | POWER-DOWN MODE | WAKE-UP METHOD | EFFECT ON CHIP'S OPERATION |
|----------------------------|--------------------|---|--|
| 000000 | No power-down | _ | _ |
| 001001 | PD1 | Wake by an enabled interrupt | CPU halted (except for the interrupt logic) Power-down mode blocks the internal clock inputs at the |
| 010001 | PD1 | Wake by an enabled or non-enabled interrupt | boundary of the CPU, preventing most of the CPU's logic from switching. During PD1, EDMA transactions can proceed between peripherals and internal memory. |
| 011010 | PD2† | Wake by a device reset | Output clock from PLL is halted, stopping the internal clock structure from switching and resulting in the entire chip being halted. All register and internal RAM contents are preserved. All functional I/O "freeze" in the last state when the PLL clock is turned off. |
| 011100 | PD3† | Wake by a device reset | Input clock to the PLL stops generating clocks. All register and internal RAM contents are preserved. All functional I/O "freeze" in the last state when the PLL clock is turned off. Following reset, the PLL needs time to re-lock, just as it does following power-up. Wake-up from PD3 takes longer than wake-up from PD2 because the PLL needs to be re-locked, just as it does following power-up. |
| All others | Reserved | _ | _ |

[†] When entering PD2 and PD3, all functional I/O remains in the previous state. However, for peripherals which are asynchronous in nature or peripherals with an external clock source, output signals may transition in response to stimulus on the inputs. Under these conditions, peripherals will not operate according to specifications.

On C6712D silicon revision 2.0 and C6712C silicon revision 1.1, the device includes a programmable PLL which allows software control of PLL bypass via the PLLEN bit in the PLLCSR register. With this enhanced functionality comes some additional considerations when entering power-down modes.

The power-down modes (PD2 and PD3) function by disabling the PLL to stop clocks to the device. However, if the PLL is bypassed (PLLEN = 0), the device will still receive clocks from the external clock input (CLKIN). Therefore, bypassing the PLL makes the power-down modes PD2 and PD3 ineffective.

Make sure that the PLL is enabled by writing a "1" to PLLEN bit (PLLCSR.0) before writing to either PD3 (CSR.11) or PD2 (CSR.10) to enter a power-down mode.

power-supply sequencing

TI DSPs do not require specific power sequencing between the core supply and the I/O supply. However, systems should be designed to ensure that neither supply is powered up for extended periods of time (>1 second) if the other supply is below the proper operating voltage.

system-level design considerations

System-level design considerations, such as bus contention, may require supply sequencing to be implemented. In this case, for **C6712**, the core supply should be powered up at the same time as, or prior to (and powered down after) the I/O buffers. For **C6712C/12D**, the core supply should be powered up prior to (and powered down after), the I/O buffers. This is to ensure that the I/O buffers receive valid inputs from the core before the output buffers are powered up, thus, preventing bus contention with other chips on the board.

power-supply design considerations

A dual-power supply with simultaneous sequencing can be used to eliminate the delay between core and I/O power up. A Schottky diode can also be used to tie the core rail to the I/O rail (see Figure 15).

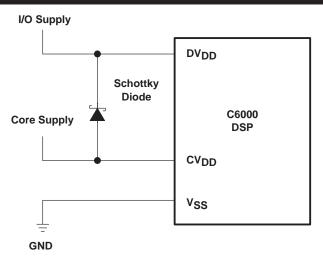


Figure 15. Schottky Diode Diagram

Core and I/O supply voltage regulators should be located close to the DSP (or DSP array) to minimize inductance and resistance in the power delivery path. Additionally, when designing for high-performance applications utilizing the C6000™ platform of DSPs, the PC board should include separate power planes for core, I/O, and ground, all bypassed with high-quality low-ESL/ESR capacitors.

C6712 device applicable only

On systems using C62x and C67x DSPs, like the C6712 device, the core may consume in excess of 2 A per DSP until the I/O supply powers on. This extra current results from uninitialized logic within the DSP(s). A normal current state returns once the I/O power supply turns on and the CPU sees a clock pulse. Decreasing the amount of time between the core supply power-up and the I/O supply power-up reduces the effects of the current draw. If the external supply to the DSP core cannot supply the excess current, the minimum core voltage may not be achieved until after normal current returns. This voltage starvation of the core supply during power up will not affect run-time operation. Voltage starvation can affect power supply systems that gate the I/O supply via the core supply, causing the I/O supply to never turn on. During the transition from excess to normal current, a voltage spike may be seen on the core supply. Care must be taken when designing overvoltage protection circuitry on the core supply to not restart the power sequence due to this spike. Otherwise, the supply may cycle indefinitely.

SGUS055 - SEPTEMBER 2004

power-supply decoupling

In order to properly decouple the supply planes from system noise, place as many capacitors (caps) as possible close to the DSP. Assuming 0603 caps, the user should be able to fit a total of 60 caps — 30 for the core supply and 30 for the I/O supply. These caps need to be close (no more than 1.25 cm maximum distance) to the DSP to be effective. Physically smaller caps are better, such as 0402, but the size needs to be evaluated from a yield/manufacturing point-of-view. Parasitic inductance limits the effectiveness of the decoupling capacitors, therefore physically smaller capacitors should be used while maintaining the largest available capacitance value. As with the selection of any component, verification of capacitor availability over the product's production lifetime needs to be considered.

IEEE 1149.1 JTAG compatibility statement

The 320C6712/12C/12D DSP requires that both \overline{TRST} and \overline{RESET} be asserted upon power up to be properly initialized. While \overline{RESET} initializes the DSP core, \overline{TRST} initializes the DSP's emulation logic. Both resets are required for proper operation.

While both $\overline{\text{RRST}}$ and $\overline{\text{RESET}}$ need to be asserted upon power up, only $\overline{\text{RESET}}$ needs to be released for the DSP to boot properly. $\overline{\text{TRST}}$ may be asserted indefinitely for normal operation, keeping the JTAG port interface and DSP's emulation logic in the reset state.

TRST only needs to be released when it is necessary to use a JTAG controller to debug the DSP or exercise the DSP's boundary scan functionality.

For maximum reliability, the 320C6712/12C/12D DSP includes an internal pulldown (IPD) on the TRST pin to ensure that TRST will always be asserted upon power up and the DSP's internal emulation logic will always be properly initialized.

JTAG controllers from Texas Instruments actively drive TRST high. However, some third-party JTAG controllers may not drive TRST high but expect the use of a pullup resistor on TRST.

When using this type of JTAG controller, assert TRST to initialize the DSP after powerup and externally drive TRST high before attempting any emulation or boundary scan operations. Following the release of RESET, the low-to-high transition of TRST must be "seen" to latch the state of EMU1 and EMU0. The EMU[1:0] pins configure the device for either Boundary Scan mode or Emulation mode. For more detailed information, see the terminal functions section of this data sheet.

EMIF device speed

The maximum EMIF speed on the C6712C/C6712D device is 100 MHz. TI recommends utilizing I/O buffer information specification (IBIS) to analyze all AC timings to determine if the maximum EMIF speed is achievable for a given board layout. To properly use IBIS models to attain accurate timing analysis for a given system, see the *Using IBIS Models for Timing Analysis* application report (literature number SPRA839).

For ease of design evaluation, Table 38 contains IBIS simulation results showing the maximum EMIF-SDRAM interface speeds for the given example boards (TYPE) and SDRAM speed grades. Timing analysis should be performed to verify that all AC timings are met for the specified board layout. Other configurations are also possible, but again, timing analysis must be done to verify proper AC timings.

To maintain signal integrity, serial termination resistors should be inserted into all EMIF output signal lines (see the Terminal Functions table for the EMIF output signals).

Table 38. C6712C/C6712D Example Boards and Maximum EMIF Speed

| | BOARD CONFIGU | IRATION | | MAXIMUM ACHIEVABLE | |
|-------------------------|----------------------------------|--|----------------------------|---|---|
| TYPE | EMIF INTERFACE COMPONENTS | BOARD TRACE | SDRAM SPEED GRADE | EMIF-SDRAM INTERFACE SPEED | |
| | | | 143 MHz 32-bit SDRAM (-7) | 100 MHz | |
| 1-Load | One bank of one | 1 to 3-inch traces with proper | 166 MHz 32-bit SDRAM (-6) | For short traces, SDRAM data output hold time on these | |
| Short Traces | 32-Bit SDRAM | termination resistors; Trace impedance $\sim 50 \Omega$ | 183 MHz 32-bit SDRAM (-55) | SDRAM speed grades cannot meet EMIF input hold time | |
| | | | 200 MHz 32-bit SDRAM (-5) | requirement (see NOTE 1). | |
| | | | 125 MHz 16-bit SDRAM (-8E) | 100 MHz | |
| l | | 1.2 to 3 inches from EMIF to | 133 MHz 16-bit SDRAM (-75) | 100 MHz | |
| 2-Loads Short Traces | One bank of two 16-Bit SDRAMs | each load, with proper termination resistors; | 143 MHz 16-bit SDRAM (-7E) | 100 MHz | |
| Onort Traces | | Trace impedance ~ 78 Ω | 167 MHz 16-bit SDRAM (-6A) | 100 MHz | |
| | | | 167 MHz 16-bit SDRAM (-6) | 100 MHz | |
| | | | 125 MHz 16-bit SDRAM (-8E) | For short traces, EMIF cannot meet SDRAM input hold requirement (see NOTE 1). | |
| | One bank of two | 1.2 to 3 inches from EMIF to | 133 MHz 16-bit SDRAM (-75) | 100 MHz | |
| 3-Loads Short Traces | 32-Bit SDRAMs | each load, with proper termination resistors; | 143 MHz 16-bit SDRAM (-7E) | 100 MHz | |
| Short fraces | One bank of buffer | Trace impedance ~ 78 Ω | 167 MHz 16-bit SDRAM (-6A) | 100 MHz | |
| | | · | 167 MHz 16-bit SDRAM (-6) | For short traces, EMIF cannot meet SDRAM input hold requirement (see NOTE 1). | |
| | | | 143 MHz 32-bit SDRAM (-7) | 83 MHz | |
| | One bank of one | | 166 MHz 32-bit SDRAM (-6) | 83 MHz | |
| 3-Loads | 32-Bit SDRAM One bank of one | 4 to 7 inches from EMIF; | 183 MHz 32-bit SDRAM (-55) | 83 MHz | |
| Long Traces | 32-Bit SBSRAM One bank of buffer | 32-Bit SBSRAM Trace impedance $\sim 63 \Omega$ | | 200 MHz 32-bit SDRAM (-5) | SDRAM data output hold time cannot meet EMIF input hold requirement (see NOTE 1). |

NOTE 1: Results are based on IBIS simulations for the given example boards (**TYPE**). Timing analysis should be performed to determine if timing requirements can be met for the particular system.

EMIF big endian mode correctness [C6712D only]

The device Endian mode pin (LENDIAN) selects the endian mode of operation (little endian or big endian) for the C6712D device. Little endian is the default setting.

When Big Endian mode is selected (LENDIAN = 0), the EMIF Big Endian mode correctness pin (EMIFBE) *must* to be pulled low. Figure 16 shows the mapping of 16-bit and 8-bit data for C6712D devices with EMIF endianness correction.

| EMIF DATA LINES (PINS) WHERE DATA PRESENT | | | | | |
|---|-------------------------------------|--|--|--|--|
| ED[15:8] (BE1) | ED[7:0] (BE0) | | | | |
| 16-Bit Device in | Any Endianness Mode | | | | |
| | 8-Bit Device in Any Endianness Mode | | | | |

[†] The C6712/C6712C devices support Little Endian mode of operation only.

Figure 16. 16/8-Bit EMIF Big Endian Mode Correctness Mapping [C6712D Only]

This new feature does *not* affect systems operating in Little Endian mode, providing the default value of the C15 pin =1 is used.



SGUS055 - SEPTEMBER 2004

bootmode

The C67x™ device resets using the active-low signal RESET and the internal reset signal (C6712C/C6712D; for the C6712 device, the RESET signal is the same as the internal reset signal). While RESET is low, the internal reset is also asserted and the device is held in reset and is initialized to the prescribed reset state. Refer to reset timing for reset timing characteristics and states of device pins during reset. The release of the internal reset signal (see the Reset Phase 3 discussion in the Reset Timing section of this data sheet) starts the processor running with the prescribed device configuration and boot mode.

The C6712/C6712C/C6712D has two type of boot mode:

Emulation boot

In Emulation boot mode, it is not necessary to load valid code into internal memory. The emulation driver will release the CPU from the "stalled" state, at which point the CPU will vector to address 0. Prior to beginning execution, the emulator sets a breakpoint at address 0. This prevents the execution of invalid code by halting the CPU prior to executing the first instruction. Emulation boot is a good tool in the debug phase of development.

EMIF boot (using default ROM timings)

Upon the release of internal reset, the 1K-Byte ROM code located in the beginning of $\overline{\text{CE1}}$ is copied to address 0 by the EDMA using the default ROM timings, while the CPU is internally "stalled". The data should be stored in the endian format that the system is using. The boot process also lets you choose the width of the ROM. In this case, the EMIF automatically assembles consecutive 8-bit bytes or 16-bit half-words to form the 32-bit instruction words to be copied. The transfer is automatically done by the EDMA as a single-frame block transfer from the ROM to address 0. After completion of the block transfer, the CPU is released from the "stalled" state and starts running from address 0.

absolute maximum ratings over operating case temperature range (unless otherwise noted)†

| Supply voltage range, | CV _{DD} (see Note 2): | (C6712C/C6712D only) | – 0.3 V to 1.8 V |
|------------------------|--------------------------------|----------------------|---|
| | | (C6712) | – 0.3 V to 2.3 V |
| Supply voltage range, | DV _{DD} (see Note 2) | | 0.3 V to 4 V |
| Input voltage ranges: | (C6712C/C6712D | only) | $-0.3 \text{ V to DV}_{DD} + 0.5 \text{ V}$ |
| | (C6712) | | 0.3 V to 4 V |
| Output voltage ranges: | (C6712C/C6712D | only) | $-0.3 \text{ V to DV}_{DD} + 0.5 \text{ V}$ |
| | (C6712) | | 0.3 V to 4 V |
| Operating case temper | ature range, T _C | | 40°C to 105°C |
| Storage temperature ra | ange, T _{stg} | | 65°C to 150°C |
| | | | |

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 2: All voltage values are with respect to VSS



SGUS055 - SEPTEMBER 2004

recommended operating conditions

| | | | MIN | NOM | MAX | UNIT | |
|---|---|--|--|-------|----------------------|------|--|
| O)/ | Complessaltana Canat | (C6712C/C6712D only) | 1.14§ | 1.20§ | 1.32 | V | |
| CVDD | Supply voltage, Core‡ | (C6712) | 1.14\$ 1.20\$ 1.32 1.71 1.8 1.89 3.13 3.3 3.47 3.14 3.3 3.46 0 0 0 0 2 2 2 2 0.8 0.3*DVDD 0.8 T -4 -8 -16 | V | | | |
| D) / | 0 | (C6712C/C6712D only) | 1.14\$ 1.20\$ 1.32 1.71 1.8 1.89 3.13 3.3 3.47 3.14 3.3 3.46 0 0 0 0 2 2 2 2 0.8 0.3*DVDD 0.8 -4 -8 -16 -8 -16 4 8 | V | | | |
| DV_{DD} | Supply voltage, I/O‡ | (C6712) | 3.14 | 3.3 | 3.46 | V | |
| V _{SS} | Supply ground | | 0 | 0 | 0 | V | |
| | High-level input voltage | All signals except CLKS1, DR1, and RESET | 2 | | | | |
| V_{IH} | (C6712C/12D only) | CLKS1, DR1, and RESET | 2 | | | V | |
| | High-level input voltage (C | 6712) | 2 | | | | |
| | Low-level input voltage | All signals except CLKS1, DR1, and RESET | | | 0.8 | | |
| \vee_{IL} | (C6712C/12D only) | CLKS1, DR1, and RESET | | | 0.3*DV _{DD} | V | |
| | Low-level input voltage (Co | 6712) | 2, and ECLKOUT – 2 CLKOUT3 | 0.8 | | | |
| | High-level output current (C6712) | All signals except CLKOUT1, CLKOUT2, and ECLKOUT | | | -4 | | |
| | | CLKOUT1, CLKOUT2, and ECLKOUT | | | -8 | | |
| | High-level output current (C6712C)¶ All signals except ECLKOUT, CLKOUT2, CLKOUT3, CLKS1, and DR1 ECLKOUT, CLKOUT2, and CLKOUT3 —1 All signals except ECLKOUT, CLKOUT3 —1 All signals except ECLKOUT, CLKOUT3 —1 All signals except ECLKOUT, CLKOUT2, CLKS1, and DR1 | | | | -8 | mA | |
| IOH | | ECLKOUT, CLKOUT2, and CLKOUT3 | | | -16 | | |
| | | -8 | mA | | | | |
| | (C6/12D)11 | ECLKOUT and CLKOUT2 | | | -16 | | |
| | Low-level output current | All signals except CLKOUT1, CLKOUT2, and ECLKOUT | 3.14 3.3 3.46 0 0 0 0 2 2 2 2 0.8 0.3*DV _{DD} 0.8 -4 -8 -16 -8 -16 4 8 8 16 3 8 | ^ | | | |
| | (C6712) | CLKOUT1, CLKOUT2, and ECLKOUT | | | 8 | mA | |
| | Low-level output current | All signals except ECLKOUT, CLKOUT2, CLKOUT3, CLKS1, and DR1 | | | 8 | mA | |
| IOH (C6712C)¶ ECLKOUT, CLKOUT2, and CLKOUT3 All signals except ECLKOUT, CLKOUT2, CLKS1, and DR1 ECLKOUT and CLKOUT2 Low-level output current (C6712C)¶ Low-level output current (C6712C)¶ Low-level output current (C6712C)¶ ECLKOUT and CLKOUT2, and ECLKOUT All signals except CLKOUT1, CLKOUT2, and ECLKOUT CLKOUT1, CLKOUT2, and ECLKOUT All signals except ECLKOUT, CLKOUT3, CLKS1, and DR1 ECLKOUT, CLKOUT2, and CLKOUT3 CLKS1 and DR1 | 16 | | | | | | |
| IOL | | CLKS1 and DR1 | | | 3 | mA | |
| | Low-level output current | All signals except ECLKOUT, CLKOUT2, CLKS1, and DR1 | | | 8 | mA | |
| | (C6712D)¶ | ECLKOUT and CLKOUT2 | | | 16 | 1 | |
| | | CLKS1 and DR1 | | | 3 | mA | |
| T _C | Operating case temperatu | re | -40 | | 105 | °C | |

[‡] For the C6712 device, the core supply should be powered up at the same time as, or prior to (and powered down after), the I/O supply. For the C6712C/12D device, the core supply should be powered up prior to (and powered down after), the I/O supply. Systems should be designed to ensure that neither supply is powered up for an extended period of time if the other supply is below the proper operating voltage.

[§] These values are compatible with existing 1.26V designs.

[¶] Refers to DC (or steady state) currents only, actual switching currents are higher. For more details, see the device-specific IBIS models.

electrical characteristics over recommended ranges of supply voltage and operating case temperature[†] (unless otherwise noted)

| | PARA | AMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|-------------------------|--|---|-----|---|---|------|
| Vон | High-level output | 12C/12D: All signals except CLKS1 and DR1 | DV _{DD} = MIN, I _{OH} = MAX | 2.4 | | | V |
| " | voltage | C6712: All signals | $DV_{DD} = MIN, I_{OH} = MAX$ | 2.4 | | 0.4 0.4 0.4 ±170 ±10 ±150 ±170 ±10 ±10 5 | V |
| | Low-level output | 12C/12D: All signals except CLKS1 and DR1 | $DV_{DD} = MIN, I_{OL} = MAX$ | | | 0.4 | V |
| VOL | voltage | 12C/12D: CLKS1 and DR1 | | | | 0.4 | V |
| | | C6712: All signals | $DV_{DD} = MIN, I_{OL} = MAX$ | | 0.4 0.4 0.4 170 ±170 ±10 ±150 ±170 ±10 336 180 430 475 50 75 7 7 | V | |
| | | 12C/12D: All signals except CLKS1 and DR1 | V _I = V _{SS} to DV _{DD} | | | ±170 | uA |
| 1 | Input current | 12C/12D: CLKS1 and DR1 | 7 | | | ±10 | uA |
| | | C6712: All signals | $V_I = V_{SS}$ to DV_{DD} | | 0.4 0.4 0.4 170 1170 110 110 110 110 1336 180 430 475 50 75 7 7 7 | uA | |
| | Off-state output | -state output CLKS1 and DR1 VO = DVDD or 0 V | | | | ±170 | uA |
| loz | current | 12C/12D: CLKS1 and DR1 | 7 | | | 0.4 0.4 0.4 170 ±170 ±150 ±170 ±10 ±10 36 30 75 7 7 7 | uA |
| | | C6712: All signals | $V_O = DV_{DD}$ or 0 V | | | 0.4 0.4 0.4 ±170 ±10 ±150 ±170 ±10 7 7 | uA |
| | Supply current, CPU - | + CPU memory access [‡] | C6712, CV _{DD} = NOM, CPU clock = 100 MHz | | 336 | 0.4 ±170 ±10 ±150 ±170 ±10 ±10 | mA |
| IDD2V | Supply current, periph | erals [‡] | C6712, CV _{DD} = NOM, CPU clock = 100 MHz | | 180 | | mA |
| | 0 | 2074004405)† | C6712C, CV _{DD} = 1.26 V, CPU clock = 150 MHz | | 430 | | mA |
| VOL I I I I I I I I I I I I I I I I I I | Core supply current (C | C6/12C/12D)+ | C6712D, CV _{DD} = 1.26 V, CPU clock = 167 MHz | | 475 | | mA |
| I _{DD3V} | Supply current, I/O pir | ns‡ | C6712, DV _{DD} = NOM, CPU clock = 100 MHz | | 50 | | mA |
| I _{DD3V} | I/O supply current (C6 | 712C/12D) [‡] | DV _{DD} = 3.3 V, EMIF speed = 100 MHz | | 75 | | mA |
| | Innut can a state a | C6712 | | 7 | <u> </u> | | |
| C _i | Input capacitance | C6712C/C6712D | | | | 7 | pF |
| | Output capacitance | C6712 | | | | 7 | pF |
| C ₀ | Output capacitance | C6712C/C6712D | | | | 7 | ρг |

[†] For test conditions shown as MIN, MAX, or NOM, use the appropriate value specified in the recommended operating conditions table.

For the **C6712C/12D** device, these currents were measured with average activity (50% high/50% low power) at 25°C case temperature and 100-MHz EMIF. This model represents a device performing high-DSP-activity operations 50% of the time, and the remainder performing low-DSP-activity operations. The high/low-DSP-activity models are defined as follows: High-DSP-Activity Model:

CPU: 8 instructions/cycle with 2 LDDW instructions [L1 Data Memory: 128 bits/cycle via LDDW instructions;

L1 Program Memory: 256 bits/cycle; L2/EMIF EDMA: 50% writes, 50% reads to/from SDRAM (50% bit-switching)]

McBSP: 2 channels at E1 rate Timers: 2 timers at maximum rate

Low-DSP-Activity Model:

CPU: 2 instructions/cycle with 1 LDH instruction [L1 Data Memory: 16 bits/cycle; L1 Program Memory: 256 bits per 4 cycles;

L2/EMIF EDMA: None]
McBSP: 2 channels at E1 rate
Timers: 2 timers at maximum rate

The actual current draw is highly application-dependent. For more details on core and I/O activity, refer to the *TMS320C6713/12C/11C Power Consumption Summary* application report (literature number SPRA889).



For the **C6712** device, these currents were measured with average activity (50% high/50% low power). For more details on CPU, peripheral, and I/O activity, see the *TMS320C62x/C67x Power Consumption Summary* application report (literature number SPRA486).

PARAMETER MEASUREMENT INFORMATION

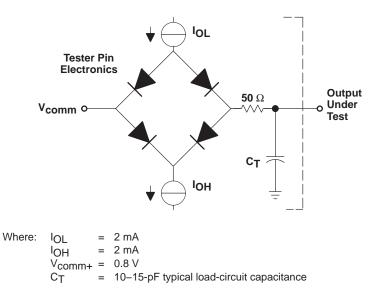
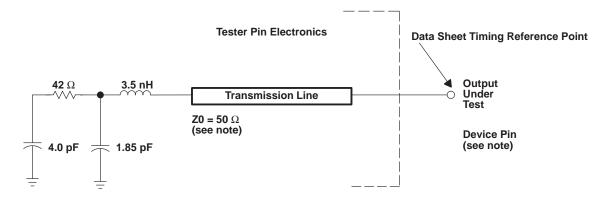


Figure 17. Test Load Circuit for AC Timing Measurements for C6712 Only



NOTE: The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. A transmission line with a delay of 2 ns or longer can be used to produce the desired transmission line effect. The transmission line is intended as a load only. It is not necessary to add or subtract the transmission line delay (2 ns or longer) from the data sheet timings.

Input requirements in this data sheet are tested with an input slew rate of < 4 Volts per nanosecond (4 V/ns) at the device pin.

Figure 18. Test Load Circuit for AC Timing Measurements for C6712C/C6712D Only

PARAMETER MEASUREMENT INFORMATION (CONTINUED)

signal transition levels

All input and output timing parameters are referenced to 1.5 V for both "0" and "1" logic levels.



Figure 19. Input and Output Voltage Reference Levels for ac Timing Measurements

All rise and fall transition timing parameters are referenced to V_{IL} MAX and V_{IH} MIN for input clocks, and V_{OL} MAX and V_{OH} MIN for output clocks.

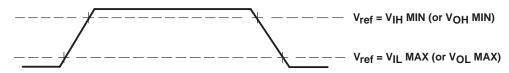


Figure 20. Rise and Fall Transition Time Voltage Reference Levels

timing parameters and board routing analysis

The timing parameter values specified in this data sheet do *not* include delays by board routings. As a good board design practice, such delays must *always* be taken into account. Timing values may be adjusted by increasing/decreasing such delays. TI recommends utilizing the available I/O buffer information specification (IBIS) models to analyze the timing characteristics correctly. To properly use IBIS models to attain accurate timing analysis for a given system, see the *Using IBIS Models for Timing Analysis* application report (literature number SPRA839). If needed, external logic hardware such as buffers may be used to compensate any timing differences.

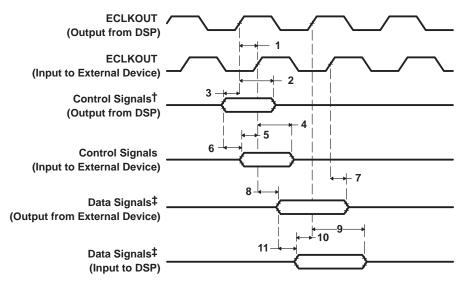
For inputs, timing is most impacted by the round-trip propagation delay from the DSP to the external device and from the external device to the DSP. This round-trip delay tends to negatively impact the input setup time margin, but also tends to improve the input hold time margins (see Table 39 and Figure 21).

Figure 21 represents a general transfer between the DSP and an external device. The figure also represents board route delays and how they are perceived by the DSP and the external device.

PARAMETER MEASUREMENT INFORMATION (CONTINUED)

Table 39. Board-Level Timings Example (see Figure 21)

| NO. | DESCRIPTION |
|-----|--|
| 1 | Clock route delay |
| 2 | Minimum DSP hold time |
| 3 | Minimum DSP setup time |
| 4 | External device hold time requirement |
| 5 | External device setup time requirement |
| 6 | Control signal route delay |
| 7 | External device hold time |
| 8 | External device access time |
| 9 | DSP hold time requirement |
| 10 | DSP setup time requirement |
| 11 | Data route delay |



[†] Control signals include data for Writes.

Figure 21. Board-Level Input/Output Timings

[‡] Data signals are generated during Reads from an external device.

INPUT AND OUTPUT CLOCKS

timing requirements for CLKIN^{†‡} (see Figure 22) [C6712]

| | | | | -100 | | | |
|-----|------------------------|----------------------------|--------|--------|--------|--------|------|
| NO. | | | CLKMOD | E = x4 | CLKMOD | E = x1 | UNIT |
| | | | MIN | MAX | MIN | MAX | |
| 1 | tc(CLKIN) | Cycle time, CLKIN | 40 | | 10 | | ns |
| 2 | tw(CLKINH) | Pulse duration, CLKIN high | 0.4C | | 0.45C | | ns |
| 3 | tw(CLKINL) | Pulse duration, CLKIN low | 0.4C | | 0.45C | | ns |
| 4 | t _t (CLKIN) | Transition time, CLKIN | | 5 | | 1 | ns |

[†] The reference points for the rise and fall transitions are measured at V_{IL} MAX and V_{IH} MIN.

timing requirements for CLKIN^{†‡§} (see Figure 22) [C6712C/C6712D]

| | | | | -167 | | | | |
|-----|------------------------|----------------------------|-------|------|------------------|-----|------|--|
| NO. | | | PLL M | _ | BYPASS (PLLEN | _ | UNIT | |
| | | | MIN | MAX | MIN | MAX | | |
| 1 | tc(CLKIN) | Cycle time, CLKIN | 6 | 83.3 | 6 | | ns | |
| 2 | tw(CLKINH) | Pulse duration, CLKIN high | 0.4C | | 0.4C | | ns | |
| 3 | tw(CLKINL) | Pulse duration, CLKIN low | 0.4C | | 0.4C | | ns | |
| 4 | t _t (CLKIN) | Transition time, CLKIN | | 5 | | 5 | ns | |

[†]The reference points for the rise and fall transitions are measured at V_{IL} MAX and V_{IH} MIN.

[§] See the PLL and PLL Controller section of this data sheet.

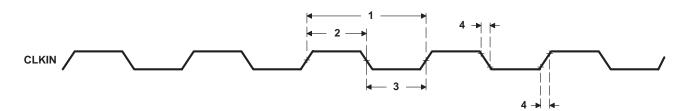


Figure 22. CLKIN Timings

 $[\]ddagger$ C = CLKIN cycle time in ns. For example, when CLKIN frequency is 25 MHz, use C = 40 ns.

 $^{^{\}ddagger}$ C = CLKIN cycle time in ns. For example, when CLKIN frequency is 25 MHz, use C = 40 ns.

INPUT AND OUTPUT CLOCKS (CONTINUED)

switching characteristics over recommended operating conditions for CLKOUT1^{†‡§} (see Figure 23) [C6712 only]

| 1 | | | | -100 |) | | |
|-----|-----------------------|------------------------------|-------------|--------------|----------|--------------|----|
| NO. | | PARAMETER | | CLKMODE = x4 | | CLKMODE = x1 | |
| | | | MIN | MAX | MIN | MAX | |
| 1 | t _C (CKO1) | Cycle time, CLKOUT1 | P - 0.7 | P + 0.7 | P - 0.7 | P + 0.7 | ns |
| 2 | tw(CKO1H) | Pulse duration, CLKOUT1 high | (P/2) - 0.7 | (P/2) + 0.7 | PH – 0.7 | PH + 0.7 | ns |
| 3 | tw(CKO1L) | Pulse duration, CLKOUT1 low | (P/2) - 0.7 | (P/2) + 0.7 | PL - 0.7 | PL + 0.7 | ns |
| 4 | t _t (CKO1) | Transition time, CLKOUT1 | | 0.6 | | 0.6 | ns |

The reference points for the rise and fall transitions are measured at VOL MAX and VOH MIN.

[§] P = 1/CPU clock frequency in nanoseconds (ns)

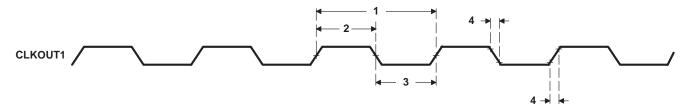


Figure 23. CLKOUT1 Timings [C6712 Only]

[‡] PH is the high period of CLKIN in ns and PL is the low period of CLKIN in ns.

INPUT AND OUTPUT CLOCKS (CONTINUED)

switching characteristics over recommended operating conditions for CLKOUT2^{†‡} (see Figure 24) [C6712]

| NO | | -10 | | | |
|-----|-----------|------------------------------|----------|----------|------|
| NO. | | PARAMETER | MIN | MIN MAX | UNIT |
| 1 | tc(CKO2) | Cycle time, CLKOUT2 | 2P - 0.7 | 2P + 0.7 | ns |
| 2 | tw(CKO2H) | Pulse duration, CLKOUT2 high | P – 0.7 | P + 0.7 | ns |
| 3 | tw(CKO2L) | Pulse duration, CLKOUT2 low | P – 0.7 | P + 0.7 | ns |
| 4 | tt(CKO2) | Transition time, CLKOUT2 | | 0.6 | ns |

[†]P = 1/CPU clock frequency in ns

switching characteristics over recommended operating conditions for CLKOUT2^{‡§} (see Figure 24) [C6712C/C6712D]

| No | | DADAMETED | -10 | | |
|-----|-----------------------|------------------------------|--------------|--------------|------|
| NO. | | PARAMETER | MIN | MAX | UNIT |
| 1 | tc(CKO2) | Cycle time, CLKOUT2 | C2 - 0.8 | C2 + 0.8 | ns |
| 2 | tw(CKO2H) | Pulse duration, CLKOUT2 high | (C2/2) - 0.8 | (C2/2) + 0.8 | ns |
| 3 | tw(CKO2L) | Pulse duration, CLKOUT2 low | (C2/2) - 0.8 | (C2/2) + 0.8 | ns |
| 4 | t _t (CKO2) | Transition time, CLKOUT2 | | 2 | ns |

 $[\]ddagger$ The reference points for the rise and fall transitions are measured at V_{OL} MAX and V_{OH} MIN.

[§] C2 = CLKOUT2 period in ns. CLKOUT2 period is determined by the PLL controller output SYSCLK2 period, which *must* be set to CPU period divide-by-2.

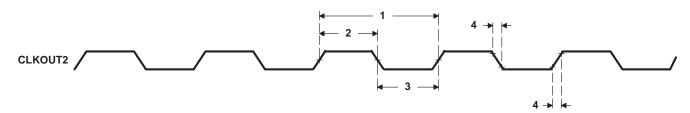


Figure 24. CLKOUT2 Timings

[‡] The reference points for the rise and fall transitions are measured at V_{OL} MAX and V_{OH} MIN.

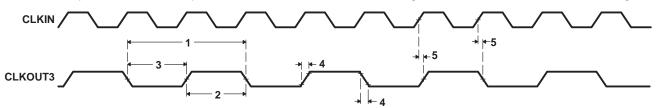
INPUT AND OUTPUT CLOCKS (CONTINUED)

switching characteristics over recommended operating conditions for CLKOUT3^{†‡} (see Figure 25) [C6712C/C6712D only]

| | PARAMETER | | 12C-167 | | 12D- | | |
|-----|-----------------------|---|--------------|--------------|--------------|--------------|------|
| NO. | | | MIN | MAX | MIN | MAX | UNIT |
| 1 | t _C (CKO3) | Cycle time, CLKOUT3 | C3 - 0.6 | C3 + 0.6 | C3 - 0.9 | C3 + 0.9 | ns |
| 2 | tw(CKO3H) | Pulse duration, CLKOUT3 high | (C3/2) - 0.6 | (C3/2) + 0.6 | (C3/2) - 0.9 | (C3/2) + 0.9 | ns |
| 3 | tw(CKO3L) | Pulse duration, CLKOUT3 low | (C3/2) - 0.6 | (C3/2) + 0.6 | (C3/2) - 0.9 | (C3/2) + 0.9 | ns |
| 4 | tt(CKO3) | Transition time, CLKOUT3 | | 2 | | 3 | ns |
| 5 | td(CLKINH-CKO3V) | Delay time, CLKIN high to CLKOUT3 valid | 1.5 | 6.5 | 1.5 | 7.5 | ns |

[†] The reference points for the rise and fall transitions are measured at V_{OL} MAX and V_{OH} MIN.

[‡]C3 = CLKOUT3 period in ns. CLKOUT3 period is a divide-down of the CPU clock, configurable via the RATIO field in the PLLDIV3 register.



NOTE A: For this example, the CLKOUT3 frequency is CLKIN divide-by-2.

Figure 25. CLKOUT3 Timings [C6712C/C6712D Only]

timing requirements for ECLKIN§ (see Figure 26)

| | | | -100 | | -167 | | |
|-----|----------------------|-----------------------------|------|-----|------|-----|------|
| NO. | | | | MAX | MIN | MAX | UNIT |
| 1 | t _C (EKI) | Cycle time, ECLKIN | 15 | | 10 | | ns |
| 2 | tw(EKIH) | Pulse duration, ECLKIN high | 6.8 | | 4.5 | | ns |
| 3 | tw(EKIL) | Pulse duration, ECLKIN low | 6.8 | | 4.5 | | ns |
| 4 | t _t (EKI) | Transition time, ECLKIN | | 3 | | 3 | ns |

[§] The reference points for the rise and fall transitions are measured at V_{IL} MAX and V_{IH} MIN.

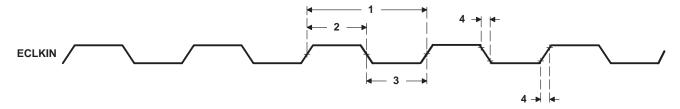


Figure 26. ECLKIN Timings

INPUT AND OUTPUT CLOCKS (CONTINUED)

switching characteristics over recommended operating conditions for ECLKOUT^{†‡§} (see Figure 27)

| NO. | DADAMETER | | -100 | | -1 | | |
|-----|----------------------------|---|----------|----------|----------|----------|------|
| | PARAMETER | | | MAX | MIN | MAX | UNIT |
| 1 | t _C (EKO) | Cycle time, ECLKOUT | E - 0.7 | E + 0.7 | E - 0.9 | E + 0.9 | ns |
| 2 | tw(EKOH) | Pulse duration, ECLKOUT high | EH – 0.7 | EH + 0.7 | EH - 0.9 | EH + 0.9 | ns |
| 3 | tw(EKOL) | Pulse duration, ECLKOUT low | EL - 0.7 | EL + 0.7 | EL - 0.9 | EL + 0.9 | ns |
| 4 | t _t (EKO) | Transition time, ECLKOUT | | 0.6 | | 2 | ns |
| 5 | t _d (EKIH-EKOH) | Delay time, ECLKIN high to ECLKOUT high | 1 | 7 | 1 | 6.5 | ns |
| 6 | td(EKIL-EKOL) | Delay time, ECLKIN low to ECLKOUT low | 1 | 7 | 1 | 6.5 | ns |

[†] The reference points for the rise and fall transitions are measured at VOL MAX and VOH MIN.

[§] EH is the high period of ECLKIN in ns and EL is the low period of ECLKIN in ns.

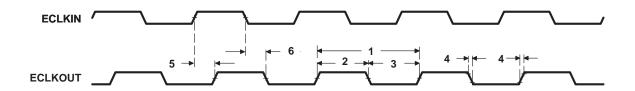


Figure 27. ECLKOUT Timings

[‡]E = ECLKIN period in ns

ASYNCHRONOUS MEMORY TIMING

timing requirements for asynchronous memory cycles^{†‡} (see Figure 28–Figure 29)

| NO | | | -100 | | -167 | | |
|-----|----------------|--|------|-----|------|-----|------|
| NO. | | | MIN | MAX | MIN | MAX | UNIT |
| 3 | tsu(EDV-AREH) | Setup time, EDx valid before ARE high | 13 | | 6.5 | | ns |
| 4 | th(AREH-EDV) | Hold time, EDx valid after ARE high | 1 | | 1 | | ns |
| 6 | tsu(ARDY-EKOH) | Setup time, ARDY valid before ECLKOUT high | 6 | | 3 | | ns |
| 7 | th(EKOH-ARDY) | Hold time, ARDY valid after ECLKOUT high | 1.7 | | 2.3 | | ns |

[†] To ensure data setup time, simply program the strobe width wide enough. ARDY is internally synchronized. The ARDY signal is recognized in the cycle for which the setup and hold time is met. To use ARDY as an asynchronous input, the pulse width of the ARDY signal should be wide enough (e.g., pulse width = 2E) to ensure setup and hold time is met.

switching characteristics over recommended operating conditions for asynchronous memory cyclesद (see Figure 28–Figure 29)

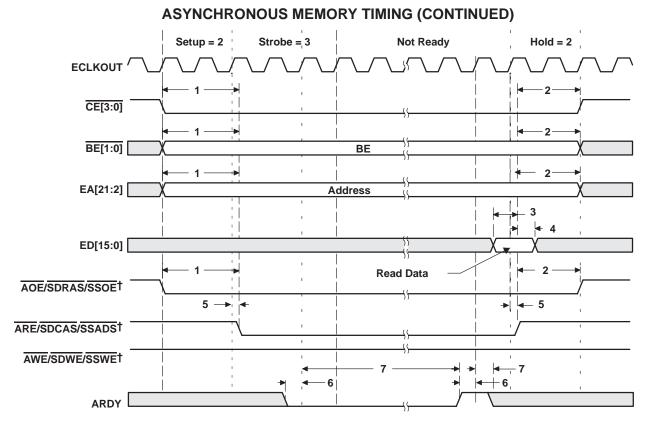
| NO | PARAMETER | | -100 | | -167 | | |
|-----|----------------------------|--|-------------------|-----|-------------------|------|----|
| NO. | | MIN | MAX | MIN | MAX | UNIT | |
| 1 | tosu(SELV-AREL) | Output setup time, select signals valid to ARE low | RS * E – 3 | | RS*E – 1.7 | | ns |
| 2 | toh(AREH-SELIV) | Output hold time, ARE high to select signals invalid | RH * E – 3 | | RH*E – 1.7 | | ns |
| 5 | t _d (EKOH-AREV) | Delay time, ECLKOUT high to ARE valid | 1.5 | 11 | 1.5 | 7 | ns |
| 8 | tosu(SELV-AWEL) | Output setup time, select signals valid to $\overline{\text{AWE}}$ low | WS * E - 3 | | WS*E – 1.7 | | ns |
| 9 | toh(AWEH-SELIV) | Output hold time, AWE high to select signals and EDx invalid | WH * E – 3 | | WH*E – 1.7 | | ns |
| 10 | t _d (EKOH-AWEV) | Delay time, ECLKOUT high to AWE valid | 1.5 | 11 | 1.5 | 7 | ns |
| 11 | tosu(EDV-AWEL) | Output setup time, ED valid to AWE low | (WS-1)*E - 1.7 | | (WS-1)*E - 1.7 | | ns |

RS = Read setup, RST = Read strobe, RH = Read hold, WS = Write setup, WST = Write strobe, WH = Write hold. These parameters are programmed via the EMIF CE space control registers.

[‡]RS = Read setup, RST = Read strobe, RH = Read hold, WS = Write setup, WST = Write strobe, WH = Write hold. These parameters are programmed via the EMIF CE space control registers.

[§] E = ECLKOUT period in ns

[¶] Select signals include: CE[3:0], BE[1:0], EA[21:2], and AOE.



[†] AOE/SDRAS/SSOE, ARE/SDCAS/SSADS, and AWE/SDWE/SSWE operate as AOE (identified under select signals), ARE, and AWE, respectively, during asynchronous memory accesses.

Figure 28. Asynchronous Memory Read Timing

ASYNCHRONOUS MEMORY TIMING (CONTINUED) Setup = 2 Strobe = 3 Hold = 2**Not Ready** ECLKOUT / CEx BE[3:0] BE 8 EA[21:2] Address **←** 11 | ED[31:0] Write Data AOE/SDRAS/SSOE† ARE/SDCAS/SSADS† **◆** 10 **◆**10 AWE/SDWE/SSWE† ARDY

Figure 29. Asynchronous Memory Write Timing



[†] AOE/SDRAS/SSOE, ARE/SDCAS/SSADS, and AWE/SDWE/SSWE operate as AOE (identified under select signals), ARE, and AWE, respectively, during asynchronous memory accesses.

SYNCHRONOUS-BURST MEMORY TIMING

timing requirements for synchronous-burst SRAM cycles[†] (see Figure 30)

| | | | -100 | | -167 | | |
|-----|----------------------------|--|------|-----|------|-----|------|
| NO. | | | MIN | MAX | MIN | MAX | UNIT |
| 6 | t _{su} (EDV-EKOH) | Setup time, read EDx valid before ECLKOUT high | 6 | | 1.5 | | ns |
| 7 | th(EKOH-EDV) | Hold time, read EDx valid after ECLKOUT high | 2.1‡ | | 2.5 | | ns |

[†] The C6712/12C/12D SBSRAM interface takes advantage of the internal burst counter in the SBSRAM. Accesses default to incrementing 4-word bursts, but random bursts and decrementing bursts are done by interrupting bursts in progress. All burst types can sustain continuous data flow. ‡ Make sure the external SBSRAM meets the timing specifications of the C6712 device. Delays or buffers may be needed to compensate for any timing differences. IBIS analysis should be used to correctly model the system interface.

switching characteristics over recommended operating conditions for synchronous-burst SRAM cycles^{†§} (see Figure 30 and Figure 31)

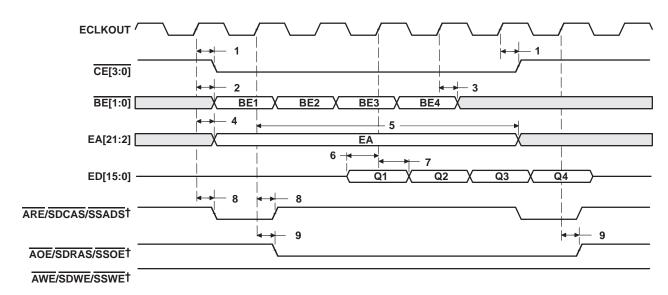
| | | | -10 | 00 | -167 | | LINUT |
|-----|---------------|---|-----|-----|------|-----|-------|
| NO. | | PARAMETER | MIN | MAX | MIN | MAX | UNIT |
| 1 | td(EKOH-CEV) | Delay time, ECLKOUT high to CEx valid | 1.5 | 11‡ | 1.2 | 7 | ns |
| 2 | td(EKOH-BEV) | Delay time, ECLKOUT high to BEx valid | | 11‡ | | 7 | ns |
| 3 | td(EKOH-BEIV) | Delay time, ECLKOUT high to BEx invalid | 1.5 | | 1.2 | | ns |
| 4 | td(EKOH-EAV) | Delay time, ECLKOUT high to EAx valid | | 11‡ | | 7 | ns |
| 5 | td(EKOH-EAIV) | Delay time, ECLKOUT high to EAx invalid | 1.5 | | 1.2 | | ns |
| 8 | td(EKOH-ADSV) | Delay time, ECLKOUT high to ARE/SDCAS/SSADS valid | 1.5 | 11‡ | 1.2 | 7 | ns |
| 9 | td(EKOH-OEV) | Delay time, ECLKOUT high to, AOE/SDRAS/SSOE valid | 1.5 | 11‡ | 1.2 | 7 | ns |
| 10 | td(EKOH-EDV) | Delay time, ECLKOUT high to EDx valid | | 11‡ | | 7 | ns |
| 11 | td(EKOH-EDIV) | Delay time, ECLKOUT high to EDx invalid | 1.5 | | 1.2 | | ns |
| 12 | td(EKOH-WEV) | Delay time, ECLKOUT high to AWE/SDWE/SSWE valid | 1.5 | 11‡ | 1.2 | 7 | ns |

[†] The C6712/12C/12D SBSRAM interface takes advantage of the internal burst counter in the SBSRAM. Accesses default to incrementing 4-word bursts, but random bursts and decrementing bursts are done by interrupting bursts in progress. All burst types can sustain continuous data flow. ‡ Make sure the external SBSRAM meets the timing specifications of the C6712 device. Delays or buffers may be needed to compensate for any timing differences. IBIS analysis should be used to correctly model the system interface.



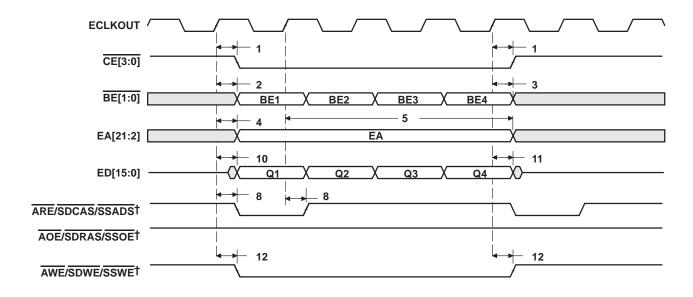
[§] ARE/SDCAS/SSADS, AOE/SDRAS/SSOE, and AWE/SDWE/SSWE operate as SSADS, SSOE, and SSWE, respectively, during SBSRAM accesses.

SYNCHRONOUS-BURST MEMORY TIMING (CONTINUED)



[†] ARE/SDCAS/SSADS, AOE/SDRAS/SSOE, and AWE/SDWE/SSWE operate as SSADS, SSOE, and SSWE, respectively, during SBSRAM accesses.

Figure 30. SBSRAM Read Timing



[†] ARE/SDCAS/SSADS, AOE/SDRAS/SSOE, and AWE/SDWE/SSWE operate as SSADS, SSOE, and SSWE, respectively, during SBSRAM accesses.

Figure 31. SBSRAM Write Timing



SYNCHRONOUS DRAM TIMING

timing requirements for synchronous DRAM cycles[†] (see Figure 32)

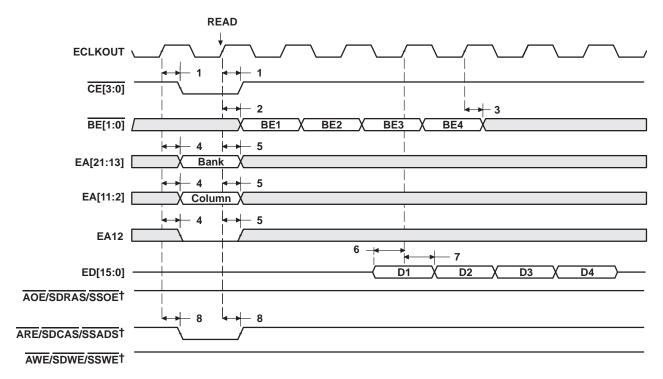
| NO | | | -10 | 00 | -10 | 67 | LINUT |
|-----|----------------------------|--|-----|-----|-----|-----|-------|
| NO. | | | MIN | MAX | MIN | MAX | UNIT |
| 6 | t _{su} (EDV-EKOH) | Setup time, read EDx valid before ECLKOUT high | 6 | | 1.5 | | ns |
| 7 | th(EKOH-EDV) | Hold time, read EDx valid after ECLKOUT high | 2.1 | | 2.5 | | ns |

[†] The C6712/12C/12D SDRAM interface takes advantage of the internal burst counter in the SDRAM. Accesses default to incrementing 4-word bursts, but random bursts and decrementing bursts are done by interrupting bursts in progress. All burst types can sustain continuous data flow.

switching characteristics over recommended operating conditions for synchronous DRAM cycles†‡ (see Figure 32–Figure 38)

| NO | | DADAMETED | -10 | 00 | -167 | | LINUT |
|-----|---------------|---|-----|-----|------|-----|-------|
| NO. | | PARAMETER | MIN | MAX | MIN | MAX | UNIT |
| 1 | td(EKOH-CEV) | Delay time, ECLKOUT high to CEx valid | 1.5 | 11 | 1.5 | 7 | ns |
| 2 | td(EKOH-BEV) | Delay time, ECLKOUT high to BEx valid | | 11 | | 7 | ns |
| 3 | td(EKOH-BEIV) | Delay time, ECLKOUT high to BEx invalid | 1.5 | | 1.5 | | ns |
| 4 | td(EKOH-EAV) | Delay time, ECLKOUT high to EAx valid | | 11 | | 7 | ns |
| 5 | td(EKOH-EAIV) | Delay time, ECLKOUT high to EAx invalid | 1.5 | | 1.5 | | ns |
| 8 | td(EKOH-CASV) | Delay time, ECLKOUT high to ARE/SDCAS/SSADS valid | 1.5 | 11 | 1.5 | 7 | ns |
| 9 | td(EKOH-EDV) | Delay time, ECLKOUT high to EDx valid | | 11 | | 7 | ns |
| 10 | td(EKOH-EDIV) | Delay time, ECLKOUT high to EDx invalid | 1.5 | | 1.5 | | ns |
| 11 | td(EKOH-WEV) | Delay time, ECLKOUT high to AWE/SDWE/SSWE valid | 1.5 | 11 | 1.5 | 7 | ns |
| 12 | td(EKOH-RAS) | Delay time, ECLKOUT high to, AOE/SDRAS/SSOE valid | 1.5 | 11 | 1.5 | 7 | ns |

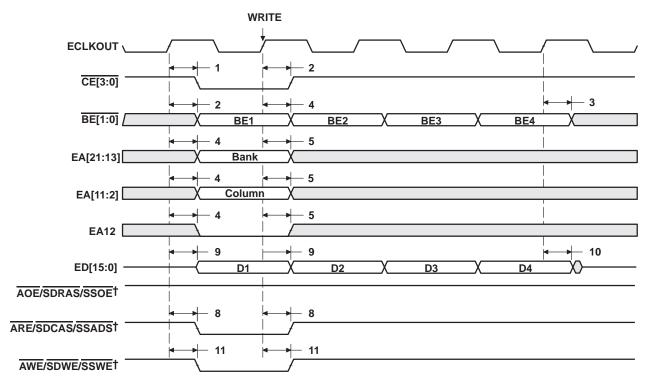
[†] The C6712/12C/12D SDRAM interface takes advantage of the internal burst counter in the SDRAM. Accesses default to incrementing 4-word bursts, but random bursts and decrementing bursts are done by interrupting bursts in progress. All burst types can sustain continuous data flow. ‡ ARE/SDCAS/SSADS, AWE/SDWE/SSWE, and AOE/SDRAS/SSOE operate as SDCAS, SDWE, and SDRAS, respectively, during SDRAM accesses.



[†] ARE/SDCAS/SSADS, AWE/SDWE/SSWE, and AOE/SDRAS/SSOE operate as SDCAS, SDWE, and SDRAS, respectively, during SDRAM accesses.

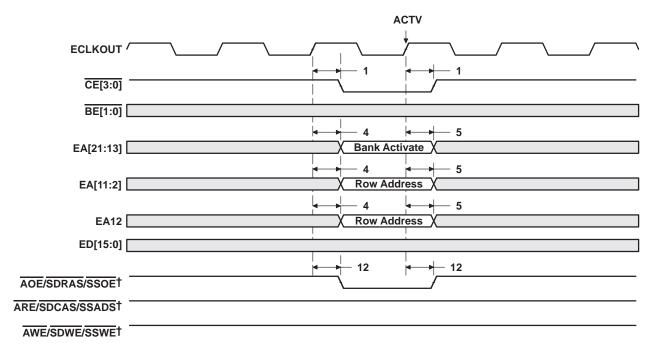
Figure 32. SDRAM Read Command (CAS Latency 3)





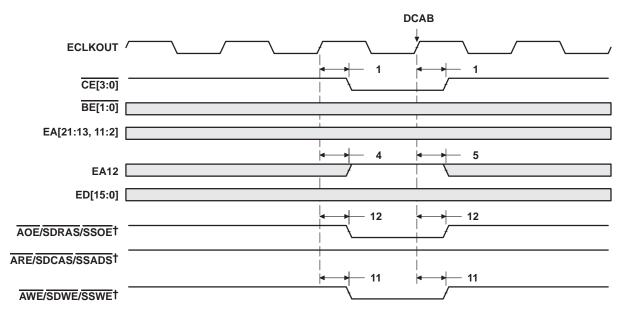
[†] ARE/SDCAS/SSADS, AWE/SDWE/SSWE, and AOE/SDRAS/SSOE operate as SDCAS, SDWE, and SDRAS, respectively, during SDRAM accesses.

Figure 33. SDRAM Write Command



[†] ARE/SDCAS/SSADS, AWE/SDWE/SSWE, and AOE/SDRAS/SSOE operate as SDCAS, SDWE, and SDRAS, respectively, during SDRAM accesses.

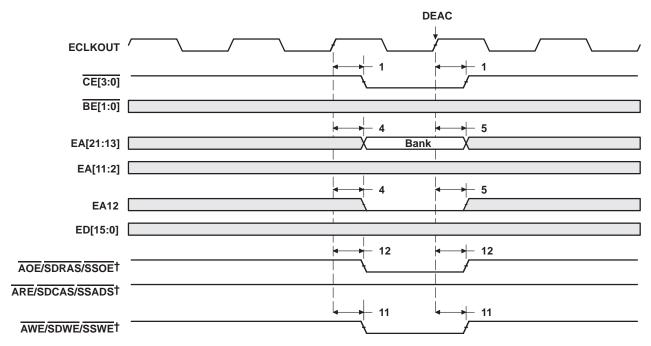
Figure 34. SDRAM ACTV Command



[†] ARE/SDCAS/SSADS, AWE/SDWE/SSWE, and AOE/SDRAS/SSOE operate as SDCAS, SDWE, and SDRAS, respectively, during SDRAM accesses.

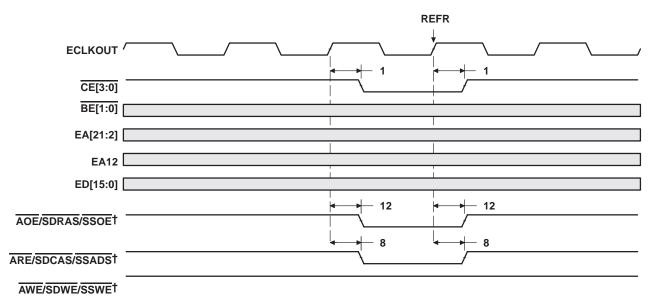
Figure 35. SDRAM DCAB Command





[†] ARE/SDCAS/SSADS, AWE/SDWE/SSWE, and AOE/SDRAS/SSOE operate as SDCAS, SDWE, and SDRAS, respectively, during SDRAM accesses.

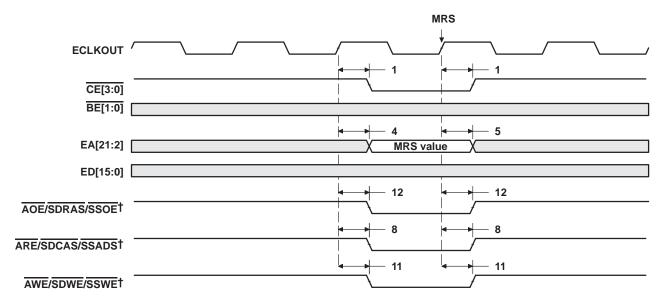
Figure 36. SDRAM DEAC Command



[†] ARE/SDCAS/SSADS, AWE/SDWE/SSWE, and AOE/SDRAS/SSOE operate as SDCAS, SDWE, and SDRAS, respectively, during SDRAM accesses.

Figure 37. SDRAM REFR Command





[†] ARE/SDCAS/SSADS, AWE/SDWE/SSWE, and AOE/SDRAS/SSOE operate as SDCAS, SDWE, and SDRAS, respectively, during SDRAM accesses.

Figure 38. SDRAM MRS Command



HOLD/HOLDA TIMING

timing requirements for the HOLD/HOLDA cycles[†] (see Figure 39)

| NO. | | -10 -10 | | UNIT |
|-----|--|------------|-----|------|
| | | MIN | MAX | |
| 3 | th(HOLDAL-HOLDL) Hold time, HOLD low after HOLDA low | Е | | ns |

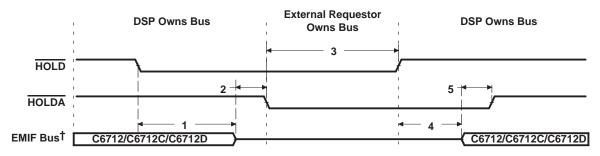
[†]E = ECLKIN period in ns

switching characteristics over recommended operating conditions for the HOLD/HOLDA cycles†‡ (see Figure 39)

| NO. | PARAMETER | | -100 -167 | | 12D- | UNIT | |
|-----|-----------------|--|--------------|-----|------|------|----|
| | | | | MAX | MIN | MAX | |
| 1 | td(HOLDL-EMHZ) | Delay time, HOLD low to EMIF Bus high impedance | 2E | § | 2E | § | ns |
| 2 | td(EMHZ-HOLDAL) | Delay time, EMIF Bus high impedance to HOLDA low | -0.1 | 2E | 0 | 2E | ns |
| 4 | td(HOLDH-EMLZ) | Delay time, HOLD high to EMIF Bus low impedance | 2E | 7E | 2E | 7E | ns |
| 5 | td(EMLZ-HOLDAH) | Delay time, EMIF Bus low impedance to HOLDA high | -1.5 | 2E | 0 | 2E | ns |

[†]E = ECLKIN period in ns

[§] All pending EMIF transactions are allowed to complete before HOLDA is asserted. If no bus transactions are occurring, then the minimum delay time can be achieved. Also, bus hold can be indefinitely delayed by setting NOHOLD = 1.



† EMIF Bus consists of CE[3:0], BE[1:0], ED[15:0], EA[21:2], ARE/SDCAS/SSADS, AOE/SDRAS/SSOE, and AWE/SDWE/SSWE.

Figure 39. HOLD/HOLDA Timing

[‡] EMIF Bus consists of CE[3:0], BE[1:0], ED[15:0], EA[21:2], ARE/SDCAS/SSADS, AOE/SDRAS/SSOE, and AWE/SDWE/SSWE.

BUSREQ TIMING

switching characteristics over recommended operating conditions for the BUSREQ cycles (see Figure 40)

| NO. | PARAMETER | | -100 | | -167 | | | |
|-----|-----------|----------------|--|-----|------|------|-----|----|
| | PARAMETER | MIN | MAX | MIN | MAX | UNIT | | |
| | 1 | td(EKOH-BUSRV) | Delay time, ECLKOUT high to BUSREQ valid | 2 | 10 | 1.5 | 7.2 | ns |

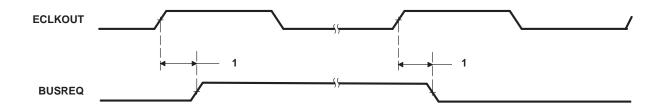


Figure 40. BUSREQ Timing

RESET TIMING [C6712]

timing requirements for reset[†] (see Figure 41)

| NO | | -10 | | | |
|-----|-----------------------|--|-----|--|------|
| NO. | | | | | UNIT |
| | | Width of the RESET pulse (PLL stable)‡ | 10P | | ns |
| 1 | ^t w(RST) | Width of the RESET pulse (PLL needs to sync up)§ | 250 | | μs |
| 14 | t _{su(BOOT)} | Setup time, BOOTMODE[1:0] configuration bits valid before RESET high | 2P | | ns |
| 15 | th(BOOT) | Hold time, BOOTMODE[1:0] configuration bits valid after RESET high | 2P | | ns |

 $[\]dagger P = 1/CPU$ clock frequency in ns. For example, when running parts at 100 MHz, use P = 10 ns.

switching characteristics over recommended operating conditions during reset^{†¶#} (see Figure 41)

| | | D. D. M. ETT. D. | -10 | 0 | |
|-----|--------------------------|--|---------|---------|------|
| NO. | | PARAMETER | MIN | MAX | UNIT |
| 2 | td(RSTL-ECKI) | Delay time, RESET low to ECLKIN synchronized internally | 2P + 3E | 3P + 4E | ns |
| 3 | td(RSTH-ECKI) | Delay time, RESET high to ECLKIN synchronized internally | 2P + 3E | 3P + 4E | ns |
| 4 | td(RSTL-EMIFZHZ) | Delay time, RESET low to EMIF Z group high impedance | 2P + 3E | | ns |
| 5 | td(RSTH-EMIFZV) | Delay time, RESET high to EMIF Z group valid | | 3P + 4E | ns |
| 6 | td(RSTL-EMIFHIV) | Delay time, RESET low to EMIF high group invalid | 2P + 3E | | ns |
| 7 | td(RSTH-EMIFHV) | Delay time, RESET high to EMIF high group valid | | 3P + 4E | ns |
| 8 | td(RSTL-EMIFLIV) | Delay time, RESET low to EMIF low group invalid | 2P + 3E | | ns |
| 9 | td(RSTH-EMIFLV) | Delay time, RESET high to EMIF low group valid | | 3P + 4E | ns |
| 12 | td(RSTL-ZHZ) | Delay time, RESET low to Z group high impedance | 2P | | ns |
| 13 | t _d (RSTH-ZV) | Delay time, RESET high to Z group valid | 2P | | ns |

 $^{^{\}dagger}P$ = 1/CPU clock frequency in ns. For example, when running parts at 100 MHz, use P = 10 ns.

EMIF high group consists of: HOLDA EMIF low group consists of: BUSREQ

Z group consists of: CLKX0, CLKX1, FSX0, FSX1, DX0, DX1, CLKR0, CLKR1, FSR0, FSR1, TOUT0, and TOUT1.



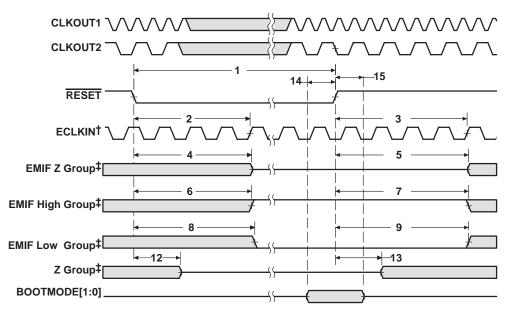
[‡] This parameter applies to CLKMODE x1 when CLKIN is stable, and applies to CLKMODE x4 when CLKIN and PLL are stable.

[§] This parameter applies to CLKMODE x4 only (it does not apply to CLKMODE x1). The RESET signal is not connected internally to the clock PLL circuit. The PLL, however, may need up to 250 µs to stabilize following device power up or after PLL configuration has been changed. During that time, RESET must be asserted to ensure proper device operation. See the clock PLL section for PLL lock times.

 $[\]P$ E = ECLKIN period in ns

[#] EMIF Z group consists of: EA[21:2], ED[15:0], CE[3:0], BE[1:0], ARE/SDCAS/SSADS, AWE/SDWE/SSWE, and AOE/SDRAS/SSOE

RESET TIMING [C6712] (CONTINUED)



† ECLKIN should be provided during reset in order to drive EMIF signals to the correct reset values. ECLKOUT continues to clock as long as ECLKIN is provided.

‡ EMIF Z group consists of: EA[21:2], ED[15:0], CE[3:0], BE[1:0], ARE/SDCAS/SSADS, AWE/SDWE/SSWE, and AOE/SDRAS/SSOE

EMIF high group consists of: HOLDA
EMIF low group consists of: BUSREQ

Z group consists of: CLKX0, CLKX1, FSX0, FSX1, DX0, DX1, CLKR0, CLKR1, FSR0, FSR1, TOUT0, and TOUT1.

Figure 41. Reset Timing [C6712]

RESET TIMING [C6712C/C6712D]

timing requirements for reset^{†‡} (see Figure 42)

| NO | | | -16 | 67 | LINUT |
|-----|-----------------------|--|-----|-----|-------|
| NO. | | | MIN | MAX | UNIT |
| 1 | tw(RST) | Pulse duration, RESET | 100 | | ns |
| 12 | t _{su(BOOT)} | Setup time, boot configuration bits valid before RESET high§ | 2P | | ns |
| 13 | th(BOOT) | Hold time, boot configuration bits valid after RESET high§ | 2P | | ns |

 $[\]dagger$ P = 1/CPU clock frequency in ns. For example, when running parts at 167 MHz, use P = 6 ns.

switching characteristics over recommended operating conditions during reset¶ (see Figure 42)

| | | DADAMETER | | | -167 | |
|-----|----------------------------|---|--------------|-----|-----------------------|------|
| NO. | | PARAMETER | | MIN | MAX | UNIT |
| 2 | ^t d(RSTH-ZV) | Delay time, external RESET high to internal reset high and all signal groups valid# | CLKMODE0 = 1 | | 512 x CLKIN period | ns |
| 3a | td(RSTL-ECKOL) | Delay time, RESET low to ECLKOUT low (6712C) | | 0 | | ns |
| 3b | td(RSTL-ECKOL) | Delay time, RESET low to ECLKOUT high impedance | e (6712D) | 0 | | ns |
| 4 | td(RSTH-ECKOV) | Delay time, RESET high to ECLKOUT valid | | | 6P | ns |
| 5a | td(RSTL-CKO2IV) | Delay time, RESET low to CLKOUT2 invalid (6712C) | | 0 | | ns |
| 5b | td(RSTL-CKO2IV) | Delay time, RESET low to CLKOUT2 high impedance | (6712D) | 0 | | ns |
| 6 | td(RSTH-CKO2V) | Delay time, RESET high to CLKOUT2 valid | | | 6P | ns |
| 7 | td(RSTL-CKO3L) | Delay time, RESET low to CLKOUT3 low | | 0 | | ns |
| 8 | td(RSTH-CKO3V) | Delay time, RESET high to CLKOUT3 valid | | | 6P | ns |
| 9 | td(RSTL-EMIFZHZ) | Delay time, RESET low to EMIF Z group high impeda | ncell | 0 | | ns |
| 10 | td(RSTL-EMIFLIV) | Delay time, RESET low to EMIF low group (BUSREQ |) invalid | 0 | | ns |
| 11 | t _d (RSTL-Z1HZ) | Delay time, RESET low to Z group high impedance | | 0 | | ns |

 $[\]P$ P = 1/CPU clock frequency in ns.

Note that while internal reset is asserted low, the CPU clock (SYSCLK1) period is equal to the input clock (CLKIN) period multiplied by 8. For example, if the CLKIN period is 20 ns, then the CPU clock (SYSCLK1) period is 20 ns x 8 = 160 ns. Therefore, P = SYSCLK1 = 160 ns while internal reset is asserted.

EMIF low group consists of: BUSREQ

Z group consists of: CLKR0, CLKR1, CLKX0, CLKX1, FSR0, FSR1, FSX0, FSX1, DX0, DX1, TOUT0, and TOUT1.

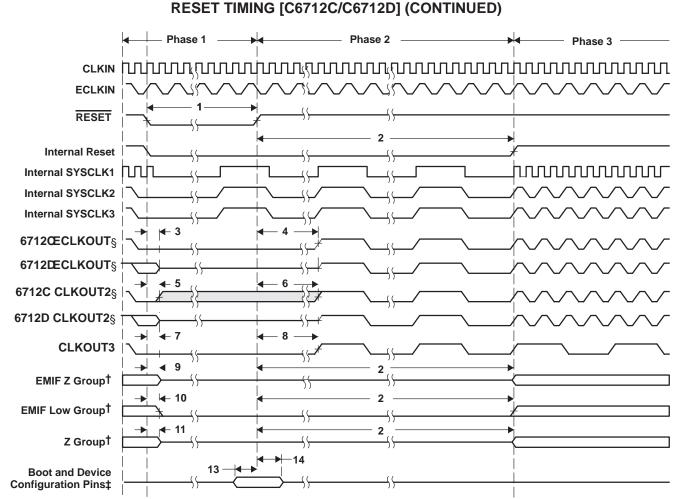


[‡] For the C6712C/12D device, the PLL is bypassed immediately after the device comes out of reset. The PLL Controller can be programmed to change the PLL mode in software. For more detailed information on the PLL Controller, see the *TMS320C6000 DSP Software-Programmable Phase-Lock Loop (PLL) Controller Reference Guide* (literature number SPRU233).

[§] The Boot and device configurations bits are latched asynchronously when RESET is transitioning high. The Boot and device configurations bits consist of: BOOTMODE[1:0] and LENDIAN.

[#] The internal reset is stretched exactly 512 x CLKIN cycles if CLKIN is used (CLKMODE0 = 1). If the input clock (CLKIN) is not stable when RESET is deasserted, the actual delay time may vary.

^{||} EMIF Z group consists of: EA[21:2], ED[15:0], \(\overline{CE}[3:0] \), \(\overline{BE}[1:0] \), \(\overline{ARE/SDCAS/SSADS} \), \(\overline{AWE/SDWE/SSWE} \), \(\overline{AOE/SDRAS/SSOE} \) and \(\ove



† EMIF Z group consists of: EA[21:2], ED[15:0], CE[3:0], BE[1:0], ARE/SDCAS/SSADS, AWE/SDWE/SSWE, AOE/SDRAS/SSOE and HOLDA

EMIF low group consists of: BUSREQ

Z group consists of: CLKR0, CLKR1, CLKX0, CLKX1, FSR0, FSR1, FSX0, FSX1, DX0, DX1, TOUT0, and TOUT1.

Figure 42. Reset Timing [C6712C/12D]

Reset Phase 1: The RESET pin is asserted. During this time, all internal clocks are running at the CLKIN frequency divide-by-8. The CPU is also running at the CLKIN frequency divide-by-8.

Reset Phase 2: The RESET pin is deasserted but the internal reset is stretched. During this time, all internal clocks are running at the CLKIN frequency divide-by-8. The CPU is also running at the CLKIN frequency divide-by-8.

Reset Phase 3: Both the RESET pin and internal reset are deasserted. During this time, all internal clocks are running at their default divide-down frequency of CLKIN. The CPU clock (SYSCLK1) is running at CLKIN frequency. The peripheral clock (SYSCLK2) is running at CLKIN frequency divide-by-2. The EMIF internal clock source (SYSCLK3) is running at CLKIN frequency divide-by-2. SYSCLK3 is reflected on the ECLKOUT pin (when EKSRC bit = 0 [default]). CLKOUT3 is running at CLKIN frequency divide-by-8.



[‡] Boot and device configurations consist of: BOOTMODE[1:0] and LENDIAN.

EXTERNAL INTERRUPT TIMING

timing requirements for external interrupts[†] (see Figure 43)

| NO | | | | 00 | -167 | | |
|-----|----------------------|---|-----|-----|------|-----|------|
| NO. | | | MIN | MAX | MIN | MAX | UNIT |
| | ^t w(ILOW) | Width of the NMI interrupt pulse low | 2P | | 2P | | ns |
| 1 | | Width of the EXT_INT interrupt pulse low | 2P | | 4P | | ns |
| 2 | tw(IHIGH) | Width of the NMI interrupt pulse high | 2P | | 2P | | ns |
| 2 | | Width of the EXT_INT interrupt pulse high | 2P | | 4P | | ns |

 $[\]dagger$ P = 1/CPU clock frequency in ns. For example, when running parts at 100 MHz, use P = 10 ns.



Figure 43. External/NMI Interrupt Timing

SM320C6712-EP, SM320C6712C-EP, SM320C6712D-EP FLOATING-POINT DIGITAL SIGNAL PROCESSORS

SGUS055 - SEPTEMBER 2004

MULTICHANNEL BUFFERED SERIAL PORT TIMING

timing requirements for McBSP^{†‡} (see Figure 44) [C6712]

| | | | | -100 | | |
|-----|---------------------------|---|------------|-----------------------------|-----|------|
| NO. | | | | MIN | MAX | UNIT |
| 2 | t _c (CKRX) | Cycle time, CLKR/X | CLKR/X ext | 2P§ | | ns |
| 3 | tw(CKRX) | Pulse duration, CLKR/X high or CLKR/X low | CLKR/X ext | 0.5t _{c(CKRX)} - 1 | | ns |
| _ | ^t su(FRH-CKRL) | Cotinations systematic ECD high hefers CLVD law | CLKR int | 20 | | |
| 5 | | Setup time, external FSR high before CLKR low | CLKR ext | 1 | | ns |
| _ | ^t h(CKRL-FRH) | 11117 | | 6 | | |
| 6 | | Hold time, external FSR high after CLKR low | CLKR ext | 3 | | ns |
| _ | | 0 | CLKR int | 22 | | |
| 7 | tsu(DRV-CKRL) | Setup time, DR valid before CLKR low | CLKR ext | 3 | | ns |
| _ | | | CLKR int | 3 | | |
| 8 | th(CKRL-DRV) | Hold time, DR valid after CLKR low | CLKR ext | 4 | | ns |
| | | | CLKX int | 23 | | |
| 10 | tsu(FXH-CKXL) | Setup time, external FSX high before CLKX low | CLKX ext | 1 | | ns |
| 4.4 | | | CLKX int | 6 | | |
| 11 | th(CKXL-FXH) | Hold time, external FSX high after CLKX low | CLKX ext | 3 | | ns |

[†] CLKRP = CLKXP = FSRP = FSXP = 0. If polarity of any of the signals is inverted, then the timing references of that signal are also inverted. ‡ P = 1/CPU clock frequency in ns. For example, when running parts at 100 MHz, use P = 10 ns.

[§] The minimum CLKR/X period is twice the CPU cycle time (2P). This means that the maximum bit rate for communications between the McBSP and other device is 50 Mbps for 100 MHz CPU clock; where the McBSP is either the master or the slave. Care must be taken to ensure that the AC timings specified in this data sheet are met. The maximum bit rate for McBSP-to-McBSP communications is 33 Mbps; therefore, the minimum CLKR/X clock cycle is either twice the CPU cycle time (2P), or 30 ns (33 MHz), whichever value is larger. For example, when running parts at 100 MHz (P = 10 ns), use 30 ns as the minimum CLKR/X clock cycle (by setting the appropriate CLKGDV ratio or external clock source). The maximum bit rate for McBSP-to-McBSP communications applies when the serial port is a master of the clock and frame syncs (with CLKR connected to CLKX, FSR connected to FSX, CLKXM = FSXM = 1, and CLKRM = FSRM = 0) in data delay 1 or 2 mode (R/XDATDLY = 01b or 10b) and the other device the McBSP communicates to is a slave.

SM320C6712-EP, SM320C6712C-EP, SM320C6712D-EP FLOATING-POINT DIGITAL SIGNAL PROCESSORS

SGUS055 - SEPTEMBER 2004

MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

timing requirements for McBSP^{†‡} (see Figure 44) [C6712C/C6712D]

| | | | | -167 | | |
|-----|----------------------------|---|------------|------------------------------|-----|------|
| NO. | | | | MIN | MAX | UNIT |
| 2 | t _C (CKRX) | Cycle time, CLKR/X | CLKR/X ext | 2P§ | | ns |
| 3 | tw(CKRX) | Pulse duration, CLKR/X high or CLKR/X low | CLKR/X ext | 0.5*t _{c(CKRX)} -1¶ | | ns |
| _ | t _{su} (FRH-CKRL) | (RL) Setup time, external FSR high before CLKR low | CLKR int | 9 | | |
| 5 t | | | CLKR ext | 1 | | ns |
| | th(CKRL-FRH) | Hald Consequent FOR Early of the OLVER Law | | 6 | | |
| 6 | | Hold time, external FSR high after CLKR low | CLKR ext | 3 | | ns |
| 7 | t _{su(DRV-CKRL)} | RV-CKRL) Setup time, DR valid before CLKR low | CLKR int | 8 | | |
| 7 | | | CLKR ext | 0 | | ns |
| | 4 | Hold fire a DD valid offer CLVD law | CLKR int | 3 | | |
| 8 | th(CKRL-DRV) | Hold time, DR valid after CLKR low | CLKR ext | 4 | | ns |
| 40 | | Outer time and soul FOV high hadon OLKV have | CLKX int | 9 | | |
| 10 | tsu(FXH-CKXL) | Setup time, external FSX high before CLKX low | CLKX ext | 1 | | ns |
| 44 | | ・レン・ EVL) Hold time, external FSX high after CLKX low | CLKX int | 6 | | |
| 11 | h(CKXL-FXH) | | CLKX ext | 3 | | ns |

[†] CLKRP = CLKXP = FSRP = FSXP = 0. If polarity of any of the signals is inverted, then the timing references of that signal are also inverted.

 $[\]ddagger$ P = 1/CPU clock frequency in ns. For example, when running parts at 167 MHz, use P = 6 ns.

[§] The minimum CLKR/X period is twice the CPU cycle time (2P) and not faster than 75 Mbps (13.3 ns). This means that the maximum bit rate for communications between the McBSP and other device is 75 Mbps for 150 MHz CPU clock; where the McBSP is either the master or the slave. Care must be taken to ensure that the AC timings specified in this data sheet are met. The maximum bit rate for McBSP-to-McBSP communications is 67 Mbps; therefore, the minimum CLKR/X clock cycle is either twice the CPU cycle time (2P), or 15 ns (67 MHz), whichever value is larger. For example, when running parts at 150 MHz (P = 6.7 ns), use 15 ns as the minimum CLKR/X clock cycle (by setting the appropriate CLKGDV ratio or external clock source). When running parts at 60 MHz (P = 16.67 ns), use 2P = 33 ns (30 MHz) as the minimum CLKR/X clock cycle. The maximum bit rate for McBSP-to-McBSP communications applies when the serial port is a master of the clock and frame syncs (with CLKR connected to CLKX, FSR connected to FSX, CLKXM = FSXM = 1, and CLKRM = FSRM = 0) in data delay 1 or 2 mode (R/XDATDLY = 01b or 10b) and the other device the McBSP communicates to is a slave.

This parameter applies to the maximum McBSP frequency. Operate serial clocks (CLKR/X) in the reasonable range of 40/60 duty cycle.

MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

switching characteristics over recommended operating conditions for McBSP^{†‡} (see Figure 44) [C6712]

| | | -1 | 00 | | | |
|-----|-----------------------------|---|------------------|--------------------|--------------------|------|
| NO. | | PARAMETER | | | | UNIT |
| 1 | td(CKSH-CKRXH) | Delay time, CLKS high to CLKR/X high for internal CLKR/X CLKS input | K generated from | 4 | 26 | ns |
| 2 | t _C (CKRX) | Cycle time, CLKR/X | CLKR/X int | 2P§¶ | | ns |
| 3 | tw(CKRX) | Pulse duration, CLKR/X high or CLKR/X low | CLKR/X int | C – 1 [#] | C + 1 [#] | ns |
| 4 | td(CKRH-FRV) | Delay time, CLKR high to internal FSR valid | CLKR int | -11 | 3 | ns |
| | | Delay time CLIVV high to internal FCV yelid | CLKX int | -11 | 3 | |
| 9 | ^t d(CKXH-FXV) | Delay time, CLKX high to internal FSX valid | CLKX ext | 3 | 9 | ns |
| 40 | | Disable time, DX high impedance following last data bit | CLKX int | -9 | 4 | |
| 12 | ^t dis(CKXH-DXHZ) | from CLKX high | CLKX ext | 3 | 9 | ns |
| 40 | | Delegation Old Whitehas DV and M | CLKX int | -9+ D1 | 7 + D2 | |
| 13 | ^t d(CKXH-DXV) | Delay time, CLKX high to DX valid | CLKX ext | 3 + D1 | 19 + D2 | ns |
| | | Delay time, FSX high to DX valid | FSX int | -1 | 3 | |
| 14 | td(FXH-DXV) | ONLY applies when in data delay 0 (XDATDLY = 00b) mode | FSX ext | 3 | 9 | ns |

[†] CLKRP = CLKXP = FSRP = FSXP = 0. If polarity of any of the signals is inverted, then the timing references of that signal are also inverted.

 $^{\#}C = HorL$

S = sample rate generator input clock = 2P if CLKSM = 1 (P = 1/CPU clock frequency)

= sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)

H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even

= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero

L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even

= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero

CLKGDV should be set appropriately to ensure the McBSP bit rate does not exceed the maximum limit (see ¶ footnote above).

Extra delay from CLKX high to DX valid applies only to the first data bit of a device, if and only if DXENA = 1 in SPCR.

If DXENA = 0, then D1 = D2 = 0

If DXENA = 1, then D1 = 2P, D2 = 4P



[‡] Minimum delay times also represent minimum output hold times.

[§] P = 1/CPU clock frequency in ns. For example, when running parts at 100 MHz, use P = 10 ns.

The minimum CLKR/X period is twice the CPU cycle time (2P). This means that the maximum bit rate for communications between the McBSP and other device is 50 Mbps for 100 MHz CPU clock; where the McBSP is either the master or the slave. Care must be taken to ensure that the AC timings specified in this data sheet are met. The maximum bit rate for McBSP-to-McBSP communications is 33 Mbps; therefore, the minimum CLKR/X clock cycle is either twice the CPU cycle time (2P), or 30 ns (33 MHz), whichever value is larger. For example, when running parts at 100 MHz (P = 10 ns), use 30 ns as the minimum CLKR/X clock cycle (by setting the appropriate CLKGDV ratio or external clock source). The maximum bit rate for McBSP-to-McBSP communications applies when the serial port is a master of the clock and frame syncs (with CLKR connected to CLKX, FSR connected to FSX, CLKXM = FSXM = 1, and CLKRM = FSRM = 0) in data delay 1 or 2 mode (R/XDATDLY = 01b or 10b) and the other device the McBSP communicates to is a slave.

MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

switching characteristics over recommended operating conditions for McBSP^{†‡} (see Figure 44) [C6712C/C6712D]

| | | DADAMETED | | | 167 | 12D- | 167 | |
|-----|-----------------------------|---|------------|--------------------|--------------------|--------------------|--------------------|------|
| NO. | | PARAMETER | | MIN | MAX | MIN | MAX | UNIT |
| 1 | td(CKSH-CKRXH) | Delay time, CLKS high to CLKR/X hi CLKR/X generated from CLKS input | • | 1.8 | 10 | 1.8 | 10 | ns |
| 2 | t _C (CKRX) | Cycle time, CLKR/X | CLKR/X int | 2P§¶ | | 2P§¶ | | ns |
| 3 | tw(CKRX) | Pulse duration, CLKR/X high or CLKR/X low | CLKR/X int | C – 1 [#] | C + 1 [#] | C – 1 [#] | C + 1 [#] | ns |
| 4 | ^t d(CKRH-FRV) | Delay time, CLKR high to internal FSR valid | CLKR int | -2 | 3 | -2 | 3 | ns |
| 9 | | Delay time, CLKX high to internal | CLKX int | -2 | 3 | -2 | 3 | no |
| 9 | ^t d(CKXH-FXV) | FSX valid | CLKX ext | 2 | 9 | 2 | 9 | ns |
| 40 | | Disable time, DX high impedance | CLKX int | -1 | 4 | -1 | 4 | |
| 12 | ^t dis(CKXH-DXHZ) | following last data bit from CLKX high | CLKX ext | 1.5 | 10 | 1.5 | 10 | ns |
| 40 | | Balandar Olivitation By add | CLKX int | -3.2 + D1 | 4 + D2 | -3.2 + D1 | 4 + D2 | |
| 13 | td(CKXH-DXV) | Delay time, CLKX high to DX valid | CLKX ext | 0.5 + D1 | 10+ D2 | 0.5 + D1 | 10+ D2 | ns |
| | | Delay time, FSX high to DX valid | FSX int | -1.5 | 4.5 | -1 | 7.5 | |
| 14 | ^t d(FXH-DXV) | ONLY applies when in data delay 0 (XDATDLY = 00b) mode | FSX ext | 2 | 9 | 2 | 11.5 | ns |

[†] CLKRP = CLKXP = FSRP = FSXP = 0. If polarity of any of the signals is inverted, then the timing references of that signal are also inverted.

 $^{\#}C = H \text{ or } L$

S =sample rate generator input clock = 2P if CLKSM = 1 (P = 1/CPU clock frequency)

= sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)

H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even

= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero

L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even

= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero

CLKGDV should be set appropriately to ensure the McBSP bit rate does not exceed the maximum limit (see ¶ footnote above).

Extra delay from CLKX high to DX valid applies only to the first data bit of a device, if and only if DXENA = 1 in SPCR.

If DXENA = 0, then D1 = D2 = 0

If DXENA = 1, then D1 = 2P, D2 = 4P



[‡] Minimum delay times also represent minimum output hold times.

[§] P = 1/CPU clock frequency in ns. For example, when running parts at 167 MHz, use P = 6 ns.

The minimum CLKR/X period is twice the CPU cycle time (2P) and not faster than 75 Mbps (13.3 ns). This means that the maximum bit rate for communications between the McBSP and other device is 75 Mbps for 150 MHz CPU clock; where the McBSP is either the master or the slave. Care must be taken to ensure that the AC timings specified in this data sheet are met. The maximum bit rate for McBSP-to-McBSP communications is 67 Mbps; therefore, the minimum CLKR/X clock cycle is either twice the CPU cycle time (2P), or 15 ns (67 MHz), whichever value is larger. For example, when running parts at 150 MHz (P = 6.7 ns), use 15 ns as the minimum CLKR/X clock cycle (by setting the appropriate CLKGDV ratio or external clock source). When running parts at 60 MHz (P = 16.67 ns), use 2P = 33 ns (30 MHz) as the minimum CLKR/X clock cycle. The maximum bit rate for McBSP-to-McBSP communications applies when the serial port is a master of the clock and frame syncs (with CLKR connected to CLKX, FSR connected to FSX, CLKXM = FSXM = 1, and CLKRM = FSRM = 0) in data delay 1 or 2 mode (R/XDATDLY = 01b or 10b) and the other device the McBSP communicates to is a slave.

MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

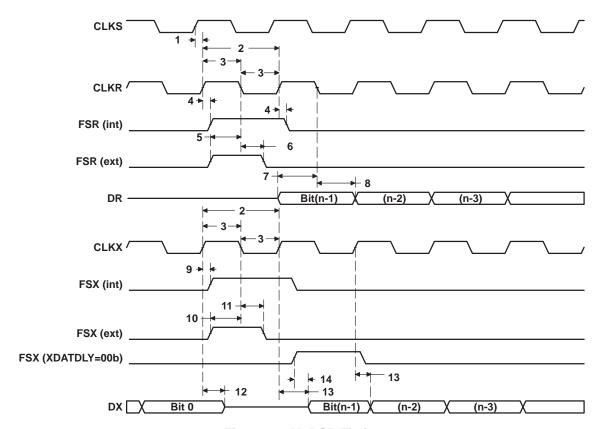


Figure 44. McBSP Timings

MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

timing requirements for FSR when GSYNC = 1 (see Figure 45)

| NO. | NO. | | 00 67 | UNIT |
|-----|---|-----|----------|------|
| | | MIN | MAX | |
| 1 | t _{su(FRH-CKSH)} Setup time, FSR high before CLKS high | 4 | | ns |
| 2 | t _{h(CKSH-FRH)} Hold time, FSR high after CLKS high | 4 | | ns |

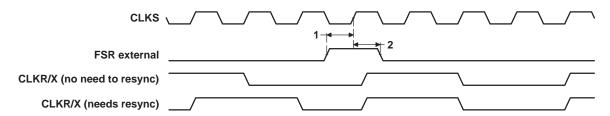


Figure 45. FSR Timing When GSYNC = 1

MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

timing requirements for McBSP as SPI master or slave: CLKSTP = 10b, CLKXP = $0^{+\frac{1}{4}}$ (see Figure 46) [C6712]

| | | | - | -100 | | |
|-----|--|-----|-----|---------|-----|------|
| NO. | | MAS | TER | SLA\ | /E | UNIT |
| | | MIN | MAX | MIN | MAX | |
| 4 | tsu(DRV-CKXL) Setup time, DR valid before CLKX low | 26 | | 2 – 6P | | ns |
| 5 | th(CKXL-DRV) Hold time, DR valid after CLKX low | 4 | | 6 + 12P | | ns |

 $^{^{\}dagger}$ P = 1/CPU clock frequency in ns. For example, when running parts at 100 MHz, use P = 10 ns.

timing requirements for McBSP as SPI master or slave: CLKSTP = 10b, CLKXP = $0^{\dagger \ddagger}$ (see Figure 46) [C6712C/C6712D]

| | | | - | -167 | | |
|-----|--|-----|-----|---------|-----|------|
| NO. | | MAS | TER | SLAV | E | UNIT |
| | | MIN | MAX | MIN | MAX | |
| 4 | tsu(DRV-CKXL) Setup time, DR valid before CLKX low | 12 | | 2 – 6P | | ns |
| 5 | th(CKXL-DRV) Hold time, DR valid after CLKX low | 4 | | 5 + 12P | | ns |

 $[\]dagger$ P = 1/CPU clock frequency in ns. For example, when running parts at 167 MHz, use P = 6 ns.

switching characteristics over recommended operating conditions for McBSP as SPI master or slave: CLKSTP = 10b, CLKXP = $0^{\dagger \ddagger}$ (see Figure 46) [C6712]

| | | | | | -100 | | | | | | |
|-----|--------------------------|---|-------|-------|--------|----------|----|--|--|--|--|
| NO. | PARAMETER | | | TER§ | SL | UNIT | | | | | |
| | | | MIN | MAX | MIN | MAX | | | | | |
| 1 | th(CKXL-FXL) | Hold time, FSX low after CLKX low¶ | T – 9 | T + 9 | | | ns | | | | |
| 2 | td(FXL-CKXH) | Delay time, FSX low to CLKX high# | L – 9 | L+9 | | | ns | | | | |
| 3 | td(CKXH-DXV) | Delay time, CLKX high to DX valid | -9 | 9 | 6P + 4 | 10P + 20 | ns | | | | |
| 6 | tdis(CKXL-DXHZ) | Disable time, DX high impedance following last data bit from CLKX low | L – 9 | L + 9 | | | ns | | | | |
| 7 | tdis(FXH-DXHZ) | Disable time, DX high impedance following last data bit from FSX high | | | 2P + 3 | 6P + 20 | ns | | | | |
| 8 | t _d (FXL-DXV) | Delay time, FSX low to DX valid | | | 4P + 2 | 8P + 20 | ns | | | | |

 $[\]dagger$ P = 1/CPU clock frequency in ns. For example, when running parts at 100 MHz, use P = 10 ns.

H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even

= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero

L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even

= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero

CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP

[#]FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).



[‡] For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

[‡] For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

[‡] For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

[§] S = Sample rate generator input clock = 2P if CLKSM = 1 (P = 1/CPU clock frequency)

⁼ Sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)

T = CLKX period = (1 + CLKGDV) * S

FSRP = FSXP = 1. As a SPI master, FSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on FSX and FSR is inverted before being used internally.

MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

switching characteristics over recommended operating conditions for McBSP as SPI master or slave: CLKSTP = 10b, CLKXP = 0^{+} (see Figure 46) [C6712C/C6712D]

| | | | | 1: | 2C-167 | | | 12 | 2D-167 | | |
|-----|-----------------------------|---|-------|---------|----------|----------|---------|-------|--------|----------|------|
| NO. | PA | PARAMETER | | MASTER§ | | AVE | MASTER§ | | SLA | AVE | UNIT |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| 1 | th(CKXL-FXL) | Hold time, FSX low after CLKX low¶ | T – 2 | T + 3 | | | T – 2 | T + 3 | | | ns |
| 2 | td(FXL-CKXH) | Delay time, FSX low to CLKX high# | L – 2 | L + 3 | | | L – 2 | L + 3 | | | ns |
| 3 | td(CKXH-DXV) | Delay time, CLKX high to DX valid | -3 | 4 | 6P + 2 | 10P + 17 | -3 | 4 | 6P + 2 | 10P + 17 | ns |
| 6 | ^t dis(CKXL-DXHZ) | Disable time, DX high impedance following last data bit from CLKX low | L – 4 | L+3 | | | L – 2 | L+3 | | | ns |
| 7 | tdis(FXH-DXHZ) | Disable time, DX high impedance following last data bit from FSX high | | | 2P + 1.5 | 6P + 17 | | | 2P + 3 | 6P + 17 | ns |
| 8 | td(FXL-DXV) | Delay time, FSX low to DX valid | | | 4P + 2 | 8P + 17 | | | 4P + 2 | 8P + 17 | ns |

 $^{^{\}dagger}$ P = 1/CPU clock frequency in ns. For example, when running parts at 167 MHz, use P = 6 ns.

H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even

= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero

L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even

= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero

CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP

[#]FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).

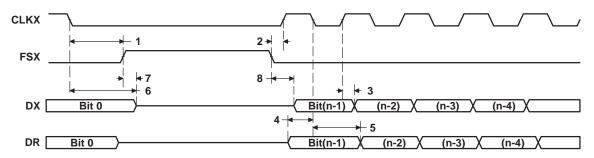


Figure 46. McBSP Timing as SPI Master or Slave: CLKSTP = 10b, CLKXP = 0

[‡] For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

[§] S = Sample rate generator input clock = 2P if CLKSM = 1 (P = 1/CPU clock frequency)

⁼ Sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)

T = CLKX period = (1 + CLKGDV) * S

[¶] FSRP = FSXP = 1. As a SPI master, FSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on FSX and FSR is inverted before being used internally.

SM320C6712-EP, SM320C6712C-EP, SM320C6712D-EP FLOATING-POINT DIGITAL SIGNAL PROCESSORS

SGUS055 - SEPTEMBER 2004

MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

timing requirements for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = $0^{+\pm}$ (see Figure 47) [C6712]

| | | | - | 100 | | |
|-----|---|-----|-----|---------|-----|------|
| NO. | | MAS | TER | SLA | /E | UNIT |
| | | MIN | MAX | MIN | MAX | |
| 4 | t _{SU(DRV-CKXH)} Setup time, DR valid before CLKX high | 26 | | 2 – 6P | | ns |
| 5 | th(CKXH-DRV) Hold time, DR valid after CLKX high | 4 | | 6 + 12P | | ns |

[†] P = 1/CPU clock frequency in ns. For example, when running parts at 100 MHz, use P = 10 ns.

timing requirements for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = $0^{\dagger \ddagger}$ (see Figure 47) [C6712C/C6712D]

| NO. | | MAS | TER | SLAV | /E | UNIT |
|-----|---|-----|-----|---------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| 4 | tsu(DRV-CKXH) Setup time, DR valid before CLKX high | 12 | | 2 – 6P | | ns |
| 5 | th(CKXH-DRV) Hold time, DR valid after CLKX high | 4 | | 5 + 12P | | ns |

 $[\]dagger P = 1/CPU$ clock frequency in ns. For example, when running parts at 167 MHz, use P = 6 ns.

switching characteristics over recommended operating conditions for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = 0^{+} (see Figure 47) [C6712]

| NO. | PARAMETER | | | ΓER§ | SL | UNIT | |
|-----|-----------------|---|-------|-------|--------|----------|----|
| | | | MIN | MAX | MIN | MAX | |
| 1 | th(CKXL-FXL) | Hold time, FSX low after CLKX low¶ | L – 9 | L + 9 | | | ns |
| 2 | td(FXL-CKXH) | Delay time, FSX low to CLKX high# | T – 9 | T + 9 | | | ns |
| 3 | td(CKXL-DXV) | Delay time, CLKX low to DX valid | -9 | 9 | 6P + 4 | 10P + 20 | ns |
| 6 | tdis(CKXL-DXHZ) | Disable time, DX high impedance following last data bit from CLKX low | -9 | 9 | 6P + 3 | 10P + 20 | ns |
| 7 | td(FXL-DXV) | Delay time, FSX low to DX valid | H – 9 | H + 9 | 4P + 2 | 8P + 20 | ns |

 $[\]dagger P = 1/CPU$ clock frequency in ns. For example, when running parts at 100 MHz, use P = 10 ns.

H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even

= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero

L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even

= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero

CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP



[‡] For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

[‡] For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

[‡] For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

[§] S = Sample rate generator input clock = 2P if CLKSM = 1 (P = 1/CPU clock frequency)

⁼ Sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)

T = CLKX period = (1 + CLKGDV) * S

[¶] FSRP = FSXP = 1. As a SPI master, FSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on FSX and FSR is inverted before being used internally.

[#]FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).

MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

switching characteristics over recommended operating conditions for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = 0^{+} (see Figure 47) [C6712C/C6712D]

| | | | | 1: | 2C-167 | | | 12 | D-167 | | |
|-----|-----------------------------|---|---------|-------|----------|----------|---------|---------|--------|----------|------|
| NO. | PARAMETER | | MASTER§ | | SLAVE | | MASTER§ | | SLAVE | | UNIT |
| | | | | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| 1 | th(CKXL-FXL) | Hold time, FSX low after CLKX low¶ | L – 2 | L + 3 | | | L – 2 | L + 3 | | | ns |
| 2 | ^t d(FXL-CKXH) | Delay time, FSX low to CLKX high# | T – 2 | T + 3 | | | T – 2 | T + 3 | | | ns |
| 3 | td(CKXL-DXV) | Delay time, CLKX low to DX valid | -3 | 4 | 6P + 2 | 10P + 17 | -3 | 4 | 6P + 2 | 10P + 17 | ns |
| 6 | ^t dis(CKXL-DXHZ) | Disable time, DX high impedance following last data bit from CLKX low | -4 | 4 | 6P + 1.5 | 10P + 17 | -2 | 4 | 6P + 3 | 10P + 17 | ns |
| 7 | t _d (FXL-DXV) | Delay time, FSX low to DX valid | H – 2 | H + 4 | 4P + 2 | 8P + 17 | H – 2 | H + 6.5 | 4P + 2 | 8P + 17 | ns |

 $[\]dagger$ P = 1/CPU clock frequency in ns. For example, when running parts at 167 MHz, use P = 6 ns.

H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even

= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero

L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even

= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero

[#]FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).

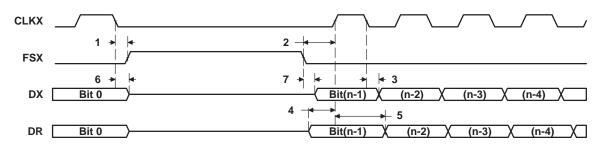


Figure 47. McBSP Timing as SPI Master or Slave: CLKSTP = 11b, CLKXP = 0

[‡] For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

[§]S = Sample rate generator input clock = 2P if CLKSM = 1 (P = 1/CPU clock frequency)

⁼ Sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)

T = CLKX period = (1 + CLKGDV) * S

FSRP = FSXP = 1. As a SPI master, FSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on FSX and FSR is inverted before being used internally.

CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP

CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP

MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

timing requirements for McBSP as SPI master or slave: CLKSTP = 10b, CLKXP = $1^{+\pm}$ (see Figure 48) [C6712]

| | | | - | 100 | | |
|-----|---|-----|-----|---------|-----|------|
| NO. | | MAS | TER | SLA | /E | UNIT |
| | | MIN | MAX | MIN | MAX | |
| 4 | t _{SU(DRV-CKXH)} Setup time, DR valid before CLKX high | 26 | | 2 – 6P | | ns |
| 5 | th(CKXH-DRV) Hold time, DR valid after CLKX high | 4 | | 6 + 12P | | ns |

[†] P = 1/CPU clock frequency in ns. For example, when running parts at 100 MHz, use P = 10 ns.

timing requirements for McBSP as SPI master or slave: CLKSTP = 10b, CLKXP = $1^{+\pm}$ (see Figure 48) [C6712C/C6712D]

| | | | - | -167 | | |
|-----|---|-----|-----|---------|-----|------|
| NO. | | MAS | TER | SLAV | /E | UNIT |
| | | MIN | MAX | MIN | MAX | |
| 4 | tsu(DRV-CKXH) Setup time, DR valid before CLKX high | 12 | | 2 – 6P | | ns |
| 5 | th(CKXH-DRV) Hold time, DR valid after CLKX high | 4 | | 5 + 12P | | ns |

 $[\]dagger P = 1/CPU$ clock frequency in ns. For example, when running parts at 167 MHz, use P = 6 ns.

switching characteristics over recommended operating conditions for McBSP as SPI master or slave: CLKSTP = 10b, CLKXP = 1^{+} (see Figure 48) [C6712]

| | | | | , | -100 | | |
|-----|----------------------------|--|-------|-------|--------|----------|------|
| NO. | | PARAMETER | MAS | ΓER§ | SL | AVE | UNIT |
| | | | MIN | MAX | MIN | MAX | |
| 1 | th(CKXH-FXL) | Hold time, FSX low after CLKX high¶ | T – 9 | T + 9 | | | ns |
| 2 | td(FXL-CKXL) | Delay time, FSX low to CLKX low# | H – 9 | H + 9 | | | ns |
| 3 | td(CKXL-DXV) | Delay time, CLKX low to DX valid | -9 | 9 | 6P + 4 | 10P + 20 | ns |
| 6 | tdis(CKXH-DXHZ) | Disable time, DX high impedance following last data bit from CLKX high | H – 9 | H + 9 | | | ns |
| 7 | ^t dis(FXH-DXHZ) | Disable time, DX high impedance following last data bit from FSX high | | | 2P + 3 | 6P + 20 | ns |
| 8 | td(FXL-DXV) | Delay time, FSX low to DX valid | | | 4P + 2 | 8P + 20 | ns |

 $[\]dagger$ P = 1/CPU clock frequency in ns. For example, when running parts at 100 MHz, use P = 10 ns.

H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even

= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero

L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even

= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero

CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP

[#]FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).



[‡] For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

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[§]S = Sample rate generator input clock = 2P if CLKSM = 1 (P = 1/CPU clock frequency)

⁼ Sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)

T = CLKX period = (1 + CLKGDV) * S

[¶] FSRP = FSXP = 1. As a SPI master, FSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on FSX and FSR is inverted before being used internally.

MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

switching characteristics over recommended operating conditions for McBSP as SPI master or slave: CLKSTP = 10b, CLKXP = 1^{+} (see Figure 48) [C6712C/C6712D]

| | | | | 12 | C-167 | | | 12 | D-167 | | |
|-----|-----------------------------|--|---------------|-------|----------|----------|-------|-------|--------|----------|----|
| NO. | PA | RAMETER | MASTER§ SLAVE | | MASTER§ | | SL | AVE | UNIT | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| 1 | th(CKXH-FXL) | Hold time, FSX low after CLKX high¶ | T – 2 | T + 3 | | | T – 2 | T + 3 | | | ns |
| 2 | td(FXL-CKXL) | Delay time, FSX low to CLKX low# | H – 2 | H + 3 | | | H – 2 | H + 3 | | | ns |
| 3 | td(CKXL-DXV) | Delay time, CLKX low to DX valid | -3 | 4 | 6P + 2 | 10P + 17 | -3 | 4 | 6P + 2 | 10P + 17 | ns |
| 6 | ^t dis(CKXH-DXHZ) | Disable time, DX high impedance following last data bit from CLKX high | H – 3.6 | H+3 | | | H – 2 | H+3 | | | ns |
| 7 | tdis(FXH-DXHZ) | Disable time, DX high impedance following last data bit from FSX high | | | 2P + 1.5 | 6P + 17 | | | 2P + 3 | 6P + 17 | ns |
| 8 | td(FXL-DXV) | Delay time, FSX low to DX valid | | | 4P + 2 | 8P + 17 | | | 4P + 2 | 8P + 17 | ns |

 $^{^{\}dagger}$ P = 1/CPU clock frequency in ns. For example, when running parts at 167 MHz, use P = 6 ns.

H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even

= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero

L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even

= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero

CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP

[#]FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).

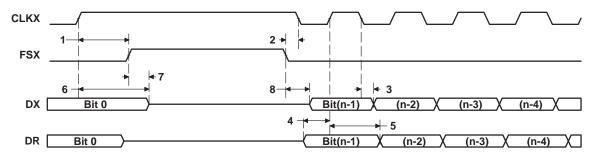


Figure 48. McBSP Timing as SPI Master or Slave: CLKSTP = 10b, CLKXP = 1

[‡] For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

 $[\]S S = Sample rate generator input clock = 2P if CLKSM = 1 (P = 1/CPU clock frequency)$

⁼ Sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)

T = CLKX period = (1 + CLKGDV) * S

[¶] FSRP = FSXP = 1. As a SPI master, FSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on FSX and FSR is inverted before being used internally.

SM320C6712-EP, SM320C6712C-EP, SM320C6712D-EP FLOATING-POINT DIGITAL SIGNAL PROCESSORS

SGUS055 - SEPTEMBER 2004

MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

timing requirements for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = 1^{+} (see Figure 49) [C6712]

| | | | - | 100 | | |
|-----|---|-----|-----|---------|-----|------|
| NO. | | MAS | TER | SLA | /E | UNIT |
| | | MIN | MAX | MIN | MAX | |
| 4 | t _{SU(DRV-CKXH)} Setup time, DR valid before CLKX high | 26 | | 2 – 6P | | ns |
| 5 | th(CKXH-DRV) Hold time, DR valid after CLKX high | 4 | | 6 + 12P | | ns |

[†] P = 1/CPU clock frequency in ns. For example, when running parts at 100 MHz, use P = 10 ns.

timing requirements for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = $1^{\dagger \ddagger}$ (see Figure 49) [C6712C/C6712D]

| | | | - | -167 | | |
|-----|---|-----|-----|---------|-----|------|
| NO. | | MAS | TER | SLAV | /E | UNIT |
| | | MIN | MAX | MIN | MAX | |
| 4 | tsu(DRV-CKXH) Setup time, DR valid before CLKX high | 12 | | 2 – 6P | | ns |
| 5 | th(CKXH-DRV) Hold time, DR valid after CLKX high | 4 | | 5 + 12P | | ns |

 $[\]dagger P = 1/CPU$ clock frequency in ns. For example, when running parts at 167 MHz, use P = 6 ns.

switching characteristics over recommended operating conditions for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = 1^{+} (see Figure 49) [C6712]

| NO. | | PARAMETER | | | SL | AVE | UNIT |
|-----|-----------------|--|-------|-------|--------|----------|------|
| | | | MIN | MAX | MIN | MAX | |
| 1 | th(CKXH-FXL) | Hold time, FSX low after CLKX high¶ | H – 9 | H + 9 | | | ns |
| 2 | td(FXL-CKXL) | Delay time, FSX low to CLKX low# | T – 9 | T + 9 | | | ns |
| 3 | td(CKXH-DXV) | Delay time, CLKX high to DX valid | -9 | 9 | 6P + 4 | 10P + 20 | ns |
| 6 | tdis(CKXH-DXHZ) | Disable time, DX high impedance following last data bit from CLKX high | -9 | 9 | 6P + 3 | 10P + 20 | ns |
| 7 | td(FXL-DXV) | Delay time, FSX low to DX valid | L-9 | L+9 | 4P + 2 | 8P + 20 | ns |

 $[\]dagger P = 1/CPU$ clock frequency in ns. For example, when running parts at 100 MHz, use P = 10 ns.

H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even

= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero

L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even

= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero

CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP



[‡] For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

[‡] For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

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[§] S = Sample rate generator input clock = 2P if CLKSM = 1 (P = 1/CPU clock frequency)

⁼ Sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)

T = CLKX period = (1 + CLKGDV) * S

[¶] FSRP = FSXP = 1. As a SPI master, FSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on FSX and FSR is inverted before being used internally.

[#]FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).

MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

switching characteristics over recommended operating conditions for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = 1^{+} (see Figure 49) [C6712C/C6712D]

| | | | | 12 | 2C-167 | | | 12[| D-167 | | |
|-----|-----------------------------|--|---------|-------|----------|----------|---------|---------|--------|----------|------|
| NO. | PARAMETER | | MASTER§ | | SLAVE | | MASTER§ | | SL | AVE | UNIT |
| | | | | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| 1 | th(CKXH-FXL) | Hold time, FSX low after CLKX high¶ | H – 2 | H + 3 | | | H – 2 | H + 3 | | | ns |
| 2 | td(FXL-CKXL) | Delay time, FSX low to CLKX low# | T – 2 | T + 3 | | | T – 2 | T + 3 | | | ns |
| 3 | td(CKXH-DXV) | Delay time, CLKX high to DX valid | -3 | 4 | 6P + 2 | 10P + 17 | -3 | 4 | 6P + 2 | 10P + 17 | ns |
| 6 | ^t dis(CKXH-DXHZ) | Disable time, DX high impedance following last data bit from CLKX high | -3.6 | 4 | 6P + 1.5 | 10P + 17 | -2 | 4 | 6P + 3 | 10P + 17 | ns |
| 7 | t _d (FXL-DXV) | Delay time, FSX low to DX valid | L – 2 | L + 4 | 4P + 2 | 8P + 17 | L – 2 | L + 6.5 | 4P + 2 | 8P + 17 | ns |

 $[\]dagger$ P = 1/CPU clock frequency in ns. For example, when running parts at 167 MHz, use P = 6 ns.

H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even

= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero

L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even

= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero

[#]FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).

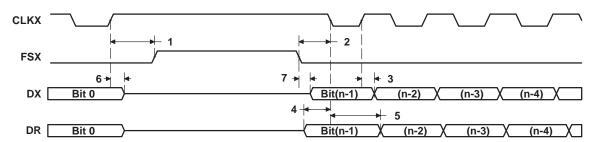


Figure 49. McBSP Timing as SPI Master or Slave: CLKSTP = 11b, CLKXP = 1

[‡] For all SPI slave modes. CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

[§] S = Sample rate generator input clock = 2P if CLKSM = 1 (P = 1/CPU clock frequency)

⁼ Sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)

T = CLKX period = (1 + CLKGDV) * S

FSRP = FSXP = 1. As a SPI master, FSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on FSX and FSR is inverted before being used internally.

CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP

CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP

TIMER TIMING

timing requirements for timer inputs[†] (see Figure 50)

| NO. | | | -10 -16 | | UNIT |
|-----|-----------------------|---------------------------|------------|-----|------|
| | | | MIN | MAX | |
| 1 | tw(TINPH) | Pulse duration, TINP high | 2P | | ns |
| 2 | ^t w(TINPL) | Pulse duration, TINP low | 2P | | ns |

 $[\]dagger$ P = 1/CPU clock frequency in ns. For example, when running parts at 100 MHz, use P = 10 ns.

switching characteristics over recommended operating conditions for timer outputs[†] (see Figure 50)

| NO. | | PARAMETER | -10 -16 | | UNIT |
|-----|-----------|---------------------------|------------|-----|------|
| | | | MIN | MAX | |
| 3 | tw(TOUTH) | Pulse duration, TOUT high | 4P-3 | | ns |
| 4 | tw(TOUTL) | Pulse duration, TOUT low | 4P-3 | | ns |

 $[\]dagger$ P = 1/CPU clock frequency in ns. For example, when running parts at 100 MHz, use P = 10 ns.

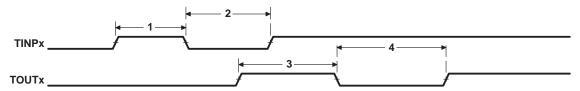


Figure 50. Timer Timing

GENERAL-PURPOSE INPUT/OUTPUT (GPIO) PORT TIMING [C6712C/C6712D ONLY]

timing requirements for GPIO inputs^{†‡} (see Figure 51)

| NO | | -167 | 7 | LINUT |
|-----|---|------|-----|-------|
| NO. | | MIN | MAX | UNIT |
| 1 | t _W (GPIH) Pulse duration, GPIx high | 4P | | ns |
| 2 | t _W (GPIL) Pulse duration, GPIx low | 4P | | ns |

 $^{^{\}dagger}$ P = 1/CPU clock frequency in ns. For example, when running parts at 167 MHz, use P = 6 ns.

switching characteristics over recommended operating conditions for GPIO outputs†§ (see Figure 51)

| No | PARAMETER | -167 | | |
|-----|---|---------|-----|------|
| NO. | | MIN N | MAX | UNIT |
| 3 | t _W (GPOH) Pulse duration, GPOx high | 12P – 3 | | ns |
| 4 | t _W (GPOL) Pulse duration, GPOx low | 12P – 3 | | ns |

 $^{^{\}dagger}$ P = 1/CPU clock frequency in ns. For example, when running parts at 167 MHz, use P = 6 ns.

[§] The number of CFGBUS cycles between two back-to-back CFGBUS writes to the GPIO register is 12 SYSCLK1 cycles; therefore, the minimum GPOx pulse width is 12P.

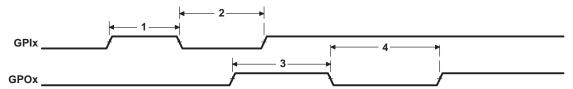


Figure 51. GPIO Port Timing

[‡] The pulse width given is sufficient to generate a CPU interrupt or an EDMA event. However, if a user wants to have the DSP recognize the GPIx changes through software polling of the GPIO register, the GPIx duration must be extended to at least 24P to allow the DSP enough time to access the GPIO register through the CFGBUS.

JTAG TEST-PORT TIMING

timing requirements for JTAG test port (see Figure 52)

| No | | | -100 | | -167 | | |
|-----|-----------------------------|--|------|-----|------|-----|------|
| NO. | | | MIN | MAX | MIN | MAX | UNIT |
| 1 | t _C (TCK) | Cycle time, TCK | 35 | | 35 | | ns |
| 3 | t _{su} (TDIV-TCKH) | Setup time, TDI/TMS/TRST valid before TCK high | 10 | | 10 | | ns |
| 4 | th(TCKH-TDIV) | Hold time, TDI/TMS/TRST valid after TCK high | 5 | | 7 | | ns |

switching characteristics over recommended operating conditions for JTAG test port (see Figure 52)

| NO. | PARAMETER | -100 | | -167 | | |
|-----|---|------|-----|------|-----|------|
| | | MIN | MAX | MIN | MAX | UNIT |
| 2 | t _d (TCKL-TDOV) Delay time, TCK low to TDO valid | -3 | 18 | 0 | 15 | ns |

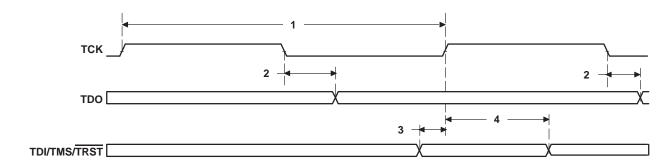
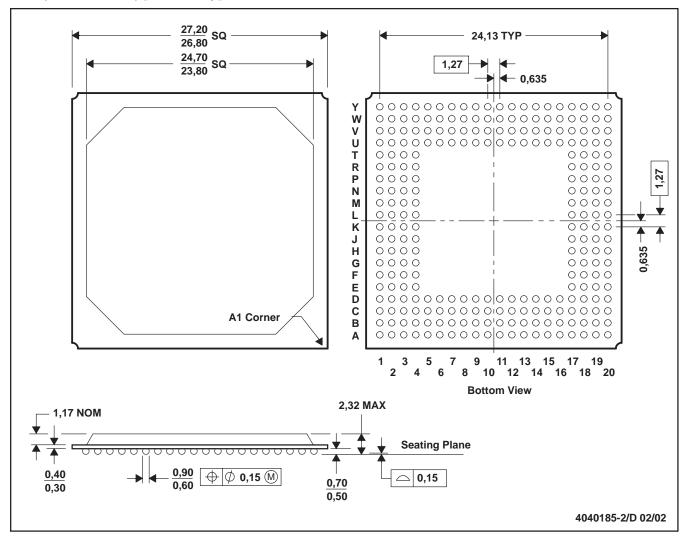


Figure 52. JTAG Test-Port Timing

MECHANICAL DATA [C6712 ONLY]

GFN (S-PBGA-N256) [C6712 only]

PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-151

thermal resistance characteristics (S-PBGA package) [C6712 only]

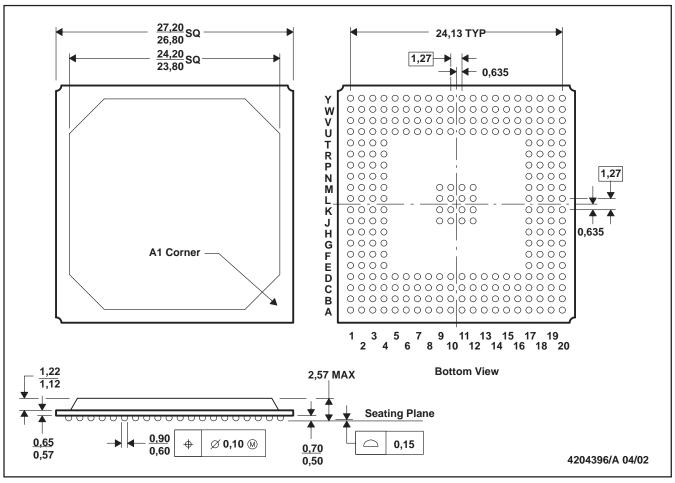
| NO | | °C/W | Air Flow (m/s)† |
|----|---------------------------------------|------|-----------------|
| 1 | R⊖ _{JC} Junction-to-case | 6.4 | N/A |
| 2 | RΘ _{JA} Junction-to-free air | 25.5 | 0.0 |
| 3 | R⊖JA Junction-to-free air | 23.1 | 0.5 |
| 4 | R⊖JA Junction-to-free air | 22.3 | 1.0 |
| 5 | R⊖JA Junction-to-free air | 21.2 | 2.0 |

[†]m/s = meters per second

MECHANICAL DATA [C6712C/C6712D ONLY]

GDP (S-PBGA-N272) [C6712C/12D only]

PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-151

thermal resistance characteristics (S-PBGA package) [C6712C/12D only]

| NO | | °C/W | Air Flow (m/s)† | | |
|---|---|------|-----------------|--|--|
| Two Signals, Two Planes (4-Layer Board) | | | | | |
| 1 | R⊖ _{JC} Junction-to-case | 9.7 | N/A | | |
| 2 | PsiJT Junction-to-package top | 1.5 | 0.0 | | |
| 3 | $R\Theta_{\mbox{\scriptsize JB}}$ Junction-to-board | 19 | N/A | | |
| 4 | RΘ _{JA} Junction-to-free air | 22 | 0.0 | | |
| 5 | RΘ _{JA} Junction-to-free air | 21 | 0.5 | | |
| 6 | RΘJA Junction-to-free air | 20 | 1.0 | | |
| 7 | RΘJA Junction-to-free air | 19 | 2.0 | | |
| 8 | RΘJA Junction-to-free air | 18 | 4.0 | | |
| 9 | Psi _{JB} Junction-to-board | 16 | 0.0 | | |

[†]m/s = meters per second



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