OMAP5912 Applications Processor

Data Manual

Literature Number: SPRS231E
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REVISION HISTORY

This data sheet revision history highlights the technical changes made to SPRS231D to generate SPRS231E.

Scope: Added 289-ball GDY package.
Added Section 4.2, Differences Between Production and Experimental Devices.
Updated parametric values, added Section 5.7.1.1, updated timing diagrams, etc.

PAGE(S) NO.	ADDITIONS/CHANGES/DELETIONS
	Global: − added 289-ball GDY package
23	Section 2.1.1.1, DSP Tools Support: − removed “Visual Linker” from list of Code Composer Studio code generation tools
26	Table 2−1, ZDY/GDY Package Terminal Assignments: − M17: changed “GPIO4(0) / MCBSP3.FSX(2) / TIMER.EVENT4(3) / SPIF.DIN(4)” to “GPIO4(0) / **SPI.CS2(1)** / MCBSP3.FSX(2) / TIMER.EVENT4(3) / SPIF.DIN(4)” − T15: changed “Reserved” to “TDO” − added “For special consideration with respect to the connection of the V_{SS} pin (ZDY/GDY ball H8), refer to Section 5.5.1, 32-kHz Oscillator and Input Clock.” footnote
33	Table 2−2, ZZG Package Terminal Assignments: − P20: changed “GPIO4(0) / MCBSP3.FSX(2) / TIMER.EVENT4(3) / SPIF.DIN(4)” to “GPIO4(0) / **SPI.CS2(1)** / MCBSP3.FSX(2) / TIMER.EVENT4(3) / SPIF.DIN(4)” − AA19: changed “Reserved” to “TDO” − added “For special consideration with respect to the connection of the V_{SS} pin (ZZG ball Y13), refer to Section 5.5.1, 32-kHz Oscillator and Input Clock.” footnote
40	Table 2−3, ZDY/GDY Package Terminal Characteristics: − SDRAM.A[13:0]: transposed ball numbers C8 and D9 − E15: updated MUX CTRL SETTING column − H14: updated SUPPLY column − K17: updated MUX CTRL SETTING column − K13: added row for RTDX.D[3] − L15: added row for RTDX.D[2] − L14: changed “MCBSP3.**E**SX” to “MCBSP3.FSX” − M17: added row for SPIF.DIN − M16: added row for RTDX.D[0] − added row for TDO signal (Ball T15) − U15: updated MUX CTRL SETTING column − M8: updated MUX CTRL SETTING column − T1: updated MUX CTRL SETTING column − G3: updated RESET STATE column − J8: updated MUX CTRL SETTING column − J5: updated PULLUP/PULLDN column − added “Slew time constraint of the $\overline{\text{EXT\_DMA\_REQ1}}$ must be lower than or equal to 10 ns (from 10% to 90% of DV_{DD}) in Mode 1.” footnote − added “Slew time constraint of the $\overline{\text{EXT\_DMA\_REQ0}}$ must be lower than or equal to 10 ns (from 10% to 90% of DV_{DD}) in Mode 1.” footnote

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61	Table 2−4, ZZG Package Terminal Characteristics: − E18: updated MUX CTRL SETTING column − J20: updated SUPPLY column − M18: updated MUX CTRL SETTING column − N20: added row for RTDX.D[3] − M15: added row for RTDX.D[2] − P19: changed “MCBSP3.**E**SX” to “MCBSP3.FSX” − P20: added row for SPIF.DIN − M14: added row for RTDX.D[0] − added row for TDO signal (Ball AA19) − P14: updated MUX CTRL SETTING column − V11: updated MUX CTRL SETTING column − Y1: updated MUX CTRL SETTING column − K8: updated RESET STATE column − M4: updated MUX CTRL SETTING column − M7: updated PULLUP/PULLDN column − added “Slew time constraint of the $\overline{\text{EXT\_DMA\_REQ1}}$ must be lower than or equal to 10 ns (from 10% to 90% of DV_{DD}) in Mode 1.” footnote − added “Slew time constraint of the $\overline{\text{EXT\_DMA\_REQ0}}$ must be lower than or equal to 10 ns (from 10% to 90% of DV_{DD}) in Mode 1.” footnote
81	Table 2−5, Signal Descriptions: − CAMERA INTERFACE section: added CAM.EXCLK signal − TDO signal: added Ball T15 for ZDY/GDY package added Ball AA19 for ZZG package − MPU_BOOT signal: updated DESCRIPTION − added “GPIO13 is used to select between full and fast boot. Set GPIO13 high to boot from the USB peripheral. Set GPIO13 low to boot from external flash on CS3.” footnote
100	Figure 3−1, OMAP5912 Functional Block Diagram: − moved Camera I/F from the block on the right to the left under the memory interface traffic controller block
104	Section 3.2.1, MPU Global Memory Map: − updated “CS1 and CS2 can be split **by software** to provide ...” NOTE
135	Table 3−29, McBSP2 Registers: − added DSP WORD ADDRESS column
138	Table 3−35, I^2C1 Registers: − added DSP WORD ADDRESS column
140	Table 3−38, MMC/SDIO2 Registers: − added DSP WORD ADDRESS column
142	Table 3−40, MPU GPIO3 Registers: − added DSP WORD ADDRESS column
143	Table 3−41, MPU GPIO4 Registers: − added DSP WORD ADDRESS column
148	Table 3−47, McBSP1 Registers: − updated addresses of MCBSP1_RCERB through MCBSP1_REV registers
151	Table 3−50, McBSP3 Registers: − updated addresses of MCBSP1_RCERB through MCBSP3_REV registers
153	Table 3−51: − changed title from “MPU **UART** TIPB Bus Switch Registers” to “MPU TIPB Bus Switch Registers”

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163	Table 3−70, DSP DMA Controller Registers: − updated address of DSP_DMA_CDFI1 (Channel 1 Destination Frame Index) − updated address of DSP_DMA_CDEI1 (Channel 1 Destination Element Index) − updated address of DSP_DMA_CDFI2 (Channel 2 Destination Frame Index) − updated address of DSP_DMA_CDEI2 (Channel 2 Destination Element Index) − updated address of DSP_DMA_CDFI3 (Channel 3 Destination Frame Index) − updated address of DSP_DMA_CDEI3 (Channel 3 Destination Element Index) − updated address of DSP_DMA_CDFI4 (Channel 4 Destination Frame Index) − updated address of DSP_DMA_CDEI4 (Channel 4 Destination Element Index) − updated address of DSP_DMA_CDFI5 (Channel 5 Destination Frame Index) − updated address of DSP_DMA_CDEI5 (Channel 5 Destination Element Index)
167	Table 3−77, DSP Level 2.1 Interrupt Handler Registers: − updated addresses of DSP_L21_SIR_IRQ_CODE through DSP_L21_ILR15 registers − removed DSP_L21_ISR (Software Interrupt Set Register) from 0x00 4C0Ah

168	Table 3−78, DSP TIPB Bridge Configuration Register:
	− 0x00 0000:
	  − changed REGISTER NAME from DSP_ID to DSP_CMR
	  − changed DESCRIPTION from “Identification Register” to “DSP Control Mode Register”
	− removed all the registers from 0x00 0002 to 0x00 006E

168	Table 3−79, DSP EMIF Configuration Registers: − 0x00 0800 (DSP_EMIF_CNTL): changed RESET VALUE from 002xh to 0000h − 0x00 0801: changed from Reserved to DSP_EMIF_GRR (DSP EMIF Global Reset Register) − removed all the registers from 0x00 0802 to 0x00 0814
170	Section 3.4, DSP External Memory (Managed by MMU): − updated “When the DSP MMU is on, ...” paragraph
170	Figure 3−2, DSP MMU Off: − DSP Memory: changed “0x05 0000” to “0x02 8000”
171	Figure 3−3, DSP MMU On: − DSP Memory: changed “0x05 0000” to “0x02 8000”
176	Updated Section 3.6.6, Pulse-Width Light (PWL)
176	Updated Section 3.6.8, HDQ/1-Wire Interface
177	Section 3.6.10, MPUIO Interface: − updated “The MPUIO feature allows communication ...” paragraph
180	Section 3.7.2, Multichannel Serial Interfaces (MCSI1 and 2): − changed “Programmable interrupt occurrence time (TX and RX)” to “Programmable interrupt **condition** (TX and RX)”
181	Section 3.8.2, General-Purpose Timers: − changed “Interrupts generated on overflow, compare, **and capture**” to “Interrupts generated on overflow and compare”
182	Section 3.8.3, Serial Port Interface (SPI): − updated “The serial port interface is a bidirectional ...” paragraph
182	Updated Section 3.8.4, Universal Asynchronous Receiver/Transmitter (UART)
184	Updated Section 3.8.5, I^2C Master/Slave Interface
185	Section 3.8.7, Multimedia Card/Secure Digital (MMC/SDIO2) Interface: − changed “OMAP5912 also support control signals ...” bullet item to “The MMC2 provides auxiliary signals for external level shifters ...”

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186	Section 3.8.9, 32-kHz Synchro Counter: − changed “This is a 32-bit **ordinary** counter, ...” to “This is a 32-bit **simple** counter, ...”
187	Section 3.9, System DMA Controller: − changed “Software **enabling**” to “Software triggering” − changed “Hardware **enabling**” to “Hardware triggering”
189	Updated Section 3.12.1, MPU/DSP Mailbox Registers
190	Section 3.12.3, MPU/DSP Shared Memory: − updated “The OMAP5912 implements a shared memory architecture via the traffic controller ...” paragraph
191	Section 3.14.1, Core and I/O Voltage Supply Connections: − updated “The OMAP5912 device is ...” paragraph
191	Figure 3−4, Supply Connections for a Typical System: − updated footnote
193	Section 4.1, Device and Development-Support Tool Nomenclature: − under “Device development evolutionary flow”, changed “X **or P**” to “X”
194	Added Section 4.2, Differences Between Production and Experimental Devices
199	Section 5.3, Electrical Characteristics Over Recommended Operating Case Temperature Range (Unless Otherwise Noted): − added $I_{DDC(Q)}$, $I_{DDC(A)}$, $I_{DDCP(A)}$, V_{DD4} − added footnotes
204	Section 5.5.2, Base Oscillator (12, 13, or 19.2 MHz) and Input Clock: − updated “The crystal must be in fundamental-mode operation ...” paragraph
205	Table 5−4: − changed title from “12-MHz to 19.2-MHz Input Clock Timing Requirements” to “12-MHz**, 13-MHz, and** 19.2-MHz Input Clock Timing Requirements”
206	Table 5−5, OMAP5912 Device Reset Timing Requirements: − added footnote about PWRON_RESET
208	Section 5.7.1, EMIFS/NOR Flash Interface Timing: − added “Section 5.7.1.1 provides information on and an example of how to calculate OMAP5912 EMIFS NOR Flash timings.” paragraph
208	Table 5−9, EMIFS/NOR Flash Interface Timing Requirements: − removed parameter F8 [$t_{su(RDYIV-OEH)}$, Setup time, FLASH.RDY high before $\overline{\text{FLASH.OE}}$ high] − changed “async modes” to “async page mode” on F21 and F22

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209	Table 5−10, EMIFS/NOR Flash Interface Switching Characteristics:
	− Added rows for F17 and F18
	− F27:
	  − updated symbol and description
	  − changed MIN value from “H − 6.6” ns to “H − 3.29” ns
	  − changed MAX value from “H + 3.29” ns to “H + 6.6” ns
	− F29: updated symbol and description
	− F30: updated symbol and description
	− F31: updated symbol and description
	− F40: updated symbol and description
	− F41: updated symbol and description
	− F42: updated symbol and description
	− F43: updated symbol and description
	− added “See Section 5.7.1.1 for information on and an example of how to calculate OMAP5912 EMIFS NOR Flash timings.” to second footnote

211	Added Section 5.7.1.1, EMIFS NOR Flash Timing Calculation Example
213	Table 5−11, Sample Timing Calculation of Table 5−9 Parametric Values Using Constraints Calculated Above: − changed “async modes” to “async page mode” on F21 and F22
214	Table 5−12, Sample Timing Calculation of Table 5−10 Parametric Values Using Constraints Calculated Above: − modified values for F13 and f15 − added rows for F17/F18
218	Figure 5−10, EMIFS/NOR Flash—Single Word Asynchronous Read, Full-Handshaking Mode Timing: − removed parameter F8
219	Figure 5−11, EMIFS/NOR Flash—Asynchronous 32-Bit Read Timing: − changed F13 to F17 − changed F15 to F18
220	Figure 5−13: − changed title from “EMIFS/NOR Flash—Single Word Asynchronous Write Timing” to “EMIFS/NOR Flash—Single Word Asynchronous Write Timing**, Full-Handshaking Mode**” − removed parameter F8
221	Figure 5−14: − changed title from “EMIFS/NOR Flash—Single Word Asynchronous Write**, Full-Handshaking Mode**” to “EMIFS/NOR Flash—Single Word Asynchronous Write”
224	Figure 5−18, EMIFS/Multiplexed NOR Flash—Single Word Asynchronous Read Timing: − changed F13 to F17
225	Figure 5−20, EMIFS/Multiplexed NOR Flash—Synchronous Burst Read Timing (Retiming Off): − changed F13 to F17
226	Table 5−14, EMIFS/NAND Flash Switching Characteristics: − NFE5: updated symbol
229	Table 5−15, EMIFF/SDR SDRAM Interface Timing Requirements: − added footnote about the CONF_VOLTAGE_SDRAM_R control bit

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229	Table 5−16, EMIFF/SDR SDRAM Interface Switching Characteristics: − SD1 [$t_{c(CLK)}$, DV_{DD4} = 1.8 V]: changed MIN value from P ns to 10.41 ns − SD1 [$t_{c(CLK)}$, DV_{DD4} = 2.75 V/3.3 V]: changed MIN value from P ns to 10.41 ns − SD3 [$t_{d(CLKH–DQMV)}$, DV_{DD4} = 1.8 V]: changed MAX value from “1.20 + D” ns to 1.20 ns − SD3 [$t_{d(CLKH–DQMV)}$, DV_{DD4} = 2.75 V/3.3 V]: changed MAX value from “1.22 + D” ns to 1.22 ns − SD4 [$t_{d(CLKH–DQMIV)}$, DV_{DD4} = 1.8 V]: changed MIN value from “0 + D” ns to 0.23 ns − SD4 [$t_{d(CLKH–DQMIV)}$, DV_{DD4} = 2.75 V/3.3 V]: changed MIN value from “0 + D” ns to 0.30 ns − added footnote about the CONF_VOLTAGE_SDRAM_R control bit − revised “P = SDRAM.CLK period in nanoseconds” footnote − revised footnote about external delay element
230	Updated Figure 5−25, EMIFF/SDR Two SDRAM RD (Read) Commands (Active Row)
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233	Table 5−17, EMIFF/Mobile DDR SDRAM Timing Requirements: − DD17 [$t_{su(DV-DQSL/H)}$]: changed MIN value from “0.76 − 0.2P” ns to −1.32 ns − DD18 [$t_{h(DQSL/H-DV)}$]: changed MIN value from “0.2P + 0.8” ns to 2.88 ns − removed “P = SDRAM.CLK period in nanoseconds” footnote − added “The control bit CONF_VOLTAGE_SDRAM_R of the register VOLTAGE_CTRL_0 must be set to 1 regardless of the DV_{DD4} voltage level.” footnote

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233	Table 5−18, EMIFF/Mobile DDR SDRAM Switching Characteristics:
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	− removed parameter DD2 [$t_{w(CLK)}$, Pulse duration, SDRAM.CLK/SDRAM.DDR-CLK]
	− DD3 [$t_{osu(CLKH-CSL)}$]: changed MIN value from “0.5P − 3.21” ns to 2.00 ns
	− DD4 [$t_{oh(CLKH-CSH)}$]: changed MIN value from “0.5P − 3.21” ns to 2.00 ns
	− DD5 [$t_{osu(CLKH-RASL)}$]:
	  − changed MIN value from “0.5P − 3.21” ns to 2.00 ns
	  − added MAX value of 5.21 ns
	− DD5A [$t_{osu(CLKH-CASL)}$]:
	  − changed MIN value from “0.5P − 3.21” ns to 2.00 ns
	  − added MAX value of 5.40 ns
	− DD6 [$t_{oh(CLKH-RASH)}$]:
	  − changed MIN value from “0.5P − 3.21” ns to 2.00 ns
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	− DD7 [$t_{osu(CLKH-BAV)}$]: changed MIN value from “0.5P − 3.21” ns to 2.00 ns
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	  − updated symbol
	  − changed MIN value from “0.3P − 2.12” ns to 1.00 ns
	− DD14:
	  − updated symbol and description
	  − changed MIN value from “0.7P − 6.28” ns to 1.01 ns
	− removed “P = SDRAM.CLK period in nanoseconds” footnote
	− removed footnote about maximum EMIFF/SDRAM clock rate
	− added “The control bit CONF_VOLTAGE_SDRAM_R of the register VOLTAGE_CTRL_0 must be set to 1 regardless of the DV_{DD4} voltage level.” footnote
	− added footnote about DLL phase value
	− added footnote about delay time

234	Updated Figure 5−31, EMIFF/Mobile DDR SDRAM—Command and Address Output Timing Definition
234	Updated Figure 5−32, EMIFF/Mobile DDR SDRAM—Memory Read Timing
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247	Table 5−33, Camera Interface Timing Requirements: − C1 {1/[$t_{c(LCLK)}$]}: changed MAX value from 48 MHz to 80 MHz − C9: changed symbol from $t_{su(LCLKH-DV)}$ to $t_{su(DV-LCLKH)}$ − C10: changed symbol from $t_{h(DV-LCLKH)}$ to $t_{h(LCLKH-DV)}$ − C11: changed symbol from $t_{su(LCLKH-DV)}$ to $t_{su(CAM.VS/HS-LCLKH)}$ − C12: changed symbol from $t_{h(DV-LCLKH)}$ to $t_{h(LCLKH-CAM.VS/HS)}$
248	Table 5−34, LCD Controller and LCDCONV Switching Characteristics: − L5: changed symbol from $t_{d(CLK-HS)}$ to $t_{d(CLK-VS)}$ − L6: changed symbol from $t_{d(CLK-VS)}$ to $t_{d(CLK-HS)}$

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- Low-Power, High-Performance CMOS Technology
  - 0.13-μm Technology
  - 192-MHz Maximum Frequency
  - 1.6 ± 5% V Core Voltage
- ARM926EJ-S™ (MPU) Core
  - Support for 32-Bit and 16-Bit (Thumb® Mode) Instruction Sets
  - 16K-Byte Instruction Cache
  - 8K-Byte Data Cache
  - Data and Program Memory Management Unit (MMU)
  - 17-Word Write Buffer
  - Two 64-Entry Translation Look-Aside Buffers (TLBs) for MMUs
- TMS320C55x™ (C55x™) DSP Core
  - One/Two Instructions Executed per Cycle
  - Dual Multipliers (Two Multiply-Accumulates per Cycle)
  - Two Arithmetic/Logic Units
  - Five Internal Data/Operand Buses (3 Read Buses and 2 Write Buses)
  - 32K x 16-Bit On-Chip Dual-Access RAM (DARAM) (64K Bytes)
  - 48K x 16-Bit On-Chip Single-Access RAM (SARAM) (96K Bytes)
  - Instruction Cache (24K Bytes)
  - Video Hardware Accelerators for DCT, iDCT, Pixel Interpolation, and Motion Estimation for Video Compression
- 250K Bytes of Shared Internal SRAM
- Memory Traffic Controller (TC)
  - 16-Bit EMIFS Supports up to 256M Bytes of External Memory (i.e., Async. ROM/RAM, NOR/NAND Flash, and Sync. Burst Flash)
  - 16-Bit EMIFF to Access up to 64M Bytes of SDRAM, Mobile SDRAM, or Mobile DDR
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- MPU Peripherals
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  - USB On-the-Go (OTG) Controller
  - 3 USB Ports, One With an Integrated Transceiver
  - Camera Interface for Parallel CMOS Sensors
  - Real-Time Clock (RTC)
  - Pulse-Width Tone (PWT) Interface
  - Pulse-Width Light (PWL) Interface
  - Keyboard Matrix Interface (6 x 5 or 8 x 8)
  - HDQ/1-Wire® Interface
  - Multimedia Card (MMC) and Secure Digital (SD) Interface
  - Up to 16 MPU General-Purpose I/Os
  - Two LED Pulse Generators (LPGs)
  - ETM9™ Trace Module for ARM926EJ-S Debug
  - 16-/18-Bit LCD Controller With Dedicated System DMA Channel
  - 32-kHz Operating System (OS) Timer
- Shared Peripherals
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  - Serial Port Interface (SPI)
  - Three Universal Asynchronous Receiver/Transmitters (UARTs) (Two Supporting SIR mode for IrDA)
  - Inter-Integrated Circuit (I^2C) Master and Slave Interface
  - Multimedia Card (MMC) and Secure Digital (SD) Interface
  - Multichannel Buffered Serial Port
  - Up to 64 Shared General-Purpose I/Os
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  - Random Number Generation
  - DES and 3DES
  - SHA-1 and MD5
- Individual Power-Saving Modes for MPU/DSP/TC
- On-Chip Scan-Based Emulation Logic
- IEEE Std 1149.1† (JTAG) Boundary Scan Logic
- Three 289-Ball BGA (Ball Grid Array) Packages (ZDY and ZZG − Lead-Free; GDY − With Lead)

† IEEE Standard 1149.1-1990 Standard Test-Access Port and Boundary Scan Architecture.

2 Introduction

This section describes the main features of the OMAP5912 device, lists the terminal assignments, and describes the function of each terminal. This data manual also provides a detailed description section, electrical specifications, parameter measurement information, and mechanical data about the available packaging.

2.1 Description

OMAP5912 is a highly integrated hardware and software platform, designed to meet the application processing needs of next-generation embedded devices.

The OMAP™ platform enables OEMs and ODMs to quickly bring to market devices featuring rich user interfaces, high processing performance, and long battery life through the maximum flexibility of a fully integrated mixed processor solution.

The dual-core architecture provides benefits of both DSP and reduced instruction set computer (RISC) technologies, incorporating a TMS320C55x DSP core and a high-performance ARM926EJ-S ARM® core.

The OMAP5912 device is designed to run leading open and embedded RISC-based operating systems, as well as the Texas Instruments (TI) DSP/BIOS™ software kernel foundation, and is available in three 289-ball ball grid array (BGA) packages (ZDY and ZZG − lead-free; GDY − with lead).

The OMAP5912 device is targeted at the following applications:

- Applications Processing Devices
- Mobile Communications
  - WAN 802.11X
  - Bluetooth™
  - GSM, GPRS, EDGE
  - CDMA
- Video and Image Processing (MPEG4, JPEG, Windows® Media Video, etc.)
- Advanced Speech Applications (text-to-speech, speech recognition)
- Audio Processing (MPEG-1 Audio Layer3 [MP3], AMR, WMA, AAC, and Other GSM Speech Codecs)
- Graphics and Video Acceleration
- Generalized Web Access
- Data Processing

2.1.1 TMS320C55x DSP Core

The DSP core of the OMAP5912 device is based on the TMS320C55x DSP generation CPU processor core. The C55x DSP architecture achieves high performance and low power through increased parallelism and total focus on reduction in power dissipation. The CPU supports an internal bus structure composed of one program bus, three data read buses, two data write buses, and additional buses dedicated to peripheral and DMA activity. These buses provide the ability to perform up to three data reads and two data writes in a single cycle. In parallel, the DMA controller can perform up to two data transfers per cycle independent of the CPU activity. The C55x CPU provides two multiply-accumulate (MAC) units, each capable of 17-bit x 17-bit multiplication in a single cycle. A central 40-bit arithmetic/logic unit (ALU) is supported by an additional 16-bit ALU. Use of the ALUs is under instruction set control, providing the ability to optimize parallel activity and power consumption. These resources are managed in the address unit (AU) and data unit (DU) of the C55x CPU.

The C55x DSPs support a variable byte width instruction set for improved code density. The instruction unit (IU) performs 32-bit program fetches from internal or external memory and queues instructions for the program unit (PU). The program unit decodes the instructions, directs tasks to AU and DU resources, and manages the fully protected pipeline. Predictive branching capability avoids pipeline flushes on execution of conditional instructions. The OMAP5912 DSP core also includes a 24K-byte instruction cache to minimize external memory accesses, improving data throughput and conserving system power.

2.1.1.1 DSP Tools Support

The 55x DSP core is supported by the industry's leading eXpressDSP™ software environment including the Code Composer Studio™ Integrated Development Environment (IDE), DSP/BIOS software kernel foundation, the TMS320™ DSP Algorithm Standard, and the industry's largest third-party network. Code Composer Studio features code generation tools including a C-Compiler, simulator, Real-Time Data Exchange (RTDX™), XDS510™ emulation device drivers, and Chip Support Libraries (CSL). DSP/BIOS is a scalable real-time software foundation available for no cost to users of Texas Instruments' DSP products, providing a preemptive task scheduler and real-time analysis capabilities with very low memory and megahertz overhead. The TMS320 DSP Algorithm Standard is a specification of coding conventions allowing fast integration of algorithms from different teams, sites, or third parties into the application framework. Texas Instruments' extensive DSP third-party network of over 400 providers brings focused competencies and complete solutions to customers.

2.1.1.2 DSP Software Support

Texas Instruments has also developed foundation software available for the 55x DSP core. The C55x DSP Library (DSPLIB) features over 50 C-callable software routines (FIR/IIR filters, Fast Fourier Transforms (FFTs), and various computational functions). The DSP Image/Video Processing Library (IMGLIB) contains over 20 software routines highly optimized for C55x DSPs and is compiled with the latest revision of the C55x DSP code generation tools. These imaging functions support a wide range of applications that include compression, video processing, machine vision, and medical imaging.

2.1.2 ARM926EJ-S RISC Processor

The MPU core is a ARM926EJ-S reduced instruction set computer (RISC) processor. The ARM926EJ-S is a 32-bit processor core that performs 32-bit or 16-bit instructions and processes 32-bit, 16-bit, or 8-bit data. The core uses pipelining so that all parts of the processor and memory system can operate continuously.

The MPU core incorporates:

- A coprocessor 15 (CP15) and protection module
- Data and program Memory Management Units (MMUs) with table look-aside buffers.
- Separate 16K-byte instruction and 8K-byte data caches. Both are four-way associative with virtual index virtual tag (VIVT).

The OMAP5912 device uses the ARM926EJ-S core in little-endian mode only. To minimize external memory access time, the ARM926EJ-S includes an instruction cache, data cache, and a write buffer. In general, these are transparent to program execution.

2.2 Terminal Assignments

Figure 2−1 illustrates the ball locations for the 289-ball ZDY/GDY package and Figure 2−2 illustrates the ball locations for the 289-ball ZZG package. Figure 2−1 and Figure 2−2 are used in conjunction with Table 2−1 and Table 2−2, respectively, to locate signal names and ball grid numbers. BGA ball numbers in Table 2−1 and Table 2−2 are read from left-to-right, top-to-bottom.

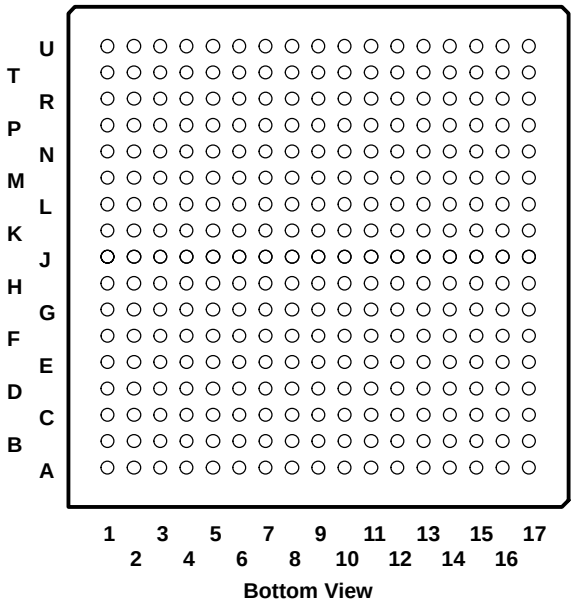

Figure 2−1. OMAP5912 289-Ball ZDY/GDY Plastic Ball Grid Array (Bottom View)

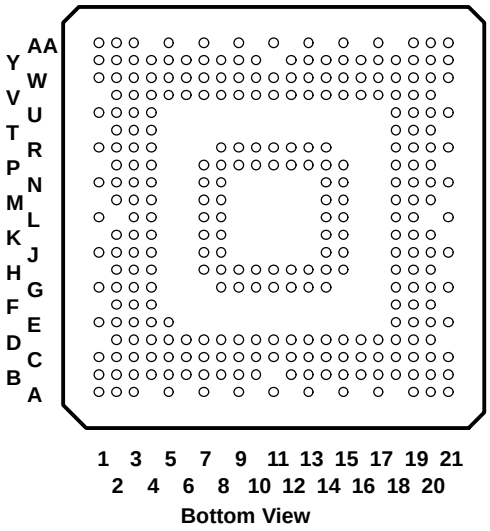

Figure 2−2. OMAP5912 289-Ball ZZG Plastic Ball Grid Array (Bottom View)

In Table 2−1 and Table 2−2, signals with multiplexed functions are highlighted in gray. Signals within a multiplexed pin name are separated with forward slashes as follows:

- **signal1/signal2/signal3** (e.g., MPUIO1/RTCK/SPIF.SCK)

Signals which are associated with specific peripherals are denoted by using the peripheral name, followed by a period, and then the signal name; as follows:

- **peripheral1.signal1** (i.e., MCSI1.DOUT)

Table 2−1. ZDY/GDY Package Terminal Assignments

ZDY/ GDY BALL NO.	SIGNAL	ZDY/ GDY BALL NO.	SIGNAL	ZDY/ GDY BALL NO.	SIGNAL	ZDY/ GDY BALL NO.	SIGNAL
A1	SDRAM.A[1]	A2	SDRAM.DQSL	A3	SDRAM.D[6]	A4	SDRAM.D[2]
A5	SDRAM.D[3]	A6	SDRAM.CLKX	A7	SDRAM.CLK	A8	SDRAM.DQMU
A9	CV_{DDDLL}	A10	SDRAM.A[7]	A11	SDRAM.D[11]	A12	SDRAM.DQSH
A13	LCD.P[12](0)/ Z_STATE†(1)/ GPIO33(7)	A14	LCD.PCLK(0)/ Z_STATE†(1)	A15	LCD.P[10](0)/ Z_STATE†(1)/ GPIO31(7)	A16	LCD.P[6](0)/ Z_STATE†(1)
A17	LCD.P[0](0)/ Z_STATE†(1)	B1	DV_{DD5}	B2	SDRAM.A[0]	B3	SDRAM.D[4]
B4	SDRAM.D[0]	B5	SDRAM.D[1]	B6	SDRAM.D[5]	B7	SDRAM.D[7]
B8	SDRAM.D[10]	B9	SDRAM.D[12]	B10	SDRAM.D[15]	B11	SDRAM.D[13]
B12	SDRAM.D[9]	B13	SDRAM.CKE	B14	LCD.P[11](0)/ Z_STATE†(1)/ GPIO32(7)	B15	LCD.VS(0)/ Z_STATE†(1)
B16	LCD.P[1](0)/ Z_STATE†(1)	B17	KB.C[2](0)/ GPIO61(7)	C1	FLASH.A[6](0)	C2	FLASH.A[2](0)
C3	SDRAM.A[3]	C4	SDRAM.BA[1]	C5	SDRAM.BA[0]	C6	SDRAM.A[8]
C7	SDRAM.DQML	C8	SDRAM.A[5]	C9	SDRAM.D[8]	C10	SDRAM.D[14]
C11	CV_{DD}	C12	LCD.P[15](0)/ Z_STATE†(1)/ GPIO2(7)	C13	LCD.P[8](0)/ Z_STATE†(1)/ GPIO29(7)	C14	DV_{DD1}
C15	LCD.P[5](0)/ Z_STATE†(1)	C16	LCD.P[2](0)/ Z_STATE†(1)	C17	KB.C[1](0)/ MPUIO6(1)	D1	FLASH.A[8](0)
D2	FLASH.A[5](0)	D3	FLASH.A[1](0)	D4	$\overline{\text{SDRAM.RAS}}$	D5	$\overline{\text{SDRAM.CAS}}$
D6	DV_{DD4}	D7	DV_{DD4}	D8	DV_{DD4}	D9	SDRAM.A[4]
D10	SDRAM.A[13]	D11	DV_{DD4}	D12	LCD.P[14](0)/ Z_STATE†(1)/ GPIO35(7)	D13	LCD.P[7](0)/ Z_STATE†(1)
D14	LCD.P[3](0)/ Z_STATE†(1)	D15	LCD.HS(0)/ Z_STATE†(1)	D16	KB.C[4](0)/ GPIO27(7)	D17	KB.R[3](0)/ MPUIO13(1)
E1	FLASH.A[9](0)	E2	FLASH.A[7](0)	E3	FLASH.A[4](0)	E4	FLASH.A[3](0)
E5	V_{SS}	E6	$\overline{\text{SDRAM.WE}}$	E7	$\overline{\text{SDRAM.CS}}$	E8	SDRAM.A[12]
E9	SDRAM.A[11]	E10	SDRAM.A[6]	E11	LCD.P[13](0)/ Z_STATE†(1)/ GPIO34(7)	E12	LCD.P[4](0)/ Z_STATE†(1)
E13	V_{SS}	E14	NC‡	E15	KB.C[3](0)/ GPIO63(6)	E16	KB.R[2[(0)/ MPUIO10(1)

† Z_STATE = high-impedance
‡ “NC” denotes “No Connect”.
§ LOW_STATE = 0
¶ Signal must be tied low.
# For special consideration with respect to the connection of the V_{SS} pin (ZDY/GDY ball H8), refer to Section 5.5.1, 32-kHz Oscillator and Input Clock.

NOTES: 1. Shading denotes signals with multiplexed functions.
2. The number within parenthesis at the end of a signal name denotes the Pin Mux setting (see the MUX CTRL SETTING column in Table 2−3 and Table 2−4).

Table 2−1. ZDY/GDY Package Terminal Assignments (Continued)

ZDY/ GDY BALL NO.	SIGNAL	ZDY/ GDY BALL NO.	SIGNAL	ZDY/ GDY BALL NO.	SIGNAL	ZDY/ GDY BALL NO.	SIGNAL
E17	KB.R[1](0)/ MPUIO9(1)	F1	FLASH.A[11](0)	F2	FLASH.A[10](0)	F3	FLASH.A[25]
F4	FLASH.A[20]	F5	FLASH.A[12](0)	F6	V_{SS}	F7	SDRAM.A[2]
F8	SDRAM.A[10]	F9	SDRAM.A[9]	F10	LCD.AC(0)/ SYS_CLK_OUT(1)/ Z_STATE†(2)	F11	LCD.P[9](0)/ Z_STATE†(1)/ GPIO30(7)
F12	V_{SS}	F13	KB.R[4](0)/ MPUIO15(1)	F14	KB.C[0](0)/ MPUIO0(1)	F15	KB.R[0](0)/ MPUIO8(1)
F16	MCBSP1.CLKX(0)/ GPIO54(7)	F17	KB.C[5](0)/ GPIO28(7)	G1	DV_{DD5}	G2	FLASH.A[15](0)
G3	FLASH.A[13](0)	G4	FLASH.A[14](0)	G5	FLASH.A[16](0)	G6	FLASH.A[17]
G7	V_{SS}	G8	CV_{DD2}	G9	CV_{DD2}	G10	CV_{DD3}
G11	V_{SS}	G12	DV_{DD1}	G13	MCBSP1.CLKS(0)/ GPIO62(7)	G14	MCBSP1.DX(0)/ MCBSP1.FSX(1)/ MCBSP1.DXZ(2)/ GPIO52(7)
G15	MCBSP1.FSX(0)/ MCBSP1.DX(1)/ MCBSP1.DXZ(2) GPIO53(7)	G16	CAM.LCLK(0)/ ETM.CLK(1)/ UWIRE.SCLK(2)/ GPIO39(7)	G17	MCBSP1.DR(0)/ GPIO51(7)	H1	LDO.FILTER
H2	FLASH.A[22]	H3	FLASH.A[18]	H4	FLASH.A[19]	H5	FLASH.A[21]
H6	$\overline{\text{FLASH.ADV}}$	H7	CV_{DD2}	H8	V_{SS}#	H9	V_{SS}
H10	V_{SS}	H11	CV_{DD3}	H12	CAM.EXCLK(0)/ ETM.SYNC[0](1)/ UWIRE.SDO(2)/ LOW_STATE§ (6)/ GPIO57(7)	H13	CAM.D[3](0)/ ETM.D[3](1)/ UART3.RX(2)/ GPIO31(7)
H14	MPU_BOOT(0)/ USB1.SUSP(2)	H15	CAM.D[6](0)/ ETM.D[6](1)/ $\overline{\text{UWIRE.CS3}}$(2)/ MMC2.CMD/ GPIO34(7)	H16	CAM.D[7](0)/ ETM.D[7](1)/ $\overline{\text{UWIRE.CS0}}$(2)/ MMC2.DAT2(3)/ GPIO35(7)	H17	CAM.D[5](0)/ ETM.D[5](1)/ UWIRE.SDI(2)/ GPIO33(7)
J1	$\overline{\text{FLASH.BE[0]}}$(0)/ $\overline{\text{FLASH.CS2UOE}}$(1)/ GPIO59(7)	J2	FLASH.A[23]	J3	$\overline{\text{FLASH.CS1}}$(0)/ $\overline{\text{FLASH.CS1L}}$(1)	J4	FLASH.A[24]
J5	GPIO62(0)/ $\overline{\text{FLASH.CS0}}$(1)	J6	$\overline{\text{FLASH.CS3}}$(0)/ GPIO3(7)	J7	FLASH.D[3]	J8	$\overline{\text{FLASH.CS2}}$(0)/ $\overline{\text{FLASH.BAA}}$(1)/ $\overline{\text{FLASH.CS2L}}$(2)

† Z_STATE = high-impedance
‡ "NC" denotes "No Connect".
§ LOW_STATE = 0
¶ Signal must be tied low.
# For special consideration with respect to the connection of the V_{SS} pin (ZDY/GDY ball H8), refer to Section 5.5.1, 32-kHz Oscillator and Input Clock.

NOTES: 1. Shading denotes signals with multiplexed functions.
2. The number within parenthesis at the end of a signal name denotes the Pin Mux setting (see the MUX CTRL SETTING column in Table 2−3 and Table 2−4).

Table 2−1. ZDY/GDY Package Terminal Assignments (Continued)

ZDY/ GDY BALL NO.	SIGNAL	ZDY/ GDY BALL NO.	SIGNAL	ZDY/ GDY BALL NO.	SIGNAL	ZDY/ GDY BALL NO.	SIGNAL
J9	V_{SS}	J10	CV_{DD3}	J11	CAM.D[4](0)/ ETM.D[4](1)/ UART3.TX(2)/ GPIO32(7)	J12	CAM.HS(0)/ ETM.PSTAT[1](1)/ UART2.CTS(2)/ MMC2.DAT0/ GPIO38(7)
J13	CAM.VS(0)/ ETM.PSTAT[2](1)/ MPUIO14(2)/ MMC2.DAT1(3)	J14	CAM.D[2](0)/ ETM.D[2](1)/ UART3.CTS(2)/ GPIO30(7)	J15	DV_{DD8}	J16	CAM.D[1](0)/ ETM.D[1](1)/ UART3.RTS(2)/ GPIO29(7)
J17	CAM.D[0](0)/ ETM.D[0](1)/ MPUIO12(2)/ MMC2.DAT3(3)	K1	FLASH.CLK(0)/ $\overline{\text{FLASH.CS2UOE}}$(1)	K2	$\overline{\text{FLASH.BE[1]}}$(0)/ $\overline{\text{FLASH.CS2UWE}}$(1)/ GPIO60(7)	K3	$\overline{\text{FLASH.CS2U}}$(0)/ GPIO5(1)
K4	NC‡	K5	CV_{DD}	K6	FLASH.D[6]	K7	FLASH.D[12]
K8	V_{SS}	K9	V_{SS}	K10	V_{SS}	K11	CV_{DD3}
K12	CAM.RSTZ(0)/ ETM.PSTAT[0](1)/ UART2.RTS(2)/ MMC2.CLK(3)/ LOW_STATE§(6)/ GPIO37(7)	K13	GPIO11(0)/ HDQ(1)/ ETM.PSTAT[5](5)/ RTDX.D[3](7)	K14	GPIO14(0)/ KB.R[6](1)/ LCD.RED0(2)/ Z_STATE†(3)	K15	UART3.RX(0)/ PWL(1)/ UART2.RX(3)/ TIMER.PWM1(4)/ GPIO49(7)
K16	GPIO15(0)/ KB.R[7](1)/ TIMER.PWM2(2)	K17	LOW_STATE§(0)/ UART3.TX(1)/ PWT(2)/ UART2.TX(4) TIMER.PWM0(5)/ GPIO50(7)	L1	FLASH.D[0]	L2	FLASH.D[2]
L3	DV_{DD5}	L4	FLASH.D[5]	L5	FLASH.D[8]	L6	FLASH.RDY(0)/ GPIO10(1)
L7	V_{SS}	L8	MCBSP2.DR(0)/ MCBSP2.DX(1)/ MCBSP2.DXZ(2)/ GPIO22(7)	L9	CV_{DDRTC}	L10	BCLK(0)/ UART3.RTS(1)/ CAM.OUTCLK(6)/ GPIO17(7)
L11	V_{SS}	L12	MPUIO2(0)/ $\overline{\text{EXT_DMA_REQ0}}$(1)/ $\overline{\text{UWIRE.CS1}}$(2)/ $\overline{\text{SPIF.CS1}}$(6)	L13	GPIO3(0)/ MCBSP3.FSX(2)/ LED1(3)/ ETM.PSTAT[3](5)/ RTDX.D[1](7)	L14	GPIO6(0)/ MCBSP3.FSX(2)/ TIMER.EVENT3(3)/ MCSI1.DIN(4)/ TMS(5)

† Z_STATE = high-impedance
‡ "NC" denotes "No Connect".
§ LOW_STATE = 0
¶ Signal must be tied low.
# For special consideration with respect to the connection of the V_{SS} pin (ZDY/GDY ball H8), refer to Section 5.5.1, 32-kHz Oscillator and Input Clock.

NOTES: 1. Shading denotes signals with multiplexed functions.
2. The number within parenthesis at the end of a signal name denotes the Pin Mux setting (see the MUX CTRL SETTING column in Table 2−3 and Table 2−4).

Table 2−1. ZDY/GDY Package Terminal Assignments (Continued)

ZDY/ GDY BALL NO.	SIGNAL	ZDY/ GDY BALL NO.	SIGNAL	ZDY/ GDY BALL NO.	SIGNAL	ZDY/ GDY BALL NO.	SIGNAL
L15	GPIO7(0)/ MMC.DAT2(1)/ TCK(3)/ MCSI1.CLK(4)/ ETM.SYNC[1](5)/ RTDX.D[2](7)	L16	GPIO12(0)/ MCBSP3.FSX(1)/ TIMER.EXTCLK(3)	L17	GPIO13(0)/ KB.R[5](1)/ LCD.BLUE0(2)/ Z_STATE†(3)	M1	FLASH.D[1]
M2	FLASH.D[4]	M3	FLASH.D[11]	M4	FLASH.D[10]	M5	$\overline{\text{FLASH.OE}}$
M6	V_{SS}	M7	CV_{DD}	M8	MMC.CLK(0)/ GPIO57(7)	M9	UART1.CTS(0)/ UART1.IRSEL(2)/ GPIO38(7)
M10	TMS	M11	I2C.SDA(0)/ GPIO48(7)	M12	V_{SS}	M13	DV_{DD9}
M14	MPUIO4(0)/ $\overline{\text{EXT\_DMA\_REQ1}}$(1)/ LED2(2)/ $\overline{\text{UWIRE.CS2}}$(3)/ $\overline{\text{SPIF.CS2}}$(4)/ MCBSP3.DR(6)	M15	GPIO1(0)/ UART3.RTS(1)	M16	GPIO2(0)/ ETM.PSTAT[4](5)/ RTDX.D[0] (7)	M17	GPIO4(0)/ SPI.CS2(1)/ MCBSP3.FSX(2)/ TIMER.EVENT4(3)/ SPIF.DIN(4)
N1	FLASH.D[7]	N2	FLASH.D[9]	N3	$\overline{\text{FLASH.RP}}$(0)/ $\overline{\text{FLASH.CS2UWE}}$(1)	N4	FLASH.D[15]
N5	V_{SS}	N6	MCBSP2.FSX(0)/ GPIO21(7)	N7	MMC.CMD/ GPIO55(7)	N8	$\overline{\text{PWRON\_RESET}}$
N9	RTC_WAKE_INT(0)/ USB1.SE0(4)/ RST_HOST_OUT(5)/ GPIO55(7)	N10	MCSI1.SYNC(0)/ MCBSP3.DR(1)/ USB1.VP(2)/ MCBSP3.FSX(4)	N11	EMU1	N12	$\overline{\text{RST\_OUT}}$(0)/ GPIO41(7)
N13	V_{SS}	N14	$\overline{\text{MPU\_RST}}$(0)/ MPUIO14(6)	N15	MPUIO1(0)/ RTCK(1)/ SPIF.SCK(6)	N16	MPUIO5(0)/ LOW_PWR(1)/ UART3.RTS(3)/ UART1.DTR(4)
N17	GPIO0(0)/ USB.VBUS(2)/ SPIF.DOUT(3)/ MMC2.CLKIN(6)	P1	FLASH.D[13]	P2	OSC1_OUT	P3	$\overline{\text{FLASH.WE}}$

† Z_STATE = high-impedance
‡ "NC" denotes "No Connect".
§ LOW_STATE = 0
¶ Signal must be tied low.
# For special consideration with respect to the connection of the V_{SS} pin (ZDY/GDY ball H8), refer to Section 5.5.1, 32-kHz Oscillator and Input Clock.

NOTES: 1. Shading denotes signals with multiplexed functions.
2. The number within parenthesis at the end of a signal name denotes the Pin Mux setting (see the MUX CTRL SETTING column in Table 2−3 and Table 2−4).

Table 2−1. ZDY/GDY Package Terminal Assignments (Continued)

ZDY/ GDY BALL NO.	SIGNAL	ZDY/ GDY BALL NO.	SIGNAL	ZDY/ GDY BALL NO.	SIGNAL	ZDY/ GDY BALL NO.	SIGNAL
P4	USB.PUEN(0)/ USB.CLKO(1)/ USB.PUDIS(3)/ Z_STATE†(4)/ $\overline{\text{LOW\_POWER}}$(6)/ GPIO58(7)	P5	UART2.BCLK(0)/ SYS_CLK_IN(6)	P6	UART2.CTS(0)/ USB2.RCV(1)/ GPIO7(2)/ USB0.RCV(5)	P7	GPIO8(0)/ $\overline{\text{TRST}}$(3)/ MCSI1.DOUT(4)/ MMC2.CMD
P8	MCSI2.CLK(0)/ USB2.SUSP(1)/ USB0.SUSP(5)/ MMC2.CLK(6)/ GPIO27(7)	P9	MMC.DAT3(0)/ MPUIO9(1)/ MPUIO6(2)	P10	$\overline{\text{RTC\_ON\_NOFF}}$(0)	P11	MCSI1.DOUT(0)/ USB1.TXD(1)/ TDO(3)/ MCBSP3.DX(4)/ GPIO18(7)/ MCBSP3.DOUT_HIZ
P12	MCSI1.DIN(0)/ USB1.RCV(1)/ EMU1(3)/ MCBSP3.DR(4)/ GPIO56(7)	P13	TCK	P14	UWIRE.SDI(0)/ UART3.DSR(1)/ UART1.DSR(2)/ MCBSP3.DR(3)/ SPIF.DIN(6)/ GPIO47(7)	P15	UWIRE.SCLK(0)/ KB.C[7](1)/ MPUIO1(2)/ UART3.CTS(4)
P16	I2C.SCL	P17	CV_{DDA}	R1	FLASH.D[14]	R2	OSC1_IN
R3	$\overline{\text{FLASH.WP}}$	R4	LOW_STATE§(0)/ UART2.TX(1)/ USB2.TXD(2)/ USB0.TXD(5)/ Z_STATE†(6)/ GPIO17(7)	R5	MCBSP2.FSR(0)/ GPIO12(1)	R6	MPUIO3(0)/ MMC2.DAT1(6)
R7	MCSI2.DIN(0)/ USB2.VP(1)/ USB0.VP(5)/ GPIO26(7)	R8	MMC.DAT0/ Z_STATE†(1)/ GPIO58(7)	R9	V_{SS}	R10	DV_{DDRTC}
R11	LOW_STATE§(0)/ UART1.RTS(1)/ UART1.IRSHDN(2)/ Z_STATE†(6)/ GPIO39(7)	R12	BCLKREQ(0)/ UART3.CTS(1)/ MMC2.DAT2(6)/ GPIO40(7)	R13	$\overline{\text{TRST}}$	R14	CONF¶

† Z_STATE = high-impedance
‡ "NC" denotes "No Connect".
§ LOW_STATE = 0
¶ Signal must be tied low.
# For special consideration with respect to the connection of the V_{SS} pin (ZDY/GDY ball H8), refer to Section 5.5.1, 32-kHz Oscillator and Input Clock.

NOTES: 1. Shading denotes signals with multiplexed functions.
2. The number within parenthesis at the end of a signal name denotes the Pin Mux setting (see the MUX CTRL SETTING column in Table 2−3 and Table 2−4).

Table 2−1. ZDY/GDY Package Terminal Assignments (Continued)

ZDY/ GDY BALL NO.	SIGNAL	ZDY/ GDY BALL NO.	SIGNAL	ZDY/ GDY BALL NO.	SIGNAL	ZDY/ GDY BALL NO.	SIGNAL
R15	UWIRE.SDO(0)/ UART3.DTR(1)/ UART1.DTR(2)/ MCBSP3.DX(3)/ UART3.RTS(4)/ MCBSP3.DXZ(5)/ SPIF.DOUT(6)/ GPIO46(7)	R16	Z_STATE†(0)/ UWIRE.CS3(1)/ KB.C[6](2)/ SPIF.CS3(3)/ UART3.RX(4)/ Z_STATE†(6)/ GPIO44(7)	R17	Z_STATE†(0)/ UWIRE.CS0(1)/ MCBSP3.CLKX(2)/ UART3.TX(4)/ SPIF.CS0(6)/ GPIO45(7)	T1	FLASH.CS1U(0)/ GPIO16(7)
T2	USB.DP(0)/ I2C.SDA(4) UART1.RX(5)/ USB.PUEN(7)	T3	CV_{DD1}	T4	LOW_STATE§(0)/ UART2.RTS(1)/ USB2.SE0(2)/ MPUIO5(3)/ MPUIO12(4)/ USB0.SE0(5)/ LOW_STATE§(6)	T5	MCBSP2.DX(0)/ MCBSP2.DR(1)/ MCBSP2.DXZ(2)/ GPIO19(7)
T6	DV_{DD3}	T7	MCLKREQ(0)/ EXT_MASTER_REQ(1)/ UART2.RX(2)/ MMC2.DAT3(6)/ GPIO23(7)	T8	MCSI2.DOUT(0)/ USB2.TXEN(1)/ USB0.TXEN(5)/ Z_STATE†(6)/ GPIO25(7)	T9	MMC.DAT2(0)/ Z_STATE†(1)/ MPUIO11(2)
T10	DV_{DD6}	T11	CLK32K_IN	T12	LOW_STATE§(0)/ UART1.TX(1)/ UART1.IRTX(2)	T13	DV_{DD7}
T14	RTCK	T15	TDO	T16	CV_{DD}	T17	BFAIL/EXT_FIQ(0)/ UART3.CTS(1)/ UART1.DSR(2)/ MMC.DATDIR1(6)
U1	USB.DM(0)/ I2C.SCL(4)/ UART1.TX(5)/ Z_STATE†(7)	U2	DV_{DD2}	U3	MCLK(0)/ MMC2.DATDIR0(6)/ GPIO24(7)	U4	UART2.RX(0)/ USB2.VM(1)/ USB0.VM(5)/ GPIO18(7)
U5	MCBSP2.CLKX(0)/ GPIO20(7)	U6	MCBSP2.CLKR(0)/ GPIO11(1)	U7	GPIO9(0)/ EMU0(3)/ MCSI1.SYNC(4)/ MMC2.DAT0	U8	MCSI2.SYNC(0)/ GIOP7(1)/ USB2.SPEED(2)/ USB0.SPEED(5)/ MMC2.CMDDIR(6)

† Z_STATE = high-impedance
‡ "NC" denotes "No Connect".
§ LOW_STATE = 0
¶ Signal must be tied low.
# For special consideration with respect to the connection of the V_{SS} pin (ZDY/GDY ball H8), refer to Section 5.5.1, 32-kHz Oscillator and Input Clock.

NOTES: 1. Shading denotes signals with multiplexed functions.
2. The number within parenthesis at the end of a signal name denotes the Pin Mux setting (see the MUX CTRL SETTING column in Table 2−3 and Table 2−4).

Table 2−1. ZDY/GDY Package Terminal Assignments (Continued)

ZDY/ GDY BALL NO.	SIGNAL	ZDY/ GDY BALL NO.	SIGNAL	ZDY/ GDY BALL NO.	SIGNAL	ZDY/ GDY BALL NO.	SIGNAL
U9	MMC.DAT1(0)/ MPUIO10(1)/ MPUIO7(2)	U10	OSC32K_OUT	U11	OSC32K_IN	U12	CLK32K_OUT(0)/ MPUIO0(4)/ USB1.SPEED(5)/ UART1.TX(6)/ GPIO36(7)
U13	UART1.RX(0)/ UART1.IRRX(2)/ GPIO37(7)	U14	Z_STATE†(0)/ MCBSP3.CLKX(1)/ USB1.TXEN(2)/ MCSI1.DIN_OUT(3)/ MCSI1.DIN(4)/ Z_STATE†(6)/ GPIO42(7)	U15	MCSI1.CLK(0)/ MCBSP3.DX(1)/ USB1.VM(2)/ TDI(3)/ MCBSP3.CLKX(4)/ GPIO43(7)	U16	EMU0
U17	TDI						

† Z_STATE = high-impedance
‡ “NC” denotes “No Connect”.
§ LOW_STATE = 0
¶ Signal must be tied low.
# For special consideration with respect to the connection of the V_{SS} pin (ZDY/GDY ball H8), refer to Section 5.5.1, 32-kHz Oscillator and Input Clock.

NOTES: 1. Shading denotes signals with multiplexed functions.
2. The number within parenthesis at the end of a signal name denotes the Pin Mux setting (see the MUX CTRL SETTING column in Table 2−3 and Table 2−4).

Table 2−2. ZZG Package Terminal Assignments

ZZG BALL NO.	SIGNAL	ZZG BALL NO.	SIGNAL	ZZG BALL NO.	SIGNAL	ZZG BALL NO.	SIGNAL
A1	SDRAM.A[3]	A2	SDRAM.A[0]	A3	CV_{DD2}	A5	DV_{DD4}
A7	DV_{DD4}	A9	CV_{DD2}	A11	CV_{DDDLL}	A13	V_{SS}
A15	CV_{DD}	A17	LCD.P[13](0)/ Z_STATE†(1)/ GPIO34(7)	A19	DV_{DD1}	A20	LCD.P[5](0)/ Z_STATE†(1)
A21	V_{SS}	B1	V_{SS}	B2	SDRAM.A[1]	B3	SDRAM.BA[0]
B4	$\overline{\text{SDRAM.CAS}}$	B5	V_{SS}	B6	SDRAM.A[2]	B7	V_{SS}
B8	SDRAM.A[10]	B9	SDRAM.A[5]	B10	DV_{DD4}	B12	SDRAM.A[9]
B13	CV_{DD3}	B14	DV_{DD4}	B15	LCD.AC(0)/ SYS_CLK_OUT(1)/ Z_STATE†(2)	B16	V_{SS}
B17	LCD.P[11](0)/ Z_STATE†(1)/ GPIO32(7)	B18	LCD.VS(0)/ Z_STATE†(1)	B19	LCD.P[6](0)/ Z_STATE†(1)	B20	CV_{DD3}
B21	LCD.P[1](0)/ Z_STATE†(1)	C1	FLASH.A[3](0)	C2	DV_{DD5}	C3	SDRAM.BA[1]
C4	SDRAM.D[6]	C5	SDRAM.D[2]	C6	SDRAM.D[1]	C7	SDRAM.D[5]
C8	SDRAM.DQML	C9	SDRAM.CLK	C10	SDRAM.D[8]	C11	SDRAM.D[12]
C12	SDRAM.D[15]	C13	SDRAM.D[11]	C14	SDRAM.DQSH	C15	LCD.PCLK(0)/ Z_STATE†(1)
C16	LCD.P[14](0)/ Z_STATE†(1)/ GPIO35(7)	C17	LCD.P[10](0)/ Z_STATE†(1)/ GPIO31(7)	C18	LCD.P[7](0)/ Z_STATE†(1)	C19	LCD.P[2](0)/ Z_STATE†(1)
C20	LCD.HS(0)/ Z_STATE†(1)	C21	KB.C[4](0)/ GPIO27(7)	D2	FLASH.A[5](0)	D3	FLASH.A[2](0)
D4	SDRAM.DQSL	D5	SDRAM.D[4]	D6	SDRAM.D[0]	D7	SDRAM.D[3]
D8	SDRAM.D[7]	D9	SDRAM.CLKX	D10	SDRAM.DQMU	D11	SDRAM.D[10]
D12	SDRAM.D[14]	D13	SDRAM.D[13]	D14	SDRAM.D[9]	D15	LCD.P[15](0)/ Z_STATE†(1)/ GPIO2(7)
D16	LCD.P[9](0)/ Z_STATE†(1)/ GPIO30(7)	D17	LCD.P[8](0)/ Z_STATE†(1)/ GPIO29(7)	D18	LCD.P[0](0)/ Z_STATE†(1)	D19	KB.C[2](0)/ GPIO61(7)
D20	KB.C[1](0)/ MPUIO6(1)	E1	FLASH.A[25]	E2	CV_{DD2}	E3	FLASH.A[7](0)
E4	FLASH.A[4](0)	E5	NC‡	E18	KB.C[3](0)/ GPIO63(6)	E19	KB.R[4](0)/ MPUIO15(1)

† Z_STATE = high-impedance
‡ "NC" denotes "No Connect".
§ LOW_STATE = 0
¶ Signal must be tied low.
# For special consideration with respect to the connection of the V_{SS} pin (ZZG ball Y13), refer to Section 5.5.1, 32-kHz Oscillator and Input Clock.

NOTES: 1. Shading denotes signals with multiplexed functions.
2. The number within parenthesis at the end of a signal name denotes the Pin Mux setting (see the MUX CTRL SETTING column in Table 2−3 and Table 2−4).

Table 2−2. ZZG Package Terminal Assignments (Continued)

ZZG BALL NO.	SIGNAL	ZZG BALL NO.	SIGNAL	ZZG BALL NO.	SIGNAL	ZZG BALL NO.	SIGNAL
E20	KB.R[3](0)/ MPUIO13(1)	E21	DV_{DD1}	F2	FLASH.A[20]	F3	FLASH.A[9](0)
F4	FLASH.A[6](0)	F18	KB.C[0](0)/ MPUIO0(1)	F19	KB.R[1](0)/ MPUIO9(1)	F20	V_{SS}
G1	V_{SS}	G2	FLASH.A[12](0)	G3	FLASH.A[11](0)	G4	FLASH.A[10](0)
G8	$\overline{\text{SDRAM.CS}}$	G9	SDRAM.A[8]	G10	SDRAM.A[4]	G11	SDRAM.A[7]
G12	SDRAM.A[6]	G13	LCD.P[12](0)/ Z_STATE†(1)/ GPIO33(7)	G14	LCD.P[3](0)/ Z_STATE†(1)	G18	KB.R[0](0)/ MPUIO8(1)
G19	KB.C[5](0)/ GPIO28(7)	G20	MCBSP1.CLKS(0)/ GPIO62(7)	G21	MCBSP1.CLKX(0)/ GPIO54(7)	H2	DV_{DD5}
H3	FLASH.A[15](0)	H4	FLASH.A[14](0)	H7	$\overline{\text{SDRAM.RAS}}$	H8	$\overline{\text{SDRAM.WE}}$
H9	SDRAM.A[12]	H10	SDRAM.A[11]	H11	SDRAM.A[13]	H12	SDRAM.CKE
H13	LCD.P[4](0)/ Z_STATE†(1)	H14	KB.R[2[(0)/ MPUIO10(1)	H15	MCBSP1.FSX(0)/ MCBSP1.DX(1)/ MCBSP1.DXZ(2) GPIO53(7)	H18	MCBSP1.DX(0)/ MCBSP1.FSX(1)/ MCBSP1.DXZ(2)/ GPIO52(7)
H19	CAM.EXCLK(0)/ ETM.SYNC[0](1)/ UWIRE.SDO(2)/ LOW_STATE§(6)/ GPIO57(7)	H20	MCBSP1.DR(0)/ GPIO51(7)	J1	LDO.FILTER	J2	FLASH.A[17]
J3	FLASH.A[19]	J4	FLASH.A[18]	J7	FLASH.A[8](0)	J8	FLASH.A[1](0)
J14	CAM.D[5](0)/ ETM.D[5](1)/ UWIRE.SDI(2)/ GPIO33(7)	J15	CAM.LCLK(0)/ ETM.CLK(1)/ UWIRE.SCLK(2)/ GPIO39(7)	J18	CAM.D[7](0)/ ETM.D[7](1)/ $\overline{\text{UWIRE.CS0}}$(2)/ MMC2.DAT2(3)/ GPIO35(7)	J19	CAM.D[6](0)/ ETM.D[6](1)/ $\overline{\text{UWIRE.CS3}}$(2)/ MMC2.CMD/ GPIO34(7)
J20	MPU_BOOT(0)/ USB1.SUSP(2)	J21	CV_{DD3}	K2	V_{SS}	K3	FLASH.A[23]
K4	FLASH.A[22]	K7	FLASH.A[16](0)	K8	FLASH.A[13](0)	K14	CAM.D[1](0)/ ETM.D[1](1)/ UART3.RTS(2)/ GPIO29(7)
K15	CAM.D[2](0)/ ETM.D[2](1)/ UART3.CTS(2)/ GPIO30(7)	K18	CAM.D[4](0)/ ETM.D[4](1)/ UART3.TX(2)/ GPIO32(7)	K19	CAM.D[3](0)/ ETM.D[3](1)/ UART3.RX(2)/ GPIO31(7)	K20	V_{SS}

† Z_STATE = high-impedance
‡ “NC” denotes “No Connect”.
§ LOW_STATE = 0
¶ Signal must be tied low.
# For special consideration with respect to the connection of the V_{SS} pin (ZZG ball Y13), refer to Section 5.5.1, 32-kHz Oscillator and Input Clock.

NOTES: 1. Shading denotes signals with multiplexed functions.
2. The number within parenthesis at the end of a signal name denotes the Pin Mux setting (see the MUX CTRL SETTING column in Table 2−3 and Table 2−4).

Table 2−2. ZZG Package Terminal Assignments (Continued)

ZZG BALL NO.	SIGNAL	ZZG BALL NO.	SIGNAL	ZZG BALL NO.	SIGNAL	ZZG BALL NO.	SIGNAL
L1	NC‡	L3	$\overline{\text{FLASH.BE[0]}}$(0)/ $\overline{\text{FLASH.CS2UOE}}$(1)/ GPIO59(7)	L4	$\overline{\text{FLASH.ADV}}$	L7	FLASH.A[24]
L8	FLASH.A[21]	L14	UART3.RX(0)/ PWL(1)/ UART2.RX(3)/ TIMER.PWM1(4)/ GPIO49(7)	L15	CAM.HS(0)/ ETM.PSTAT[1](1)/ UART2.CTS(2)/ MMC2.DAT0/ GPIO38(7)	L18	CAM.VS(0)/ ETM.PSTAT[2](1)/ MPUIO14(2)/ MMC2.DAT1(3)
L19	CAM.D[0](0)/ ETM.D[0](1)/ MPUIO12(2)/ MMC2.DAT3(3)	L21	DV_{DD8}	M2	CV_{DD}	M3	$\overline{\text{FLASH.CS1}}$(0)/ $\overline{\text{FLASH.CS1L}}$(1)
M4	$\overline{\text{FLASH.CS2}}$(0)/ $\overline{\text{FLASH.BAA}}$(1)/ $\overline{\text{FLASH.CS2L}}$(2)	M7	GPIO62(0)/ $\overline{\text{FLASH.CS0}}$(1)	M8	$\overline{\text{FLASH.BE[1]}}$(0)/ $\overline{\text{FLASH.CS2UWE}}$(1)/ GPIO60(7)	M14	GPIO2(0)/ ETM.PSTAT[4](5)/ RTDX.D[0] (7)
M15	GPIO7(0)/ MMC.DAT2(1)/ TCK(3)/ MCSI1.CLK(4)/ ETM.SYNC[1](5)/ RTDX.D[2](7)	M18	LOW_STATE§(0)/ UART3.TX(1)/ PWT(2)/ UART2.TX(4) TIMER.PWM0(5)/ GPIO50(7)	M19	CAM.RSTZ(0)/ ETM.PSTAT[0](1)/ UART2.RTS(2)/ MMC2.CLK(3)/ LOW_STATE§(6)/ GPIO37(7)	M20	GPIO15(0)/ KB.R[7](1)/ TIMER.PWM2(2)
N1	V_{SS}	N2	FLASH.D[1]	N3	FLASH.CLK(0)/ $\overline{\text{FLASH.CS2UOE}}$(1)	N4	FLASH.D[0]
N7	FLASH.D[2]	N8	$\overline{\text{FLASH.CS3}}$(0)/ GPIO3(7)	N14	Z_STATE†(0)/ $\overline{\text{UWIRE.CS0}}$(1)/ MCBSP3.CLKX(2)/ UART3.TX(4)/ $\overline{\text{SPIF.CS0}}$(6)/ GPIO45(7)	N15	MPUIO2(0)/ $\overline{\text{EXT_DMA_REQ0}}$(1)/ $\overline{\text{UWIRE.CS1}}$(2)/ $\overline{\text{SPIF.CS1}}$(6)
N18	GPIO12(0)/ MCBSP3.FSX(1)/ TIMER.EXTCLK(3)	N19	GPIO13(0)/ KB.R[5](1)/ LCD.BLUE0(2)/ Z_STATE†(3)	N20	GPIO11(0)/ HDQ(1)/ ETM.PSTAT[5](5)/ RTDX.D[3](7)	N21	GPIO14(0)/ KB.R[6](1)/ LCD.RED0(2)/ Z_STATE†(3)
P2	FLASH.D[3]	P3	$\overline{\text{FLASH.CS2U}}$(0)/ GPIO5(1)	P4	FLASH.D[4]	P7	FLASH.D[5]
P8	FLASH.D[11]	P9	USB.DP(0)/ I2C.SDA(4) UART1.RX(5)/ USB.PUEN(7)	P10	MCBSP2.DR(0)/ MCBSP2.DX(1)/ MCBSP2.DXZ(2)/ GPIO22(7)	P11	MMC.CMD/ GPIO55(7)

† Z_STATE = high-impedance
‡ "NC" denotes "No Connect".
§ LOW_STATE = 0
¶ Signal must be tied low.
# For special consideration with respect to the connection of the V_{SS} pin (ZZG ball Y13), refer to Section 5.5.1, 32-kHz Oscillator and Input Clock.
NOTES: 1. Shading denotes signals with multiplexed functions.
2. The number within parenthesis at the end of a signal name denotes the Pin Mux setting (see the MUX CTRL SETTING column in Table 2−3 and Table 2−4).

Table 2−2. ZZG Package Terminal Assignments (Continued)

ZZG BALL NO.	SIGNAL	ZZG BALL NO.	SIGNAL	ZZG BALL NO.	SIGNAL	ZZG BALL NO.	SIGNAL
P12	V_{SS}	P13	CLK32K_IN	P14	MCSI1.CLK(0)/ MCBSP3.DX(1)/ USB1.VM(2)/ TDI(3)/ MCBSP3.CLKX(4)/ GPIO43(7)	P15	Z_STATE†(0)/ UWIRE.CS3(1)/ KB.C[6](2)/ SPIF.CS3(3)/ UART3.RX(4)/ Z_STATE†(6)/ GPIO44(7)
P18	GPIO3(0)/ MCBSP3.FSX(2)/ LED1(3)/ ETM.PSTAT[3](5)/ RTDX.D[1](7)	P19	GPIO6(0)/ MCBSP3.FSX(2)/ TIMER.EVENT3(3)/ MCSI1.DIN(4)/ TMS(5)	P20	GPIO4(0)/ SPI.CS2(1)/ MCBSP3.FSX(2)/ TIMER.EVENT4(3)/ SPIF.DIN(4)	R1	DV_{DD5}
R2	FLASH.D[6]	R3	FLASH.D[7]	R4	FLASH.D[8]	R8	USB.DM(0)/ I2C.SCL(4)/ UART1.TX(5)/ Z_STATE†(7)
R9	UART2.RX(0)/ USB2.VM(1)/ USB0.VM(5)/ GPIO18(7)	R10	MCLKREQ(0)/ EXT_MASTER_REQ(1)/ UART2.RX(2)/ MMC2.DAT3(6)/ GPIO23(7)	R11	MMC.DAT0/ Z_STATE†(1)/ GPIO58(7)	R12	PWRON_RESET
R13	CLK32K_OUT(0)/ MPUIO0(4)/ USB1.SPEED(5)/ UART1.TX(6)/ GPIO36(7)	R14	UART1.CTS(0)/ UART1.IRSEL(2)/ GPIO38(7)	R18	GPIO0(0)/ USB.VBUS(2)/ SPIF.DOUT(3)/ MMC2.CLKIN(6)	R19	GPIO1(0)/ UART3.RTS(1)
R20	CV_{DD3}	R21	V_{SS}	T2	FLASH.D[9]	T3	FLASH.D[10]
T4	FLASH.D[14]	T18	I2C.SCL	T19	MPUIO4(0)/ EXT_DMA_REQ1(1)/ LED2(2)/ UWIRE.CS2(3)/ SPIF.CS2(4)/ MCBSP3.DR(6)	T20	MPUIO5(0)/ LOW_PWR(1)/ UART3.RTS(3)/ UART1.DTR(4)
U1	FLASH.D[12]	U2	V_{SS}	U3	FLASH.D[13]	U4	FLASH.OE
U18	UWIRE.SDI(0)/ UART3.DSR(1)/ UART1.DSR(2)/ MCBSP3.DR(3)/ SPIF.DIN(6)/ GPIO47(7)	U19	MPUIO1(0)/ RTCK(1)/ SPIF.SCK(6)	U20	MPU_RST(0)/ MPUIO14(6)	U21	DV_{DD9}

† Z_STATE = high-impedance
‡ “NC” denotes “No Connect”.
§ LOW_STATE = 0
¶ Signal must be tied low.
# For special consideration with respect to the connection of the V_{SS} pin (ZZG ball Y13), refer to Section 5.5.1, 32-kHz Oscillator and Input Clock.

NOTES: 1. Shading denotes signals with multiplexed functions.
2. The number within parenthesis at the end of a signal name denotes the Pin Mux setting (see the MUX CTRL SETTING column in Table 2−3 and Table 2−4).

Table 2−2. ZZG Package Terminal Assignments (Continued)

ZZG BALL NO.	SIGNAL	ZZG BALL NO.	SIGNAL	ZZG BALL NO.	SIGNAL	ZZG BALL NO.	SIGNAL
V2	FLASH.RDY(0)/ GPIO10(1)	V3	FLASH.D[15]	V4	$\overline{\text{FLASH.WP}}$	V5	MCLK(0)/ MMC2.DATDIR0(6)/ GPIO24(7)
V6	LOW_STATE§(0)/ UART2.TX(1)/ USB2.TXD(2)/ USB0.TXD(5)/ Z_STATE†(6)/ GPIO17(7)	V7	MCBSP2.CLKR(0)/ GPIO11(1)	V8	MPUIO3(0)/ MMC2.DAT1(6)	V9	MCSI2.SYNC(0)/ GIOP7(1)/ USB2.SPEED(2)/ USB0.SPEED(5)/ MMC2.CMDDIR(6)
V10	MMC.DAT1(0)/ MPUIO10(1)/ MPUIO7(2)	V11	MMC.CLK(0)/ GPIO57(7)	V12	DV_{DDRTC}	V13	OSC32K_IN
V14	UART1.RX(0)/ UART1.IRRX(2)/ GPIO37(7)	V15	MCSI1.DIN(0)/ USB1.RCV(1)/ EMU1(3)/ MCBSP3.DR(4)/ GPIO56(7)	V16	EMU0	V17	TMS
V18	CONF¶	V19	UWIRE.SCLK(0)/ KB.C[7](1)/ MPUIO1(2)/ UART3.CTS(4)	V20	I2C.SDA(0)/ GPIO48(7)	W1	$\overline{\text{FLASH.RP}}$(0)/ $\overline{\text{FLASH.CS2UWE}}$(1)
W2	$\overline{\text{FLASH.WE}}$	W3	OSC1_OUT	W4	USB.PUEN(0)/ USB.CLKO(1)/ USB.PUDIS(3)/ Z_STATE†(4)/ $\overline{\text{LOW_POWER}}$(6)/ GPIO58(7)	W5	LOW_STATE§(0)/ UART2.RTS(1)/ USB2.SE0(2)/ MPUIO5(3)/ MPUIO12(4)/ USB0.SE0(5)/ LOW_STATE§(6)
W6	MCBSP2.FSR(0)/ GPIO12(1)	W7	MCBSP2.FSX(0)/ GPIO21(7)	W8	GPIO9(0)/ EMU0(3)/ MCSI1.SYNC(4)/ MMC2.DAT0	W9	MCSI2.DOUT(0)/ USB2.TXEN(1)/ USB0.TXEN(5)/ Z_STATE†(6)/ GPIO25(7)
W10	MMC.DAT2(0)/ Z_STATE†(1)/ MPUIO11(2)	W11	MMC.DAT3(0)/ MPUIO9(1)/ MPUIO6(2)	W12	CV_{DDRTC}	W13	RTC_WAKE_INT(0)/ USB1.SE0(4)/ RST_HOST_OUT(5)/ GPIO55(7)

† Z_STATE = high-impedance
‡ "NC" denotes "No Connect".
§ LOW_STATE = 0
¶ Signal must be tied low.
# For special consideration with respect to the connection of the V_{SS} pin (ZZG ball Y13), refer to Section 5.5.1, 32-kHz Oscillator and Input Clock.

NOTES: 1. Shading denotes signals with multiplexed functions.
2. The number within parenthesis at the end of a signal name denotes the Pin Mux setting (see the MUX CTRL SETTING column in Table 2−3 and Table 2−4).

Table 2−2. ZZG Package Terminal Assignments (Continued)

ZZG BALL NO.	SIGNAL	ZZG BALL NO.	SIGNAL	ZZG BALL NO.	SIGNAL	ZZG BALL NO.	SIGNAL
W14	MCSI1.DOUT(0)/ USB1.TXD(1)/ TDO(3)/ MCBSP3.DX(4)/ GPIO18(7)/ MCBSP3.DOUT_HIZ	W15	BCLKREQ(0)/ UART3.CTS(1)/ MMC2.DAT2(6)/ GPIO40(7)	W16	Z_STATE†(0)/ MCBSP3.CLKX(1)/ USB1.TXEN(2)/ MCSI1.DIN_OUT(3)/ MCSI1.DIN(4)/ Z_STATE†(6)/ GPIO42(7)	W17	EMU1
W18	TCK	W19	BFAIL/$\overline{\text{EXT\_FIQ}}$(0)/ UART3.CTS(1)/ UART1.DSR(2)/ MMC.DATDIR1(6)	W20	V_{SS}	W21	UWIRE.SDO(0)/ UART3.DTR(1)/ UART1.DTR(2)/ MCBSP3.DX(3)/ UART3.RTS(4)/ MCBSP3.DXZ(5)/ SPIF.DOUT(6)/ GPIO46(7)
Y1	$\overline{\text{FLASH.CS1U}}$(0)/ GPIO16(7)	Y2	OSC1_IN	Y3	V_{SS}	Y4	UART2.BCLK(0)/ SYS_CLK_IN(6)
Y5	UART2.CTS(0)/ USB2.RCV(1)/ GPIO7(2)/ USB0.RCV(5)	Y6	MCBSP2.CLKX(0)/ GPIO20(7)	Y7	DV_{DD3}	Y8	GPIO8(0)/ $\overline{\text{TRST}}$(3)/ MCSI1.DOUT(4)/ MMC2.CMD
Y9	CV_{DD}	Y10	MCSI2.CLK(0)/ USB2.SUSP(1)/ USB0.SUSP(5)/ MMC2.CLK(6)/ GPIO27(7)	Y12	$\overline{\text{RTC\_ON\_NOFF}}$(0)	Y13	V_{SS}#
Y14	LOW_STATE§(0)/ UART1.TX(1)/ UART1.IRTX(2)	Y15	BCLK(0)/ UART3.RTS(1)/ CAM.OUTCLK(6)/ GPIO17(7)	Y16	DV_{DD7}	Y17	RTCK
Y18	$\overline{\text{TRST}}$	Y19	TDI	Y20	CV_{DD}	Y21	CV_{DDA}
AA1	V_{SS}	AA2	DV_{DD2}	AA3	CV_{DD1}	AA5	MCBSP2.DX(0)/ MCBSP2.DR(1)/ MCBSP2.DXZ(2)/ GPIO19(7)
AA7	V_{SS}	AA9	MCSI2.DIN(0)/ USB2.VP(1)/ USB0.VP(5)/ GPIO26(7)	AA11	DV_{DD6}	AA13	OSC32K_OUT

† Z_STATE = high-impedance
‡ “NC” denotes “No Connect”.
§ LOW_STATE = 0
¶ Signal must be tied low.
# For special consideration with respect to the connection of the V_{SS} pin (ZZG ball Y13), refer to Section 5.5.1, 32-kHz Oscillator and Input Clock.
NOTES: 1. Shading denotes signals with multiplexed functions.
2. The number within parenthesis at the end of a signal name denotes the Pin Mux setting (see the MUX CTRL SETTING column in Table 2−3 and Table 2−4).

Table 2−2. ZZG Package Terminal Assignments (Continued)

ZZG BALL NO.	SIGNAL	ZZG BALL NO.	SIGNAL	ZZG BALL NO.	SIGNAL	ZZG BALL NO.	SIGNAL
AA15	LOW_STATE§(0)/ UART1.RTS(1)/ UART1.IRSHDN(2)/ Z_STATE†(6)/ GPIO39(7)	AA17	MCSI1.SYNC(0)/ MCBSP3.DR(1)/ USB1.VP(2)/ MCBSP3.FSX(4)	AA19	TDO	AA20	$\overline{\text{RST\_OUT}}$(0)/ GPIO41(7)
AA21	V_{SS}						

† Z_STATE = high-impedance
‡ “NC” denotes “No Connect”.
§ LOW_STATE = 0
¶ Signal must be tied low.
# For special consideration with respect to the connection of the V_{SS} pin (ZZG ball Y13), refer to Section 5.5.1, 32-kHz Oscillator and Input Clock.
NOTES: 1. Shading denotes signals with multiplexed functions.
2. The number within parenthesis at the end of a signal name denotes the Pin Mux setting (see the MUX CTRL SETTING column in Table 2−3 and Table 2−4).

2.3 Terminal Characteristics and Multiplexing

Table 2−3 describes terminal characteristics and the signals multiplexed on each ball for the ZDY/GDY package. Table 2−4 describes terminal characteristics and the signals multiplexed on each ball for the ZZG package. The table column headers are explained below:

- **BALL NO.:** The package ball number.
- **SIGNAL NAME:** The names of all the signals that are multiplexed on each ball.
- **TYPE:** The signal direction.
- **MUX CTRL SETTING:** Shows control of multiplexing modes.
- **PULLUP/PULLDN:** Denotes the presence of an internal pullup or pulldown. Pullups and pulldowns can be enabled or disabled via software.
- **BUFFER STRENGTH:** Drive strength of the associated output buffer.
- **OTHER:** Contains various terminal information, such as buffer type, boundary scan capability, and gating/inhibit functionality.
- **RESET STATE:** The state of the terminal at reset.
- **SUPPLY:** The voltage supply which powers the terminal's I/O buffers.

NOTE: Care must be taken to avoid assigning multiple balls to the same signal. Violations may cause unexpected results.

Table 2−3. ZDY/GDY Package Terminal Characteristics

ZDY/ GDY BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING (see Notes 3 and 4)	PULLUP/ PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
E7	$\overline{\text{SDRAM.CS}}$	O	NA		2 mA (Lv) 3 mA (Hv)	A	1	DV_{DD4}
A12	SDRAM.DQSH	I/O	NA		2 mA (Lv) 3 mA (Hv)	A, K	0	DV_{DD4}
A2	SDRAM.DQSL	I/O	NA		2 mA (Lv) 3 mA (Hv)	A, K	0	DV_{DD4}
D5	$\overline{\text{SDRAM.CAS}}$	O	NA		2 mA (Lv) 3 mA (Hv)	A	1	DV_{DD4}
D4	$\overline{\text{SDRAM.RAS}}$	O	NA		2 mA (Lv) 3 mA (Hv)	A	1	DV_{DD4}

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20-µA internal pulldown, PD100=100-µA internal pulldown, PU20 = 20-µA internal pullup, PU100 = 100-µA internal pullup. Pullup or pulldown can be enabled or disabled by software.

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVCMOS input/output
B = SUBLVDS input/ouput
C = USB transceiver input/ouput
D = I^2C input/output buffers
E = Analog oscillator terminals
F = Boundary-scannable terminal
G1 = Terminal may be gated by BFAIL
G2 = Terminal may be gated by GPIO9 and MPUIO3
G3 = Terminal my be gated by BFAIL and OMAP5912 Internal Reset
H1 = Terminal may be 3-stated by BFAIL input
H3 = MCSI1.DOUT pin can be forced into a high-impedance state by the OMAP5912 HIGH_IMP3 control bit
K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

‖ Slew time constraint of the $\overline{\text{EXT\_DMA\_REQ1}}$ must be lower than or equal to 10 ns (from 10% to 90% of DV_{DD}) in Mode 1.

☆Slew time constraint of the $\overline{\text{EXT\_DMA\_REQ0}}$ must be lower than or equal to 10 ns (from 10% to 90% of DV_{DD}) in Mode 1.

NOTES: 3. NA denotes no multiplexing on the ball
4. 'Regx' denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

Table 2−3. ZDY/GDY Package Terminal Characteristics (Continued)

ZDY/ GDY BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING (see Notes 3 and 4)	PULLUP/ PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
C7	SDRAM.DQML	O	NA		2 mA (Lv) 3 mA (Hv)	A, K	0	DV_{DD4}
A8	SDRAM.DQMU	O	NA		2 mA (Lv) 3 mA (Hv)	A, K	0	DV_{DD4}
E6	$\overline{\text{SDRAM.WE}}$	O	NA		2 mA (Lv) 3 mA (Hv)	A	1	DV_{DD4}
D10 E8 E9 F8 F9 C6 A10 E10 C8 D9 C3 F7 A1 B2	SDRAM.A[13:0]	O	NA		2 mA (Lv) 3 mA (Hv)	A	0	DV_{DD4}
C4 C5	SDRAM.BA[1:0]	O	NA		2 mA (Lv) 3 mA (Hv)	A	0	DV_{DD4}
B10 C10 B11 B9 A11 B8 B12 C9 B7 A3 B6 B3 A5 A4 B5 B4	SDRAM.D[15:0]	I/O	NA		2 mA (Lv) 3 mA (Hv)	A, K	0	DV_{DD4}
A7	SDRAM.CLK	O	NA		2 mA (Lv) 3 mA (Hv)	A, K	U	DV_{DD4}
A6	SDRAM.CLKX	O	NA		2 mA (Lv) 3 mA (Hv)	A, K	0	DV_{DD4}
B13	SDRAM.CKE	O	NA		2 mA (Lv) 3 mA (Hv)	A	1	DV_{DD4}

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20-µA internal pulldown, PD100=100-µA internal pulldown, PU20 = 20-µA internal pullup, PU100 = 100-µA internal pullup. Pullup or pulldown can be enabled or disabled by software.

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVCMOS input/output
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G1 = Terminal may be gated by BFAIL
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G3 = Terminal my be gated by BFAIL and OMAP5912 Internal Reset
H1 = Terminal may be 3-stated by BFAIL input
H3 = MCSI1.DOUT pin can be forced into a high-impedance state by the OMAP5912 HIGH_IMP3 control bit
K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

‖ Slew time constraint of the $\overline{\text{EXT\_DMA\_REQ1}}$ must be lower than or equal to 10 ns (from 10% to 90% of DV_{DD}) in Mode 1.

☆Slew time constraint of the $\overline{\text{EXT\_DMA\_REQ0}}$ must be lower than or equal to 10 ns (from 10% to 90% of DV_{DD}) in Mode 1.

NOTES: 3. NA denotes no multiplexing on the ball
4. ‘Regx’ denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

Table 2−3. ZDY/GDY Package Terminal Characteristics (Continued)

ZDY/ GDY BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING (see Notes 3 and 4)	PULLUP/ PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
F10	LCD.AC	O	RegD[11:9] = 000		2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD1}
	SYS_CLK_OUT	O	RegD[11:9] = 001					
	Z_STATE	Z	RegD[11:9] = 010					
A14	LCD.PCLK	O	RegD[17:15] = 000		2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD1}
	Z_STATE	Z	RegD[17:15] = 001					
C12	LCD.P[15]	O	RegD[20:18] = 000		2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD1}
	Z_STATE	Z	RegD[20:18] = 001					
	GPIO2	I/O	RegD[20:18] = 111					
D12	LCD.P[14]	O	RegD[23:21] = 000		2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD1}
	Z_STATE	Z	RegD[23:21] = 001					
	GPIO35	I/O	RegD[23:21] = 111					
E11	LCD.P[13]	O	RegD[26:24] = 000		2 mA (Lv) 3 mA (Hv)	F, A, G1	0	DV_{DD1}
	Z_STATE	Z	RegD[26:24] = 001					
	GPIO34	I/O	RegD[26:24] = 111					
A13	LCD.P[12]	O	RegD[29:27] = 000		2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD1}
	Z_STATE	Z	RegD[29:27] = 001					
	GPIO33	I/O	RegD[29:27] = 111					
B14	LCD.P[11]	O	RegE[2:0] = 000		2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD1}
	Z_STATE	Z	RegE[2:0] = 001					
	GPIO32	I/O	RegE[2:0] = 111					
A15	LCD.P[10]	O	RegE[5:3] = 000		2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD1}
	Z_STATE	Z	RegE[5:3] = 001					
	GPIO31	I/O	RegE[5:3] = 111					
F11	LCD.P[9]	O	RegE[8:6] = 000		2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD1}
	Z_STATE	Z	RegE[8:6] = 001					
	GPIO30	I/O	RegE[8:6] = 111					
B15	LCD.VS	O	RegE[11:9] = 000		2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD1}
	Z_STATE	Z	RegE[11:9] = 001					

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20-µA internal pulldown, PD100=100-µA internal pulldown, PU20 = 20-µA internal pullup, PU100 = 100-µA internal pullup. Pullup or pulldown can be enabled or disabled by software.

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVCMOS input/output
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H3 = MCSI1.DOUT pin can be forced into a high-impedance state by the OMAP5912 HIGH_IMP3 control bit
K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

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☆Slew time constraint of the $\overline{\text{EXT\_DMA\_REQ0}}$ must be lower than or equal to 10 ns (from 10% to 90% of DV_{DD}) in Mode 1.

NOTES: 3. NA denotes no multiplexing on the ball
4. 'Regx' denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

Table 2−3. ZDY/GDY Package Terminal Characteristics (Continued)

ZDY/ GDY BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING (see Notes 3 and 4)	PULLUP/ PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
C13	LCD.P[8] Z_STATE GPIO29	O Z I/O	RegE[14:12] = 000 RegE[14:12] = 001 RegE[14:12] = 111		2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD1}
D13	LCD.P[7] Z_STATE	O Z	RegE[17:15] = 000 RegE[17:15] = 001		2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD1}
A16	LCD.P[6] Z_STATE	O Z	RegE[20:18] = 000 RegE[20:18] = 001		2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD1}
C15	LCD.P[5] Z_STATE	O Z	RegE[23:21] = 000 RegE[23:21] = 001		2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD1}
E12	LCD.P[4] Z_STATE	O Z	RegE[26:24] = 000 RegE[26:24] = 001		2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD1}
D14	LCD.P[3] Z_STATE	O Z	RegE[29:27] = 000 RegE[29:27] = 001		2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD1}
C16	LCD.P[2] Z_STATE	O Z	RegF[2:0] = 000 RegF[2:0] = 001		2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD1}
B16	LCD.P[1] Z_STATE	O Z	RegF[5:3] = 000 RegF[5:3] = 001		2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD1}
A17	LCD.P[0] Z_STATE	O Z	RegF[8:6] = 000 RegF[8:6] = 001		2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD1}
D15	LCD.HS Z_STATE	O Z	RegD[14:12] = 000 RegD[14:12] = 001		2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD1}
D16	KB.C[4] GPIO27	O I/O	Reg3[5:3] = 000 Reg3[5:3] = 111	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	0	DV_{DD1}
E15	KB.C[3] GPIO63	O I/O	Reg3[8:6] = 000 Reg3[8:6] = 110	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	0	DV_{DD1}
B17	KB.C[2] GPIO61	O I/O	Reg3[11:9] = 000 Reg3[11:9] = 111	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	0	DV_{DD1}
C17	KB.C[1] MPUIO6	O I/O	Reg3[14:12] = 000 Reg3[14:12] = 001	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	0	DV_{DD1}

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20-µA internal pulldown, PD100=100-µA internal pulldown, PU20 = 20-µA internal pullup, PU100 = 100-µA internal pullup. Pullup or pulldown can be enabled or disabled by software.

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¶ A = Standard LVCMOS input/output
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G3 = Terminal my be gated by BFAIL and OMAP5912 Internal Reset
H1 = Terminal may be 3-stated by BFAIL input
H3 = MCSI1.DOUT pin can be forced into a high-impedance state by the OMAP5912 HIGH_IMP3 control bit
K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

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☆Slew time constraint of the $\overline{\text{EXT\_DMA\_REQ0}}$ must be lower than or equal to 10 ns (from 10% to 90% of DV_{DD}) in Mode 1.

NOTES: 3. NA denotes no multiplexing on the ball
4. ‘Regx’ denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

Table 2−3. ZDY/GDY Package Terminal Characteristics (Continued)

ZDY/ GDY BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING (see Notes 3 and 4)	PULLUP/ PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
F14	KB.C[0] MPUIO0	O I/O	Reg3[17:15] = 000 Reg3[17:15] = 001	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	0	DV_{DD1}
F13	KB.R[4] MPUIO15	I I/O	Reg3[20:18] = 000 Reg3[20:18] = 001	PU100, PD20	2 mA (Lv) 3 mA (Hv)	A, F	Z	DV_{DD1}
D17	KB.R[3] MPUIO13	I I/O	Reg3[23:21] = 000 Reg3[23:21] = 001	PU100, PD20	2 mA (Lv) 3 mA (Hv)	A, F	Z	DV_{DD1}
E16	KB.R[2] MPUIO10	I I/O	Reg3[26:24] = 000 Reg3[26:24] = 001	PU100, PD20	2 mA (Lv) 3 mA (Hv)	A, F	Z	DV_{DD1}
E17	KB.R[1] MPUIO9	I I/O	Reg3[29:27] = 000 Reg3[29:27] = 001	PU100, PD20	2 mA (Lv) 3 mA (Hv)	A, F	Z	DV_{DD1}
F15	KB.R[0] MPUIO8	I I/O	Reg4[2:0] = 000 Reg4[2:0] = 001	PU100, PD20	2 mA (Lv) 3 mA (Hv)	A, F	Z	DV_{DD1}
F17	KB.C[5] GPIO28	O I/O	Reg3[2:0] = 000 Reg3[2:0] = 111	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	0	DV_{DD1}
G13	MCBSP1.CLKS GPIO62	I I/O	Reg4[8:6] = 000 Reg4[8:6] = 111	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	−	DV_{DD1}
F16	MCBSP1.CLKX GPIO54	I/O I/O	Reg4[11:9] = 000 Reg4[11:9] = 111	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	Z	DV_{DD1}
G15	MCBSP1.FSX MCBSP1.DX MCBSP1.DXZ GPIO53	I/O O O/Z I/O	Reg4[14:12] = 000 Reg4[14:12] = 001 Reg4[14:12] = 010 Reg4[14:12] = 111	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	Z	DV_{DD1}
G14	MCBSP1.DX MCBSP1.ESX MCBSP1.DXZ GPIO52	O I/O O/Z I/O	Reg4[17:15] = 000 Reg4[17:15] = 001 Reg4[17:15] = 010 Reg4[17:15] = 111	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD1}
G17	MCBSP1.DR GPIO51	I I/O	Reg4[20:18] = 000 Reg4[20:18] = 111	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	LZ	DV_{DD1}

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20-µA internal pulldown, PD100=100-µA internal pulldown, PU20 = 20-µA internal pullup, PU100 = 100-µA internal pullup. Pullup or pulldown can be enabled or disabled by software.

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K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

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NOTES: 3. NA denotes no multiplexing on the ball
4. ‘Regx’ denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

Table 2−3. ZDY/GDY Package Terminal Characteristics (Continued)

ZDY/ GDY BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING (see Notes 3 and 4)	PULLUP/ PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
H12	CAM.EXCLK	O	Reg4[23:21] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD8}
	ETM.SYNC[0]	O	Reg4[23:21] = 001					
	UWIRE.SDO	O	Reg4[23:21] = 010					
	LOW_STATE	O	Reg4[23:21] = 110					
	GPIO57	I/O	Reg4[23:21] = 111					
G16	CAM.LCLK	I	Reg4[26:24] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	Z	DV_{DD8}
	ETM.CLK	O	Reg4[26:24] = 001					
	UWIRE.SCLK	O	Reg4[26:24] = 010					
	GPIO39	I/O	Reg4[26:24] = 111					
H14	MPU_BOOT	I	Reg8[29:27] = 000		2 mA (Lv) 3 mA (Hv)	A, F	−	DV_{DD8}
	USB1.SUSP	O	Reg8[29:27] = 010					
H16	CAM.D[7]	I	Reg4[29:27] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	Z	DV_{DD8}
	ETM.D[7]	O	Reg4[29:27] = 001					
	$\overline{\text{UWIRE.CS0}}$	O	Reg4[29:27] = 010					
	MMC2.DAT2	I/O	Reg4[29:27] = 011					
	GPIO35	I/O	Reg4[29:27] = 111					
H15	CAM.D[6]	I	Reg5[2:0] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	Z	DV_{DD8}
	ETM.D[6]	O	Reg5[2:0] = 001					
	$\overline{\text{UWIRE.CS3}}$	O	Reg5[2:0] = 010					
	MMC2.CMD	I/O	Reg5[2:0] = 011					
	GPIO34	I/O	Reg5[2:0] = 111					
H17	CAM.D[5]	I	Reg5[5:3] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	Z	DV_{DD8}
	ETM.D[5]	O	Reg5[5:3] = 001					
	UWIRE.SDI	I	Reg5[5:3] = 010					
	GPIO33	I/O	Reg5[5:3] = 111					
J11	CAM.D[4]	I	Reg5[8:6] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	Z	DV_{DD8}
	ETM.D[4]	O	Reg5[8:6] = 001					
	UART3.TX	O	Reg5[8:6] = 010					
	GPIO32	I/O	Reg5[8:6] = 111					

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20-µA internal pulldown, PD100=100-µA internal pulldown, PU20 = 20-µA internal pullup, PU100 = 100-µA internal pullup. Pullup or pulldown can be enabled or disabled by software.

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NOTES: 3. NA denotes no multiplexing on the ball
4. ‘Regx’ denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

Table 2−3. ZDY/GDY Package Terminal Characteristics (Continued)

ZDY/ GDY BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING (see Notes 3 and 4)	PULLUP/ PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
H13	CAM.D[3]	I	Reg5[11:9] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	Z	DV_{DD8}
	ETM.D[3]	O	Reg5[11:9] = 001					
	UART3.RX	I	Reg5[11:9] = 010					
	GPIO31	I/O	Reg5[11:9] = 111					
J14	CAM.D[2]	I	Reg5[14:12] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	Z	DV_{DD8}
	ETM.D[2]	O	Reg5[14:12] = 001					
	UART3.CTS	I	Reg5[14:12] = 010					
	GPIO30	I/O	Reg5[14:12] = 111					
J16	CAM.D[1]	I	Reg5[17:15] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	Z	DV_{DD8}
	ETM.D[1]	O	Reg5[17:15] = 001					
	UART3.RTS	O	Reg5[17:15] = 010					
	GPIO29	I/O	Reg5[17:15] = 111					
J17	CAM.D[0]	I	Reg5[20:18] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	Z	DV_{DD8}
	ETM.D[0]	O	Reg5[20:18] = 001					
	MPUIO12	I/O	Reg5[20:18] = 010					
	MMC2.DAT3	I/O	Reg5[20:18] = 011					
J13	CAM.VS	I	Reg5[23:21] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	Z	DV_{DD8}
	ETM.PSTAT[2]	O	Reg5[23:21] = 001					
	MPUIO14	I/O	Reg5[23:21] = 010					
	MMC2.DAT1	I/O	Reg5[23:21] = 011					
J12	CAM.HS	I	Reg5[26:24] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	Z	DV_{DD8}
	ETM.PSTAT[1]	O	Reg5[26:24] = 001					
	UART2.CTS	I	Reg5[26:24] = 010					
	MMC2.DAT0	I/O	Reg5[26:24] = 011					
	GPIO38	I/O	Reg5[26:24] = 111					

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20-µA internal pulldown, PD100=100-µA internal pulldown, PU20 = 20-µA internal pullup, PU100 = 100-µA internal pullup. Pullup or pulldown can be enabled or disabled by software.

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NOTES: 3. NA denotes no multiplexing on the ball
4. ‘Regx’ denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

Table 2−3. ZDY/GDY Package Terminal Characteristics (Continued)

ZDY/ GDY BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING (see Notes 3 and 4)	PULLUP/ PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
K12	CAM.RSTZ	O	Reg5[29:27] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD8}
	ETM.PSTAT[0]	O	Reg5[29:27] = 001					
	UART2.RTS	O	Reg5[29:27] = 010					
	MMC2.CLK	O	Reg5[29:27] = 011					
	LOW_STATE	O	Reg5[29:27] = 110					
	GPIO37	I/O	Reg5[29:27] = 111					
K17	LOW_STATE	O	Reg6[2:0] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD9}
	UART3.TX	O	Reg6[2:0] = 001					
	PWT	O	Reg6[2:0] = 010					
	UART2.TX	O	Reg6[2:0] = 100					
	TIMER.PWM0	O	Reg6[2:0] = 101					
	GPIO50	I/O	Reg6[2:0] = 111					
K15	UART3.RX	I	Reg6[5:3] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	−	DV_{DD9}
	PWL	O	Reg6[5:3] = 001					
	UART2.RX	I	Reg6[5:3] = 011					
	TIMER.PWM1	O	Reg6[5:3] = 100					
	GPIO49	I/O	Reg6[5:3] = 111					
K16	GPIO15	I/O	Reg6[8:6] = 000	PU100, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	LZ	DV_{DD9}
	KB.R[7]	I	Reg6[8:6] = 001					
	TIMER.PWM2	O	Reg6[8:6] = 010					
K14	GPIO14	I/O	Reg6[11:9] = 000	PU100, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	LZ	DV_{DD9}
	KB.R[6]	I	Reg6[11:9] = 001					
	LCD.RED0	O	Reg6[11:9] = 010					
	Z_STATE	Z	Reg6[11:9] = 011					
L17	GPIO13	I/O	Reg6[14:12] = 000	PU100, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	LZ	DV_{DD9}
	KB.R[5]	I	Reg6[14:12] = 001					
	LCD.BLUE0	O	Reg6[14:12] = 010					
	Z_STATE	Z	Reg6[14:12] = 011					

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20-µA internal pulldown, PD100=100-µA internal pulldown, PU20 = 20-µA internal pullup, PU100 = 100-µA internal pullup. Pullup or pulldown can be enabled or disabled by software.

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVCMOS input/output
B = SUBLVDS input/ouput
C = USB transceiver input/ouput
D = I^2C input/output buffers
E = Analog oscillator terminals
F = Boundary-scannable terminal
G1 = Terminal may be gated by BFAIL
G2 = Terminal may be gated by GPIO9 and MPUIO3
G3 = Terminal my be gated by BFAIL and OMAP5912 Internal Reset
H1 = Terminal may be 3-stated by BFAIL input
H3 = MCSI1.DOUT pin can be forced into a high-impedance state by the OMAP5912 HIGH_IMP3 control bit
K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

‖ Slew time constraint of the $\overline{\text{EXT\_DMA\_REQ1}}$ must be lower than or equal to 10 ns (from 10% to 90% of DV_{DD}) in Mode 1.

☆Slew time constraint of the $\overline{\text{EXT\_DMA\_REQ0}}$ must be lower than or equal to 10 ns (from 10% to 90% of DV_{DD}) in Mode 1.

NOTES: 3. NA denotes no multiplexing on the ball
4. ‘Regx’ denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

Table 2−3. ZDY/GDY Package Terminal Characteristics (Continued)

ZDY/ GDY BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING (see Notes 3 and 4)	PULLUP/ PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
L16	GPIO12	I/O	Reg6[17:15] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	LZ	DV_{DD9}
	MCBSP3.FSX	I/O	Reg6[17:15] = 001					
	TIMER.EXTCLK	I	Reg6[17:15] = 011					
K13	GPIO11	I/O	Reg6[20:18] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	LZ	DV_{DD9}
	HDQ	I/O	Reg6[20:18] = 001					
	ETM.PSTAT[5]	O	Reg6[20:18] = 101					
	RTDX.D[3]	I/O	Reg6[20:18] = 111					
L15	GPIO7	I/O	Reg6[23:21] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	LZ	DV_{DD9}
	MMC.DAT2	I/O	Reg6[23:21] = 001					
	TCK	I	Reg6[23:21] = 011					
	MCSI1.CLK	I/O	Reg6[23:21] = 100					
	ETM.SYNC[1]	O	Reg6[23:21] = 101					
	RTDX.D[2]	I/O	Reg6[23:21] = 111					
L14	GPIO6	I/O	Reg6[26:24] = 000	PD100, PU20	2 mA (Lv) 3 mA (Hv)	A, F, G1	LZ	DV_{DD9}
	MCBSP3.FSX	I/O	Reg6[26:24] = 010					
	TIMER.EVENT3	I	Reg6[26:24] = 011					
	MCSI1.DIN	I	Reg6[26:24] = 100					
	TMS	I	Reg6[26:24] = 101					
M17	GPIO4	I/O	Reg6[29:27] = 000	PD100, PU20	2 mA (Lv) 3 mA (Hv)	A, F, G1	LZ	DV_{DD9}
	MCBSP3.FSX	I/O	Reg6[29:27] = 010					
	TIMER.EVENT4	I	Reg6[29:27] = 011					
	SPIF.DIN	I	Reg6[29:27] = 100					
L13	GPIO3	I/O	Reg7[2:0] = 000	PU100, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	LZ	DV_{DD9}
	MCBSP3.FSX	I/O	Reg7[2:0] = 010					
	LED1	O	Reg7[2:0] = 011					
	ETM.PSTAT[3]	O	Reg7[2:0] = 101					
M16	GPIO2	I/O	Reg7[5:3] = 000	PU100, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	LZ	DV_{DD9}
	ETM.PSTAT[4]	O	Reg7[5:3] = 101					
	RTDX.D[0]	I/O	Reg7[5:3] = 111					

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20-µA internal pulldown, PD100=100-µA internal pulldown, PU20 = 20-µA internal pullup, PU100 = 100-µA internal pullup. Pullup or pulldown can be enabled or disabled by software.

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVCMOS input/output
B = SUBLVDS input/ouput
C = USB transceiver input/ouput
D = I^2C input/output buffers
E = Analog oscillator terminals
F = Boundary-scannable terminal
G1 = Terminal may be gated by BFAIL
G2 = Terminal may be gated by GPIO9 and MPUIO3
G3 = Terminal my be gated by BFAIL and OMAP5912 Internal Reset
H1 = Terminal may be 3-stated by BFAIL input
H3 = MCSI1.DOUT pin can be forced into a high-impedance state by the OMAP5912 HIGH_IMP3 control bit
K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

‖ Slew time constraint of the $\overline{\text{EXT\_DMA\_REQ1}}$ must be lower than or equal to 10 ns (from 10% to 90% of DV_{DD}) in Mode 1.

☆Slew time constraint of the $\overline{\text{EXT\_DMA\_REQ0}}$ must be lower than or equal to 10 ns (from 10% to 90% of DV_{DD}) in Mode 1.

NOTES: 3. NA denotes no multiplexing on the ball
4. ‘Regx’ denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

Table 2−3. ZDY/GDY Package Terminal Characteristics (Continued)

ZDY/ GDY BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING (see Notes 3 and 4)	PULLUP/ PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
M15	GPIO1	I/O	Reg7[8:6] = 000	PU100, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	LZ	DV_{DD9}
	UART3.RTS	O	Reg7[8:6] = 001					
N17	GPIO0	I/O	Reg7[11:9] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	LZ	DV_{DD9}
	USB.VBUS	I	Reg7[11:9] = 010					
	SPIF.DOUT	O	Reg7[11:9] = 011					
	MMC2.CLKIN	I	Reg7[11:9] = 110					
N16	MPUIO5	I/O	Reg7[14:12] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	LZ	DV_{DD9}
	LOW_PWR	O	Reg7[14:12] = 001					
	UART3.RTS	O	Reg7[14:12] = 011					
	UART1.DTR	O	Reg7[14:12] = 100					
M14	MPUIO4	I/O	Reg7[17:15] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	LZ	DV_{DD9}
	$\overline{\text{EXT\_DMA\_REQ1}}$‖	I	Reg7[17:15] = 001					
	LED2	O	Reg7[17:15] = 010					
	$\overline{\text{UWIRE.CS2}}$	O	Reg7[17:15] = 011					
	$\overline{\text{SPIF.CS2}}$	O	Reg7[17:15] = 100					
	MCBSP3.DR	I	Reg7[17:15] = 110					
L12	MPUIO2	I/O	Reg7[20:18] = 000	PU100, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	LZ	DV_{DD9}
	$\overline{\text{EXT\_DMA\_REQ0}}$☆	I	Reg7[20:18] = 001					
	$\overline{\text{UWIRE.CS1}}$	O	Reg7[20:18] = 010					
	$\overline{\text{SPIF.CS1}}$	O	Reg7[20:18] = 110					
N14	$\overline{\text{MPU\_RST}}$	I	Reg9[8:6] = 000		2 mA (Lv) 3 mA (Hv)	A, F	−	DV_{DD9}
	MPUIO14	I/O	Reg9[8:6] = 110					
N15	MPUIO1	I/O	Reg7[23:21] = 000	PU100, PD20	2 mA (Lv) 3 mA (Hv)	A, F	Z	DV_{DD9}
	RTCK	I/O	Reg7[23:21] = 001					
	SPIF.SCK	I/O	Reg7[23:21] = 110					
P16	I2C.SCL	I/O/Z	Reg7[26:24] = 000		2 mA (Lv) 3 mA (Hv)	D	Z	DV_{DD9}
M11	I2C.SDA	I/O/Z	Reg7[29:27] = 000		2 mA (Lv) 3 mA (Hv)	D	Z	DV_{DD9}
	GPIO48	I	Reg7[29:27] = 111					

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20-µA internal pulldown, PD100=100-µA internal pulldown, PU20 = 20-µA internal pullup, PU100 = 100-µA internal pullup. Pullup or pulldown can be enabled or disabled by software.

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVCMOS input/output
B = SUBLVDS input/ouput
C = USB transceiver input/ouput
D = I^2C input/output buffers
E = Analog oscillator terminals
F = Boundary-scannable terminal
G1 = Terminal may be gated by BFAIL
G2 = Terminal may be gated by GPIO9 and MPUIO3
G3 = Terminal my be gated by BFAIL and OMAP5912 Internal Reset
H1 = Terminal may be 3-stated by BFAIL input
H3 = MCSI1.DOUT pin can be forced into a high-impedance state by the OMAP5912 HIGH_IMP3 control bit
K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

‖ Slew time constraint of the $\overline{\text{EXT\_DMA\_REQ1}}$ must be lower than or equal to 10 ns (from 10% to 90% of DV_{DD}) in Mode 1.

☆Slew time constraint of the $\overline{\text{EXT\_DMA\_REQ0}}$ must be lower than or equal to 10 ns (from 10% to 90% of DV_{DD}) in Mode 1.

NOTES: 3. NA denotes no multiplexing on the ball
4. ‘Regx’ denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

Table 2−3. ZDY/GDY Package Terminal Characteristics (Continued)

ZDY/ GDY BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING (see Notes 3 and 4)	PULLUP/ PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
P14	UWIRE.SDI	I	Reg8[2:0] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	LZ	DV_{DD9}
	UART3.DSR	O	Reg8[2:0] = 001					
	UART1.DSR	I	Reg8[2:0] = 010					
	MCBSP3.DR	I	Reg8[2:0] = 011					
	SPIF.DIN	I/O	Reg8[2:0] = 110					
	GPIO47	I/O	Reg8[2:0] = 111					
R15	UWIRE.SDO	O	Reg8[5:3] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD9}
	UART3.DTR	O	Reg8[5:3] = 001					
	UART1.DTR	O	Reg8[5:3] = 010					
	MCBSP3.DX	O	Reg8[5:3] = 011					
	UART3.RTS	O	Reg8[5:3] = 100					
	MCBSP3.DXZ	O/Z	Reg8[5:3] = 101					
	SPIF.DOUT	I/O	Reg8[5:3] = 110					
	GPIO46	I/O	Reg8[5:3] = 111					
P15	UWIRE.SCLK	O	Reg8[8:6] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD9}
	KB.C[7]	O	Reg8[8:6] = 001					
	MPUIO1	I/O	Reg8[8:6] = 010					
	UART3.CTS	I	Reg8[8:6] = 100					
R17	Z_STATE	Z	Reg8[11:9] = 000	PU100, PD20	2 mA (Lv) 3 mA (Hv)	A, F	Z	DV_{DD9}
	$\overline{\text{UWIRE.CS0}}$	O	Reg8[11:9] = 001					
	MCBSP3.CLKX	I/O	Reg8[11:9] = 010					
	UART3.TX	O	Reg8[11:9] = 100					
	$\overline{\text{SPIF.CS0}}$	I/O	Reg8[11:9] = 110					
	GPIO45	I/O	Reg8[11:9] = 111					

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20-µA internal pulldown, PD100=100-µA internal pulldown, PU20 = 20-µA internal pullup, PU100 = 100-µA internal pullup. Pullup or pulldown can be enabled or disabled by software.

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVCMOS input/output
B = SUBLVDS input/ouput
C = USB transceiver input/ouput
D = I^2C input/output buffers
E = Analog oscillator terminals
F = Boundary-scannable terminal
G1 = Terminal may be gated by BFAIL
G2 = Terminal may be gated by GPIO9 and MPUIO3
G3 = Terminal my be gated by BFAIL and OMAP5912 Internal Reset
H1 = Terminal may be 3-stated by BFAIL input
H3 = MCSI1.DOUT pin can be forced into a high-impedance state by the OMAP5912 HIGH_IMP3 control bit
K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

‖ Slew time constraint of the $\overline{\text{EXT\_DMA\_REQ1}}$ must be lower than or equal to 10 ns (from 10% to 90% of DV_{DD}) in Mode 1.

☆Slew time constraint of the $\overline{\text{EXT\_DMA\_REQ0}}$ must be lower than or equal to 10 ns (from 10% to 90% of DV_{DD}) in Mode 1.

NOTES: 3. NA denotes no multiplexing on the ball
4. ‘Regx’ denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

Table 2−3. ZDY/GDY Package Terminal Characteristics (Continued)

ZDY/ GDY BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING (see Notes 3 and 4)	PULLUP/ PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
R16	Z_STATE	Z	Reg8[14:12] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	Z	DV_{DD9}
	$\overline{\text{UWIRE.CS3}}$	O	Reg8[14:12] = 001					
	KB.C[6]	O	Reg8[14:12] = 010					
	$\overline{\text{SPIF.CS3}}$	O	Reg8[14:12] = 011					
	UART3.RX	I	Reg8[14:12] = 100					
	Z_STATE	Z	Reg8[14:12] = 110					
	GPIO44	I/O	Reg8[14:12] = 111					
T17	BFAIL/$\overline{\text{EXT\_FIQ}}$	I	Reg8[17:15] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	Z	DV_{DD9}
	UART3.CTS	I	Reg8[17:15] = 001					
	UART1.DSR	I	Reg8[17:15] = 010					
	MMC2.DATDIR1	O	Reg8[17:15] = 110					
N12	$\overline{\text{RST\_OUT}}$	O	Reg9[11:9] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	0	DV_{DD9}
	GPIO41	I/O	Reg9[11:9] = 111					
R14	CONF	I	NA	PU20, PD20		A	LZ	DV_{DD9}
U17	TDI	I	NA	PD100, PU20		A	LZ	DV_{DD9}
T15	TDO	O	0		2 mA (Lv) 3 mA (Hv)		Z	DV_{DD9}
M10	TMS	I	NA	PD100, PU20		A	LZ	DV_{DD9}
P13	TCK	I	NA	PD100, PU20		A	LZ	DV_{DD9}
R13	$\overline{\text{TRST}}$	I	NA	PU20, PD20		A	−	DV_{DD9}
U16	EMU0	I/O	NA	PU100, PD20	2 mA (Lv) 3 mA (Hv)	A	Input	DV_{DD9}
N11	EMU1	I/O	NA	PU100, PD20	2 mA (Lv) 3 mA (Hv)	A	Input	DV_{DD9}
T14	RTCK	I/O	NA		2 mA (Lv) 3 mA (Hv)	A	−	DV_{DD9}

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20-µA internal pulldown, PD100=100-µA internal pulldown, PU20 = 20-µA internal pullup, PU100 = 100-µA internal pullup. Pullup or pulldown can be enabled or disabled by software.

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVCMOS input/output
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C = USB transceiver input/ouput
D = I^2C input/output buffers
E = Analog oscillator terminals
F = Boundary-scannable terminal
G1 = Terminal may be gated by BFAIL
G2 = Terminal may be gated by GPIO9 and MPUIO3
G3 = Terminal my be gated by BFAIL and OMAP5912 Internal Reset
H1 = Terminal may be 3-stated by BFAIL input
H3 = MCSI1.DOUT pin can be forced into a high-impedance state by the OMAP5912 HIGH_IMP3 control bit
K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

‖ Slew time constraint of the $\overline{\text{EXT\_DMA\_REQ1}}$ must be lower than or equal to 10 ns (from 10% to 90% of DV_{DD}) in Mode 1.

☆Slew time constraint of the $\overline{\text{EXT\_DMA\_REQ0}}$ must be lower than or equal to 10 ns (from 10% to 90% of DV_{DD}) in Mode 1.

NOTES: 3. NA denotes no multiplexing on the ball
4. 'Regx' denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

Table 2−3. ZDY/GDY Package Terminal Characteristics (Continued)

ZDY/ GDY BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING (see Notes 3 and 4)	PULLUP/ PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
N10	MCSI1.SYNC	I/O	RegA[5:3] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	LZ	DV_{DD7}
	MCBSP3.DR	I	RegA[5:3] = 001					
	USB1.VP	I	RegA[5:3] = 010					
	MCBSP3.FSX	I/O	RegA[5:3] = 100					
U15	MCSI1.CLK	I/O	RegA[8:6] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	LZ	DV_{DD7}
	MCBSP3.DX	O	RegA[8:6] = 001					
	USB1.VM	I	RegA[8:6] = 010					
	TDI	I	RegA[8:6] = 011					
	MCBSP3.CLKX	I/O	RegA[8:6] = 100					
	GPIO43	I/O	RegA[8:6] = 111					
U14	Z_STATE	Z	Reg9[5:3] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	Z	DV_{DD7}
	MCBSP3.CLKX	I/O	Reg9[5:3] = 001					
	USB1.TXEN	O	Reg9[5:3] = 010					
	MCSI1.DIN_OUT	O	Reg9[5:3] = 011					
	MCSI1.DIN	I	Reg9[5:3] = 100					
	Z_STATE	Z	Reg9[5:3] = 110					
	GPIO42	I/O	Reg9[5:3] = 111					
P12	MCSI1.DIN	I	RegA[11:9] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	Z	DV_{DD7}
	USB1.RCV	I	RegA[11:9] = 001					
	EMU1	I/O	RegA[11:9] = 011					
	MCBSP3.DR	I	RegA[11:9] = 100					
	GPIO56	I/O	RegA[11:9] = 111					
R12	BCLKREQ	I	Reg9[29:27] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	LZ	DV_{DD7}
	UART3.CTS	I	Reg9[29:27] = 001					
	MMC2.DAT2	I/O	Reg9[29:27] = 110					
	GPIO40	I/O	Reg9[29:27] = 111					

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20-µA internal pulldown, PD100=100-µA internal pulldown, PU20 = 20-µA internal pullup, PU100 = 100-µA internal pullup. Pullup or pulldown can be enabled or disabled by software.

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVCMOS input/output
B = SUBLVDS input/ouput
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G1 = Terminal may be gated by BFAIL
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G3 = Terminal my be gated by BFAIL and OMAP5912 Internal Reset
H1 = Terminal may be 3-stated by BFAIL input
H3 = MCSI1.DOUT pin can be forced into a high-impedance state by the OMAP5912 HIGH_IMP3 control bit
K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

‖ Slew time constraint of the $\overline{\text{EXT\_DMA\_REQ1}}$ must be lower than or equal to 10 ns (from 10% to 90% of DV_{DD}) in Mode 1.

☆Slew time constraint of the $\overline{\text{EXT\_DMA\_REQ0}}$ must be lower than or equal to 10 ns (from 10% to 90% of DV_{DD}) in Mode 1.

NOTES: 3. NA denotes no multiplexing on the ball
4. ‘Regx’ denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

Table 2−3. ZDY/GDY Package Terminal Characteristics (Continued)

ZDY/ GDY BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING (see Notes 3 and 4)	PULLUP/ PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
L10	BCLK	O	RegA[2:0] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD7}
	UART3.RTS	O	RegA[2:0] = 001					
	CAM.OUTCLK	O	RegA[2:0] = 110					
	GPIO17	I/O	RegA[2:0] = 111					
R11	LOW_STATE	O	Reg9[14:12] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD7}
	UART1.RTS	O	Reg9[14:12] = 001					
	UART1.IRSHDN	O	Reg9[14:12] = 010					
	Z_STATE	Z	Reg9[14:12] = 110					
	GPIO39	I/O	Reg9[14:12] = 111					
M9	UART1.CTS	I	Reg9[17:15] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	LZ	DV_{DD7}
	UART1.IRSEL	O	Reg9[17:15] = 010					
	GPIO38	I/O	Reg9[17:15] = 111					
U13	UART1.RX	I	Reg9[20:18] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	LZ	DV_{DD7}
	UART1.IRRX	I	Reg9[20:18] = 010					
	GPIO37	I/O	Reg9[20:18] = 111					
T12	LOW_STATE	O	Reg9[23:21] = 000		2 mA (Lv) 3 mA (Hv)	A, B, F, G1	0	DV_{DD7}
	UART1.TX	O	Reg9[23:21] = 001					
	UART1.IRTX	O	Reg9[23:21] = 010					
P11	MCSI1.DOUT	O	Reg9[26:24] = 000		2 mA (Lv) 3 mA (Hv)	A, B, F, G1, H3	0	DV_{DD7}
	USB1.TXD	O	Reg9[26:24] = 001					
	TDO	O	Reg9[26:24] = 011					
	MCBSP3.DX	O	Reg9[26:24] = 100					
	GPIO18	I/O	Reg9[26:24] = 111					
U12	CLK32K_OUT	O	RegA[14:12] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A	U	DV_{DDRTC}
	MPUIO0	I/O	RegA[14:12] = 100					
	USB1.SPEED	O	RegA[14:12] = 101					
	UART1.TX	O	RegA[14:12] = 110					
	GPIO36	I/O	RegA[14:12] = 111					
U11	OSC32K_IN	−	NA			E	NA	NA

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20-µA internal pulldown, PD100=100-µA internal pulldown, PU20 = 20-µA internal pullup, PU100 = 100-µA internal pullup. Pullup or pulldown can be enabled or disabled by software.

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVCMOS input/output
B = SUBLVDS input/ouput
C = USB transceiver input/ouput
D = I^2C input/output buffers
E = Analog oscillator terminals
F = Boundary-scannable terminal
G1 = Terminal may be gated by BFAIL
G2 = Terminal may be gated by GPIO9 and MPUIO3
G3 = Terminal my be gated by BFAIL and OMAP5912 Internal Reset
H1 = Terminal may be 3-stated by BFAIL input
H3 = MCSI1.DOUT pin can be forced into a high-impedance state by the OMAP5912 HIGH_IMP3 control bit
K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

‖ Slew time constraint of the $\overline{\text{EXT\_DMA\_REQ1}}$ must be lower than or equal to 10 ns (from 10% to 90% of DV_{DD}) in Mode 1.

☆Slew time constraint of the $\overline{\text{EXT\_DMA\_REQ0}}$ must be lower than or equal to 10 ns (from 10% to 90% of DV_{DD}) in Mode 1.

NOTES: 3. NA denotes no multiplexing on the ball
4. ‘Regx’ denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

Table 2−3. ZDY/GDY Package Terminal Characteristics (Continued)

ZDY/ GDY BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING (see Notes 3 and 4)	PULLUP/ PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
U10	OSC32K_OUT	−	NA			E	NA	NA
N9	RTC_WAKE_INT	O	Reg9[2:0] = 000		2 mA (Lv) 3 mA (Hv)	A, B	0	DV_{DDRTC}
	USB1.SE0	O	Reg9[2:0] = 100					
	RST_HOST_OUT	O	Reg9[2:0] = 101					
	GPIO55	I/O	Reg9[2:0] = 111					
P10	RTC_ON_NOFF	I	Reg8[20:18] = 000		2 mA (Lv) 3 mA (Hv)	A, B, G1	Z	DV_{DDRTC}
T11	CLK32K_IN	I	RegA[17:15] = 000			A	Input	DV_{DDRTC}
N8	$\overline{\text{PWRON\_RESET}}$	I	NA			A	Input	DV_{DDRTC}
P9	MMC.DAT3	I/O	Reg10[17:15] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	Z	DV_{DD6}
	MPUIO9	I/O	Reg10[17:15] = 001					
	MPUIO6	I/O	Reg10[17:15] = 010					
M8	MMC.CLK	O	RegA[23:21] = 000	PD100, PU20	2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD6}
	GPIO57	I/O	RegA[23:21] = 111					
R8	MMC.DAT0	I/O	RegB[2:0] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	Z	DV_{DD6}
	Z_STATE	Z	RegB[2:0] = 001					
	GPIO58	I/O	RegB[2:0] = 111					
T9	MMC.DAT2	I/O	RegA[20:18] = 000	PD100, PU20	2 mA (Lv) 3 mA (Hv)	A, F, G1	Z	DV_{DD6}
	Z_STATE	Z	RegA[20:18] = 001					
	MPUIO11	I/O	RegA[20:18] = 010					
U9	MMC.DAT1	I/O	RegA[26:24] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	Z	DV_{DD6}
	MPUIO10	I/O	RegA[26:24] = 001					
	MPUIO7	I/O	RegA[26:24] = 010					
N7	MMC.CMD	I/O	RegA[29:27] = 000	PD100, PU20	2 mA (Lv) 3 mA (Hv)	A, F, G1	Z	DV_{DD6}
	GPIO55	I/O	RegA[29:27] = 111					
P8	MCSI2.CLK	I/O	RegB[5:3] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	LZ	DV_{DD3}
	USB2.SUSP	O	RegB[5:3] = 001					
	USB0.SUSP	O	RegB[5:3] = 101					
	MMC2.CLK	O	RegB[5:3] = 110					
	GPIO27	I/O	RegB[5:3] = 111					

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20-µA internal pulldown, PD100=100-µA internal pulldown, PU20 = 20-µA internal pullup, PU100 = 100-µA internal pullup. Pullup or pulldown can be enabled or disabled by software.

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G3 = Terminal my be gated by BFAIL and OMAP5912 Internal Reset
H1 = Terminal may be 3-stated by BFAIL input
H3 = MCSI1.DOUT pin can be forced into a high-impedance state by the OMAP5912 HIGH_IMP3 control bit
K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

‖ Slew time constraint of the $\overline{\text{EXT\_DMA\_REQ1}}$ must be lower than or equal to 10 ns (from 10% to 90% of DV_{DD}) in Mode 1.

☆Slew time constraint of the $\overline{\text{EXT\_DMA\_REQ0}}$ must be lower than or equal to 10 ns (from 10% to 90% of DV_{DD}) in Mode 1.

NOTES: 3. NA denotes no multiplexing on the ball
4. 'Regx' denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

Table 2−3. ZDY/GDY Package Terminal Characteristics (Continued)

ZDY/ GDY BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING (see Notes 3 and 4)	PULLUP/ PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
R7	MCSI2.DIN	I	RegB[8:6] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	LZ	DV_{DD3}
	USB2.VP	I	RegB[8:6] = 001					
	USB0.VP	I	RegB[8:6] = 101					
	GPIO26	I/O	RegB[8:6] = 111					
T8	MCSI2.DOUT	O	RegB[11:9] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G2	0	DV_{DD3}
	USB2.TXEN	O	RegB[11:9] = 001					
	USB0.TXEN	O	RegB[11:9] = 101					
	Z_STATE	Z	RegB[11:9] = 110					
	GPIO25	I/O	RegB[11:9] = 111					
U8	MCSI2.SYNC	I/O	RegB[14:12] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	LZ	DV_{DD3}
	GPIO7	I/O	RegB[14:12] = 001					
	USB2.SPEED	O	RegB[14:12] = 010					
	USB0.SPEED	O	RegB[14:12] = 110					
	MMC2.CMDDIR	O	RegB[14:12] = 111					
T7	MCLKREQ	I	RegB[20:18] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	LZ	DV_{DD3}
	EXT_MASTER_REQ	O	RegB[20:18] = 001					
	UART2.RX	I	RegB[20:18] = 010					
	MMC2.DAT3	I/O	RegB[20:18] = 110					
	GPIO23	I/O	RegB[20:18] = 111					
U7	GPIO9	I/O	RegB[23:21] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G3	LZ	DV_{DD3}
	EMU0	I/O	RegB[23:21] = 011					
	MCSI1.SYNC	I/O	RegB[23:21] = 100					
	MMC2.DAT0	I/O	RegB[23:21] = 110					
P7	GPIO8	I/O	RegB[26:24] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G3	LZ	DV_{DD3}
	$\overline{TRST}$	I	RegB[26:24] = 011					
	MCSI1.DOUT	O	RegB[26:24] = 100					
	MMC2.CMD	I/O	RegB[26:24] = 110					
R6	MPUIO3	I/O	RegB[29:27] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	LZ	DV_{DD3}
	MMC2.DAT1	I/O	RegB[29:27] = 110					

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20-µA internal pulldown, PD100=100-µA internal pulldown, PU20 = 20-µA internal pullup, PU100 = 100-µA internal pullup. Pullup or pulldown can be enabled or disabled by software.

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H1 = Terminal may be 3-stated by BFAIL input
H3 = MCSI1.DOUT pin can be forced into a high-impedance state by the OMAP5912 HIGH_IMP3 control bit
K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

‖ Slew time constraint of the $\overline{EXT\_DMA\_REQ1}$ must be lower than or equal to 10 ns (from 10% to 90% of DV_{DD}) in Mode 1.

☆Slew time constraint of the $\overline{EXT\_DMA\_REQ0}$ must be lower than or equal to 10 ns (from 10% to 90% of DV_{DD}) in Mode 1.

NOTES: 3. NA denotes no multiplexing on the ball
4. ‘Regx’ denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

Table 2−3. ZDY/GDY Package Terminal Characteristics (Continued)

ZDY/ GDY BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING (see Notes 3 and 4)	PULLUP/ PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
L8	MCBSP2.DR	I	RegC[2:0] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G2	LZ	DV_{DD3}
	MCBSP2.DX	O	RegC[2:0] = 001					
	MCBSP2.DXZ	O/Z	RegC[2:0] = 010					
	GPIO22	I/O	RegC[2:0] = 111					
N6	MCBSP2.FSX	I/O	RegC[5:3] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G2	LZ	DV_{DD3}
	GPIO21	I/O	RegC[5:3] = 111					
U6	MCBSP2.CLKR	I/O	RegC[8:6] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	Z	DV_{DD3}
	GPIO11	I/O	RegC[8:6] = 001					
U5	MCBSP2.CLKX	I/O	RegC[11:9] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G2	LZ	DV_{DD3}
	GPIO20	I/O	RegC[11:9] = 111					
R5	MCBSP2.FSR	I/O	RegC[14:12] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	Z	DV_{DD3}
	GPIO12	I/O	RegC[14:12] = 001					
T5	MCBSP2.DX	O	RegC[17:15] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G2	0	DV_{DD3}
	MCBSP2.DR	I	RegC[17:15] = 001					
	MCBSP2.DXZ	O/Z	RegC[17:15] = 010					
	GPIO19	I/O	RegC[17:15] = 111					
U4	UART2.RX	I	RegC[20:18] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	LZ	DV_{DD3}
	USB2.VM	I	RegC[20:18] = 001					
	USB0.VM	I	RegC[20:18] = 101					
	GPIO18	I/O	RegC[20:18] = 111					
P6	UART2.CTS	I	RegC[23:21] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	LZ	DV_{DD3}
	USB2.RCV	I	RegC[23:21] = 001					
	GPIO7	I/O	RegC[23:21] = 010					
	USB0.RCV	I	RegC[23:21] = 101					

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20-µA internal pulldown, PD100=100-µA internal pulldown, PU20 = 20-µA internal pullup, PU100 = 100-µA internal pullup. Pullup or pulldown can be enabled or disabled by software.

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVCMOS input/output
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G3 = Terminal my be gated by BFAIL and OMAP5912 Internal Reset
H1 = Terminal may be 3-stated by BFAIL input
H3 = MCSI1.DOUT pin can be forced into a high-impedance state by the OMAP5912 HIGH_IMP3 control bit
K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

‖ Slew time constraint of the $\overline{\text{EXT\_DMA\_REQ1}}$ must be lower than or equal to 10 ns (from 10% to 90% of DV_{DD}) in Mode 1.

☆Slew time constraint of the $\overline{\text{EXT\_DMA\_REQ0}}$ must be lower than or equal to 10 ns (from 10% to 90% of DV_{DD}) in Mode 1.

NOTES: 3. NA denotes no multiplexing on the ball
4. ‘Regx’ denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

Table 2−3. ZDY/GDY Package Terminal Characteristics (Continued)

ZDY/ GDY BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING (see Notes 3 and 4)	PULLUP/ PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
T4	LOW_STATE	O	RegC[26:24] = 000		2 mA (Lv) 3 mA (Hv)	A, F, G2	0	DV_{DD3}
	UART2.RTS	O	RegC[26:24] = 001					
	USB2.SE0	O	RegC[26:24] = 010					
	MPUIO5	I/O	RegC[26:24] = 011					
	MPUIO12	I/O	RegC[26:24] = 100					
	USB0.SE0	O	RegC[26:24] = 101					
	LOW_STATE	O	RegC[26:24] = 110					
R4	LOW_STATE	O	RegC[29:27] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G2	0	DV_{DD3}
	UART2.TX	O	RegC[29:27] = 001					
	USB2.TXD	O	RegC[29:27] = 010					
	USB0.TXD	O	RegC[29:27] = 101					
	Z_STATE	Z	RegC[29:27] = 110					
	GPIO17	I/O	RegC[29:27] = 111					
P5	UART2.BCLK	O	RegD[2:0] = 000		2 mA (Lv) 3 mA (Hv)	A, F, G2	0	DV_{DD3}
	SYS_CLK_IN	I	RegD[2:0] = 110					
U3	MCLK	O	RegB[17:15] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD3}
	MMC2.DATDIR0	O	RegB[17:15] = 110					
	GPIO24	I/O	RegB[17:15] = 111					
P4	USB.PUEN	O	RegD[5:3] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	1	DV_{DD2}
	USB.CLKO	O	RegD[5:3] = 001					
	USB.PUDIS	O	RegD[5:3] = 011					
	Z_STATE	Z	RegD[5:3] = 100					
	$\overline{\text{LOW\_POWER}}$	O	RegD[5:3] = 110					
	GPIO58	I/O	RegD[5:3] = 111					
T2	USB.DP	I/O	USBTCTL[6:4] = 000		18.3 mA (in USB mode)	C	Z	DV_{DD2}
	I2C.SDA	I/O/Z	USBTCTL[6:4] = 100					
	UART1.RX	I	USBTCTL[6:4] = 101					
	USB.PUEN	O	USBTCTL[6:4] = 111					

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20-µA internal pulldown, PD100=100-µA internal pulldown, PU20 = 20-µA internal pullup, PU100 = 100-µA internal pullup. Pullup or pulldown can be enabled or disabled by software.

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H1 = Terminal may be 3-stated by BFAIL input
H3 = MCSI1.DOUT pin can be forced into a high-impedance state by the OMAP5912 HIGH_IMP3 control bit
K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

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NOTES: 3. NA denotes no multiplexing on the ball
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Table 2−3. ZDY/GDY Package Terminal Characteristics (Continued)

ZDY/ GDY BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING (see Notes 3 and 4)	PULLUP/ PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
U1	USB.DM I2C.SCL UART1.TX Z_STATE	I/O I/O/Z O Z	 USBTCTL[6:4] = 100 USBTCTL[6:4] = 101 USBTCTL[6:4] = 111		18.3 mA (in USB mode)	C	Z	DV_{DD2}
R2	OSC1_IN	I	NA			E	NA	NA
P2	OSC1_OUT	O	NA			E	NA	NA
T1	$\overline{\text{FLASH.CS1U}}$ GPIO16	O I/O	RegF[14:12] = 000 RegF[14:12] = 111		2 mA (Lv) 3 mA (Hv)	A, F	1	DV_{DD5}
R3	$\overline{\text{FLASH.WP}}$	O	NA		2 mA (Lv) 3 mA (Hv)	A	0	DV_{DD5}
P3	$\overline{\text{FLASH.WE}}$	O	NA		2 mA (Lv) 3 mA (Hv)	A	1	DV_{DD5}
N3	$\overline{\text{FLASH.RP}}$ $\overline{\text{FLASH.CS2UWE}}$	O O	RegF[23:21] = 000 RegF[23:21] = 001		2 mA (Lv) 3 mA (Hv)	A	0	DV_{DD5}
M5	$\overline{\text{FLASH.OE}}$	O	NA		2 mA (Lv) 3 mA (Hv)	A	1	DV_{DD5}
F3 J4 J2 H2 H5 F4 H4 H3 G6	FLASH.A[25:17]	O	NA		2 mA (Lv) 3 mA (Hv)	A, G1	0	DV_{DD5}
G5	FLASH.A[16]	O	Reg11[5:3] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, G1	0	DV_{DD5}
G2	FLASH.A[15]	O	Reg11[8:6] = 000		2 mA (Lv) 3 mA (Hv)	A, G1	0	DV_{DD5}
G4	FLASH.A[14]	O	Reg11[11:9] = 000		2 mA (Lv) 3 mA (Hv)	A, G1	0	DV_{DD5}
G3	FLASH.A[13]	O	Reg11[14:12] = 000		2 mA (Lv) 3 mA (Hv)	A, G1	0	DV_{DD5}
F5	FLASH.A[12]	O	Reg11[17:15] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, G1	0	DV_{DD5}

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20-µA internal pulldown, PD100=100-µA internal pulldown, PU20 = 20-µA internal pullup, PU100 = 100-µA internal pullup. Pullup or pulldown can be enabled or disabled by software.

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H1 = Terminal may be 3-stated by BFAIL input
H3 = MCSI1.DOUT pin can be forced into a high-impedance state by the OMAP5912 HIGH_IMP3 control bit
K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

‖ Slew time constraint of the $\overline{\text{EXT\_DMA\_REQ1}}$ must be lower than or equal to 10 ns (from 10% to 90% of DV_{DD}) in Mode 1.

☆Slew time constraint of the $\overline{\text{EXT\_DMA\_REQ0}}$ must be lower than or equal to 10 ns (from 10% to 90% of DV_{DD}) in Mode 1.

NOTES: 3. NA denotes no multiplexing on the ball
4. ‘Regx’ denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

Table 2−3. ZDY/GDY Package Terminal Characteristics (Continued)

ZDY/ GDY BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING (see Notes 3 and 4)	PULLUP/ PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
F1	FLASH.A[11]	O	Reg11[20:18] = 000		2 mA (Lv) 3 mA (Hv)	A, G1	0	DV_{DD5}
F2	FLASH.A[10]	O	Reg11[23:21] = 000		2 mA (Lv) 3 mA (Hv)	A, G1	0	DV_{DD5}
E1	FLASH.A[9]	O	Reg11[26:24] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, G1	0	DV_{DD5}
D1	FLASH.A[8]	O	Reg12[5:3] = 000		2 mA (Lv) 3 mA (Hv)	A, G1	0	DV_{DD5}
E2	FLASH.A[7]	O	Reg12[8:6] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, G1	0	DV_{DD5}
C1	FLASH.A[6]	O	Reg12[11:9] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, G1	0	DV_{DD5}
D2	FLASH.A[5]	O	Reg12[14:12] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, G1	0	DV_{DD5}
E3	FLASH.A[4]	O	Reg12[17:15] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, G1	0	DV_{DD5}
E4	FLASH.A[3]	O	Reg12[20:18] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, G1	0	DV_{DD5}
C2	FLASH.A[2]	O	Reg12[23:21] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, G1	0	DV_{DD5}
D3	FLASH.A[1]	O	Reg12[26:24] = 000		2 mA (Lv) 3 mA (Hv)	A, G1	0	DV_{DD5}
N4 R1 P1 K7 M3 M4 N2 L5 N1 K6 L4 M2 J7 L2 M1 L1	FLASH.D[15:0]	I/O	NA		2 mA (Lv) 3 mA (Hv)	A, K	0	DV_{DD5}

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20-µA internal pulldown, PD100=100-µA internal pulldown, PU20 = 20-µA internal pullup, PU100 = 100-µA internal pullup. Pullup or pulldown can be enabled or disabled by software.

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVCMOS input/output
B = SUBLVDS input/ouput
C = USB transceiver input/ouput
D = I^2C input/output buffers
E = Analog oscillator terminals
F = Boundary-scannable terminal
G1 = Terminal may be gated by BFAIL
G2 = Terminal may be gated by GPIO9 and MPUIO3
G3 = Terminal my be gated by BFAIL and OMAP5912 Internal Reset
H1 = Terminal may be 3-stated by BFAIL input
H3 = MCSI1.DOUT pin can be forced into a high-impedance state by the OMAP5912 HIGH_IMP3 control bit
K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

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☆Slew time constraint of the $\overline{\text{EXT\_DMA\_REQ0}}$ must be lower than or equal to 10 ns (from 10% to 90% of DV_{DD}) in Mode 1.

NOTES: 3. NA denotes no multiplexing on the ball
4. ‘Regx’ denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

Table 2−3. ZDY/GDY Package Terminal Characteristics (Continued)

ZDY/ GDY BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING (see Notes 3 and 4)	PULLUP/ PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
K1	FLASH.CLK	O	Reg10[23:21] = 000		2 mA (Lv) 3 mA (Hv)	A, K, G1	0	DV_{DD5}
	$\overline{\text{FLASH.CS2UOE}}$	O	Reg10[23:21] = 001					
L6	FLASH.RDY	I	RegF[29:27] = 000	PU100, PD20	2 mA (Lv) 3 mA (Hv)	A, F	Input	DV_{DD5}
	GPIO10	I/O	RegF[29:27] = 001					
H6	$\overline{\text{FLASH.ADV}}$	O	NA		2 mA (Lv) 3 mA (Hv)	A	1	DV_{DD5}
J8	$\overline{\text{FLASH.CS2}}$	O	RegD[8:6] = 000		2 mA (Lv) 3 mA (Hv)	A	1	DV_{DD5}
	$\overline{\text{FLASH.BAA}}$	O	RegD[8:6] = 001					
	$\overline{\text{FLASH.CS2L}}$	O	RegD[8:6] = 010					
J5	GPIO62	I/O	Reg10[2:0] = 000	PU100	2 mA (Lv) 3 mA (Hv)	A, F, G1	Input	DV_{DD5}
	$\overline{\text{FLASH.CS0}}$	O	Reg10[2:0] = 001					
J3	$\overline{\text{FLASH.CS1}}$	O	Reg10[29:27] = 000		2 mA (Lv) 3 mA (Hv)	A	1	DV_{DD5}
	$\overline{\text{FLASH.CS1L}}$	O	Reg10[29:27] = 001					
K3	$\overline{\text{FLASH.CS2U}}$	O	Reg10[20:18] = 000		2 mA (Lv) 3 mA (Hv)	A, F	1	DV_{DD5}
	GPIO5	I/O	Reg10[20:18] = 001					
J1	$\overline{\text{FLASH.BE[0]}}$	O	Reg10[8:6] = 000		2 mA (Lv) 3 mA (Hv)	A, F	0	DV_{DD5}
	$\overline{\text{FLASH.CS2UOE}}$	O	Reg10[8:6] = 001					
	GPIO59	I/O	Reg10[8:6] = 111					
K2	$\overline{\text{FLASH.BE[1]}}$	O	Reg10[5:3] = 000		2 mA (Lv) 3 mA (Hv)	A, F	0	DV_{DD5}
	$\overline{\text{FLASH.CS2UWE}}$	O	Reg10[5:3] = 001					
	GPIO60	I/O	Reg10[5:3] = 111					
J6	$\overline{\text{FLASH.CS3}}$	O	Reg10[26:24] = 000		2 mA (Lv) 3 mA (Hv)	A, F	1	DV_{DD5}
	GPIO3	I/O	Reg10[26:24] = 111					

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20-µA internal pulldown, PD100=100-µA internal pulldown, PU20 = 20-µA internal pullup, PU100 = 100-µA internal pullup. Pullup or pulldown can be enabled or disabled by software.

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVCMOS input/output
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H3 = MCSI1.DOUT pin can be forced into a high-impedance state by the OMAP5912 HIGH_IMP3 control bit
K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

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NOTES: 3. NA denotes no multiplexing on the ball
4. ‘Regx’ denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

Table 2−4. ZZG Package Terminal Characteristics

ZZG BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING (see Notes 3 and 4)	PULLUP/ PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
G8	$\overline{\text{SDRAM.CS}}$	O	NA		2 mA (Lv) 3 mA (Hv)	A	1	DV_{DD4}
C14	SDRAM.DQSH	I/O	NA		2 mA (Lv) 3 mA (Hv)	A, K	0	DV_{DD4}
D4	SDRAM.DQSL	I/O	NA		2 mA (Lv) 3 mA (Hv)	A, K	0	DV_{DD4}
B4	$\overline{\text{SDRAM.CAS}}$	O	NA		2 mA (Lv) 3 mA (Hv)	A	1	DV_{DD4}
H7	$\overline{\text{SDRAM.RAS}}$	O	NA		2 mA (Lv) 3 mA (Hv)	A	1	DV_{DD4}
C8	SDRAM.DQML	O	NA		2 mA (Lv) 3 mA (Hv)	A, K	0	DV_{DD4}
D10	SDRAM.DQMU	O	NA		2 mA (Lv) 3 mA (Hv)	A, K	0	DV_{DD4}
H8	$\overline{\text{SDRAM.WE}}$	O	NA		2 mA (Lv) 3 mA (Hv)	A	1	DV_{DD4}
H11 H9 H10 B8 B12 G9 G11 G12 B9 G10 A1 B6 B2 A2	SDRAM.A[13:0]	O	NA		2 mA (Lv) 3 mA (Hv)	A	0	DV_{DD4}
C3 B3	SDRAM.BA[1:0]	O	NA		2 mA (Lv) 3 mA (Hv)	A	0	DV_{DD4}

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20-µA internal pulldown, PD100=100-µA internal pulldown, PU20 = 20-µA internal pullup, PU100 = 100-µA internal pullup. Pullup or pulldown can be enabled or disabled by software.

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Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

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NOTES: 3. NA denotes no multiplexing on the ball
4. ‘Regx’ denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

Table 2−4. ZZG Package Terminal Characteristics (Continued)

ZZG BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING (see Notes 3 and 4)	PULLUP/ PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
C12 D12 D13 C11 C13 D11 D14 C10 D8 C4 C7 D5 D7 C5 C6 D6	SDRAM.D[15:0]	I/O	NA		2 mA (Lv) 3 mA (Hv)	A, K	0	DV_{DD4}
C9	SDRAM.CLK	O	NA		2 mA (Lv) 3 mA (Hv)	A, K	U	DV_{DD4}
D9	SDRAM.CLKX	O	NA		2 mA (Lv) 3 mA (Hv)	A, K	0	DV_{DD4}
H12	SDRAM.CKE	O	NA		2 mA (Lv) 3 mA (Hv)	A	1	DV_{DD4}
B15	LCD.AC SYS_CLK_OUT Z_STATE	O O Z	RegD[11:9] = 000 RegD[11:9] = 001 RegD[11:9] = 010		2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD1}
C15	LCD.PCLK Z_STATE	O Z	RegD[17:15] = 000 RegD[17:15] = 001		2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD1}
D15	LCD.P[15] Z_STATE GPIO2	O Z I/O	RegD[20:18] = 000 RegD[20:18] = 001 RegD[20:18] = 111		2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD1}
C16	LCD.P[14] Z_STATE GPIO35	O Z I/O	RegD[23:21] = 000 RegD[23:21] = 001 RegD[23:21] = 111		2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD1}
A17	LCD.P[13] Z_STATE GPIO34	O Z I/O	RegD[26:24] = 000 RegD[26:24] = 001 RegD[26:24] = 111		2 mA (Lv) 3 mA (Hv)	F, A, G1	0	DV_{DD1}

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20-µA internal pulldown, PD100=100-µA internal pulldown, PU20 = 20-µA internal pullup, PU100 = 100-µA internal pullup. Pullup or pulldown can be enabled or disabled by software.

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H3 = MCSI1.DOUT pin can be forced into a high-impedance state by the OMAP5912 HIGH_IMP3 control bit
K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

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Table 2−4. ZZG Package Terminal Characteristics (Continued)

ZZG BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING (see Notes 3 and 4)	PULLUP/ PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
G13	LCD.P[12]	O	RegD[29:27] = 000		2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD1}
	Z_STATE	Z	RegD[29:27] = 001					
	GPIO33	I/O	RegD[29:27] = 111					
B17	LCD.P[11]	O	RegE[2:0] = 000		2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD1}
	Z_STATE	Z	RegE[2:0] = 001					
	GPIO32	I/O	RegE[2:0] = 111					
C17	LCD.P[10]	O	RegE[5:3] = 000		2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD1}
	Z_STATE	Z	RegE[5:3] = 001					
	GPIO31	I/O	RegE[5:3] = 111					
D16	LCD.P[9]	O	RegE[8:6] = 000		2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD1}
	Z_STATE	Z	RegE[8:6] = 001					
	GPIO30	I/O	RegE[8:6] = 111					
B18	LCD.VS	O	RegE[11:9] = 000		2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD1}
	Z_STATE	Z	RegE[11:9] = 001					
D17	LCD.P[8]	O	RegE[14:12] = 000		2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD1}
	Z_STATE	Z	RegE[14:12] = 001					
	GPIO29	I/O	RegE[14:12] = 111					
C18	LCD.P[7]	O	RegE[17:15] = 000		2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD1}
	Z_STATE	Z	RegE[17:15] = 001					
B19	LCD.P[6]	O	RegE[20:18] = 000		2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD1}
	Z_STATE	Z	RegE[20:18] = 001					
A20	LCD.P[5]	O	RegE[23:21] = 000		2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD1}
	Z_STATE	Z	RegE[23:21] = 001					
H13	LCD.P[4]	O	RegE[26:24] = 000		2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD1}
	Z_STATE	Z	RegE[26:24] = 001					
G14	LCD.P[3]	O	RegE[29:27] = 000		2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD1}
	Z_STATE	Z	RegE[29:27] = 001					
C19	LCD.P[2]	O	RegF[2:0] = 000		2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD1}
	Z_STATE	Z	RegF[2:0] = 001					

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20-µA internal pulldown, PD100=100-µA internal pulldown, PU20 = 20-µA internal pullup, PU100 = 100-µA internal pullup. Pullup or pulldown can be enabled or disabled by software.

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Table 2−4. ZZG Package Terminal Characteristics (Continued)

ZZG BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING (see Notes 3 and 4)	PULLUP/ PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
B21	LCD.P[1] Z_STATE	O Z	RegF[5:3] = 000 RegF[5:3] = 001		2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD1}
D18	LCD.P[0] Z_STATE	O Z	RegF[8:6] = 000 RegF[8:6] = 001		2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD1}
C20	LCD.HS Z_STATE	O Z	RegD[14:12] = 000 RegD[14:12] = 001		2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD1}
C21	KB.C[4] GPIO27	O I/O	Reg3[5:3] = 000 Reg3[5:3] = 111	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	0	DV_{DD1}
E18	KB.C[3] GPIO63	O I/O	Reg3[8:6] = 000 Reg3[8:6] = 110	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	0	DV_{DD1}
D19	KB.C[2] GPIO61	O I/O	Reg3[11:9] = 000 Reg3[11:9] = 111	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	0	DV_{DD1}
D20	KB.C[1] MPUIO6	O I/O	Reg3[14:12] = 000 Reg3[14:12] = 001	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	0	DV_{DD1}
F18	KB.C[0] MPUIO0	O I/O	Reg3[17:15] = 000 Reg3[17:15] = 001	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	0	DV_{DD1}
E19	KB.R[4] MPUIO15	I I/O	Reg3[20:18] = 000 Reg3[20:18] = 001	PU100, PD20	2 mA (Lv) 3 mA (Hv)	A, F	Z	DV_{DD1}
E20	KB.R[3] MPUIO13	I I/O	Reg3[23:21] = 000 Reg3[23:21] = 001	PU100, PD20	2 mA (Lv) 3 mA (Hv)	A, F	Z	DV_{DD1}
H14	KB.R[2] MPUIO10	I I/O	Reg3[26:24] = 000 Reg3[26:24] = 001	PU100, PD20	2 mA (Lv) 3 mA (Hv)	A, F	Z	DV_{DD1}
F19	KB.R[1] MPUIO9	I I/O	Reg3[29:27] = 000 Reg3[29:27] = 001	PU100, PD20	2 mA (Lv) 3 mA (Hv)	A, F	Z	DV_{DD1}
G18	KB.R[0] MPUIO8	I I/O	Reg4[2:0] = 000 Reg4[2:0] = 001	PU100, PD20	2 mA (Lv) 3 mA (Hv)	A, F	Z	DV_{DD1}
G19	KB.C[5] GPIO28	O I/O	Reg3[2:0] = 000 Reg3[2:0] = 111	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	0	DV_{DD1}
G20	MCBSP1.CLKS GPIO62	I I/O	Reg4[8:6] = 000 Reg4[8:6] = 111	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	−	DV_{DD1}

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20-µA internal pulldown, PD100=100-µA internal pulldown, PU20 = 20-µA internal pullup, PU100 = 100-µA internal pullup. Pullup or pulldown can be enabled or disabled by software.

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☆Slew time constraint of the $\overline{\text{EXT\_DMA\_REQ0}}$ must be lower than or equal to 10 ns (from 10% to 90% of DV_{DD}) in Mode 1.

NOTES: 3. NA denotes no multiplexing on the ball
4. ‘Regx’ denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

Table 2−4. ZZG Package Terminal Characteristics (Continued)

ZZG BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING (see Notes 3 and 4)	PULLUP/ PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
G21	MCBSP1.CLKX	I/O	Reg4[11:9] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	Z	DV_{DD1}
	GPIO54	I/O	Reg4[11:9] = 111					
H15	MCBSP1.FSX	I/O	Reg4[14:12] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	Z	DV_{DD1}
	MCBSP1.DX	O	Reg4[14:12] = 001					
	MCBSP1.DXZ	O/Z	Reg4[14:12] = 010					
	GPIO53	I/O	Reg4[14:12] = 111					
H18	MCBSP1.DX	O	Reg4[17:15] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD1}
	MCBSP1.ESX	I/O	Reg4[17:15] = 001					
	MCBSP1.DXZ	O/Z	Reg4[17:15] = 010					
	GPIO52	I/O	Reg4[17:15] = 111					
H20	MCBSP1.DR	I	Reg4[20:18] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	LZ	DV_{DD1}
	GPIO51	I/O	Reg4[20:18] = 111					
H19	CAM.EXCLK	O	Reg4[23:21] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD8}
	ETM.SYNC[0]	O	Reg4[23:21] = 001					
	UWIRE.SDO	O	Reg4[23:21] = 010					
	LOW_STATE	O	Reg4[23:21] = 110					
	GPIO57	I/O	Reg4[23:21] = 111					
J15	CAM.LCLK	I	Reg4[26:24] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	Z	DV_{DD8}
	ETM.CLK	O	Reg4[26:24] = 001					
	UWIRE.SCLK	O	Reg4[26:24] = 010					
	GPIO39	I/O	Reg4[26:24] = 111					
J20	MPU_BOOT	I	Reg8[29:27] = 000		2 mA (Lv) 3 mA (Hv)	A, F	−	DV_{DD8}
	USB1.SUSP	O	Reg8[29:27] = 010					
J18	CAM.D[7]	I	Reg4[29:27] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	Z	DV_{DD8}
	ETM.D[7]	O	Reg4[29:27] = 001					
	$\overline{\text{UWIRE.CS0}}$	O	Reg4[29:27] = 010					
	MMC2.DAT2	I/O	Reg4[29:27] = 011					
	GPIO35	I/O	Reg4[29:27] = 111					

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20-µA internal pulldown, PD100=100-µA internal pulldown, PU20 = 20-µA internal pullup, PU100 = 100-µA internal pullup. Pullup or pulldown can be enabled or disabled by software.

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVCMOS input/output
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F = Boundary-scannable terminal
G1 = Terminal may be gated by BFAIL
G2 = Terminal may be gated by GPIO9 and MPUIO3
G3 = Terminal my be gated by BFAIL and OMAP5912 Internal Reset
H1 = Terminal may be 3-stated by BFAIL input
H3 = MCSI1.DOUT pin can be forced into a high-impedance state by the OMAP5912 HIGH_IMP3 control bit
K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

‖ Slew time constraint of the $\overline{\text{EXT\_DMA\_REQ1}}$ must be lower than or equal to 10 ns (from 10% to 90% of DV_{DD}) in Mode 1.

☆Slew time constraint of the $\overline{\text{EXT\_DMA\_REQ0}}$ must be lower than or equal to 10 ns (from 10% to 90% of DV_{DD}) in Mode 1.

NOTES: 3. NA denotes no multiplexing on the ball
4. ‘Regx’ denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

Table 2−4. ZZG Package Terminal Characteristics (Continued)

ZZG BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING (see Notes 3 and 4)	PULLUP/ PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
J19	CAM.D[6]	I	Reg5[2:0] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	Z	DV_{DD8}
	ETM.D[6]	O	Reg5[2:0] = 001					
	$\overline{\text{UWIRE.CS3}}$	O	Reg5[2:0] = 010					
	MMC2.CMD	I/O	Reg5[2:0] = 011					
	GPIO34	I/O	Reg5[2:0] = 111					
J14	CAM.D[5]	I	Reg5[5:3] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	Z	DV_{DD8}
	ETM.D[5]	O	Reg5[5:3] = 001					
	UWIRE.SDI	I	Reg5[5:3] = 010					
	GPIO33	I/O	Reg5[5:3] = 111					
K18	CAM.D[4]	I	Reg5[8:6] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	Z	DV_{DD8}
	ETM.D[4]	O	Reg5[8:6] = 001					
	UART3.TX	O	Reg5[8:6] = 010					
	GPIO32	I/O	Reg5[8:6] = 111					
K19	CAM.D[3]	I	Reg5[11:9] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	Z	DV_{DD8}
	ETM.D[3]	O	Reg5[11:9] = 001					
	UART3.RX	I	Reg5[11:9] = 010					
	GPIO31	I/O	Reg5[11:9] = 111					
K15	CAM.D[2]	I	Reg5[14:12] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	Z	DV_{DD8}
	ETM.D[2]	O	Reg5[14:12] = 001					
	UART3.CTS	I	Reg5[14:12] = 010					
	GPIO30	I/O	Reg5[14:12] = 111					
K14	CAM.D[1]	I	Reg5[17:15] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	Z	DV_{DD8}
	ETM.D[1]	O	Reg5[17:15] = 001					
	UART3.RTS	O	Reg5[17:15] = 010					
	GPIO29	I/O	Reg5[17:15] = 111					
L19	CAM.D[0]	I	Reg5[20:18] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	Z	DV_{DD8}
	ETM.D[0]	O	Reg5[20:18] = 001					
	MPUIO12	I/O	Reg5[20:18] = 010					
	MMC2.DAT3	I/O	Reg5[20:18] = 011					

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20-µA internal pulldown, PD100=100-µA internal pulldown, PU20 = 20-µA internal pullup, PU100 = 100-µA internal pullup. Pullup or pulldown can be enabled or disabled by software.

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¶ A = Standard LVCMOS input/output
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H1 = Terminal may be 3-stated by BFAIL input
H3 = MCSI1.DOUT pin can be forced into a high-impedance state by the OMAP5912 HIGH_IMP3 control bit
K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

‖ Slew time constraint of the $\overline{\text{EXT\_DMA\_REQ1}}$ must be lower than or equal to 10 ns (from 10% to 90% of DV_{DD}) in Mode 1.

☆Slew time constraint of the $\overline{\text{EXT\_DMA\_REQ0}}$ must be lower than or equal to 10 ns (from 10% to 90% of DV_{DD}) in Mode 1.

NOTES: 3. NA denotes no multiplexing on the ball
4. ‘Regx’ denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

Table 2−4. ZZG Package Terminal Characteristics (Continued)

ZZG BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING (see Notes 3 and 4)	PULLUP/ PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
L18	CAM.VS	I	Reg5[23:21] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	Z	DV_{DD8}
	ETM.PSTAT[2]	O	Reg5[23:21] = 001					
	MPUIO14	I/O	Reg5[23:21] = 010					
	MMC2.DAT1	I/O	Reg5[23:21] = 011					
L15	CAM.HS	I	Reg5[26:24] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	Z	DV_{DD8}
	ETM.PSTAT[1]	O	Reg5[26:24] = 001					
	UART2.CTS	I	Reg5[26:24] = 010					
	MMC2.DAT0	I/O	Reg5[26:24] = 011					
	GPIO38	I/O	Reg5[26:24] = 111					
M19	CAM.RSTZ	O	Reg5[29:27] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD8}
	ETM.PSTAT[0]	O	Reg5[29:27] = 001					
	UART2.RTS	O	Reg5[29:27] = 010					
	MMC2.CLK	O	Reg5[29:27] = 011					
	LOW_STATE	O	Reg5[29:27] = 110					
	GPIO37	I/O	Reg5[29:27] = 111					
M18	LOW_STATE	O	Reg6[2:0] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD9}
	UART3.TX	O	Reg6[2:0] = 001					
	PWT	O	Reg6[2:0] = 010					
	UART2.TX	O	Reg6[2:0] = 100					
	TIMER.PWM0	O	Reg6[2:0] = 101					
	GPIO50	I/O	Reg6[2:0] = 111					
L14	UART3.RX	I	Reg6[5:3] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	−	DV_{DD9}
	PWL	O	Reg6[5:3] = 001					
	UART2.RX	I	Reg6[5:3] = 011					
	TIMER.PWM1	O	Reg6[5:3] = 100					
	GPIO49	I/O	Reg6[5:3] = 111					
M20	GPIO15	I/O	Reg6[8:6] = 000	PU100, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	LZ	DV_{DD9}
	KB.R[7]	I	Reg6[8:6] = 001					
	TIMER.PWM2	O	Reg6[8:6] = 010					

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20-µA internal pulldown, PD100=100-µA internal pulldown, PU20 = 20-µA internal pullup, PU100 = 100-µA internal pullup. Pullup or pulldown can be enabled or disabled by software.

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H1 = Terminal may be 3-stated by BFAIL input
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K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

‖ Slew time constraint of the $\overline{\text{EXT\_DMA\_REQ1}}$ must be lower than or equal to 10 ns (from 10% to 90% of DV_{DD}) in Mode 1.

☆Slew time constraint of the $\overline{\text{EXT\_DMA\_REQ0}}$ must be lower than or equal to 10 ns (from 10% to 90% of DV_{DD}) in Mode 1.

NOTES: 3. NA denotes no multiplexing on the ball
4. ‘Regx’ denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

Table 2−4. ZZG Package Terminal Characteristics (Continued)

ZZG BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING (see Notes 3 and 4)	PULLUP/ PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
N21	GPIO14	I/O	Reg6[11:9] = 000	PU100, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	LZ	DV_{DD9}
	KB.R[6]	I	Reg6[11:9] = 001					
	LCD.RED0	O	Reg6[11:9] = 010					
	Z_STATE	Z	Reg6[11:9] = 011					
N19	GPIO13	I/O	Reg6[14:12] = 000	PU100, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	LZ	DV_{DD9}
	KB.R[5]	I	Reg6[14:12] = 001					
	LCD.BLUE0	O	Reg6[14:12] = 010					
	Z_STATE	Z	Reg6[14:12] = 011					
N18	GPIO12	I/O	Reg6[17:15] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	LZ	DV_{DD9}
	MCBSP3.FSX	I/O	Reg6[17:15] = 001					
	TIMER.EXTCLK	I	Reg6[17:15] = 011					
N20	GPIO11	I/O	Reg6[20:18] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	LZ	DV_{DD9}
	HDQ	I/O	Reg6[20:18] = 001					
	ETM.PSTAT[5]	O	Reg6[20:18] = 101					
	RTDX.D[3]	I/O	Reg6[20:18] = 111					
M15	GPIO7	I/O	Reg6[23:21] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	LZ	DV_{DD9}
	MMC.DAT2	I/O	Reg6[23:21] = 001					
	TCK	I	Reg6[23:21] = 011					
	MCSI1.CLK	I/O	Reg6[23:21] = 100					
	ETM.SYNC[1]	O	Reg6[23:21] = 101					
	RTDX.D[2]	I/O	Reg6[23:21] = 111					
P19	GPIO6	I/O	Reg6[26:24] = 000	PD100, PU20	2 mA (Lv) 3 mA (Hv)	A, F, G1	LZ	DV_{DD9}
	MCBSP3.FSX	I/O	Reg6[26:24] = 010					
	TIMER.EVENT3	I	Reg6[26:24] = 011					
	MCSI1.DIN	I	Reg6[26:24] = 100					
	TMS	I	Reg6[26:24] = 101					
P20	GPIO4	I/O	Reg6[29:27] = 000	PD100, PU20	2 mA (Lv) 3 mA (Hv)	A, F, G1	LZ	DV_{DD9}
	MCBSP3.FSX	I/O	Reg6[29:27] = 010					
	TIMER.EVENT4	I	Reg6[29:27] = 011					
	SPIF.DIN	I	Reg6[29:27] = 100					

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20-µA internal pulldown, PD100=100-µA internal pulldown, PU20 = 20-µA internal pullup, PU100 = 100-µA internal pullup. Pullup or pulldown can be enabled or disabled by software.

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

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‖ Slew time constraint of the $\overline{\text{EXT\_DMA\_REQ1}}$ must be lower than or equal to 10 ns (from 10% to 90% of DV_{DD}) in Mode 1.

☆Slew time constraint of the $\overline{\text{EXT\_DMA\_REQ0}}$ must be lower than or equal to 10 ns (from 10% to 90% of DV_{DD}) in Mode 1.

NOTES: 3. NA denotes no multiplexing on the ball
4. ‘Regx’ denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

Table 2−4. ZZG Package Terminal Characteristics (Continued)

ZZG BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING (see Notes 3 and 4)	PULLUP/ PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
P18	GPIO3	I/O	Reg7[2:0] = 000	PU100, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	LZ	DV_{DD9}
	MCBSP3.FSX	I/O	Reg7[2:0] = 010					
	LED1	O	Reg7[2:0] = 011					
	ETM.PSTAT[3]	O	Reg7[2:0] = 101					
M14	GPIO2	I/O	Reg7[5:3] = 000	PU100, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	LZ	DV_{DD9}
	ETM.PSTAT[4]	O	Reg7[5:3] = 101					
	RTDX.D[0]	I/O	Reg7[5:3] = 111					
R19	GPIO1	I/O	Reg7[8:6] = 000	PU100, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	LZ	DV_{DD9}
	UART3.RTS	O	Reg7[8:6] = 001					
R18	GPIO0	I/O	Reg7[11:9] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	LZ	DV_{DD9}
	USB.VBUS	I	Reg7[11:9] = 010					
	SPIF.DOUT	O	Reg7[11:9] = 011					
	MMC2.CLKIN	I	Reg7[11:9] = 110					
T20	MPUIO5	I/O	Reg7[14:12] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	LZ	DV_{DD9}
	LOW_PWR	O	Reg7[14:12] = 001					
	UART3.RTS	O	Reg7[14:12] = 011					
	UART1.DTR	O	Reg7[14:12] = 100					
T19	MPUIO4	I/O	Reg7[17:15] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	LZ	DV_{DD9}
	$\overline{\text{EXT\_DMA\_REQ1}}$‖	I	Reg7[17:15] = 001					
	LED2	O	Reg7[17:15] = 010					
	$\overline{\text{UWIRE.CS2}}$	O	Reg7[17:15] = 011					
	$\overline{\text{SPIF.CS2}}$	O	Reg7[17:15] = 100					
	MCBSP3.DR	I	Reg7[17:15] = 110					
N15	MPUIO2	I/O	Reg7[20:18] = 000	PU100, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	LZ	DV_{DD9}
	$\overline{\text{EXT\_DMA\_REQ0}}$☆	I	Reg7[20:18] = 001					
	$\overline{\text{UWIRE.CS1}}$	O	Reg7[20:18] = 010					
	$\overline{\text{SPIF.CS1}}$	O	Reg7[20:18] = 110					
U20	$\overline{\text{MPU\_RST}}$	I	Reg9[8:6] = 000		2 mA (Lv) 3 mA (Hv)	A, F	−	DV_{DD9}
	MPUIO14	I/O	Reg9[8:6] = 110					

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20-µA internal pulldown, PD100=100-µA internal pulldown, PU20 = 20-µA internal pullup, PU100 = 100-µA internal pullup. Pullup or pulldown can be enabled or disabled by software.

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☆Slew time constraint of the $\overline{\text{EXT\_DMA\_REQ0}}$ must be lower than or equal to 10 ns (from 10% to 90% of DV_{DD}) in Mode 1.

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Table 2−4. ZZG Package Terminal Characteristics (Continued)

ZZG BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING (see Notes 3 and 4)	PULLUP/ PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
U19	MPUIO1	I/O	Reg7[23:21] = 000	PU100, PD20	2 mA (Lv) 3 mA (Hv)	A, F	Z	DV_{DD9}
	RTCK	I/O	Reg7[23:21] = 001					
	SPIF.SCK	I/O	Reg7[23:21] = 110					
T18	I2C.SCL	I/O/Z	Reg7[26:24] = 000		2 mA (Lv) 3 mA (Hv)	D	Z	DV_{DD9}
V20	I2C.SDA	I/O/Z	Reg7[29:27] = 000		2 mA (Lv) 3 mA (Hv)	D	Z	DV_{DD9}
	GPIO48	I	Reg7[29:27] = 111					
U18	UWIRE.SDI	I	Reg8[2:0] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	LZ	DV_{DD9}
	UART3.DSR	O	Reg8[2:0] = 001					
	UART1.DSR	I	Reg8[2:0] = 010					
	MCBSP3.DR	I	Reg8[2:0] = 011					
	SPIF.DIN	I/O	Reg8[2:0] = 110					
	GPIO47	I/O	Reg8[2:0] = 111					
W21	UWIRE.SDO	O	Reg8[5:3] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD9}
	UART3.DTR	O	Reg8[5:3] = 001					
	UART1.DTR	O	Reg8[5:3] = 010					
	MCBSP3.DX	O	Reg8[5:3] = 011					
	UART3.RTS	O	Reg8[5:3] = 100					
	MCBSP3.DXZ	O/Z	Reg8[5:3] = 101					
	SPIF.DOUT	I/O	Reg8[5:3] = 110					
	GPIO46	I/O	Reg8[5:3] = 111					
V19	UWIRE.SCLK	O	Reg8[8:6] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD9}
	KB.C[7]	O	Reg8[8:6] = 001					
	MPUIO1	I/O	Reg8[8:6] = 010					
	UART3.CTS	I	Reg8[8:6] = 100					

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20-µA internal pulldown, PD100=100-µA internal pulldown, PU20 = 20-µA internal pullup, PU100 = 100-µA internal pullup. Pullup or pulldown can be enabled or disabled by software.

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVCMOS input/output
B = SUBLVDS input/ouput
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G1 = Terminal may be gated by BFAIL
G2 = Terminal may be gated by GPIO9 and MPUIO3
G3 = Terminal my be gated by BFAIL and OMAP5912 Internal Reset
H1 = Terminal may be 3-stated by BFAIL input
H3 = MCSI1.DOUT pin can be forced into a high-impedance state by the OMAP5912 HIGH_IMP3 control bit
K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

‖ Slew time constraint of the $\overline{\text{EXT\_DMA\_REQ1}}$ must be lower than or equal to 10 ns (from 10% to 90% of DV_{DD}) in Mode 1.

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NOTES: 3. NA denotes no multiplexing on the ball
4. ‘Regx’ denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

Table 2−4. ZZG Package Terminal Characteristics (Continued)

ZZG BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING (see Notes 3 and 4)	PULLUP/ PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
N14	Z_STATE	Z	Reg8[11:9] = 000	PU100, PD20	2 mA (Lv) 3 mA (Hv)	A, F	Z	DV_{DD9}
	$\overline{\text{UWIRE.CS0}}$	O	Reg8[11:9] = 001					
	MCBSP3.CLKX	I/O	Reg8[11:9] = 010					
	UART3.TX	O	Reg8[11:9] = 100					
	$\overline{\text{SPIF.CS0}}$	I/O	Reg8[11:9] = 110					
	GPIO45	I/O	Reg8[11:9] = 111					
P15	Z_STATE	Z	Reg8[14:12] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	Z	DV_{DD9}
	$\overline{\text{UWIRE.CS3}}$	O	Reg8[14:12] = 001					
	KB.C[6]	O	Reg8[14:12] = 010					
	$\overline{\text{SPIF.CS3}}$	O	Reg8[14:12] = 011					
	UART3.RX	I	Reg8[14:12] = 100					
	Z_STATE	Z	Reg8[14:12] = 110					
	GPIO44	I/O	Reg8[14:12] = 111					
W19	BFAIL/$\overline{\text{EXT\_FIQ}}$	I	Reg8[17:15] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	Z	DV_{DD9}
	UART3.CTS	I	Reg8[17:15] = 001					
	UART1.DSR	I	Reg8[17:15] = 010					
	MMC2.DATDIR1	O	Reg8[17:15] = 110					
AA20	$\overline{\text{RST\_OUT}}$	O	Reg9[11:9] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	0	DV_{DD9}
	GPIO41	I/O	Reg9[11:9] = 111					
V18	CONF	I	NA	PU20, PD20		A	LZ	DV_{DD9}
Y19	TDI	I	NA	PD100, PU20		A	LZ	DV_{DD9}
AA19	TDO	O	0		2 mA (Lv) 3 mA (Hv)		Z	DV_{DD9}
V17	TMS	I	NA	PD100, PU20		A	LZ	DV_{DD9}
W18	TCK	I	NA	PD100, PU20		A	LZ	DV_{DD9}
Y18	$\overline{\text{TRST}}$	I	NA	PU20, PD20		A	−	DV_{DD9}

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20-µA internal pulldown, PD100=100-µA internal pulldown, PU20 = 20-µA internal pullup, PU100 = 100-µA internal pullup. Pullup or pulldown can be enabled or disabled by software.

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H1 = Terminal may be 3-stated by BFAIL input
H3 = MCSI1.DOUT pin can be forced into a high-impedance state by the OMAP5912 HIGH_IMP3 control bit
K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

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Table 2−4. ZZG Package Terminal Characteristics (Continued)

ZZG BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING (see Notes 3 and 4)	PULLUP/ PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
V16	EMU0	I/O	NA	PU100, PD20	2 mA (Lv) 3 mA (Hv)	A	Input	DV_{DD9}
W17	EMU1	I/O	NA	PU100, PD20	2 mA (Lv) 3 mA (Hv)	A	Input	DV_{DD9}
Y17	RTCK	I/O	NA		2 mA (Lv) 3 mA (Hv)	A	−	DV_{DD9}
AA17	MCSI1.SYNC	I/O	RegA[5:3] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	LZ	DV_{DD7}
	MCBSP3.DR	I	RegA[5:3] = 001					
	USB1.VP	I	RegA[5:3] = 010					
	MCBSP3.FSX	I/O	RegA[5:3] = 100					
P14	MCSI1.CLK	I/O	RegA[8:6] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	LZ	DV_{DD7}
	MCBSP3.DX	O	RegA[8:6] = 001					
	USB1.VM	I	RegA[8:6] = 010					
	TDI	I	RegA[8:6] = 011					
	MCBSP3.CLKX	I/O	RegA[8:6] = 100					
	GPIO43	I/O	RegA[8:6] = 111					
W16	Z_STATE	Z	Reg9[5:3] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	Z	DV_{DD7}
	MCBSP3.CLKX	I/O	Reg9[5:3] = 001					
	USB1.TXEN	O	Reg9[5:3] = 010					
	MCSI1.DIN_OUT	O	Reg9[5:3] = 011					
	MCSI1.DIN	I	Reg9[5:3] = 100					
	Z_STATE	Z	Reg9[5:3] = 110					
	GPIO42	I/O	Reg9[5:3] = 111					
V15	MCSI1.DIN	I	RegA[11:9] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	Z	DV_{DD7}
	USB1.RCV	I	RegA[11:9] = 001					
	EMU1	I/O	RegA[11:9] = 011					
	MCBSP3.DR	I	RegA[11:9] = 100					
	GPIO56	I/O	RegA[11:9] = 111					

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20-µA internal pulldown, PD100=100-µA internal pulldown, PU20 = 20-µA internal pullup, PU100 = 100-µA internal pullup. Pullup or pulldown can be enabled or disabled by software.

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K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

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Table 2−4. ZZG Package Terminal Characteristics (Continued)

ZZG BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING (see Notes 3 and 4)	PULLUP/ PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
W15	BCLKREQ	I	Reg9[29:27] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	LZ	DV_{DD7}
	UART3.CTS	I	Reg9[29:27] = 001					
	MMC2.DAT2	I/O	Reg9[29:27] = 110					
	GPIO40	I/O	Reg9[29:27] = 111					
Y15	BCLK	O	RegA[2:0] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD7}
	UART3.RTS	O	RegA[2:0] = 001					
	CAM.OUTCLK	O	RegA[2:0] = 110					
	GPIO17	I/O	RegA[2:0] = 111					
AA15	LOW_STATE	O	Reg9[14:12] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD7}
	UART1.RTS	O	Reg9[14:12] = 001					
	UART1.IRSHDN	O	Reg9[14:12] = 010					
	Z_STATE	Z	Reg9[14:12] = 110					
	GPIO39	I/O	Reg9[14:12] = 111					
R14	UART1.CTS	I	Reg9[17:15] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	LZ	DV_{DD7}
	UART1.IRSEL	O	Reg9[17:15] = 010					
	GPIO38	I/O	Reg9[17:15] = 111					
V14	UART1.RX	I	Reg9[20:18] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	LZ	DV_{DD7}
	UART1.IRRX	I	Reg9[20:18] = 010					
	GPIO37	I/O	Reg9[20:18] = 111					
Y14	LOW_STATE	O	Reg9[23:21] = 000		2 mA (Lv) 3 mA (Hv)	A, B, F, G1	0	DV_{DD7}
	UART1.TX	O	Reg9[23:21] = 001					
	UART1.IRTX	O	Reg9[23:21] = 010					
W14	MCSI1.DOUT	O	Reg9[26:24] = 000		2 mA (Lv) 3 mA (Hv)	A, B, F, G1, H3	0	DV_{DD7}
	USB1.TXD	O	Reg9[26:24] = 001					
	TDO	O	Reg9[26:24] = 011					
	MCBSP3.DX	O	Reg9[26:24] = 100					
	GPIO18	I/O	Reg9[26:24] = 111					

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20-µA internal pulldown, PD100=100-µA internal pulldown, PU20 = 20-µA internal pullup, PU100 = 100-µA internal pullup. Pullup or pulldown can be enabled or disabled by software.

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Table 2−4. ZZG Package Terminal Characteristics (Continued)

ZZG BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING (see Notes 3 and 4)	PULLUP/ PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
R13	CLK32K_OUT	O	RegA[14:12] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A	U	DV_{DDRTC}
	MPUIO0	I/O	RegA[14:12] = 100					
	USB1.SPEED	O	RegA[14:12] = 101					
	UART1.TX	O	RegA[14:12] = 110					
	GPIO36	I/O	RegA[14:12] = 111					
V13	OSC32K_IN	−	NA			E	NA	NA
AA13	OSC32K_OUT	−	NA			E	NA	NA
W13	RTC_WAKE_INT	O	Reg9[2:0] = 000		2 mA (Lv) 3 mA (Hv)	A, B	0	DV_{DDRTC}
	USB1.SE0	O	Reg9[2:0] = 100					
	RST_HOST_OUT	O	Reg9[2:0] = 101					
	GPIO55	I/O	Reg9[2:0] = 111					
Y12	RTC_ON_NOFF	I	Reg8[20:18] = 000		2 mA (Lv) 3 mA (Hv)	A, B, G1	Z	DV_{DDRTC}
P13	CLK32K_IN	I	RegA[17:15] = 000			A	Input	DV_{DDRTC}
R12	$\overline{\text{PWRON\_RESET}}$	I	NA			A	Input	DV_{DDRTC}
W11	MMC.DAT3	I/O	Reg10[17:15] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	Z	DV_{DD6}
	MPUIO9	I/O	Reg10[17:15] = 001					
	MPUIO6	I/O	Reg10[17:15] = 010					
V11	MMC.CLK	O	RegA[23:21] = 000	PD100, PU20	2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD6}
	GPIO57	I/O	RegA[23:21] = 111					
R11	MMC.DAT0	I/O	RegB[2:0] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	Z	DV_{DD6}
	Z_STATE	Z	RegB[2:0] = 001					
	GPIO58	I/O	RegB[2:0] = 111					
W10	MMC.DAT2	I/O	RegA[20:18] = 000	PD100, PU20	2 mA (Lv) 3 mA (Hv)	A, F, G1	Z	DV_{DD6}
	Z_STATE	Z	RegA[20:18] = 001					
	MPUIO11	I/O	RegA[20:18] = 010					
V10	MMC.DAT1	I/O	RegA[26:24] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	Z	DV_{DD6}
	MPUIO10	I/O	RegA[26:24] = 001					
	MPUIO7	I/O	RegA[26:24] = 010					

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Table 2−4. ZZG Package Terminal Characteristics (Continued)

ZZG BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING (see Notes 3 and 4)	PULLUP/ PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
P11	MMC.CMD	I/O	RegA[29:27] = 000	PD100, PU20	2 mA (Lv) 3 mA (Hv)	A, F, G1	Z	DV_{DD6}
	GPIO55	I/O	RegA[29:27] = 111					
Y10	MCSI2.CLK	I/O	RegB[5:3] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	LZ	DV_{DD3}
	USB2.SUSP	O	RegB[5:3] = 001					
	USB0.SUSP	O	RegB[5:3] = 101					
	MMC2.CLK	O	RegB[5:3] = 110					
	GPIO27	I/O	RegB[5:3] = 111					
AA9	MCSI2.DIN	I	RegB[8:6] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	LZ	DV_{DD3}
	USB2.VP	I	RegB[8:6] = 001					
	USB0.VP	I	RegB[8:6] = 101					
	GPIO26	I/O	RegB[8:6] = 111					
W9	MCSI2.DOUT	O	RegB[11:9] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G2	0	DV_{DD3}
	USB2.TXEN	O	RegB[11:9] = 001					
	USB0.TXEN	O	RegB[11:9] = 101					
	Z_STATE	Z	RegB[11:9] = 110					
	GPIO25	I/O	RegB[11:9] = 111					
V9	MCSI2.SYNC	I/O	RegB[14:12] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	LZ	DV_{DD3}
	GPIO7	I/O	RegB[14:12] = 001					
	USB2.SPEED	O	RegB[14:12] = 010					
	USB0.SPEED	O	RegB[14:12] = 110					
	MMC2.CMDDIR	O	RegB[14:12] = 111					
R10	MCLKREQ	I	RegB[20:18] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	LZ	DV_{DD3}
	EXT_MASTER_REQ	O	RegB[20:18] = 001					
	UART2.RX	I	RegB[20:18] = 010					
	MMC2.DAT3	I/O	RegB[20:18] = 110					
	GPIO23	I/O	RegB[20:18] = 111					
W8	GPIO9	I/O	RegB[23:21] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G3	LZ	DV_{DD3}
	EMU0	I/O	RegB[23:21] = 011					
	MCSI1.SYNC	I/O	RegB[23:21] = 100					
	MMC2.DAT0	I/O	RegB[23:21] = 110					

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Table 2−4. ZZG Package Terminal Characteristics (Continued)

ZZG BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING (see Notes 3 and 4)	PULLUP/ PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
Y8	GPIO8	I/O	RegB[26:24] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G3	LZ	DV_{DD3}
	$\overline{TRST}$	I	RegB[26:24] = 011					
	MCSI1.DOUT	O	RegB[26:24] = 100					
	MMC2.CMD	I/O	RegB[26:24] = 110					
V8	MPUIO3	I/O	RegB[29:27] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	LZ	DV_{DD3}
	MMC2.DAT1	I/O	RegB[29:27] = 110					
P10	MCBSP2.DR	I	RegC[2:0] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G2	LZ	DV_{DD3}
	MCBSP2.DX	O	RegC[2:0] = 001					
	MCBSP2.DXZ	O/Z	RegC[2:0] = 010					
	GPIO22	I/O	RegC[2:0] = 111					
W7	MCBSP2.FSX	I/O	RegC[5:3] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G2	LZ	DV_{DD3}
	GPIO21	I/O	RegC[5:3] = 111					
V7	MCBSP2.CLKR	I/O	RegC[8:6] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	Z	DV_{DD3}
	GPIO11	I/O	RegC[8:6] = 001					
Y6	MCBSP2.CLKX	I/O	RegC[11:9] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G2	LZ	DV_{DD3}
	GPIO20	I/O	RegC[11:9] = 111					
W6	MCBSP2.FSR	I/O	RegC[14:12] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	Z	DV_{DD3}
	GPIO12	I/O	RegC[14:12] = 001					
AA5	MCBSP2.DX	O	RegC[17:15] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G2	0	DV_{DD3}
	MCBSP2.DR	I	RegC[17:15] = 001					
	MCBSP2.DXZ	O/Z	RegC[17:15] = 010					
	GPIO19	I/O	RegC[17:15] = 111					
R9	UART2.RX	I	RegC[20:18] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	LZ	DV_{DD3}
	USB2.VM	I	RegC[20:18] = 001					
	USB0.VM	I	RegC[20:18] = 101					
	GPIO18	I/O	RegC[20:18] = 111					
Y5	UART2.CTS	I	RegC[23:21] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F	LZ	DV_{DD3}
	USB2.RCV	I	RegC[23:21] = 001					
	GPIO7	I/O	RegC[23:21] = 010					
	USB0.RCV	I	RegC[23:21] = 101					

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20-µA internal pulldown, PD100=100-µA internal pulldown, PU20 = 20-µA internal pullup, PU100 = 100-µA internal pullup. Pullup or pulldown can be enabled or disabled by software.

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVCMOS input/output
B = SUBLVDS input/ouput
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E = Analog oscillator terminals
F = Boundary-scannable terminal
G1 = Terminal may be gated by BFAIL
G2 = Terminal may be gated by GPIO9 and MPUIO3
G3 = Terminal my be gated by BFAIL and OMAP5912 Internal Reset
H1 = Terminal may be 3-stated by BFAIL input
H3 = MCSI1.DOUT pin can be forced into a high-impedance state by the OMAP5912 HIGH_IMP3 control bit
K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

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☆Slew time constraint of the $\overline{EXT\_DMA\_REQ0}$ must be lower than or equal to 10 ns (from 10% to 90% of DV_{DD}) in Mode 1.

NOTES: 3. NA denotes no multiplexing on the ball
4. ‘Regx’ denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

Table 2−4. ZZG Package Terminal Characteristics (Continued)

ZZG BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING (see Notes 3 and 4)	PULLUP/ PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
W5	LOW_STATE	O	RegC[26:24] = 000		2 mA (Lv)	A, F, G2	0	DV_{DD3}
	UART2.RTS	O	RegC[26:24] = 001		3 mA (Hv)			
	USB2.SE0	O	RegC[26:24] = 010					
	MPUIO5	I/O	RegC[26:24] = 011					
	MPUIO12	I/O	RegC[26:24] = 100					
	USB0.SE0	O	RegC[26:24] = 101					
	LOW_STATE	O	RegC[26:24] = 110					
V6	LOW_STATE	O	RegC[29:27] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G2	0	DV_{DD3}
	UART2.TX	O	RegC[29:27] = 001					
	USB2.TXD	O	RegC[29:27] = 010					
	USB0.TXD	O	RegC[29:27] = 101					
	Z_STATE	Z	RegC[29:27] = 110					
	GPIO17	I/O	RegC[29:27] = 111					
Y4	UART2.BCLK	O	RegD[2:0] = 000		2 mA (Lv) 3 mA (Hv)	A, F, G2	0	DV_{DD3}
	SYS_CLK_IN	I	RegD[2:0] = 110					
V5	MCLK	O	RegB[17:15] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	0	DV_{DD3}
	MMC2.DATDIR0	O	RegB[17:15] = 110					
	GPIO24	I/O	RegB[17:15] = 111					
W4	USB.PUEN	O	RegD[5:3] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, F, G1	1	DV_{DD2}
	USB.CLKO	O	RegD[5:3] = 001					
	USB.PUDIS	O	RegD[5:3] = 011					
	Z_STATE	Z	RegD[5:3] = 100					
	$\overline{\text{LOW\_POWER}}$	O	RegD[5:3] = 110					
	GPIO58	I/O	RegD[5:3] = 111					
P9	USB.DP	I/O	USBTCTL[6:4] = 000		18.3 mA (in USB mode)	C	Z	DV_{DD2}
	I2C.SDA	I/O/Z	USBTCTL[6:4] = 100					
	UART1.RX	I	USBTCTL[6:4] = 101					
	USB.PUEN	O	USBTCTL[6:4] = 111					

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20-µA internal pulldown, PD100=100-µA internal pulldown, PU20 = 20-µA internal pullup, PU100 = 100-µA internal pullup. Pullup or pulldown can be enabled or disabled by software.

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

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H3 = MCSI1.DOUT pin can be forced into a high-impedance state by the OMAP5912 HIGH_IMP3 control bit
K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

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NOTES: 3. NA denotes no multiplexing on the ball
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Table 2−4. ZZG Package Terminal Characteristics (Continued)

ZZG BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING (see Notes 3 and 4)	PULLUP/ PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
R8	USB.DM I2C.SCL UART1.TX Z_STATE	I/O I/O/Z O Z	 USBTCTL[6:4] = 100 USBTCTL[6:4] = 101 USBTCTL[6:4] = 111		18.3 mA (in USB mode)	C	Z	DV_{DD2}
Y2	OSC1_IN	I	NA			E	NA	NA
W3	OSC1_OUT	O	NA			E	NA	NA
Y1	$\overline{\text{FLASH.CS1U}}$ GPIO16	O I/O	RegF[14:12] = 000 RegF[14:12] = 111		2 mA (Lv) 3 mA (Hv)	A, F	1	DV_{DD5}
V4	$\overline{\text{FLASH.WP}}$	O	NA		2 mA (Lv) 3 mA (Hv)	A	0	DV_{DD5}
W2	$\overline{\text{FLASH.WE}}$	O	NA		2 mA (Lv) 3 mA (Hv)	A	1	DV_{DD5}
W1	$\overline{\text{FLASH.RP}}$ $\overline{\text{FLASH.CS2UWE}}$	O O	RegF[23:21] = 000 RegF[23:21] = 001		2 mA (Lv) 3 mA (Hv)	A	0	DV_{DD5}
U4	$\overline{\text{FLASH.OE}}$	O	NA		2 mA (Lv) 3 mA (Hv)	A	1	DV_{DD5}
E1 L7 K3 K4 L8 F2 J3 J4 J2	FLASH.A[25:17]	O	NA		2 mA (Lv) 3 mA (Hv)	A, G1	0	DV_{DD5}
K7	FLASH.A[16]	O	Reg11[5:3] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, G1	0	DV_{DD5}
H3	FLASH.A[15]	O	Reg11[8:6] = 000		2 mA (Lv) 3 mA (Hv)	A, G1	0	DV_{DD5}
H4	FLASH.A[14]	O	Reg11[11:9] = 000		2 mA (Lv) 3 mA (Hv)	A, G1	0	DV_{DD5}
K8	FLASH.A[13]	O	Reg11[14:12] = 000		2 mA (Lv) 3 mA (Hv)	A, G1	0	DV_{DD5}
G2	FLASH.A[12]	O	Reg11[17:15] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, G1	0	DV_{DD5}
G3	FLASH.A[11]	O	Reg11[20:18] = 000		2 mA (Lv) 3 mA (Hv)	A, G1	0	DV_{DD5}

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20-µA internal pulldown, PD100=100-µA internal pulldown, PU20 = 20-µA internal pullup, PU100 = 100-µA internal pullup. Pullup or pulldown can be enabled or disabled by software.

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G1 = Terminal may be gated by BFAIL
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H3 = MCSI1.DOUT pin can be forced into a high-impedance state by the OMAP5912 HIGH_IMP3 control bit
K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

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Table 2−4. ZZG Package Terminal Characteristics (Continued)

ZZG BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING (see Notes 3 and 4)	PULLUP/ PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
G4	FLASH.A[10]	O	Reg11[23:21] = 000		2 mA (Lv) 3 mA (Hv)	A, G1	0	DV_{DD5}
F3	FLASH.A[9]	O	Reg11[26:24] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, G1	0	DV_{DD5}
J7	FLASH.A[8]	O	Reg12[5:3] = 000		2 mA (Lv) 3 mA (Hv)	A, G1	0	DV_{DD5}
E3	FLASH.A[7]	O	Reg12[8:6] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, G1	0	DV_{DD5}
F4	FLASH.A[6]	O	Reg12[11:9] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, G1	0	DV_{DD5}
D2	FLASH.A[5]	O	Reg12[14:12] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, G1	0	DV_{DD5}
E4	FLASH.A[4]	O	Reg12[17:15] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, G1	0	DV_{DD5}
C1	FLASH.A[3]	O	Reg12[20:18] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, G1	0	DV_{DD5}
D3	FLASH.A[2]	O	Reg12[23:21] = 000	PU20, PD20	2 mA (Lv) 3 mA (Hv)	A, G1	0	DV_{DD5}
J8	FLASH.A[1]	O	Reg12[26:24] = 000		2 mA (Lv) 3 mA (Hv)	A, G1	0	DV_{DD5}
V3 T4 U3 U1 P8 T3 T2 R4 R3 R2 P7 P4 P2 N7 N2 N4	FLASH.D[15:0]	I/O	NA		2 mA (Lv) 3 mA (Hv)	A, K	0	DV_{DD5}
N3	FLASH.CLK $\overline{\text{FLASH.CS2UOE}}$	O O	Reg10[23:21] = 000 Reg10[23:21] = 001		2 mA (Lv) 3 mA (Hv)	A, K, G1	0	DV_{DD5}
V2	FLASH.RDY GPIO10	I I/O	RegF[29:27] = 000 RegF[29:27] = 001	PU100, PD20	2 mA (Lv) 3 mA (Hv)	A, F	Input	DV_{DD5}
L4	$\overline{\text{FLASH.ADV}}$	O	NA		2 mA (Lv) 3 mA (Hv)	A	1	DV_{DD5}

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20-µA internal pulldown, PD100=100-µA internal pulldown, PU20 = 20-µA internal pullup, PU100 = 100-µA internal pullup. Pullup or pulldown can be enabled or disabled by software.

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Table 2−4. ZZG Package Terminal Characteristics (Continued)

ZZG BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING (see Notes 3 and 4)	PULLUP/ PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
M4	$\overline{\text{FLASH.CS2}}$	O	RegD[8:6] = 000		2 mA (Lv) 3 mA (Hv)	A	1	DV_{DD5}
	$\overline{\text{FLASH.BAA}}$	O	RegD[8:6] = 001					
	$\overline{\text{FLASH.CS2L}}$	O	RegD[8:6] = 010					
M7	GPIO62	I/O	Reg10[2:0] = 000	PU100	2 mA (Lv) 3 mA (Hv)	A, F, G1	Input	DV_{DD5}
	$\overline{\text{FLASH.CS0}}$	O	Reg10[2:0] = 001					
M3	$\overline{\text{FLASH.CS1}}$	O	Reg10[29:27] = 000		2 mA (Lv) 3 mA (Hv)	A	1	DV_{DD5}
	$\overline{\text{FLASH.CS1L}}$	O	Reg10[29:27] = 001					
P3	$\overline{\text{FLASH.CS2U}}$	O	Reg10[20:18] = 000		2 mA (Lv) 3 mA (Hv)	A, F	1	DV_{DD5}
	GPIO5	I/O	Reg10[20:18] = 001					
L3	$\overline{\text{FLASH.BE[0]}}$	O	Reg10[8:6] = 000		2 mA (Lv) 3 mA (Hv)	A, F	0	DV_{DD5}
	$\overline{\text{FLASH.CS2UOE}}$	O	Reg10[8:6] = 001					
	GPIO59	I/O	Reg10[8:6] = 111					
M8	$\overline{\text{FLASH.BE[1]}}$	O	Reg10[5:3] = 000		2 mA (Lv) 3 mA (Hv)	A, F	0	DV_{DD5}
	$\overline{\text{FLASH.CS2UWE}}$	O	Reg10[5:3] = 001					
	GPIO60	I/O	Reg10[5:3] = 111					
N8	$\overline{\text{FLASH.CS3}}$	O	Reg10[26:24] = 000		2 mA (Lv) 3 mA (Hv)	A, F	1	DV_{DD5}
	GPIO3	I/O	Reg10[26:24] = 111					

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20-µA internal pulldown, PD100=100-µA internal pulldown, PU20 = 20-µA internal pullup, PU100 = 100-µA internal pullup. Pullup or pulldown can be enabled or disabled by software.

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NOTES: 3. NA denotes no multiplexing on the ball
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2.4 Signal Description

Table 2−5 provides a description of the signals on OMAP5912. Many signals are available on multiple pins, depending upon the software configuration of the pin multiplexing options.

Table 2−5. Signal Descriptions

SIGNAL	ZDY/ GDY BALL#	ZZG BALL#	DESCRIPTION	TYPE†
EXTERNAL MEMORY INTERFACE FAST (EMIFF) SDRAM INTERFACE				
$\overline{\text{SDRAM.CS}}$	E7	G8	SDRAM chip-select	O
SDRAM.DQSH	A12	C14	DDR DQ strobe high	I/O
SDRAM.DQSL	A2	D4	DDR DQ strobe low	I/O
$\overline{\text{SDRAM.CAS}}$	D5	B4	SDRAM column address strobe. $\overline{\text{SDRAM.CAS}}$ is active (low) during reads, writes, and the REFR and MRS commands to SDRAM memory.	O
SDRAM.DQML	C7	C8	SDRAM lower data mask. Active-high data mask for the lower byte of the SDRAM data bus (SDRAM.D[7:0]). The data mask outputs allow for both 16-bit-wide and 8-bit-wide accesses to SDRAM memory.	O
SDRAM.DQMU	A8	D10	SDRAM upper data mask. Active-high data mask for the upper byte of the SDRAM data bus (SDRAM.D[15:8]). The data mask outputs allow for both 16-bit-wide and 8-bit-wide accesses to SDRAM memory.	O
$\overline{\text{SDRAM.RAS}}$	D4	H7	SDRAM row address strobe. $\overline{\text{SDRAM.RAS}}$ is active (low) during ACTV, DCAB, REFR, and MRS commands to SDRAM memory.	O
$\overline{\text{SDRAM.WE}}$	E6	H8	SDRAM write enable. $\overline{\text{SDRAM.WE}}$ is active (low) during writes, DCAB, and MRS commands to SDRAM memory.	O
SDRAM.A[13:0]	D10 E8 E9 F8 F9 C6 A10 E10 C8 D9 C3 F7 A1 B2	H11 H9 H10 B8 B12 G9 G11 G12 B9 G10 A1 B6 B2 A2	SDRAM address bus. Provides row and column address information to the SDRAM memory as well as MRS command data. SDRAM.A[10] also serves as a control signal to define specific commands to SDRAM memory.	O
SDRAM.BA[1:0]	C4 C5	C3 B3	SDRAM bank address bus. Provides the bank address to SDRAM memories	O
SDRAM.D[15:0]	B10 C10 B11 B9 A11 B8 B12 C9 B7 A3 B6 B3 A5 A4 B5 B4	C12 D12 D13 C11 C13 D11 D14 C10 D8 C4 C7 D5 D7 C5 C6 D6	SDRAM data bus. SDRAM.D[15:0] provides data exchange between the traffic controller and SDRAM memory.	I/O
SDRAM.CLK	A7	C9	SDRAM clock. Clock for synchronization SDRAM memory commands/accesses.	O
SDRAM.CLKX	A6	D9	DDR clock. Inverted clock for synchronization DDR memory commands/accesses	O
SDRAM.CKE	B13	H12	SDRAM clock enable (active-high). Asserting this signal enables the SDRAM clock for normal operation; negating puts SDRAM memory into low-power mode.	O

† I = Input, O = Output, Z = High-Impedance

‡ GPIO13 is used to select between full and fast boot. Set GPIO13 high to boot from the USB peripheral. Set GPIO13 low to boot from external flash on CS3.

Table 2−5. Signal Descriptions (Continued)

SIGNAL	ZDY/ GDY BALL#	ZZG BALL#	DESCRIPTION	TYPE†
EXTERNAL MEMORY INTERFACE SLOW (EMIFS) FLASH AND ASYNCHRONOUS MEMORY INTERFACE				
FLASH.A[25:1]	F3 J4 J2 H2 H5 F4 H4 H3 G6 G5 G2 G4 G3 F5 F1 F2 E1 D1 E2 C1 D2 E3 E4 C2 D3	E1 L7 K3 K4 L8 F2 J3 J4 J2 K7 H3 H4 K8 G2 G3 G4 F3 J7 E3 F4 D2 E4 C1 D3 J8	EMIFS address bus. Address output bus for all EMIFS accesses.	O
FLASH.D[15:0]	N4 R1 P1 K7 M3 M4 N2 L5 N1 K6 L4 M2 J7 L2 M1 L1	V3 T4 U3 U1 P8 T3 T2 R4 R3 R2 P7 P4 P2 N7 N2 N4	EMIFS data bus. Bidirectional 16-bit data bus used to transfer read and write data during EMIFS accesses. The 16-bit data bus becomes address/data in case the EMIFS is configured in address/data multiplexed mode.	I/O
FLASH.CLK	K1	N3	Flash clock. Clock output that is active during synchronous modes of flash operation for synchronous burst flash memories.	O
FLASH.RDY	L6	V2	Flash ready. Active-high ready input used to suspend the flash interface when the external memory or asynchronous device is not ready to continue the current cycle.	I
$\overline{\text{FLASH.ADV}}$	H6	L4	Flash address valid. Active-low control signal used to indicate a valid address is present on the FLASH.A[25:1] bus.	O
$\overline{\text{FLASH.BAA}}$	J8	M4	Flash burst advance acknowledge. Active-low control signal used with Advanced Micro Devices™ E burst flash.	O
$\overline{\text{FLASH.BE[1:0]}}$	K2 J1	M8 L3	Flash byte enables. Active-low byte enable signals used to perform byte-wide accesses to memories or devices that support byte enables.	O
$\overline{\text{FLASH.CS0}}$	J5	M7	Flash chip-select bit 0	O
$\overline{\text{FLASH.CS1}}$	J3	M3	Flash chip-select bit 1	O
$\overline{\text{FLASH.CS1L}}$	J3	M3	Lower half of $\overline{\text{FLASH.CS1}}$ address range	O
$\overline{\text{FLASH.CS1U}}$	T1	Y1	Upper half of $\overline{\text{FLASH.CS1}}$ address range	O
$\overline{\text{FLASH.CS2}}$	J8	M4	Flash chip-select bit 2	O
$\overline{\text{FLASH.CS2L}}$	J8	M4	Lower half of $\overline{\text{FLASH.CS2}}$ address range	O
$\overline{\text{FLASH.CS2U}}$	K3	P3	Upper half of $\overline{\text{FLASH.CS2}}$ address range	O
$\overline{\text{FLASH.CS2UOE}}$	J1 K1	L3 N3	$\overline{\text{FLASH.CS2U}}$ gated with $\overline{\text{FLASH.OE}}$. Output enable if EMIFS is used to interface with external flash.	O
$\overline{\text{FLASH.CS2UWE}}$	K2 N3	M8 W1	$\overline{\text{FLASH.CS2U}}$ gated with $\overline{\text{FLASH.WE}}$. Write enable if EMIFS is used to interface with external flash.	O
$\overline{\text{FLASH.CS3}}$	J6	N8	Flash chip-select bit 3. If MPU_BOOT is high and the device is an emulation device, select external boot memory.	O

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‡ GPIO13 is used to select between full and fast boot. Set GPIO13 high to boot from the USB peripheral. Set GPIO13 low to boot from external flash on CS3.

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Table 2−5. Signal Descriptions (Continued)

SIGNAL	ZDY/ GDY BALL#	ZZG BALL#	DESCRIPTION	TYPE†
EXTERNAL MEMORY INTERFACE SLOW (EMIFS) FLASH AND ASYNCHRONOUS MEMORY INTERFACE (CONTINUED)				
$\overline{\text{FLASH.OE}}$	M5	U4	Flash output enable. Active-low output enable output for Flash or SRAM memories or asynchronous devices.	O
$\overline{\text{FLASH.RP}}$	N3	W1	Flash power down (TI Flash devices) or reset output (Intel® Flash devices)	O
$\overline{\text{FLASH.WE}}$	P3	W2	Flash write enable. Active-low write enable output for Flash or SRAM memories or asynchronous devices.	O
$\overline{\text{FLASH.WP}}$	R3	V4	Flash write protect. Active-low output for hardware write protection feature on standard memory devices.	O
MULTIMEDIA CARD/SECURE DIGITAL INPUT/OUTPUT INTERFACES (MMC/SDIOs)				
MMC.CLK	M8	V11	MMC/SDIO1 clock. Clock output to the MMC/SD card.	O
MMC.CMD	N7	P11	MMC/SDIO1 command. MMC/SD commands are transferred to/from this pin.	I/O
MMC.DAT0	R8	R11	MMC/SDIO1 data bit 0. MMC.DAT0 functions as data bit 0 during MMC and secure digital operation.	I/O
MMC.DAT1	U9	V10	SD card data bit 1. Data bit 1 is used in 4-bit secure digital mode.	I/O
MMC.DAT2	T9 L15	W10 M15	SD card data bit 2. Data bit 2 is used in 4-bit secure digital mode.	I/O
MMC.DAT3	P9	W11	SD card data bit 3. Data bit 3 is used in 4-bit secure digital mode.	I/O
MMC2.CLK	K12 P8	M19 Y10	MMC/SDIO2 clock. Clock output to the MMC/SD card.	O
MMC2.CLKIN	N17	R18	MMC/SDIO2 clock feedback	I
MMC2.CMD	P7 H15	Y8 J19	MMC/SDIO2 command. MMC/SD commands are transferred to/from this pin.	I/O
MMC2.CMDDIR	U8	V9	MMC/SDIO2 command direction control	O
MMC2.DAT0	J12 U7	L15 W8	MMC/SDIO2 data bit 0. MMC2.DAT0 functions as data bit 0 during MMC and secure digital operation.	I/O
MMC2.DAT1	J13 R6	L18 V8	MMC/SDIO2 card data bit 1	I/O
MMC2.DAT2	H16 R12	J18 W15	MMC/SDIO2 card data bit 2	I/O
MMC2.DAT3	J17 T7	L19 R10	MMC/SDIO2 card data bit 3	I/O
MMC2.DATDIR0	U3	V5	MMC/SDIO2 data bit 0 direction control	O
MMC2.DATDIR1	T17	W19	MMC/SDIO2 data bit 1, 2, 3 direction control	O

† I = Input, O = Output, Z = High-Impedance

‡ GPIO13 is used to select between full and fast boot. Set GPIO13 high to boot from the USB peripheral. Set GPIO13 low to boot from external flash on CS3.

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Table 2−5. Signal Descriptions (Continued)

SIGNAL	ZDY/ GDY BALL#	ZZG BALL#	DESCRIPTION	TYPE†
MULTICHANNEL BUFFERED SERIAL PORTS (McBSPs)				
MCBSP1.CLKX	F16	G21	McBSP1 bit clock	I/O
MCBSP1.CLKS	G13	G20	McBSP1 clock input	I
MCBSP1.DR	G17	H20	McBSP1 data input	I
MCBSP1.DX	G14	H18	McBSP1 data output	O
	G15	H15		
MCBSP1.DXZ	G15	H15	McBSP1 data output (for multichannel mode)	O/Z
	G14	H18		
MCBSP1.FSX	G15	H15	McBSP1 frame synchronization	I/O
	G14	H18		
MCBSP2.CLKR	U6	V7	McBSP2 receive clock	I/O
MCBSP2.CLKX	U5	Y6	McBSP2 transmit clock	I/O
MCBSP2.DR	L8	P10	McBSP2 data input	I
	T5	AA5		
MCBSP2.DX	L8	P10	McBSP2 data output	O
	T5	AA5		
MCBSP2.DXZ	L8	P10	McBSP2 data output (for multichannel mode)	O/Z
	T5	AA5		
MCBSP2.FSR	R5	W6	McBSP2 receive frame synchronization	I/O
MCBSP2.FSX	N6	W7	McBSP2 transmit frame synchronization	I/O
MCBSP3.CLKX	U14	W16	McBSP3 clock	I/O
	R17	N14		
	U15	P14		
MCBSP3.DR	N10	AA17	McBSP3 data input	I
	P14	U18		
	P12	V15		
	M14	T19		
MCBSP3.DX	U15	P14	McBSP3 data output	O
	R15	W21		
	P11	W14		
MCBSP3.DXZ	R15	W21	McBSP3 data output (for multichannel mode)	O/Z
MCBSP3.FSX	L16	N18	McBSP3 frame synchronization	I/O
	L13	P18		
	L14	P19		
	M17	P20		
	N10	AA17		

† I = Input, O = Output, Z = High-Impedance

‡ GPIO13 is used to select between full and fast boot. Set GPIO13 high to boot from the USB peripheral. Set GPIO13 low to boot from external flash on CS3.

Table 2−5. Signal Descriptions (Continued)

SIGNAL	ZDY/ GDY BALL#	ZZG BALL#	DESCRIPTION	TYPE†
MULTICHANNEL SERIAL INTERFACES (MCSIs)				
MCSI1.CLK	U15 L15	P14 M15	MCSI1 bit clock	I/O
MCSI1.DIN	L14 P12 U14	P19 V15 W16	MCSI1 data input	I
MCSI1.DOUT	P11 P7	W14 Y8	MCSI1 data output	O
MCSI1.DIN_OUT	U14	W16	MCSI1 data-in looped backout	O
MCSI1.SYNC	N10 U7	AA17 W8	MCSI1 frame synchronization	I/O
MCSI2.CLK	P8	Y10	MCSI2 bit clock	I/O
MCSI2.DIN	R7	AA9	MCSI2 data input	I
MCSI2.DOUT	T8	W9	MCSI2 data output	O
MCSI2.SYNC	U8	V9	MCSI2 frame synchronization	I/O
SERIAL PORT INTERFACE (SPI)				
$\overline{\text{SPIF.CS0}}$	R17	N14	SPI output chip-selects in master mode/input chip-select when SPI is in slave mode.	I/O
$\overline{\text{SPIF.CS1}}$	L12	N15		O
$\overline{\text{SPIF.CS2}}$	M14	T19		
$\overline{\text{SPIF.CS3}}$	R16	P15		
SPIF.SCK	N15	U19	SPI output clock in master mode. SPI input clock in slave mode.	I/O
SPIF.DIN	M17	P20	SPI data-In in master mode. SPI data-out in slave mode.	I/O
	P14	U18		I/O
SPIF.DOUT	N17	R18	SPI data-out in master mode. SPI data-in in slave mode.	I/O
	R15	W21		I/O
UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER (UART) INTERFACES				
UART1.CTS	M9	R14	UART1 clear to send	I
UART1.DSR	P14 T17	U18 W19	UART1 data set ready	I
UART1.DTR	R15 N16	W21 T20	UART1 data terminal ready	O
UART1.RTS	R11	AA15	UART1 request to send	O
UART1.RX	U13 T2	V14 P9	UART1 receive data	I
UART1.TX	T12 U1 U12	Y14 R8 R13	UART1 transmit data	O
UART1.IRTX	T12	Y14	UART1 IrDA transmit data	O
UART1.IRRX	U13	V14	UART1 IrDA receive data	I

† I = Input, O = Output, Z = High-Impedance

‡ GPIO13 is used to select between full and fast boot. Set GPIO13 high to boot from the USB peripheral. Set GPIO13 low to boot from external flash on CS3.

Table 2−5. Signal Descriptions (Continued)

SIGNAL	ZDY/ GDY BALL#	ZZG BALL#	DESCRIPTION	TYPE†
UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER (UART) INTERFACES (CONTINUED)				
UART1.IRSEL	M9	R14	UART1 IrDA mode select for external transceiver	O
UART1.IRSHDN	R11	AA15	UART1 IrDA mode select for external transceiver	O
UART2.BCLK	P5	Y4	UART2 baud clock. A clock of 16x	O
UART2.CTS	P6	Y5	UART2 clear to send	I
	J12	L15		
UART2.RTS	T4	W5	UART2 request to send	O
	K12	M19		
UART2.RX	U4	R9	UART2 receive data	I
	T7	R10		
	K15	L14		
UART2.TX	R4	V6	UART2 transmit data	O
	K17	M18		
UART3.CTS	R12	W15	UART3 clear to send	I
	T17	W19		
	J14	K15		
	P15	V19		
UART3.DSR	P14	U18	UART3 data set ready	I
UART3.DTR	R15	W21	UART3 data terminal ready	O
UART3.RTS	M15	R19	UART3 request to send in UART mode SD_MODE in IrDA mode	O
	L10	Y15		
	J16	K14		
	N16	T20		
	R15	W21		
UART3.RX	K15	L14	UART3 receive data	I
	H13	K19		
	R16	P15		
UART3.TX	K17	M18	UART3 transmit data	O
	J11	K18		
	R17	N14		
USB (INTEGRATED TRANSCEIVER)				
USB.DM	U1	R8	USB differential (–) line	I/O
USB.DP	T2	P9	USB differential (+) line	I/O

† I = Input, O = Output, Z = High-Impedance

‡ GPIO13 is used to select between full and fast boot. Set GPIO13 high to boot from the USB peripheral. Set GPIO13 low to boot from external flash on CS3.

Table 2−5. Signal Descriptions (Continued)

SIGNAL	ZDY/ GDY BALL#	ZZG BALL#	DESCRIPTION	TYPE†
USB PORT 0				
USB0.RCV	P6	Y5	USB port 0 receive data	I
USB0.SE0	T4	W5	USB port 0 single-ended zero	O
USB0.SPEED	U8	V9	USB 0 speed	O
USB0.SUSP	P8	Y10	USB 0 suspend	O
USB0.TXD	R4	V6	USB port 0 transmit data	O
USB0.TXEN	T8	W9	USB port 0 transmit enable	O
USB0.VM	U4	R9	USB port 0 V minus receive data	I
USB0.VP	R7	AA9	USB port 0 V plus receive data	I
USB PORT 1				
USB1.RCV	P12	V15	USB port 1 receive data	I
USB1.SE0	N9	W13	USB port 1 single-ended zero	O
USB1.SPEED	U12	R13	USB port 1 bus segment speed control	O
USB1.SUSP	H14	J20	USB port 1 bus segment suspend control	O
USB1.TXD	P11	W14	USB port 1 transmit data	O
USB1.TXEN	U14	W16	USB port 1 transmit enable	O
USB1.VM	U15	P14	USB port 1 V minus receive data	I
USB1.VP	N10	AA17	USB port 1 V plus receive data	I
USB PORT 2				
USB2.RCV	P6	Y5	USB port 2 receive data	I
USB2.SE0	T4	W5	USB port 2 single-ended zero	O
USB2.SPEED	U8	V9	Low-speed USB device or full-speed USB device	O
USB2.SUSP	P8	Y10	USB port 2 bus segment suspend control	O
USB2.TXD	R4	V6	USB port 2 transmit data	O
USB2.TXEN	T8	W9	USB port 2 transmit enable	O
USB2.VM	U4	R9	USB port 2 V minus receive data	I
USB2.VP	R7	AA9	USB port 2 V plus receive data	I
UNIVERSAL SERIAL BUS (USB) MISCELLANEOUS SIGNALS				
USB.CLKO	P4	W4	USB clock output. 6-MHz divided clock output of the internal USB DPLL provided for reference. Common for all USB host and function peripherals.	O
USB.VBUS	N17	R18	USB voltage bus enable. USB.VBUS is an input which allows the OMAP5912 device to detect whether the USB cable is connected or not. USB.VBUS must be connected to USB power from the USB cable through a voltage translation buffer to convert the 5-V power from the USB cable to within the 3.3-V nominal range specified for the OMAP device input.	I
USB.PUEN	P4 T2	W4 P9	USB pullup enable	O
USB.PUDIS	P4	W4	USB pullup disable	O

† I = Input, O = Output, Z = High-Impedance

‡ GPIO13 is used to select between full and fast boot. Set GPIO13 high to boot from the USB peripheral. Set GPIO13 low to boot from external flash on CS3.

Table 2−5. Signal Descriptions (Continued)

SIGNAL	ZDY/ GDY BALL#	ZZG BALL#	DESCRIPTION	TYPE†
INTER-INTEGRATED CIRCUIT (I^2C) MASTER AND SLAVE INTERFACE				
I2C.SCL	P16 U1	T18 R8	I^2C serial clock	I/O
I2C.SDA	M11 T2	V20 P9	I^2C serial data	I/O
HDQ/1-Wire INTERFACE				
HDQ	K13	N20	HDQ/1-Wire interface. HDQ optionally implements one of two serial protocols: HDQ or 1-Wire.	I/O
MICROWIRE™ INTERFACE				
$\overline{\text{UWIRE.CS0}}$	R17 H16	N14 J18	MICROWIRE chip-select 0. The output selects a single MICROWIRE device (configurable as active-high or active-low).	O
$\overline{\text{UWIRE.CS1}}$	L12	N15	MICROWIRE chip-select 1	
$\overline{\text{UWIRE.CS2}}$	M14	T19	MICROWIRE chip-select 2	
$\overline{\text{UWIRE.CS3}}$	R16 H15	P15 J19	MICROWIRE chip-select 3	
UWIRE.SCLK	P15 G16	V19 J15	MICROWIRE serial clock. This pin drives a clock to a MICROWIRE device. The active edge is software-configurable.	O
UWIRE.SDI	P14 H17	U18 J14	MICROWIRE serial data input	I
UWIRE.SDO	R15 H12	W21 H19	MICROWIRE serial data output	O
CAMERA INTERFACE				
CAM.OUTCLK	L10	Y15	Camera output clock	O
CAM.D[7:0]	H16 H15 H17 J11 H13 J14 J16 J17	J18 J19 J14 K18 K19 K15 K14 L19	Camera digital image data bits	I
CAM.HS	J12	L15	Camera interface horizontal synchronization. Horizontal synchronization input from external camera sensor.	I
CAM.LCLK	G16	J15	Camera interface line clock. Input clock to provide external timing reference from camera sensor logic	I
CAM.RSTZ	K12	M19	Camera interface reset. Reset output used to reset or Initialize external camera sensor logic.	O
CAM.VS	J13	L18	Camera vertical synchronization	I
CAM.EXCLK	H12	H19	Camera interface external clock. Output clock used to provide a timing reference to a camera sensor.	O

† I = Input, O = Output, Z = High-Impedance

‡ GPIO13 is used to select between full and fast boot. Set GPIO13 high to boot from the USB peripheral. Set GPIO13 low to boot from external flash on CS3.

MICROWIRE is a registered trademark of National Semiconductor Corporation.

Table 2−5. Signal Descriptions (Continued)

SIGNAL	ZDY/ GDY BALL#	ZZG BALL#	DESCRIPTION	TYPE†
LCD AND LCDCONV INTERFACE				
LCD.AC	F10	B15	LCD AC-bias. LCD.AC signals the LCD display to switch the polarity of the row and column power supplies to counteract charge buildup causing DC offset. In TFT mode, LCD.AC is used as the output enable to latch LCD pixel data using the pixel clock.	O
LCD.BLUE0	L17	N19	Blue bit 0 in 18-bit LCD output mode	O
LCD.HS	D15	C20	LCD horizontal sync. LCD_HSYNC is the line clock that signals the end of a line of pixels to the LCD display panel. In TFT mode, LCD_HSYNC is the horizontal synchronization signal.	O
LCD.PCLK	A14	C15	LCD pixel clock output. Clock output provided to synchronize pixel data to LCD display panels. In passive mode, LCD_PCLK transitions only when LCD.P[15:0] is valid. In active mode, LCD_PCLK transitions continuously and LCD.AC is used as the output enable when LCD.P[15:0] is valid.	O
LCD.P[15:0]	C12 D12 E11 A13 B14 A15 F11 C13 D13 A16 C15 E12 D14 C16 B16 A17	D15 C16 A17 G13 B17 C17 D16 D17 C18 B19 A20 H13 G14 C19 B21 D18	LCD pixel data bits	O
LCD.RED0	K14	N21	Red bit 0 in 18-bit LCD output mode	O
LCD.VS	B15	B18	LCD vertical synchronization (sync) output. LCD.VS is the frame clock that signals the start of a new frame of pixels to the LCD display panel. In TFT mode, LCD.VS is the vertical synchronization signal.	O

† I = Input, O = Output, Z = High-Impedance

‡ GPIO13 is used to select between full and fast boot. Set GPIO13 high to boot from the USB peripheral. Set GPIO13 low to boot from external flash on CS3.

Table 2−5. Signal Descriptions (Continued)

SIGNAL	ZDY/ GDY BALL#	ZZG BALL#	DESCRIPTION	TYPE†
JTAG/EMULATION INTERFACE				
TCK	P13 L15	W18 M15	IEEE Standard 1149.1 test clock. TCK is normally a free-running clock signal with a 50% duty cycle. The changes on the test access port (TAP) of input signals TDI and TMS are clocked into the TAP controller, instruction register, or selected test data register on the rising edge of TCK. Changes at the TAP output signal TDO occur on the falling edge of TCK.	I
RTCK	T14 N15	Y17 U19	ARM926EJ-S return clock emulation	I/O
RTDX.D[0]	M16	M14	Emulation data transmit	I/O
RTDX.D[1]	L13	P18	Emulation data transmit	I/O
RTDX.D[2]	L15	M15	Emulation data transmit	I/O
RTDX.D[3]	K13	N20	Emulation data transmit	I/O
TDI	U17 U15	Y19 P14	IEEE Standard 1149.1 test data input. TDI is clocked into the selected register (instruction or data) on the rising edge of TCK.	I
TDO	P11 T15	W14 AA19	IEEE Standard 1149.1 test data output. The contents of the selected register (instruction or data) are shifted out of TDO on the falling edge of TCK. TDO is in the high-impedance state except when the scanning of data is in progress.	O
TMS	M10 L14	V17 P19	IEEE Standard 1149.1 test mode select. This serial control input is clocked into the TAP controller on the rising edge of TCK.	I
$\overline{\text{TRST}}$	R13 P7	Y18 Y8	IEEE Standard 1149.1 test reset. $\overline{\text{TRST}}$, when high, gives the IEEE standard 1149.1 scan system control of the operations of the device. If $\overline{\text{TRST}}$ is not connected, or driven low, the device operates in its functional mode, and the IEEE standard 1149.1 signals are ignored. **WARNING:** By default, the internal pulldown on $\overline{\text{TRST}}$ is disabled. An external pulldown is needed for proper operation of the device in functional mode.	I
EMU1	N11 P12	W17 V15	Emulation pin 1. When $\overline{\text{TRST}}$ is driven high, EMU1 is used as an interrupt to or from the emulator system and is defined as input/output by way of the IEEE standard 1149.1 scan system.	I/O
EMU0	U16 U7	V16 W8	EMU0 V16 Emulation pin 0. When $\overline{\text{TRST}}$ is driven high, EMU0 is used as an interrupt to or from the emulator system and is defined as input/output by way of the IEEE standard 1449.1 scan system.	I/O

† I = Input, O = Output, Z = High-Impedance

‡ GPIO13 is used to select between full and fast boot. Set GPIO13 high to boot from the USB peripheral. Set GPIO13 low to boot from external flash on CS3.

Table 2−5. Signal Descriptions (Continued)

SIGNAL	ZDY/ GDY BALL#	ZZG BALL#	DESCRIPTION	TYPE†
SHARED GENERAL-PURPOSE IO MODULES (GPIOs)				
GPIO63	E15	E18	General-Purpose IOs module 4. GPIO pins can be accessed and controlled by either the DSP Public Peripheral Bus or the MPU Public Peripheral Bus.	I/O
GPIO62	J5 G13	M7 G20		
GPIO61	B17	D19		
GPIO60	K2	M8		
GPIO59	J1	L3		
GPIO58	R8 P4	R11 W4		
GPIO57	M8 H12	V11 H19		
GPIO56	P12	V15		
GPIO55	N7 N9	P11 W13		
GPIO54	F16	G21		
GPIO53	G15	H15		
GPIO52	G14	H18		
GPIO51	G17	H20		
GPIO50	K17	M18		
GPIO49	K15	L14		
GPIO48	M11	V20		

† I = Input, O = Output, Z = High-Impedance

‡ GPIO13 is used to select between full and fast boot. Set GPIO13 high to boot from the USB peripheral. Set GPIO13 low to boot from external flash on CS3.

Table 2−5. Signal Descriptions (Continued)

SIGNAL	ZDY/ GDY BALL#	ZZG BALL#	DESCRIPTION	TYPE†
SHARED GENERAL-PURPOSE IO MODULES (GPIOs) (CONTINUED)				
GPIO47	P14	U18	General-Purpose IOs module 3. GPIO pins can be accessed and controlled by either the DSP Public Peripheral Bus or the MPU Public Peripheral Bus.	I/O
GPIO46	R15	W21		
GPIO45	R17	N14		
GPIO44	R16	P15		
GPIO43	U15	P14		
GPIO42	U14	W16		
GPIO41	N12	AA20		
GPIO40	R12	W15		
GPIO39	R11	AA15		
	G16	J15		
GPIO38	M9	R14		
	J12	L15		
GPIO37	U13	V14		
	K12	M19		
GPIO36	U12	R13		
GPIO35	H16	J18		
	D12	C16		
GPIO34	H15	J19		
	E11	A17		
GPIO33	H17	J14		
	A13	G13		
GPIO32	J11	K18		
	B14	B17		

† I = Input, O = Output, Z = High-Impedance

‡ GPIO13 is used to select between full and fast boot. Set GPIO13 high to boot from the USB peripheral. Set GPIO13 low to boot from external flash on CS3.

Table 2−5. Signal Descriptions (Continued)

SIGNAL	ZDY/ GDY BALL#	ZZG BALL#	DESCRIPTION	TYPE†
SHARED GENERAL-PURPOSE IO MODULES (GPIOs) (CONTINUED)				
GPIO31	H13 A15	K19 C17	General-Purpose IOs module 2. GPIO pins can be accessed and controlled by either the DSP Public Peripheral Bus or the MPU Public Peripheral Bus.	I/O
GPIO30	J14 F11	K15 D16		
GPIO29	J16 C13	K14 D17		
GPIO28	F17	G19		
GPIO27	P8 D16	Y10 C21		
GPIO26	R7	AA9		
GPIO25	T8	W9		
GPIO24	U3	V5		
GPIO23	T7	R10		
GPIO22	L8	P10		
GPIO21	N6	W7		
GPIO20	U5	Y6		
GPIO19	T5	AA5		
GPIO18	P11 U4	W14 R9		
GPIO17	L10 R4	Y15 V6		
GPIO16	T1	Y1		

† I = Input, O = Output, Z = High-Impedance

‡ GPIO13 is used to select between full and fast boot. Set GPIO13 high to boot from the USB peripheral. Set GPIO13 low to boot from external flash on CS3.

Table 2−5. Signal Descriptions (Continued)

SIGNAL	ZDY/ GDY BALL#	ZZG BALL#	DESCRIPTION	TYPE†
SHARED GENERAL-PURPOSE IO MODULES (GPIOs) (CONTINUED)				
GPIO15	K16	M20	General-Purpose IOs module 1. GPIO pins can be accessed and controlled by either the DSP Public Peripheral Bus or the MPU Public Peripheral Bus.	I/O
GPIO14	K14	N21		
GPIO13‡	L17	N19		
GPIO12	L16	N18		
	R5	W6		
GPIO11	K13	N20		
	U6	V7		
GPIO10	L6	V2		
GPIO9	U7	W8		
GPIO8	P7	Y8		
GPIO7	L15	M15		
	U8	V9		
	P6	Y5		
GPIO6	L14	P19		
GPIO5	K3	P3		
GPIO4	M17	P20		
GPIO3	L13	P18		
	J6	N8		
GPIO2	M16	M14		
	C12	D15		
GPIO1	M15	R19	Value sampled at power-up reset selects protocol on EMIFS interface. If 0 is sampled, protocol is non-address/data multiplexed. If 1 is sampled, protocol is address/data multiplexed.	I/O
GPIO0	N17	R18		

† I = Input, O = Output, Z = High-Impedance

‡ GPIO13 is used to select between full and fast boot. Set GPIO13 high to boot from the USB peripheral. Set GPIO13 low to boot from external flash on CS3.

Table 2−5. Signal Descriptions (Continued)

SIGNAL	ZDY/ GDY BALL#	ZZG BALL#	DESCRIPTION	TYPE†
MPU GENERAL-PURPOSE IO (MPUIOs)				
MPUIO15	F13	E19	MPU general-purpose I/O. MPUIO pins may only be used by the MPU core.	I/O
MPUIO14	J13 N14	L18 U20		
MPUIO13	D17	E20		
MPUIO12	J17 T4	L19 W5		
MPUIO11	T9	W10		
MPUIO10	U9 E16	V10 H14		
MPUIO9	P9 E17	W11 F19		
MPUIO8	F15	G18		
MPUIO7	U9	V10		
MPUIO6	C17 P9	D20 W11		
MPUIO5	N16 T4	T20 W5		
MPUIO4	M14	T19		
MPUIO3	R6	V8		
MPUIO2	L12	N15		
MPUIO1	N15 P15	U19 V19		
MPUIO0	F14 U12	F18 R13		
KEYBOARD MATRIX INTERFACE				
KB.C[7:0]	P15 R16 F17 D16 E15 B17 C17 F14	V19 P15 G19 C21 E18 D19 D20 F18	Keyboard matrix column outputs. KB.Cx column outputs are used in conjunction with the KB.Rx row inputs to implement a 6 x 5 or 8 x 8 keyboard matrix.	O
KB.R[7:0]	K16 K14 L17 F13 D17 E16 E17 F15	M20 N21 N19 E19 E20 H14 F19 G18	Keyboard matrix row inputs. KB.Rx row inputs are used in conjunction with the KB.Cx column outputs to implement a 6 x 5 or 8 x 8 keyboard matrix.	I
LED PULSE GENERATOR (LPG)				
LED1	L13	P18	LED pulse generator output 1. LED1 produces a static or pulsing output used to drive an external LED indicator.	O
LED2	M14	T19	LED pulse generator output 2. LED2 produces a static or pulsing output used to drive an external LED indicator.	O

† I = Input, O = Output, Z = High-Impedance

‡ GPIO13 is used to select between full and fast boot. Set GPIO13 high to boot from the USB peripheral. Set GPIO13 low to boot from external flash on CS3.

Table 2−5. Signal Descriptions (Continued)

SIGNAL	ZDY/ GDY BALL#	ZZG BALL#	DESCRIPTION	TYPE†
PULSE-WIDTH TONE (PWT) AND PULSE-WIDTH LIGHT (PWL) INTERFACE				
PWL	K15	L14	Pulse-width light output. The PWL output pin provides a pseudo-random modulated voltage output used for LCD or keypad backlighting.	O
PWT	K17	M18	Pulse-width tone output. The PWT output pin provides a modulated output for use with an external buzzer.	O
GENERAL-PURPOSE TIMERS				
TIMER.EVENT3	L14	P19	Event capture input signal for GP timer 3	I
TIMER.EVENT4	M17	P20	Event capture input signal for GP timer 4	I
TIMER.EXTCLK	L16	N18	Input clock for the GP timers	I
TIMER.PWM2	K16	M20	PWM output of GP timer 2	O
TIMER.PWM1	K15	L14	PWM output of GP timer 1	O
TIMER.PWM0	K17	M18	PWM output of GP timer 0	O
EMBEDDED TRACE MACROCELL™ (ETM™) INTERFACE				
ETM.CLK	G16	J15	ETM9™ trace clock	O
ETM.PSTAT[5:0]	K13 M16 L13 J13 J12 K12	N20 M14 P18 L18 L15 M19	ETM9 trace pipe state bits	O
ETM.D[7:0]	H16 H15 H17 J11 H13 J14 J16 J17	J18 J19 J14 K18 K19 K15 K14 L19	ETM9 trace packet bits	O
ETM.SYNC[1:0]	L15 H12	M15 H19	ETM9 trace synchronization bits	O
DEVICE CLOCK PINS				
CLK32K_IN	T11	P13	32-kHz clock input. Digital CMOS 32-kHz clock input driven by an external 32-kHz oscillator if the internal 32-kHz oscillator is not used.	I
CLK32K_OUT	U12	R13	32-kHz clock output. Clock output reflecting the internal 32-kHz clock.	O
OSC32K_IN	U11	V13	32-kHz crystal XI connection. Analog clock input to 32-kHz oscillator for use with external crystal.	I
OSC32K_OUT	U10	AA13	32-kHz crystal XO connection. Analog output from 32-kHz oscillator for use with external crystal.	O
SYS_CLK_IN	P5	Y4	Reserved	I
SYS_CLK_OUT	F10	B15	Reserved	O
OSC1_IN	R2	Y2	Base crystal XI connection. Analog input to base oscillator for use with external crystal or to be driven by external 19.2-MHz or 12/13-MHz oscillator. (Reset Mode 0)	I
OSC1_OUT	P2	W3	Base crystal XO connection. Analog output from base oscillator for use with external 19.2-MHz or 12/13-MHz crystal. (Reset Mode 0)	O
BCLK	L10	Y15	General-purpose clock output that can be configured to run at 12 or 13 MHz (depending on base oscillator frequency) or 48 MHz. BCLK can be configured to drive constantly or only when the BCLKREQ signal is asserted active-high.	O
BCLKREQ	R12	W15	BCLK clock request. Active-high request input that allows an external device to request that BCLK be driven.	I

† I = Input, O = Output, Z = High-Impedance

‡ GPIO13 is used to select between full and fast boot. Set GPIO13 high to boot from the USB peripheral. Set GPIO13 low to boot from external flash on CS3.

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Table 2−5. Signal Descriptions (Continued)

SIGNAL	ZDY/ GDY BALL#	ZZG BALL#	DESCRIPTION	TYPE†
DEVICE CLOCK PINS (CONTINUED)				
MCLK	U3	V5	General-purpose master clock output that may be configured to run at 12 or 13 MHz (depending on base oscillator frequency) or 48 MHz. MCLK can be configured to drive constantly or only when the MCLKREQ signal is asserted active-high.	O
MCLKREQ	T7	R10	MCLK clock request. Active-high request input that allows an external device to request that MCLK be driven.	I
RESET LOGIC PINS				
$\overline{\text{PWRON\_RESET}}$	N8	R12	Reset input to device. Active-low asynchronous reset input resets the entire OMAP5912 device.	I
$\overline{\text{MPU\_RST}}$	N14	U20	MPU reset input. Active-low asynchronous reset input resets the MPU core. NOTE: $\overline{\text{MPU\_RST}}$ must meet minimum specified pulse width requirements and must be free of glitching to guard against potential operational issues.	I
$\overline{\text{RST\_OUT}}$	N12	AA20	Reset output. Active-low output is asserted when $\overline{\text{RST\_OUT}}$ is active (after synchronization).	O
INTERRUPTS AND MISCELLANEOUS CONTROL AND CONFIGURATION PINS				
MPU_BOOT	H14	J20	MPU boot mode. Pull this signal high to the I/O rail during boot. Protocol (address/data multiplexed or address/data non-multiplexed) is determined by the value on GPIO1.	I
BFAIL/$\overline{\text{EXT\_FIQ}}$	T17	W19	Battery power failure and external FIQ interrupt input. BFAIL can be used to gate certain input pins when battery power is low or failing. The pins that can be gated are configured via software. This pin can also optionally be used as an external FIQ interrupt source to the MPU. The function of this pin is configurable via software. For more details, see the *OMAP5912 Multimedia Processor Power Management Reference Guide* (literature number SPRU753).	I
$\overline{\text{EXT\_DMA\_REQ0}}$	L12	N15	External DMA request. $\overline{\text{EXT\_DMA\_REQ0}}$ provides DMA request inputs which external devices can use to trigger system DMA transfers. The system DMA must be configured in software to respond to these external requests.	I
$\overline{\text{EXT\_DMA\_REQ1}}$	M14	T19	External DMA request. $\overline{\text{EXT\_DMA\_REQ1}}$ provides DMA request inputs which external devices may use to trigger system DMA transfers. The system DMA must be configured in software to respond to these external requests.	I
LOW_PWR	N16	T20	Low-power request output. This active-high output indicates that the OMAP5912 device is in a LOW_PWR sleep mode. During reset and functional modes, LOW_PWR is driven low. This signal can be used to indicate a low-power state to external power management devices in a system.	O
$\overline{\text{LOW\_POWER}}$	P4	W4	Inverted polarity of the LOW_PWR signal	O
$\overline{\text{RTC\_ON\_NOFF}}$	P10	Y12	Active-low asynchronous reset signal if real-time clock (RTC) is used.	I
RTC_WAKE_INT	N9	W13	RTC wake-up interrupt. RTC periodic interrupt to external power device to restart the main power supplies when RTC times out.	O

† I = Input, O = Output, Z = High-Impedance

‡ GPIO13 is used to select between full and fast boot. Set GPIO13 high to boot from the USB peripheral. Set GPIO13 low to boot from external flash on CS3.

Table 2−5. Signal Descriptions (Continued)

SIGNAL	ZDY/ GDY BALL#	ZZG BALL#	DESCRIPTION	TYPE†
INTERRUPTS AND MISCELLANEOUS CONTROL AND CONFIGURATION PINS (CONTINUED)				
EXT_MASTER_REQ	T7	R10	External master request. If the base clock is provided by an external device instead of an on-chip oscillator, a high level on this output indicates to the external device that the clock must be driven. A low level indicates that the OMAP5912 device is in sleep mode and the 12- or 13-MHz external clock source is not necessary.	O
RST_HOST_OUT	N9	W13	A software-controllable reset or shutdown output to an external device	O
CONF	R14	V18	OMAP5912 configuration input. Must be tied low for normal operations.	I
POWER SUPPLIES				
CV_{DD}	C11 K5 M7 T16	A15 M2 Y9 Y20	Core supply voltage. Supplies power to OMAP5912 core logic and low-voltage sections of I/O.	Power
CV_{DD1}	T3	AA3	Core supply voltage 1. Supplies power to OMAP5912 core logic.	Power
CV_{DD2}	H7 G9 G8	A3 A9 E2	Core supply voltage 2. Supplies power to the MPU subsystem logic and memory.	Power
CV_{DD3}	G10 H11 K11 J10	B13 B20 J21 R20	Core supply voltage 3. Supplies power to the DSP subsystem logic and memory. If the DSP system is not used, can be grounded after the isolation control in ULPD is set.	Power
CV_{DDRTC}	L9	W12	Core supply voltage for the RTC. Supplies power to the RTC core logic. Can be connected to CV_{DD} if the RTC is not used as a standalone.	Power
CV_{DDA}	P17	Y21	Analog supply voltage. Supplies power to the analog phase-locked loop (APLL) used to provide 48-MHz clock to peripherals such as USB, UART, or MMC/SD/SDIO peripherals. Note: The voltage to this supply pin must be kept as clean as possible to maximize performance by minimizing clock jitter.	Power
CV_{DDDLL}	A9	A11	Core supply voltage for the digitally controlled delay element (calibration module) used to control read and write timings to external dual data rate (DDR) SDRAM. It is recommended that an RC (R = 10 Ω, C = 100 nF) low-pass filter be implemented externally to filter switching noises.	Power
DV_{DD1}	C14 G12	A19 E21	I/O supply voltage 1. Supplies power to the majority of peripheral I/O buffers. DV_{DD1} can be connected in common with the other DV_{DD} supplies if the same operating voltage is desired.	Power
DV_{DD2}	U2	AA2	I/O supply voltage 2. Supplies power to the internal USB transceiver buffers of USB port 0. DV_{DD2} can optionally be used for USB connect and disconnect detection by connecting DV_{DD2} to the power from the USB bus in the system. DV_{DD2} can be connected in common with the other DV_{DD} supplies if the same operating voltage is desired.	Power
DV_{DD3}	T6	Y7	I/O supply voltage 3. Supplies power to the MCSI2 and McBSP2 peripheral I/O buffers as well as to GPIO[9:8] I/O buffers. The DV_{DD3} supply can operate within a high-voltage or low-voltage range. DV_{DD3} can be connected in common with the other DV_{DD} supplies if the same operating voltage is desired.	Power
DV_{DD4}	D6 D7 D8 D11	A5 A7 B10 B14	I/O supply voltage 4. Supplies power to the DDR/SDRAM interface I/O buffers. The DV_{DD4} supply can operate within a high-voltage or low-voltage range. DV_{DD4} can be connected in common with the other DV_{DD} supplies if the same operating voltage is desired.	Power
DV_{DD5}	B1 G1 L3	C2 H2 R1	I/O supply voltage 5. Supplies power to the flash interface I/O buffers. The DV_{DD5} supply can operate within a high-voltage or low-voltage range. DV_{DD5} can be connected in common with the other DV_{DD} supplies if the same operating voltage is desired.	Power

† I = Input, O = Output, Z = High-Impedance

‡ GPIO13 is used to select between full and fast boot. Set GPIO13 high to boot from the USB peripheral. Set GPIO13 low to boot from external flash on CS3.

Table 2−5. Signal Descriptions (Continued)

SIGNAL	ZDY/ GDY BALL#	ZZG BALL#	DESCRIPTION	TYPE†
POWER SUPPLIES (CONTINUED)				
DV_{DD6}	T10	AA11	I/O supply voltage 6. Supplies power to the MMC/SD1 interface I/O buffers. DV_{DD6} can be connected in common with the other DV_{DD} supplies if the same operating voltage is desired.	Power
DV_{DD7}	T13	Y16	I/O supply voltage 7. Supplies power to the McBSP3, MCSI1, UART, and USB port 1 I/O buffers. DV_{DD7} can be connected in common with the other DV_{DD} supplies if the same operating voltage is desired.	Power
DV_{DD8}	J15	L21	I/O supply voltage 8. Supplies power to the camera interface (I/F) and embedded trace macrocell (ETM) I/O buffers. DV_{DD8} can be connected in common with the other DV_{DD} supplies if the same operating voltage is desired.	Power
DV_{DD9}	M13	U21	I/O supply voltage 9. Supplies power to the GPIO (except GPIO[9:8]), MPUIO, and MICROWIRE I/O buffers. DV_{DD9} can be connected in common with the other DV_{DD} supplies if the same operating voltage is desired.	Power
DV_{DDRTC}	R10	V12	I/O supply voltage for the RTC I/O. (RTC_ON_NOFF, RTC_WAKE_INT, CLK32K_IN, CLK32K_OUT, OSC32K_OUT, OSC32K_IN, $\overline{\text{PWRON\_RESET}}$). DV_{DDRTC} can be connected in common with the other DV_{DD} supplies if the same operating voltage is desired and the RTC is not used in standalone.	Power
LDO.FILTER	H1	J1	A regulated supply is delivered by an embedded LDO to the DPLL macro(s).The regulated supply is available on the bond pad. A decoupling capacitor of 1 μF must be connected externally between LDO.FILTER and the ground.	Power
V_{SS}	F6 E13 E5 G7 F12 K10 K9 H9 H10 M12 J9 R9 M6 K8 L11 N5 H8 G11 N13 L7	A13 A21 B1 B5 B7 B16 F20 G1 K2 K20 N1 P12 R21 U2 W20 Y3 Y13 AA1 AA7 AA21	Common ground for all core and I/O-Voltage supplies.	Power

† I = Input, O = Output, Z = High-Impedance

‡ GPIO13 is used to select between full and fast boot. Set GPIO13 high to boot from the USB peripheral. Set GPIO13 low to boot from external flash on CS3.

3 Functional Overview

The following functional overview is based on the block diagram in Figure 3−1.

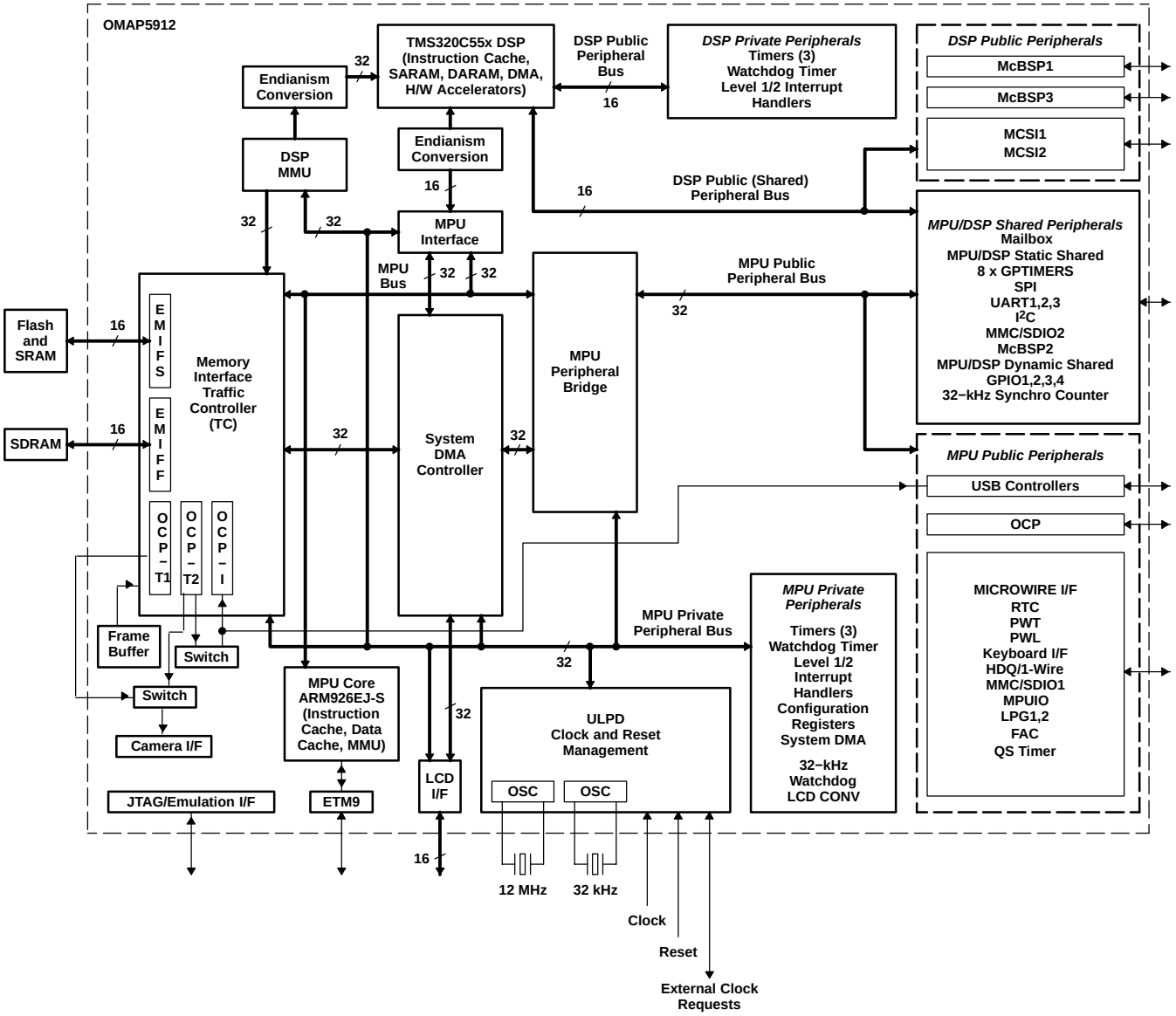


Figure 3−1. OMAP5912 Functional Block Diagram

3.1 Functional Block Diagram Features

The OMAP5912 devices include the following functional blocks:

- ARM926EJS megacell including:
  - ARM926EJS, supporting the operating system
  - MMU with translation lookaside buffer (TLBx)
  - L1 16K-byte, four-way, set-associative instruction cache
  - L1 8K-byte, four-way, set-associative data cache with write buffer
- MPU interrupt handler level 1
- Embedded trace macrocell module, ETM version 2.a in a 13-bit mode configuration or in a 17-bit demultiplexed mode configuration
- C55x DSP subsystem:
  - Embedded ICE emulator interface through JTAG port
  - TMS320C55x (C55x) DSP rev 2.1
  - L1 cache (24K bytes)
  - 16K-byte, two-way, set-associative instruction cache
  - 2 × 4K-byte RAM set for instruction
  - DARAM 64K-byte, zero-wait state, 32-bit organization
  - SARAM 96K-byte, zero-wait state, 32-bit organization
  - PDROM (32K bytes)
  - DMA controller: Six physical channels, five ports
  - DSP trace module
  - Hardware accelerators motion estimation (ME), discrete/inverse discrete cosine transform (DCT/IDCT), and pixel interpolation (PI)
  - DSP interrupt handler level 1 in the C55x DSP core
- DSP MMU
- DSP level 2 interrupt handler enabling connection to 16 additional interrupt lines outside OMAP. The priority of each interrupt line is controlled by software.
- DSP interrupt interface enabling connection to the interrupt lines coming out of the level 2 interrupt handler and the interrupt lines requiring higher priority. The outcome interrupt of this module is then connected to the DSP megacell to be processed by the DSP. This module mainly ensures that all interrupts going to the DSP megacell are level-sensitive.
- DSP peripherals:
  - 3 × 16-bit DSP private timers
  - 1 × 16-bit DSP private watchdog
- Mailboxes:

  Four mailboxes are implemented:
  - Two read/write accessible by MPU, read-only by the DSP
  - Two read/write accessible by the DSP, read-only by the MPU

  Each mailbox is implemented with 2 × 16-bit registers. When a write is done into a register by one processor, it generates an interrupt; this interrupt is released by the read access of the other processor.

- MPU peripherals
  - 3 × 32-bit private timers; their clock is either the OMAP3.2 reference input clock or the divided MPU clock.
  - 1 × 16-bit private watchdog; can be configured as a 16-bit general-purpose timer by software. Its clock is the OMAP3.2 reference input clock divided by 14.
- External LCD controller support, in addition to the OMAP LCD controller
  - LCD controller with its own tearing-effect logic
- Memory traffic controller
  - External memory interface slow (EMIFS); connects external device memories (such as common flash and SRAM memories). This interface enables 16-bit data accesses and provides four chip-selects; each chip-select is able to support up to 64M bytes address space through a 25-bit address bus.
  - External memory interface fast (EMIFF) is a memory interface that enables16-bit data SDRAM memory access. It supports connection to a maximum of 64M bytes of SDRAM. The address width is 16 bits and two bank selection bits are also provided. The OMAP5912 chip provides interfacing with a maximum of four banks of 64M × 16-bit SDRAM memory with DDR capability.
- Hardware security accelerators
  - DES/3DES
  - SHA1/MD5
  - Random number generator
  - Support provided by third-party software library
  - Bootloader
- Emulator interface through JTAG port
- Two DPLLs:
  - OMAP provides a single DPLL for the following clock domains:
  - MPU/traffic controller clock domain
  - DSP clock domain
- The OMAP gigacell enables the software to define either:
  - Two coupled domains in scalable mode. This means that only one DPLL is active and the other clocks are a multiple of it.
  - Mixed mode: In this case only one domain is working in asynchronous mode. The other domains are in scalable mode.
  - Endianism conversion for DSP
  - The DSP uses big-endian format, whereas the MPU uses little-endian format. Also, as a rule, the OMAP5912 chip works in little endian format. Thus, the endianism conversion is useful for all memory or peripheral accesses from on-chip peripherals or all shared memories to the C55x DSP.
- The OMAP3.2 is considered to be a subchip of OMAP5912. To connect the OMAP peripherals, six buses are delivered:
  - MPU shared TIPB
  - MPU private TIPB
  - DSP shared TIPB
  - DSP private TIPB
  - OCP T1/T2 (master)
  - OCP-I (slave)

- MPU private peripherals (accessible only by the MPU)
  - Three 32-bit general-purpose timers
  - Watchdog timer
  - Level 1/level 2 interrupt handlers
  - Configuration registers for pin multiplexing and other device-level configurations
  - DES/3DES
  - SHA1/MD5
  - LCD controller supporting monochrome panels or STN and TFT color panels
  - LCDCONV to provide 18 bits (instead of 16 bits) to the LCD interface
- DSP private peripherals (accessible only by the DSP)
  - Three 32-bit general-purpose timers
  - Watchdog timer
  - Level 1/level 2 interrupt handlers
- MPU public peripherals (accessible by the MPU and the system DMA)
  - USB interface
  - Camera interface providing connectivity to CMOS image sensors
  - MICROWIRE serial interface
  - Real-time clock module (RTC)
  - Pulse-width tone (PWT)
  - Pulse-width light (PWL)
  - Keyboard interface (6×5 or 8×8 matrix)
  - HDQ/1-Wire interface for serial communication to battery management devices
  - Multimedia card/secure digital (MMC/SDIO1)
  - Up to 16 MPU general-purpose I/Os (MPUIOs)
  - LED pulse generators (LPG)
  - Frame adjustment counter (FAC)
  - 32-kHz OS timer
- DSP public peripherals (accessible by the DSP, DSP DMA, and the MPU via the MPU interface)
  - Two multichannel buffered serial port (McBSP1 and 3)
  - Two multichannel serial interfaces (MCSI1 and 2)
- MPU/DSP shared peripherals (controlling processor is selected by the MPU)
  - Four mailboxes for interprocessor communications
  - Eight general-purpose timers
  - Serial port interface (SPI)
  - Three UARTs (UART1 and UART3 have SIR mode for IrDA operation)
  - Inter-integrated circuit (I^2C) multimode master and slave interface
  - Multimedia card/secure digital (MMC/SDIO2)
  - Multichannel buffered serial port (McBSP2)
  - Up to 64 general-purpose I/O pins with interrupt capability to either processor
  - 32-kHz synchro counter
- MPU/DSP shared peripherals (accessible via OCP-T2 port)
- MPU/DSP shared peripherals (accessible via OCP-T2 or OCP-T1 port)
  - TI Camera I/F (//)

3.2 MPU Memory Maps

3.2.1 MPU Global Memory Map

The MPU has a unified address space; therefore, the internal and external memories for program and data, as well as peripheral registers and configuration registers, are all accessed within the same address space. The MPU space is always addressed using byte addressing. Table 3−1 provides a high level illustration of the entire MPU addressable space. Table 3−2 shows the chip-select mapping. More details about the peripheral and configuration registers are provided in Section 3.2.2, MPU Subsystem Registers Memory Map.

Table 3−1. OMAP5912 MPU Global Memory Map

BGA BALL # DEVICE NAME	SIGNAL START ADDRESS (HEX)	BGA BALL # END ADDRESS (HEX)	SIGNAL SIZE	SIGNAL DATA ACCESS TYPE	SIGNAL COMMENT
EMIFS					
CS0	0000 0000	03FF FFFF	64M bytes		
Boot ROM	0000 0000	0000 FFFF	64K bytes	32-bit Ex/R	
Reserved boot ROM	0001 0000	0003 FFFF	192K bytes	32-bit Ex/R	
Reserved	0004 0000	001F FFFF			
Reserved	0020 0000	0020 3FFF			
Reserved	0020 4000	0020 FFFF			
Reserved	0021 0000	0021 000F			
Reserved	0021 0010	0021 002F			
Reserved	0021 0030	01FF FFFF			
NOR flash	0200 0000	03FF FFFF	32M bytes	8/16/32-bit Ex/R/W	16-bit or 32-bit organized
CS1	0400 0000	07FF FFFF	64M bytes		
NOR flash	0400 0000	07FF FFFF	64M bytes	8/16/32-bit Ex/R/W	16-bit or 32-bit organized
CS2	0800 0000	0BFF FFFF	64M bytes		
NOR flash	0800 0000	0BFF FFFF	64M bytes	8/16/32-bit Ex/R/W	16-bit or 32-bit organized
CS3	0C00 0000	0FFF FFFF	64M bytes		
NOR flash	0C00 0000	0FFF FFFF	64M bytes	8/16/32-bit Ex/R/W	16-bit or 32-bit organized
EMIFF					
SDRAM external	1000 0000	13FF FFFF	64M bytes	16-bit Ex/R/W	
Reserved	1400 0000	1FFF FFFF			
L3 OCP T1					
Frame buffer	2000 0000	2003 E7FF	250K bytes	32-bit Ex/R/W	
Reserved	2003 E800	2007 CFFF			
Reserved	2007 D000	2007 D3FF			
Reserved	2007 D400	2007 D7FF			
TI Camera I/F (//)	2007 D800	2007 DFFF	2K bytes	32-bit Ex/R/W	
L3 OCP T2					
Reserved	3000 0000	3000 0FFF			
Reserved	3000 1000	3000 1FFF			
Reserved	3000 2000	3000 21FF			
Reserved	3000 2200	3007 D7FF			
TI Camera I/F (//)	3007 D800	3007 DFFF	2K bytes	32-bit Ex/R/W	
Reserved	3007 E000	30FF FFFF			

Table 3−1. OMAP5912 MPU Global Memory Map (Continued)

BGA BALL # DEVICE NAME	SIGNAL START ADDRESS (HEX)	BGA BALL # END ADDRESS (HEX)	SIGNAL SIZE	SIGNAL DATA ACCESS TYPE	SIGNAL COMMENT
Reserved	3100 0000	34FF FFFF			
Reserved	3500 0000	7FFF FFFF			
DSP MPUI Interface					
MPUI memory + MPUI peripheral	E000 0000	E101 FFFF			Reserved memory space
Reserved	E102 0000	EFFF FFFF			
TIPB Peripheral and Control Registers					
Reserved	F000 0000	FFFA FFFF			
OMAP5912 peripherals	FFFB 0000	FFFE FFFF			
Reserved	FFFF 0000	FFFF FFFF			

NOTE:

CS1 and CS2 can be split **by software** to provide up to four chip-selects. In this case, each chip-select can support 32M bytes of asynchronous memory.

Table 3−2. Chip-Select Mapping

CHIP SELECT	START ADDRESS	END ADDRESS	NOR FLASH SIZE
CS1a	0x0400 0000	0x05FF FFFF	32M bytes
CS1b	0x0600 0000	0x07FF FFFF	32M bytes
CS2a	0x0800 0000	0x09FF FFFF	32M bytes
CS2b	0x0A00 0000	0x0BFF FFFF	32M bytes

3.2.2 MPU Subsystem Registers Memory Map

The MPU accesses peripheral and configuration registers in the same way that internal and external memory are accessed. The following tables specify the MPU base addresses where each set of registers is accessed. All accesses to these registers must utilize the appropriate access width (8-, 16-, or 32-bit-wide accesses) as indicated in the tables. Accessing registers with the incorrect access width are illegal.

WARNING: Access to Reserved areas is illegal.

3.2.2.1 MPU Private Peripheral Registers

The MPU private peripheral registers include the following:

- MPU Level 2 Interrupt Handler Registers
- LCDCONV Registers
- LCD Controller Registers
- MPU Timer1 Registers
- MPU Timer2 Registers
- MPU Timer3 Registers
- MPU Watchdog Timer Registers
- MPU Level 1 Interrupt Handler Registers
- System DMA Controller Registers

Table 3−3. MPU Level 2 Interrupt Handler Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:0000	MPU_L2_ITR	Interrupt Register	32	R/W	0000 0000h
FFFE:0004	MPU_L2_MIR	Interrupt Mask Register	32	R/W	FFFFFFFFh
FFFE:0008	RESERVED	Reserved			
FFFE:000C	RESERVED	Reserved			
FFFE:0010	MPU_L2_SIR_IRQ	Interrupt Encoded Source (IRQ) Register	32	R	0000 0000h
FFFE:0014	MPU_L2_SIR_FIQ	Interupt Encoded Source (FIQ) Register	32	R	0000 0000h
FFFE:0018	MPU_L2_CONTROL	Interrupt Control Register	32	R/W	0000 0000h
FFFE:001C	MPU_L2_ILR0	Interrupt Priority Level For IRQ 0 Register	32	R/W	0000 0000h
FFFE:0020	MPU_L2_ILR1	Interrupt Priority Level For IRQ 1 Register	32	R/W	0000 0000h
FFFE:0024	MPU_L2_ILR2	Interrupt Priority Level For IRQ 2 Register	32	R/W	0000 0000h
FFFE:0028	MPU_L2_ILR3	Interrupt Priority Level For IRQ 3 Register	32	R/W	0000 0000h
FFFE:002C	MPU_L2_ILR4	Interrupt Priority Level For IRQ 4 Register	32	R/W	0000 0000h
FFFE:0030	MPU_L2_ILR5	Interrupt Priority Level For IRQ 5 Register	32	R/W	0000 0000h
FFFE:0034	MPU_L2_ILR6	Interrupt Priority Level For IRQ 6 Register	32	R/W	0000 0000h
FFFE:0038	MPU_L2_ILR7	Interrupt Priority Level For IRQ 7 Register	32	R/W	0000 0000h
FFFE:003C	MPU_L2_ILR8	Interrupt Priority Level For IRQ 8 Register	32	R/W	0000 0000h
FFFE:0040	MPU_L2_ILR9	Interrupt Priority Level For IRQ 9 Register	32	R/W	0000 0000h
FFFE:0044	MPU_L2_ILR10	Interrupt Priority Level For IRQ 10 Register	32	R/W	0000 0000h

Table 3−3. MPU Level 2 Interrupt Handler Registers (Continued)

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:0048	MPU_L2_ILR11	Interrupt Priority Level For IRQ 11 Register	32	R/W	0000 0000h
FFFE:004C	MPU_L2_ILR12	Interrupt Priority Level For IRQ 12 Register	32	R/W	0000 0000h
FFFE:0050	MPU_L2_ILR13	Interrupt Priority Level For IRQ 13 Register	32	R/W	0000 0000h
FFFE:0054	MPU_L2_ILR14	Interrupt Priority Level For IRQ 14 Register	32	R/W	0000 0000h
FFFE:0058	MPU_L2_ILR15	Interrupt Priority Level For IRQ 15 Register	32	R/W	0000 0000h
FFFE:005C	MPU_L2_ILR16	Interrupt Priority Level For IRQ 16 Register	32	R/W	0000 0000h
FFFE:0060	MPU_L2_ILR17	Interrupt Priority Level For IRQ 17 Register	32	R/W	0000 0000h
FFFE:0064	MPU_L2_ILR18	Interrupt Priority Level For IRQ 18 Register	32	R/W	0000 0000h
FFFE:0068	MPU_L2_ILR19	Interrupt Priority Level For IRQ 19 Register	32	R/W	0000 0000h
FFFE:006C	MPU_L2_ILR20	Interrupt Priority Level For IRQ 20 Register	32	R/W	0000 0000h
FFFE:0070	MPU_L2_ILR21	Interrupt Priority Level For IRQ 21 Register	32	R/W	0000 0000h
FFFE:0074	MPU_L2_ILR22	Interrupt Priority Level For IRQ 22 Register	32	R/W	0000 0000h
FFFE:0078	MPU_L2_ILR23	Interrupt Priority Level For IRQ 23 Register	32	R/W	0000 0000h
FFFE:007C	MPU_L2_ILR24	Interrupt Priority Level For IRQ 24 Register	32	R/W	0000 0000h
FFFE:0080	MPU_L2_ILR25	Interrupt Priority Level For IRQ 25 Register	32	R/W	0000 0000h
FFFE:0084	MPU_L2_ILR26	Interrupt Priority Level For IRQ 26 Register	32	R/W	0000 0000h
FFFE:0088	MPU_L2_ILR27	Interrupt Priority Level For IRQ 27 Register	32	R/W	0000 0000h
FFFE:008C	MPU_L2_ILR28	Interrupt Priority Level For IRQ 28 Register	32	R/W	0000 0000h
FFFE:0090	MPU_L2_ILR29	Interrupt Priority Level For IRQ 29 Register	32	R/W	0000 0000h
FFFE:0094	MPU_L2_ILR30	Interrupt Priority Level For IRQ 30 Register	32	R/W	0000 0000h
FFFE:0098	MPU_L2_ILR31	Interrupt Priority Level For IRQ 31 Register	32	R/W	0000 0000h
FFFE:009C	MPU_L2_ISR	Software Interrupt Set Register	32	W	0000 0000h
FFFE:00A0	MPU_L2_STATUS	Status Register	32	R	0000 0000h
FFFE:00A4	MPU_L2_OCP_CFG	OCP Configuration Register	32	R/W	0000 0000h
FFFE:00A8	MPU_L2_INTH_REV	Interrupt Controller Revision ID	32	R	0000 0000h

Table 3−4. LCDCONV Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:3000 − FFFE:301F	LCDCONV_R_LOOK_UP	R Look-up Table Register File	8	R/W	undefined
FFFE:3020 − FFFE:303F	LCDCONV_B_LOOK_UP	B Look-up Table Register File	8	R/W	undefined
FFFE:3040− FFFE:307F	LCDCONV_G_LOOK_UP	G Look-up Table Register File	8	R/W	undefined
FFFE:3080	LCDCONV_CONTROL	Control Register	8	R/W	0000h
FFFE:3084	LCDCONV_DEV_REV	Device Revision Register	8	R	undefined

Table 3−5. LCD Controller Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:C000	LCD_CONTROL	LCD Control Register	32	R/W	xx00 0000h
FFFE:C004	LCD_TIMING0	LCD Timing0 Register	32	R/W	0000 000Fh
FFFE:C008	LCD_TIMING1	LCD Timing1 Register	32	R/W	0000 0000h
FFFE:C00C	LCD_TIMING2	LCD TIming2 Register	32	R/W	xx00 0000h
FFFE:C010	LCD_STATUS	LCD Status Register	32	R/W	xxxx xxx0h
FFFE:C014	LCD_SUBPANEL	LCD Subpanel Display Register	32	R/W	xx00 0000h
FFFE:C018	LCD_LINEINT	LCD Line Interrupt Register	32	R/W	xxxx xx00h
FFFE:C01C	LCD_DISPLAYSTATUS	LCD Display Status Register	32	R/W	xxxx x3FFh

Table 3−6. MPU Timer1 Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:C500	MPU_CNTL_TIMER1	MPU Timer1 Control Register	32	R/W	0000 0000h
FFFE:C504	MPU_LOAD_TIMER1	MPU Timer1 Load Register	32	W	undefined
FFFE:C508	MPU_READ_TIMER1	MPU Timer1 Read Register	32	R	undefined

Table 3−7. MPU Timer2 Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:C600	MPU_CNTL_TIMER2	MPU Timer2 Control Register	32	R/W	0000 0000h
FFFE:C604	MPU_LOAD_TIMER2	MPU Timer2 Load Register	32	W	undefined
FFFE:C608	MPU_READ_TIMER2	MPU Timer2 Read Register	32	R	undefined

Table 3−8. MPU Timer3 Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:C700	MPU_CNTL_TIMER3	MPU Timer3 Control Register	32	R/W	0000 0000h
FFFE:C704	MPU_LOAD_TIME3	MPU Timer3 Load Register	32	W	undefined
FFFE:C708	MPU_READ_TIMER3	MPU Timer3 Read Register	32	R	undefined

Table 3−9. MPU Watchdog Timer Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:C800	MPU_WDT_CNTL_TIMER	MPU Watchdog Timer Control Register	32	R/W	0000 0E02h
FFFE:C804	MPU_WDT_LOAD_TIMER	MPU Watchdog Timer Load Register	32	W	xxxx FFFFh
FFFE:C804	MPU_WDT_READ_TIMER	MPU Watchdog Timer Read Register	32	R	xxxx FFFFh
FFFE:C808	MPU_WDT_TIMER_MODE	MPU Watchdog Timer Mode Register	32	R/W	0000 8000h

Table 3−10. MPU Level 1 Interrupt Handler Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:CB00	MPU_L1_ITR	Interrupt Register	32	R/W	0000 0000h
FFFE:CB04	MPU_L1_MIR	Interrupt Mask Register	32	R/W	FFFF FFFFh
FFFE:CB08	RESERVED	Reserved			
FFFE:CB0C	RESERVED	Reserved			
FFFE:CB10	MPU_L1_SIR_IRQ_CODE	Interrupt Encoded Source (IRQ) Register	32	R	0000 0000h
FFFE:CB14	MPU_L1_SIR_FIQ_CODE	Interupt Encoded Source (FIQ) Register	32	R	0000 0000h
FFFE:CB18	MPU_L1_CONTROL	Interrupt Control Register	32	R/W	0000 0000h
FFFE:CB1C	MPU_L1_ILR0	Interrupt Priority Level For IRQ 0 Register	32	R/W	0000 0000h
FFFE:CB20	MPU_L1_ILR1	Interrupt Priority Level For IRQ 1 Register	32	R/W	0000 0000h
FFFE:CB24	MPU_L1_ILR2	Interrupt Priority Level For IRQ 2 Register	32	R/W	0000 0000h
FFFE:CB28	MPU_L1_ILR3	Interrupt Priority Level For IRQ 3 Register	32	R/W	0000 0000h
FFFE:CB2C	MPU_L1_ILR4	Interrupt Priority Level For IRQ 4 Register	32	R/W	0000 0000h
FFFE:CB30	MPU_L1_ILR5	Interrupt Priority Level For IRQ 5 Register	32	R/W	0000 0000h
FFFE:CB34	MPU_L1_ILR6	Interrupt Priority Level For IRQ 6 Register	32	R/W	0000 0000h
FFFE:CB38	MPU_L1_ILR7	Interrupt Priority Level For IRQ 7 Register	32	R/W	0000 0000h
FFFE:CB3C	MPU_L1_ILR8	Interrupt Priority Level For IRQ 8 Register	32	R/W	0000 0000h
FFFE:CB40	MPU_L1_ILR9	Interrupt Priority Level For IRQ 9 Register	32	R/W	0000 0000h
FFFE:CB44	MPU_L1_ILR10	Interrupt Priority Level For IRQ 10 Register	32	R/W	0000 0000h
FFFE:CB48	MPU_L1_ILR11	Interrupt Priority Level For IRQ 11 Register	32	R/W	0000 0000h
FFFE:CB4C	MPU_L1_ILR12	Interrupt Priority Level For IRQ 12 Register	32	R/W	0000 0000h
FFFE:CB50	MPU_L1_ILR13	Interrupt Priority Level For IRQ 13 Register	32	R/W	0000 0000h
FFFE:CB54	MPU_L1_ILR14	Interrupt Priority Level For IRQ 14 Register	32	R/W	0000 0000h
FFFE:CB58	MPU_L1_ILR15	Interrupt Priority Level For IRQ 15 Register	32	R/W	0000 0000h
FFFE:CB5C	MPU_L1_ILR16	Interrupt Priority Level For IRQ 16 Register	32	R/W	0000 0000h
FFFE:CB60	MPU_L1_ILR17	Interrupt Priority Level For IRQ 17 Register	32	R/W	0000 0000h
FFFE:CB64	MPU_L1_ILR18	Interrupt Priority Level For IRQ 18 Register	32	R/W	0000 0000h
FFFE:CB68	MPU_L1_ILR19	Interrupt Priority Level For IRQ 19 Register	32	R/W	0000 0000h
FFFE:CB6C	MPU_L1_ILR20	Interrupt Priority Level For IRQ 20 Register	32	R/W	0000 0000h
FFFE:CB70	MPU_L1_ILR21	Interrupt Priority Level For IRQ 21 Register	32	R/W	0000 0000h
FFFE:CB74	MPU_L1_ILR22	Interrupt Priority Level For IRQ 22 Register	32	R/W	0000 0000h
FFFE:CB78	MPU_L1_ILR23	Interrupt Priority Level For IRQ 23 Register	32	R/W	0000 0000h
FFFE:CB7C	MPU_L1_ILR24	Interrupt Priority Level For IRQ 24 Register	32	R/W	0000 0000h
FFFE:CB80	MPU_L1_ILR25	Interrupt Priority Level For IRQ 25 Register	32	R/W	0000 0000h
FFFE:CB84	MPU_L1_ILR26	Interrupt Priority Level For IRQ 26 Register	32	R/W	0000 0000h
FFFE:CB88	MPU_L1_ILR27	Interrupt Priority Level For IRQ 27 Register	32	R/W	0000 0000h
FFFE:CB8C	MPU_L1_ILR28	Interrupt Priority Level For IRQ 28 Register	32	R/W	0000 0000h
FFFE:CB90	MPU_L1_ILR29	Interrupt Priority Level For IRQ 29 Register	32	R/W	0000 0000h
FFFE:CB94	MPU_L1_ILR30	Interrupt Priority Level For IRQ 30 Register	32	R/W	0000 0000h
FFFE:CB98	MPU_L1_ILR31	Interrupt Priority Level For IRQ 31 Register	32	R/W	0000 0000h
FFFE:C9C	MPU_L1_ISR	Interrupt Priority Level For IRQ 0 Register	32	R/W	0000 0000h
FFFE:CBA0	MPU_L1_ENHANCED_CNTL	Enhanced Control Register	32	R/W	0000 0000h

Table 3−11. System DMA Controller Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:D800	SYS_DMA_CSDP_CH0	Logical Channel 0 Source/Destination Parameters Register	16	RW	0000h
FFFE:D802	SYS_DMA_CCR_CH0	Logical Channel 0 Control Register	16	RW	0000h
FFFE:D804	SYS_DMA_CICR_CH0	Logical Channel 0 Interrupt Control Register	16	RW	0003h
FFFE:D806	SYS_DMA_CSR_CH0	Logical Channel 0 Status Register	16	R	0000h
FFFE:D808	SYS_DMA_CSSA_L_CH0	Logical Channel 0 Source Start Address Register LSB	16	RW	undef
FFFE:D80A	SYS_DMA_CSSA_U_CH0	Logical Channel 0 Source Start Address Register MSB	16	RW	undef
FFFE:D80C	SYS_DMA_CDSA_L_CH0	Logical Channel 0 Destination Start Address Register LSB	16	RW	undef
FFFE:D80E	SYS_DMA_CDSA_U_CH0	Logical Channel 0 Destination Start Address Register MSB	16	RW	undef
FFFE:D810	SYS_DMA_CEN_CH0	Logical Channel 0 Element Number Register	16	RW	undef
FFFE:D812	SYS_DMA_CFN_CH0	Logical Channel 0 Frame Number Register	16	RW	undef
FFFE:D814	SYS_DMA_CSFI_CH0	Logical Channel 0 Source Frame Index Register	16	RW	undef
FFFE:D816	SYS_DMA_CSEI_CH0	Logical Channel 0 Source Element Index Register	16	RW	undef
FFFE:D818	SYS_DMA_CSAC_CH0	Logical Channel 0 Source Address Counter Register	16	R	undef
FFFE:D81A	SYS_DMA_CDAC_CH0	Logical Channel 0 Destination Address Counter Register	16	R	undef
FFFE:D81C	SYS_DMA_CDEI_CH0	Logical Channel 0 Destination Element Index Register	16	RW	undef
FFFE:D81E	SYS_DMA_CDFI_CH0	Logical Channel 0 Destination Frame Index Register	16	RW	undef
FFFE:D820	SYS_DMA_COLOR_L_CH0	Logical Channel 0 Color Parameter Register, Lower Bits	16	RW	undef
FFFE:D822	SYS_DMA_COLOR_U_CH0	Logical Channel 0 Color Parameter Register, Upper Bits	16	RW	undef
FFFE:D824	SYS_DMA_CCR2	Channel Control Register 2	16	RW	undef
FFFE:D828	SYS_DMA_CLNK_CTRL	Channel Link Control Register	16	RW	undef
FFFE:D82A	SYS_DMA_LCH_CTRL	Logical Channel Control Register	16	RW	undef
FFFE:D82C − FFFE:D83F		Reserved			
FFFE:D840	SYS_DMA_CSDP_CH1	Logical Channel 1 Source/Destination Parameters Register	16	RW	0000h
FFFE:D842	SYS_DMA_CCR_CH1	Logical Channel 1 Control Register	16	RW	0000h
FFFE:D844	SYS_DMA_CICR_CH1	Logical Channel 1 Interrupt Control Register	16	RW	0003h
FFFE:D846	SYS_DMA_CSR_CH1	Logical Channel 1 Status Register	16	R	0000h
FFFE:D848	SYS_DMA_CSSA_L_CH1	Logical Channel 1 Source Start Address Register LSB	16	RW	undef
FFFE:D84A	SYS_DMA_CSSA_U_CH1	Logical Channel 1 Source Start Address Register MSB	16	RW	undef
FFFE:D84C	SYS_DMA_CDSA_L_CH1	Logical Channel 1 Destination Start Address Register LSB	16	RW	undef
FFFE:D84E	SYS_DMA_CDSA_U_CH1	Logical Channel 1 Destination Start Address Register MSB	16	RW	undef

Table 3−11. System DMA Controller Registers (Continued)

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:D850	SYS_DMA_CEN_CH1	Logical Channel 1 Element Number Register	16	RW	undef
FFFE:D852	SYS_DMA_CFN_CH1	Logical Channel 1 Frame Number Register	16	RW	undef
FFFE:D854	SYS_DMA_CSFI_CH1	Logical Channel 1 Source Frame Index Register	16	RW	undef
FFFE:D856	SYS_DMA_CSEI_CH1	Logical Channel 1 Source Element Index Register	16	RW	undef
FFFE:D858	SYS_DMA_CSAC_CH1	Logical Channel 1 Source Address Counter Register	16	R	undef
FFFE:D85A	SYS_DMA_CDAC_CH1	Logical Channel 1 Destination Address Counter Register	16	R	undef
FFFE:D85C	SYS_DMA_CDEI_CH1	Logical Channel 1 Destination Element Index Register	16	RW	undef
FFFE:D85E	SYS_DMA_CDFI_CH1	Logical Channel 1 Destination Frame Index Register	16	RW	undef
FFFE:D860	SYS_DMA_COLOR_L_CH0	Logical Channel 1 Color Parameter Register, Lower Bits	16	RW	undef
FFFE:D862	SYS_DMA_COLOR_U_CH0	Logical Channel 1 Color Parameter Register, Upper Bits	16	RW	undef
FFFE:D864	SYS_DMA_CCR2	Channel Control Register 2	16	RW	undef
FFFE:D868	SYS_DMA_CLNK_CTRL	Channel Link Control Register	16	RW	undef
FFFE:D86A	SYS_DMA_LCH_CTRL	Logical Channel Control Register	16	RW	undef
FFFE:D86C − FFFE:D87F		Reserved			
FFFE:D880	SYS_DMA_CSDP_CH2	Logical Channel 2 Source/Destination Parameters Register	16	RW	0000h
FFFE:D882	SYS_DMA_CCR_CH2	Logical Channel 2 Control Register	16	RW	0000h
FFFE:D884	SYS_DMA_CICR_CH2	Logical Channel 2 Interrupt Control Register	16	RW	0003h
FFFE:D886	SYS_DMA_CSR_CH2	Logical Channel 2 Status Register	16	R	0000h
FFFE:D888	SYS_DMA_CSSA_L_CH2	Logical Channel 2 Source Start Address Register LSB	16	RW	undef
FFFE:D88A	SYS_DMA_CSSA_U_CH2	Logical Channel 2 Source Start Address Register MSB	16	RW	undef
FFFE:D88C	SYS_DMA_CDSA_L_CH2	Logical Channel 2 Destination Start Address Register LSB	16	RW	undef
FFFE:D88E	SYS_DMA_CDSA_U_CH2	Logical Channel 2 Destination Start Address Register MSB	16	RW	undef
FFFE:D890	SYS_DMA_CEN_CH2	Logical Channel 2 Element Number Register	16	RW	undef
FFFE:D892	SYS_DMA_CFN_CH2	Logical Channel 2 Frame Number Register	16	RW	undef
FFFE:D894	SYS_DMA_CSFI_CH2	Logical Channel 2 Source Frame Index Register	16	RW	undef
FFFE:D896	SYS_DMA_CSEI_CH2	Logical Channel 2 Source Element Index Register	16	RW	undef
FFFE:D898	SYS_DMA_CSAC_CH2	Logical Channel 2 Source Address Counter Register	16	R	undef
FFFE:D89A	SYS_DMA_CDAC_CH2	Logical Channel 2 Destination Address Counter Register	16	R	undef
FFFE:D89C	SYS_DMA_CDEI_CH2	Logical Channel 2 Destination Element Index Register	16	RW	undef

Table 3−11. System DMA Controller Registers (Continued)

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:D89E	SYS_DMA_CDFI_CH2	Logical Channel 2 Destination Frame Index Register	16	RW	undef
FFFE:D8A0	SYS_DMA_COLOR_L_CH0	Logical Channel 2 Color Parameter Register, Lower Bits	16	RW	undef
FFFE:D8A2	SYS_DMA_COLOR_U_CH0	Logical Channel 2 Color Parameter Register, Upper Bits	16	RW	undef
FFFE:D8A4	SYS_DMA_CCR2	Channel Control Register 2	16	RW	undef
FFFE:D8A8	SYS_DMA_CLNK_CTRL	Channel Link Control Register	16	RW	undef
FFFE:D8AA	SYS_DMA_LCH_CTRL	Logical Channel Control Register	16	RW	undef
FFFE:D8AC − FFFE:D8BF		Reserved			
FFFE:D8C0	SYS_DMA_CSDP_CH3	Logical Channel 3 Source/Destination Parameters Register	16	RW	0000h
FFFE:D8C2	SYS_DMA_CCR_CH3	Logical Channel 3 Control Register	16	RW	0000h
FFFE:D8C4	SYS_DMA_CICR_CH3	Logical Channel 3 Interrupt Control Register	16	RW	0003h
FFFE:D8C6	SYS_DMA_CSR_CH3	Logical Channel 3 Status Register	16	R	0000h
FFFE:D8C8	SYS_DMA_CSSA_L_CH3	Logical Channel 3 Source Start Address Register LSB	16	RW	undef
FFFE:D8CA	SYS_DMA_CSSA_U_CH3	Logical Channel 3 Source Start Address Register MSB	16	RW	undef
FFFE:D8CC	SYS_DMA_CDSA_L_CH3	Logical Channel 3 Destination Start Address Register LSB	16	RW	undef
FFFE:D8CE	SYS_DMA_CDSA_U_CH3	Logical Channel 3 Destination Start Address Register MSB	16	RW	undef
FFFE:D8D0	SYS_DMA_CEN_CH3	Logical Channel 3 Element Number Register	16	RW	undef
FFFE:D8D2	SYS_DMA_CFN_CH3	Logical Channel 3 Frame Number Register	16	RW	undef
FFFE:D8D4	SYS_DMA_CSFI_CH3	Logical Channel 3 Source Frame Index Register	16	RW	undef
FFFE:D8D6	SYS_DMA_CSEI_CH3	Logical Channel 3 Source Element Index Register	16	RW	undef
FFFE:D8D8	SYS_DMA_CSAC_CH3	Logical Channel 3 Source Address Counter Register	16	R	undef
FFFE:D8DA	SYS_DMA_CDAC_CH3	Logical Channel 3 Destination Address Counter Register	16	R	undef
FFFE:D8DC	SYS_DMA_CDEI_CH3	Logical Channel 3 Destination Element Index Register	16	RW	undef
FFFE:D8DE	SYS_DMA_CDFI_CH3	Logical Channel 3 Destination Frame Index Register	16	RW	undef
FFFE:D8E0	SYS_DMA_COLOR_L_CH3	Logical Channel 3 Color Parameter Register, Lower Bits	16	RW	undef
FFFE:D8E2	SYS_DMA_COLOR_U_CH3	Logical Channel 3 Color Parameter Register, Upper Bits	16	RW	undef
FFFE:D8E4	SYS_DMA_CCR2	Channel Control Register 2	16	RW	undef
FFFE:D8E8	SYS_DMA_CLNK_CTRL	Channel Link Control Register	16	RW	undef
FFFE:D8EA	SYS_DMA_LCH_CTRL	Logical Channel Control Register	16	RW	undef
FFFE:D8EC − FFFE:D8FF		Reserved			
FFFE:D900	SYS_DMA_CSDP_CH4	Logical Channel 4 Source/Destination Parameters Register	16	RW	0000h

Table 3−11. System DMA Controller Registers (Continued)

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:D902	SYS_DMA_CCR_CH4	Logical Channel 4 Control Register	16	RW	0000h
FFFE:D904	SYS_DMA_CICR_CH4	Logical Channel 4 Interrupt Control Register	16	RW	0003h
FFFE:D906	SYS_DMA_CSR_CH4	Logical Channel 4 Status Register	16	R	0000h
FFFE:D908	SYS_DMA_CSSA_L_CH4	Logical Channel 4 Source Start Address Register LSB	16	RW	undef
FFFE:D90A	SYS_DMA_CSSA_U_CH4	Logical Channel 4 Source Start Address Register MSB	16	RW	undef
FFFE:D90C	SYS_DMA_CDSA_L_CH4	Logical Channel 4 Destination Start Address Register LSB	16	RW	undef
FFFE:D90E	SYS_DMA_CDSA_U_CH4	Logical Channel 4 Destination Start Address Register MSB	16	RW	undef
FFFE:D910	SYS_DMA_CEN_CH4	Logical Channel 4 Element Number Register	16	RW	undef
FFFE:D912	SYS_DMA_CFN_CH4	Logical Channel 4 Frame Number Register	16	RW	undef
FFFE:D914	SYS_DMA_CSFI_CH4	Logical Channel 4 Source Frame Index Register	16	RW	undef
FFFE:D916	SYS_DMA_CSEI_CH4	Logical Channel 4 Source Element Index Register	16	RW	undef
FFFE:D918	SYS_DMA_CSAC_CH4	Logical Channel 4 Source Address Counter Register	16	R	undef
FFFE:D91A	SYS_DMA_CDAC_CH4	Logical Channel 4 Destination Address Counter Register	16	R	undef
FFFE:D91C	SYS_DMA_CDEI_CH4	Logical Channel 4 Destination Element Index Register	16	RW	undef
FFFE:D91E	SYS_DMA_CDFI_CH4	Logical Channel 4 Destination Frame Index Register	16	RW	undef
FFFE:D920	SYS_DMA_COLOR_L_CH4	Logical Channel 4 Color Parameter Register, Lower Bits	16	RW	undef
FFFE:D822	SYS_DMA_COLOR_U_CH4	Logical Channel 4 Color Parameter Register, Upper Bits	16	RW	undef
FFFE:D824	SYS_DMA_CCR2	Channel Control Register 2	16	RW	undef
FFFE:D828	SYS_DMA_CLNK_CTRL	Channel Link Control Register	16	RW	undef
FFFE:D82A	SYS_DMA_LCH_CTRL	Logical Channel Control Register	16	RW	undef
FFFE:D92C − FFFE:D93F		Reserved			
FFFE:D940	SYS_DMA_CSDP_CH5	Logical Channel 5 Source/Destination Parameters Register	16	RW	0000h
FFFE:D942	SYS_DMA_CCR_CH5	Logical Channel 5 Control Register	16	RW	0000h
FFFE:D944	SYS_DMA_CICR_CH5	Logical Channel 5 Interrupt Control Register	16	RW	0003h
FFFE:D946	SYS_DMA_CSR_CH5	Logical Channel 5 Status Register	16	R	0000h
FFFE:D948	SYS_DMA_CSSA_L_CH5	Logical Channel 5 Source Start Address Register LSB	16	RW	undef
FFFE:D94A	SYS_DMA_CSSA_U_CH5	Logical Channel 5 Source Start Address Register MSB	16	RW	undef
FFFE:D94C	SYS_DMA_CDSA_L_CH5	Logical Channel 5 Destination Start Address Register LSB	16	RW	undef
FFFE:D94E	SYS_DMA_CDSA_U_CH5	Logical Channel 5 Destination Start Address Register MSB	16	RW	undef
FFFE:D950	SYS_DMA_CEN_CH5	Logical Channel 5 Element Number Register	16	RW	undef

Table 3−11. System DMA Controller Registers (Continued)

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:D952	SYS_DMA_CFN_CH5	Logical Channel 5 Frame Number Register	16	RW	undef
FFFE:D954	SYS_DMA_CSFI_CH5	Logical Channel 5 Source Frame Index Register	16	RW	undef
FFFE:D956	SYS_DMA_CSEI_CH5	Logical Channel 5 Source Element Index Register	16	RW	undef
FFFE:D958	SYS_DMA_CSAC_CH5	Logical Channel 5 Source Address Counter Register	16	R	undef
FFFE:D95A	SYS_DMA_CDAC_CH5	Logical Channel 5 Destination Address Counter Register	16	R	undef
FFFE:D95C	SYS_DMA_CDEI_CH5	Logical Channel 5 Destination Element Index Register	16	RW	undef
FFFE:D95E	SYS_DMA_CDFI_CH5	Logical Channel 5 Destination Frame Index Register	16	RW	undef
FFFE:D960	SYS_DMA_COLOR_L_CH0	Logical Channel 5 Color Parameter Register, Lower Bits	16	RW	undef
FFFE:D962	SYS_DMA_COLOR_U_CH0	Logical Channel 5 Color Parameter Register, Upper Bits	16	RW	undef
FFFE:D964	SYS_DMA_CCR2	Channel Control Register 2	16	RW	undef
FFFE:D968	SYS_DMA_CLNK_CTRL	Channel Link Control Register	16	RW	undef
FFFE:D96A	SYS_DMA_LCH_CTRL	Logical Channel Control Register	16	RW	undef
FFFE:D96C − FFFE:D97F		Reserved			
FFFE:D980	SYS_DMA_CSDP_CH6	Logical Channel 6 Source/Destination Parameters Register	16	RW	0000h
FFFE:D982	SYS_DMA_CCR_CH6	Logical Channel 6 Control Register	16	RW	0000h
FFFE:D984	SYS_DMA_CICR_CH6	Logical Channel 6 Interrupt Control Register	16	RW	0003h
FFFE:D986	SYS_DMA_CSR_CH6	Logical Channel 6 Status Register	16	R	0000h
FFFE:D988	SYS_DMA_CSSA_L_CH6	Logical Channel 6 Source Start Address Register LSB	16	RW	undef
FFFE:D98A	SYS_DMA_CSSA_U_CH6	Logical Channel 6 Source Start Address Register MSB	16	RW	undef
FFFE:D98C	SYS_DMA_CDSA_L_CH6	Logical Channel 6 Destination Start Address Register LSB	16	RW	undef
FFFE:D98E	SYS_DMA_CDSA_U_CH6	Logical Channel 6 Destination Start Address Register MSB	16	RW	undef
FFFE:D990	SYS_DMA_CEN_CH6	Logical Channel 6 Element Number Register	16	RW	undef
FFFE:D992	SYS_DMA_CFN_CH6	Logical Channel 6 Frame Number Register	16	RW	undef
FFFE:D994	SYS_DMA_CSFI_CH6	Logical Channel 6 Source Frame Index Register	16	RW	undef
FFFE:D996	SYS_DMA_CSEI_CH6	Logical Channel 6 Source Element Index Register	16	RW	undef
FFFE:D998	SYS_DMA_CSAC_CH6	Logical Channel 6 Source Address Counter Register	16	R	undef
FFFE:D99A	SYS_DMA_CDAC_CH6	Logical Channel 6 Destination Address Counter Register	16	R	undef
FFFE:D99C	SYS_DMA_CDEI_CH6	Logical Channel 6 Destination Element Index Register	16	RW	undef
FFFE:D99E	SYS_DMA_CDFI_CH6	Logical Channel 6 Destination Frame Index Register	16	RW	undef

Table 3−11. System DMA Controller Registers (Continued)

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:D9A0	SYS_DMA_COLOR_L_CH6	Logical Channel 6 Color Parameter Register, Lower Bits	16	RW	undef
FFFE:D9A2	SYS_DMA_COLOR_U_CH6	Logical Channel 6 Color Parameter Register, Upper Bits	16	RW	undef
FFFE:D9A4	SYS_DMA_CCR2	Channel Control Register 2	16	RW	undef
FFFE:D9A8	SYS_DMA_CLNK_CTRL	Channel Link Control Register	16	RW	undef
FFFE:D9AA	SYS_DMA_LCH_CTRL	Logical Channel Control Register	16	RW	undef
FFFE:D9AC − FFFE:D9BF		Reserved			
FFFE:D9C0	SYS_DMA_CSDP_CH7	Logical Channel 7 Source/Destination Parameters Register	16	RW	0000h
FFFE:D9C2	SYS_DMA_CCR_CH7	Logical Channel 7 Control Register	16	RW	0000h
FFFE:D9C4	SYS_DMA_CICR_CH7	Logical Channel 7 Interrupt Control Register	16	RW	0003h
FFFE:D9C6	SYS_DMA_CSR_CH7	Logical Channel 7 Status Register	16	R	0000h
FFFE:D9C8	SYS_DMA_CSSA_L_CH7	Logical Channel 7 Source Start Address Register LSB	16	RW	undef
FFFE:D9CA	SYS_DMA_CSSA_U_CH7	Logical Channel 7 Source Start Address Register MSB	16	RW	undef
FFFE:D9CC	SYS_DMA_CDSA_L_CH7	Logical Channel 7 Destination Start Address Register LSB	16	RW	undef
FFFE:D9CE	SYS_DMA_CDSA_U_CH7	Logical Channel 7 Destination Start Address Register MSB	16	RW	undef
FFFE:D9D0	SYS_DMA_CEN_CH7	Logical Channel 7 Element Number Register	16	RW	undef
FFFE:D9D2	SYS_DMA_CFN_CH7	Logical Channel 7 Frame Number Register	16	RW	undef
FFFE:D9D4	SYS_DMA_CSFI_CH7	Logical Channel 7 Source Frame Index Register	16	RW	undef
FFFE:D9D6	SYS_DMA_CSEI_CH7	Logical Channel 7 Source Element Index Register	16	RW	undef
FFFE:D9D8	SYS_DMA_CSAC_CH7	Logical Channel 7 Source Address Counter Register	16	R	undef
FFFE:D9DA	SYS_DMA_CDAC_CH7	Logical Channel 7 Destination Address Counter Register	16	R	undef
FFFE:D9DC	SYS_DMA_CDEI_CH7	Logical Channel 7 Destination Element Index Register	16	RW	undef
FFFE:D9DE	SYS_DMA_CDFI_CH7	Logical Channel 7 Destination Frame Index Register	16	RW	undef
FFFE:D9E0	SYS_DMA_COLOR_L_CH7	Logical Channel 7 Color Parameter Register, Lower Bits	16	RW	undef
FFFE:D9E2	SYS_DMA_COLOR_U_CH7	Logical Channel 7 Color Parameter Register, Upper Bits	16	RW	undef
FFFE:D9E4	SYS_DMA_CCR2	Channel Control Register 2	16	RW	undef
FFFE:D9E8	SYS_DMA_CLNK_CTRL	Channel Link Control Register	16	RW	undef
FFFE:D9EA	SYS_DMA_LCH_CTRL	Logical Channel Control Register	16	RW	undef
FFFE:D9EC − FFFE:D9FF		Reserved			
FFFE:DA00	SYS_DMA_CSDP_CH8	Logical Channel 8 Source/Destination Parameters Register	16	RW	0000h
FFFE:DA02	SYS_DMA_CCR_CH8	Logical Channel 8 Control Register	16	RW	0000h

Table 3−11. System DMA Controller Registers (Continued)

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:DA04	SYS_DMA_CICR_CH8	Logical Channel 8 Interrupt Control Register	16	RW	0003h
FFFE:DA06	SYS_DMA_CSR_CH8	Logical Channel 8 Status Register	16	R	0000h
FFFE:DA08	SYS_DMA_CSSA_L_CH8	Logical Channel 8 Source Start Address Register LSB	16	RW	undef
FFFE:DA0A	SYS_DMA_CSSA_U_CH8	Logical Channel 8 Source Start Address Register MSB	16	RW	undef
FFFE:DA0C	SYS_DMA_CDSA_L_CH8	Logical Channel 8 Destination Start Address Register LSB	16	RW	undef
FFFE:DA0E	SYS_DMA_CDSA_U_CH8	Logical Channel 8 Destination Start Address Register MSB	16	RW	undef
FFFE:DA10	SYS_DMA_CEN_CH8	Logical Channel 8 Element Number Register	16	RW	undef
FFFE:DA12	SYS_DMA_CFN_CH8	Logical Channel 8 Frame Number Register	16	RW	undef
FFFE:DA14	SYS_DMA_CSFI_CH8	Logical Channel 8 Source Frame Index Register	16	RW	undef
FFFE:DA16	SYS_DMA_CSEI_CH8	Logical Channel 8 Source Element Index Register	16	RW	undef
FFFE:DA18	SYS_DMA_CSAC_CH8	Logical Channel 8 Source Address Counter Register	16	R	undef
FFFE:DA1A	SYS_DMA_CDAC_CH8	Logical Channel 8 Destination Address Counter Register	16	R	undef
FFFE:DA1C	SYS_DMA_CDEI_CH8	Logical Channel 8 Destination Element Index Register	16	RW	undef
FFFE:DA1E	SYS_DMA_CDFI_CH8	Logical Channel 8 Destination Frame Index Register	16	RW	undef
FFFE:DA20	SYS_DMA_COLOR_L_CH8	Logical Channel 8 Color Parameter Register, Lower Bits	16	RW	undef
FFFE:DA22	SYS_DMA_COLOR_U_CH8	Logical Channel 8 Color Parameter Register, Upper Bits	16	RW	undef
FFFE:DA24	SYS_DMA_CCR2	Channel Control Register 2	16	RW	undef
FFFE:DA28	SYS_DMA_CLNK_CTRL	Channel Link Control Register	16	RW	undef
FFFE:DA2A	SYS_DMA_LCH_CTRL	Logical Channel Control Register	16	RW	undef
FFFE:DB2C − FFFE:DA3F		Reserved			
FFFE:DA40	SYS_DMA_CSDP_CH9	Logical Channel 9 Source/Destination Parameters Register	16	RW	0000h
FFFE:DA42	SYS_DMA_CCR_CH9	Logical Channel 9 Control Register	16	RW	0000h
FFFE:DA44	SYS_DMA_CICR_CH9	Logical Channel 9 Interrupt Control Register	16	RW	0003h
FFFE:DA46	SYS_DMA_CSR_CH9	Logical Channel 9 Status Register	16	R	0000h
FFFE:DA48	SYS_DMA_CSSA_L_CH9	Logical Channel 9 Source Start Address Register LSB	16	RW	undef
FFFE:DA4A	SYS_DMA_CSSA_U_CH9	Logical Channel 9 Source Start Address Register MSB	16	RW	undef
FFFE:DA4C	SYS_DMA_CDSA_L_CH9	Logical Channel 9 Destination Start Address Register LSB	16	RW	undef
FFFE:DA4E	SYS_DMA_CDSA_U_CH9	Logical Channel 9 Destination Start Address Register MSB	16	RW	undef
FFFE:DA50	SYS_DMA_CEN_CH9	Logical Channel 9 Element Number Register	16	RW	undef
FFFE:DA52	SYS_DMA_CFN_CH9	Logical Channel 9 Frame Number Register	16	RW	undef

Table 3−11. System DMA Controller Registers (Continued)

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:DA54	SYS_DMA_CSFI_CH9	Logical Channel 9 Source Frame Index Register	16	RW	undef
FFFE:DA56	SYS_DMA_CSEI_CH9	Logical Channel 9 Source Element Index Register	16	RW	undef
FFFE:DA58	SYS_DMA_CSAC_CH9	Logical Channel 9 Source Address Counter Register	16	R	undef
FFFE:DA5A	SYS_DMA_CDAC_CH9	Logical Channel 9 Destination Address Counter Register	16	R	undef
FFFE:DA5C	SYS_DMA_CDEI_CH9	Logical Channel 9 Destination Element Index Register	16	RW	undef
FFFE:DA5E	SYS_DMA_CDFI_CH9	Logical Channel 9 Destination Frame Index Register	16	RW	undef
FFFE:DA60	SYS_DMA_COLOR_L_CH9	Logical Channel 9 Color Parameter Register, Lower Bits	16	RW	undef
FFFE:DA62	SYS_DMA_COLOR_U_CH9	Logical Channel 9 Color Parameter Register, Upper Bits	16	RW	undef
FFFE:DA64	SYS_DMA_CCR2	Channel Control Register 2	16	RW	undef
FFFE:DA68	SYS_DMA_CLNK_CTRL	Channel Link Control Register	16	RW	undef
FFFE:DA6A	SYS_DMA_LCH_CTRL	Logical Channel Control Register	16	RW	undef
FFFE:DA6C − FFFE:DA7F		Reserved			
FFFE:DA80	SYS_DMA_CSDP_CH10	Logical Channel 10 Source/Destination Parameters Register	16	RW	0000h
FFFE:DA82	SYS_DMA_CCR_CH10	Logical Channel 10 Control Register	16	RW	0000h
FFFE:DA84	SYS_DMA_CICR_CH10	Logical Channel 10 Interrupt Control Register	16	RW	0003h
FFFE:DA86	SYS_DMA_CSR_CH10	Logical Channel 10 Status Register	16	R	0000h
FFFE:DA88	SYS_DMA_CSSA_L_CH10	Logical Channel 10 Source Start Address Register LSB	16	RW	undef
FFFE:DA8A	SYS_DMA_CSSA_U_CH10	Logical Channel 10 Source Start Address Register MSB	16	RW	undef
FFFE:DA8C	SYS_DMA_CDSA_L_CH10	Logical Channel 10 Destination Start Address Register LSB	16	RW	undef
FFFE:DA8E	SYS_DMA_CDSA_U_CH10	Logical Channel 10 Destination Start Address Register MSB	16	RW	undef
FFFE:DA90	SYS_DMA_CEN_CH10	Logical Channel 10 Element Number Register	16	RW	undef
FFFE:DA92	SYS_DMA_CFN_CH10	Logical Channel 10 Frame Number Register	16	RW	undef
FFFE:DA94	SYS_DMA_CSFI_CH10	Logical Channel 10 Source Frame Index Register	16	RW	undef
FFFE:DA96	SYS_DMA_CSEI_CH10	Logical Channel 10 Source Element Index Register	16	RW	undef
FFFE:DA98	SYS_DMA_CSAC_CH10	Logical Channel 10 Source Address Counter Register	16	R	undef
FFFE:DA9A	SYS_DMA_CDAC_CH10	Logical Channel 10 Destination Address Counter Register	16	R	undef
FFFE:DA9C	SYS_DMA_CDEI_CH10	Logical Channel 10 Destination Element Index Register	16	RW	undef
FFFE:DA9E	SYS_DMA_CDFI_CH10	Logical Channel 10 Destination Frame Index Register	16	RW	undef

Table 3−11. System DMA Controller Registers (Continued)

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:DAA0	SYS_DMA_COLOR_L_CH0	Logical Channel 10 Color Parameter Register, Lower Bits	16	RW	undef
FFFE:DAA2	SYS_DMA_COLOR_U_CH0	Logical Channel 10 Color Parameter Register, Upper Bits	16	RW	undef
FFFE:DAA4	SYS_DMA_CCR2	Channel Control Register 2	16	RW	undef
FFFE:DAA8	SYS_DMA_CLNK_CTRL	Channel Link Control Register	16	RW	undef
FFFE:DAAA	SYS_DMA_LCH_CTRL	Logical Channel Control Register	16	RW	undef
FFFE:DAAC − FFFE:DABF		Reserved			
FFFE:DAC0	SYS_DMA_CSDP_CH11	Logical Channel 11 Source/Destination Parameters Register	16	RW	0000h
FFFE:DAC2	SYS_DMA_CCR_CH11	Logical Channel 11 Control Register	16	RW	0000h
FFFE:DAC4	SYS_DMA_CICR_CH11	Logical Channel 11 Interrupt Control Register	16	RW	0003h
FFFE:DAC6	SYS_DMA_CSR_CH11	Logical Channel 11 Status Register	16	R	0000h
FFFE:DAC8	SYS_DMA_CSSA_L_CH11	Logical Channel 11 Source Start Address Register LSB	16	RW	undef
FFFE:DACA	SYS_DMA_CSSA_U_CH11	Logical Channel 11 Source Start Address Register MSB	16	RW	undef
FFFE:DACC	SYS_DMA_CDSA_L_CH11	Logical Channel 11 Destination Start Address Register LSB	16	RW	undef
FFFE:DACE	SYS_DMA_CDSA_U_CH11	Logical Channel 11 Destination Start Address Register MSB	16	RW	undef
FFFE:DAD0	SYS_DMA_CEN_CH11	Logical Channel 11 Element Number Register	16	RW	undef
FFFE:DAD2	SYS_DMA_CFN_CH11	Logical Channel 11 Frame Number Register	16	RW	undef
FFFE:DAD4	SYS_DMA_CSFI_CH11	Logical Channel 11 Source Frame Index Register	16	RW	undef
FFFE:DAD6	SYS_DMA_CSEI_CH11	Logical Channel 11 Source Element Index Register	16	RW	undef
FFFE:DAD8	SYS_DMA_CSAC_CH11	Logical Channel 11 Source Address Counter Register	16	R	undef
FFFE:DADA	SYS_DMA_CDAC_CH11	Logical Channel 11 Destination Address Counter Register	16	R	undef
FFFE:DADC	SYS_DMA_CDEI_CH11	Logical Channel 11 Destination Element Index Register	16	RW	undef
FFFE:DADE	SYS_DMA_CDFI_CH11	Logical Channel 11 Destination Frame Index Register	16	RW	undef
FFFE:DAE0	SYS_DMA_COLOR_L_C11	Logical Channel 11 Color Parameter Register, Lower Bits	16	RW	undef
FFFE:DAE2	SYS_DMA_COLOR_U_CH11	Logical Channel 11 Color Parameter Register, Upper Bits	16	RW	undef
FFFE:DAE4	SYS_DMA_CCR2	Channel Control Register 2	16	RW	undef
FFFE:DAE8	SYS_DMA_CLNK_CTRL	Channel Link Control Register	16	RW	undef
FFFE:DAEA	SYS_DMA_LCH_CTRL	Logical Channel Control Register	16	RW	undef
FFFE:DAEC − FFFE:DAFF		Reserved			
FFFE:DB00	SYS_DMA_CSDP_CH12	Logical Channel 12 Source/Destination Parameters Register	16	RW	0000h
FFFE:DB02	SYS_DMA_CCR_CH12	Logical Channel 12 Control Register	16	RW	0000h

Table 3−11. System DMA Controller Registers (Continued)

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:DB04	SYS_DMA_CICR_CH12	Logical Channel 12 Interrupt Control Register	16	RW	0003h
FFFE:DB06	SYS_DMA_CSR_CH12	Logical Channel 12 Status Register	16	R	0000h
FFFE:DB08	SYS_DMA_CSSA_L_CH12	Logical Channel 12 Source Start Address Register LSB	16	RW	undef
FFFE:DB0A	SYS_DMA_CSSA_U_CH12	Logical Channel 12 Source Start Address Register MSB	16	RW	undef
FFFE:DB0C	SYS_DMA_CDSA_L_CH12	Logical Channel 12 Destination Start Address Register LSB	16	RW	undef
FFFE:DB0E	SYS_DMA_CDSA_U_CH12	Logical Channel 12 Destination Start Address Register MSB	16	RW	undef
FFFE:DB10	SYS_DMA_CEN_CH12	Logical Channel 12 Element Number Register	16	RW	undef
FFFE:DB12	SYS_DMA_CFN_CH12	Logical Channel 12 Frame Number Register	16	RW	undef
FFFE:DB14	SYS_DMA_CSFI_CH12	Logical Channel 12 Source Frame Index Register	16	RW	undef
FFFE:DB16	SYS_DMA_CSEI_CH12	Logical Channel 12 Source Element Index Register	16	RW	undef
FFFE:DB18	SYS_DMA_CSAC_CH12	Logical Channel 12 Source Address Counter Register	16	R	undef
FFFE:DB1A	SYS_DMA_CDAC_CH12	Logical Channel 12 Destination Address Counter Register	16	R	undef
FFFE:DB1C	SYS_DMA_CDEI_CH12	Logical Channel 12 Destination Element Index Register	16	RW	undef
FFFE:DB1E	SYS_DMA_CDFI_CH12	Logical Channel 12 Destination Frame Index Register	16	RW	undef
FFFE:DB20	SYS_DMA_COLOR_L_CH12	Logical Channel 12 Color Parameter Register, Lower Bits	16	RW	undef
FFFE:DB22	SYS_DMA_COLOR_U_CH12	Logical Channel12 Color Parameter Register, Upper Bits	16	RW	undef
FFFE:DB24	SYS_DMA_CCR2	Channel Control Register 2	16	RW	undef
FFFE:DB28	SYS_DMA_CLNK_CTRL	Channel Link Control Register	16	RW	undef
FFFE:DB2A	SYS_DMA_LCH_CTRL	Logical Channel Control Register	16	RW	undef
FFFE:DB2C − FFFE:DB3F		Reserved			
FFFE:DB40	SYS_DMA_CSDP_CH13	Logical Channel 13 Source/Destination Parameters Register	16	RW	0000h
FFFE:DB42	SYS_DMA_CCR_CH13	Logical Channel 13 Control Register	16	RW	0000h
FFFE:DB44	SYS_DMA_CICR_CH13	Logical Channel 13 Interrupt Control Register	16	RW	0003h
FFFE:DB46	SYS_DMA_CSR_CH13	Logical Channel 13 Status Register	16	R	0000h
FFFE:DB48	SYS_DMA_CSSA_L_CH13	Logical Channel 13 Source Start Address Register LSB	16	RW	undef
FFFE:DB4A	SYS_DMA_CSSA_U_CH13	Logical Channel 13 Source Start Address Register MSB	16	RW	undef
FFFE:DB4C	SYS_DMA_CDSA_L_CH13	Logical Channel 13 Destination Start Address Register LSB	16	RW	undef
FFFE:DB4E	SYS_DMA_CDSA_U_CH13	Logical Channel 13 Destination Start Address Register MSB	16	RW	undef

Table 3−11. System DMA Controller Registers (Continued)

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:DB50	SYS_DMA_CEN_CH13	Logical Channel 13 Element Number Register	16	RW	undef
FFFE:DB52	SYS_DMA_CFN_CH13	Logical Channel 13 Frame Number Register	16	RW	undef
FFFE:DB54	SYS_DMA_CSFI_CH13	Logical Channel 13 Source Frame Index Register	16	RW	undef
FFFE:DB56	SYS_DMA_CSEI_CH13	Logical Channel 13 Source Element Index Register	16	RW	undef
FFFE:DB58	SYS_DMA_CSAC_CH13	Logical Channel 13 Source Address Counter Register	16	R	undef
FFFE:DB5A	SYS_DMA_CDAC_CH13	Logical Channel 13 Destination Address Counter Register	16	R	undef
FFFE:DB5C	SYS_DMA_CDEI_CH13	Logical Channel 13 Destination Element Index Register	16	RW	undef
FFFE:DB5E	SYS_DMA_CDFI_CH13	Logical Channel 13 Destination Frame Index Register	16	RW	undef
FFFE:DB60	SYS_DMA_COLOR_L_CH13	Logical Channel 13 Color Parameter Register, Lower Bits	16	RW	undef
FFFE:DB62	SYS_DMA_COLOR_U_CH13	Logical Channel 13 Color Parameter Register, Upper Bits	16	RW	undef
FFFE:DB64	SYS_DMA_CCR2	Channel Control Register 2	16	RW	undef
FFFE:DB68	SYS_DMA_CLNK_CTRL	Channel Link Control Register	16	RW	undef
FFFE:DB6A	SYS_DMA_LCH_CTRL	Logical Channel Control Register	16	RW	undef
FFFE:DB60 − FFFE:DB7F		Reserved			
FFFE:DB80	SYS_DMA_CSDP_CH14	Logical Channel 14 Source/Destination Parameters Register	16	RW	0000h
FFFE:DB82	SYS_DMA_CCR_CH14	Logical Channel 14 Control Register	16	RW	0000h
FFFE:DB84	SYS_DMA_CICR_CH14	Logical Channel 14 Interrupt Control Register	16	RW	0003h
FFFE:DB86	SYS_DMA_CSR_CH14	Logical Channel 14 Status Register	16	R	0000h
FFFE:DB88	SYS_DMA_CSSA_L_CH14	Logical Channel 14 Source Start Address Register LSB	16	RW	undef
FFFE:DB8A	SYS_DMA_CSSA_U_CH14	Logical Channel 14 Source Start Address Register MSB	16	RW	undef
FFFE:DB8C	SYS_DMA_CDSA_L_CH14	Logical Channel 14 Destination Start Address Register LSB	16	RW	undef
FFFE:DB8E	SYS_DMA_CDSA_U_CH14	Logical Channel 14 Destination Start Address Register MSB	16	RW	undef
FFFE:DB90	SYS_DMA_CEN_CH14	Logical Channel 14 Element Number Register	16	RW	undef
FFFE:DB92	SYS_DMA_CFN_CH14	Logical Channel 14 Frame Number Register	16	RW	undef
FFFE:DB94	SYS_DMA_CSFI_CH14	Logical Channel 14 Source Frame Index Register	16	RW	undef
FFFE:DB96	SYS_DMA_CSEI_CH14	Logical Channel 14 Source Element Index Register	16	RW	undef
FFFE:DB98	SYS_DMA_CSAC_CH14	Logical Channel 14 Source Address Counter Register	16	R	undef
FFFE:DB9A	SYS_DMA_CDAC_CH14	Logical Channel 14 Destination Address Counter Register	16	R	undef

Table 3−11. System DMA Controller Registers (Continued)

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:DB9C	SYS_DMA_CDEI_CH14	Logical Channel 14 Destination Element Index Register	16	RW	undef
FFFE:DB9E	SYS_DMA_CDFI_CH14	Logical Channel 14 Destination Frame Index Register	16	RW	undef
FFFE:DBA0	SYS_DMA_COLOR_L_CH14	Logical Channel 14 Color Parameter Register, Lower Bits	16	RW	undef
FFFE:DBA2	SYS_DMA_COLOR_U_CH14	Logical Channel 14 Color Parameter Register, Upper Bits	16	RW	undef
FFFE:DBA4	SYS_DMA_CCR2	Channel Control Register 2	16	RW	undef
FFFE:DBA8	SYS_DMA_CLNK_CTRL	Channel Link Control Register	16	RW	undef
FFFE:DBAA	SYS_DMA_LCH_CTRL	Logical Channel Control Register	16	RW	undef
FFFE:DBAC − FFFE:DBBF		Reserved			
FFFE:DBC0	SYS_DMA_CSDP_CH15	Logical Channel 15 Source/Destination Parameters Register	16	RW	0000h
FFFE:DBC2	SYS_DMA_CCR_CH15	Logical Channel 15 Control Register	16	RW	0000h
FFFE:DBC4	SYS_DMA_CICR_CH15	Logical Channel 15 Interrupt Control Register	16	RW	0003h
FFFE:DBC6	SYS_DMA_CSR_CH15	Logical Channel 15 Status Register	16	R	0000h
FFFE:DBC8	SYS_DMA_CSSA_L_CH15	Logical Channel 15 Source Start Address Register LSB	16	RW	undef
FFFE:DBCA	SYS_DMA_CSSA_U_CH15	Logical Channel 15 Source Start Address Register MSB	16	RW	undef
FFFE:DBCC	SYS_DMA_CDSA_L_CH15	Logical Channel 15 Destination Start Address Register LSB	16	RW	undef
FFFE:DBCE	SYS_DMA_CDSA_U_CH15	Logical Channel 15 Destination Start Address Register MSB	16	RW	undef
FFFE:DBD0	SYS_DMA_CEN_CH15	Logical Channel 15 Element Number Register	16	RW	undef
FFFE:DBD2	SYS_DMA_CFN_CH15	Logical Channel 15 Frame Number Register	16	RW	undef
FFFE:DBD4	SYS_DMA_CSFI_CH15	Logical Channel 15 Source Frame Index Register	16	RW	undef
FFFE:DBD6	SYS_DMA_CSEI_CH15	Logical Channel 15 Source Element Index Register	16	RW	undef
FFFE:DBD8	SYS_DMA_CSAC_CH15	Logical Channel 15 Source Address Counter Register	16	R	undef
FFFE:DBDA	SYS_DMA_CDAC_CH15	Logical Channel 15 Destination Address Counter Register	16	R	undef
FFFE:DBDC	SYS_DMA_CDEI_CH15	Logical Channel 15 Destination Element Index Register	16	RW	undef
FFFE:DBDE	SYS_DMA_CDFI_CH15	Logical Channel 15 Destination Frame Index Register	16	RW	undef
FFFE:DBE0	SYS_DMA_COLOR_L_CH15	Logical Channel 15 Color Parameter Register, Lower Bits	16	RW	undef
FFFE:DBE2	SYS_DMA_COLOR_U_CH15	Logical Channel 15 Color Parameter Register, Upper Bits	16	RW	undef
FFFE:DBE4	SYS_DMA_CCR2	Channel Control Register 2	16	RW	undef
FFFE:DBE8	SYS_DMA_CLNK_CTRL	Channel Link Control Register	16	RW	undef
FFFE:DBEA	SYS_DMA_LCH_CTRL	Logical Channel Control Register	16	RW	undef

Table 3−11. System DMA Controller Registers (Continued)

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:DBEC − FFFE:DBFF		Reserved			
FFFE:DC00	SYS_DMA_GCR	System DMA Global Control Register	16	RW	0000h
FFFE:DC02		Reserved			
FFFE:DC04	SYS_DMA_GSCR	System DMA Software Compatible Register	16	RW	0000h
FFFE:DC06		Reserved			
FFFE:DC08	SYS_DMA_GRST	System DMA Global Software Reset Control Register	16	RW	0000h
FFFE:DC0A − FFFE:DC41		Reserved			
FFFE:DC42	SYS_DMA_HW_ID	System DMA Version ID Register	16	R	0001h
FFFE:DC44	SYS_DMA_PCh2_ID	System DMA Physical Channel 2 Version ID Register	16	R	0001h
FFFE:DC46	SYS_DMA_PCh0_ID	System DMA Physical Channel 0 Version ID Register	16	R	0001h
FFFE:DC48	SYS_DMA_PCh1_ID	System DMA Physical Channel 1 Version ID Register	16	R	0001h
FFFE:DC4A − FFFE:DC4D		Reserved			
FFFE:DC4E	SYS_DMA_CAPS_0_U	System DMA Global DMA Capability U Register 0	16	R	000Ch
FFFE:DC50	SYS_DMA_CAPS_0_L	System DMA Global DMA Capability L Register 0	16	R	0000h
FFFE:DC52	SYS_DMA_CAPS_1_U	System DMA Global DMA Capability U Register 1	16	R	undef
FFFE:DC54	SYS_DMA_CAPS_1_L	System DMA Global DMA Capability L Register 1	16	R	0000h
FFFE:DC56	SYS_DMA_CAPS_2	System DMA Global DMA Capability Register 2	16	R	01FFh
FFFE:DC58	SYS_DMA_CAPS_3	System DMA Global DMA Capability Register 3	16	R	001Fh
FFFE:DC5A	SYS_DMA_CAPS_4	System DMA Global DMA Capability Register 4	16	R	007Fh
FFFE:DC5C − FFFE:DC5F		Reserved			
FFFE:DC60	SYS_DMA_PCh2_SR	System DMA Physical Channel 2 Status Register	16	R	00FFh
FFFE:DC62 − FFFE:DC7F		Reserved			
FFFE:DC80	SYS_DMA_PCh0_SR	System DMA Physical Channel 0 Status Register	16	R	00FFh
FFFE:DC82	SYS_DMA_PCh1_SR	System DMA Physical Channel 1 Status Register	16	R	00FFh
FFFE:DC84 − FFFE:DCC0		Reserved			

3.2.2.2 MPU Public Peripheral Registers

The MPU public peripheral registers include the following:

- USB On-the-Go (OTG) Registers
- MICROWIRE Registers
- USB Client Registers
- Real-Time Clock (RTC) Registers
- MPUIO (Keyboard Included) Registers
- Pulse Width Light (PWL) Registers
- Pulse Width Tone (PWT) Registers
- MMC/SDIO1 Registers
- OS Timer 32-kHz Registers
- USB Host Registers
- Frame Adjustment Counter (FAC) Registers
- HDQ/1-Wire Interface Registers
- LED Pulse Generator 1 (LPG1) Registers
- LED Pulse Generator 2 (LPG2) Registers

Table 3−12. USB On-the-Go (OTG) Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFB:0700	USB_OTG_REV	USB On-the-Go Revision Number	32	R	0000 0000h
FFFB:0704	USB_OTG_SYSCON1	USB On-the-Go Configuration Register 1	32	R/W	0000 0000h
FFFB:0708	USB_OTG_SYSCON2	USB On-the-Go Configuration Register 2	32	R/W	0000 0000h
FFFB:070C	USB_OTG_CTRL	USB On-the-Go Control Register	32	R/W	0000 0000h
FFFB:0710	USB_OTG_IRQ_EN	USB On-the-Go Interrupt Enable Register	32	R/W	0000 0000h
FFFB:0714	USB_OTG_IRQ_SRC	USB On-the-Go Interrtup Status Register	32	R/W	0000 0000h
FFFB:0718	USB_OTG_OUTCTRL	USB On-the-Go Output Pins Control Register	32	R/W	0000 0000h
FFFB:0720	USB_OTG_TEST	USB On-the-Go Test Register	32	R/W	0000 0000h
FFFB:07FC	USB_OTG_VC	USB On-the-Go Vendor Code Register	32	R	undefined

Table 3−13. MICROWIRE Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFB:3000	MWIRE_RDR	MICROWIRE Receive Data Register	16	R	undefined
FFFB:3000	MWIRE_TDR	MICROWIRE Transmit Data Register	16	W	undefined
FFFB:3004	MWIRE_CSR	MICROWIRE Control And Status Register	16	R/W	undefined
FFFB:3008	MWIRE_SR1	MICROWIRE Setup Register for CS0 and CS1	16	R/W	undefined
FFFB:300C	MWIRE_SR2	MICROWIRE Setup Register for CS2 and CS3	16	R/W	undefined
FFFB:3010	MWIRE_SR3	MICROWIRE Setup Register for Internal Clock	16	R/W	undefined
FFFB:3014	MWIRE_SR4	MICROWIRE Setup Register for Clock Polarity	16	R/W	undefined
FFFB:3018	MWIRE_SR5	MICROWIRE Setup Register for Transmit Mode	16	R/W	0000h

Table 3−14. USB Client Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFB:4000	USB_CLNT_REV	USB Client Revision Register	16	R	0x0021
FFFB:4004	USB_CLNT_EP_NUM	USB Client Endpoint Selection Register	16	R/W	0x0000
FFFB:4008	USB_CLNT_DATA	USB Client Data Register	16	R/W	0x0000
FFFB:400C	USB_CLNT_CTRL	USB Client Control Register	16	R	0x0000
FFFB:4010	USB_CLNT_STAT_FLG	USB Client Status Flag Register	16	R	0x8202
FFFB:4014	USB_CLNT_RXFSTAT	USB Client Receive FIFO Status Register	16	R	0x0000
FFFB:4018	USB_CLNT_SYSCON1	USB Client System Configuration 1 Register	16	R/W	0x0000
FFFB:401C	USB_CLNT_SYSCON2	USB Client System Configuration 2 Register	16	R/W	0x0000
FFFB:4020	USB_CLNT_DEVSTAT	USB Client Device Status Register	16	R	0x0000
FFFB:4024	USB_CLNT_SOF	USB Client Start of Frame Register	16	R	0x0000
FFFB:4028	USB_CLNT_IRQ_EN	USB Client Interrupt Enable Register	16	R/W	0x0000
FFFB:402C	USB_CLNT_DMA_IRQ_EN	USB Client DMA Interrupt Enable Register	16	R/W	0x0000
FFFB:4030	USB_CLNT_IRQ_SRC	USB Client Interrupt Source Register	16	R/W	0x0000
FFFB:4034	USB_CLNT_EPN_STAT	USB Client Non-ISO Endpoint Interrupt Enable Register	16	R	0x0000
FFFB:4038	USB_CLNT_DMAIN_STAT	USB Client Non-ISO DMA Interrupt Enable Register	16	R	0x0000
FFFB:403C	Reserved				
FFFB:4040	USB_CLNT_RXDMA_CFG	USB Client DMA Receive Channels Configuration Register	16	R/W	0x0000
FFFB:4044	USB_CLNT_TXDMA_CFG	USB Client DMA Transmit Channels Configuration Register	16	R/W	0x0000
FFFB:4048	USB_CLNT_DATA_DMA	USB Client DMA FIFO Data Register	16	R/W	0x0000
FFFB:404C	Reserved				
FFFB:4050	USB_CLNT_TXDMA0	USB Client Transmit DMA Control 0 Register	16	R/W	0x0000
FFFB:4054	USB_CLNT_TXDMA1	USB Client Transmit DMA Control 1 Register	16	R/W	0x0000
FFFB:4058	USB_CLNT_TXDMA2	USB Client Transmit DMA Control 2 Register	16	R/W	0x0000
FFFB:405C	Reserved				
FFFB:4060	USB_CLNT_RXDMA0	USB Client Receive DMA Control 0 Register	16	R	0x0000
FFFB:4064	USB_CLNT_RXDMA1	USB Client Receive DMA Control 1 Register	16	R	0x0000
FFFB:4068	USB_CLNT_RXDMA2	USB Client Receive DMA Control 2 Register	16	R	0x0000

† During reset, Bit 15 is zero and other bit values are undetermined (i.e., the values are unknown until the first write access.)

Table 3−14. USB Client Registers (Continued)

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFB:406C − FFFB:407F	Reserved				
FFFB:4084	USB_CLNT_EP1_RX	USB Client Receive Endpoint Configuration 1 Register	16	R/W	0x0†
FFFB:4088	USB_CLNT_EP2_RX	USB Client Receive Endpoint Configuration 2 Register	16	R/W	0x0†
FFFB:408C	USB_CLNT_EP3_RX	USB Client Receive Endpoint Configuration 3 Register	16	R/W	0x0†
FFFB:4090	USB_CLNT_EP4_RX	USB Client Receive Endpoint Configuration 4 Register	16	R/W	0x0†
FFFB:4094	USB_CLNT_EP5_RX	USB Client Receive Endpoint Configuration 5 Register	16	R/W	0x0†
FFFB:4098	USB_CLNT_EP6_RX	USB Client Receive Endpoint Configuration 6 Register	16	R/W	0x0†
FFFB:409C	USB_CLNT_EP7_RX	USB Client Receive Endpoint Configuration 7 Register	16	R/W	0x0†
FFFB:40A0	USB_CLNT_EP8_RX	USB Client Receive Endpoint Configuration 8 Register	16	R/W	0x0†
FFFB:40A4	USB_CLNT_EP9_RX	USB Client Receive Endpoint Configuration 9 Register	16	R/W	0x0†
FFFB:40A8	USB_CLNT_EP10_RX	USB Client Receive Endpoint Configuration 10 Register	16	R/W	0x0†
FFFB:40AC	USB_CLNT_EP11_RX	USB Client Receive Endpoint Configuration 11 Register	16	R/W	0x0†
FFFB:40B0	USB_CLNT_EP12_RX	USB Client Receive Endpoint Configuration 12 Register	16	R/W	0x0†
FFFB:40B4	USB_CLNT_EP13_RX	USB Client Receive Endpoint Configuration 13 Register	16	R/W	0x0†
FFFB:40B8	USB_CLNT_EP14_RX	USB Client Receive Endpoint Configuration 14 Register	16	R/W	0x0†
FFFB:40BC	USB_CLNT_EP15_RX	USB Client Receive Endpoint Configuration 15 Register	16	R/W	0x0†
FFFB:40C0	Reserved				
FFFB:40C4	USB_CLNT_EP1_TX	USB Client Transmit Endpoint Configuration 1 Register	16	R/W	0x0†
FFFB:40C8	USB_CLNT_EP2_TX	USB Client Transmit Endpoint Configuration 2 Register	16	R/W	0x0†
FFFB:40CC	USB_CLNT_EP3_TX	USB Client Transmit Endpoint Configuration 3 Register	16	R/W	0x0†
FFFB:40D0	USB_CLNT_EP4_TX	USB Client Transmit Endpoint Configuration 4 Register	16	R/W	0x0†
FFFB:40D4	USB_CLNT_EP5_TX	USB Client Transmit Endpoint Configuration 5 Register	16	R/W	0x0†
FFFB:40D8	USB_CLNT_EP6_TX	USB Client Transmit Endpoint Configuration 6 Register	16	R/W	0x0†
FFFB:40DC	USB_CLNT_EP7_TX	USB Client Transmit Endpoint Configuration 7 Register	16	R/W	0x0†
FFFB:40E0	USB_CLNT_EP8_TX	USB Client Transmit Endpoint Configuration 8 Register	16	R/W	0x0†

† During reset, Bit 15 is zero and other bit values are undetermined (i.e., the values are unknown until the first write access.)

Table 3−14. USB Client Registers (Continued)

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFB:40E4	USB_CLNT_EP9_TX	USB Client Transmit Endpoint Configuration 9 Register	16	R/W	0x0†
FFFB:40E8	USB_CLNT_EP10_TX	USB Client Transmit Endpoint Configuration 10 Register	16	R/W	0x0†
FFFB:40EC	USB_CLNT_EP11_TX	USB Client Transmit Endpoint Configuration 11 Register	16	R/W	0x0†
FFFB:40F0	USB_CLNT_EP12_TX	USB Client Transmit Endpoint Configuration 12 Register	16	R/W	0x0†
FFFB:40F4	USB_CLNT_EP13_TX	USB Client Transmit Endpoint Configuration 13 Register	16	R/W	0x0†
FFFB:40F8	USB_CLNT_EP14_TX	USB Client Transmit Endpoint Configuration 14 Register	16	R/W	0x0†
FFFB:40FC	USB_CLNT_EP15_TX	USB Client Transmit Endpoint Configuration 15 Register	16	R/W	0x0†

† During reset, Bit 15 is zero and other bit values are undetermined (i.e., the values are unknown until the first write access.)

Table 3−15. Real-Time Clock (RTC) Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFB:4800	SECONDS_REG	RTC Seconds Register	8	R/W	00h
FFFB:4804	MINUTES_REG	RTC Minutes Register	8	R/W	00h
FFFB:4808	HOURS_REG	RTC Hours Register	8	R/W	00h
FFFB:480C	DAYS_REG	RTC Days Register	8	R/W	01h
FFFB:4810	MONTHS_REG	RTC Months Register	8	R/W	01h
FFFB:4814	YEARS_REG	RTC Years Register	8	R/W	00h
FFFB:4818	WEEK_REG	RTC Weeks Register	8	R/W	00h
FFFB:481C		Reserved			
FFFB:4820	ALARM_SECONDS_REG	RTC Alarm Seconds Register	8	R/W	00h
FFFB:4824	ALARM_MINUTES_REG	RTC Alarm Minutes Register	8	R/W	00h
FFFB:4828	ALARM_HOURS_REG	RTC Alarm Hours Register	8	R/W	00h
FFFB:482C	ALARM_DAYS_REG	RTC Alarm Days Register	8	R/W	01h
FFFB:4830	ALARM_MONTHS_REG	RTC Alarm Months Register	8	R/W	01h
FFFB:4834	ALARM_YEARS_REG	RTC Alarm Years Register	8	R/W	00h
FFFB:4838 − FFFB:483F		Reserved			
FFFB:4840	RTC_CTRL_REG	RTC Control Register	8	R/W	00h
FFFB:4844	RTC_STATUS_REG	RTC Status Register	8	R/W	00h
FFFB:4848	RTC_INTERRUPTS_REG	RTC Interrupts Register	8	R/W	00h
FFFB:484C	RTC_COMP_LSB_REG	RTC Compensation LSB Register	8	R/W	00h
FFFB:4850	RTC_COMP_MSB_REG	RTC Compensation MSB Register	8	RW	00h
FFFB:4854	RTC_OSC_REG	RTC Oscillator Register	8	RW	0Bh

Table 3−16. MPUIO (Keyboard) Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFB:5000	MPUIO_INPUT_LATCH	MPUIO General Purpose Input Register	16	R	0000h
FFFB:5004	MPUIO_OUTPUT	MPUIO General Purpose Output Register	16	R/W	0000h
FFFB:5008	MPUIO_IO_CNTL	MPUIO In/Out Control Register for General-Purpose I/O	16	R/W	FFFFh
FFFB:5010	MPUIO_KBD_LATCH	MPUIO Keyboard Row Input Register	16	R	FFFFh
FFFB:5014	MPUIO_KBC	MPUIO Keyboard Column Ouput Register	16	R/W	FF00h
FFFB:5018	MPUIO_GPIO_EVENT	MPUIO GPIO Event Mode Register	16	R/W	0FE0h
FFFB:501C	MPUIO_GPIO_EDGE	MPUIO GPIO Interrupt Edge Register	16	R/W	0000h
FFFB:5020	MPUIO_KBD_INT	MPUIO Keyboard Interrupt Register	16	R	FFFFh
FFFB:5024	MPUIO_GPIO_INT	MPUIO GPIO Interrupt Register	16	R	0000h
FFFB:5028	MPUIO_KBD_MASKIT	MPUIO Keyboard Interrupt Mask Register	16	R/W	FFFEh
FFFB:502C	MPUIO_GPIO_MASKIT	MPUIO GPIO Interrupt Mask Register	16	R/W	0000h
FFFB:5030	MPUIO_GPIO_DBNC	MPUIO GPIO Debouncing Register	16	R/W	EF00h
FFFB:5034	MPUIO_GPIO_LATCH	MPUIO GPIO Latch Register	16	R	0000h

Table 3−17. Pulse Width Light (PWL) Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFB:5800	PWL_LEVEL	PWL Level Register	8	R/W	00h
FFFB:5804	PWL_CONTROL	PWL Control Register	8	R/W	00h

Table 3−18. Pulse Width Tone (PWT) Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFB:6000	PWT_FRC	PWT Frequency Control Register	8	R/W	00h
FFFB:6004	PWT_VRC	PWT Volume Control Register	8	R/W	00h
FFFB:6008	PWT_GCR	PWT General Control Register	8	R/W	00h

Table 3−19. MMC/SDIO1 Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFB:7800	MPU_MMC_CMD	MMC Command Register	16	R/W	0000h
FFFB:7804	MPU_MMC_ARGL	MMC Argument Register Low	16	R/W	0000h
FFFB:7808	MPU_MMC_ARGH	MMC Argument Register High	16	R/W	0000h
FFFB:780C	MPU_MMC_CON	MMC Module Configuration Register	16	R/W	0000h
FFFB:7810	MPU_MMC_STAT	MMC Module Status Register	16	R/W	0000h
FFFB:7814	MPU_MMC_IE	MMC System Interrupt Enable Register	16	R/W	0000h
FFFB:7818	MPU_MMC_CTO	MMC Command Time−Out Register	16	R/W	0000h
FFFB:781C	MPU_MMC_DTO	MMC Data Read Time−Out Register	16	R/W	0000h
FFFB:7820	MPU_MMC_DATA	MMC Data Access Register	16	R/W	0000h
FFFB:7824	MPU_MMC_BLEN	MMC Block Length Register	16	R/W	0000h
FFFB:7828	MPU_MMC_NBLK	MMC Numberf of Blocks Register	16	R/W	0000h
FFFB:782C	MPU_MMC_BUF	MMC Buffer Configuration Register	16	R/W	0000h

Table 3−19. MMC/SDIO1 Registers (Continued)

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFB:7830		Reserved			
FFFB:7834	MPU_MMC_SDIO	MMC SDIO Configuration Register	16	R/W	0000h
FFFB:7838	MPU_MMC_SYST	MMC System Test Register	16	R/W	0000h
FFFB:783C	MPU_MMC_REV	MMC Module Revision Register	16	R	undefined
FFFB:7840	MPU_MMC_RSP0	MMC Command Response Register 0	16	R	0000h
FFFB:7844	MPU_MMC_RSP1	MMC Command Response Register 1	16	R	0000h
FFFB:7848	MPU_MMC_RSP2	MMC Command Response Register 2	16	R	0000h
FFFB:784C	MPU_MMC_RSP3	MMC Command Response Register 3	16	R	0000h
FFFB:7850	MPU_MMC_RSP4	MMC Command Response Register 4	16	R	0000h
FFFB:7854	MPU_MMC_RSP5	MMC Command Response Register 5	16	R	0000h
FFFB:7858	MPU_MMC_RSP6	MMC Command Response Register 6	16	R	0000h
FFFB:785C	MPU_MMC_RSP7	MMC Command Response Register 7	16	R	0000h
FFFB:7860	MPU_MMC_IOSR	MMC Command Response IOSR Register	16	R/W	0000h
FFFB:7864	MPU_MMC_SYSC	MMC System Control Register	16	R/W	0000h
FFFB:7868	MPU_MMC_SYSS	MMC System Status Register	16	R	0000h

Table 3−20. OS Timer 32-kHz Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFB:9000	OS_TIMER_TICK_VAL	OS Timer 32K Tick Value Register	32	R/W	00FF FFFFh
FFFB:9004	OS_TIMER_TICK_CNTR	OS TIimer 32k Tick Counter Register	32	R	00FF FFFFh
FFFB:9008	OS_TIMER_CTRL	OS Timer 32k Timer Control Register	32	R/W	0000 0008h

Table 3−21. USB Host Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFB:A000h	USB_HC_REVISION	USB Host Controller OHCI Revision Number Register	R	32	0000 0010h
FFFB:A004h	USB_HC_CONTROL	USB Host Controller Operating Mode Register	R/W	32	xxxx xx00h
FFFB:A008h	USB_HC_CMD_STAT	USB Host Controller Command and Status Register	R/W	32	xxxx 0000h
FFFB:A00Ch	USB_HC_INT_STAT	USB Host Controller Interrupt Status Register	R/W	32	xxxx xxx0h
FFFB:A010h	USB_HC_INT_EN	USB Host Controller Interrupt Enable Register	R/W	32	xxxx xx00h
FFFB:A014h	USB_HC_INT_NEN	USB Host Controller Interrupt Disable Register	R/W	32	xxxx xxx0h
FFFB:A018h	USB_HC_HCCA	USB Host Controller HCCA Physical Address Register	R/W	32	0000 0000h
FFFB:A01Ch	USB_HC_PRD_CUR_EN	USB Host Controller Physical Address of Current Period Endpoint Descriptor Register	R/W	32	0000 0000h
FFFB:A020h	USB_HC_CTRL_HEAD	USB Host Controller Physical Address of Head of Control Endpoint Descriptor List Register	R/W	32	0000 0000h
FFFB:A024h	USB_HC_CTRL_CUR_EN	USB Host Controller Physical Address of Current Control Endpoint Descriptor Register	R/W	32	0000 0000h
FFFB:A028h	USB_HC_BLK_HEAD_EN	USB Host Controller Physical Address of Head of Bulk End Point Descriptor List Register	R/W	32	0000 0000h
FFFB:A02Ch	USB_HC_BLK_CUR_EN	USB Host Controller Physical Address of Current Bulk Endpoint Descriptor Register	R/W	32	0000 0000h

† Bit 0 is zero.

Table 3−21. USB Host Registers (Continued)

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFB:A030h	USB_HC_DN_HEAD	USB Host Controller Physical Address of Head of List of Retired Transfer Descriptor Register	R	32	0000 0000h
FFFB:A034h	USB_HC_FM_INTVRL	USB Host Controller Frame Interval Register	R/W	32	0000 xEDFh
FFFB:A038h	USB_HC_FM_RMN	USB Host Controller Frame Remaining Register	R	32	0000 0000h
FFFB:A03Ch	USB_HC_FM_NMB	USB Host Controller Frame Number Remaining Register	R	32	0000 0000h
FFFB:A040h	USB_HC_PRD_SRT	USB Host Controller Period Start Register	R/W	32	xxxx x000h
FFFB:A044h	USB_HC_LSPD_TRSH	USB Host Controller Low Speed Threshold Register	R/W	32	0Axx X203h
FFFB:A048h	USB_HC_RH_DSC_A	USB Host Controller Root Hub A Register	R/W	32	0000 0000h
FFFB:A04Ch	USB_HC_RH_DSC_B	USB Host Controller Root Hub B Register	R/W	32	0000 0000h
FFFB:A050h	USB_HC_RH_STS	USB Host Controller Root Hub Register	R/W	32	0000 0000h
FFFB:A054h	USB_HC_RH_PRT_STS1	USB Host Controller Port 1 Control and Status Register	R/W	32	0000 0100h
FFFB:A058h	USB_HC_RH_PRT_STS2	USB Host Controller Port 2 Control and Status Register	R/W	32	0000 0100h
FFFB:A05Ch	USB_HC_RH_PRT_STS3	USB Host Controller Port 3 Control and Status Register	R/W	32	0000 0100h
FFFB:A060h− FFFB:A0DFh		Reserved			
FFFB:A0E0h	USB_HC_UE_ADDR	USB Host Contrroller Host UE Address Register	R	32	0000 0000h
FFFB:A0E4h	USB_HC_UE_STAT	USB Host Contrroller Host UE Status Register	R	32	XXXX XXX†
FFFB:A0E8h	USB_HC_TM_OUT_CTRL	USB Host Controller Time Out Control Register	R/W	32	0000 0000h
FFFB:A0ECh	USB_HC_HST_REV	USB Host Controller Host Revision Register	R	32	XXXX XXX†

† Bit 0 is zero.

Table 3−22. Frame Adjustment Counter (FAC) Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFB:A800	FAC_CNT	FAC Frame Adjustment Reference Counter Register	16	R/W	0000h
FFFB:A810	FAC_SYNC_CNT	FAC Sync Counter Register	16	R	0000h
FFFB:A814	FAC_START_CNT	FAC Start Counter Register	16	R	0000h
FFFB:A804	FAC_CNT_RSLT	FAC Frame Starter Count Register	16	R	0000h
FFFB:A808	FAC_CTRL	FAC Control Register	16	R/W	0000h
FFFB:A80C	FAC_STATUS	FAC Status Register	16	R	0000h

Table 3−23. HDQ/1-Wire Interface Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFB:C000	HDQ_TX_DATA	HDQ Transmit Register	32	R/W	0000 0000h
FFFB:C004	HDQ_RX_BUF	HDQ Receive Buffer Register	32	R	0000 0000h
FFFB:C008	HDQ_CNTL_STAT	HDQ Control and Status Register	32	R/W	0000 0000h
FFFB:C00C	HDQ_INT_STAT	HDQ Interrupt Status Register	32	R	0000 0000h

Table 3−24. LED Pulse Generator 1 (LPG1) Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFB:D000	LPG1_CNTL	LPG1 Control Register	8	R/W	00h
FFFB:D004	LPG1_PWR_MNGT	LPG1 Power Mangement Register	8	R/W	00h

Table 3−25. LED Pulse Generator 2 (LPG2) Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFB:D800	LPG2_CNTL	LPG2 Control Register	8	R/W	00h
FFFB:D804	LPG2_PWR_MNGT	LPG2 Power Mangement Register	8	R/W	00h

3.2.2.3 MPU/DSP Shared Peripheral Registers

The MPU public peripheral registers include the following:

- UART1 Registers
- UART2 Registers
- SPI1 Registers
- McBSP2 Registers
- General-Purpose Timer 1 Registers
- General-Purpose Timer 2 Registers
- General-Purpose Timer 3 Registers
- General-Purpose Timer 4 Registers
- General-Purpose Timer 5 Registers
- I^2C1 Registers
- General-Purpose Timer 6 Registers
- General-Purpose Timer 7 Registers
- MMC/SDIO2 Registers
- UART 3 Registers
- MPU GPIO3 Registers
- MPU GPIO4 Registers
- 32-kHz Synchro Count Registers
- General-Purpose Timer 8 Registers
- MPU GPIO1 Registers
- MPU GPIO2 Registers
- MPU/DSP Shared Mailbox Registers

Table 3−26. UART1 Registers

DSP WORD ADDRESS	MPU BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 8000h	FFFB:0000	UART1_RHR	UART1 receive holding register	8	R	Undefined
0x00 8000h	FFFB:0000	UART1_THR	UART1 transmit holding register	8	W	Undefined
0x00 8000h	FFFB:0000	UART1_DLL	UART1 divisor latch low register	8	R/W	00h
0x00 8001h	FFFB:0004	UART1_IER	UART1 interrupt enable register	8	R/W	00h
0x00 8001h	FFFB:0004	UART1_DLH	UART1 divisor latch high register	8	R/W	00h
0x00 8002h	FFFB:0008	UART1_IIR	UART1 interrupt identification register	8	R	01h
0x00 8002h	FFFB:0008	UART1_FCR	UART1 FIFO control register	8	W	00h
0x00 8002h	FFFB:0008	UART1_EFR	UART1 enhanced feature register	8	R/W	00h
0x00 8003h	FFFB:000C	UART1_LCR	UART1 line control register	8	R/W	00h
0x00 8004h	FFFB:0010	UART1_MCR	UART1 modem control register	8	R/W	00h
0x00 8004h	FFFB:0010	UART1_XON1	UART1 XON1 register	8	R/W	00h
0x00 8005h	FFFB:0014	UART1_LSR	UART1 mode register	8	R	60h
0x00 8005h	FFFB:0014	UART1_XON2	UART1 XON2 register	8	R/W	00h
0x00 8006h	FFFB:0018	UART1_MSR	UART1 modem status register	8	R	Undefined
0x00 8006h	FFFB:0018	UART1_TCR	UART1 transmission control register	8	R/W	0Fh
0x00 8006h	FFFB:0018	UART1_XOFF1	UART1 XOFF1 register	8	R/W	00h
0x00 8007h	FFFB:001C	UART1_SPR	UART1 scratchpad register	8	R/W	00h
0x00 8007h	FFFB:001C	UART1_TLR	UART1 trigger level register	8	R/W	00h
0x00 8007h	FFFB:001C	UART1_XOFF2	UART1 XOFF2 register	8	R/W	00h
0x00 8008h	FFFB:0020	UART1_MDR1	UART1 mode definition 1 register	8	R/W	07h
0x00 8009h	FFFB:0024	UART1_MDR2	UART1 mode definition register 2	8	R/W	00h
0x00 800Ah	FFFB:0028	UART1_SFLSR	UART1 status FIFO line status register	8	R	00h
0x00 800Ah	FFFB:0028	UART1_TXFLL	UART1 transmit frame length low	8	W	00h
0x00 800Bh	FFFB:002C	UART1_RESUME	UART1 resume register	8	R	00h
0x00 800Bh	FFFB:002C	UART1_TXFLH	UART1 transmit frame length high	8	W	00h
0x00 800Ch	FFFB:0030	UART1_SFREGL	UART1 status FIFO low register	8	R	Undefined
0x00 800Ch	FFFB:0030	UART1_RXFLL	UART1 receive frame length low	8	W	00h
0x00 800Dh	FFFB:0034	UART1_SFREGH	UART1 status FIFO high register	8	R	Undefined
0x00 800Dh	FFFB:0034	UART1_RXFLH	UART1 receive frame length high	8	W	00h
0x00 800Eh	FFFB:0038	UART1_UASR	UART1 autobauding status register	8	R	00h
0x00 800Eh	FFFB:0038	UART1_BLR	UART1 BOF control register	8	R/W	40h
0x00 800Fh	FFFB:003C	UART1_ACREG	UART1 auxiliary control register	8	R/W	00h
0x00 8010h	FFFB:0040	UART1_SCR	UART1 supplementary control register	8	R/W	00h
0x00 8011h	FFFB:0044	UART1_SSR	UART1 supplementary status register	8	R	00h
0x00 8012h	FFFB:0048	UART1_EBLR	UART1 BOF length register	8	R/W	00h
0x00 8013h	FFFB:004C		Reserved			
0x00 8014h	FFFB:0050	UART1_MVR	UART1 module version register	8	R	−
0x00 8015h	FFFB:0054	UART1_SYSC	UART1 system configuration register	8	R/W	00h
0x00 8016h	FFFB:0058	UART1_SYSS	UART1 system status register	8	R/W	00h
0x00 8017h	FFFB:005C	UART1_WER	UART1 wake-up enable register	8	R/W	7Fh

Table 3−27. UART2 Registers

DSP WORD ADDRESS	MPU BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 8400h	FFFB:0800	UART2_RHR	UART2 receive holding register	8	R	Undefined
0x00 8400h	FFFB:0800	UART2_THR	UART2 transmit holding register	8	W	Undefined
0x00 8400h	FFFB:0800	UART2_DLL	UART2 divisor latch low register	8	R/W	00h
0x00 8401h	FFFB:0804	UART2_IER	UART2 interrupt enable register	8	R/W	00h
0x00 8401h	FFFB:0804	UART2_DLH	UART2 divisor latch high register	8	R/W	00h
0x00 8402h	FFFB:0808	UART2_IIR	UART2 interrupt identification register	8	R	01h
0x00 8402h	FFFB:0808	UART2_FCR	UART2 FIFO control register	8	W	00h
0x00 8402h	FFFB:0808	UART2_EFR	UART2 enhanced feature register	8	R/W	00h
0x00 8403h	FFFB:080C	UART2_LCR	UART2 line control register	8	R/W	00h
0x00 8404h	FFFB:0810	UART2_MCR	UART2 modem control register	8	R/W	00h
0x00 8404h	FFFB:0810	UART2_XON1	UART2 XON1 register	8	R/W	00h
0x00 8405h	FFFB:0814	UART2_LSR	UART2 mode register	8	R	60h
0x00 8405h	FFFB:0814	UART2_XON2	UART2 XON2 register	8	R/W	00h
0x00 8406h	FFFB:0818	UART2_MSR	UART2 modem status register	8	R	Undefined
0x00 8406h	FFFB:0818	UART2_TCR	UART2 transmission control register	8	R/W	0Fh
0x00 8406h	FFFB:0818	UART2_XOFF	UART2 XOFF1 register	8	R/W	00h
0x00 8407h	FFFB:081C	UART2_SPR	UART2 scratchpad register	8	R/W	00h
0x00 8407h	FFFB:081C	UART2_TLR	UART2 trigger level register	8	R/W	00h
0x00 8407h	FFFB:081C	UART2_XOFF2	UART2 XOFF2 register	8	R/W	00h
0x00 8408h	FFFB:0820	UART2_MDR1	UART2 mode definition 1 register	8	R/W	07h
0x00 8409h	FFFB:0824	UART2_MDR2	UART2 mode definition register 2	8	R/W	00h
0x00 840Ah	FFFB:0828	UART2_SFLSR	UART2 status FIFO line status register	8	R	00h
0x00 840Ah	FFFB:0828	UART2_TXFLL	UART2 transmit frame length low	8	W	00h
0x00 840Bh	FFFB:082C	UART2_RESUME	UART2 resume register	8	R	00h
0x00 840Bh	FFFB:082C	UART2_TXFLH	UART2 transmit frame length high	8	W	00h
0x00 840Ch	FFFB:0830	UART2_SFREGL	UART2 status FIFO low register	8	R	Undefined
0x00 840Ch	FFFB:0830	UART2_RXFLL	UART2 receive frame length low	8	W	00h
0x00 840Dh	FFFB:0834	UART2_SFREGH	UART2 status FIFO high register	8	R	Undefined
0x00 840Dh	FFFB:0834	UART2_RXFLH	UART2 receive frame length high	8	W	00h
0x00 840Eh	FFFB:0838	UART2_UASR	UART2 autobauding status register	8	R	00h
0x00 840Eh	FFFB:0838	UART2_BLR	UART2 BOF control register	8	R/W	40h
0x00 840Fh	FFFB:083C	UART2_ACREG	UART2 auxiliary control register	8	R/W	00h
0x00 8410h	FFFB:0840	UART2_SCR	UART2 supplementary control register	8	R/W	00h
0x00 8411h	FFFB:0844	UART2_SSR	UART2 supplementary status register	8	R	00h
0x00 8412h	FFFB:0848	UART2_EBLR	UART2 BOF length register	8	R/W	00h
0x00 8413h	FFFB:084C		Reserved			
0x00 8414h	FFFB:0850	UART2_MVR	UART2 module version register	8	R	−
0x00 8415h	FFFB:0854	UART2_SYSC	UART2 system configuration register	8	R/W	00h
0x00 8416h	FFFB:0858	UART2_SYSS	UART2 system status register	8	R/W	00h
0x00 8417h	FFFB:085C	UART2_WER	UART2 wake-up enable register	8	R/W	7Fh

Table 3−28. SPI1 Registers

DSP WORD ADDRESS	BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 8600h	FFFB:0C00	SPI1_REV	Module Version Register	32	R	0000 00XXh
0x00 8602h − 0x00 8607h	FFFB:0C04 − FFFB:0C0F		Reserved			
0x00 8608h	FFFB:0C10	SPI1_SCR	System Configuration Register	32	R/W	0000 0020h
0x00 860Ah	FFFB:0C14	SPI1_SSR	System Status Register	32	R	0000 0000h
0x00 860Ch	FFFB:0C18	SPI1_ISR	Interrupt Status Register	32	R/W	0000 0000h
0x00 860Eh	FFFB:0C1C	SPI1_IER	Interrupt Enable Register	32	R/W	0000 0000h
0x00 8610h	FFFB:0C20		Reserved			
0x00 8612h	FFFB:0C24	SPI1_SET1	Setup 1 Register	32	R/W	0000 0000h
0x00 8614h	FFFB:0C28	SPI1_SET2	Setup 2 Register	32	R/W	0000 0000h
0x00 8616h	FFFB:0C2C	SPI1_CTRL	Control Register	32	R/W	0000 0000h
0x00 8618h	FFFB:0C30	SPI1_DSR	Data Status Register	32	R	0000 0002h
0x00 861Ah	FFFB:0C34	SPI1_TX	Transmit Register	32	R/W	0000 0000h
0x00 861Ch	FFFB:0C38	SPI1_RX	Receive Register	32	R	0000 0000h
0x00 861Eh	FFFB:0C3C	SPI1_TEST	Test Register	32	R/W	0000 0000h

Table 3−29. McBSP2 Registers

DSP WORD ADDRESS	MPU BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 8800h	FFFB:1000	MCBSP2_DRR2	McBSP2 Data receive register 2	16	R/W	0000h
0x00 8801h	FFFB:1002	MCBSP2_DRR1	McBSP2 Data receive register 1	16	R/W	0000h
0x00 8802h	FFFB:1004	MCBSP2_DXR2	McBSP2 Data transmit register 2	16	R/W	0000h
0x00 8803h	FFFB:1006	MCBSP2_DXR1	McBSP2 Data transmit register 1	16	R/W	0000h
0x00 8804h	FFFB:1008	MCBSP2_SPCR2	McBSP2 Serial port control register 2	16	R/W	0000h
0x00 8805h	FFFB:100A	MCBSP2_SPCR1	McBSP2 Serial port control register 1	16	R/W	0000h
0x00 8806h	FFFB:100C	MCBSP2_RCR2	McBSP2 Receive control register 2	16	R//W	0000h
0x00 8807h	FFFB:100E	MCBSP2_RCR1	McBSP2 Receive control register 1	16	R/W	0000h
0x00 8808h	FFFB:1010	MCBSP2_XCR2	McBSP2 Transmit control register 2	16	R/W	0000h
0x00 8809h	FFFB:1012	MCBSP2_XCR1	McBSP2 Transmit control register 1	16	R/W	0000h
0x00 880Ah	FFFB:1014	MCBSP2_SRGR2	McBSP2 Sample rate generator register 2	16	R/W	2000h
0x00 880Bh	FFFB:1016	MCBSP2_SRGR1	McBSP2 Sample rate generator register 1	16	R/W	0001h
0x00 880Ch	FFFB:1018	MCBSP2_MCR2	McBSP2 Multichannel register 2	16	R/W	0000h
0x00 880Dh	FFFB:101A	MCBSP2_MCR1	McBSP2 Multichannel register 1	16	R/W	0000h
0x00 880Eh	FFFB:101C	MCBSP2_RCERA	McBSP2 Receive channel enable register partition A	16	R/W	0000h
0x00 880Fh	FFFB:101E	MCBSP2_RCERB	McBSP2 Receive channel enable register partition B	16	R/W	0000h
0x00 8810h	FFFB:1020	MCBSP2_XCERA	McBSP2 Transmit channel enable register partition A	16	R/W	0000h
0x00 8811h	FFFB:1022	MCBSP2_XCERB	McBSP2 Transmit channel enable register partition B	16	R/W	0000h
0x00 8812h	FFFB:1024	MCBSP2_PCR0	McBSP2 Pin control register 0	16	R/W	0000h
0x00 8813h	FFFB:1026	MCBSP2_RCERC	McBSP2 Receive channel enable register partition C	16	R/W	0000h
0x00 8814h	FFFB:1028	MCBSP2_RCERD	McBSP2 Receive channel enable register partition D	16	R/W	0000h
0x00 8815h	FFFB:102A	MCBSP2_XCERC	McBSP2 Transmit channel enable register partition C	16	R/W	0000h
0x00 8816h	FFFB:102C	MCBSP2_XCERD	McBSP2 Transmit channel enable register partition D	16	R/W	0000h
0x00 8817h	FFFB:102E	MCBSP2_RCERE	McBSP2 Receive channel enable register partition E	16	R/W	0000h
0x00 8818h	FFFB:1030	MCBSP2_RCERF	McBSP2 Receive channel enable register partition F	16	R/W	0000h
0x00 8819h	FFFB:1032	MCBSP2_XCERE	McBSP2 Transmit channel enable register partition E	16	R/W	0000h
0x00 881Ah	FFFB:1034	MCBSP2_XCERF	McBSP2 Transmit channel enable register partition F	16	R/W	0000h
0x00 881Bh	FFFB:1036	MCBSP2_RCERG	McBSP2 Receive channel enable register partition G	16	R/W	0000h
0x00 881Ch	FFFB:1038	MCBSP2_RCERH	McBSP2 Receive channel enable register partition H	16	R/W	0000h
0x00 881Dh	FFFB:103A	MCBSP2_XCERG	McBSP2 Transmit channel enable register partition G	16	R/W	0000h
0x00 881Eh	FFFB:103C	MCBSP2_XCERH	McBSP2 Transmit channel enable register partition H	16	R/W	0000h
0x00 881Fh	FFFB:103E	MCBSP2_REV	McBSP2 Version register	16	R/W	0011h

Table 3−30. General-Purpose Timer1 Registers

DSP WORD ADDRESS	MPU BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 8A00h	FFFB:1400	GPTMR1_TIDR	GPTimer1 Identification Register	16/32	R	0000 0010h
0x00 8A02h	FFFB:1404		Reserved			
0x00 8A08h	FFFB:1410	GPTMR1_TIOCP_CFG	GPTimer1 OCP Configuration Register	16/32	R/W	0000 0000h
0x00 8A0Ah	FFFB:1414	GPTMR1_TISTAT	GPTimer1 System Status Register	16/32	R	0000 0000h
0x00 8A0Ch	FFFB:1418	GPTMR1_TISR	GPTimer1 Status Register	16/32	R/W	0000 0000h
0x00 8A0Eh	FFFB:141C	GPTMR1_TIER	GPTimer1 Interrupt Enable Register	16/32	R/W	0000 0000h
0x00 8A10h	FFFB:1420	GPTMR1_TWER	GPTimer1 Wake Up Enable Register	16/32	R/W	0000 0000h
0x00 8A12h	FFFB:1424	GPTMR1_TCLR	GPTimer1 Control Register	16/32	R/W	0000 0000h
0x00 8A14h	FFFB:1428	GPTMR1_TCRR	GPTimer1 Counter Register	16/32	R/W	0000 0000h
0x00 8A16h	FFFB:142C	GPTMR1_TLDR	GPTimer1 Load Register	16/32	R/W	0000 0000h
0x00 8A18h	FFFB:1430	GPTMR1_TTGR	GPTimer1 Trigger Register	16/32	R/W	FFFF FFFFh
0x00 8A1Ah	FFFB:1434	GPTMR1_TWPS	GPTimer1 Write Posted Register	16/32	R	0000 0000h
0x00 8A1Ch	FFFB:1438	GPTMR1_TMAR	GPTimer1 Match Register	16/32	R/W	0000 0000h
0x00 8A20h	FFFB:1440	GPTMR1_TSICR	GPTimer1 Synchronization Interface Control Register	16/32	R/W	0000 0004h

Table 3−31. General-Purpose Timer2 Registers

DSP WORD ADDRESS	MPU BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 8E00h	FFFB:1C00	GPTMR2_TIDR	GPTimer2 Identification Register	16/32	R	0000 0010h
0x00 8E02h	FFFB:1C04		Reserved			
0x00 8E08h	FFFB:1C10	GPTMR2_TIOCP_CFG	GPTimer2 OCP Configuration Register	16/32	R/W	0000 0000h
0x00 8E0Ah	FFFB:1C14	GPTMR2_TISTAT	GPTimer2 System Status Register	16/32	R	0000 0000h
0x00 8E0Ch	FFFB:1C18	GPTMR2_TISR	GPTimer2 Status Register	16/32	R/W	0000 0000h
0x00 8E0Eh	FFFB:1C1C	GPTMR2_TIER	GPTimer2 Interrupt Enable Register	16/32	R/W	0000 0000h
0x00 8E10h	FFFB:1C20	GPTMR2_TWER	GPTimer2 Wake Up Enable Register	16/32	R/W	0000 0000h
0x00 8E12h	FFFB:1C24	GPTMR2_TCLR	GPTimer2 Control Register	16/32	R/W	0000 0000h
0x00 8E14h	FFFB:1C28	GPTMR2_TCRR	GPTimer2 Counter Register	16/32	R/W	0000 0000h
0x00 8E16h	FFFB:1C2C	GPTMR2_TLDR	GPTimer2 Load Register	16/32	R/W	0000 0000h
0x00 8E18h	FFFB:1C30	GPTMR2_TTGR	GPTimer2 Trigger Register	16/32	R/W	FFFF FFFFh
0x00 8E1Ah	FFFB:1C34	GPTMR2_TWPS	GPTimer2 Write Posted Register	16/32	R	0000 0000h
0x00 8E1Ch	FFFB:1C38	GPTMR2_TMAR	GPTimer2 Match Register	16/32	R/W	0000 0000h
0x00 8E20h	FFFB:1C40	GPTMR2_TSICR	GPTimer2 Synchronization Interface Control Register	16/32	R/W	0000 0004h

Table 3−32. General-Purpose Timer3 Registers

DSP WORD ADDRESS	MPU BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 9200h	FFFB:2400	GPTMR3_TIDR	GPTimer3 Identification Register	16/32	R	0000 0010h
0x00 9202h	FFFB:2404		Reserved			
0x00 9208h	FFFB:2410	GPTMR3_TIOCP_CFG	GPTimer3 OCP Configuration Register	16/32	R/W	0000 0000h
0x00 920Ah	FFFB:2414	GPTMR3_TISTAT	GPTimer3 System Status Register	16/32	R	0000 0000h
0x00 920Ch	FFFB:2418	GPTMR3_TISR	GPTimer3 Status Register	16/32	R/W	0000 0000h
0x00 920Eh	FFFB:241C	GPTMR3_TIER	GPTimer3 Interrupt Enable Register	16/32	R/W	0000 0000h
0x00 9210h	FFFB:2420	GPTMR3_TWER	GPTimer3 Wake Up Enable Register	16/32	R/W	0000 0000h
0x00 9212h	FFFB:2424	GPTMR3_TCLR	GPTimer3 Control Register	16/32	R/W	0000 0000h
0x00 9214h	FFFB:2428	GPTMR3_TCRR	GPTimer3 Counter Register	16/32	R/W	0000 0000h
0x00 9216h	FFFB:242C	GPTMR3_TLDR	GPTimer3 Load Register	16/32	R/W	0000 0000h
0x00 9218h	FFFB:2430	GPTMR3_TTGR	GPTimer3 Trigger Register	16/32	R/W	FFFF FFFFh
0x00 921Ah	FFFB:2434	GPTMR3_TWPS	GPTimer3 Write Posted Register	16/32	R	0000 0000h
0x00 921Ch	FFFB:2438	GPTMR3_TMAR	GPTimer3 Match Register	16/32	R/W	0000 0000h
0x00 9220h	FFFB:2440	GPTMR3_TSICR	GPTimer3 Synchronization Interface Control Register	16/32	R/W	0000 0004h

Table 3−33. General-Purpose Timer4 Registers

DSP WORD ADDRESS	MPU BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 9600h	FFFB:2C00	GPTMR4_TIDR	GPTimer4 Identification Register	16/32	R	0000 0010h
0x00 9602h	FFFB:2C04		Reserved			
0x00 9608h	FFFB:2C10	GPTMR4_TIOCP_CFG	GPTimer4 OCP Configuration Register	16/32	R/W	0000 0000h
0x00 960Ah	FFFB:2C14	GPTMR4_TISTAT	GPTimer4 System Status Register	16/32	R	0000 0000h
0x00 960Ch	FFFB:2C18	GPTMR4_TISR	GPTimer4 Status Register	16/32	R/W	0000 0000h
0x00 960Eh	FFFB:2C1C	GPTMR4_TIER	GPTimer4 Interrupt Enable Register	16/32	R/W	0000 0000h
0x00 9610h	FFFB:2C20	GPTMR4_TWER	GPTimer4 Wake Up Enable Register	16/32	R/W	0000 0000h
0x00 9612h	FFFB:2C24	GPTMR4_TCLR	GPTimer4 Control Register	16/32	R/W	0000 0000h
0x00 9614h	FFFB:2C28	GPTMR4_TCRR	GPTimer4 Counter Register	16/32	R/W	0000 0000h
0x00 9616h	FFFB:2C2C	GPTMR4_TLDR	GPTimer4 Load Register	16/32	R/W	0000 0000h
0x00 9618h	FFFB:2C30	GPTMR4_TTGR	GPTimer4 Trigger Register	16/32	R/W	FFFF FFFFh
0x00 961Ah	FFFB:2C34	GPTMR4_TWPS	GPTimer4 Write Posted Register	16/32	R	0000 0000h
0x00 961Ch	FFFB:2C38	GPTMR4_TMAR	GPTimer4 Match Register	16/32	R/W	0000 0000h
0x00 9620h	FFFB:2C40	GPTMR4_TSICR	GPTimer4 Synchronization Interface Control Register	16/32	R/W	0000 0004h

Table 3−34. General-Purpose Timer5 Registers

DSP WORD ADDRESS	MPU BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 9A00h	FFFB:3400	GPTMR5_TIDR	GPTimer5 Identification Register	16/32	R	0000 0010h
0x00 9A02h	FFFB:3404		Reserved			
0x00 9A08h	FFFB:3410	GPTMR5_TIOCP_CFG	GPTimer5 OCP Configuration Register	16/32	R/W	0000 0000h
0x00 9A0Ah	FFFB:3414	GPTMR5_TISTAT	GPTimer5 System Status Register	16/32	R	0000 0000h
0x00 9A0Ch	FFFB:3418	GPTMR5_TISR	GPTimer5 Status Register	16/32	R/W	0000 0000h
0x00 9A0Eh	FFFB:341C	GPTMR5_TIER	GPTimer5 Interrupt Enable Register	16/32	R/W	0000 0000h
0x00 9A10h	FFFB:3420	GPTMR5_TWER	GPTimer5 Wake Up Enable Register	16/32	R/W	0000 0000h
0x00 9A12h	FFFB:3424	GPTMR5_TCLR	GPTimer5 Control Register	16/32	R/W	0000 0000h
0x00 9A14h	FFFB:3428	GPTMR5_TCRR	GPTimer5 Counter Register	16/32	R/W	0000 0000h
0x00 9A16h	FFFB:342C	GPTMR5_TLDR	GPTimer5 Load Register	16/32	R/W	0000 0000h
0x00 9A18h	FFFB:3430	GPTMR5_TTGR	GPTimer5 Trigger Register	16/32	R/W	FFFF FFFFh
0x00 9A1Ah	FFFB:3434	GPTMR5_TWPS	GPTimer5 Write Posted Register	16/32	R	0000 0000h
0x00 9A1Ch	FFFB:3438	GPTMR5_TMAR	GPTimer5 Match Register	16/32	R/W	0000 0000h
0x00 9A20h	FFFB:3440	GPTMR5_TSICR	GPTimer5 Synchronization Interface Control Register	16/32	R/W	0000 0004h

Table 3−35. I^2C1 Registers

DSP WORD ADDRESS	MPU BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 9C00h	FFFB:3800	I2C1_REV	I^2C1 Module Version Register	16	R/W	0022h
0x00 9C02h	FFFB:3804	I2C1_IE	I^2C1 Interrupt Enable Register	16	R/W	0000h
0x00 9C04h	FFFB:3808	I2C1_STAT	I^2C1 Status Register	16	R	0000h
0x00 9C06h	FFFB:380C		Reserved			
0x00 9C08h	FFFB:3810	I2C1_SYSS	I^2C1 System Status Register	16	R	0000h
0x00 9C0Ah	FFFB:3814	I2C1_BUF	I^2C1 Buffer Configuration Register	16	R/W	0000h
0x00 9C0Ch	FFFB:3818	I2C1_CNT	I^2C1 Data Counter Register	16	R/W	0000h
0x00 9C0Eh	FFFB:381C	I2C1_DATA	I^2C1 Data Access Register	16	R/W	0000h
0x00 9C10h	FFFB:3820	I2C1_SYSC	I^2C1 System Configuration Register	16	R/W	0000h
0x00 9C12h	FFFB:3824	I2C1_CON	I^2C1 Configuration Register	16	R/W	0000h
0x00 9C14h	FFFB:3828	I2C1_OA	I^2C1 Own Address Register	16	R/W	0000h
0x00 9C16h	FFFB:382C	I2C1_SA	I^2C1 Slave Address Register	16	R/W	03FFh
0x00 9C18h	FFFB:3830	I2C1_PSC	I^2C1 Clock Prescaler Register	16	R/W	0000h
0x00 9C1Ah	FFFB:3834	I2C1_SCLL	I^2C1 SCL Low Timer Register	16	R/W	0000h
0x00 9C1Ch	FFFB:3838	I2C1_SCLH	I^2C1 SCL High Timer Register	16	R/W	0000h
0x00 9C1Eh	FFFB:383C	I2C1_SYSTEST	I^2C1 System Test Register	16	R/W	0000h

Table 3−36. General-Purpose Timer6 Registers

DSP WORD ADDRESS	MPU BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 9E00h	FFFB:3C00	GPTMR6_TIDR	GPTimer6 Identification Register	16/32	R	0000 0010h
0x00 9E02h	FFFB:3C04		Reserved			
0x00 9E08h	FFFB:3C10	GPTMR6_TIOCP_CFG	GPTimer6 OCP Configuration Register	16/32	R/W	0000 0000h
0x00 9E0Ah	FFFB:3C14	GPTMR6_TISTAT	GPTimer6 System Status Register	16/32	R	0000 0000h
0x00 9E0Ch	FFFB:3C18	GPTMR6_TISR	GPTimer6 Status Register	16/32	R/W	0000 0000h
0x00 9E0Eh	FFFB:3C1C	GPTMR6_TIER	GPTimer6 Interrupt Enable Register	16/32	R/W	0000 0000h
0x00 9E10h	FFFB:3C20	GPTMR6_TWER	GPTimer6 Wake Up Enable Register	16/32	R/W	0000 0000h
0x00 9E12h	FFFB:3C24	GPTMR6_TCLR	GPTimer6 Control Register	16/32	R/W	0000 0000h
0x00 9E14h	FFFB:3C28	GPTMR6_TCRR	GPTimer6 Counter Register	16/32	R/W	0000 0000h
0x00 9E16h	FFFB:3C2C	GPTMR6_TLDR	GPTimer6 Load Register	16/32	R/W	0000 0000h
0x00 9E18h	FFFB:3C30	GPTMR6_TTGR	GPTimer6 Trigger Register	16/32	R/W	FFFF FFFFh
0x00 9E1Ah	FFFB:3C34	GPTMR6_TWPS	GPTimer6 Write Posted Register	16/32	R	0000 0000h
0x00 9E1Ch	FFFB:3C38	GPTMR6_TMAR	GPTimer6 Match Register	16/32	R/W	0000 0000h
0x00 9E20h	FFFB:3C40	GPTMR6_TSICR	GPTimer6 Synchronization Interface Control Register	16/32	R/W	0000 0004h

Table 3−37. General-Purpose Timer7 Registers

DSP WORD ADDRESS	BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 BA00h	FFFB:7400	GPTMR7_TIDR	GPTimer7 Identification Register	16/32	R	0000 0010h
0x00 BA02h	FFFB:7404		Reserved			
0x00 BA08h	FFFB:7410	GPTMR7_TIOCP_CFG	GPTimer7 OCP Configuration Register	16/32	R/W	0000 0000h
0x00 BA0Ah	FFFB:7414	GPTMR7_TISTAT	GPTimer7 System Status Register	16/32	R	0000 0000h
0x00 BA0Ch	FFFB:7418	GPTMR7_TISR	GPTimer7 Status Register	16/32	R/W	0000 0000h
0x00 BA0Eh	FFFB:741C	GPTMR7_TIER	GPTimer7 Interrupt Enable Register	16/32	R/W	0000 0000h
0x00 BA10h	FFFB:7420	GPTMR7_TWER	GPTimer7 Wake Up Enable Register	16/32	R/W	0000 0000h
0x00 BA12h	FFFB:7424	GPTMR7_TCLR	GPTimer7 Control Register	16/32	R/W	0000 0000h
0x00 BA14h	FFFB:7428	GPTMR7_TCRR	GPTimer7 Counter Register	16/32	R/W	0000 0000h
0x00 BA16h	FFFB:742C	GPTMR7_TLDR	GPTimer7 Load Register	16/32	R/W	0000 0000h
0x00 BA18h	FFFB:7430	GPTMR7_TTGR	GPTimer7 Trigger Register	16/32	R/W	FFFF FFFFh
0x00 BA1Ah	FFFB:7434	GPTMR7_TWPS	GPTimer7 Write Posted Register	16/32	R	0000 0000h
0x00 BA1Ch	FFFB:7438	GPTMR7_TMAR	GPTimer7 Match Register	16/32	R/W	0000 0000h
0x00 BA20h	FFFB:7440	GPTMR7_TSICR	GPTimer7 Synchronization Interface Control Register	16/32	R/W	0000 0004h

Table 3−38. MMC/SDIO2 Registers

DSP WORD ADDRESS	MPU BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 BE00h	FFFB:7C00	MMC2_CMD	MMC2 Command Register	16	R/W	0000h
0x00 BE02h	FFFB:7C04	MMC2_ARGL	MMC2 Argument Register Low	16	R/W	0000h
0x00 BE04h	FFFB:7C08	MMC2_ARGH	MMC2 Argument Register High	16	R/W	0000h
0x00 BE06h	FFFB:7C0C	MMC2_CON	MMC2 Module Configuration Register	16	R/W	0000h
0x00 BE08h	FFFB:7C10	MMC2_STAT	MMC2 Module Status Register	16	R/W	0000h
0x00 BE0Ah	FFFB:7C14	MMC2_IE	MMC2 System Interrupt Enable Register	16	R/W	0000h
0x00 BE0Ch	FFFB:7C18	MMC2_CTO	MMC2 Command Time-Out Register	16	R/W	0000h
0x00 BE0Eh	FFFB:7C1C	MMC2_DTO	MMC2 Data Read Time-Out Register	16	R/W	0000h
0x00 BE10h	FFFB:7C20	MMC2_DATA	MMC2 Data Access Register	16	R/W	0000h
0x00 BE12h	FFFB:7C24	MMC2_BLEN	MMC2 Block Length Register	16	R/W	0000h
0x00 BE14h	FFFB:7C28	MMC2_NBLK	MMC2 Numberf of Blocks Register	16	R/W	0000h
0x00 BE16h	FFFB:7C2C	MMC2_BUF	MMC2 Buffer Configuration Register	16	R/W	0000h
0x00 BE18h	FFFB:7C30		Reserved			
0x00 BE1Ah	FFFB:7C34	MMC2_SDIO	MMC2 SDIO Configuration Register	16	R/W	0000h
0x00 BE1Ch	FFFB:7C38	MMC2_SYST	MMC2 System Test Register	16	R/W	0000h
0x00 BE1Eh	FFFB:7C3C	MMC2_REV	MMC2 Module Revision Register	16	R	undefined
0x00 BE20h	FFFB:7C40	MMC2_RSP0	MMC2 Command Response Register 0	16	R	0000h
0x00 BE22h	FFFB:7C44	MMC2_RSP1	MMC2 Command Response Register 1	16	R	0000h
0x00 BE24h	FFFB:7C48	MMC2_RSP2	MMC2 Command Response Register 2	16	R	0000h
0x00 BE26h	FFFB:7C4C	MMC2_RSP3	MMC2 Command Response Register 3	16	R	0000h
0x00 BE28h	FFFB:7C50	MMC2_RSP4	MMC2 Command Response Register 4	16	R	0000h
0x00 BE2Ah	FFFB:7C54	MMC2_RSP5	MMC2 Command Response Register 5	16	R	0000h
0x00 BE2Ch	FFFB:7C58	MMC2_RSP6	MMC2 Command Response Register 6	16	R	0000h
0x00 BE2Eh	FFFB:7C5C	MMC2_RSP7	MMC2 Command Response Register 7	16	R	0000h
0x00 BE30h	FFFB:7C60	MMC2_IOSR	MMC2 Command Response IOSR Register	16	R/W	0000h
0x00 BE32h	FFFB:7C64	MMC2_SYSC	MMC2 System Control Register	16	R/W	0000h
0x00 BE34h	FFFB:7C68	MMC2_SYSS	MMC2 System Status Register	16	R	0000h

Table 3−39. UART3 Registers

DSP WORD ADDRESS	MPU BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 CC00h	FFFB:9800	UART3_RHR	UART3 receive holding register	8	R	Undefined
0x00 CC00h	FFFB:9800	UART3_THR	UART3 transmit holding register	8	W	Undefined
0x00 CC00h	FFFB:9800	UART3_DLL	UART3 divisor latch low register	8	R/W	00h
0x00 CC01h	FFFB:9804	UART3_IER	UART3 interrupt enable register	8	R/W	00h
0x00 CC01h	FFFB:9804	UART3_DLH	UART3 divisor latch high register	8	R/W	00h
0x00 CC02h	FFFB:9808	UART3_IIR	UART3 interrupt identification register	8	R	01h
0x00 CC02h	FFFB:9808	UART3_FCR	UART3 FIFO control register	8	W	00h
0x00 CC02h	FFFB:9808	UART3_EFR	UART3 enhanced feature register	8	R/W	00h
0x00 CC03h	FFFB:980C	UART3_LCR	UART3 line control register	8	R/W	00h
0x00 CC04h	FFFB:9810	UART3_MCR	UART3 modem control register	8	R/W	00h
0x00 CC04h	FFFB:9810	UART1_XON1	UART3 XON1 register	8	R/W	00h
0x00 CC05h	FFFB:9814	UART3_LSR	UART3 mode register	8	R	60h
0x00 CC05h	FFFB:9814	UART3_XON2	UART3 XON2 register	8	R/W	00h
0x00 CC06h	FFFB:9818	UART3_MSR	UART3 modem status register	8	R	Undefined
0x00 CC06h	FFFB:9818	UART3_TCR	UART3 transmission control register	8	R/W	0Fh
0x00 CC06h	FFFB:9818	UART3_XOFF1	UART3 XOFF1 register	8	R/W	00h
0x00 CC07h	FFFB:981C	UART3_SPR	UART3 scratchpad register	8	R/W	00h
0x00 CC07h	FFFB:981C	UART3_TLR	UART3 trigger level register	8	R/W	00h
0x00 CC07h	FFFB:981C	UART3_XOFF2	UART3 XOFF2 register	8	R/W	00h
0x00 CC08h	FFFB:9820	UART3_MDR1	UART3 mode definition 1 register	8	R/W	07h
0x00 CC09h	FFFB:9824	UART3_MDR2	UART3 mode definition register 2	8	R/W	00h
0x00 CC0Ah	FFFB:9828	UART3_SFLSR	UART3 status FIFO line status register	8	R	00h
0x00 CC0Ah	FFFB:9828	UART3_TXFLL	UART3 transmit frame length low	8	W	00h
0x00 CC0Bh	FFFB:982C	UART3_RESUME	UART3 resume register	8	R	00h
0x00 CC0Bh	FFFB:982C	UART3_TXFLH	UART3 transmit frame length high	8	W	00h
0x00 CC0Ch	FFFB:9830	UART3_SFREGL	UART3 status FIFO low register	8	R	Undefined
0x00 CC0Ch	FFFB:9830	UART3_RXFLL	UART3 receive frame length low	8	W	00h
0x00 CC0Dh	FFFB:9834	UART3_SFREGH	UART3 status FIFO high register	8	R	Undefined
0x00 CC0Dh	FFFB:9834	UART3_RXFLH	UART3 receive frame length high	8	W	00h
0x00 CC0Eh	FFFB:9838	UART3_UASR	UART3 autobauding status register	8	R	00h
0x00 CC0Eh	FFFB:9838	UART3_BLR	UART3 BOF control register	8	R/W	40h
0x00 CC0Fh	FFFB:983C	UART3_ACREG	UART3 auxiliary control register	8	R/W	00h
0x00 CC10h	FFFB:9840	UART3_SCR	UART3 supplementary control register	8	R/W	00h
0x00 CC11h	FFFB:9844	UART3_SSR	UART3 supplementary status register	8	R	00h
0x00 CC12h	FFFB:9848	UART3_EBLR	UART3 BOF length register	8	R/W	00h
0x00 CC13h	FFFB:984C		Reserved			
0x00 CC14h	FFFB:9850	UART3_MVR	UART3 module version register	8	R	−
0x00 CC15h	FFFB:9854	UART3_SYSC	UART3 system configuration register	8	R/W	00h
0x00 CC16h	FFFB:9858	UART3_SYSS	UART3 system status register	8	R/W	00h
0x00 CC17h	FFFB:985C	UART3_WER	UART3 wake-up enable register	8	R/W	7Fh

Table 3−40. MPU GPIO3 Registers

DSP WORD ADDRESS	MPU BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 DA00h	FFFB:B400	GPIO3_REVISION	GPIO3 Revision Register	16/32	R	0000 00xxh
0x00 DA08h	FFFB:B410	GPIO3_SYSCONFIG	GPIO3 System Configuration Register	16/32	R/W	0000 0000h
0x00 DA0Ah	FFFB:B414	GPIO3_SYSSTATUS	GPIO3 System Status Register	16/32	R	0000 0000h
0x00 DA0Ch	FFFB:B418	GPIO3_IRQSTATUS1	GPIO3 Interrupt Status1 Register	16/32	R/W	0000 0000h
0x00 DA0Eh	FFFB:B41C	GPIO3_IRQENABLE1	GPIO3 Interrupt Enable1 Register	16/32	R/W	0000 0000h
0x00 DA10h	FFFB:B420	GPIO3_IRQSTATUS2	GPIO3 Interrupt Status2 Register	16/32	R/W	0000 0000h
0x00 DA12h	FFFB:B424	GPIO3_IRQENABLE2	GPIO3 Interrupt Enable2 Register	16/32	R/W	0000 0000h
0x00 DA14h	FFFB:B428	GPIO3_WAKEUPENABLE	GPIO3 Wake-up Enable Register	16/32	R/W	0000 0000h
0x00 DA16h	FFFB:B42C	GPIO3_DATAIN	GPIO3 Data Input Register	16/32	R	0000 0000h
0x00 DA18h	FFFB:B430	GPIO3_DATAOUT	GPIO3 Data Output Register	16/32	R/W	0000 0000h
0x00 DA1Ah	FFFB:B434	GPIO3_DIRECTION	GPIO3 Direction Control Register	16/32	R/W	0000 FFFFh
0x00 DA1Ch	FFFB:B438	GPIO3_EDGE_CTRL1	GPIO3 Edge Control 1 Register	16/32	R/W	0000 0000h
0x00 DA1Eh	FFFB:B43C	GPIO3_EDGE_CTRL2	GPIO3 Edge Control 2 Register	16/32	R/W	0000 0000h
0x00 DA4Eh	FFFB:B49C	GPIO3_CLEAR_IRQENABLE1	GPIO3 Clear Interrupt Enable1 Register	16/32	R/W	0000 0000h
0x00 DA52h	FFFB:B4A4	GPIO3_CLEAR_IRQENABLE2	GPIO3 Clear Interrupt Enable2 Register	16/32	R/W	0000 0000h
0x00 DA54h	FFFB:B4A8	GPIO3_CLEAR_WAKEUPENA	GPIO3 Clear Wake-up Enable Register	16/32	R/W	0000 0000h
0x00 DA58h	FFFB:B4B0	GPIO3_CLEAR_DATAOUT	GPIO3 Clear Data Output Register	16/32	R/W	0000 0000h
0x00 DA6Eh	FFFB:B4DC	GPIO3_SET_IRQENABLE1	GPIO3 Set Interrupt Enable1 Register	16/32	R/W	0000 0000h
0x00 DA72h	FFFB:B4E4	GPIO3_SET_IRQENABLE2	GPIO3 Set Interrupt Enable2 Register	16/32	R/W	0000 0000h
0x00 DA74h	FFFB:B4E8	GPIO3_SET_WAKEUPENA	GPIO3 Set Wake-up Enable Register	16/32	R/W	0000 0000h
0x00 DA78h	FFFB:B4F0	GPIO3_SET_DATAOUT	GPIO3 Set Data Output Register	16/32	R/W	0000 0000h

Table 3−41. MPU GPIO4 Registers

DSP WORD ADDRESS	MPU BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 DE00h	FFFB:BC00	GPIO4_REVISION	GPIO4 Revision Register	16/32	R	0000 00xxh
0x00 DE08h	FFFB:BC10	GPIO4_SYSCONFIG	GPIO4 System Configuration Register	16/32	R/W	0000 0000h
0x00 DE0Ah	FFFB:BC14	GPIO4_SYSSTATUS	GPIO4 System Status Register	16/32	R	0000 0000h
0x00 DE0Ch	FFFB:BC18	GPIO4_IRQSTATUS1	GPIO4 Interrupt Status1 Register	16/32	R/W	0000 0000h
0x00 DE0Eh	FFFB:BC1C	GPIO4_IRQENABLE1	GPIO4 Interrupt Enable1 Register	16/32	R/W	0000 0000h
0x00 DE10h	FFFB:BC20	GPIO4_IRQSTATUS2	GPIO4 Interrupt Status2 Register	16/32	R/W	0000 0000h
0x00 DE12h	FFFB:BC24	GPIO4_IRQENABLE2	GPIO4 Interrupt Enable2 Register	16/32	R/W	0000 0000h
0x00 DE14h	FFFB:BC28	GPIO4_WAKEUPENABLE	GPIO4 Wake-up Enable Register	16/32	R/W	0000 0000h
0x00 DE16h	FFFB:BC2C	GPIO4_DATAIN	GPIO4 Data Input Register	16/32	R	0000 0000h
0x00 DE18h	FFFB:BC30	GPIO4_DATAOUT	GPIO4 Data Output Register	16/32	R/W	0000 0000h
0x00 DE1Ah	FFFB:BC34	GPIO4_DIRECTION	GPIO4 Direction Control Register	16/32	R/W	0000 FFFFh
0x00 DE1Ch	FFFB:BC38	GPIO4_EDGE_CTRL1	GPIO4 Edge Control 1 Register	16/32	R/W	0000 0000h
0x00 DE1Eh	FFFB:BC3C	GPIO4_EDGE_CTRL2	GPIO4 Edge Control 2 Register	16/32	R/W	0000 0000h
0x00 DE4Eh	FFFB:BC9C	GPIO4_CLEAR_IRQENABLE1	GPIO4 Clear Interrupt Enable1 Register	16/32	R/W	0000 0000h
0x00 DE52h	FFFB:BCA4	GPIO4_CLEAR_IRQENABLE2	GPIO4 Clear Interrupt Enable2 Register	16/32	R/W	0000 0000h
0x00 DE54h	FFFB:BCA8	GPIO4_CLEAR_WAKEUPENA	GPIO4 Clear Wake-up Enable Register	16/32	R/W	0000 0000h
0x00 DE58h	FFFB:BCB0	GPIO4_CLEAR_DATAOUT	GPIO4 Clear Data Output Register	16/32	R/W	0000 0000h
0x00 DE6Eh	FFFB:BCDC	GPIO4_SET_IRQENABLE1	GPIO4 Set Interrupt Enable1 Register	16/32	R/W	0000 0000h
0x00 DE72h	FFFB:BCE4	GPIO4_SET_IRQENABLE2	GPIO4 Set Interrupt Enable2 Register	16/32	R/W	0000 0000h
0x00 DE74h	FFFB:BCE8	GPIO4_SET_WAKEUPENA	GPIO4 Set Wake-up Enable Register	16/32	R/W	0000 0000h
0x00 DE78h	FFFB:BCF0	GPIO4_SET_DATAOUT	GPIO4 Set Data Output Register	16/32	R/W	0000 0000h

Table 3−42. 32-kHz Synchro Count Registers

MPU BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFB:D400	32K_SYNC_CNT_REV	32k Synchro Count CID Revision Register	32	R	0000 0010h
FFFB:D410	32K_SYNC_CNT_CR	32k Synchro Count Counter Register	32	R	0000 0003h

Table 3−43. General-Purpose Timer8 Registers

DSP WORD ADDRESS	MPU BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 C200h	FFFB:D400	GPTMR8_TIDR	GPTimer8 Identification Register	16/32	R	0000 0010h
0x00 C202h	FFFB:D404		Reserved			
0x00 C208h	FFFB:D410	GPTMR8_TIOCP_CFG	GPTimer8 OCP Configuration Register	16/32	R/W	0000 0000h
0x00 C20Ah	FFFB:D414	GPTMR8_TISTAT	GPTimer8 System Status Register	16/32	R	0000 0000h
0x00 C20Ch	FFFB:D418	GPTMR8_TISR	GPTimer8 Status Register	16/32	R/W	0000 0000h
0x00 C20Eh	FFFB:D41C	GPTMR8_TIER	GPTimer8 Interrupt Enable Register	16/32	R/W	0000 0000h
0x00 C210h	FFFB:D420	GPTMR8_TWER	GPTimer8 Wake Up Enable Register	16/32	R/W	0000 0000h
0x00 C212h	FFFB:D424	GPTMR8_TCLR	GPTimer8 Control Register	16/32	R/W	0000 0000h
0x00 C214h	FFFB:D428	GPTMR8_TCRR	GPTimer8 Counter Register	16/32	R/W	0000 0000h
0x00 C216h	FFFB:D42C	GPTMR8_TLDR	GPTimer8 Load Register	16/32	R/W	0000 0000h
0x00 C218h	FFFB:D430	GPTMR8_TTGR	GPTimer8 Trigger Register	16/32	R/W	FFFF FFFFh
0x00 C21Ah	FFFB:D434	GPTMR8_TWPS	GPTimer8 Write Posted Register	16/32	R	0000 0000h
0x00 C21Ch	FFFB:D438	GPTMR8_TMAR	GPTimer8 Match Register	16/32	R/W	0000 0000h
0x00 C220h	FFFB:D440	GPTMR8_TSICR	GPTimer8 Synchronization Interface Control Register	16/32	R/W	0000 0004h

Table 3−44. MPU GPIO1 Registers

DSP WORD ADDRESS	MPU BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 F200h	FFFB:E400	GPIO1_REVISION	GPIO1 Revision Register	16/32	R	0000 00xxh
0x00 F208h	FFFB:E410	GPIO1_SYSCONFIG	GPIO1 System Configuration Register	16/32	R/W	0000 0000h
0x00 F20Ah	FFFB:E414	GPIO1_SYSSTATUS	GPIO1 System Status Register	16/32	R	0000 0000h
0x00 F20Ch	FFFB:E418	GPIO1_IRQSTATUS1	GPIO1 Interrupt Status1 Register	16/32	R/W	0000 0000h
0x00 F20Eh	FFFB:E41C	GPIO1_IRQENABLE1	GPIO1 Interrupt Enable1 Register	16/32	R/W	0000 0000h
0x00 F210h	FFFB:E420	GPIO1_IRQSTATUS2	GPIO1 Interrupt Status2 Register	16/32	R/W	0000 0000h
0x00 F212h	FFFB:E424	GPIO1_IRQENABLE2	GPIO1 Interrupt Enable2 Register	16/32	R/W	0000 0000h
0x00 F214h	FFFB:E428	GPIO1_WAKEUPENABLE	GPIO1 Wake-up Enable Register	16/32	R/W	0000 0000h
0x00 F216h	FFFB:E42C	GPIO1_DATAIN	GPIO1 Data Input Register	16/32	R	0000 0000h
0x00 F218h	FFFB:E430	GPIO1_DATAOUT	GPIO1 Data Output Register	16/32	R/W	0000 0000h
0x00 F21Ah	FFFB:E434	GPIO1_DIRECTION	GPIO1 Direction Control Register	16/32	R/W	0000 FFFFh
0x00 F21Ch	FFFB:E438	GPIO1_EDGE_CTRL1	GPIO1 Edge Control 1 Register	16/32	R/W	0000 0000h
0x00 F21Eh	FFFB:E43C	GPIO1_EDGE_CTRL2	GPIO1 Edge Control 2 Register	16/32	R/W	0000 0000h
0x00 F24Eh	FFFB:E49C	GPIO1_CLEAR_IRQENABLE1	GPIO1 Clear Interrupt Enable1 Register	16/32	R/W	0000 0000h
0x00 F252h	FFFB:E4A4	GPIO1_CLEAR_IRQENABLE2	GPIO1 Clear Interrupt Enable2 Register	16/32	R/W	0000 0000h
0x00 F254h	FFFB:E4A8	GPIO1_CLEAR_WAKEUPENA	GPIO1 Clear Wake-up Enable Register	16/32	R/W	0000 0000h
0x00 F258h	FFFB:E4B0	GPIO1_CLEAR_DATAOUT	GPIO1 Clear Data Output Register	16/32	R/W	0000 0000h
0x00 F26Eh	FFFB:E4DC	GPIO1_SET_IRQENABLE1	GPIO1 Set Interrupt Enable1 Register	16/32	R/W	0000 0000h
0x00 F272h	FFFB:E4E4	GPIO1_SET_IRQENABLE2	GPIO1 Set Interrupt Enable2 Register	16/32	R/W	0000 0000h
0x00 F274h	FFFB:E4E8	GPIO1_SET_WAKEUPENA	GPIO1 Set Wake-up Enable Register	16/32	R/W	0000 0000h
0x00 F278h	FFFB:E4F0	GPIO1_SET_DATAOUT	GPIO1 Set Data Output Register	16/32	R/W	0000 0000h

Table 3−45. MPU GPIO2 Registers

DSP WORD ADDRESS	MPU BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 F600h	FFFB:EC00	GPIO2_REVISION	GPIO2 Revision Register	16/32	R	0000 00xxh
0x00 F608h	FFFB:EC10	GPIO2_SYSCONFIG	GPIO2 System Configuration Register	16/32	R/W	0000 0000h
0x00 F60Ah	FFFB:EC14	GPIO2_SYSSTATUS	GPIO2 System Status Register	16/32	R	0000 0000h
0x00 F60Ch	FFFB:EC18	GPIO2_IRQSTATUS1	GPIO2 Interrupt Status1 Register	16/32	R/W	0000 0000h
0x00 F60Eh	FFFB:EC1C	GPIO2_IRQENABLE1	GPIO2 Interrupt Enable1 Register	16/32	R/W	0000 0000h
0x00 F610h	FFFB:EC20	GPIO2_IRQSTATUS2	GPIO2 Interrupt Status2 Register	16/32	R/W	0000 0000h
0x00 F612h	FFFB:EC24	GPIO2_IRQENABLE2	GPIO2 Interrupt Enable2 Register	16/32	R/W	0000 0000h
0x00 F614h	FFFB:EC28	GPIO2_WAKEUPENABLE	GPIO2 Wake-up Enable Register	16/32	R/W	0000 0000h
0x00 F616h	FFFB:EC2C	GPIO2_DATAIN	GPIO2 Data Input Register	16/32	R	0000 0000h
0x00 F618h	FFFB:EC30	GPIO2_DATAOUT	GPIO2 Data Output Register	16/32	R/W	0000 0000h
0x00 F61Ah	FFFB:EC34	GPIO2_DIRECTION	GPIO2 Direction Control Register	16/32	R/W	0000 FFFFh
0x00 F61Ch	FFFB:EC38	GPIO2_EDGE_CTRL1	GPIO2 Edge Control 1 Register	16/32	R/W	0000 0000h
0x00 F61Eh	FFFB:EC3C	GPIO2_EDGE_CTRL2	GPIO2 Edge Control 2 Register	16/32	R/W	0000 0000h
0x00 F64Eh	FFFB:EC9C	GPIO2_CLEAR_IRQENABLE1	GPIO2 Clear Interrupt Enable1 Register	16/32	R/W	0000 0000h
0x00 F652h	FFFB:ECA4	GPIO2_CLEAR_IRQENABLE2	GPIO2 Clear Interrupt Enable2 Register	16/32	R/W	0000 0000h
0x00 F654h	FFFB:ECA8	GPIO2_CLEAR_WAKEUPENA	GPIO2 Clear Wake-up Enable Register	16/32	R/W	0000 0000h
0x00 F658h	FFFB:ECB0	GPIO2_CLEAR_DATAOUT	GPIO2 Clear Data Output Register	16/32	R/W	0000 0000h
0x00 F66Eh	FFFB:ECDC	GPIO2_SET_IRQENABLE1	GPIO2 Set Interrupt Enable1 Register	16/32	R/W	0000 0000h
0x00 F672h	FFFB:ECE4	GPIO2_SET_IRQENABLE2	GPIO2 Set Interrupt Enable2 Register	16/32	R/W	0000 0000h
0x00 F674h	FFFB:ECE8	GPIO2_SET_WAKEUPENA	GPIO2 Set Wake-up Enable Register	16/32	R/W	0000 0000h
0x00 F678h	FFFB:ECF0	GPIO2_SET_DATAOUT	GPIO2 Set Data Output Register	16/32	R/W	0000 0000h

Table 3−46. MPU/DSP Shared Mailbox Registers

DSP WORD ADDRESS	MPU BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	MPU ACCESS TYPE	DSP ACCESS TYPE	RESET VALUE
0x00 F800h	FFFC:F000	ARM2DSP1	MPU to DSP 1 Data Register	16	R/W	R	0000h
0x00 F802h	FFFC:F004	ARM2DSP1B	MPU to DSP 1 Command Register	16	R/W	R	0000h
0x00 F804h	FFFC:F008	DSP2ARM1	DSP to MPU 1 Data Register	16	R	R/W	0000h
0x00 F806h	FFFC:F00C	DSP2ARM1B	DSP to MPU 1 Command Register	16	R	R/W	0000h
0x00 F808h	FFFC:F010	DSP2ARM2	DSP to MPU 2 Data Register	16	R	R/W	0000h
0x00 F80Ah	FFFC:F014	DSP2ARM2B	DSP to MPU 2 Command Register	16	R	R/W	0000h
0x00 F80Ch	FFFC:F018	ARM2DSP1_FLAG	MPU to DSP 1 Flag Register	16	R	R	undef
0x00 F80Eh	FFFC:F01C	DSP2ARM1_FLAG	DSP to MPU 1 Flag Register	16	R	R	undef
0x00 F810h	FFFC:F020	DSP2ARM2_FLAG	DSP to MPU 2 Flag Register	16	R	R	undef
0x00 F812h	FFFC:F024	ARM2DSP2	MPU to DSP 2 Data Register	16	R/W	R	0000h
0x00 F814h	FFFC:F028	ARM2DSP2B	MPU to DSP 2 Command Register	16	R/W	R	0000h
0x00 F816h	FFFC:F02C	ARM2DSP2_FLAG	MPU to DSP 2 Flag Register	16	R	R	undef

3.2.2.4 DSP Public Peripheral Registers (Accessible Via MPUI Port)

The MPU public peripheral registers include the following:

- McBSP1 Registers
- MCSI1 Registers
- MCSI2 Registers
- McBSP3 Registers

Table 3−47. McBSP1 Registers

DSP WORD ADDRESS	MPU BYTE ADDRESS (VIA MPUI)	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 8C00h	E101:1800	MCBSP1_DRR2	McBSP1 Data receive register 2	16	R/W	0000h
0x00 8C01h	E101:1802	MCBSP1_DRR1	McBSP1 Data receive register 1	16	R/W	0000h
0x00 8C02h	E101:1804	MCBSP1_DXR2	McBSP1 Data transmit register 2	16	R/W	0000h
0x00 8C03h	E101:1806	MCBSP1_DXR1	McBSP1 Data transmit register 1	16	R/W	0000h
0x00 8C04h	E101:1808	MCBSP1_SPCR2	McBSP1 Serial port control register 2	16	R/W	0000h
0x00 8C05h	E101:180A	MCBSP1_SPCR1	McBSP1 Serial port control register 1	16	R/W	0000h
0x00 8C06h	E101:180C	MCBSP1_RCR2	McBSP1 Receive control register 2	16	R//W	0000h
0x00 8C07h	E101:180E	MCBSP1_RCR1	McBSP1 Receive control register 1	16	R/W	0000h
0x00 8C08h	E101:1810	MCBSP1_XCR2	McBSP1 Transmit control register 2	16	R/W	0000h
0x00 8C09h	E101:1812	MCBSP1_XCR1	McBSP1 Transmit control register 1	16	R/W	0000h
0x00 8C0Ah	E101:1814	MCBSP1_SRGR2	McBSP1 Sample rate generator register 2	16	R/W	2000h
0x00 8C0Bh	E101:1816	MCBSP1_SRGR1	McBSP1 Sample rate generator register 1	16	R/W	0001h
0x00 8C0Ch	E101:1818	MCBSP1_MCR2	McBSP1 Multichannel register 2	16	R/W	0000h
0x00 8C0Dh	E101:181A	MCBSP1_MCR1	McBSP1 Multichannel register 1	16	R/W	0000h
0x00 8C0Eh	E101:181C	MCBSP1_RCERA	McBSP1 Receive channel enable register partition A	16	R/W	0000h
0x00 8C0Fh	E101:181E	MCBSP1_RCERB	McBSP1 Receive channel enable register partition B	16	R/W	0000h
0x00 8C10h	E101:1820	MCBSP1_XCERA	McBSP1 Transmit channel enable register partition A	16	R/W	0000h
0x00 8C11h	E101:1822	MCBSP1_XCERB	McBSP1 Transmit channel enable register partition B	16	R/W	0000h
0x00 8C12h	E101:1824	MCBSP1_PCR0	McBSP1 Pin control register 0	16	R/W	0000h
0x00 8C13h	E101:1826	MCBSP1_RCERC	McBSP1 Receive channel enable register partition C	16	R/W	0000h
0x00 8C14h	E101:1828	MCBSP1_RCERD	McBSP1 Receive channel enable register partition D	16	R/W	0000h
0x00 8C15h	E101:182A	MCBSP1_XCERC	McBSP1 Transmit channel enable register partition C	16	R/W	0000h
0x00 8C16h	E101:182C	MCBSP1_XCERD	McBSP1 Transmit channel enable register partition D	16	R/W	0000h
0x00 8C17h	E101:182E	MCBSP1_RCERE	McBSP1 Receive channel enable register partition E	16	R/W	0000h
0x00 8C18h	E101:1830	MCBSP1_RCERF	McBSP1 Receive channel enable register partition F	16	R/W	0000h
0x00 8C19h	E101:1832	MCBSP1_XCERE	McBSP1 Transmit channel enable register partition E	16	R/W	0000h

Table 3−47. McBSP1 Registers (Continued)

DSP WORD ADDRESS	MPU BYTE ADDRESS (VIA MPUI)	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 8C1Ah	E101:1834	MCBSP1_XCERF	McBSP1 Transmit channel enable register partition F	16	R/W	0000h
0x00 8C1Bh	E101:1836	MCBSP1_RCERG	McBSP1 Receive channel enable register partition G	16	R/W	0000h
0x00 8C1Ch	E101:1838	MCBSP1_RCERH	McBSP1 Receive channel enable register partition H	16	R/W	0000h
0x00 8C1Dh	E101:183A	MCBSP1_XCERG	McBSP1 Transmit channel enable register partition G	16	R/W	0000h
0x00 8C1Eh	E101:183C	MCBSP1_XCERH	McBSP1 Transmit channel enable register partition H	16	R/W	0000h
0x00 8C1Fh	E101:183E	MCBSP1_REV	McBSP1 Version register	16	R/W	0011h

Table 3−48. MCSI1 Registers

DSP WORD ADDRESS	MPU BYTE ADDRESS (VIA MPUI)	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 9400h	E101:2800	MCSI1_CONTROL_REG	MCSI1 control register	16	R/W	0000h
0x00 9401h	E101:2802	MCSI1_MAIN_PARAMETERS_REG	MCSI1 main parameters register	16	R/W	0000h
0x00 9402h	E101:2804	MCSI1_INTERRUPTS_REG	MCSI1 interrupts register	16	R/W	0000h
0x00 9403h	E101:2806	MCSI1_CHANNEL_USED_REG	MCSI1 channel used register	16	R/W	0000h
0x00 9404h	E101:2808	MCSI1_OVER_CLOCK_REG	MCSI1 over-clock register	16	R/W	0000h
0x00 9405h	E101:280A	MCSI1_CLOCK_FREQUENCY_ REG	MCSI1 clock frequency register	16	R/W	0000h
0x00 9406h	E101:280C	MCSI1_STATUS_REG	MCSI1 status register	16	R/W	0000h
0x00 9407h− 0x00 941Fh		Reserved				
0x00 9420h	E101:2840	MCSI1_TX0	MCSI1 transmit word register 0	16	R/W	Undefined
0x00 9421h	E101:2842	MCSI1_TX1	MCSI1 transmit word register 1	16	R/W	Undefined
0x00 9422h	E101:2844	MCSI1_TX2	MCSI1 transmit word register 2	16	R/W	Undefined
0x00 9423h	E101:2846	MCSI1_TX3	MCSI1 transmit word register 3	16	R/W	Undefined
0x00 9424h	E101:2848	MCSI1_TX4	MCSI1 transmit word register 4	16	R/W	Undefined
0x00 9425h	E101:284A	MCSI1_TX5	MCSI1 transmit word register 5	16	R/W	Undefined
0x00 9426h	E101:284C	MCSI1_TX6	MCSI1 transmit word register 6	16	R/W	Undefined
0x00 9427h	E101:284E	MCSI1_TX7	MCSI1 transmit word register 7	16	R/W	Undefined
0x00 9428h	E101:2850	MCSI1_TX8	MCSI1 transmit word register 8	16	R/W	Undefined
0x00 9429h	E101:2852	MCSI1_TX9	MCSI1 transmit word register 9	16	R/W	Undefined
0x00 942Ah	E101:2854	MCSI1_TX10	MCSI1 transmit word register 10	16	R/W	Undefined
0x00 942Bh	E101:2856	MCSI1_TX11	MCSI1 transmit word register 11	16	R/W	Undefined
0x00 942Ch	E101:2858	MCSI1_TX12	MCSI1 transmit word register 12	16	R/W	Undefined
0x00 942Dh	E101:285A	MCSI1_TX13	MCSI1 transmit word register 13	16	R/W	Undefined
0x00 942Eh	E101:285C	MCSI1_TX14	MCSI1 transmit word register 14	16	R/W	Undefined
0x00 942Fh	E101:285E	MCSI1_TX15	MCSI1 transmit word register 15	16	R/W	Undefined
0x00 9430h	E101:2860	MCSI1_RX0	MCSI1 receive word register 0	16	R	Undefined
0x00 9431h	E101:2862	MCSI1_RX1	MCSI1 receive word register 1	16	R	Undefined
0x00 9432h	E101:2864	MCSI1_RX2	MCSI1 receive word register 2	16	R	Undefined

Table 3−48. MCSI1 Registers (Continued)

DSP WORD ADDRESS	MPU BYTE ADDRESS (VIA MPUI)	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 9433h	E101:2866	MCSI1_RX3	MCSI1 receive word register 3	16	R	Undefined
0x00 9434h	E101:2868	MCSI1_RX4	MCSI1 receive word register 4	16	R	Undefined
0x00 9435h	E101:286A	MCSI1_RX5	MCSI1 receive word register 5	16	R	Undefined
0x00 9436h	E101:286C	MCSI1_RX6	MCSI1 receive word register 6	16	R	Undefined
0x00 9437h	E101:286E	MCSI1_RX7	MCSI1 receive word register 7	16	R	Undefined
0x00 9438h	E101:2870	MCSI1_RX8	MCSI1 receive word register 8	16	R	Undefined
0x00 9439h	E101:2872	MCSI1_RX9	MCSI1 receive word register 9	16	R	Undefined
0x00 943Ah	E101:2874	MCSI1_RX10	MCSI1 receive word register 10	16	R	Undefined
0x00 943Bh	E101:2876	MCSI1_RX11	MCSI1 receive word register 11	16	R	Undefined
0x00 943Ch	E101:2878	MCSI1_RX12	MCSI1 receive word register 12	16	R	Undefined
0x00 943Dh	E101:287A	MCSI1_RX13	MCSI1 receive word register 13	16	R	Undefined
0x00 943Eh	E101:287C	MCSI1_RX14	MCSI1 receive word register 14	16	R	Undefined
0x00 943Fh	E101:287E	MCSI1_RX15	MCSI1 receive word register 15	16	R	Undefined

Table 3−49. MCSI2 Registers

DSP WORD ADDRESS	MPU BYTE ADDRESS (VIA MPUI)	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 9000h	E101:2000	MCSI2_CONTROL_REG	MCSI2 control register	16	R/W	0000h
0x00 9001h	E101:2002	MCSI2_MAIN_PARAMETERS_REG	MCSI2 main parameters register	16	R/W	0000h
0x00 9002h	E101:2004	MCSI2_INTERRUPTS_REG	MCSI2 interrupts register	16	R/W	0000h
0x00 9003h	E101:2006	MCSI2_CHANNEL_USED_REG	MCSI2 channel used register	16	R/W	0000h
0x00 9004h	E101:2008	MCSI2_OVER_CLOCK_REG	MCSI2 over-clock register	16	R/W	0000h
0x00 9005h	E101:200A	MCSI2_CLOCK_FREQUENCY_ REG	MCSI2 clock frequency register	16	R/W	0000h
0x00 9006h	E101:200C	MCSI2_STATUS_REG	MCSI2 status register	16	R/W	0000h
0x00 9007h − 0x00 901Fh		Reserved				
0x00 9020h	E101:2040	MCSI2_TX0	MCSI2 transmit word register 0	16	R/W	Undefined
0x00 9021h	E101:2042	MCSI2_TX1	MCSI2 transmit word register 1	16	R/W	Undefined
0x00 9022h	E101:2044	MCSI2_TX2	MCSI2 transmit word register 2	16	R/W	Undefined
0x00 9023h	E101:2046	MCSI2_TX3	MCSI2 transmit word register 3	16	R/W	Undefined
0x00 9024h	E101:2048	MCSI2_TX4	MCSI2 transmit word register 4	16	R/W	Undefined
0x00 9025h	E101:204A	MCSI2_TX5	MCSI2 transmit word register 5	16	R/W	Undefined
0x00 9026h	E101:204C	MCSI2_TX6	MCSI2 transmit word register 6	16	R/W	Undefined
0x00 9027h	E101:204E	MCSI2_TX7	MCSI2 transmit word register 7	16	R/W	Undefined
0x00 9028h	E101:2050	MCSI2_TX8	MCSI2 transmit word register 8	16	R/W	Undefined
0x00 9029h	E101:2052	MCSI2_TX9	MCSI2 transmit word register 9	16	R/W	Undefined
0x00 902Ah	E101:2054	MCSI2_TX10	MCSI2 transmit word register 10	16	R/W	Undefined
0x00 902Bh	E101:2056	MCSI2_TX11	MCSI2 transmit word register 11	16	R/W	Undefined
0x00 902Ch	E101:2058	MCSI2_TX12	MCSI2 transmit word register 12	16	R/W	Undefined
0x00 902Dh	E101:205A	MCSI2_TX13	MCSI2 transmit word register 13	16	R/W	Undefined
0x00 902Eh	E101:205C	MCSI2_TX14	MCSI2 transmit word register 14	16	R/W	Undefined
0x00 902Fh	E101:205E	MCSI2_TX15	MCSI2 transmit word register 15	16	R/W	Undefined

Table 3−49. MCSI2 Registers (Continued)

DSP WORD ADDRESS	MPU BYTE ADDRESS (VIA MPUI)	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 9030h	E101:2060	MCSI2_RX0	MCSI2 receive word register 0	16	R	Undefined
0x00 9031h	E101:2062	MCSI2_RX1	MCSI2 receive word register 1	16	R	Undefined
0x00 9032h	E101:2064	MCSI2_RX2	MCSI2 receive word register 2	16	R	Undefined
0x00 9033h	E101:2066	MCSI2_RX3	MCSI2 receive word register 3	16	R	Undefined
0x00 9034h	E101:2068	MCSI2_RX4	MCSI2 receive word register 4	16	R	Undefined
0x00 9035h	E101:206A	MCSI2_RX5	MCSI2 receive word register 5	16	R	Undefined
0x00 9036h	E101:206C	MCSI2_RX6	MCSI2 receive word register 6	16	R	Undefined
0x00 9037h	E101:206E	MCSI2_RX7	MCSI2 receive word register 7	16	R	Undefined
0x00 9038h	E101:2070	MCSI2_RX8	MCSI2 receive word register 8	16	R	Undefined
0x00 9039h	E101:2072	MCSI2_RX9	MCSI2 receive word register 9	16	R	Undefined
0x00 903Ah	E101:2074	MCSI2_RX10	MCSI2 receive word register 10	16	R	Undefined
0x00 903Bh	E101:2076	MCSI2_RX11	MCSI2 receive word register 11	16	R	Undefined
0x00 903Ch	E101:2078	MCSI2_RX12	MCSI2 receive word register 12	16	R	Undefined
0x00 903Dh	E101:207A	MCSI2_RX13	MCSI2 receive word register 13	16	R	Undefined
0x00 903Eh	E101:207C	MCSI2_RX14	MCSI2 receive word register 14	16	R	Undefined
0x00 903Fh	E101:207E	MCSI2_RX15	MCSI2 receive word register 15	16	R	Undefined

Table 3−50. McBSP3 Registers

DSP WORD ADDRESS	MPU BYTE ADDRESS (VIA MPUI)	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 B800h	E101:7000	MCBSP3_DRR2	McBSP3 Data receive register 2	16	R/W	0000h
0x00 B801h	E101:7002	MCBSP3_DRR1	McBSP3 Data receive register 1	16	R/W	0000h
0x00 B802h	E101:7004	MCBSP3_DXR2	McBSP3 Data transmit register 2	16	R/W	0000h
0x00 B803h	E101:7006	MCBSP3_DXR1	McBSP3 Data transmit register 1	16	R/W	0000h
0x00 B804h	E101:7008	MCBSP3_SPCR2	McBSP3 Serial port control register 2	16	R/W	0000h
0x00 B805h	E101:700A	MCBSP3_SPCR1	McBSP3 Serial port control register 1	16	R/W	0000h
0x00 B806h	E101:700C	MCBSP3_RCR2	McBSP3 Receive control register 2	16	R//W	0000h
0x00 B807h	E101:700E	MCBSP3_RCR1	McBSP3 Receive control register 1	16	R/W	0000h
0x00 B808h	E101:7010	MCBSP3_XCR2	McBSP3 Transmit control register 2	16	R/W	0000h
0x00 B809h	E101:7012	MCBSP3_XCR1	McBSP3 Transmit control register 1	16	R/W	0000h
0x00 B80Ah	E101:7014	MCBSP3_SRGR2	McBSP3 Sample rate generator register 2	16	R/W	2000h
0x00 B80Bh	E101:7016	MCBSP3_SRGR1	McBSP3 Sample rate generator register 1	16	R/W	0001h
0x00 B80Ch	E101:7018	MCBSP3_MCR2	McBSP3 Multichannel register 2	16	R/W	0000h
0x00 B80Dh	E101:701A	MCBSP3_MCR1	McBSP3 Multichannel register 1	16	R/W	0000h
0x00 B80Eh	E101:701C	MCBSP3_RCERA	McBSP3 Receive channel enable register partition A	16	R/W	0000h
0x00 B80Fh	E101:701E	MCBSP3_RCERB	McBSP3 Receive channel enable register partition B	16	R/W	0000h
0x00 B810h	E101:7020	MCBSP3_XCERA	McBSP3 Transmit channel enable register partition A	16	R/W	0000h
0x00 B811h	E101:7022	MCBSP3_XCERB	McBSP3 Transmit channel enable register partition B	16	R/W	0000h
0x00 B812h	E101:7024	MCBSP3_PCR0	McBSP3 Pin control register 0	16	R/W	0000h

Table 3−50. McBSP3 Registers (Continued)

DSP WORD ADDRESS	MPU BYTE ADDRESS (VIA MPUI)	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 B813h	E101:7026	MCBSP3_RCERC	McBSP3 Receive channel enable register partition C	16	R/W	0000h
0x00 B814h	E101:7028	MCBSP3_RCERD	McBSP3 Receive channel enable register partition D	16	R/W	0000h
0x00 B815h	E101:702A	MCBSP3_XCERC	McBSP3 Transmit channel enable register partition C	16	R/W	0000h
0x00 B816h	E101:702C	MCBSP3_XCERD	McBSP3 Transmit channel enable register partition D	16	R/W	0000h
0x00 B817h	E101:702E	MCBSP3_RCERE	McBSP3 Receive channel enable register partition E	16	R/W	0000h
0x00 B818h	E101:7030	MCBSP3_RCERF	McBSP3 Receive channel enable register partition F	16	R/W	0000h
0x00 B819h	E101:7032	MCBSP3_XCERE	McBSP3 Transmit channel enable register partition E	16	R/W	0000h
0x00 B81Ah	E101:7034	MCBSP3_XCERF	McBSP3 Transmit channel enable register partition F	16	R/W	0000h
0x00 B81Bh	E101:7036	MCBSP3_RCERG	McBSP3 Receive channel enable register partition G	16	R/W	0000h
0x00 B81Ch	E101:7038	MCBSP3_RCERH	McBSP3 Receive channel enable register partition H	16	R/W	0000h
0x00 B81Dh	E101:703A	MCBSP3_XCERG	McBSP3 Transmit channel enable register partition G	16	R/W	0000h
0x00 B81Eh	E101:703C	MCBSP3_XCERH	McBSP3 Transmit channel enable register partition H	16	R/W	0000h
0x00 B81Fh	E101:703E	MCBSP3_REV	McBSP3 Version register	16	R/W	0011h

3.2.2.5 MPU Configuration Registers

The MPU public peripheral registers include the following:

- MPU TIPB Bus Switch Registers
- Ultra Low-Power Device Peripheral Registers
- OMAP5912 Configuration Registers
- Device Die Identification Registers
- Production Identification Registers
- L3 OCP Initiator Registers
- MPU Interface (MPUI) Registers
- TIPB (Private) Bridge 1 Configuration Registers
- Traffic Controller Registers
- MPU Clock/Reset/Power Mode Control Registers
- DPLL1 Configuration Register
- DSP MMU Registers
- TIPB (Public) Bridge2 Configuration Registers

Table 3−51. MPU TIPB Bus Switch Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFB:C800	UART1_SSW_CONF	UART1 Peripheral Ownership Register	32	R/W	0000 0001h
FFFB:C820	UART2_SSW_CONF	UART2 Peripheral Ownership Register	32	R/W	0000 0001h
FFFB:C840	UART3_SSW_CONF	UART3 Peripheral Ownership Register	32	R/W	0000 0001h
FFFB:C890	MCBSP2_SSW_CONF	McBSP2 Peirpheral Ownership Register	32	R/W	0000 0001h
FFFB:C8A0	I2C_SSW_CONF	I2C Peripheral Ownership Register	32	R/W	0000 0001h
FFFB:C8B0	SPI_SSW_CONF	SPI Peripheral Ownership Register	32	R/W	0000 0001h
FFFB:C8C0	DUALMODETIMER1_SSW_CONF	Dual Mode Timer1 Ownership Register	32	R/W	0000 0001h
FFFB:C8D0	DUALMODETIMER2_SSW_CONF	Dual Mode Timer2 Ownership Register	32	R/W	0000 0001h
FFFB:C8E0	DUALMODETIMER3_SSW_CONF	Dual Mode Timer3 Ownership Register	32	R/W	0000 0001h
FFFB:C8F0	DUALMODETIMER4_SSW_CONF	Dual Mode Timer4 Ownership Register	32	R/W	0000 0001h
FFFB:C900	DUALMODETIMER5_SSW_CONF	Dual Mode Timer5 Ownership Register	32	R/W	0000 0001h
FFFB:C910	DUALMODETIMER6_SSW_CONF	Dual Mode Timer6 Ownership Register	32	R/W	0000 0001h
FFFB:C930	DUALMODETIMER7_SSW_CONF	Dual Mode Timer7 Ownership Register	32	R/W	0000 0001h
FFFB:C940	DUALMODETIMER8_SSW_CONF	Dual Mode Timer8 Ownership Register	32	R/W	0000 0001h
FFFB:C960	MMCSD2_SSW_CONF	MMCSD2 Ownership Register	32	R/W	0000 0001h

Table 3−52. Ultra Low-Power Device Peripheral Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:0800	COUNTER_32_LSB	ULPD 32-kHz Counter Register LSB	16	R	0001h
FFFE:0804	COUNTER_32_MSB	ULPD 32-kHz Counter Register MSB	16	R	0001h
FFFE:0808	COUNTER_HIGH_FREQ_LSB	ULPD High-Frequency Counter LSB Register	16	R	0001h
FFFE:080C	COUNTER_HIGH_FREQ_MSB	ULPD High-Frequency Counter MSB Register	16	R	0000h
FFFE:0810	GAUGING_CTRL_REG	ULPD Gauging Control Register	16	R/W	0000h
FFFE:0814	IT_STATUS_REG	ULPD Interrupt Status Register	16	R	0000h
FFFE:0818 − FFFE:0820		Reserved			
FFFE:0824	SETUP_ULPD1_REG	ULPD Wakeup Time Setup Register	16	R/W	03FFh
FFFE:0828 − FFFE:082C		Reserved			
FFFE:0830	CLOCK_CTRL_REG	ULPD Clock Control Register	16	R/W	0000h
FFFE:0834	SOFT_REQ_REG	ULPD Soft Clock Request Register	16	R/W	0000h
FFFE:0838	COUNTER_32_FIQ_REG	ULPD Modem Shutdown Delay Register	16	R/W	0001h
FFFE:083C	DPLL_CTRL_REG	ULPD USB DPLL Control Register	16	R/W	2211h
FFFE:0840	STATUS_REQ_REG	ULPD Hardware Request Status Register	16	R/W	undef
FFFE:0844		Reserved			
FFFE:0848	LOCK_TIME_REG	ULPD APLL Lock Time Register	16	R/W	0960h
FFFE:084C	APLL_CTRL_REG	ULPD APLL Control Register	16	R/W	undef
FFFE:0850	POWER_CTRL_REG	ULPD Power Control Register	16	R/W	0008h

Table 3−53. OMAP5912 Configuration Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:1000	FUNC_MUX_CTRL_0	Functional Mux Control Register 0	32	R/W	0000 0000h
FFFE:1004	FUNC_MUX_CTRL_1	Functional Mux Control Register 1	32	R/W	0000 0000h
FFFE:1008	FUNC_MUX_CTRL_2	Functional Mux Control Register 2	32	R/W	0000 0000h
FFFE:100C	COMP_MODE_CTRL_0	I/O Multiplex Enable Register 0	32	R/W	0000 0000h
FFFE:1010	FUNC_MUX_CTRL_3	Functional Mux Control Register 3	32	R/W	0000 0000h
FFFE:1014	FUNC_MUX_CTRL_4	Functional Mux Control Register 4	32	R/W	0000 0000h
FFFE:1018	FUNC_MUX_CTRL_5	Functional Mux Control Register 5	32	R/W	0000 0000h
FFFE:101C	FUNC_MUX_CTRL_6	Functional Mux Control Register 6	32	R/W	0000 0000h
FFFE:1020	FUNC_MUX_CTRL_7	Functional Mux Control Register 7	32	R/W	0000 0000h
FFFE:1024	FUNC_MUX_CTRL_8	Functional Mux Control Register 8	32	R/W	0000 0000h
FFFE:1028	FUNC_MUX_CTRL_9	Functional Mux Control Register 9	32	R/W	0000 0000h
FFFE:102C	FUNC_MUX_CTRL_A	Functional Mux Control Register A	32	R/W	0000 0000h
FFFE:1030	FUNC_MUX_CTRL_B	Functional Mux Control Register B	32	R/W	0000 0000h
FFFE:1034	FUNC_MUX_CTRL_C	Functional Mux Control Register C	32	R/W	0000 0000h
FFFE:1038	FUNC_MUX_CTRL_D	Functional Mux Control Register D	32	R/W	0000 0000h
FFFE:1040	PULL_DWN_CTRL_0	Pull Down Control Register 0	32	R/W	0000 0000h
FFFE:1044	PULL_DWN_CTRL_1	Pull Down Control Register 1	32	R/W	0000 0000h
FFFE:1048	PULL_DWN_CTRL_2	Pull Down Control Register 2	32	R/W	0000 0000h

Table 3−53. OMAP5912 Configuration Registers (Continued)

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:104C	PULL_DWN_CTRL_3	Pull Down Control Register 3	32	R/W	0000 0000h
FFFE:1050	GATE_INH_CTRL_0	Gate Inhibit Control Register 0	32	R/W	0000 0000h
FFFE:1058	CONF_REV	Configuration Revision	32	R	0000 0002h
FFFE:1060	VOLTAGE_CTRL_0	Voltage Control Register 0	32	R/W	0000 0000h
FFFE:1064	USB_TRANSCEIVER_CTRL	USB Transceiver Control Register	32	R/W	0000 0006h
FFFE:1068	LDO_PWRDN_CTRL	LDO Power Down Control Register	32	R/W	0000 0000h
FFFE:1080	MOD_CONF_CTRL_0	Module Configuration Register 0	32	R/W	0000 0000h
FFFE:1090	FUNC_MUX_CTRL_E	Function Mux Control Register E	32	R/W	0000 0000h
FFFE:1094	FUNC_MUX_CTRL_F	Function Mux Control Register F	32	R/W	0000 0000h
FFFE:1098	FUNC_MUX_CTRL_10	Function Mux Control Register 10	32	R/W	0000 0000h
FFFE:109C	FUNC_MUX_CTRL_11	Function Mux Control Register 11	32	R/W	0000 0000h
FFFE:10A0	FUNC_MUX_CTRL_12	Function Mux Control Register 12	32	R/W	0000 0000h
FFFE:10AC	PULL_DWN_CTRL_4	Pull Down Control Register 4	32	R/W	0000 0000h
FFFE:10B4	PU_PD_SEL_0	Pull Up Pull Down Slection Register 0	32	R/W	0000 0000h
FFFE:10B8	PU_PD_SEL_1	Pull Up Pull Down Slection Register 1	32	R/W	0000 0000h
FFFE:10B8	PU_PD_SEL_2	Pull Up Pull Down Slection Register 2	32	R/W	0000 0000h
FFFE:10C0	PU_PD_SEL_3	Pull Up Pull Down Slection Register 3	32	R/W	0000 0000h
FFFE:10C4	PU_PD_SEL_4	Pull Up Pull Down Slection Register 4	32	R/W	0000 0000h
FFFE:10D0	FUNC_MUX_DSP_DMA_A	DSP DMA Functional Mux Register A	32	R/W	undef
FFFE:10D4	FUNC_MUX_DSP_DMA_B	DSP DMA Functional Mux Register B	32	R/W	undef
FFFE:10D8	FUNC_MUX_DSP_DMA_C	DSP DMA Functional Mux Register C	32	R/W	undef
FFFE:10DC	FUNC_MUX_DSP_DMA_D	DSP DMA Functional Mux Register D	32	R/W	undef
FFFE:10EC	FUNC_MUX_ARM_DMA_A	ARM DMA Functional Mux Register A	32	R/W	undef
FFFE:10F0	FUNC_MUX_ARM_DMA_B	ARM DMA Functional Mux Register B	32	R/W	undef
FFFE:10F4	FUNC_MUX_ARM_DMA_C	ARM DMA Functional Mux Register C	32	R/W	undef
FFFE:10F8	FUNC_MUX_ARM_DMA_D	ARM DMA Functional Mux Register D	32	R/W	undef
FFFE:10FC	FUNC_MUX_ARM_DMA_E	ARM DMA Functional Mux Register E	32	R/W	undef
FFFE:1100	FUNC_MUX_ARM_DMA_F	ARM DMA Functional Mux Register F	32	R/W	undef
FFFE:1104	FUNC_MUX_ARM_DMA_G	ARM DMA Functional Mux Register G	32	R/W	undef
FFFE:1110	MOD_CONF_CTRL_1	Module Confguration Control Register 1	32	R/W	undef
FFFE:1120	SECCTRL	Secure Mode Control Register	32	R/W	0000 0D1Ah
FFFE:1130	CONF_STATUS	Confguration Status Register	32	R	0000 0000h
FFFE:1140	RESET_CTRL	Reset Control Register	32	R/W	0000 007Fh
FFFE:1150	MOD_CONF_CTRL_2	Configuration Control Register 2	32	R/W	0000 0002h

Table 3−54. Device Die Identification Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:1800	DIE_ID_LSB	Device Die Identification Register (LSB)	32	R	undef
FFFE:1804	DIE_ID_MSB	Device Die Identification Register (MSB)	32	R	undef

Table 3−55. Production Identification Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:2000	PROD_ID_REG0	Production Identification Register0	32	R	undef
FFFE:2004	PROD_ID_REG1	Production Identification Register1	32	R	undef

Table 3−56. L3 OCP Initiator Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:C320	ADDR_FAULT	Address Fault Register	32	R	0000 0000h
FFFE:C324	MCMD_FAULT	Master Command Fault Register	32	R	0000 0000h
FFFE:C328	S_INTERRUPT0	Interrupt Sensitvity Register0	32	R/W	0000 0003h
FFFE:C330	S_INTERRUPT1	Interrupt Sensitvity Register1	32	R/W	0000 0003h
FFFE:C334	PROTECT	Memory Protect Register	32	R/W	0000 0000h
FFFE:C338	SECURE_MODE	Secure Mode Register	32	R/W	0000 007Fh
FFFE:C32C	ABORT_TYPE	Abort Type Register	32	R	0000 0000h

Table 3−57. MPU Interface (MPUI) Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:C900	CTRL_REG	MPUI Control Register	32	R/W	0003 FFFFh
FFFE:C904	DEBUG_ADDR	MPUI Debug Address Register	32	R	00FF FFFFh
FFFE:C908	DEBUG_DATA	MPUI Debug Data Register	32	R	FFFF FFFFh
FFFE:C90C	DEBUG_FLAG	MPUI Debug Flag Register	32	R	0000 1800h
FFFE:C910	STATUS_REG	MPUI Status Register	32	R	0000 1FFFh
FFFE:C914	DSP_STATUS_REG	MPUI DSP Status Register	32	R	0000 0000h
FFFE:C918	DSP_BOOT_CONFIG	MPUI Boot Configuration Register	32	R/W	0000 0000h
FFFE:C91C	DSP_API_CONFIG	MPUI DSP AP Configuration Register	32	R/W	0000 FFFFh
FFFE:C920	DSP_MISC_CONFIG	MPUI Miscellaneous Configuration Register	32	R/W	0000 0000h
FFFE:C924	ENHANCED_CTL	Enhanced Control Register	32	R/W	0000 0000h

Table 3−58. TIPB (Private) Bridge 1 Configuration Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:CA00	TIPB_CNTL	Private TIPB Control Register	16 or 32	R/W	FF11h
FFFE:CA04	TIPB_BUS_ALLOC	Private TIPB Bus Allocation Register	16 or 32	R/W	0009h
FFFE:CA08	MPU_TIPB_CNTL	Private MPU TIPB Control Register	16 or 32	R/W	0000h
FFFE:CA0C	ENHANCED_TIPB_CNTL	Private Enhanced TIPB Control Register	16 or 32	R/W	000Fh
FFFE:CA10	ADDRESS_DBG	Private Debug Address Register	16 or 32	R	FFFFh
FFFE:CA14	DATA_DEBUG_LOW	Private Debug Data LSB Register	16 or 32	R	FFFFh
FFFE:CA18	DATA_DEBUG_HIGH	Private Debug Data MSB Register	16 or 32	R	FFFFh
FFFE:CA1C	DEBUG_CNTR_SIG	Private Debug Control Signals Register	16 or 32	R	00FCh
FFFE:CA20	ACCESS_CNTL	Private Access Control Register	16 or 32	R/W	0001h

Table 3−59. Traffic Controller EMIFS Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:CC0C	EMIFS_CONFIG_REG	EMIFS Configuration Register	32	R/W	undef
FFFE:CC10	EMIFS_CS0_CONFIG	EMIFS nCS0 Configuration Register	32	R/W	undef
FFFE:CC14	EMIFS_CS1_CONFIG	EMIFS nCS1 Configuration Register	32	R/W	undef
FFFE:CC18	EMIFS_CS2_CONFIG	EMIFS nCS2 Configuration Register	32	R/W	undef
FFFE:CC1C	EMIFS_CS3_CONFIG	EMIFS nCS3 Configuration Register	32	R/W	undef
FFFE:CC28	EMIFS_TIMEOUT1	EMIFS Dynamic Priority Timeout 1 Register	32	R/W	0000 0000h
FFFE:CC2C	EMIFS_TIMEOUT2	EMIFS Dynamic Priority Timeout 2 Register	32	R/W	0000 0000h
FFFE:CC30	EMIFS_TIMEOUT3	EMIFS Dynamic Priority Timeout 3 Register	32	R/W	0000 0000h
FFFE:CC34	ENDIANISM	Endianism Register	32	R/W	0000 0000h
FFFE:CC38		Reserved			
FFFE:CC40	EMIFS_CFG_DYN_WAIT	EMIFS Dynamic Wait-States Register	32	R/W	0000 0000h
FFFE:CC44	EMIFS_ABORT_ADDR	EMIFS Abort Address Register	32	R	0000 0000h
FFFE:CC48	EMIFS_ABORT_TYPE	EMIFS Abort Type Register	32	R	0000 0000h
FFFE:CC4C	EMIFS_ABORT_TIMEOUT	EMIFS Abort Timeout Register	32	R/W	0000 01FFh
FFFE:CC50	EMIFS_ADV_CS0_CONFIG	Advanced EMIFS Chip Select Configuration Register nCS0	32	R/W	0000 0000h
FFFE:CC54	EMIFS_ADV_CS1_CONFIG	Advanced EMIFS Chip Select Configuration Register nCS1	32	R/W	0000 0000h
FFFE:CC58	EMIFS_ADV_CS2_CONFIG	Advanced EMIFS Chip Select Configuration Register nCS2	32	R/W	0000 0000h
FFFE:CC5C	EMIFS_ADV_CS3_CONFIG	Advanced EMIFS Chip Select Configuration Register nCS3	32	R/W	0000 0000h

Table 3−60. Traffic Controller OCP−T1/OCP−T2 Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:CC00	OCP_T1_PRIO	OCP−T1 LRU Priority Register	32	R/W	0000 0000h
FFFE:CCA0	OCP_T1_TIMEOUT1	OCP−T1 Dynamic Priority Time-out Register 1	32	R/W	0000 0000h
FFFE:CCA4	OCP_T1_TIMEOUT2	OCP−T1 Dynamic Priority Time-out Register 2	32	R/W	0000 0000h
FFFE:CCA8	OCP_T1_TIMEOUT3	OCP−T1 Dynamic Priority Time-out Register 3	32	R/W	0000 0000h
FFFE:CCAC	OCP_T1_ABORT_TIMEOUT	OCP−T1 Abort Time-out Register	32	R/W	0000 01FFh
FFFE:CCB0	OCP_T1_ABORT_ADDR	OCP−T1 Abort Address Register	32	R	0000 0000h
FFFE:CCB4	OCP_T1_ABORT_TYPE	OCP−T1 Abort Type Register	32	R	0000 0000h
FFFE:CCB8	CONFIG_REG	OCP Target Configuration Register	32	R/W	0000 0000h
FFFE:CCD0	OCP_T2_PRIO	OCP−T2 LRU Priority Register	32	R/W	0000 0000h
FFFE:CCD4	OCP_T2_TIMEOUT1	OCP−T2 Dynamic Priority Time-out Register 1	32	R/W	0000 0000h
FFFE:CCD8	OCP_T2_TIMEOUT2	OCP−T2 Dynamic Priority Time-out Register 2	32	R/W	0000 0000h
FFFE:CCDC	OCP_T2_TIMEOUT3	OCP−T2 Dynamic Priority Time-out Register 3	32	R/W	0000 0000h
FFFE:CCE0	OCP_T2_ABORT_TIMEOUT	OCP−T2 Abort Time-out Register	32	R/W	0000 01FFh
FFFE:CCE4	OCP_T2_ABORT_ADDR	OCP−T2 Abort Address Register	32	R	0000 0000h
FFFE:CCE8	OCP_T2_ABORT_TYPE	OCP−T2 Abort Type Register	32	R	0000 0000h

Table 3−61. Traffic Controller OCPI Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:C320	OCP_ADDR_FAULT	OCPI Address Fault Register	32	R	0000 0000h
FFFE:C324	OCP_MCMD_FAULT	OCP Master Command Fault Register	32	R	0000 0000h
FFFE:C328	OCP_SINT0	OCP Sinterrupt 0 Register	32	R/W	0000 0003h
FFFE:C32C	OCP_ABORT_TYPE	OCP Abort Type Register	32	R/W	0000 0000h
FFFE:C330	OCP_SINT1	OCP Sinterrupt 1 Register	32	R/W	0000 0003h
FFFE:C334	OCP_PROT	OCP Protection Register	32	R/W	0000 0000h
FFFE:C338	OCP_SMOD	OCPI Secure Mode Register	32	R/W	0000 003Fh

Table 3−62. Traffic Controller EMIFF Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:CC08	EMIFF_PRIO_REG	EMIFF Priority Register	32	R/W	0000 0000h
FFFE:CC20	EMIFF_SDRAM_CONFIG	EMIFF SDRAM Configuration Register	32	R/W	0061 8800h
FFFE:CC24	EMIFF_MRS	EMIFF SDRAM MRS Register	32	R/W	0000 0037h
FFFE:CC3C	EMIFF_SDRAM_CONFIG_2	EMIFF SDRAM Configuration Register 2	32	R/W	0000 0003h
FFFE:CC64	DLL_WRT_CTL	DLL WRT Control Register (write byte)	32	R/W	0000 0000h
FFFE:CC68	DLL_WRT_STAT	DLL WRT Status Register (read lower byte)	32	R	0000 0000h
FFFE:CC70	EMIFF_MRS_NEW	EMIFF SDRAM MRS Register (duplicate)	32	R/W	0000 0037h
FFFE:CC74	EMIFF_EMRS0	EMIFF SDRAM EMRS 0 Register	32	R/W	0000 0000h
FFFE:CC78	EMIFF_EMRS1	EMIFF SDRAM EMRS 1 Register	32	R/W	0000 0000h
FFFE:CC80	EMIFF_OP	EMIFF SDRAM Operation Register	32	R/W	0000 0004h
FFFE:CC84	EMIFF_MCMD	EMIFF SDRAM Manual Command Register	32	R/W	0000 0000h
FFFE:CC8C	EMIFF_TIMEOUT1	EMIFF Dynamic Arb. Priority Timeout 1 Register	32	R/W	0000 0000h
FFFE:CC90	EMIFF_TIMEOUT2	EMIFF Dynamic Arb. Priority Timeout 2 Register	32	R/W	0000 0000h
FFFE:CC94	EMIFF_TIMEOUT3	EMIFF Dynamic Arb. Priority Timeout 3 Register	32	R/W	0000 0000h
FFFE:CC98	EMIFF_ABORT_ADDR	EMIFF Abort Address Register	32	R	0000 0000h
FFFE:CC9C	EMIFF_ABORT_TYPE	EMIFF Abort Type Register	32	R	0000 0000h
FFFE:CCC0	DLL_URD_CTL	DLL URD Control Register (read upper byte)	32	R/W	0000 0000h
FFFE:CCC4	DLL_URD_STAT	DLL URD Status Register (read upper byte)	32	R	0000 0000h
FFFE:CCC8	EMIFF_EMRS2	EMIFF SDRAM EMRS 2 Register	32	R/W	0000 0000h
FFFE:CCCC	DLL_LRD_CTL	DLL LRD Control Register (read lower byte)	32	R/W	0000 0000h
FFFE:CCBC	DLL_LRD_STAT	DLL LRD Status Register (read lower byte)	32	R	0000 0000h

Table 3−63. MPU Clock/Reset/Power Mode Control Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:CE00	ARM_CKCTL	MPU Clock Control Register	32	R/W	3000h
FFFE:CE04	ARM_IDLECT1	MPU Idle Control 1 Register	32	R/W	0400h
FFFE:CE08	ARM_IDLECT2	MPU Idle Control 2 Register	32	R/W	0100h
FFFE:CE0C	ARM_EWUPCT	MPU External Wakeup Control Register	32	R/W	003Fh
FFFE:CE10	ARM_RSTCT1	MPU Reset Control 1 Register	32	R/W	0000h
FFFE:CE14	ARM_RSTCT2	MPU Reset Control 2 Register	32	R/W	0000h
FFFE:CE18	ARM_SYSST	MPU System Status Register	32	R/W	0038h
FFFE:CE1C	ARM_CKOUT1	MPU Clock Out Definition Register 1	32	R/W	0015h
FFFE:CE20	ARM_CKOUT2	MPU Clock Out Definition Register 2	32	R/W	0000h
FFFE:CE24	ARM_IDLECT3	MPU Idle Enable Control Register 3	32	R/W	0015h

Table 3−64. DPLL1 Configuration Register

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:CF00	DPLL1_CTL_REG	DPLL1 Control Register	32	R/W	0000 2002h

Table 3−65. DSP MMU Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:D200	DSP_MMU_PREFETCH_REG	DSP MMU Prefetch Register	16	R/W	0000h
FFFE:D204	DSP_MMU_WALKING_ST_REG	DSP MMU Prefetch Status Register	16	R	0000h
FFFE:D208	DSP_MMU_CNTL_REG	DSP MMU Control Register	16	R/W	0000h
FFFE:D20C	DSP_MMU_FAULT_AD_H_REG	DSP MMU Fault Address Register MSB	16	R	0000h
FFFE:D210	DSP_MMU_FAULT_AD_L_REG	DSP MMU Fault Address Register LSB	16	R	0000h
FFFE:D214	DSP_MMU_F_ST_REG	DSP MMU Fault Status Register	16	R	0000h
FFFE:D218	DSP_MMU_IT_ACK_REG	DSP MMU IT Acknowledge Register	16	W	0000h
FFFE:D21C	DSP_MMU_TTB_H_REG	DSP MMU TTB Register MSB	16	R/W	0000h
FFFE:D220	DSP_MMU_TTB_L_REG	DSP MMU TTB Register LSB	16	R/W	0000h
FFFE:D224	DSP_MMU_LOCK_REG	DSP MMU Lock Counter Register	16	R/W	0000h
FFFE:D228	DSP_MMU_LD_TLB_REG	DSP MMU Load Entry TLB Register	16	R/W	0000h
FFFE:D22C	DSP_MMU_CAM_H_REG	DSP MMU CAM Entry Register MSB	16	R/W	0000h
FFFE:D230	DSP_MMU_CAM_L_REG	DSP MMU CAM Entry Register LSB	16	R/W	0000h
FFFE:D234	DSP_MMU_RAM_H_REG	DSP MMU RAM Entry Register MSB	16	R/W	0000h
FFFE:D238	DSP_MMU_RAM_L_REG	DSP MMU RAM Entry Register LSB	16	R/W	0000h
FFFE:D23C	DSP_MMU_GFLUSH_REG	DSP MMU Global Flush Register	16	R/W	0000h
FFFE:D240	DSP_MMU_FLUSH_ENTRY_REG	DSP MMU Individual Flush Register	16	R/W	0000h
FFFE:D244	DSP_MMU_READ_CAM_H_REG	DSP MMU Read CAM Register MSB	16	R/W	0000h
FFFE:D248	DSP_MMU_READ_CAM_L_REG	DSP MMU Read CAM Register LSB	16	R/W	0000h
FFFE:D24C	DSP_MMU_READ_RAM_H_REG	DSP MMU Read RAM Register MSB	16	R/W	0000h
FFFE:D250	DSP_MMU_READ_RAM_L_REG	DSP MMU Read RAM Register LSB	16	R/W	0000h

Table 3−66. TIPB (Public) Bridge 2 Configuration Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:D300	TIPB_CNTL	Public TIPB Control Register	16 or 32	R/W	FF11h
FFFE:D304	TIPB_BUS_ALLOC	Public TIPB Bus Allocation Register	16 or 32	R/W	0009h
FFFE:D308	MPU_TIPB_CNTL	Public MPU TIPB Control Register	16 or 32	R/W	0000h
FFFE:D30C	ENHANCED_TIPB_CNTL	Public Enhanced TIPB Control Register	16 or 32	R/W	0007h
FFFE:D310	ADDRESS_DBG	Public Debug Address Register	16 or 32	R	FFFFh
FFFE:D314	DATA_DEBUG_LOW	Public Debug Data LSB Register	16 or 32	R	FFFFh
FFFE:D318	DATA_DEBUG_HIGH	Public Debug Data MSB Register	16 or 32	R	FFFFh
FFFE:D31C	DEBUG_CNTR_SIG	Public Debug Control Signals Register	16 or 32	R	00F8h

3.3 DSP Memory Maps

The DSP supports a unified program/data memory map (program and data accesses are made to the same physical space); however, peripheral registers are located in a separate I/O space which is accessed via the DSP's port instructions.

3.3.1 DSP Global Memory Map

The DSP Subsystem contains 160K bytes of on-chip SRAM (64K bytes of DARAM and 96K bytes of SARAM). The MPU also has access to these memories via the MPUI (MPU Interface) port. The DSP also has access to the shared system SRAM (250K bytes) and both EMIF spaces (EMIFF and EMIFS) via the DSP Memory Management Unit (MMU) which is configured by the MPU.

Table 3−67 shows the high-level program/data memory map for the DSP subsystem. DSP data accesses utilize 16-bit word addresses while DSP program fetches utilize byte addressing.

Table 3−67. DSP Global Memory Map

BYTE ADDRESS RANGE	WORD ADDRESS RANGE	INTERNAL MEMORY	EXTERNAL MEMORY†
0x00 0000 − 0x00 FFFF	0x00 0000 − 0x00 7FFF	DARAM 64K bytes	
0x01 0000 − 0x02 7FFF	0x00 8000 − 0x01 3FFF	SARAM 96K bytes	
0x02 8000 − 0x04 FFFF	0x01 4000 − 0x02 7FFF	Reserved	
0x05 0000 − 0xFF 7FFF	0x02 8000 − 0x7F BFFF		Managed by DSP MMU
0xFF 8000 − 0xFF FFFF	0x7F C000 − 0x7F FFFF	PDROM (MPNMC = 0)	Managed by DSP MMU (MPNMC =1)

† This space could be external memory or internal shared system memory, depending on the DSP MMU configuration.

3.3.2 On-Chip Dual-Access RAM (DARAM)

The DARAM is located in the byte address range 000000h−00FFFFh and is composed of eight blocks of 8K bytes each (see Table 3−68). Each DARAM block can perform two accesses per cycle (two reads, two writes, or a read and a write).

Table 3−68. DARAM Blocks

DSP BYTE ADDRESS RANGE	DSP WORD ADDRESS RANGE	MEMORY BLOCK
0x00 0000 − 0x00 1FFF	0x00 0000 − 0x00 0FFF	DARAM 0
0x00 2000 − 0x00 3FFF	0x00 1000 − 0x001FFF	DARAM 1
0x00 4000 − 0x00 5FFF	0x00 2000 − 0x00 2FFF	DARAM 2
0x00 6000 − 0x00 7FFF	0x00 3000 − 0x00 3FFF	DARAM 3
0x00 8000 − 0x00 9FFF	0x00 4000 − 0x00 4FFF	DARAM 4
0x00 A000 − 0x00 BFFF	0x00 5000 − 0x00 5FFF	DARAM 5
0x00 C000 − 0x00 DFFF	0x00 6000 − 0x00 6FFF	DARAM 6
0x00 E000 − 0x00 FFFF	0x00 7000 − 0x00 7FFF	DARAM 7

3.3.3 On-Chip Single-Access RAM (SARAM)

The SARAM is located at the byte address range 010000h−027FFFh and is composed of 12 blocks of 8K bytes each (see Table 3−69). Each SARAM block can perform one access per cycle (one read or one write).

Table 3−69. SARAM Blocks

DSP BYTE ADDRESS RANGE	DSP WORD ADDRESS RANGE	MEMORY BLOCK
0x01 0000 − 0x01 1FFF	0x00 8000 − 0x00 8FFF	SARAM 0
0x01 2000 − 0x01 3FFF	0x00 9000 − 0x00 9FFF	SARAM 1
0x01 4000 − 0x01 5FFF	0x00 A000 − 0x00 AFFF	SARAM 2
0x01 6000 − 0x01 7FFF	0x00 B000 − 0x00 BFFF	SARAM 3
0x01 8000 − 0x01 9FFF	0x00 C000 − 0x00 CFFF	SARAM 4
0x01 A000 − 0x01 BFFF	0x00 D000 − 0x00 DFFF	SARAM 5
0x01 C000 − 0x01 DFFF	0x00 E000 − 0x00 EFFF	SARAM 6
0x01 E000 − 0x01 FFFF	0x00 F000 − 0x00 FFFF	SARAM 7
0x02 0000 − 0x02 1FFF	0x01 0000 − 0x01 0FFF	SARAM 8
0x02 2000 − 0x02 3FFF	0x01 1000 − 0x01 1FFF	SARAM 9
0x02 4000 − 0x02 5FFF	0x01 2000 − 0x01 2FFF	SARAM 10
0x02 6000 − 0x02 7FFF	0x01 3000 − 0x01 3FFF	SARAM 11

3.3.4 DSP I/O Space Memory Map

The DSP I/O space is a separate address space from the data/program memory space. The I/O space is accessed via the DSP's port instructions. The DSP I/O space is accessed using 16-bit word addresses. Table 3−70 to Table 3−82 specify the DSP base addresses where each set of registers is accessed. All accesses to these registers must utilize the appropriate access width as indicated in the tables. Accessing registers with the incorrect access width may cause unexpected results, including a TI Peripheral Bus (TIPB) bus error and associated TIPB interrupt.

3.3.4.1 DSP Private Peripheral Registers

The DSP Private Registers include the following:

- DSP DMA Controller Registers
- DSP Timer1 Registers
- DSP Timer2 Registers
- DSP Timer3 Registers
- DSP Watchdog Timer Registers
- DSP Level 2.0 Interrupt Handler Registers
- DSP Interrupt Interface Registers
- DSP Level 2.1 Interrupt Handler Registers

Table 3−70. DSP DMA Controller Registers

DSP WORD ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 0C00h	DSP_DMA_CSDP0	Channel 0 Source/Destination Parameters Register	16	R/W	0000h
0x00 0C01h	DSP_DMA_CCR0	Channel 0 Control Register	16	R/W	0000h
0x00 0C02h	DSP_DMA_CICR0	Channel 0 Interrupt Control Register	16	R/W	0003h
0x00 0C03h	DSP_DMA_CSR0	Channel 0 Status Register	16	R	0000h
0x00 0C04h	DSP_DMA_CSSA_L0	Channel 0 Source Start Address Register LSB	16	R/W	undef
0x00 0C05h	DSP_DMA_CSSA_U0	Channel 0 Source Start Address Register MSB	16	R/W	undef
0x00 0C06h	DSP_DMA_CDSA_L0	Channel 0 Destination Start Address Register LSB	16	R/W	undef
0x00 0C07h	DSP_DMA_CDSA_U0	Channel 0 Destination Start Address Register MSB	16	R/W	undef
0x00 0C08h	DSP_DMA_CEN0	Channel 0 Element Number Register	16	R/W	undef
0x00 0C09h	DSP_DMA_CFN0	Channel 0 Frame Number Register	16	R/W	undef
0x00 0C0Ah	DSP_DMA_CSFI0	Channel 0 Frame Index Register	16	R/W	undef
0x00 0C0Bh	DSP_DMA_CSEI0	Channel 0 Element Index Register	16	R/W	undef
0x00 0C0Ch	DSP_DMA_CSAC0	Channel 0 Source Address Counter Register	16	R/W	undef
0x00 0C0Dh	DSP_DMA_CDAC0	Channel 0 Destination Address Counter Register	16	R/W	undef
0x00 0C0Eh	DSP_DMA_CDEI0	Channel 0 Destination Element Index	16	R/W	undef
0x00 0C0Fh	DSP_DMA_CDFI0	Channel 0 Destination Frame Index	16	R/W	undef
0x00 0C10h − 0x00 0C1Fh		Reserved			
0x00 0C20h	DSP_DMA_CSDP1	Channel 1 Source/Destination Parameters Register	16	R/W	0000h
0x00 0C21h	DSP_DMA_CCR1	Channel 1 Control Register	16	R/W	0000h
0x00 0C22h	DSP_DMA_CICR1	Channel 1 Interrupt Control Register	16	R/W	0003h
0x00 0C23h	DSP_DMA_CSR1	Channel 1 Status Register	16	R	0000h
0x00 0C24h	DSP_DMA_CSSA_L1	Channel 1 Source Start Address Register LSB	16	R/W	undef
0x00 0C25h	DSP_DMA_CSSA_U1	Channel 1 Source Start Address Register MSB	16	R/W	undef
0x00 0C26h	DSP_DMA_CDSA_L1	Channel 1 Destination Start Address Register LSB	16	R/W	undef
0x00 0C27h	DSP_DMA_CDSA_U1	Channel 1 Destination Start Address Register MSB	16	R/W	undef
0x00 0C28h	DSP_DMA_CEN1	Channel 1 Element Number Register	16	R/W	undef
0x00 0C29h	DSP_DMA_CFN1	Channel 1 Frame Number Register	16	R/W	undef
0x00 0C2Ah	DSP_DMA_CSFI1	Channel 1 Frame Index Register	16	R/W	undef
0x00 0C2Bh	DSP_DMA_CSEI1	Channel 1 Element Index Register	16	R/W	undef
0x00 0C2Ch	DSP_DMA_CSAC1	Channel 1 Source Address Counter Register	16	R/W	undef
0x00 0C2Dh	DSP_DMA_CDAC1	Channel 1 Destination Address Counter Register	16	R/W	undef
0x00 0C2Eh	DSP_DMA_CDEI1	Channel 1 Destination Element Index	16	R/W	undef
0x00 0C2Fh	DSP_DMA_CDFI1	Channel 1 Destination Frame Index	16	R/W	undef
0x00 0C30h − 0x00 0C3Fh		Reserved			
0x00 0C40h	DSP_DMA_CSDP2	Channel 2 Source/Destination Parameters Register	16	R/W	0000h
0x00 0C41h	DSP_DMA_CCR2	Channel 2 Control Register	16	R/W	0000h
0x00 0C42h	DSP_DMA_CICR2	Channel 2 Interrupt Control Register	16	R/W	0003h
0x00 0C43h	DSP_DMA_CSR2	Channel 2 Status Register	16	R	0000h
0x00 0C44h	DSP_DMA_CSSA_L2	Channel 2 Source Start Address Register LSB	16	R/W	undef
0x00 0C45h	DSP_DMA_CSSA_U2	Channel 2 Source Start Address Register MSB	16	R/W	undef
0x00 0C46h	DSP_DMA_CDSA_L2	Channel 2 Destination Start Address Register LSB	16	R/W	undef
0x00 0C47h	DSP_DMA_CDSA_U2	Channel 2 Destination Start Address Register MSB	16	R/W	undef

Table 3−70. DSP DMA Controller Registers (Continued)

DSP WORD ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 0C48h	DSP_DMA_CEN2	Channel 2 Element Number Register	16	R/W	undef
0x00 0C49h	DSP_DMA_CFN2	Channel 2 Frame Number Register	16	R/W	undef
0x00 0C4Ah	DSP_DMA_CSFI2	Channel 2 Frame Index Register	16	R/W	undef
0x00 0C4Bh	DSP_DMA_CSEI2	Channel 2 Element Index Register	16	R/W	undef
0x00 0C4Ch	DSP_DMA_CSAC2	Channel 2 Source Address Counter Register	16	R/W	undef
0x00 0C4Dh	DSP_DMA_CDAC2	Channel 2 Destination Address Counter Register	16	R/W	undef
0x00 0C4Eh	DSP_DMA_CDEI2	Channel 2 Destination Element Index	16	R/W	undef
0x00 0C4Fh	DSP_DMA_CDFI2	Channel 2 Destination Frame Index	16	R/W	undef
0x00 0C50h − 0x00 0C5Fh		Reserved			
0x00 0C60h	DSP_DMA_CSDP3	Channel 3 Source/Destination Parameters Register	16	R/W	0000h
0x00 0C61h	DSP_DMA_CCR3	Channel 3 Control Register	16	R/W	0000h
0x00 0C62h	DSP_DMA_CICR3	Channel 3 Interrupt Control Register	16	R/W	0003h
0x00 0C63h	DSP_DMA_CSR3	Channel 3 Status Register	16	R	0000h
0x00 0C64h	DSP_DMA_CSSA_L3	Channel 3 Source Start Address Register LSB	16	R/W	undef
0x00 0C65h	DSP_DMA_CSSA_U3	Channel 3 Source Start Address Register MSB	16	R/W	undef
0x00 0C66h	DSP_DMA_CDSA_L3	Channel 3 Destination Start Address Register LSB	16	R/W	undef
0x00 0C67h	DSP_DMA_CDSA_U3	Channel 3 Destination Start Address Register MSB	16	R/W	undef
0x00 0C68h	DSP_DMA_CEN3	Channel 3 Element Number Register	16	R/W	undef
0x00 0C69h	DSP_DMA_CFN3	Channel 3 Frame Number Register	16	R/W	undef
0x00 0C6Ah	DSP_DMA_CSFI3	Channel 3 Frame Index Register	16	R/W	undef
0x00 0C6Bh	DSP_DMA_CSEI3	Channel 3 Element Index Register	16	R/W	undef
0x00 0C6Ch	DSP_DMA_CSAC3	Channel 3 Source Address Counter Register	16	R/W	undef
0x00 0C6Dh	DSP_DMA_CDAC3	Channel 3 Destination Address Counter Register	16	R/W	undef
0x00 0C6Eh	DSP_DMA_CDEI3	Channel 3 Destination Element Index	16	R/W	undef
0x00 0C6Fh	DSP_DMA_CDFI3	Channel 3 Destination Frame Index	16	R/W	undef
0x00 0C70h − 0x00 0C7Fh		Reserved			
0x00 0C80h	DSP_DMA_CSDP4	Channel 4 Source/Destination Parameters Register	16	R/W	0000h
0x00 0C81h	DSP_DMA_CCR4	Channel 4 Control Register	16	R/W	0000h
0x00 0C82h	DSP_DMA_CICR4	Channel 4 Interrupt Control Register	16	R/W	0003h
0x00 0C83h	DSP_DMA_CSR4	Channel 4 Status Register	16	R	0000h
0x00 0C84h	DSP_DMA_CSSA_L4	Channel 4 Source Start Address Register LSB	16	R/W	undef
0x00 0C85h	DSP_DMA_CSSA_U4	Channel 4 Source Start Address Register MSB	16	R/W	undef
0x00 0C86h	DSP_DMA_CDSA_L4	Channel 4 Destination Start Address Register LSB	16	R/W	undef
0x00 0C87h	DSP_DMA_CDSA_U4	Channel 4 Destination Start Address Register MSB	16	R/W	undef
0x00 0C88h	DSP_DMA_CEN4	Channel 4 Element Number Register	16	R/W	undef
0x00 0C89h	DSP_DMA_CFN4	Channel 4 Frame Number Register	16	R/W	undef
0x00 0C8Ah	DSP_DMA_CSFI4	Channel 4 Frame Index Register	16	R/W	undef
0x00 0C8Bh	DSP_DMA_CSEI4	Channel 4 Element Index Register	16	R/W	undef
0x00 0C8Ch	DSP_DMA_CSAC4	Channel 4 Source Address Counter Register	16	R/W	undef
0x00 0C8Dh	DSP_DMA_CDAC4	Channel 4 Destination Address Counter Register	16	R/W	undef
0x00 0C8Eh	DSP_DMA_CDEI4	Channel 4 Destination Element Index	16	R/W	undef
0x00 0C8Fh	DSP_DMA_CDFI4	Channel 4 Destination Frame Index	16	R/W	undef

Table 3−70. DSP DMA Controller Registers (Continued)

DSP WORD ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 0C90h − 0x00 0C9Fh		Reserved			
0x00 0CA0h	DSP_DMA_CSDP5	Channel 5 Source/Destination Parameters Register	16	RW	0000h
0x00 0CA1h	DSP_DMA_CCR5	Channel 5 Control Register	16	R/W	0000h
0x00 0CA2h	DSP_DMA_CICR5	Channel 5 Interrupt Control Register	16	R/W	0003h
0x00 0CA3h	DSP_DMA_CSR5	Channel 5 Status Register	16	R	0000h
0x00 0CA4h	DSP_DMA_CSSA_L5	Channel 5 Source Start Address Register LSB	16	R/W	undef
0x00 0CA5h	DSP_DMA_CSSA_U5	Channel 5 Source Start Address Register MSB	16	R/W	undef
0x00 0CA6h	DSP_DMA_CDSA_L5	Channel 5 Destination Start Address Register LSB	16	R/W	undef
0x00 0CA7h	DSP_DMA_CDSA_U5	Channel 5 Destination Start Address Register MSB	16	R/W	undef
0x00 0CA8h	DSP_DMA_CEN5	Channel 5 Element Number Register	16	R/W	undef
0x00 0CA9h	DSP_DMA_CFN5	Channel 5 Frame Number Register	16	R/W	undef
0x00 0CAAh	DSP_DMA_CSFI5	Channel 5 Frame Index Register	16	R/W	undef
0x00 0CABh	DSP_DMA_CSEI5	Channel 5 Element Index Register	16	R/W	undef
0x00 0CACh	DSP_DMA_CSAC5	Channel 5 Source Address Counter Register	16	R/W	undef
0x00 0CADh	DSP_DMA_CDAC5	Channel 5 Destination Address Counter Register	16	R/W	undef
0x00 0CAEh	DSP_DMA_CDEI5	Channel 5 Destination Element Index	16	R/W	undef
0x00 0CAFh	DSP_DMA_CDFI5	Channel 5 Destination Frame Index	16	R/W	undef
0x00 0CB0h − 0x00 0DFFh		Reserved			
0x00 0E00h	DSP_DMA_GCR	Global Control Register	16	R/W	0008h
0x00 0E01h	DSP_DMA_GTCR	Global Timeout Control Register	16	R/W	0000h
0x00 0E02h	DSP_DMA_GSCR	Global Software Incompatible Control Register	16	R/W	0000h

Table 3−71. DSP Timer1 Registers

DSP WORD ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 2800h	DSP_TMR1_CNTL	DSP Timer1 Control Register	16	R/W	0000h
0x00 2802h	DSP_TMR1_LOAD_LO	DSP Timer1 Load Register Low	16	W	undef
0x00 2803h	DSP_TMR1_LOAD_HI	DSP Timer1 Load Register High	16	W	undef
0x00 2804h	DSP_TMR1_READ_LO	DSP Timer1 Read Register Low	16	R	undef
0x00 2805h	DSP_TMR1_READ_HI	DSP Timer1 Read Register High	16	R	undef

Table 3−72. DSP Timer2 Registers

DSP WORD ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 2C00h	DSP_TMR2_CNTL	DSP Timer2 Control Register	16	R/W	0000h
0x00 2C02h	DSP_TMR2_LOAD_LO	DSP Timer2 Load Register Low	16	W	undef
0x00 2C03h	DSP_TMR2_LOAD_HI	DSP Timer2 Load Register High	16	W	undef
0x00 2C04h	DSP_TMR2_READ_LO	DSP Timer2 Read Register Low	16	R	undef
0x00 2C05h	DSP_TMR2_READ_HI	DSP Timer2 Read Register High	16	R	undef

Table 3−73. DSP Timer3 Registers

DSP WORD ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 3000h	DSP_TMR3_CNTL	DSP Timer3 Control Register	16	R/W	0000h
0x00 3002h	DSP_TMR3_LOAD_LO	DSP Timer3 Load Register Low	16	W	undef
0x00 3003h	DSP_TMR3_LOAD_HI	DSP Timer3 Load Register High	16	W	undef
0x00 3004h	DSP_TMR3_READ_LO	DSP Timer3 Read Register Low	16	R	undef
0x00 3005h	DSP_TMR3_READ_HI	DSP Timer3 Read Register High	16	R	undef

Table 3−74. DSP Watchdog Timer Registers

DSP WORD ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 3400h	DSP_WD_CNTL_TIMER	DSP Watchdog Control Timer	16	R/W	0E02h
0x00 3402h	DSP_WD_LOAD_TIMER	DSP Watchdog Load Timer	16	W	FFFFh
0x00 3402h	DSP_WD_READ_TIMER	DSP Watchdog Read Timer	16	R	FFFFh
0x00 3404h	DSP_WD_TIMER_MODE	DSP Watchdog Timer Mode	16	R/W	8000h

Table 3−75. DSP Level 2.0 Interrupt Handler Registers

DSP WORD ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 4800h	DSP_L2_ITR	Interrupt Register	16	RW	0000h
0x00 4802h	DSP_L2_MIR	Mask Interrupt Register	16	RW	FFFFh
0x00 4804h	DSP_L2_SIR_IRQ_CODE	IRQ Interrupt Encoded Source Register	16	R	0000h
0x00 4806h	DSP_L2_SIR_FIQ_CODE	FIQ Interrupt Encoded Source Register	16	R	0000h
0x00 4808h	DSP_L2_CONTROL_REG	Interrupt Control Register	16	RW	0000h
0x00 480Ah	DSP_L2_ISR	Software Interrupt Set Register	16	RW	0000h
0x00 480Ch	DSP_L2_ILR0	Interrupt 0 Priority Level Register	16	RW	0000h
0x00 480Eh	DSP_L2_ILR1	Interrupt 1 Priority Level Register	16	RW	0000h
0x00 4810h	DSP_L2_ILR2	Interrupt 2 Priority Level Register	16	RW	0000h
0x00 4812h	DSP_L2_ILR3	Interrupt 3 Priority Level Register	16	RW	0000h
0x00 4814h	DSP_L2_ILR4	Interrupt 4 Priority Level Register	16	RW	0000h
0x00 4816h	DSP_L2_ILR5	Interrupt 5 Priority Level Register	16	RW	0000h
0x00 4818h	DSP_L2_ILR6	Interrupt 6 Priority Level Register	16	RW	0000h
0x00 481Ah	DSP_L2_ILR7	Interrupt 7 Priority Level Register	16	RW	0000h
0x00 481Ch	DSP_L2_ILR8	Interrupt 8 Priority Level Register	16	RW	0000h
0x00 481Eh	DSP_L2_ILR9	Interrupt 9 Priority Level Register	16	RW	0000h
0x00 4820h	DSP_L2_ILR10	Interrupt 10 Priority Level Register	16	RW	0000h
0x00 4822h	DSP_L2_ILR11	Interrupt 11 Priority Level Register	16	RW	0000h
0x00 4824h	DSP_L2_ILR12	Interrupt 12 Priority Level Register	16	RW	0000h
0x00 4826h	DSP_L2_ILR13	Interrupt 13 Priority Level Register	16	RW	0000h
0x00 4828h	DSP_L2_ILR14	Interrupt 14 Priority Level Register	16	RW	0000h
0x00 482Ah	DSP_L2_ILR15	Interrupt 15 Priority Level Register	16	RW	0000h

Table 3−76. DSP Interrupt Interface Registers

DSP WORD ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 3800h	ET_LS_CTRL_HI	Edge Triggered/Level Sensitive Control Register High	16	R/W	0000h
0x00 3801h	ET_LS_CTRL_LO	Edge Triggered/Level Sensitive Control Register Low	16	R/W	0000h
0x00 3800h	RST_LVL_HI	Reset Level Control Register High	16	R/W	0000h
0x00 3801h	RST_LVL_LO	Reset Level Control Register Low	16	R/W	0000h

Table 3−77. DSP Level 2.1 Interrupt Handler Registers

DSP WORD ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 4C00h	DSP_L21_ITR	Interrupt Register	16	R/W	0000h
0x00 4C02h	DSP_L21_MIR	Mask Interrupt Register	16	R/W	FFFFh
0x00 4C08h	DSP_L21_SIR_IRQ_CODE	IRQ Interrupt Encoded Source Register	16	R	0000h
0x00 4C0Ah	DSP_L21_SIR_FIQ_CODE	FIQ Interrupt Encoded Source Register	16	R	0000h
0x00 4C0Ch	DSP_L21_CONTROL_REG	Interrupt Control Register	16	R/W	0000h
0x00 4C0Eh	DSP_L21_ILR0	Interrupt 0 Priority Level Register	16	R/W	0000h
0x00 4C10h	DSP_L21_ILR1	Interrupt 1 Priority Level Register	16	R/W	0000h
0x00 4C12h	DSP_L21_ILR2	Interrupt 2 Priority Level Register	16	R/W	0000h
0x00 4C14h	DSP_L21_ILR3	Interrupt 3 Priority Level Register	16	R/W	0000h
0x00 4C16h	DSP_L21_ILR4	Interrupt 4 Priority Level Register	16	R/W	0000h
0x00 4C18h	DSP_L21_ILR5	Interrupt 5 Priority Level Register	16	R/W	0000h
0x00 4C1Ah	DSP_L21_ILR6	Interrupt 6 Priority Level Register	16	R/W	0000h
0x00 4C1Ch	DSP_L21_ILR7	Interrupt 7 Priority Level Register	16	R/W	0000h
0x00 4C1Eh	DSP_L21_ILR8	Interrupt 8 Priority Level Register	16	R/W	0000h
0x00 4C20h	DSP_L21_ILR9	Interrupt 9 Priority Level Register	16	R/W	0000h
0x00 4C22h	DSP_L21_ILR10	Interrupt 10 Priority Level Register	16	R/W	0000h
0x00 4C24h	DSP_L21_ILR11	Interrupt 11 Priority Level Register	16	R/W	0000h
0x00 4C26h	DSP_L21_ILR12	Interrupt 12 Priority Level Register	16	RW	0000h
0x00 4C28h	DSP_L21_ILR13	Interrupt 13 Priority Level Register	16	R/W	0000h
0x00 4C2Ah	DSP_L21_ILR14	Interrupt 14 Priority Level Register	16	R/W	0000h
0x00 4C2Ch	DSP_L21_ILR15	Interrupt 15 Priority Level Register	16	R/W	0000h

3.3.4.2 DSP Configuration Registers

The DSP Private Registers include the following:

- DSP TIPB Bridge Configuration Register
- DSP EMIF Configuration Registers
- DSP I-CACHE Registers
- DSP Clock Mode Registers
- DSP TIPB Bus Switch Registers

Table 3−78. DSP TIPB Bridge Configuration Register

DSP WORD ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 0000	DSP_CMR	DSP Control Mode Register	32	R/W	5555 5555h

Table 3−79. DSP EMIF Configuration Registers

DSP WORD ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 0800	DSP_EMIF_CNTL	DSP EMIF Global Control Register	16	R/W	0000h
0x00 0801	DSP_EMIF_GRR	DSP EMIF Global Reset Register	16	W	xxxxh

Table 3−80. DSP I-Cache Registers

DSP WORD ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 1400	DSP_ICACHE_GCR	DSP ICache Global Control Register	16	R/W	0004h
0x00 1401	DSP_ICACHE_FLAR0	DSP ICache Flush Line Address Register 0	16	R/W	0000h
0x00 1402	DSP_ICACHE_FLAR1	DSP ICache Flush Line Address Register 1	16	R/W	0000h
0x00 1403	DSP_ICACHE_NWCR	DSP ICache N Way Control Register	16	R/W	0001h
0x00 1404	DSP_ICACHE_SR	DSP ICache Status Register	16	R/W	0000h
0x00 1405	DSP_ICACHE_R1_CR	DSP ICache 1/2 Ramset 1 Control Register	16	R	0001h
0x00 1406	DSP_ICACHE_R1_TR	DSP ICache 1/2 Ramset 1 Tag Register	16	R/W	0000h
0x00 1407	DSP_ICACHE_R2_CR	DSP ICache 1/2 Ramset 2 Control Register	16	R/W	0001h
0x00 1408	DSP_ICACHE_R2_TR	DSP ICache 1/2 Ramset 2 Tag Register	16	R/W	0000h

Table 3−81. DSP Clock Mode Registers

DSP WORD ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 4000	DSP_CKTL	DSP Clock Control Register	16	R/W	0190h
0x00 4002	DSP_IDLCT1	DSP Idle Control 1 Register	16	R/W	0040h
0x00 4004	DSP_IDLCT2	DSP Idle Control 2Register	16	R/W	0000h
0x00 4006		Reserved			
0x00 4008		Reserved			
0x00 400A	DSP_RSTCT2	DSP Reset Control 2 Register	16	R/W	0000h
0x00 400C	DSP_SYSST	DSP System Information Register	16	R/W	0000h

Table 3−82. DSP TIPB Bus Switch Registers

DSP WORD ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 E400	DSP_UART1_SSW_CONF	UART1 Peripheral Ownership Register	32	R/W	0000 00001h
0x00 E410	DSP_UART2_SSW_CONF	UART2 Peripheral Ownership Register	32	R/W	0000 00001h
0x00 E420	DSP_UART3_SSW_CONF	UART3 Peripheral Ownership Register	32	R/W	0000 00001h
0x00 E448	DSP_MCBSP2_SSW_CONF	MCBSP2 Peripheral Ownership Register	32	R/W	0000 00001h
0x00 E450	DSP_I2C_SSW_CONF	I2C Peripheral Ownership Register	32	R/W	0000 00001h
0x00 E458	DSP_SPI_SSW_CONF	SPI Peripheral Ownership Register	32	R/W	0000 00001h
0x00 E460	DSP_GPTIMER1_SSW_CONF	GPTIMER1 Peripheral Ownership Register	32	R/W	0000 00001h
0x00 E468	DSP_GPTIMER2_SSW_CONF	GPTIMER2 Peripheral Ownership Register	32	R/W	0000 00001h
0x00 E470	DSP_GPTIMER3_SSW_CONF	GPTIMER3 Peripheral Ownership Register	32	R/W	0000 00001h
0x00 E478	DSP_GPTIMER4_SSW_CONF	GPTIMER4 Peripheral Ownership Register	32	R/W	0000 00001h
0x00 E480	DSP_GPTIMER5_SSW_CONF	GPTIMER5 Peripheral Ownership Register	32	R/W	0000 00001h
0x00 E488	DSP_GPTIMER6_SSW_CONF	GPTIMER6 Peripheral Ownership Register	32	R/W	0000 00001h
0x00 E498	DSP_GPTIMER7_SSW_CONF	GPTIMER7 Peripheral Ownership Register	32	R/W	0000 00001h
0x00 E4A0	DSP_GPTIMER8_SSW_CONF	GPTIMER8 Peripheral Ownership Register	32	R/W	0000 00001h
0x00 E4A8		Reserved			
0x00 E4B0	DSP_MMCSD2_SSW_CONF	MMC/SDIO 2 Peripheral Ownership Register	32	R/W	0000 00001h

3.4 DSP External Memory (Managed by MMU)

When the DSP MMU is off, the 24 address lines are directly copied to the traffic controller without any modification. There is no virtual-to-physical address translation. All the addresses between 0x05 0000 and 0x00FF 8000 (0x00FF FFFF if DSP bit MP/$\overline{MC}$ = 1) are redirected to the first sector of Flash (CS0) in the shared memory space (shared by MPU and DSP). See Figure 3−2.

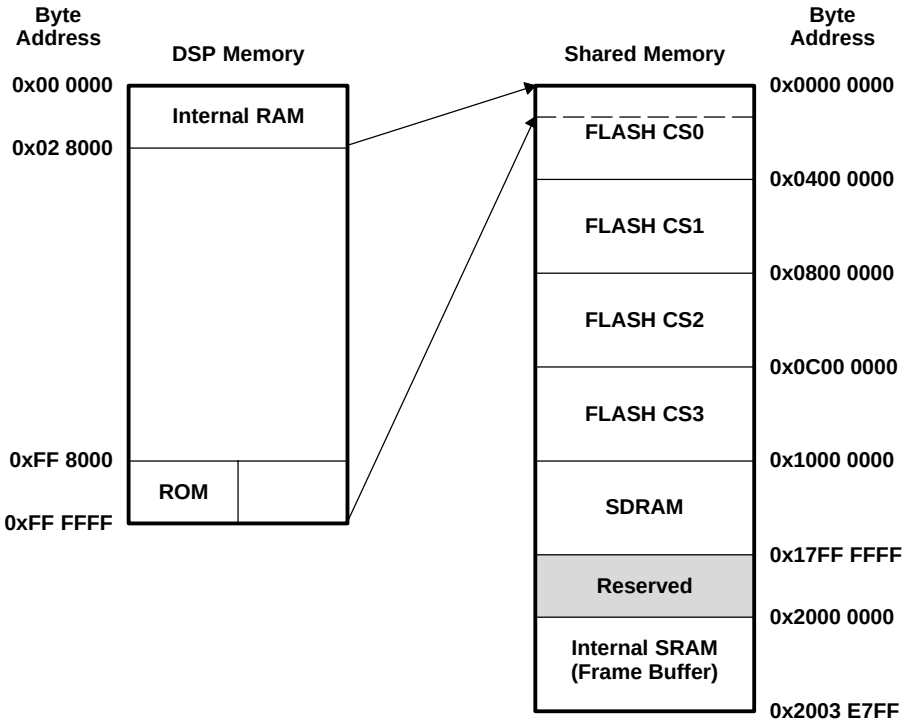


Figure 3−2. DSP MMU Off

When the DSP MMU is on, the 24 address lines (virtual address) are relocated within a physical 32-bit address by the DSP MMU. The DSP MMU is controlled by the MPU. If the DSP MMU is off, the DSP cannot see the MPU address 0x0000 0000. See Figure 3−3.

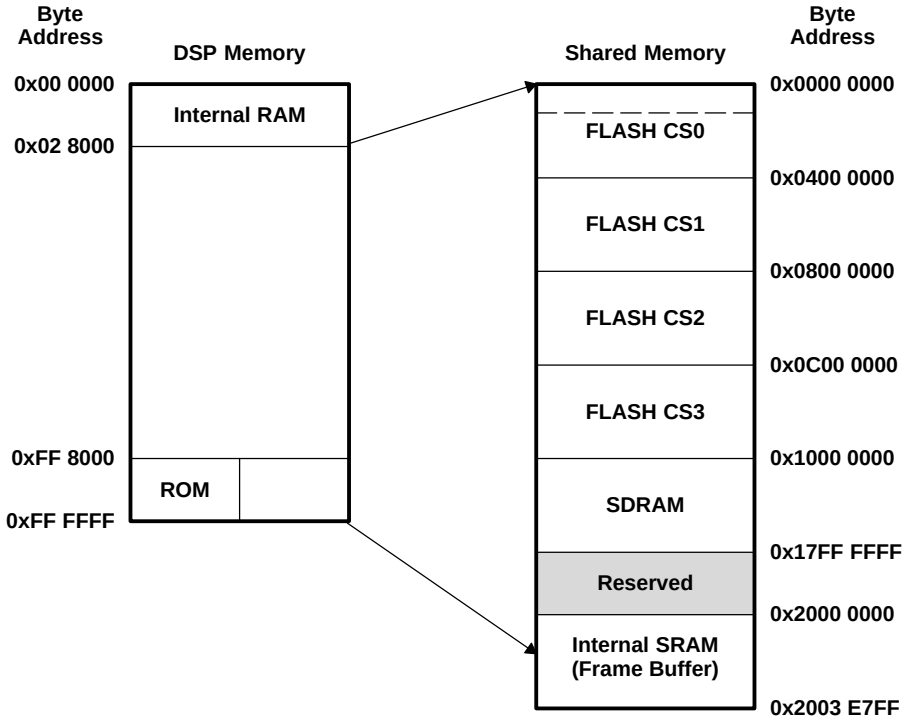


Figure 3−3. DSP MMU On

3.5 MPU and DSP Private Peripherals

The MPU and DSP each have their own separate private peripheral bus. Peripherals on each of these private buses may only be accessed by their respective processors.

3.5.1 Timers

The MPU and DSP have three 32-bit timers available on their respective private TIPBs. These timers are used by the operating system to provide general-purpose housekeeping functions or, in the case of the DSP, to also provide synchronization of real-time processing functions. These timers can be configured either in autoreload or one-shot mode with on-the-fly read capability. The timers generate an interrupt to the respective processor (MPU or DSP) when the timer down-counter is equal to zero.

3.5.2 Watchdog Timer

The MPU and DSP each have a single watchdog timer. Each watchdog timer can be configured as either a watchdog timer or a general-purpose timer.

A watchdog timer requires that the MPU or DSP software or OS periodically write to the appropriate WDT count register before the counter underflows. If the counter underflows, the WDT generates a reset to the appropriate processor (MPU or DSP). The DSP WDT resets only the DSP processor while the MPU WDT resets both processors (MPU and DSP). The watchdog timers are useful for detecting user programs that are stuck in an infinite loop, resulting in loss of program control or in a runaway condition.

When used as a general-purpose timer, the WDT is a 16-bit timer configurable either in autoreload or one-shot mode with on-the-fly read capability. The timer generates an interrupt to the respective processor (MPU or DSP) when the timer's down-counter is equal to zero.

3.5.3 Interrupt Handlers

The MPU and DSP have two levels of interrupt handling each, allowing up to 160 interrupts on the MPU and 98 interrupts on the DSP. This is necessary because of the large number of integrated peripherals on the OMAP5912 device. Some peripherals can generate interrupts to both processors.

3.5.4 LCD Controller (MPU Only)

The OMAP5912 devices include an LCD controller that interfaces with most industry-standard LCD displays. The LCD controller is configured by the MPU and utilizes a dedicated channel on the system DMA to transfer data from the frame buffer. The frame buffer can be implemented using external SDRAM via the EMIFF. Using the frame buffer as its data source, the system DMA must provide data to the FIFO at the front end of the LCD controller data path at a rate sufficient to support the chosen display mode and resolution. Optimal performance is achieved when using the internal SRAM as the frame buffer.

The panel size is programmable and can be any width (line length) from 16 to 1024 pixels in 16-pixel increments. The number of lines is set by programming the total number of pixels in the LCD. The total frame size is programmable up to 1024 $\times$ 1024; however, frame sizes and frame rates supported in specific applications depend upon the available memory bandwidth allowed by the specific application as well as the maximum configurable pixel clock rate.

The screen is intended to be mapped to the frame buffer as one contiguous block where each horizontal line of pixels is mapped to a set of consecutive bytes of words in the frame memory.

The main features of the LCD controller are:

- Dedicated 64-entry × 16-bit FIFO
- Dedicated LCD DMA channel for LCD display
- Programmable display including support for 2-, 4-, 8-, 12-, and 16-bit graphics modes
- Programmable display resolutions up to 1024 pixels by 1024 lines (assuming sufficient system bandwidth)
- Support for passive monochrome (STN) displays
- Support for passive color (STN) displays
- Support for active color (TFT) displays
- Patented dithering algorithm, providing:
  - 15 grayscale levels for monochrome passive displays
  - 3375 colors for color passive displays
  - 65536 colors for active color displays
  - 256-entry × 12-bit palette
- Programmable pixel rate
- Pixel clock plus horizontal and vertical synchronization signals
- ac-bias drive signal
- Active display enable signal

3.5.5 LCDCONV (MPU Only)

This module enables to provide a 16-bit to 18-bit LCD data conversion to the LCD interface. It supports two operating modes:

- 16-bit LCD mode
- 18-bit LCD mode

The mode switching is done by software by setting a dedicated bit in its control register. The software is also able to know which mode is currently in use by looking in a status register. When 16-bit LCD mode is used, the module operates in bypass mode, where all the 16-bit LCD pixel data coming from the frame buffer is directly provided to an external LCD interface. When the 18-bit LCD mode is used, the 16-bit LCD pixel signal is converted to an 18-bit LCD pixel signal through a Red, Green, Blue color (RGB) lookup table. Then the 18-bit LCD pixel format adds a LSB bit to the R (coding Red color) and B (Blue color) signals.

3.5.6 Random Number Generator (RNG) (MPU Only)

The MPU secure features include a random-number-generator (RNG) module that provides a true, nondeterministic noise source for the purpose of generating keys, initializing vectors (IVs), and other random-number requirements. It is designed for FIPS 140-1 compliance 43, facilitating system certification to this security standard. It also includes built-in self-test (BIST) logic that allows for the testing of the randomness of the module output and its compliance with FIPS 140-1 standard. An ANSI X9.17, annex C post-processor is available to meet the NIST requirements of FIPS 140-1.

The RNG module is made of a hardware-based nondeterministic random-number-generator core and a wrapper, which provides bus interface, clock, reset, and test features.

NOTES:

- It takes 160 RNG clock cycles to generate a new key.
- After each host read access to the key output register, a new key starts to be completed.

3.5.7 DES/3DES (MPU Only)

The DES/3DES module provides hardware-accelerated data encryption/decryption functions. It can run either the single DES algorithm or the triple DES algorithm in compliance with FIPS 46-3 standard. It supports electronic codebook (ECB) and cipher-block chaining (CBC) modes of operation. It does not support the cipher-feedback (CF) and the output-feedback (OFB) modes of operation in hardware.

The DES/3DES module includes the following features:

- 8-byte input and output buffers
- 56-bit key size, plus 8-bit error detection per key (up to 3 keys)
- 16 (DES) round cycles per 8 bytes of data block
- 48 (3DES) round cycles per 8 bytes of data block
- Write and read DMA channels
- MPU write and read
- No IRQs

3.5.8 SHA1/MD5 (MPU Only)

The SHA1/MD5 security module provides hardware-accelerated hash functions. It can run either the SHA-1 algorithm in compliance with FIPS 180-1 standard, or the MD5 message-digest algorithm developed by Rivest in 1991. Up to 2^{27}-1 bytes (128M bytes) of data can be hashed in a single operation to produce a 160-bit signature in the case of SHA-1, and 128-bit signature in the case of MD5.

NOTE:

- The SHA-1 algorithm takes 80 steps per 512-bit block of data to be processed.
- The MD5 algorithm takes 64 steps per 512-bit block of data to be processed.
- Each step takes one clock cycle.
- Blocks are processed sequentially, which means that to start processing a new block, the accelerator must wait for the end of the previous 80 operation steps (for SHA-1, 64 for MD5) of the previous block.
- The SHA-1/MD5 can interface with a host or with a DMA.

3.6 MPU Public Peripherals

Peripherals on the MPU Public Peripheral bus may only be accessed by the MPU and the system DMA controller, which is configured by the MPU. This bus is called a public bus because it is accessible by the system DMA controller. The DSP cannot access peripherals on this bus.

3.6.1 USB Interface

The OMAP5912 processor provides several varieties of USB functionality, including:

- USB host: OMAP5912 provides a three-port USB Specification Revision 1.1-compliant host controller, which is based on the OHCI Specification for USB Release 1.0a.
- USB device: OMAP5912 provide a full-speed USB device.
- USB On-The-Go (OTG): OMAP5912 acts as an OTG dual-role device; the USB device functionality and one port of the USB host controller act in concert to provide an OTG port.

Flexible multiplexing of signals from the OMAP5912 USB host controller, USB function controller, and other peripherals allows for a wide variety of system-level USB capabilities. Many of the OMAP5912 pins can be used for USB-related signals or for signals from other peripherals. The top-level pin multiplexing controls each pin individually and allows for the selection of one of several possible internal pin signal interconnections.

When these shared pins are programmed for use as USB signals, the OMAP5912 USB signal multiplexing selects how the signals associated with the three OMAP5912 USB host ports and the OMAP5912 USB function controller can be brought out to OMAP5912 pins.

The USB host controller (HC) is a three-port controller that communicates with USB devices at low-speed (1.5M bit-per-second maximum) and full-speed (12M bit-per-second maximum) data rates. It is compatible with the Universal Serial Bus Specification Revision 2.0 and the OpenHCI − Open Host Controller Interface Specification for USB, Release 1.0a, which is available on the Internet, and is hereafter called the OHCI Specification for USB. It is assumed that users of the OMAP5912 USB host controller are already familiar with the USB Specification and OHCI Specification for USB.

The OMAP5912 OTG controller can use one of the USB host controller ports as part of a USB OTG-capable connection. When used for an OTG connection, the host controller port acts as the upstream device when OMAP5912 controls the OTG link, and the USB function controller acts as the downstream device when OMAP5912 acts as an OTG downstream device.

The USB host controller implements the register set and makes use of the memory data structures defined in the OHCI Specification for USB. These registers and data structures are the mechanism by which a USB host controller driver software package can control the USB host controller. The OHCI Specification for USB also defines how the USB host controller implementation must interact with those registers and data structures in system memory. The OMAP5912 MPU accesses these registers via the MPU public peripheral bus.

NOTE: USB 2.0 hi-speed is not supported.

3.6.2 Camera Interface

The camera interface is an 8-bit external port that can be used to accept data from an external camera sensor. The interface handles multiple image formats synchronized on vertical and horizontal synchronization signals. Data transfer to the camera interface can be done synchronously or asynchronously.

The camera interface module converts the 8-bit data transfers into 32-bit words and utilizes a 128-word buffer to facilitate efficient data transfer to memory. Data can be transferred from the camera interface buffer to internal memory by the system DMA controller or directly by the MPU.

This interface is accessible through the OCP-T1 or OCP-T2 port.

3.6.3 MICROWIRE Serial Interface

The MICROWIRE interface is a serial synchronous interface that can drive up to four serial external components. This interface is compatible with the MICROWIRE standard and is seen as the master.

MICROWIRE is typically used to transmit control and status information to external peripheral devices or to transmit data to or from small nonvolatile memories such as serial EEPROMs or serial flash devices.

3.6.4 Real-Time Clock (RTC)

The RTC peripheral provides an embedded real-time clock module that can be directly accessible from the MPU. The RTC peripheral is powered independently of the OMAP5912 MPU core power.

The RTC module has the following features:

- Time information (seconds/minutes/hours) directly in BCD code
- Calendar information (day/month/year/day of the week) directly in BCD code up to year 2099
- Interrupts generation, periodically (1s/1m/1h/1d period) or at a precise time of the day (alarm function)
- 30-s time correction
- Oscillator frequency calibration

3.6.5 Pulse-Width Tone (PWT)

The pulse-width tone (PWT) peripheral generates a modulated frequency signal for use with an external buzzer. The frequency is programmable between 349 Hz and 5276 Hz with 12 half-tone frequencies per octave. The volume level of the output is also programmable.

3.6.6 Pulse-Width Light (PWL)

The pulse-width light (PWL) peripheral allows the control of the backlight of the LCD and the keypad by employing a 4096-bit random sequence. This voltage level control technique decreases the spectral power at the modulator harmonic frequencies. The block uses a switchable 32-kHz clock, independent of UPLD.

3.6.7 Keyboard Interface

Keyboard is composed of specific MPUIOs dedicated for 6 x 5 or 8 x 8 keyboard connection:

- Eight inputs (KB.R[7:0]) for row lines
- Eight outputs (KB.C[7:0]) for column lines

The keyboard feature allows communication with a keyboard. The MPUIO or keyboard interface supports keyboards with up to eight rows and eight columns and has the capability to detect multiple key presses. A keyboard event is signaled to the host by an interrupt.

3.6.8 HDQ/1-Wire Interface

This module allows implementation of both HDQ and 1-Wire protocols. These protocols use a single wire to communicate between a master and a slave device. The HDQ/1-Wire pin is open-drain and requires an external pullup resistor.

HDQ and 1-Wire interfaces can be found on commercially available battery and power management devices. The interface can be used to send command and monitor its status between OMAP5912 and such devices.

3.6.9 Multimedia Card/Secure Digital (MMC/SDIO1) Interface

The MMC/SDIO1 host controller provides an interface between the MPU and MMC/SD/SDIO memory cards plus up to four serial flash cards, and it also handles MMC/SDIO transactions with minimum local host intervention. The following combinations of external devices are supported:

- One or more MMC memory cards sharing the same bus
- One single SD memory card or SDIO card

The application interface is responsible for managing transaction semantics; the MMC/SDIO1 host controller deals with MMC/SDIO protocol at transmission level, packing data, adding CRC, start/end bit and checking for syntactical correctness. SD mode wide bus width is also supported (1- or 4-bit data lines).

The application interface can send every MMC/SDIO command and either poll for the status of the adapter or wait for an interrupt request, which is sent back in case of exceptions or to notify for end of operations. The application interface can read card responses or flag register. It can also mask individually interrupt sources. All these operations can be performed reading and writing control registers. The MMC/SDIO1 peripheral also supports two DMA channels.The main features of the MMC/SDIO1 module are:

- Full compliance with MMC command/response sets as defined in the MMC standard specifications v.3.1
- Full compliance with SD command/response sets as defined in the SD physical layer specifications v.1.0
- Full compliance with SDIO command/response sets as defined in the SDIO card specification v1.0
- Flexible architecture, allowing support for new command structure

- Built-in 64-byte FIFO for buffered read or write
- 16-bit-wide access bus to maximize bus throughput
- Designed for low power
- Wide interrupt capability
- Programmable clock generation
- Two DMA channels

NOTE:

The MMC/SDIO1 interface includes all the MMC/SDIO pins except the direction controls (data and control).

3.6.10 MPUIO Interface

The MPUIO feature allows communication with an external device through as many as 16 MPUIOs. These MPUIOs can be configured on a pin-by-pin basis as inputs or outputs. When configured as input, each MPUIO can be individually selected to generate interrupts on a level change (rising or falling edge). In normal operation, the MPUIO inputs are latched at the falling edge of 32 kHz. In event capture mode, one of the MPUIO inputs can be assigned a clock source, and all the other inputs are latched on its falling edge. The polarity can be configured with the MPUIO_INT_EDGE_REG register.

The MPUIO module functional clock domain is clocked by the OMAP5912 32-kHz clock. This clock is always fed into the block, regardless of the state of the chip (awake, asleep, or idle). This allows external event latching and interrupt generation even when the system is in idle mode, to wake up the system via interrupt.

The MPUIO module interfaces with the host through a TIPB bus. The MPU peripheral clock resynchronizes register access to the module and avoids time-out on the TIPB bus caused by the functional clock being too slow.

3.6.11 LED Pulse Generators (LPG)

There are two separate LED pulse generator (LPG) modules. Each LPG module provides an output for an indication LED. The blinking period is programmable between 152 ms and 4 s or the LED can be switched on or off permanently.

3.6.12 Frame Adjustment Counter (FAC)

The frame adjustment counter (FAC) is a simple peripheral that counts the number of rising edges of one signal (start of frame interrupt of the USB function) during a programmable number of rising edges of a second signal (transmit frame synchronization of McBSP2). The FAC may only be used with these specific USB Function and McBSP2 signals. The count value can be used by system-level software to adjust the duration of the two time domains with respect to each other to reduce overflow and underflow. If the data being transferred is audio data, this module can be part of a solution that reduces pops and clicks. The FAC module generates one second-level interrupt to the MPU.

3.6.13 Operating System (OS) Timer

A programmable interval timer is required to generate a periodic interrupt, also called system clock tick, to the OS. This is used to keep track of the current time and to control the operation of device drivers.

Key functions are:

- Read current value of the timer
- Generate interrupt as the timer down-counts to zero
- Reset the interrupt by writing an 1 to the interrupt bit in the control register
- Timer interrupt period: Irq_rate = (Tick_value_reg + 1) / 32768
- Maximum tick value register is 0xFFFF, so maximum timer interrupt period is 2 sec.

3.7 DSP Public Peripherals

Peripherals on the DSP Public Peripheral bus are directly accessible by the DSP and DSP DMA. These peripherals may also be accessed by the MPU and System DMA Controller via the MPUI interface. The MPUI interface must be properly configured to allow this access.

3.7.1 Multichannel Buffered Serial Ports (McBSP1 and 3)

The multichannel buffered serial port (McBSP) provides a high-speed, full-duplex synchronous serial port that allows direct interface to audio codecs and various other system devices. The DSP public peripheral bus has access to two McBSPs: McBSP1 and McBSP3.

NOTE: All of the standard McBSP pins are not necessarily available on every McBSP on the OMAP5912 devices. In the case of the two DSP McBSPs, the following pins are available:

McBSP1 pins:

- CLKX (data bit clock)
- FSX (data bit frame sync)
- DX and DR (transmit and receive data)
- CLKS (external reference to sample rate generator)

McBSP3 pins:

- CLKX (transmit clock)
- FSX (transmit frame sync)
- DX and DR (transmit and receive data)

CLKX and FSX of McBSP1 and McBSP3 are used for both transmitting and receiving.

The functional clock to the McBSP1 and McBSP3 is fixed at the OMAP5912 base operating frequency (12, 13, or 19.2 MHz). The bit-clock rate for these McBSPs is therefore limited to 6, 6.5, or 9.6 MHz (one half the base frequency).

Only McBSP1 has the CLKS pin available. If the sample rate generator (SRG) is used on McBSP1, the reference clock to the SRG can be configured to be either an external reference provided on the CLKS pin, or the internal base (12, 13, or 19.2-MHz) device clock. However, if the SRG is used on McBSP3, the only reference clock available to this SRG is the base device clock as clock reference.

3.7.2 Multichannel Serial Interfaces (MCSI1 and 2)

The MCSI provides a flexible serial interface with multichannel transmission capability. The MCSI allows the DSP to access a variety of external devices, such as audio codecs and other types of analog converters. The DSP public peripheral bus has access to two MCSIs: MCSI1 and MCSI2. These MCSIs provide full-duplex transmission and master or slave clock control. All transmission parameters are configurable to cover the maximum number of operating conditions. The MCSIs have the following features:

- Master or slave clock control (transmitter clock and frame synchronization pulse)
  - Programmable transmitter clock frequency in master mode of up to one half the OMAP5912 base frequency (12,13, or 19.2 MHz)
  - Receiver clock frequency in slave mode of up to the base frequency (12,13, or 19.2 MHz)
- Single-channel or multichannel (x16) frame structure
- Programmable word length: 3 to 16 bits
- Full-duplex transmission
- Programmable frame configuration
  - Continuous or burst transmission
  - Normal or alternate framing
  - Normal or inverted frame and clock polarities
  - Short or long frame pulse
  - Programmable oversize frame length
  - Programmable frame length
- Programmable interrupt condition (TX and RX)
  - Error detection with interrupt generation on wrong frame length
  - System DMA support for both TX and RX data transfers

3.8 Shared Peripherals

The shared peripherals are connected to both the MPU Public Peripheral bus and the DSP Public Peripheral bus. Connections are achieved via a TI Peripheral Bus Switch, which must be configured to allow MPU or DSP access. The other shared peripherals have permanent connections to both public peripheral buses, although read and write accesses to each peripheral register may differ.

3.8.1 Mailbox Registers

Four sets of shared mailbox registers are available for communication between the DSP and MPU:

- Two reads/writes accessible by the MPU, read-only by the DSP
- Two reads/writes accessible by the DSP, read-only by the MPU

Each mailbox is implemented with 2×16-bit registers. When a processor writes to a register, it generates an interrupt; this interrupt is released by a read access by the other processor.

These registers are discussed further in Section 3.12, Interprocessor Communication.

3.8.2 General-Purpose Timers

OMAP5912 consists of eight 32-bit timers with the following features:

- Counter timer with compare and capture modes
- Autoreload mode
- Start-stop mode
- Programmable divider clock source
- 16-/32-bit addressing
- On-the-fly read/write registers
- Interrupts generated on overflow and compare
- Interrupt enable
- Wake-up enable
- Write posted mode
- Dedicated input trigger for capture mode and dedicated output trigger/PWM signal

Each timer module contains a free-running upward counter with autoreload capability on overflow. The timer counter can be read and written on-the-fly (while counting). The timer module includes compare logic to allow interrupt event on programmable counter matching value. A dedicated output signal can be pulsed or toggled on overflow and match event. This offers timing stamp trigger signal or PWM (pulse width modulation) signal sources. A dedicated input signal can be used to trigger automatic timer counter capture and interrupt event, on programmable input signal transition type. A programmable clock divider (prescaler) allows reduction of the timer input clock frequency. All internal timer interrupt sources are merged into one module interrupt line and one wake-up line. Each internal interrupt sources can be independently enabled/disabled with a dedicated bit of the TIER register for the interrupt features and a dedicated bit of TWER for the wake-up.

Each timer has three possible clock sources:

- the 32-kHz clock
- the system clock
- an external clock source

NOTE:

- Three of the eight dual-mode timer PWM outputs are connected at OMAP5912 I/Os. Two of the eight dual-mode timer input capture are connected at OMAP5912 I/Os. The system clock can come either from OMAP or directly from the input clock.
- Can wake up the system when the clock is configured as 32-kHz through its own interrupt through a general-purpose timer

3.8.3 Serial Port Interface (SPI)

The serial port interface is a bidirectional, four-line interface with:

- the clock used to shift-in and shift-out data
- the device enable
- the data input
- the data output

This serial port interface is based on a looped shift-register, thus allowing both transmit and receive modes. It can operate either in master or slave mode, using MPU or DMA control.

In master mode, the SPI provides up to four chip-selects for external devices. In slave mode, the SPI has its own chip-select.

In master mode, the maximum SPI data rate is the same as the system clock frequency; in slave mode, the clock of the serial data out is provided by an external device at lower data rate.

3.8.4 Universal Asynchronous Receiver/Transmitter (UART)

The OMAP5912 includes three universal asynchronous receiver/transmitter (UART) peripherals which are accessible on the DSP public and MPU public peripheral buses. All three UARTs are standard 16C750-compatible UARTs implementing an asynchronous transfer protocol with various flow control options. UART1 and UART3 can function as general UART or can optionally function as IrDA interface.

NOTE:

Unlike dual-mode timers, the UART is a “dynamically” shared peripheral and does not have any configuration (switch) register.

The clock source for the UART1 and UART3 is:

- APLL output

The clock source for the UART2 can be:

- system clock or the sleep clock
- APLL output

The main features of the UART peripherals include:

- Selectable UART/autobaud modes
- Dual 64-entry FIFOs for received and transmitted data payload

- Programmable and selectable transmit and receive FIFO trigger levels for DMA and interrupt generation
- Programmable sleep mode
- Complete status-reporting capabilities in both normal and sleep mode
- Frequency prescaler values from 0 to 65535 to generate the variable baud rates
- Baud rate from 300 bits/s up to 1.5M bits/s
- Autobauding between 1200 bits/s and 115.2K bits/s
- Software/hardware flow control
  - Programmable XON/XOFF characters
  - Programmable auto-RTS and auto-CTS
- Programmable serial interface characteristics
  - 5-, 6-, 7-, or 8-bit characters
  - Even-, odd-, or no-parity bit generation and detection
  - 1, 1.5, or 2 stop-bit generation
  - False start bit detection
  - Line break generation and detection
- Internal test and loopback capabilities
- Modem control functions (CTS, RTS, DSR, DTR)

  NOTE: DSR and DTR are not available on UART2.

The key features of the IrDA mode (UART1 and 3) are:

- Support of slow infrared (SIR) configuration (baud rate up to 115.2Kbauds)
- Support of medium infrared (MIR) configuration (baud rate 0.576Mbits/s, and 1.152Mbits/s in the following range [1.1508Mbits/s to 1.1532Mbits/s])
- Support of fast infrared (FIR) configuration (baud rate at 4Mbauds, the effective frequency baud rate is 8Mbits/s in the following range [7.9992Mbits/s to 8.0008Mbits/s])
- Frame formatting: addition of variable xBOF characters and EOF characters
- Uplink/downlink CRC generation/detection
- Asynchronous transparency (automatic insertion of break character)
- 8-entry status FIFO available to monitor frame length and frame errors

3.8.5 I²C Master/Slave Interface

The I²C peripheral provides an interface between a local host (LH) (e.g., MPU, DSP or system DMA) and I²C-bus compatible devices. External components can serially transmit/receive up to 8 bits of data to/from the LH device through the I²C interface.

The I²C peripheral supports multimaster mode, which allows multiple devices to control the bus. Each I²C device is recognized by a unique address and can operate as either transmitter or receiver, depending on its function. Furthermore, the device connected to the I²C bus can also be considered a master or a slave when performing data transfers. A master device generates the clock signals to initiate a data transfer. A slave device is addressed by this master during the data transfer.

The I²C interface with the local host is compliant with 8-/16-bit OCP protocol. The interface clock and the functional clock are independent. The I²C master/slave interface supports the following features:

- Compliant to Philips I²C-bus specification version 2.1
- Support standard mode (up to 100K bits/s) and fast mode (up to 400K bits/s)
- In the master only I²C operating mode of OMAP5912, standard mode is supported up to 83K bits/s.
- 7-bit and 10-bit device addressing modes
- General call
- Start/restart/stop
- Multimaster transmitter/slave receiver mode
- Multimaster receiver/slave transmitter mode
- Combined master transmit/receive and receive/transmit mode
- Built-in FIFO for buffered read or write
- Module enable/disable capability
- Programmable clock generation
- Two DMA channels

The I²C master/slave interface does not support the following features:

- High-speed (HS) mode for transfer rates up to 3.4M bits
- C-bus compatibility mode

3.8.6 Multichannel Buffered Serial Port (McBSP2)

The multichannel buffered serial port (McBSP) provides a high-speed, full-duplex serial port that allows direct interface to audio codecs, and various other system devices. The McBSP provides:

- Full-duplex communication
- Double-buffer data registers, which allow a continuous data stream
- Independent framing and clocking for receive and transmit

In addition, the McBSP has the following capabilities:

- Direct interface to:
  - T1/E1 framers
  - MVIP switching-compatible and ST-BUS compliant devices
  - IOM-2 compliant device
  - AC97-compliant device
  - I2S-compliant device
  - Serial peripheral interface (SPI)
- Multichannel transmit and receive of up to 128 channels per frame
- A variety of data sizes, including: 8, 12, 16, 20, 24, or 32 bits
- μ-law and A-law companding
- Programmable polarity for both frame synchronization and data clocks
- Programmable internal clock and frame generation

  NOTE: All of the standard McBSP signals are not necessarily available on every McBSP on the OMAP5912 device.

In the case of the MPU McBSP2, the following pins are available:

- CLKX and CLKR (transmit and receive clocks)
- FSX and FSR (transmit and receive frame syncs)
- DX and DR (transmit and receive data)

The functional clock to the McBSP2 peripheral is configurable to the DPLL clock rate with a divider of 1, 2, 4, or 8. McBSP2 does not have a CLKS external clock reference pin. Therefore, if the McBSP2 sample rate generator (SRG) is used, the only reference clock available to the SRG is a programmable clock from the MPU domain.

3.8.7 Multimedia Card/Secure Digital (MMC/SDIO2) Interface

The MMC/SDIO2 host controller provides an interface between OMAP5912 and MMC/SD/SDIO memory cards, and handles MMC/SD transactions with minimum local host intervention. The following combinations of external devices are supported:

- One or more MMC memory cards sharing the same bus
- One single SD memory card or SDIO card

The application interface is responsible for managing transaction semantics; the MMC/SDIO2 host controller deals with MMC/SDIO protocol at transmission level, packing data, adding CRC, start/end bit and checking for syntactical correctness. SD mode wide bus width is also supported (1- or 4-bit data lines).

The application interface can send every MMC/SDIO command and either poll for the status of the adapter or wait for an interrupt request, which is sent back in case of exceptions or to warn for end of operations. The application interface can read card responses or flag register. It can also mask individually interrupt sources. All these operations can be performed reading and writing control registers. The MMC/SDIO2 peripheral also supports two DMA channels.

The main features of the MMC/SDIO2 module are:

- Full compliance with MMC command/response sets as defined in the MMC standard specifications v.3.1
- Full compliance with SD command/response sets as defined in the SD physical layer specifications v.1.0
- Full compliance with SDIO command/response sets as defined in the SDIO card specification v1.0
- Flexible architecture, allowing support for new command structure
- Built-in 64-byte FIFO for buffered read or write
- 16-bit-wide access bus between MMC/SDIO2 interface and the local hosts to maximize bus throughput
- Designed for low power
- Wide interrupt capability
- Programmable clock generation
- Two DMA channels
- The MMC2 provides auxiliary signals for external level shifters. MMC2.CMDDIR indicates the direction of the MMC2.CMD signal. MMC2.DATDIR0 and MMC2.DATDIR1 indicate the direction of the MMC2.DAT0 signal and MMC2.DAT[3:1] signals, respectively.

NOTE:

- The MMC/SDIO2 clock is multiplexed between the 48-MHz clock (APLL output) and the system clock (19.2 MHz or 12 MHz).
- At reset, the MMC/SDIO2 clock selection is the system clock.
- The MMC/SDIO2 module is routed at the OMAP5912 level. The OMAP5912 configuration selects only the part of the interface which is required.

3.8.8 General-Purpose I/O (GPIO)

OMAP5912 includes 4 GPIO peripherals of 16 GPIO pins each. There are up to 64 shared GPIO pins. Each GPIO pin is independently configurable as either input or output. If configured as input, each pin can be configurable to generate an interrupt upon detection of its signal level change. As both the MPU and the DSP can access the GPIO, consideration must be taken for its arbitration.

The general-purpose input/output (GPIO) peripheral can be used for the following types of applications:

- Input/output data
- Generation of an interrupt in active mode upon the detection of external events
- Generation of a wake-up request in idle mode upon the detection of external events

3.8.9 32-kHz Synchro Counter

This is a 32-bit simple counter, clocked by the falling edge of the 32-kHz clock. It is reset while the Power Up Reset ($\overline{\text{PWRON\_RESET}}$) primary I/O is active (main OMAP5912 reset), then on the rising edge of $\overline{\text{PWRON\_RESET}}$ ($\overline{\text{PWRON\_RESET}}$ release), it starts to count indefinitely. When the highest value is reached, it wraps back to zero and starts running again.

MPU and DSP have the capability to read the count value at higher frequency from the peripheral interface. The MPU can read it from a 32-bit peripheral access, whereas the DSP can only access it through two consecutive 16-bit accesses.

3.9 System DMA Controller

The system direct memory access (DMA) controller transfers data between points in the memory space without intervention by the MPU. The system DMA allows movements of data to and from internal memory, external memory, and peripherals to occur in the background of MPU operation. It is designed to off-load the block data transfer function from the MPU processor. The system DMA is configured by the MPU via the MPU private peripheral bus.

System DMA consists of:

- Seventeen logical channels
- Seven physical ports + one for configuration
- Four physical channels

The ports are connected to the L3 OCP targets, the external memory, the TIPB bridge, the MPUI, and one dedicated port connected to an LCD controller. The system DMA controller can be controlled via the MPU private TIPB or by an external host via the OCP-I port. The system DMA controller is designed for low-power operation. It is partitioned into several clock domains where each clock domain is enabled only when it is used. All clocks are disabled when no DMA transfers are active (synchronous to the MPU TIPB, this feature is totally under hardware control; no specific programming is needed). Five different logical channels types are supported; each one represents a specific feature set:

- LCh-2D for memory-to-memory transfers, 1D and 2D
- LCh-P for peripheral transfers
- LCh-PD for peripheral transfers on a dedicated channel
- LCh-G for graphical transfers/operations
- LCh-D for display transfers

The available features are:

- Support for up to four address modes:
  - Constant
  - Post-increment
  - Single indexing
  - Double indexing
- Different indexing for source-respective destination
- Logical channel chaining
- Software triggering
- Hardware triggering
- Logical channel interleaving
- Logical channel preemption
- Two choices of logical channel arbitration of physical resources: round robin or fixed
- Two levels of logical channel priority
- Constant fill
- Transparent copy
- Rotation 0, 90, 180, and 270

There are seven ports enabling:

- Memory-to-memory transfers
- Peripheral-to-memory transfers
- Memory-to-peripheral transfers
- Peripheral-to-peripheral transfers
- Binary backward-compatible by default configuration
- Up to four logical channels active in parallel

The logical channel dedicated to the display, LCh-D, has several additional features:

- Channel can be shared by two LCD controllers
- Supports both single- and dual-block modes
- Supports separate indexing and numbering for dual-block mode for both elements and frames

3.10 DSP DMA Controller

The DSP subsystem has its own dedicated DMA controller, which is entirely independent of the MPU or the system DMA controller. The DSP DMA controller has many of the same major features as the system DMA controller.

The DSP DMA Controller has six generic channels and five physical ports available for source or destination data. These five ports are the SARAM port, DARAM port, EMIF (external memory port), DSP TIPB port, and MPUI port. The DSP may configure the DSP DMA controller to transfer data between the SARAM, DARAM, EMIF, and TIPB ports; but the MPUI port is a dedicated port used for MPU or system DMA initiated transfers to DSP subsystem resources. The SARAM and DARAM ports are used to access local DSP memories and the TIPB port is used to access the registers of the DSP peripherals. The EMIF port of the DSP DMA controller is used to access the Traffic Controller via the DSP MMU (Memory Management Unit).

3.11 Traffic Controller (Memory Interfaces)

The traffic controller (TC) manages all accesses by the MPU, DSP, system DMA, and local bus to the OMAP5912 system memory resources. The TC provides access to three different memory interfaces: external memory interface slow (EMIFS), external memory interface fast (EMIFF), and internal memory interface (OCP T1). The OCP T1 allows access to the 250K bytes of on-chip frame buffer. The EMIFS provides 16-bit-wide access to asynchronous or synchronous memories or devices.

The EMIFF provides 16-bit-wide access to SDR, mobile SDR, and mobile DDR memories.

The TC provides the functions of arbitrating contending accesses to the same memory interface from different initiators (MPU, DSP, system DMA, local bus), synchronization of accesses due to the initiators and the memory interfaces running at different clock rates, and the buffering of data allowing burst access for more efficient multiplexing of transfers from multiple initiators to the memory interfaces.

The TC architecture allows simultaneous transfers between initiators and different memory interfaces without penalty. For instance, if the MPU is accessing the EMIFF at the same time the DSP is accessing the IMIF, transfers may occur simultaneously since there is no contention for resources. There are three separate ports to the TC from the system DMA (one for each of the memory interfaces), allowing for greater bandwidth capability between the system DMA and the TC.

3.12 Interprocessor Communication

Several mechanisms allow for communication between the MPU and the DSP on the OMAP5912 device. These include mailbox registers, MPU Interface, and shared memory space.

3.12.1 MPU/DSP Mailbox Registers

The MPU and DSP processors can communicate with each other via a mailbox-interrupt mechanism. There are four sets of mailbox registers located in public TIPB space. The registers are shared between the two processors, so the MPU and DSP may both access these registers within their own public TIPB space, but read/write accessibility of each register is different for each processor.

There are four sets of mailbox registers: two for the MPU to send messages and issue an interrupt to the DSP, the other two for the DSP to send messages and issue an interrupt to the MPU. Each set of mailbox registers consists of two 16-bit registers and a 1-bit flag register. The interrupting processor can use one 16-bit register to pass a data word to the interrupted processor and the other 16-bit register to pass a command word.

Communication is achieved when one processor writes to a command-word register, which causes an interrupt to the other processor and sets the corresponding flag register. The interrupted processor acknowledges by reading the command word, which also clears the flag register. A data-word register is also available in each mailbox register for optional 16-bit data.

The information communicated by the command and data words are entirely user-defined. The data word can be optionally used to indicate an address pointer or status word.

3.12.2 MPU Interface (MPUI)

The MPU interface (MPUI) allows the MPU and the system DMA controller to communicate with the DSP and its peripherals. The MPUI allows access to the full memory space (16M bytes) of the DSP and the DSP public peripheral bus. Thus, the MPU and system DMA controller both have read and write access to the complete DSP I/O space (128K bytes), including the control registers of the DSP public peripherals.

The MPUI port supports the following features:

- Four access modes:
  - Shared-access mode (SAM) for MPU access of DSP SARAM, DARAM, and external memory interface
  - Shared-access mode (SAM) for peripheral bus access
  - Host-only mode (HOM) for SARAM access
  - Host-only mode (HOM) for peripheral bus access
- Interrupt to MPU if access time-out occurs
- Programmable priority scheme (MPU versus DMA)
- Packing and unpacking of data (16 bits to 32 bits, and vice versa)
- 32-bit single-access support
- Software control endianism conversion
- System DMA capability to full memory space (16M bytes)
- System DMA capability to the DSP public TIPB peripherals (up to 128K bytes space)

This port can be used for many functions, such as: MPU loading of program code into DSP program memory space, sharing of data between MPU and DSP, implementing interprocessing communication protocols via shared memory, or allowing MPU to use and control DSP public TIPB peripherals.

3.12.3 MPU/DSP Shared Memory

The OMAP5912 implements a shared memory architecture via the traffic controller. Therefore, the MPU and DSP both have access to the shared SRAM (250K bytes) as well as to the EMIFF and EMIFS memory space. Through the DSP memory management unit (MMU), the MPU controls which regions of shared memory space the DSP is allowed to access. By setting up regions of shared memory, and defining a protocol for the MPU and DSP to access this shared memory, an interprocessor communication mechanism may be implemented. This method can be used in conjunction with the mailbox registers to create handshaking interrupts that properly synchronize the MPU and DSP accesses to shared memory. Utilizing the shared memory in this fashion may be useful when the desired data to be passed between the MPU and DSP is larger than the two 16-bit words provided by each set of mailbox command and data registers.

For example, the MPU may need to provide the DSP with a list of pointers to perform a specific task as opposed to a single command and single pointer. Using shared memory and the mailboxes, the DSP can read the list of pointers from shared memory after receiving the interrupt caused by an MPU write to the mailbox command register.

3.13 DSP Hardware Accelerators

The TMS320C55x DSP core within the OMAP5912 device utilizes three powerful hardware accelerator modules which assist the DSP core in implementing specific algorithms that are commonly used in video compression applications such as MPEG4 encoders/decoders. These accelerators allow implementation of such algorithms using fewer DSP instruction cycles and dissipating less power than implementations using only the DSP core. The hardware accelerators are utilized via functions from the TMS320C55x Image/Video Processing Library available from Texas Instruments.

Utilizing the hardware accelerators, the Texas Instruments Image/Video Processing Library implements many useful functions, which include the following:

- Forward and Inverse Discrete Cosine Transform (DCT) (used for video compression/decompression)
- Motion Estimation (used for compression standards such as MPEG video encoding and H.26x encoding)
- Pixel Interpolation (enabling high-performance fractal-pixel motion estimation)
- Quantization/Dequantization (useful for JPEG, MPEG, H.26x Encoding/Decoding)
- Flexible 1D/2D Wavelet Processing (useful for JPEG2000, MPEG4, and other compression standards)
- Boundary and Perimeter Computation (useful for Machine Vision applications)
- Image Threshold and Histogram Computations (useful for various Image Analysis applications)

3.13.1 DCT/iDCT Accelerator

The DCT/iDCT hardware accelerator is used to implement Forward and Inverse DCT (Discrete Cosine Transform) algorithms. These DCT/iDCT algorithms can be used to implement a wide range of video compression standards including JPEG Encode/Decode, MPEG Video Encode/Decode, and H.26x Encode/Decode.

3.13.2 Motion Estimation Accelerator

The Motion Estimation hardware accelerator implements a high-performance motion estimation algorithm, enabling MPEG Video encoder or H.26x encoder applications. Motion estimation is typically one of the most computation-intensive operations in video-encoding systems.

3.13.3 Pixel Interpolation Accelerator

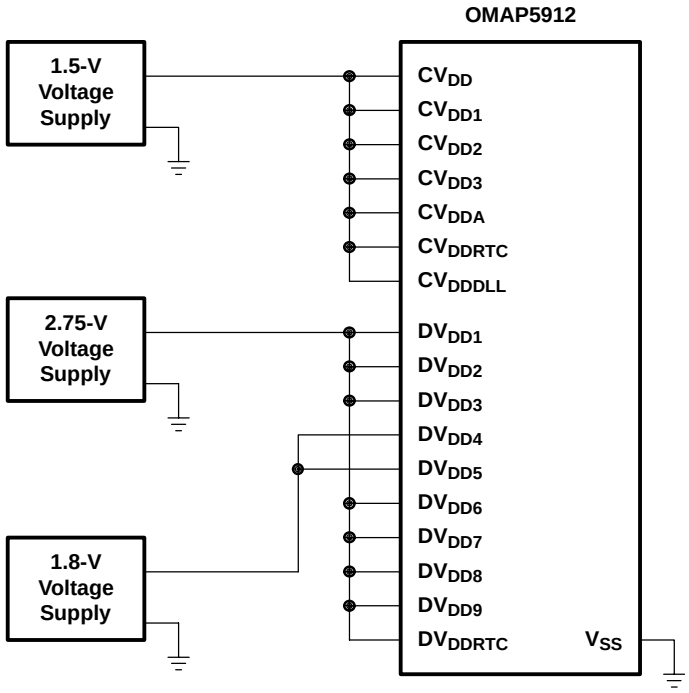
The Pixel Interpolation Accelerator enables high-performance pixel-interpolation algorithms, which allows for powerful fractal pixel motion estimation when used in conjunction with the Motion Estimation Accelerator. Such algorithms provide significant improvement to video-encoding applications.

3.14 Power Supply Connection Examples

3.14.1 Core and I/O Voltage Supply Connections

The OMAP5912 device is flexible regarding the implementation of the core and I/O voltage supplies of the device.

In a typical system, all of the core voltage supplies (CV_{DDx}) may be connected together and powered from one common supply. Likewise, all of the I/O voltage supplies (DV_{DDx}) may be connected together and powered from a common supply. Figure 3−4 illustrates this common system configuration.



NOTE: In this example, SDRAM (DV_{DD4}) and FLASH (DV_{DD5}) I/O voltage supplies are connected to 1.8 V and the other I/O voltage supplies are connected to 2.75 V. Each I/O voltage supply (DV_{DDx}) can be configured to either 1.8 V or 2.75 V nominal with corresponding bits in the VOLTAGE_CTRL_0 register.

Figure 3−4. Supply Connections for a Typical System

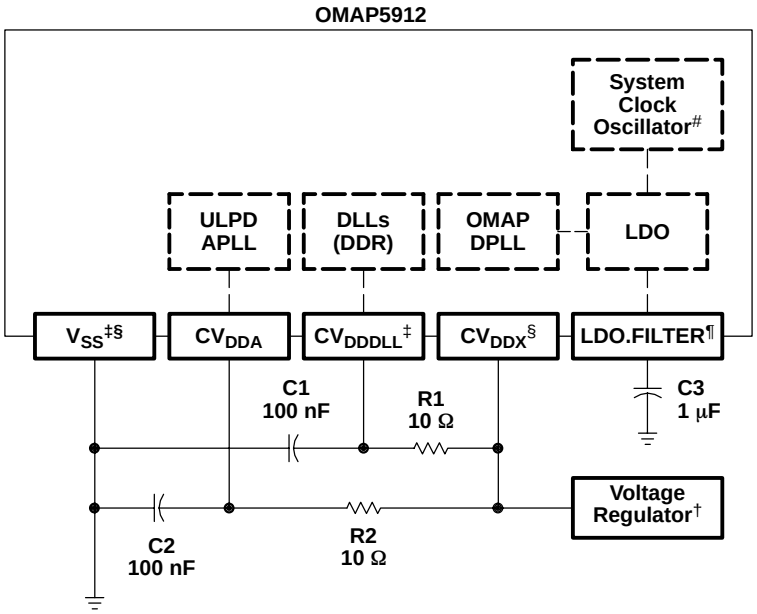
In the previous example, all CV_{DDx} pins are connected in common. However, the OMAP5912 has dedicated CV_{DD} pins that supply power to different sections of the chip. This feature can be useful in prototyping phases to troubleshoot power management features and perform advanced power analysis. By isolating each CV_{DDx} bus from the power source through isolation jumpers or current sense resistors, the current draw into different domains may be measured separately. This type of supply isolation must only be done during prototyping as production system designs should connect all the CV_{DDx} pins together, preferably to a common board plane.

NOTE:

There is no specific power sequencing for the different voltage supplies as long as all CV_{DDx} and DV_{DDx} voltages are ramped to valid operating levels within 500 ms of one another. Additionally, if certain I/O pins are unused in a specific system application, the DV_{DDx} supply pins that power these I/O must still be connected to valid operating voltage levels.

3.14.2 Core Voltage Noise Isolation

Two CV_{DD} pins on OMAP5912, CV_{DDA} and CV_{DDDLL}, are dedicated to supply power for the ULPD APLL and for the DLL elements of the DDR interface, respectively. In addition to using sound board design principles, these dedicated pins allow for added supply noise isolation circuitry to enable maximum performance. An example circuit is shown in Figure 3−5.



NOTES: A. This circuit is provided only as an example. Specific board layout implementation must minimize noise on the OMAP5912 voltage supply pins.

B. Unless otherwise noted in this document, all V_{SS} pins on the OMAP5912 are common and must be connected directly to a common ground; however, the discrete capacitor in the RC filter circuit should be placed as close as possible to the V_{SS} pins [ZZG balls AA21 (or W20) and A13; ZDY/GDY balls L7 (or L11) and F6].

C. For special consideration with respect to the connection of V_{SS} pin (ZZG ball Y13; ZDY/GDY ball H8), refer to Section 5.5.1, 32-kHz Oscillator and Input Clock.

† The voltage regulator must be selected to provide a voltage source with minimal low frequency noise.

‡ If a dedicated voltage regulator is not available for CV_{DDDLL} in the system, a simple low-pass RC filter can be used to isolate the cells from the switching noise of other digital circuits.

§ Common CV_{DD} for rest of chip.

¶ A regulated supply is delivered to DPLL macro(s) and available on unique bond pad. A decoupling capacitor of 1 μF must be connected externally between the pin called LDO. FILTER (ZZG ball J1; ZDY/GDY ball H1) and the ground.

System clock oscillator frequency = 12, 13, or 19.2 MHz.

Figure 3−5. External RC Circuits for Noise Isolation

4 Documentation Support

Extensive documentation supports all OMAP platform of devices from product announcement through applications development. The following types of documentation are available to support the design and use of the OMAP platform of applications processor devices:

- Device-specific data sheets
- Development-support tools
- Hardware and software application reports

A series of DSP textbooks is published by Prentice-Hall and John Wiley & Sons to support digital signal processing research and education. The TMS320 DSP newsletter, *Details on Signal Processing*, is published quarterly and distributed to update TMS320 DSP customers on product information.

Information regarding Texas Instruments (TI) OMAP and DSP products is also available on the Worldwide Web at *http://www.ti.com* uniform resource locator (URL).

4.1 Device and Development-Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all OMAP™ devices and support tools. Each OMAP™ commercial family member has one of three prefixes: X, P, or Null (e.g., **X**OMAP-DM270MGVL-B). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (X/TMDX) through fully qualified production devices/tools (Null/TMDS).

Device development evolutionary flow:

X Experimental device that is not necessarily representative of the final device's electrical specifications

P Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification

Null Fully-qualified production device

Support tool development evolutionary flow:

TMDX Development support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully qualified development support product

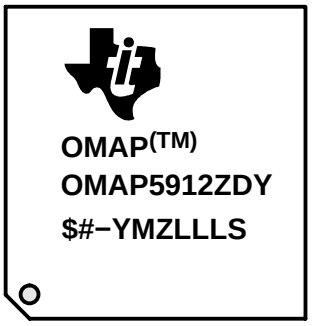
X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Null devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

The device revision can be determined by the symbols marked on the top of the ZDY package as shown in Figure 4−1. Some prototype devices may have markings different from those shown in Figure 4−1 with the device name in the following format: aOMAP5912xxx where a = product level and xxx = package designator.



$ = Internal TI Designator
 # = Revision Number
YMZLLLS = Internal TI Designator

NOTE: Qualified devices are marked with no prefix at the beginning of the device name, while nonqualified devices are marked with the letter X at the beginning of the device name.

Figure 4−1. Example Markings for OMAP5912 ZDY Package

4.2 Differences Between Production and Experimental Devices

The XOMAP5912 and POMAP5912 devices included some peripherals and functions that are not available on the OMAP5912 production silicon. See Table 4−1 for a list of the differences in peripherals.

For more information, see the following reference guides:

- *OMAP5912 Multimedia Processor OMAP3.2 Subsystem Reference Guide* (literature number SPRU749)
- *OMAP5912 Multimedia Processor Initialization Reference Guide* (literature number SPRU752)
- *OMAP5912 Multimedia Processor Power Management Reference Guide* (literature number SPRU753)
- *OMAP5912 Multimedia Processor Direct Memory Access (DMA) Support Reference Guide* (literature number SPRU755)
- *OMAP5912 Multimedia Processor Camera Interface Support Reference Guide* (literature number SPRU763)
- *OMAP5912 Multimedia Processor Display Interface Support Reference Guide* (literature number SPRU764)

Table 4−1. Changes to the OMAP5912

XOMAP5912 OR POMAP5912	SUPPORTED		OMAP5912
Compact Flash Peripheral	Yes	No	Compact Flash Peripheral
SOSSI Peripheral	Yes	No	SOSSI Peripheral
VLYNQ Peripheral	Yes	No	VLYNQ Peripheral
CCP Peripheral	Yes	No	CCP Peripheral
EMIFF DDR interface provides the same performance as SDR	Yes	Yes	EMIFF DDR interface runs at full DDR performance. New register bits and configuration information added in SPRU749.
Camera interface connected via TIPB bus	Yes	Yes	Camera interface connected via OCP bus. Performance improvement and new registers added in SPRU763.
LCD Interface	Yes	Yes	LCD interface additional register bits added in SPRU764.
Only General Purpose (Mode 0) is supported	Yes	Yes	Only General Purpose (Mode 0) is supported

Table 4−1. Changes to the OMAP5912 (Continued)

XOMAP5912 OR POMAP5912	SUPPORTED		OMAP5912
MMC SPI mode	No	No	MMC SPI mode
Stacked DDR	No	No	Stacked DDR
SSI, SST, SSR, STI, GDD	No	No	SSI, SST, SSR, STI, GDD
eFUSE, effuses	No	No	eFUSE, effuses
Windows tracer	No	No	Windows tracer
Mode 1 and 2, high security	No	No	Mode 1 and 2, high security
Emulation devices	No	No	Emulation Devices

5 Electrical Specifications

This section provides the absolute maximum ratings and the recommended operating conditions for the OMAP5912 device.

All electrical and switching characteristics in this data manual are valid over the recommended operating conditions unless otherwise specified.

5.1 Absolute Maximum Ratings

The list of absolute maximum ratings are specified over operating case temperature. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Section 5.2, Recommended Operating Conditions, is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All supply voltage values (core and I/O) are with respect to V_{SS}.

This section provides the absolute maximum ratings for the OMAP5912 device.

Supply voltage range (core), CV_{DD}, CV_{DD2}, CV_{DDA},CV_{DDRTC}, CV_{DDDLL} . . . . . −0.5 V to 2.1 V
Supply voltage range (I/O), $DV_{DD1/2/3/4/5/6/7/8/9/RTC}$, 1.8 V nominal . . . . . −0.5 V to 2.1 V
2.75 V and 3.3 V nominal . . . . . −0.5 V to 4.2 V
Input voltage range, V_I (12, 13, or 19.2 MHz and 32-kHz oscillator) . . . . . −0.5 V to 2.1 V
Input voltage range, V_I (standard LVCMOS), 1.8 V nominal . . . . . −0.5 V to (2.1 or DV_{DD} + 0.5)† V
2.75 V and 3.3 V nominal . . . . −0.5 V to (4.2 or DV_{DD} + 0.5)† V
Input voltage range, V_I (USB transceivers) . . . . . −0.5 V to DV_{DD} + 0.5 V
Input voltage range, V_I (I^2C) . . . . . − 0.5 V to 4.5 V
Output voltage range, V_O (standard LVCMOS), 1.8 V nominal . . . . . −0.5 V to (2.1 or DV_{DD} + 0.5)† V
2.75 V and 3.3 V nominal . . −0.5 V to (4.2 or DV_{DD} + 0.5)† V
Output voltage range, V_O (USB transceivers) . . . . . −0.5 V to DV_{DD} + 0.5 V
Output voltage range, V_O (I^2C) . . . . . −0.5 V to 4.5 V
Operating temperature range, T_C . . . . . −40°C to 85°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Max voltage is the lower value of the two expressions

5.2 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
$CV_{DD1/2/3/RTC}$	OMAP5912 supply voltage, core†‡	Low-power standby mode§	1.05	1.1	1.21	V
		Active mode	1.525	1.6	1.65	
CV_{DDA}	Supply voltage for analog PLL		1.525	1.6	1.65	V
CV_{DDDLL}	Core supply voltage for the DDR interface digitally controlled delay element (DCDL)¶		1.525	1.6	1.65	V
$DV_{DD1/2/3/4/5/6/7/8/9/RTC}$	Device supply voltage, I/O‡	Low-voltage range#	1.65	1.8	1.95	V
		High-voltage range#	2.5	2.75 or 3.3	3.6	
DV_{DD2}	Device supply voltage, I/O	Internal USB transceiver not used	1.65	1.8	1.95	V
		Internal USB transceiver used	3	3.3	3.6	
$CV_{DD} - DV_{DD}$	Device supply voltage difference‖				1.65	V
$DV_{DD} - CV_{DD}$	Device supply voltage difference‖				2.55	V
LDO.FILTER☆	Internal DPLL and 12, 13, or 19.2-MHz oscillator supply voltage□	Low-power standby mode§	1.05	1.1	1.21	V
		Active mode	1.43	1.5	1.65	
V_{SS}	Device supply voltage, GND			0		V
V_{IH}	High-level input voltage, I/O	Standard LVCMOS	0.7 DV_{DD}			V
		ZZG balls P9 and R8 (ZDY/GDY balls T2 and U1) are not used for USB differential voltage	2			
V_{IL}	Low-level input voltage, I/O	Standard LVCMOS			0.3 DV_{DD}	V
		ZZG balls P9 and R8 (ZDY/GDY balls T2 and U1) are not used for USB differential voltage			0.8	
V_I	Input voltage	ZZG balls P9 and R8 (ZDY/GDY balls T2 and U1) are used for USB	0.8		2.5	V
		OSC1 and OSC32K pins			CV_{DD}	
V_{ID}	Differential input voltage	ZZG balls P9 and R8 (ZDY/GDY balls T2 and U1) are used for USB	±200			mV

† All core voltage supplies must be tied to the same voltage level (within 50 mV).
‡ In Split-power mode (CV_{DDx} and DV_{DDx} = 0), RTC has to be supplied with CV_{DDRTC} = 1.05 V min and DV_{DDRTC} = 1.65 V min.
§ Low-power standby is defined as follows: the device is in deep-sleep mode and LOW_PWR = 1. The device runs from 32-kHz clock in this mode.
¶ To filter switching noises, it is recommended that an RC (R = 10 Ω, C = 100 nF) low-pass filter be implemented externally.
# Corresponding DV_{DD} mode bit must be configured in the Voltage_control_0 register.
‖ In systems where the CV_{DDx} and DV_{DDx} power supplies are ramped at generally the same time (within 500 ms of one another), there are no specific power sequencing requirements for the supplies. The only sequencing requirement is that the maximum voltage difference between CV_{DD} and DV_{DD} is not exceeded for greater than 500 ms. Likewise, if different voltages are used for the separate DV_{DDx} supplies, all DV_{DDx} supplies should be ramped up to valid voltage levels within 500 ms of one another.
☆ An external capacitor (C = 1 µF ± 10%) must be connected between LDO.FILTER and V_{SS} to provide decoupling capacitance for the regulator.
□ LDO has to be powered down by setting LDO_PWRDN_CNTL[0] in OMAP5912 configuration.

5.2 Recommended Operating Conditions (Continued)

			MIN	NOM	MAX	UNIT
I_{OH}	High-level output current	Low-voltage range DV_{DDmin} = 1.65 V			−2	mA
		High-voltage range DV_{DDmin} = 2.5 V			−3	mA
		18.3-mA drive strength buffers			−18.3	mA
I_{OL}	Low-level output current	Low-voltage range DV_{DDmin} = 1.65 V			2	mA
		High-voltage range DV_{DDmin} = 2.5 V			3	
		18.3-mA drive strength buffers			18.3	
T_C	Operating case temperature		−40		85	°C

† All core voltage supplies must be tied to the same voltage level (within 50 mV).
‡ In Split-power mode (CV_{DDx} and DV_{DDx} = 0), RTC has to be supplied with CV_{DDRTC} = 1.05 V min and DV_{DDRTC} = 1.65 V min.
§ Low-power standby is defined as follows: the device is in deep-sleep mode and LOW_PWR = 1. The device runs from 32-kHz clock in this mode.
¶ To filter switching noises, it is recommended that an RC (R = 10 Ω, C = 100 nF) low-pass filter be implemented externally.
# Corresponding DV_{DD} mode bit must be configured in the Voltage_control_0 register.
‖ In systems where the CV_{DDx} and DV_{DDx} power supplies are ramped at generally the same time (within 500 ms of one another), there are no specific power sequencing requirements for the supplies. The only sequencing requirement is that the maximum voltage difference between CV_{DD} and DV_{DD} is not exceeded for greater than 500 ms. Likewise, if different voltages are used for the separate DV_{DDx} supplies, all DV_{DDx} supplies should be ramped up to valid voltage levels within 500 ms of one another.
☆ An external capacitor (C = 1 µF ± 10%) must be connected between LDO.FILTER and V_{SS} to provide decoupling capacitance for the regulator.
□ LDO has to be powered down by setting LDO_PWRDN_CNTL[0] in OMAP5912 configuration.

5.3 Electrical Characteristics Over Recommended Operating Case Temperature Range (Unless Otherwise Noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	Standard LVCMOS	I_O = rated, DV_{DD} = 1.65 V to 3.6 V		0.8 DV_{DD}			V
		ZZG balls P9 and R8 (ZDY/GDY balls T2 and U1) are not used for USB differential voltage	I_O = −18.3 mA		DV_{DD} − 0.5			
V_{OL}	Low-level output voltage	Standard LVCMOS	I_O = rated, DV_{DD} = 1.65 V to 3.6 V				0.22 DV_{DD}	V
		ZZG balls P9 and R8 (ZDY/GDY balls T2 and U1) are not used for USB differential voltage	I_O = 18.3 mA				0.28	
		I^2C	Fast mode at 2-mA load		0		0.4	
			Fast mode at 3-mA load		0		0.6	
			Standard mode at 2-mA load		0		0.4	
I_I	Input current	Inputs without internal pullups/pulldowns enabled	V_I = V_I MAX to V_I MIN	Low-voltage range	−1		1	µA
				High-voltage range	−1		1	
		Input pins with 20-µA pulldowns enabled	DV_{DD} = MAX, V_I = V_{SS} to V_{DD}	Low-voltage range	5	10	25	
				High-voltage range	15	30	95	
		Input pins with 100-µA pulldowns enabled	DV_{DD} = MAX, V_I = V_{SS} to V_{DD}	Low-voltage range	55	100	185	
				High-voltage range	35	67	185	
		Input pins with 20-µA pullups enabled	CV_{DD} = MAX, V_I = V_{SS} to V_{DD}	Low-voltage range	−25	−10	−5	
				High-voltage range	−95	−30	−15	
		Input pins with 100-µA pullups enabled	CV_{DD} = MAX, V_I = V_{SS} to V_{DD}	Low-voltage range	−185	−100	−55	
				High-voltage range	−185	−67	−35	
I_{OZ}	Input current for outputs in high-impedance				− 20		20	µA
$I_{DDC(Q)}$	Core voltage supply current quiescent		Sum of CV_{DDx} currents. (Deep sleep mode with CV_{DD} = 1.6 V and DSP in IDLE at 25°C.)			290		µA
			Sum of CV_{DDx} currents. (Deep sleep mode with CV_{DD} = 1.6 V and DSP in RESET at 25°C.)			280		
$I_{DDC(A)}$	Core voltage supply current active		Sum of CV_{DDx}†			326		mA

† ARM926 running Dhrystone algorithm and DSP runnning GSM Full Rate Vocoder in internal memory. CV_{DD} = 1.6 V, DV_{DD} = 3.3 V, V_{DD4} = 1.8 V).

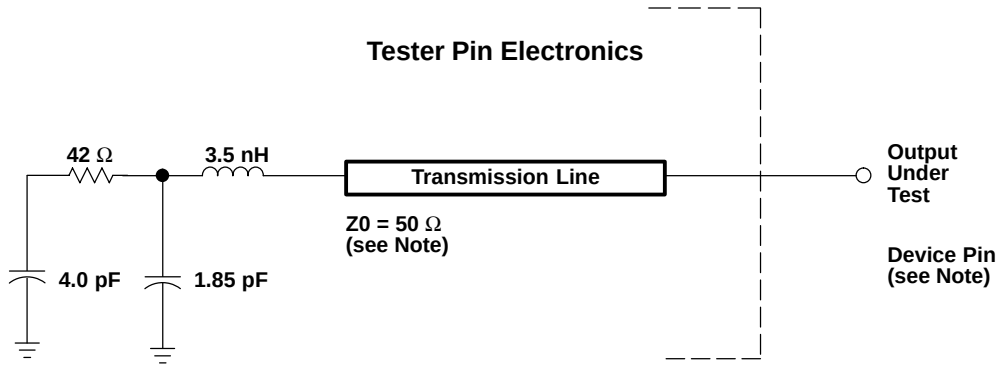
NOTE: These power measurements were taken at 25°C on an OMAP5912 OSK, running Dhrystone benchmark on the ARM and GSM vocoder on the DSP. These typical case numbers can vary based on board layout or application code being run. Please use this information only as a general guideline. In order to get more accurate power estimates, you should expect to do your own power measurements with your own set up and application code running.

5.3 Electrical Characteristics Over Recommended Operating Case Temperature Range (Unless Otherwise Noted) (Continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{DDCP(A)}$	Core and I/O voltage supply current active	Sum of CV_{DDx} and DV_{DDx} currents†		393		mA
V_{DD4}				6		mA
C_i	Input capacitance	ZZG balls P9 and R8 (ZDY/GDY balls T2 and U1) (USB)		7		pF
		All other I/O pins		4		
C_o	Output capacitance	ZZG balls P9 and R8 (ZDY/GDY balls T2 and U1) (USB)		7		pF
		All other I/O pins		4		

† ARM926 running Dhrystone algorithm and DSP runnning GSM Full Rate Vocoder in internal memory. CV_{DD} = 1.6 V, DV_{DD} = 3.3 V, V_{DD4} = 1.8 V).

NOTE: These power measurements were taken at 25°C on an OMAP5912 OSK, running Dhrystone benchmark on the ARM and GSM vocoder on the DSP. These typical case numbers can vary based on board layout or application code being run. Please use this information only as a general guideline. In order to get more accurate power estimates, you should expect to do your own power measurements with your own set up and application code running.



NOTE: The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. A transmission line with a delay of 2 ns or longer can be used to produce the desired transmission line effect. The transmission line is intended as a load only. It is not necessary to add or subtract the transmission line delay (2 ns or longer) from the data sheet timings.

Input requirements in this data sheet are tested with an input slew rate of < 4 Volts per nanosecond (4 V/ns) at the device pin.

Figure 5−1. 3.3-V Test Load Circuit

5.4 Timing Parameter Symbology

Timing parameter symbols used in the timing requirements and switching characteristics tables are created in accordance with JEDEC Standard 100. To shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

Lowercase subscripts and their meanings:	
a	access time
c	cycle time (period)
d	delay time
dis	disable time
en	enable time
f	fall time
h	hold time
r	rise time
su	setup time
t	transition time
v	valid time
w	pulse duration (width)
X	Unknown, changing, or don’t care level

Letters and symbols and their meanings:	
H	High
L	Low
V	Valid
Z	High impedance

5.5 Clock Specifications

This section provides the timing requirements and switching characteristics for the OMAP5912 system clock signals.

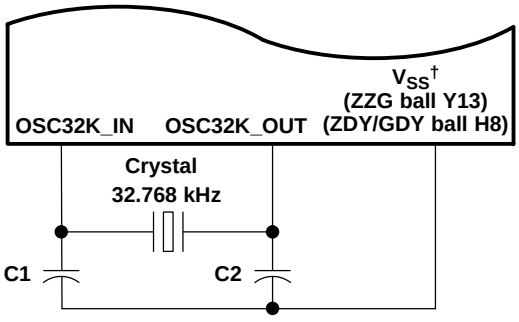
5.5.1 32-kHz Oscillator and Input Clock

The 32.768-kHz clock signal (often abbreviated to 32-kHz) may be supplied by either the on-chip 32-kHz oscillator (requiring an external crystal) or an external CMOS signal.

The on-chip oscillator requires an external 32.768-kHz crystal connected across the OSC32K_IN and OSC32K_OUT pins. The connection of the required circuit, consisting of the crystal and two load capacitors, is shown in Figure 5−2. The load capacitors, C_1 and C_2, should be chosen such that the equation below is satisfied (recommended values are $C_1 = C_2 = 10$ pF). C_L in the equation is the load specified for the crystal. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator pins (OSC32K_IN and OSC32K_OUT) and to the V_{SS} pin closest to the oscillator pins (ZZG ball Y13; ZDY/GDY ball H8).

NOTE 1: Do not connect V_{SS} (ZZG ball Y13; ZDY/GDY ball H8) to the common board ground but only to the oscillator circuit as shown.

$$C_L = \frac{C_1 C_2}{(C_1 + C_2)}$$

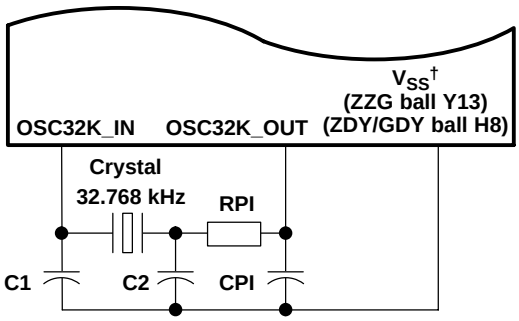


† Do not connect V_{SS} (ZZG ball Y13; ZDY/GDY ball H8) to the common board ground but only to the oscillator circuit as shown.

Figure 5−2. 32-kHz Oscillator External Crystal

NOTE 2: Recommended maximum series resistance specification of the crystal is 100 kΩ or less at 32 kHz. Series resistance at any other parasitic resonance of the crystal should be greater than 100 kΩ. For crystals whose parasitic resonance has maximum series resistor less than 100 kΩ, a PI-network (Figure 5−3) is needed between the OSC32K_OUT pin and the crystal to suppress oscillation at frequencies other than 32 kHz. The PI-network creates a pole to reduce the negative resistance at frequencies greater than 32 kHz.

The recommended PI-network for use with these crystals is CPI = 10 pF total and RPI = 390 kΩ ± 5%



† Do not connect V_{SS} (ZZG ball Y13; ZDY/GDY ball H8) to the common board ground but only to the oscillator circuit as shown.

Figure 5−3. 32-kHz Oscillator External Crystal With PI-Network

NOTE 3: When the internal oscillator is used to generate the 32-kHz clock, the CLK32K_IN pin must be tied to V_{SS}. Otherwise, the 32-kHz clock is corrupted and the device fails.
If the external CMOS clock is used to provide the 32-kHz clock, the OSC32K_IN (XI) pin must be tied to CV_{DD}. The OSC32K_OUT (XO) pin must be tied to V_{SS}.

Table 5−1 shows the switching characteristics of the 32-kHz oscillator and Table 5−2 shows the input requirements of the 32-kHz clock input.

Table 5−1. 32-kHz Oscillator Switching Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Start-up time (from power up until oscillating at stable frequency of 32.768 kHz)	C1 = C2 = 10 pF, CV_{DD} = 1.35 V		200	800	ms
I_{DDA}, active current consumption			4		µA
Oscillation frequency			32.768		kHz

Table 5−2. 32-kHz Input Clock Timing Requirements

NO.			MIN	NOM	MAX	UNIT
CK1	$1/t_{cyc}$	Frequency		32.768		kHz
CK2	t_f	Fall time			25	ns
CK3	t_r	Rise time			25	ns
CK4		Duty cycle (high-to-low ratio)	30		70	%
CK5		Frequency stability†	−250		250	ppm

† The frequency stability requirement for the 32-kHz crystal is necessary for proper compensation by the on-chip real-time clock (RTC) module. If the on-chip RTC is not used, the OMAP5912 has no frequency stability requirement. However, specific systems may require tighter frequency stability. TI recommends that designers carefully choose an external crystal that meets their system requirements for frequency stability across the expected temperature range.

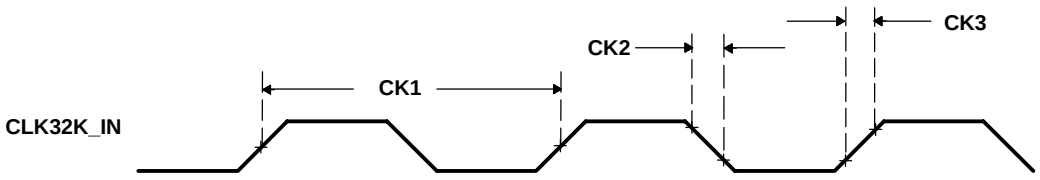


Figure 5−4. 32-kHz Input Clock

5.5.2 Base Oscillator (12, 13, or 19.2 MHz) and Input Clock

The internal base system oscillator is enabled following a device reset. The oscillator requires an external crystal to be connected across the OSC1_IN and OSC1_OUT pins. If the internal oscillator is not used (configured in software), an external clock source (12,13, 19.2 MHz) must be applied to the OSC1_IN pin, and the OSC1_OUT pin must be left unconnected. Because the internal oscillator can be used as a clock source to the OMAP DPLL, the 12-,13-, or 19.2-MHz crystal oscillation frequency can be multiplied to generate the DSP clock, MPU clock, traffic controller clock.

The crystal must be in fundamental-mode operation, and parallel resonant, with a maximum effective series resistance of 50 Ω and a power dissipation of 0.5 mW. The connection of the required circuit, consisting of the crystal and two load capacitors, is shown in Figure 5−5. The load capacitors, C_1 and C_2, must be chosen such that the equation below is satisfied (recommended values are $C_1 = C_2 = 2C_L$). C_L in the equation is the load specified for the crystal. All discrete components used to implement the oscillator circuit must be placed as close as possible to the associated oscillator pins (OSC1_IN and OSC1_OUT) and to the V_{SS} pins closest to the oscillator pins (ZZG balls AA1 and Y3; ZDY/GDY balls G11 and N5).

NOTE: The base oscillator is powered by the embedded LDO. If an external clock source is used instead of using the on-chip oscillator, care must be taken that the voltage level driven onto the OSC1_IN pin is no greater than the LDO voltage level.

$$C_1 = C_2 = 2C_L \quad (C_L = \text{Crystal Load Capacitance})$$

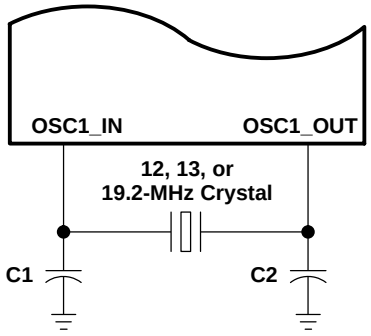


Figure 5−5. Internal System Oscillator External Crystal

If USB host function is used, it is recommended that a very low PPM crystal (≤ 50 ppm) be used for the 12,13, or 19.2 MHz oscillator circuit. If the USB host function is not used, then a crystal of ≤ 180 ppm is recommended. When selecting a crystal, the system design must take into account the temperature and aging characteristics of a crystal versus the user environment and expected lifetime of the system.

Table 5−3 shows the switching characteristics of the base oscillator.

Table 5−3. Base Oscillator Switching Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Start-up time (from power up until oscillating at stable frequency of 12,13, or 19.2 MHz)	C1 = C2 = 10 pF, CV_{DD} = 1.3V		1.7	3	ms
I_{DDA}, active current consumption	C1 = C2 = 10 pF, CV_{DD} = 1.5V		220		µA
Oscillation frequency			12 to 19.2		MHz

Table 5−4 and Figure 5−6 show the clock timing requirements for using an external system clock source.

Table 5−4. 12-MHz, 13-MHz, and 19.2-MHz Input Clock Timing Requirements†

NO.				MIN	NOM	MAX	UNIT
SCK1	$t_{c(OSC1\_IN)}$	Frequency			12 to 19.2		MHz
SCK2	$t_{f(OSC1\_IN)}$	Fall time				5	ns
SCK3	$t_{r(OSC1\_IN)}$	Rise time				5	ns
SCK4	$t_{w(OSC1\_IN)}$	Duty cycle (high-to-low ratio)		40		60	%
SCK5	$t_{j(OSC1\_IN)}$	Frequency stability	USB host function is used	−50		50	ppm
			USB host function is not used	−180		180	

† The clock signal level must not exceed CV_{DD}. See Section 5.2, Recommended Operating Conditions.

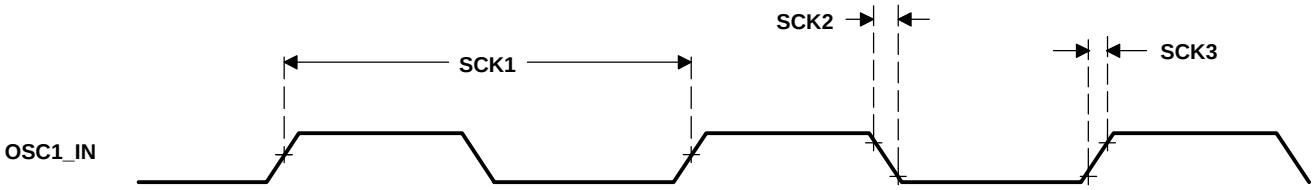


Figure 5−6. Input Clock Timings

5.6 Reset Timing

This section provides the timing requirements for the OMAP5912 hardware reset signals.

5.6.1 OMAP5912 Device Reset

The $\overline{\text{PWRON\_RESET}}$ signal is the active-low asynchronous reset input responsible for the reset of the entire OMAP5912 device. When using an external crystal to supply the 32-kHz system clock, $\overline{\text{PWRON\_RESET}}$ must be asserted low a minimum of two 32-kHz clock cycles longer than the worst-case start-up time of the 32-kHz oscillator after stable power supplies (see Figure 5−7). If an external CMOS input signal is used to source 32 kHz, $\overline{\text{PWRON\_RESET}}$ must be asserted low a minimum of two 32-kHz clock cycles after stable power supplies. See Table 5−5 and Table 5−6.

Table 5−5. OMAP5912 Device Reset Timing Requirements

NO.			MIN	MAX	UNIT
RS1	$t_{w(PWRON\_RST)}$	Pulse duration, $\overline{\text{PWRON\_RESET}}$ low†	800		ms

† The rising and falling edge duration of PWRON_RESET is characterized with a max t_r/t_f = 10 ns. (Timing value is given from 10% to 90% of the signal.)

Table 5−6. OMAP5912 Device Reset Switching Characteristics

NO.	PARAMETER		MIN	MAX	UNIT
RS2	$t_{d(PWRONH-RSTH)}$	Delay time, $\overline{\text{PWRON\_RESET}}$ high to $\overline{\text{RST\_OUT}}$ high		T + 10‡	µs

‡ T = P*(C + 7), P = period of 32-kHz clock, C = Value of ULPD wakeup time setup register, SETUP_ULPD1_REG (Default 03FFh)

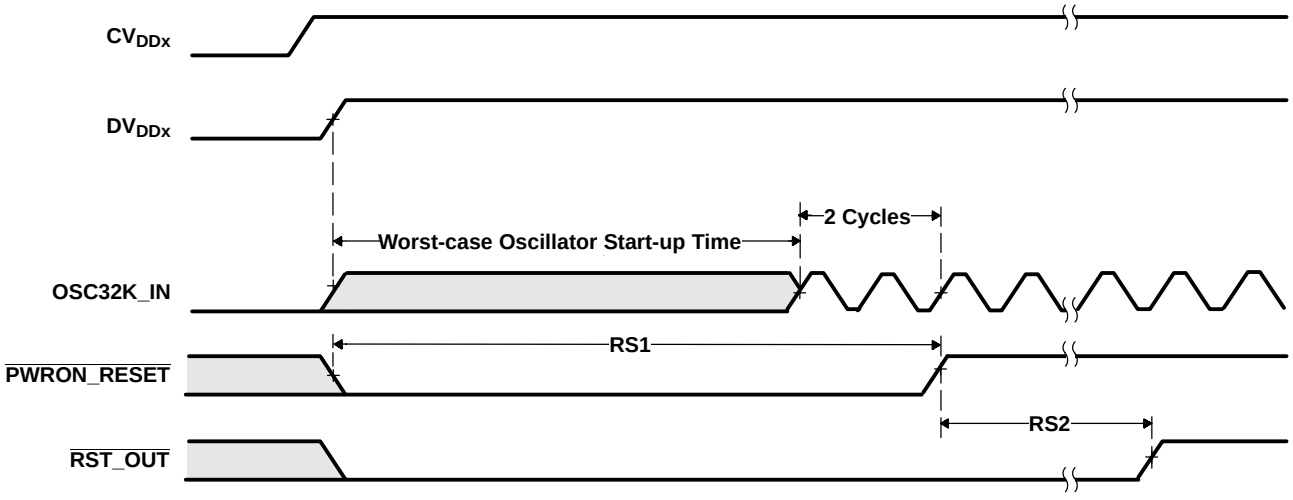


Figure 5−7. Device Reset Timings

5.6.2 OMAP5912 MPU Core Reset

The MPU_RST signal is the active-low asynchronous input responsible for the reset of the OMAP5912 MPU core. Stable power supplies are assumed prior to MPU_RST assertion. Figure 5−8 illustrates the behavior of MPU_RST and RST_OUT. In Figure 5−8, a logic-high level is assumed on the PWRON_RESET input. In the case where an application ties the PWRON_RESET and MPU_RST together, the behavior described in Section 5.6.1, OMAP5912 Device Reset, will override. See Table 5−7 and Table 5−8.

Table 5−7. MPU_RST Timing Requirements

NO.			MIN	MAX	UNIT
M3	$t_{w(MPU\_RST)}$	Pulse duration, MPU_RST low	50		µs

Table 5−8. MPU_RST Switching Characteristics†

NO.	PARAMETER			MIN	MAX	UNIT
M1	$t_{d(MPUL-RSTL)}$	Delay time, MPU_RST low to RST_OUT low			1	µs
M2	$t_{d(MPUH-RSTH)}$	Delay time, MPU_RST high to RST_OUT high	MPU_RST asserted during OMAP5912 awake state		10	µs
			MPU_RST asserted during OMAP5912 deep-sleep state		T + 10†	

† T = P*(C + 7), P = period of 32-kHz clock, C = Value of ULPD wakeup time setup register, SETUP_ULPD1_REG (Default 03FFh)

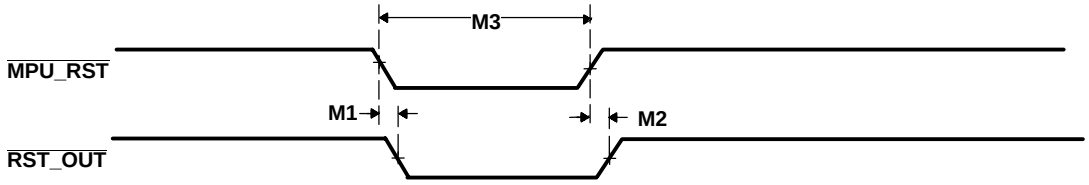
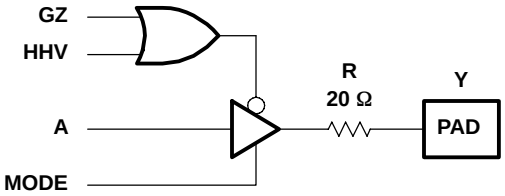


Figure 5−8. MPU Core Reset Timings

5.7 External Memory Interface Timing

Some EMIFF and EMIFS output terminals have the following particularity:

A serial resistor of 20 Ω is included at the output of the terminal to match with PCB line impedance and ensure proper signal integrity. See Table 2−3 (ZDY/GDY Package Terminal Characteristics) and Table 2−4 (ZZG Package Terminal Characteristics) for the list of terminals, which are concerned.



5.7.1 EMIFS/NOR Flash Interface Timing

Table 5−9 and Table 5−10 assume testing over recommended operating conditions (see Figure 5−9 through Figure 5−20).

Section 5.7.1.1 provides information on and an example of how to calculate OMAP5912 EMIFS NOR Flash timings.

Table 5−9. EMIFS/NOR Flash Interface Timing Requirements†

NO			DV_{DD5} = 1.8 V/2.75 V/3.3 V NOMINAL			UNIT
					MIN MAX	
F5	$t_{su(DV-OEH)}$	Setup time, read data valid before $\overline{FLASH.OE}$ high	Async modes		20.7	ns
F6	$t_{h(OEH-DV)}$	Hold time, read data valid after $\overline{FLASH.OE}$ high	Async modes		−4.1	ns
F7	$t_{w(RDYV)}$	FLASH.RDY low duration	Async modes		3P + 2.6‡	ns
F21	$t_{su(DV-AIV)}$	Setup time, read data valid before Address invalid	Async page mode		25.3	ns
F22	$t_{h(AIV-DV)}$	Hold time, read data valid after Address invalid	Async page mode		−3.5	ns
F33	$t_{h(CLKH-DV)}$	Hold time, read data valid after FLASH.CLK	Sync modes	RT=0§	−3.6	ns
				RT=1§	13.54	
F34	$t_{su(DV-CLKH)}$	Setup time, read data valid before FLASH.CLK	Sync modes	RT=0§	16.4	ns
				RT=1§	1	
F38	$t_{su(RDYV-CLKH)}$	Setup time, FLASH.RDY low before FLASH.CLK	Sync modes	RT=0§	18.4	ns
				RT=1§	1.1	
F39	$t_{h(CLKH-RDYIV)}$	Hold time, FLASH.RDY low after FLASH.CLK	Sync modes	RT=0§	−4.7	ns
				RT=1§	10.8	

† The maximum EMIFS/flash clock rate is limited to the maximum traffic controller clock rate for the OMAP5912, provided all EMIFS/flash timing constraints are met.

‡ P = EMIFS clock period (REF_CLK)

§ When the RT field in the EMIFS configuration register is set, input data is retimed to the external FLASH.CLK signal. The RT = 1 setting is only valid in synchronous modes. The RT = 0 setting in synchronous modes is assured only for EMIFS clock (REF_CLK) frequencies of 50 MHz and lower.

Table 5−10. EMIFS/NOR Flash Interface Switching Characteristics†‡

NO	PARAMETER			DV_{DD5} = 1.8 V/2.75 V/3.3 V NOMINAL		UNIT
				MIN	MAX	
F1	$t_{w(CSV)}$	$\overline{FLASH.CSx}$ low duration—Read operation	Async modes	A − 7	A + 7	ns
F3	$t_{d(CSV-ADIV)}$	Delay time, $\overline{FLASH.CSx}$ low to $\overline{FLASH.ADV}$ high	Async modes	B − 8.2	B + 4.53	ns
			Sync modes	M − 8.2	M + 4.53	
F4	$t_{d(CSV-OEIV)}$	Delay time, $\overline{FLASH.CSx}$ low to $\overline{FLASH.OE}$ high	Async modes	C − 7.3	C + 4.11	ns
F9	$t_{d(CSV-AV)}$	Delay time, $\overline{FLASH.CSx}$ low to address valid	Async and sync modes	−8.7	7.8	ns
F10	$t_{d(CSV-BEV)}$	Delay time, $\overline{FLASH.CSx}$ low to $\overline{FLASH.BEx}$ valid	Async and sync modes	−5.4	3.9	ns
F11	$t_{d(CSIV-BEIV)}$	Delay time, $\overline{FLASH.CSx}$ high to $\overline{FLASH.BEx}$ invalid	Async and sync modes	−5.4	3.9	ns
F12	$t_{d(CSV-ADV)}$	Delay time, $\overline{FLASH.CSx}$ low to $\overline{FLASH.ADV}$ low	Async and sync modes	−8.2	4.53	ns
F13	$t_{d(CSV-OEV)}$	Delay time, $\overline{FLASH.CSx}$ low to $\overline{FLASH.OE}$ low	Async (OESETUP = 0) and sync modes	− 7.3	4.11	ns
F14	$t_{d(CSIV-ADIV)}$	Delay time, $\overline{FLASH.CSx}$ high to $\overline{FLASH.ADV}$ high	Async modes	−8.2	4.53	ns
F15	$t_{d(CSIV-OEIV)}$	Delay time, $\overline{FLASH.CSx}$ high to $\overline{FLASH.OE}$ high	Async (OEHOLD = 0) and sync modes	− 7.3	4.11	ns
F16	$t_{d(CSV-OEV)}$	$\overline{FLASH.CSx}$ high duration—Read operation	Async modes	J − 7	J + 7	ns
F17	$t_{w(CSIV)}$	Delay time, $\overline{FLASH.CSx}$ low to $\overline{FLASH.OE}$ low	Async (OESETUP ≠ 0) modes	K − 7.3	K + 4.11	ns
F18	$t_{w(CSIV)}$	Delay time, $\overline{FLASH.OEx}$ high to $\overline{FLASH.CSx}$ high	Async (OEHOLD ≠ 0) modes	L − 7.3	L + 4.11	ns
F19	$t_{w(AV)}$	Address valid duration—1st access	Async modes	A − 5.6	A + 6.25	ns
F20	$t_{w(AV)}$	Address valid duration—2nd, 3rd, and 4th accesses	Async modes	D − 5.6	D + 6.25	ns
F23	$t_{w(CSV)}$	$\overline{FLASH.CSx}$ low duration—Write operation	Async modes	E − 7	E + 7	ns
F23/2	$t_{w(WEV)}$	$\overline{FLASH.WE}$ low duration—Write operation	Async modes	G − 1.4	G + 1.4	ns
F25	$t_{d(CSV-WEV)}$	Delay time, $\overline{FLASH.CSx}$ low to $\overline{FLASH.WE}$ low	Async modes	F − 6.6	F + 3.29	ns
F27	$t_{d(WEIV-CSIV)}$	Delay time, $\overline{FLASH.WE}$ high to $\overline{FLASH.CSx}$ high	Async modes	H − 3.29	H + 6.6	ns

† The maximum EMIFS/flash clock rate is limited to the maximum traffic controller clock rate for the OMAP5912, provided all EMIFS/flash timing constraints are met.

‡ See Section 5.7.1.1 for information on and an example of how to calculate OMAP5912 EMIFS NOR Flash timings.

A = (RDWST + 2) * EMIFS clock period (REF_CLK)
B = (ADVHOLD + 1) * EMIFS clock period (REF_CLK)
C = (RDWST – OEHOLD +2) * EMIFS clock period (REF_CLK)
D = (PGWST + 1) * EMIFS clock period (REF_CLK)
E = (WRWST + WELEN + 3) * EMIFS clock period (REF_CLK)
F = (WRWST + 1) * EMIFS clock period (REF_CLK)
G = (WELEN + 1) * EMIFS clock period (REF_CLK)
H = 1 * EMIFS clock period (REF_CLK)
I = 0.5 * EMIFS clock period (REF_CLK)
J = (BTWST + 1) * EMIFS clock period (REF_CLK)
K = OESETUP * EMIFS clock period (REF_CLK)
L = OEHOLD * EMIFS clock period (REF_CLK)
M = (ADVHOLD + 1) * EMIFS clock period (REF_CLK) + 1 TC_CK period

Table 5−10. EMIFS/NOR Flash Interface Switching Characteristics†‡ (Continued)

NO	PARAMETER			DV_{DD5} = 1.8 V/2.75 V/3.3 V NOMINAL		UNIT
				MIN	MAX	
F27/2	$t_{d(WEIV-AIV)}$	Delay time, $\overline{\text{FLASH.WE}}$ high to FLASH.A[25:1] invalid	Async modes	P − 3.5	P + 6.3	ns
F27/3	$t_{d(WEIV-DIV)}$	Delay time, $\overline{\text{FLASH.WE}}$ high to FLASH.D[15:0] invalid	Async modes	P − 4.4	P + 1.812	ns
F28	$t_{d(CSV-DLZ)}$	Delay time, $\overline{\text{FLASH.CSx}}$ low to data bus driven	Async modes	−13.9	0.4	ns
F29	$t_{d(CSV-DV)}$	Delay time, $\overline{\text{FLASH.CSx}}$ low to data bus valid	Async modes	−12.9	2.19	ns
F30	$t_{d(CSIV-DIV)}$	Delay time, $\overline{\text{FLASH.CSx}}$ high to data bus invalid	Async modes	−12.9	2.19	ns
F31	$t_{d(CSIV-DHZ)}$	Delay time, $\overline{\text{FLASH.CSx}}$ high to data bus high Z	Async modes	−13.9	0.4	ns
F35	$t_{d(CLKH-BAA)}$	Delay time, FLASH.CLK high to $\overline{\text{FLASH.BAA}}$ transition	Sync modes	I + 0.68	I + 8	ns
F36	$t_{d(CSV-CLKV)}$	Delay time, $\overline{\text{FLASH.CSx}}$ low to FLASH.CLK high	$\overline{\text{FLASH.CS0}}$ Sync modes	H − 9.3		ns
			$\overline{\text{FLASH.CS1}}$, $\overline{\text{FLASH.CS2}}$, $\overline{\text{FLASH.CS3}}$ Sync modes	H − 8.1		ns
F37	$t_{d(CLKIV-CSIV)}$	Delay time, FLASH.CLK invalid to $\overline{\text{FLASH.CSx}}$ high	Sync modes	H + 0.1		ns
F40	$t_{d(OEV-DIV)}$	Delay time, $\overline{\text{FLASH.OE}}$ low to data bus invalid	Async and sync modes	−4.8	0.64	ns
F41	$t_{d(OEV-DHZ)}$	Delay time, $\overline{\text{FLASH.OE}}$ low to data bus high Z	Async and sync modes	−8.9	0.5	ns
F42	$t_{d(WEV-DIV)}$	Delay time, $\overline{\text{FLASH.WE}}$ low to data bus invalid	Async and sync modes	−4.5	1.93	ns
F43	$t_{d(WEV-DV)}$	Delay time, $\overline{\text{FLASH.WE}}$ low to data bus valid	Async and sync modes	−4.5	1.93	ns

† The maximum EMIFS/flash clock rate is limited to the maximum traffic controller clock rate for the OMAP5912, provided all EMIFS/flash timing constraints are met.

‡ See Section 5.7.1.1 for information on and an example of how to calculate OMAP5912 EMIFS NOR Flash timings.
A = (RDWST + 2) * EMIFS clock period (REF_CLK)
B = (ADVHOLD + 1) * EMIFS clock period (REF_CLK)
C = (RDWST – OEHOLD +2) * EMIFS clock period (REF_CLK)
D = (PGWST + 1) * EMIFS clock period (REF_CLK)
E = (WRWST + WELEN + 3) * EMIFS clock period (REF_CLK)
F = (WRWST + 1) * EMIFS clock period (REF_CLK)
G = (WELEN + 1) * EMIFS clock period (REF_CLK)
H = 1 * EMIFS clock period (REF_CLK)
I = 0.5 * EMIFS clock period (REF_CLK)
J = (BTWST + 1) * EMIFS clock period (REF_CLK)
K = OESETUP * EMIFS clock period (REF_CLK)
L = OEHOLD * EMIFS clock period (REF_CLK)
M = (ADVHOLD + 1) * EMIFS clock period (REF_CLK) + 1 TC_CK period

5.7.1.1 EMIFS NOR Flash Timing Calculation Example

The following registers/fields and clock settings are used to calculate OMAP5912 EMIFS NOR Flash timings:

- **FCLKDIV.** Bits [1:0] of the EMIFS Chip-Select Configuration Registers (EMIFS_CCS0, EMIFS_CCS1, EMIFS_CCS2, and EMIFS_CCS3).

  FCLKDIV controls the TC_CK divider REF_CLK:

  - If FCLKDIV = 00: REF_CLK = TC_CK divide by 1
  - If FCLKDIV = 01: REF_CLK = TC_CK divide by 2
  - If FCLKDIV = 10: REF_CLK = TC_CK divide by 4
  - If FCLKDIV = 11: REF_CLK = TC_CK divide by 6

- **RDWST.** Bits [7:4] of the EMIFS Chip-Select Configuration Registers (EMIFS_CCS0, EMIFS_CCS1, EMIFS_CCS2, and EMIFS_CCS3).

  RDWST controls the wait states cycle number for asynchronous read operations and the initial idle time for asynchronous read page mode and synchronous read mode.

  Value range: 0000 to 1111

- **WRWST.** Bits [11:8] of the EMIFS Chip-Select Configuration Registers (EMIFS_CCS0, EMIFS_CCS1, EMIFS_CCS2, and EMIFS_CCS3).

  WRWST controls the wait states cycle number for write operations.

  Value range: 0000 to 1111

- **PGWSTEN.** Bit [31] of the EMIFS Chip-Select Configuration Registers (EMIFS_CCS0, EMIFS_CCS1, EMIFS_CCS2, and EMIFS_CCS3).

  PGWSTEN is specification.

  - If PGWSTEN = 0: PGWST is specified by PGWST / WELEN Bits [15:12]
  - If PGWSTEN = 1: PGWST is specified by PGWST Bits [30:27]

- **PGWST / WELEN.** Bits [15:12] of the EMIFS Chip-Select Configuration Registers (EMIFS_CCS0, EMIFS_CCS1, EMIFS_CCS2, and EMIFS_CCS3).

  PGWST / WELEN controls the wait states cycle number between accesses in a page for asynchronous page mode. It also controls the $\overline{WE}$ pulse length during a write access.

  - If PGWSTEN = 0: this bit specifies both PGWST and WELEN
  - If PGWSTEN = 1: this bit specifies only PGWST

  Value range: 0000 to 1111

- **BTWST.** Bits [26:23] of the EMIFS Chip-Select Configuration Registers (EMIFS_CCS0, EMIFS_CCS1, EMIFS_CCS2, and EMIFS_CCS3).

  BTWST controls the IDLE cycle number for bus turnaround and $\overline{CS}$ high-pulse-width timing.

  Value range: 0000 to 1111

- **OE_SETUP.** Bits [3:0] of the Advanced EMIFS Chip-Select Configuration Registers (EMIFS_ACS0, EMIFS_ACS1, EMIFS_ACS2, and EMIFS_ACS3).

  OE_SETUP controls the number of cycles inserted from $\overline{CS}$ low to $\overline{OE}$ low.

  Value range: 0000 to 1111

- **OE_HOLD.** Bits [7:4] of the Advanced EMIFS Chip-Select Configuration Registers (EMIFS_ACS0, EMIFS_ACS1, EMIFS_ACS2, and EMIFS_ACS3).

  OE_HOLD controls the number of cycles inserted from $\overline{OE}$ high to $\overline{CS}$ high.

  Value range: 0000 to 1111

- **TC_CK.** Traffic controller clock

- **REF_CLK.** EMIFS clock period

- **ADVHOLD.** Bit [8] of the Advanced EMIFS Chip-Select Configuration Registers (EMIFS_ACS0, EMIFS_ACS1, EMIFS_ACS2, and EMIFS_ACS3).

  ADVHOLD controls the $\overline{ADV}$ pulse width low.

  Value range: 0 to 1

EXAMPLE

REF_CLK = 10.42 ns

RDWST = 0

ADVHOLD = 0

TC_CK = 10.42 ns

OE_HOLD = 0

PGWST = 0

WRWST = 0

WELEN = 0

BTWST = 0

OE_SETUP = 0

FCLKDIV = 0

Using the above register and clock settings, the following timing constraints are calculated using the EMIFS NOR FLASH timing calculator, which is available through Texas Instruments:

P = 10.42 ns

A = 20.84 ns

B = 10.42 ns

M = 20.84 ns

C = 20.84 ns

D = 10.42 ns

E = 31.26 ns

F = 10.42 ns

G = 10.42 ns

H = 10.42 ns

I = 5.21 ns

J = 10.42 ns

K = 0 ns

L = 0 ns

Table 5−11 and Table 5−12 show a sample timing calculation of the Table 5−9 and Table 5−10 parametric values using the constraints calculated above.

Table 5−11. Sample Timing Calculation of Table 5−9 Parametric Values Using Constraints Calculated Above

NO					DATASHEET VALUES (FROM TABLE 5−9) DV_{DD5} = 1.8 V/2.75 V/3.3 V NOMINAL		AUTOMATIC TIMING CALCULATIONS DV_{DD5} = 1.8 V/2.75 V/3.3 V NOMINAL		UNIT
					MIN	MAX	MIN	MAX	
F5	$t_{su(DV-OEH)}$	Setup time, read data valid before $\overline{\text{FLASH.OE}}$ high	Async modes		20.7		20.7		ns
F6	$t_{h(OEH-DV)}$	Hold time, read data valid after $\overline{\text{FLASH.OE}}$ high	Async modes		−4.1		−4.1		ns
F7	$t_{w(RDYV)}$	FLASH.RDY low duration	Async modes		3P + 2.6‡		33.86		ns
F21	$t_{su(DV-AIV)}$	Setup time, read data valid before Address invalid	Async page mode		25.3		25.3		ns
F22	$t_{h(AIV-DV)}$	Hold time, read data valid after Address invalid	Async page mode		−3.5		−3.5		ns
F33	$t_{h(CLKH-DV)}$	Hold time, read data valid after FLASH.CLK	Sync modes	RT=0§	−3.6		−3.6		ns
				RT=1§	13.54		13.54		
F34	$t_{su(DV-CLKH)}$	Setup time, read data valid before FLASH.CLK	Sync modes	RT=0§	16.4		16.4		ns
				RT=1§	1		1		
F38	$t_{su(RDYV-CLKH)}$	Setup time, FLASH.RDY low before FLASH.CLK	Sync modes	RT=0§	18.4		18.4		ns
				RT=1§	1.1		1.1		
F39	$t_{h(CLKH-RDYIV)}$	Hold time, FLASH.RDY low after FLASH.CLK	Sync modes	RT=0§	−4.7		−4.7		ns
				RT=1§	10.8		10.8		

† The maximum EMIFS/flash clock rate is limited to the maximum traffic controller clock rate for the OMAP5912, provided all EMIFS/flash timing constraints are met.

‡ P = EMIFS clock period (REF_CLK)

§ When the RT field in the EMIFS configuration register is set, input data is retimed to the external FLASH.CLK signal. The RT = 1 setting is only valid in synchronous modes. The RT = 0 setting in synchronous modes is assured only for EMIFS clock (REF_CLK) frequencies of 50 MHz and lower.

Table 5−12. Sample Timing Calculation of Table 5−10 Parametric Values Using Constraints Calculated Above

NO	PARAMETER			DATASHEET VALUES (FROM TABLE 5−10) DV_{DD5} = 1.8 V/2.75 V/3.3 V NOMINAL		AUTOMATIC TIMING CALCULATIONS DV_{DD5} = 1.8 V/2.75 V/3.3 V NOMINAL		UNIT
				MIN	MAX	MIN	MAX	
F1	$t_{w(CSV)}$	$\overline{FLASH.CSx}$ low duration—Read operation	Async modes	A − 7	A + 7	13.84	27.84	ns
F3	$t_{d(CSV-ADIV)}$	Delay time, $\overline{FLASH.CSx}$ low to $\overline{FLASH.ADV}$ high	Async modes	B − 8.2	B + 4.53	2.22	14.95	ns
			Sync modes	M − 8.2	M + 4.53	12.64	25.37	
F4	$t_{d(CSV-OEIV)}$	Delay time, $\overline{FLASH.CSx}$ low to $\overline{FLASH.OE}$ high	Async modes	C − 7.3	C + 4.11	13.54	24.95	ns
F9	$t_{d(CSV-AV)}$	Delay time, $\overline{FLASH.CSx}$ low to address valid	Async and sync modes	−8.7	7.8	−8.7	7.8	ns
F10	$t_{d(CSV-BEV)}$	Delay time, $\overline{FLASH.CSx}$ low to $\overline{FLASH.BEx}$ valid	Async and sync modes	−5.4	3.9	−5.4	3.9	ns
F11	$t_{d(CSIV-BEIV)}$	Delay time, $\overline{FLASH.CSx}$ high to $\overline{FLASH.BEx}$ invalid	Async and sync modes	−5.4	3.9	−5.4	3.9	ns
F12	$t_{d(CSV-ADV)}$	Delay time, $\overline{FLASH.CSx}$ low to $\overline{FLASH.ADV}$ low	Async and sync modes	−8.2	4.53	−8.2	4.53	ns
F13	$t_{d(CSV-OEV)}$	Delay time, $\overline{FLASH.CSx}$ low to $\overline{FLASH.OE}$ low	Async (OESETUP = 0) and sync modes	− 7.3	4.11	−7.3	4.11	ns
F14	$t_{d(CSIV-ADIV)}$	Delay time, $\overline{FLASH.CSx}$ high to $\overline{FLASH.ADV}$ high	Async modes	−8.2	4.53	−8.2	4.53	ns

† The maximum EMIFS/flash clock rate is limited to the maximum traffic controller clock rate for the OMAP5912, provided all EMIFS/flash timing constraints are met.

‡ See Section 5.7.1.1 for information on and an example of how to calculate OMAP5912 EMIFS NOR Flash timings.

A = (RDWST + 2) * EMIFS clock period (REF_CLK)
B = (ADVHOLD + 1) * EMIFS clock period (REF_CLK)
C = (RDWST – OEHOLD +2) * EMIFS clock period (REF_CLK)
D = (PGWST + 1) * EMIFS clock period (REF_CLK)
E = (WRWST + WELEN + 3) * EMIFS clock period (REF_CLK)
F = (WRWST + 1) * EMIFS clock period (REF_CLK)
G = (WELEN + 1) * EMIFS clock period (REF_CLK)
H = 1 * EMIFS clock period (REF_CLK)
I = 0.5 * EMIFS clock period (REF_CLK)
J = (BTWST + 1) * EMIFS clock period (REF_CLK)
K = OESETUP * EMIFS clock period (REF_CLK)
L = OEHOLD * EMIFS clock period (REF_CLK)
M = (ADVHOLD + 1) * EMIFS clock period (REF_CLK) + 1 TC_CK period

Table 5−12. Sample Timing Calculation of Table 5−10 Parametric Values Using Constraints Calculated Above (Continued)

NO	PARAMETER			DATASHEET VALUES (FROM TABLE 5−10) DV_{DD5} = 1.8 V/2.75 V/3.3 V NOMINAL		AUTOMATIC TIMING CALCULATIONS DV_{DD5} = 1.8 V/2.75 V/3.3 V NOMINAL		UNIT
				MIN	MAX	MIN	MAX	
F15	$t_{d(CSIV-OEIV)}$	Delay time, $\overline{FLASH.CSx}$ high to $\overline{FLASH.OE}$ high	Async (OEHOLD = 0) and sync modes	− 7.3	4.11	−7.3	4.11	ns
F16	$t_{w(CSIV)}$	$\overline{FLASH.CSx}$ high duration—Read operation	Async modes	J − 7	J + 7	3.42	17.42	ns
F17	$t_{d(CSV−OEV)}$	Delay time, $\overline{FLASH.CSx}$ low to $\overline{FLASH.OE}$ low	Async modes	K − 7.3	K + 4.11	− 7.3	4.11	ns
F18	$t_{d(OEIV−CSIV)}$	Delay time, $\overline{FLASH..OE}$ high to $\overline{FLASH.CSx}$ high	Async modes	L − 7.3	L + 4.11	− 7.3	4.11	ns
F19	$t_{w(AV)}$	Address valid duration—1st access	Async modes	A − 5.6	A + 6.25	15.24	27.07	ns
F20	$t_{w(AV)}$	Address valid duration—2nd, 3rd, and 4th accesses	Async modes	D − 5.6	D + 6.25	4.82	16.65	ns
F23	$t_{w(CSV)}$	$\overline{FLASH.CSx}$ low duration—Write operation	Async modes	E − 7	E + 7	24.26	38.26	ns
F23/2	$t_{w(WEV)}$	$\overline{FLASH.WE}$ low duration—Write operation	Async modes	G − 1.4	G + 1.4	9.02	11.82	ns
F25	$t_{d(CSV-WEV)}$	Delay time, $\overline{FLASH.CSx}$ low to $\overline{FLASH.WE}$ low	Async modes	F − 6.6	F + 3.29	3.82	13.71	ns

† The maximum EMIFS/flash clock rate is limited to the maximum traffic controller clock rate for the OMAP5912, provided all EMIFS/flash timing constraints are met.

‡ See Section 5.7.1.1 for information on and an example of how to calculate OMAP5912 EMIFS NOR Flash timings.
A = (RDWST + 2) * EMIFS clock period (REF_CLK)
B = (ADVHOLD + 1) * EMIFS clock period (REF_CLK)
C = (RDWST – OEHOLD +2) * EMIFS clock period (REF_CLK)
D = (PGWST + 1) * EMIFS clock period (REF_CLK)
E = (WRWST + WELEN + 3) * EMIFS clock period (REF_CLK)
F = (WRWST + 1) * EMIFS clock period (REF_CLK)
G = (WELEN + 1) * EMIFS clock period (REF_CLK)
H = 1 * EMIFS clock period (REF_CLK)
I = 0.5 * EMIFS clock period (REF_CLK)
J = (BTWST + 1) * EMIFS clock period (REF_CLK)
K = OESETUP * EMIFS clock period (REF_CLK)
L = OEHOLD * EMIFS clock period (REF_CLK)
M = (ADVHOLD + 1) * EMIFS clock period (REF_CLK) + 1 TC_CK period

Table 5−12. Sample Timing Calculation of Table 5−10 Parametric Values Using Constraints Calculated Above (Continued)

NO	PARAMETER			DATASHEET VALUES (FROM TABLE 5−10) DV_{DD5} = 1.8 V/2.75 V/3.3 V NOMINAL		AUTOMATIC TIMING CALCULATIONS DV_{DD5} = 1.8 V/2.75 V/3.3 V NOMINAL		UNIT
				MIN	MAX	MIN	MAX	
F27	$t_{d(WEIV-CSIV)}$	Delay time, $\overline{FLASH.WE}$ high to $\overline{FLASH.CSx}$ high	Async modes	H − 3.29	H + 6.6	7.13	17.02	ns
F27/2	$t_{d(WEIV-AIV)}$	Delay time, $\overline{FLASH.WE}$ high to FLASH.A[25:1] invalid	Async modes	P − 3.5	P + 6.3	6.92	16.72	ns
F27/3	$t_{d(WEIV-DIV)}$	Delay time, $\overline{FLASH.WE}$ high to FLASH.D[15:0] invalid	Async modes	P − 4.4	P + 1.812	6.02	12.23	ns
F28	$t_{d(CSV-DLZ)}$	Delay time, $\overline{FLASH.CSx}$ low to data bus driven	Async modes	−13.9	0.4	−13.9	0.4	ns
F29	$t_{d(CSV-DV)}$	Delay time, $\overline{FLASH.CSx}$ low to data bus valid	Async modes	−12.9	2.19	−12.9	2.19	ns
F30	$t_{d(CSIV-DIV)}$	Delay time, $\overline{FLASH.CSx}$ high to data bus invalid	Async modes	−12.9	2.19	−12.9	2.19	ns
F31	$t_{d(CSIV-DHZ)}$	Delay time, $\overline{FLASH.CSx}$ high to data bus high Z	Async modes	−13.9	0.4	−13.9	0.4	ns
F35	$t_{d(CLKH-BAA)}$	Delay time, FLASH.CLK high to $\overline{FLASH.BAA}$ transition	Sync modes	I + 0.68	I + 8	5.89	13.21	ns

† The maximum EMIFS/flash clock rate is limited to the maximum traffic controller clock rate for the OMAP5912, provided all EMIFS/flash timing constraints are met.

‡ See Section 5.7.1.1 for information on and an example of how to calculate OMAP5912 EMIFS NOR Flash timings.

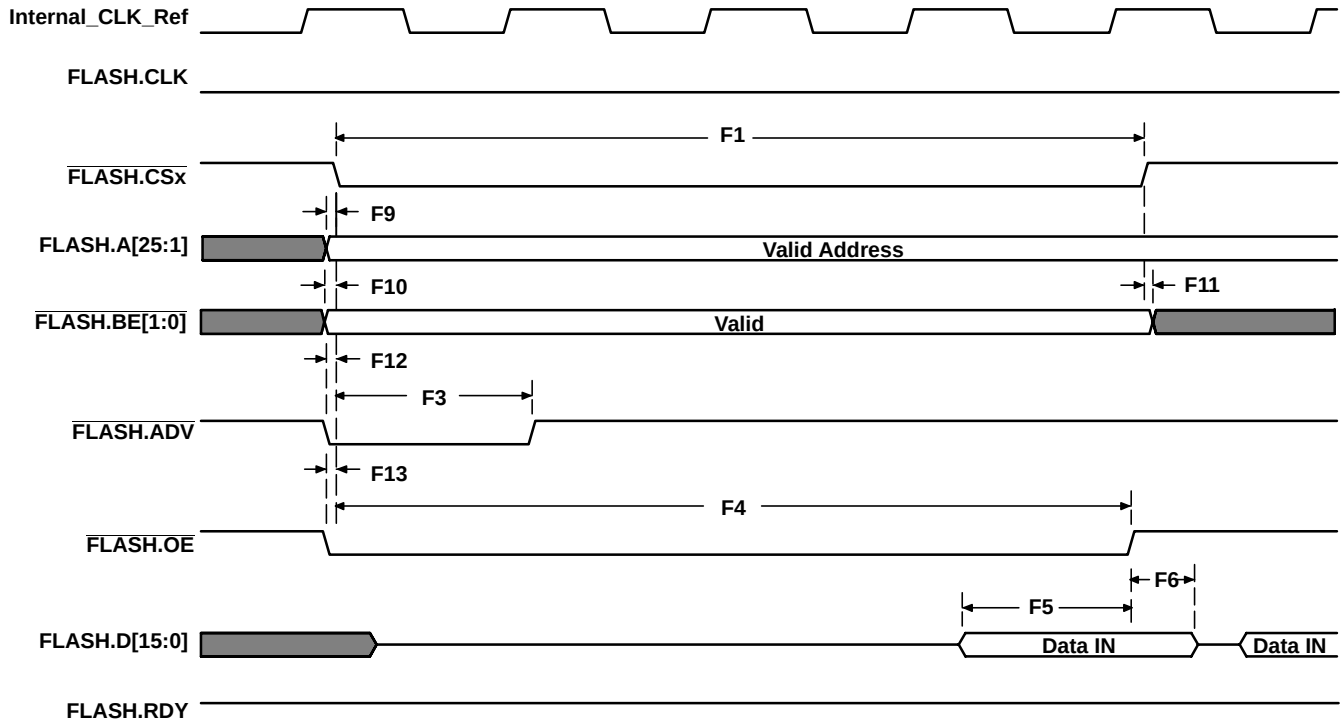
A = (RDWST + 2) * EMIFS clock period (REF_CLK)
B = (ADVHOLD + 1) * EMIFS clock period (REF_CLK)
C = (RDWST – OEHOLD +2) * EMIFS clock period (REF_CLK)
D = (PGWST + 1) * EMIFS clock period (REF_CLK)
E = (WRWST + WELEN + 3) * EMIFS clock period (REF_CLK)
F = (WRWST + 1) * EMIFS clock period (REF_CLK)
G = (WELEN + 1) * EMIFS clock period (REF_CLK)
H = 1 * EMIFS clock period (REF_CLK)
I = 0.5 * EMIFS clock period (REF_CLK)
J = (BTWST + 1) * EMIFS clock period (REF_CLK)
K = OESETUP * EMIFS clock period (REF_CLK)
L = OEHOLD * EMIFS clock period (REF_CLK)
M = (ADVHOLD + 1) * EMIFS clock period (REF_CLK) + 1 TC_CK period

Table 5−12. Sample Timing Calculation of Table 5−10 Parametric Values Using Constraints Calculated Above (Continued)

NO	PARAMETER			DATASHEET VALUES (FROM TABLE 5−10) DV_{DD5} = 1.8 V/2.75 V/3.3 V NOMINAL		AUTOMATIC TIMING CALCULATIONS DV_{DD5} = 1.8 V/2.75 V/3.3 V NOMINAL		UNIT
				MIN	MAX	MIN	MAX	
F36	$t_{d(CSV-CLKV)}$	Delay time, $\overline{\text{FLASH.CSx}}$ low to FLASH.CLK high	$\overline{\text{FLASH.CS0}}$ Sync modes	H − 9.3		1.12		ns
			$\overline{\text{FLASH.CS1}}$, $\overline{\text{FLASH.CS2}}$, $\overline{\text{FLASH.CS3}}$ Sync modes	H − 8.1		2.32		ns
F37	$t_{d(CLKIV-CSIV)}$	Delay time, FLASH.CLK invalid to $\overline{\text{FLASH.CSx}}$ high	Sync modes	H + 0.1		10.52		ns
F40	$t_{d(OEV-DIV)}$	Delay time, $\overline{\text{FLASH.OE}}$ low to data bus invalid	Async and sync modes	−4.8	0.64	−4.8	0.64	ns
F41	$t_{d(OEV-DHZ)}$	Delay time, $\overline{\text{FLASH.OE}}$ low to data bus high Z	Async and sync modes	−8.9	0.5	−8.9	0.5	ns
F42	$t_{d(WEV-DIV)}$	Delay time, $\overline{\text{FLASH.WE}}$ low to data bus invalid	Async and sync modes	−4.5	1.93	−4.5	1.93	ns
F43	$t_{d(WEV-DV)}$	Delay time, $\overline{\text{FLASH.WE}}$ low to data bus valid	Async and sync modes	−4.5	1.93	−4.5	1.93	ns

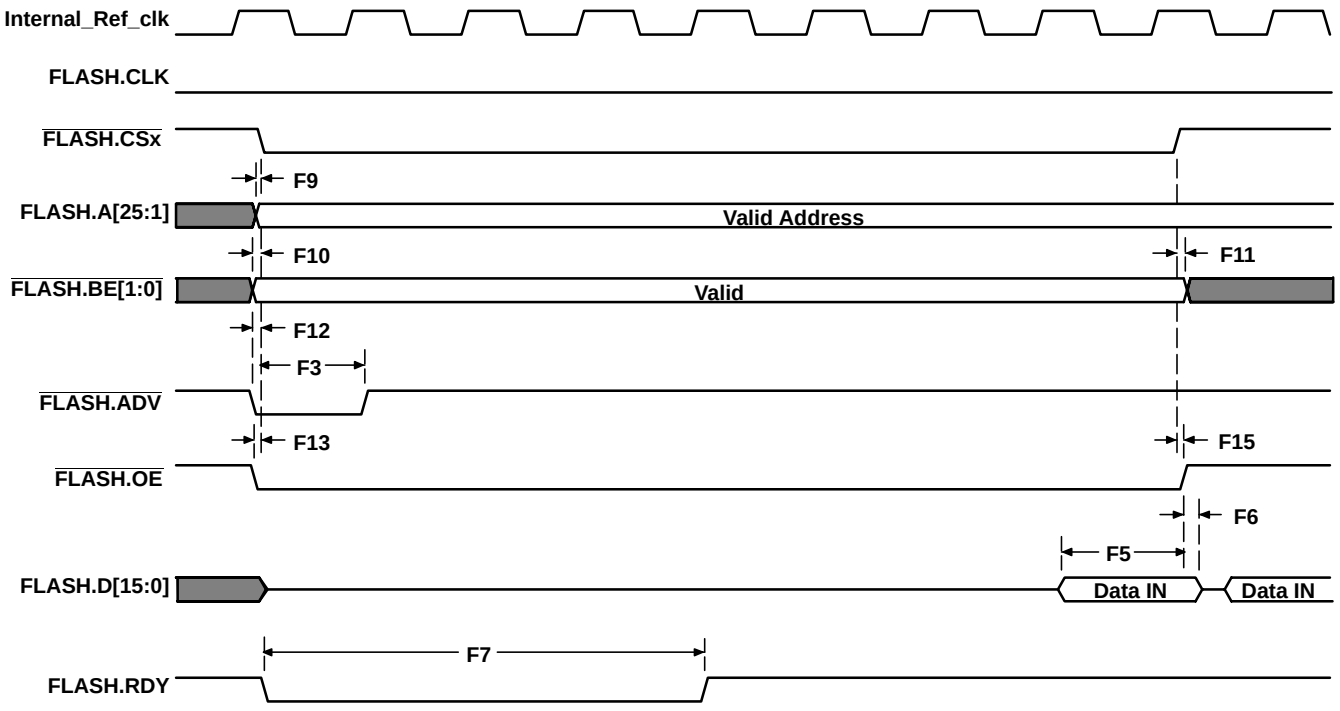
† The maximum EMIFS/flash clock rate is limited to the maximum traffic controller clock rate for the OMAP5912, provided all EMIFS/flash timing constraints are met.

‡ See Section 5.7.1.1 for information on and an example of how to calculate OMAP5912 EMIFS NOR Flash timings.
A = (RDWST + 2) * EMIFS clock period (REF_CLK)
B = (ADVHOLD + 1) * EMIFS clock period (REF_CLK)
C = (RDWST – OEHOLD +2) * EMIFS clock period (REF_CLK)
D = (PGWST + 1) * EMIFS clock period (REF_CLK)
E = (WRWST + WELEN + 3) * EMIFS clock period (REF_CLK)
F = (WRWST + 1) * EMIFS clock period (REF_CLK)
G = (WELEN + 1) * EMIFS clock period (REF_CLK)
H = 1 * EMIFS clock period (REF_CLK)
I = 0.5 * EMIFS clock period (REF_CLK)
J = (BTWST + 1) * EMIFS clock period (REF_CLK)
K = OESETUP * EMIFS clock period (REF_CLK)
L = OEHOLD * EMIFS clock period (REF_CLK)
M = (ADVHOLD + 1) * EMIFS clock period (REF_CLK) + 1 TC_CK period



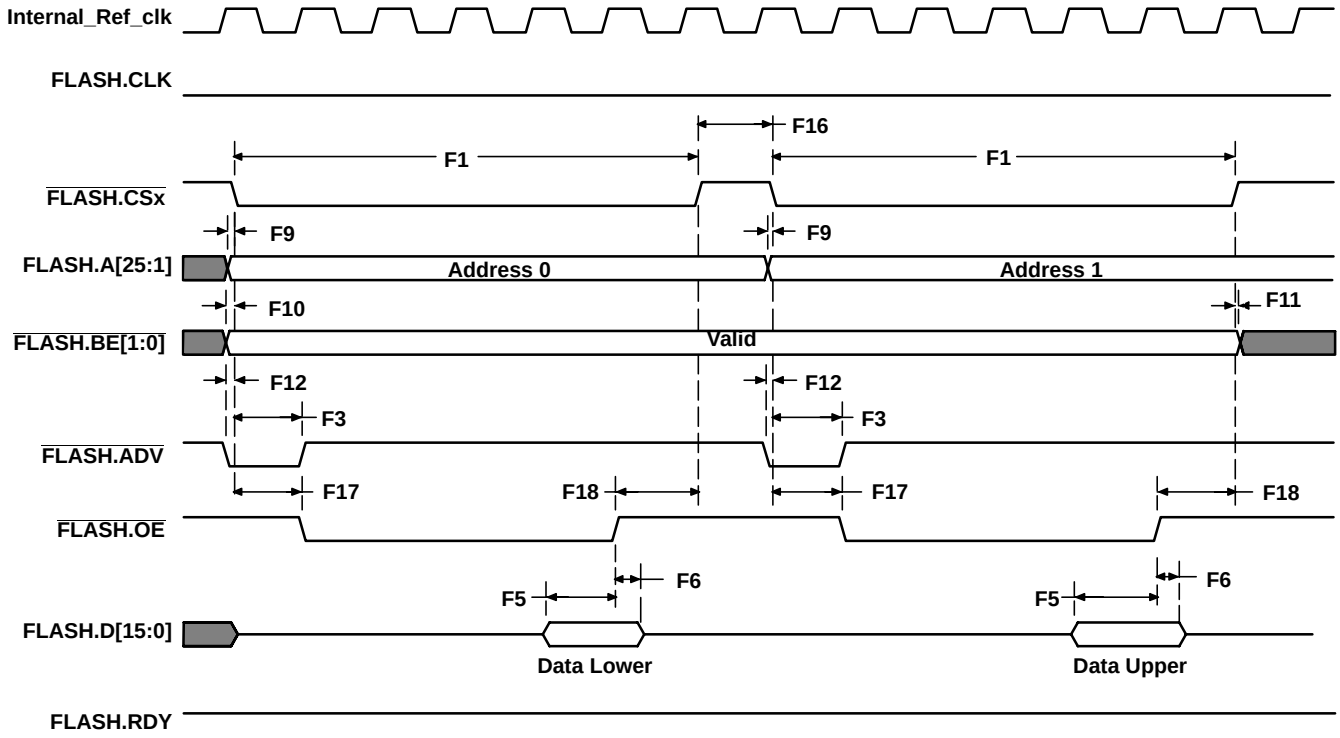
NOTE: RDWST = 2, ADVHOLD = 0, OESETUP = 0, OEHOLD = 0.

Figure 5−9. EMIFS/NOR Flash—Single Word Asynchronous Read



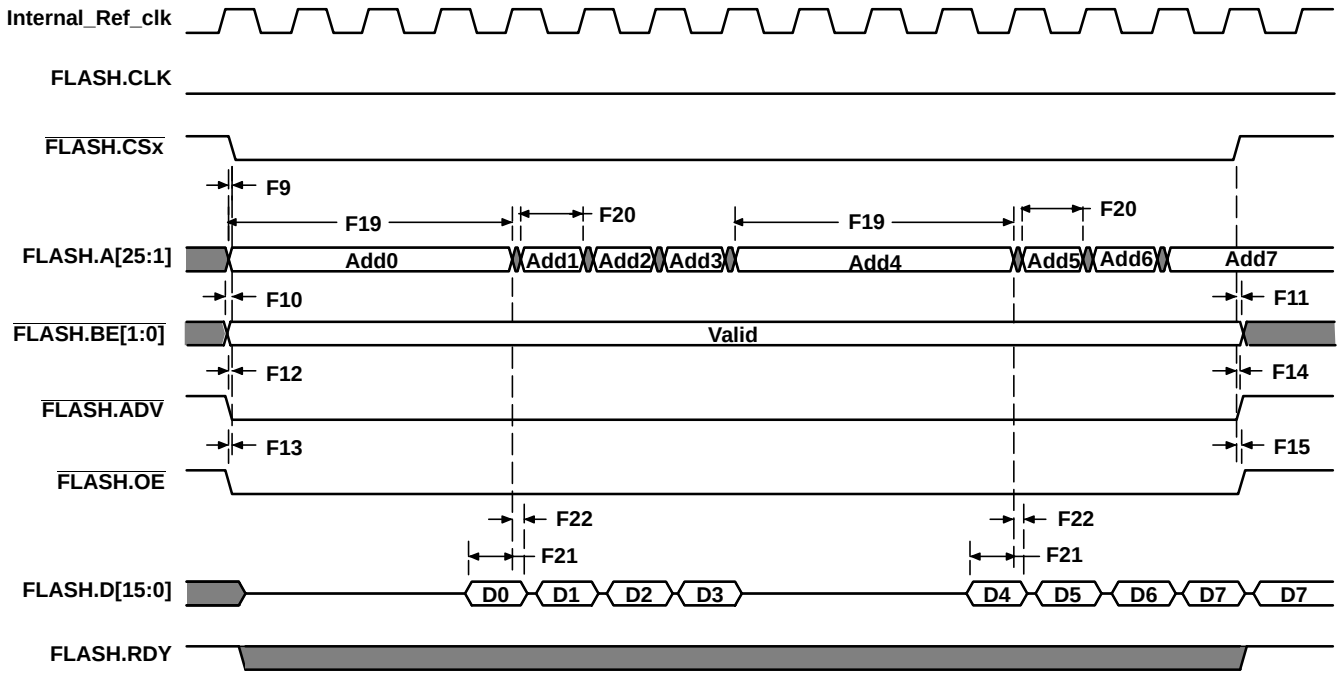
NOTE: RDWST = 2, ADVHOLD = 0, OESETUP = 0, OEHOLD = 0.

Figure 5−10. EMIFS/NOR Flash—Single Word Asynchronous Read, Full-Handshaking Mode Timing



NOTE: RDWST = 4, ADVHOLD = 0, OESETUP = 1, OEHOLD = 1, BTWST = 0, BTMODE = 0.

Figure 5−11. EMIFS/NOR Flash—Asynchronous 32-Bit Read Timing



NOTE: RDWST = 2, PGWST = 0

Figure 5−12. EMIFS/NOR Flash—Asynchronous Read, Page Mode 8 x 16-Bit Timing

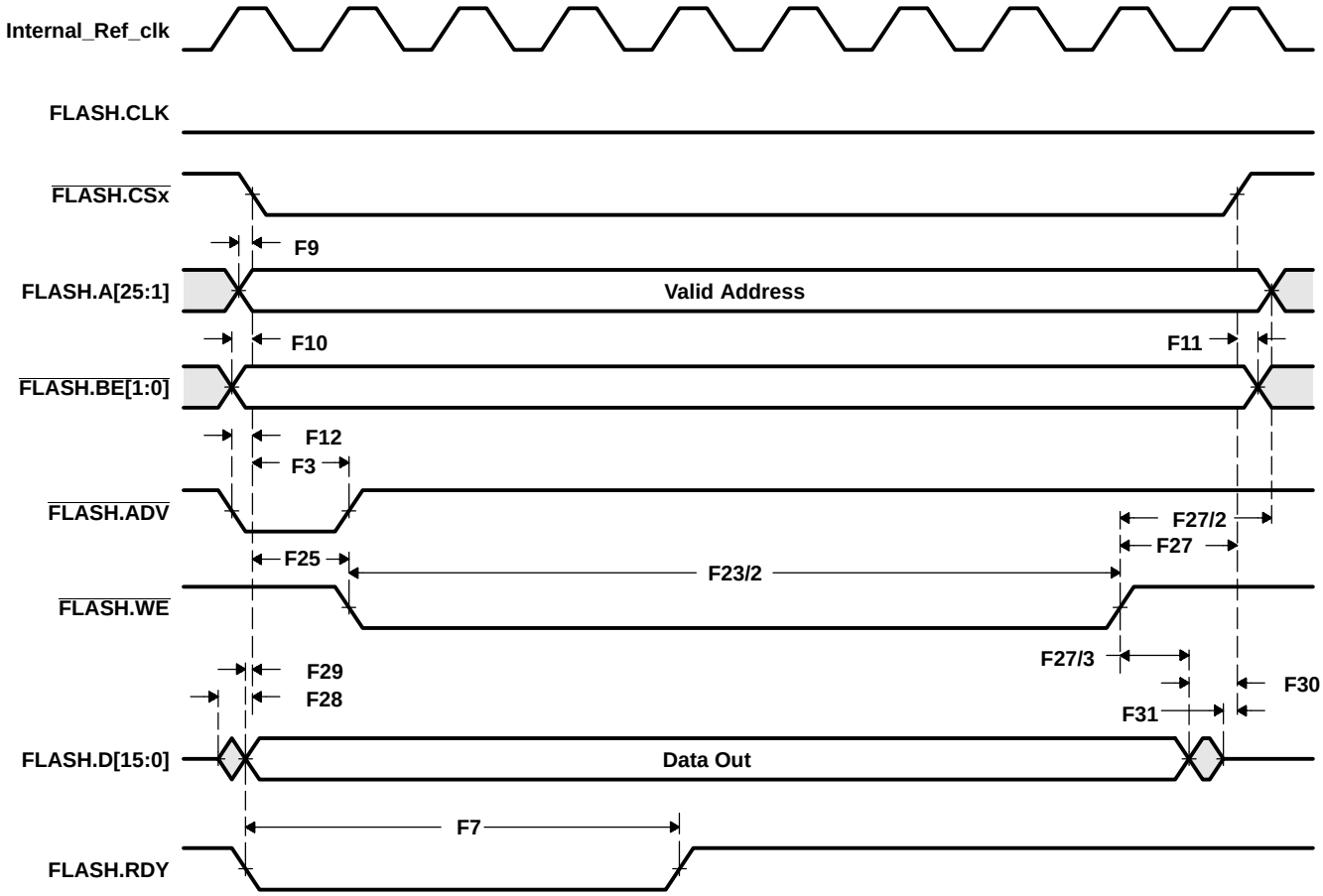


Figure 5−13. EMIFS/NOR Flash—Single Word Asynchronous Write Timing, Full-Handshaking Mode

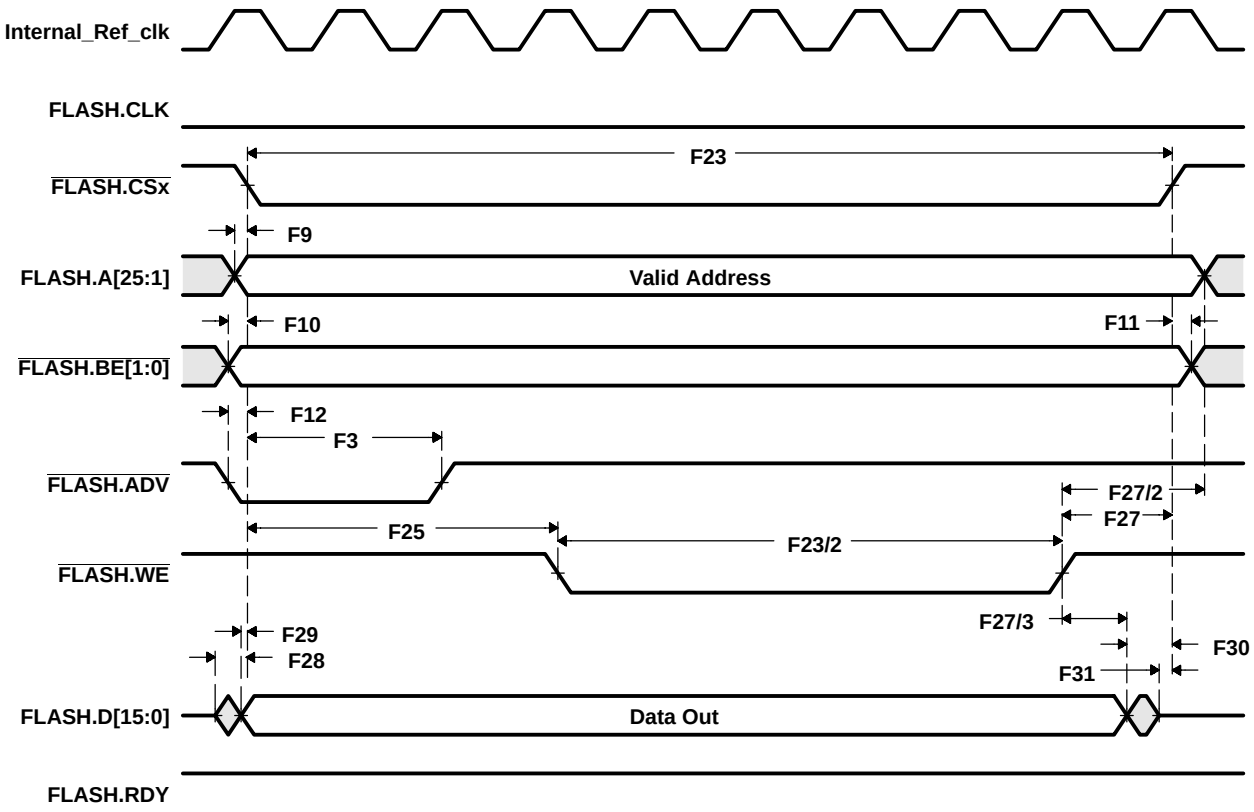
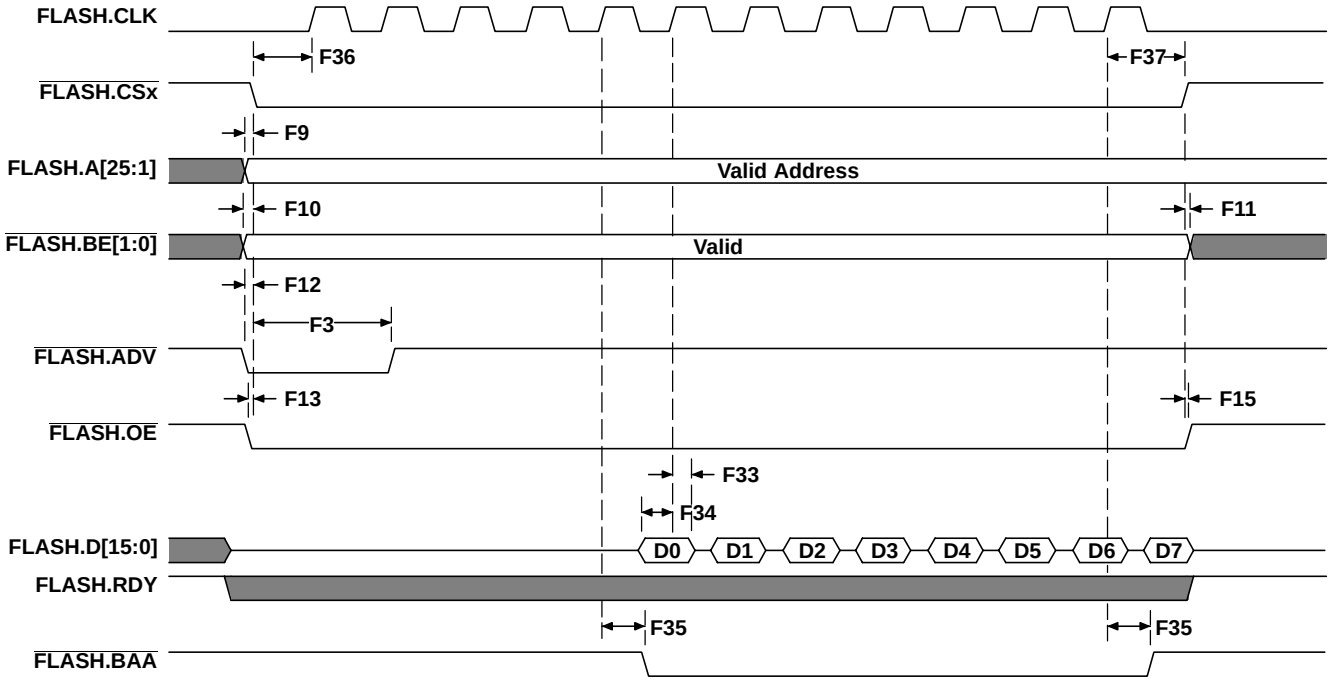
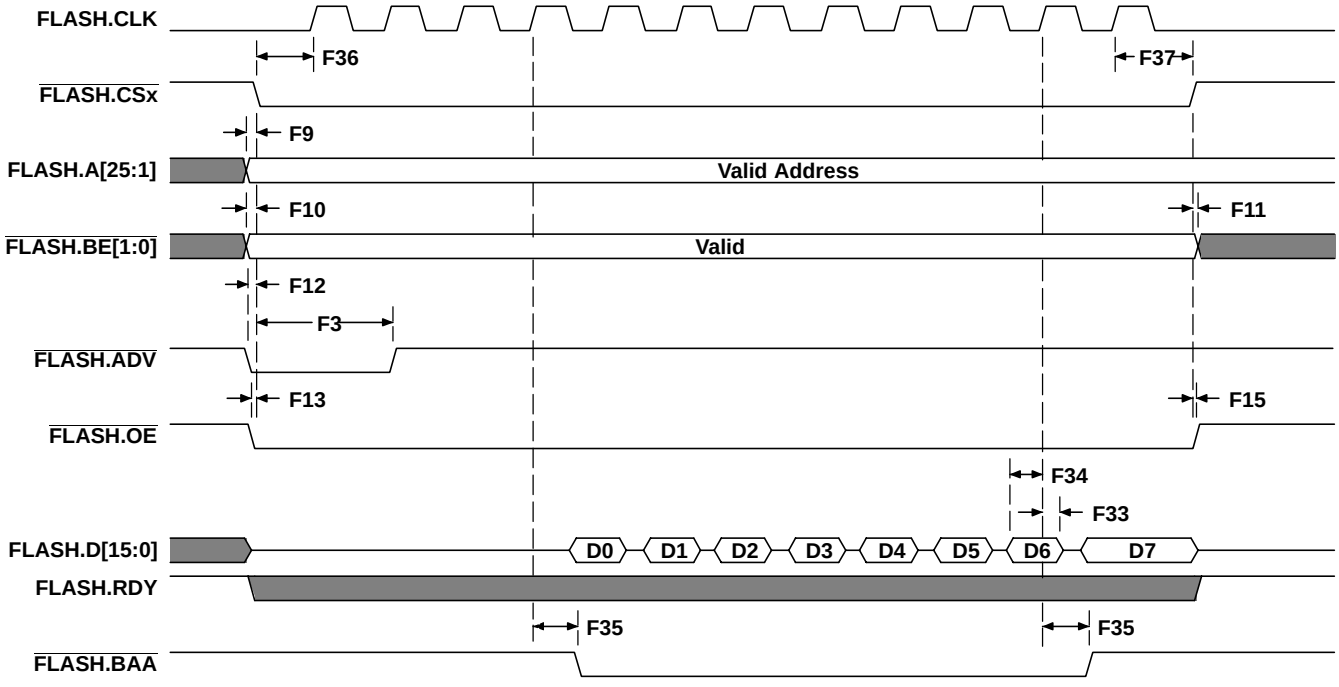


Figure 5−14. EMIFS/NOR Flash—Single Word Asynchronous Write



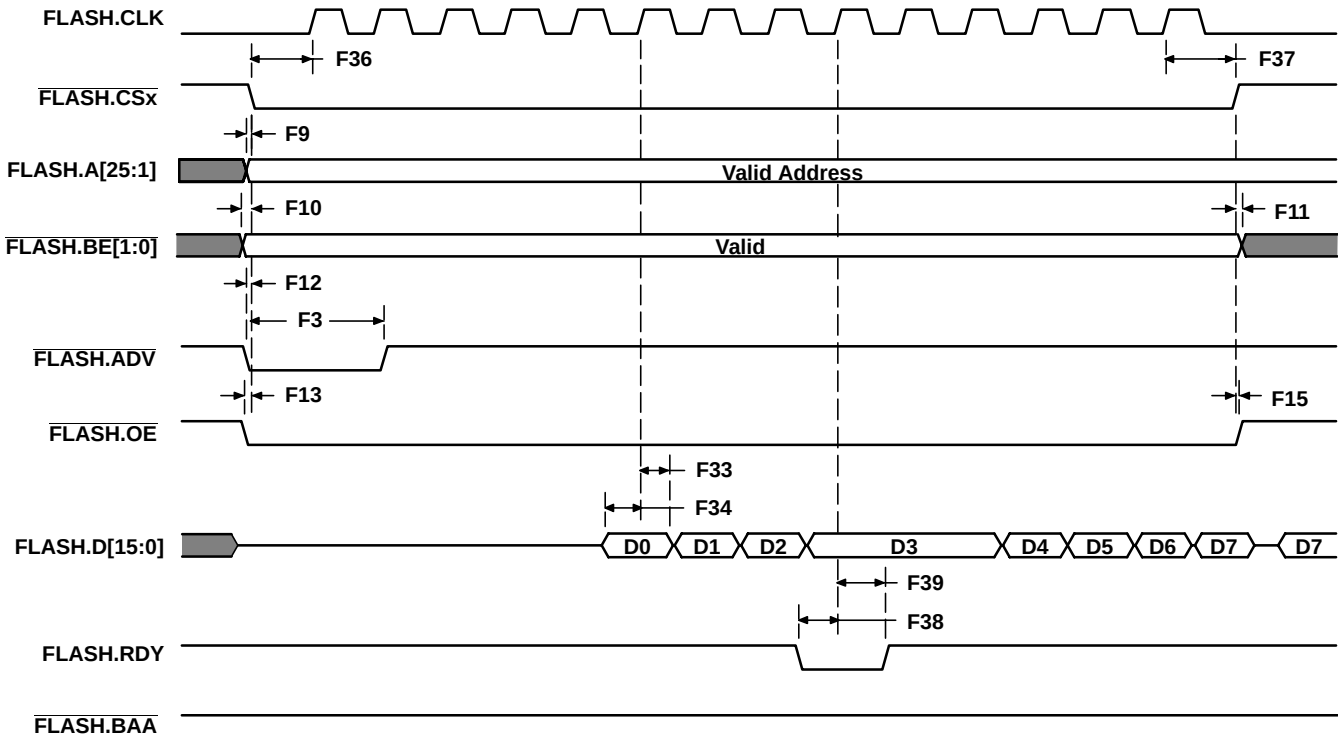
NOTE: RDWST = 4, ADVHOLD = 0

Figure 5−15. EMIFS/NOR Flash—Synchronous Burst Read Timing (Retiming Off, Mode 4)



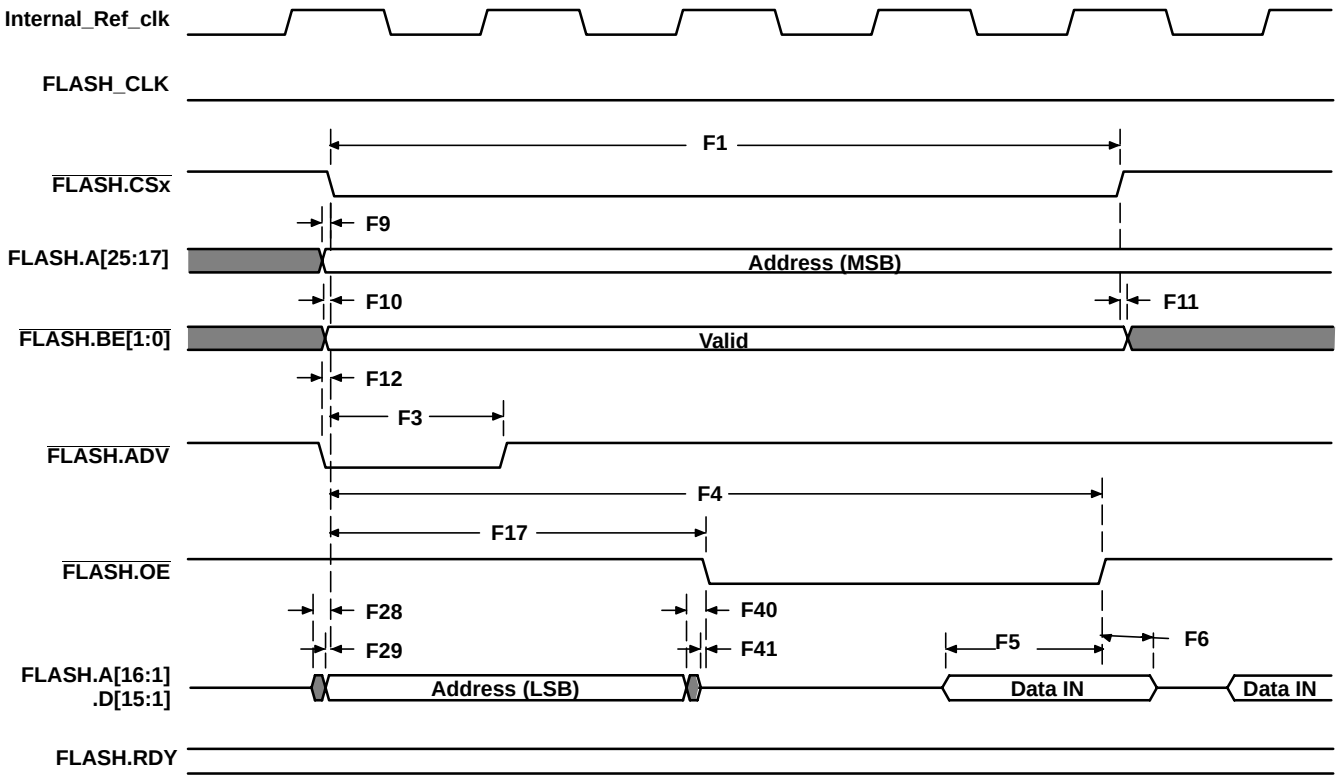
NOTE: RDWST = 4, ADVHOLD = 0

Figure 5−16. EMIFS/NOR Flash—Synchronous Burst Read Timing (Retiming On, Mode 4)



NOTE: RDWST = 4, ADVHOLD = 0

Figure 5−17. EMIFS/NOR Flash—Synchronous Burst Read Timing (Retiming Off, Mode 5)



NOTE: RDWST = 2, ADVHOLD = 0, OESETUP = 2, OEHOLD = 0

Figure 5−18. EMIFS/Multiplexed NOR Flash—Single Word Asynchronous Read Timing

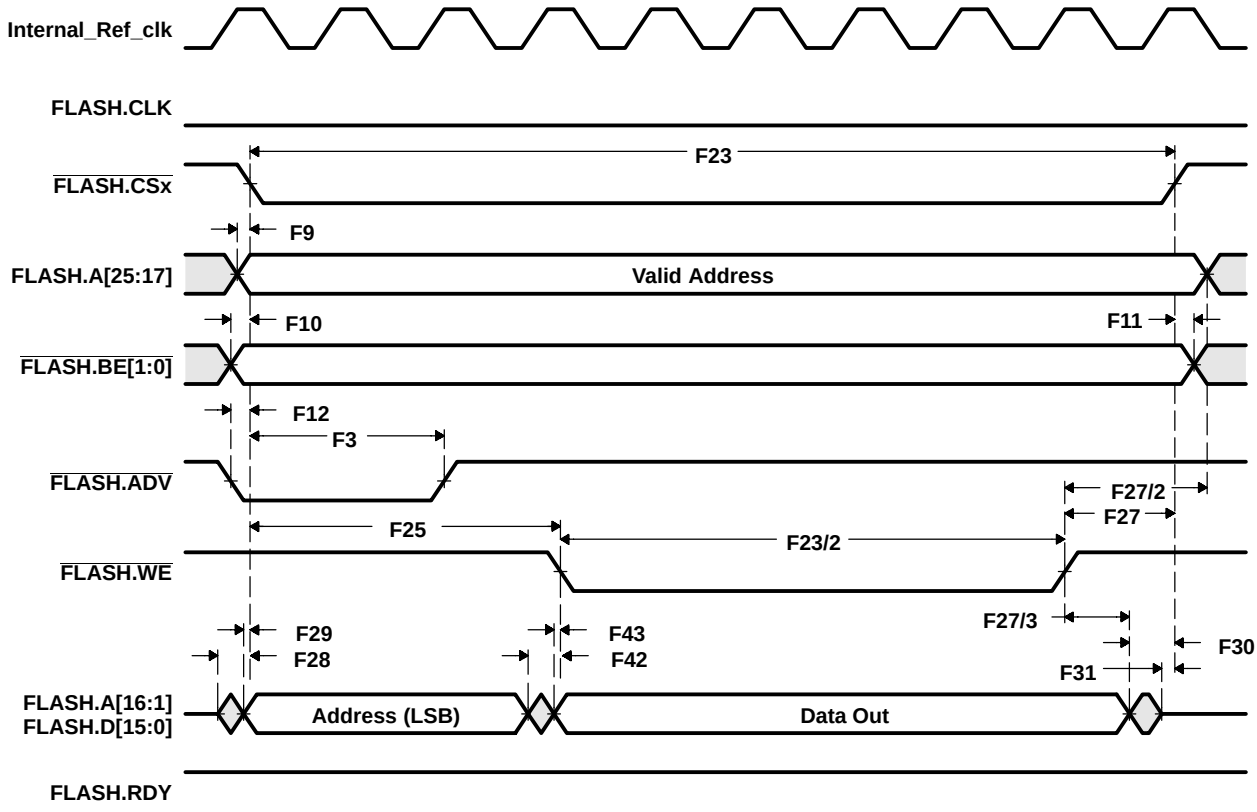
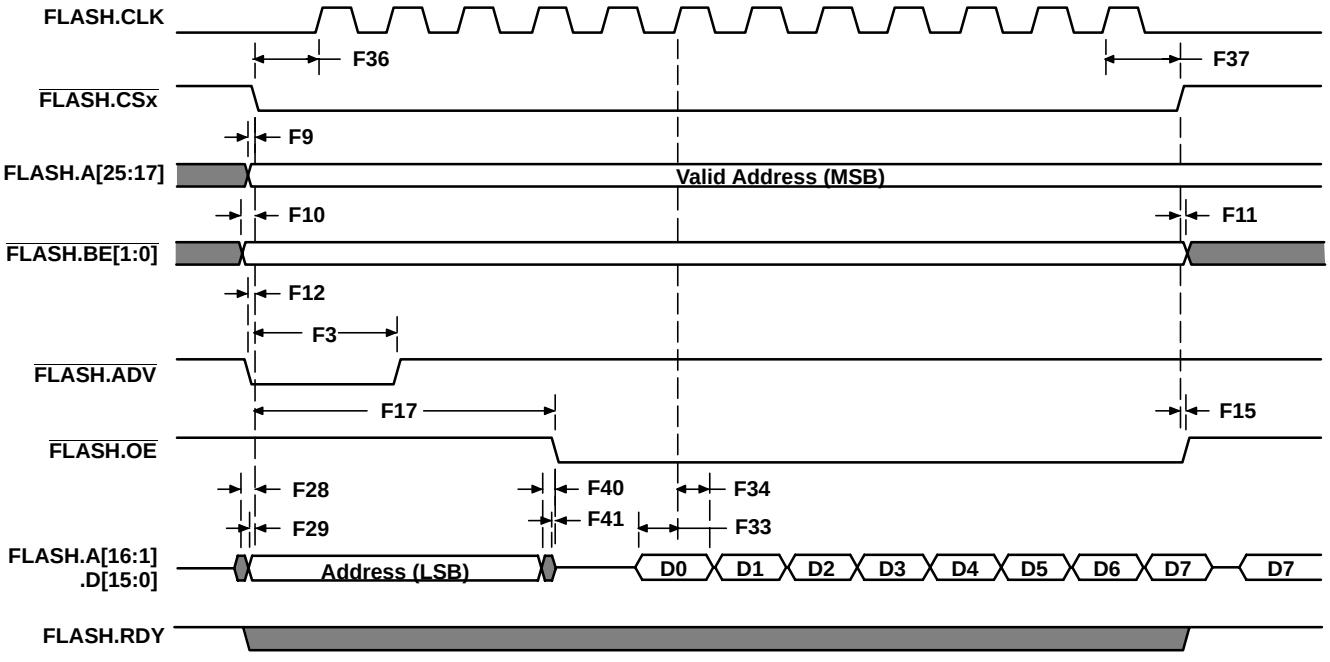


Figure 5−19. EMIFS/Multiplexed NOR Flash—Single Word Asynchronous Write Timing



NOTE: RDWST = 4, ADVHOLD = 0, OESETUP = 4

Figure 5−20. EMIFS/Multiplexed NOR Flash—Synchronous Burst Read Timing (Retiming Off)

5.7.2 EMIFS/NAND Flash Timing

Table 5−13 and Table 5−14 assume testing over operating conditions (see Figure 5−21 through Figure 5−24).

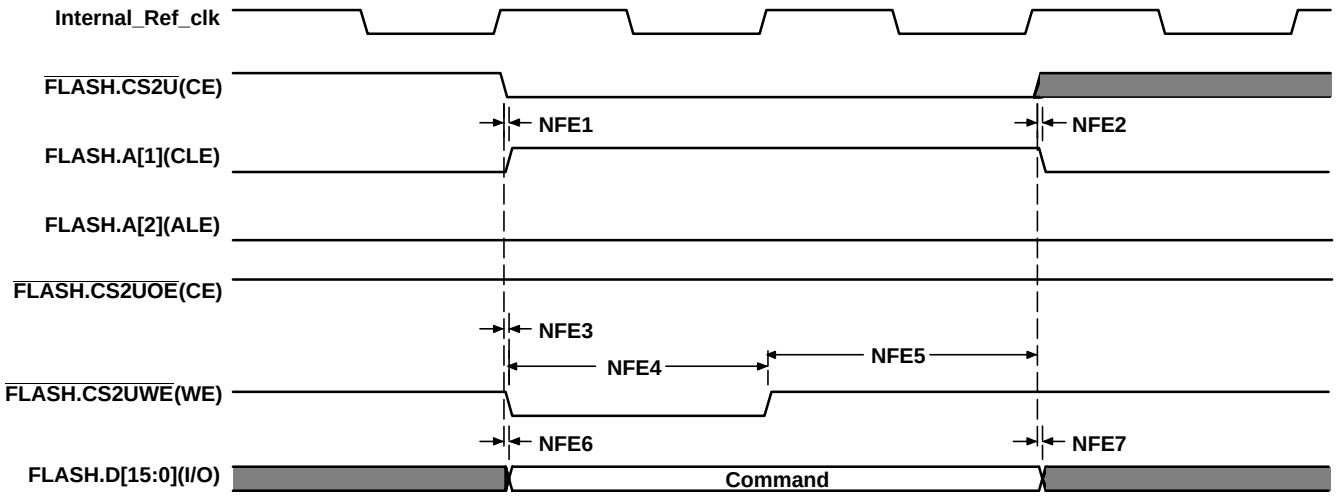
Table 5−13. EMIFS/NAND Flash Timing Requirements

NO			DV_{DD5} = 1.8 V NOMINAL		DV_{DD5} = 2.75 V/3.3 V NOMINAL		UNIT
			MIN	MAX	MIN	MAX	
NFE14	$t_{su(DV-REH)}$	Setup time, input FLASH.D[15:0] valid before $\overline{\text{FLASH.CS2UOE}}$(RE) high	33.75		30.75		ns
NFE15	$t_{h(REH-DV)}$	Hold time, input FLASH.D[15:0] valid after $\overline{\text{FLASH.CS2UOE}}$(RE) high	−2		−2		ns

Table 5−14. EMIFS/NAND Flash Switching Characteristics

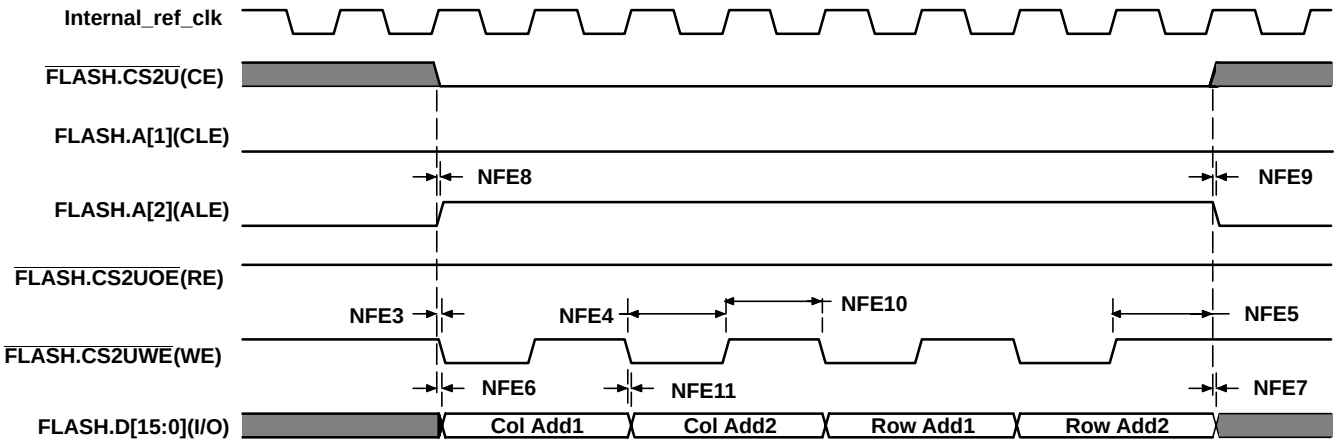
NO	PARAMETER		DV_{DD5} = 1.8 V NOMINAL		DV_{DD5} = 2.75 V/3.3 V NOMINAL		UNIT
			MIN	MAX	MIN	MAX	
NFE1	$t_{d(CEV-CLEV)}$	Delay time, $\overline{\text{FLASH.CS2U}}$(CE) low to FLASH.A[1] (CLE) high	−0.75	−0.15	−1.2	−0.15	ns
NFE2	$t_{d(CEIV-CLEIV)}$	Delay time, $\overline{\text{FLASH.CS2U}}$(CE) high to FLASH.A[1] (CLE) low	−1.2	−0.15	−1	−0.15	ns
NFE3	$t_{d(CEV-WEV)}$	Delay time, $\overline{\text{FLASH.CS2U}}$(CE) low to $\overline{\text{FLASH.CS2UWE}}$(WE) low	−0.6	3.15	−0.6	3.5	ns
NFE4	$t_{w(WEV)}$	$\overline{\text{FLASH.CS2UWE}}$(WE) low duration	P − 2.25†	P + 0.45†	P − 2.1†	P + 0.6†	ns
NFE5	$t_{d(WEIV-CEIV)}$	Delay time, $\overline{\text{FLASH.CS2UWE}}$(WE) high to $\overline{\text{FLASH.CS2U}}$(CE) high	P − 0.9†	P + 2†	P − 0.9†	P + 1.8†	ns
NFE6	$t_{d(CEV-DV)}$	Delay time, $\overline{\text{FLASH.CS2U}}$(CE) low to FLASH.D[15:0] (I/O) valid	−7.35	−0.55	−6.15	−0.65	ns
NFE7	$t_{d(CEIV-DIV)}$	Delay time, $\overline{\text{FLASH.CS2U}}$(CE) high to FLASH.D[15:0] (I/O) invalid	−7.2	−0.6	−6.15	−0.65	ns
NFE8	$t_{d(CEV-ALEV)}$	Delay time, $\overline{\text{FLASH.CS2U}}$(CE) low to FLASH.A[2] (ALE) high	−1.65	−0.15	−1.8	−0.2	ns
NFE9	$t_{d(CEIV-ALEIV)}$	Delay time, $\overline{\text{FLASH.CS2U}}$(CE) high to FLASH.A[2] (ALE) low	−1.65	−0.2	−1.8	−0.2	ns
NFE10	$t_{w(WEIV)}$	$\overline{\text{FLASH.CS2UWE}}$(WE) high duration	P − 4.5†	P + 2.25†	P − 0.6†	P + 2.1†	ns
NFE11	$t_{d(WEV-DV)}$	Delay time, $\overline{\text{FLASH.CS2UWE}}$(WE) low to FLASH.D[15:0] (I/O) valid/invalid	−10.35	−0.5	−9.15	−0.6	ns
NFE12	$t_{w(REV)}$	$\overline{\text{FLASH.CS2UOE}}$(RE) low duration	P − 3.15†	P + 3†	P − 3.15†	P + 2.85†	ns
NFE13	$t_{w(REIV)}$	$\overline{\text{FLASH.CS2UOE}}$(RE) high duration	P − 3.15†	P + 3.15†	P − 2.85†	P + 3.15†	ns

† P = EMIFS clock period (Ref_clk).



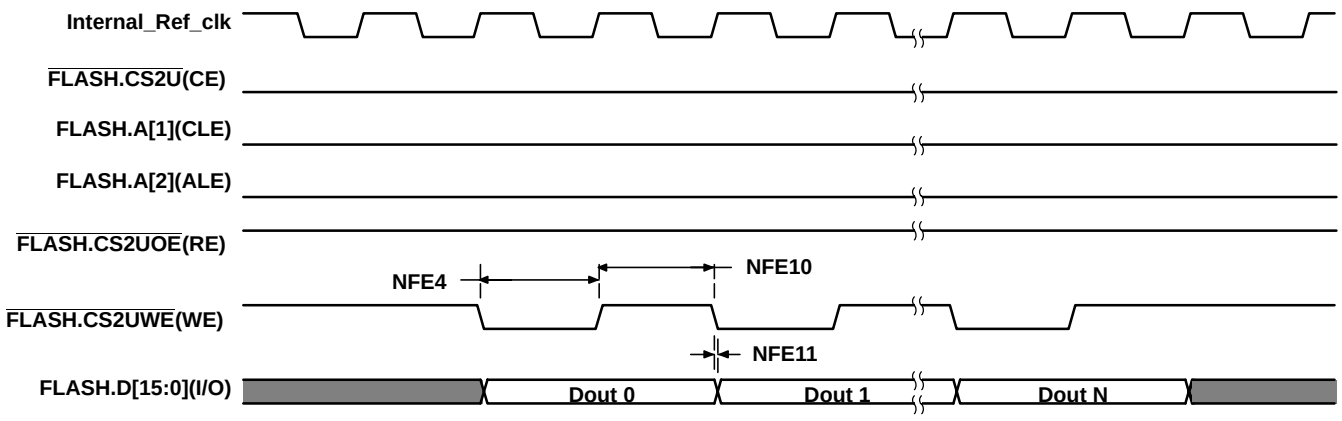
NOTES: A. FLASH.CLK is not driven during this mode of operation. The signal shown represents the internal FLASH.CLK signal given as a reference.
B. In case of use of a NAND CE care flash type, FLASH.CS2U is a combination of a GPIO (controlled by software—no timing) and CS2U (internal).

Figure 5−21. EMIFS/NAND Flash—Command Latch Timing



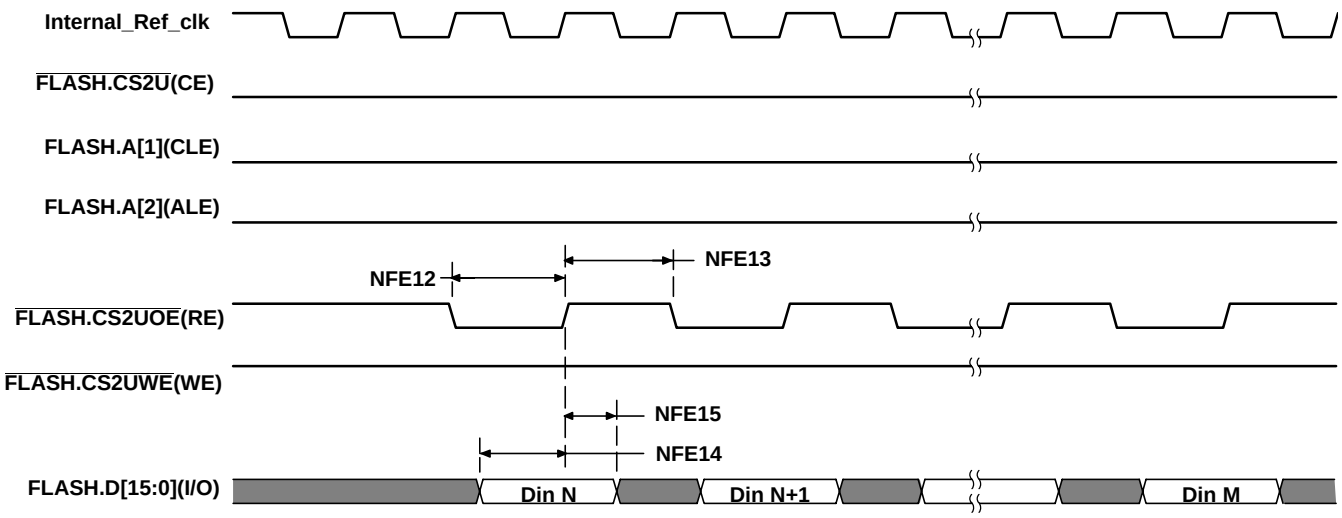
NOTES: A. FLASH.CLK is not driven during this mode of operation. The signal shown represents the internal FLASH.CLK signal given as a reference.
B. In case of use of a NAND CE care flash type, FLASH.CS2U is a combination of a GPIO (controlled by software—no timing) and CS2U (internal).

Figure 5−22. EMIFS/NAND Flash—Address Latch Timing



NOTES: A. FLASH.CLK is not driven during this mode of operation. The signal shown represents the internal FLASH.CLK signal given as a reference.
B. In case of use of a NAND CE care flash type, FLASH.CS2U is a combination of a GPIO (controlled by software—no timing) and CS2U (internal).

Figure 5−23. EMIFS/NAND Flash—Memory Write Timing



NOTES: A. FLASH.CLK is not driven during this mode of operation. The signal shown represents the internal FLASH.CLK signal given as a reference.
B. In case of use of a NAND CE care flash type, FLASH.CS2U is a combination of a GPIO (controlled by software—no timing) and CS2U (internal).

Figure 5−24. EMIFS/NAND Flash—Memory Read Timing

5.8 EMIFF/SDR SDRAM Interface Timing

Table 5−15 and Table 5−16 assume testing over recommended operating conditions (see Figure 5−25 through Figure 5−30).

Table 5−15. EMIFF/SDR SDRAM Interface Timing Requirements

NO			DV_{DD4} = 1.8 V NOMINAL†		DV_{DD4} = 2.75 V/3.3 V NOMINAL†		UNIT
			MIN	MAX	MIN	MAX	
SD7	$t_{su(DV–CLKH)}$	Setup time, read data valid before SDRAM.CLK high	1		1		ns
SD8	$t_{h(CLKH–DV)}$	Hold time, read data valid after SDRAM.CLK high	1.5		1.5		ns

† The control bit CONF_VOLTAGE_SDRAM_R of the register VOLTAGE_CTRL_0 must be set to 1 regardless of the DV_{DD4} voltage level.

Table 5−16. EMIFF/SDR SDRAM Interface Switching Characteristics‡§

NO	PARAMETER		DV_{DD4} = 1.8 V NOMINAL†		DV_{DD4} = 2.75 V/3.3 V NOMINAL†		UNIT
			MIN	MAX	MIN	MAX	
SD1	$t_{c(CLK)}$	Cycle time, SDRAM.CLK	10.41		10.41		ns
SD2	$t_{w(CLK)}$	Pulse duration, SDRAM.CLK high or low	0.45P	0.55P	0.45P	0.55P	ns
SD3	$t_{d(CLKH–DQMV)}$	Delay time, SDRAM.CLK high to SDRAM.DQMx valid		1.20¶		1.22¶	ns
SD4	$t_{d(CLKH–DQMIV)}$	Delay time, SDRAM.CLK high to SDRAM.DQMx invalid	0.23¶		0.30¶		ns
SD5	$t_{d(CLKH–AV)}$	Delay time, SDRAM.CLK high to SDRAM.A[13:0] address valid		0.5P + 1.49		0.5P + 1.63	ns
SD6	$t_{d(CLKH–AIV)}$	Delay time, SDRAM.CLK high to SDRAM.A[13:0] address invalid	0.5P		0.5P		ns
SD9	$t_{d(CLKH–SDCASL)}$	Delay time, SDRAM.CLK high to $\overline{\text{SDRAM.CAS}}$ low	0.5P	0.5P + 1.18	0.5P	0.5P + 1.40	ns
SD10	$t_{d(CLKH–SDCASH)}$	Delay time, SDRAM.CLK high to $\overline{\text{SDRAM.CAS}}$ high	0.5P	0.5P + 1.18	0.5P	0.5P + 1.40	ns
SD11	$t_{d(CLKH–DV)}$	Delay time, SDRAM.CLK high to SDRAM.D[15:0] data valid		0.5P + 0.60		0.5P + 0.75	ns
SD12	$t_{d(CLKH–DIV)}$	Delay time, SDRAM.CLK high to SDRAM.D[15:0] data invalid	0.5P		0.5P		ns
SD13	$t_{d(CLKH–SDWEL)}$	Delay time, SDRAM.CLK high to $\overline{\text{SDRAM.WE}}$ low	0.5P	0.5P + 1.26	0.5P	0.5P + 1.44	ns
SD14	$t_{d(CLKH–SDWEH)}$	Delay time, SDRAM.CLK high to $\overline{\text{SDRAM.WE}}$ high	0.5P	0.5P + 1.26	0.5P	0.5P + 1.44	ns
SD15	$t_{d(CLKH–BAV)}$	Delay time, SDRAM.CLK high to SDRAM.BA[1:0] valid		0.5P + 1.44		0.5P + 1.55	ns
SD16	$t_{d(CLKH–BAIV)}$	Delay time, SDRAM.CLK high to SDRAM.BA[1:0] invalid	0.5P		0.5P		ns
SD17	$t_{d(CLKH–RASL)}$	Delay time, SDRAM.CLK high to $\overline{\text{SDRAM.RAS}}$ low	0.5P	0.5P + 1.50	0.5P	0.5P + 1.78	ns
SD18	$t_{d(CLKH–RASH)}$	Delay time, SDRAM.CLK high to $\overline{\text{SDRAM.RAS}}$ high	0.5P	0.5P + 1.50	0.5P	0.5P + 1.78	ns

† The control bit CONF_VOLTAGE_SDRAM_R of the register VOLTAGE_CTRL_0 must be set to 1 regardless of the DV_{DD4} voltage level.
‡ The maximum EMIFF/SDRAM clock rate is limited to the maximum traffic controller clock rate for the OMAP5912.
§ P = SDRAM.CLK period in nanoseconds. Minimum value of P is determined by maximum traffic controller frequency.
¶ An external delay element of between 1 ns to 5 ns must be added to the OMAP5912 DQM signal for proper operation with SDRAMs.

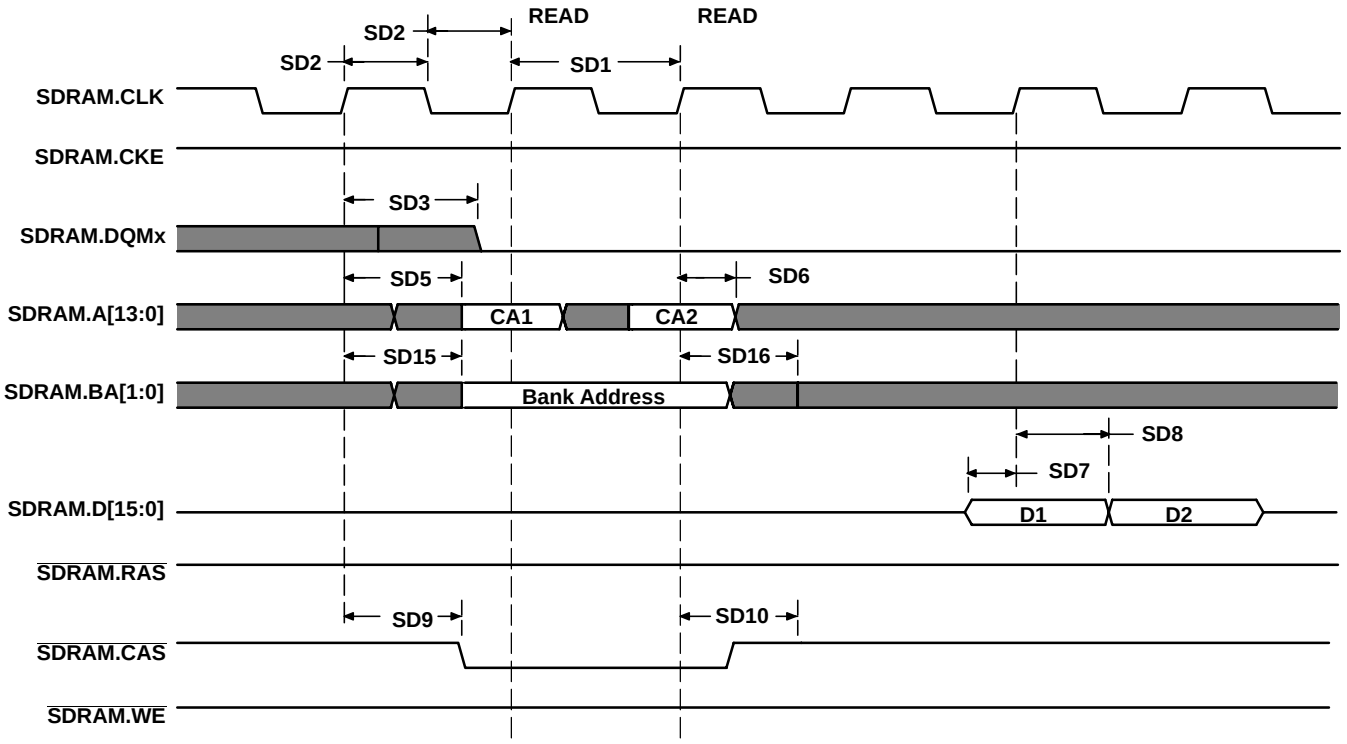


Figure 5−25. EMIFF/SDR Two SDRAM RD (Read) Commands (Active Row)

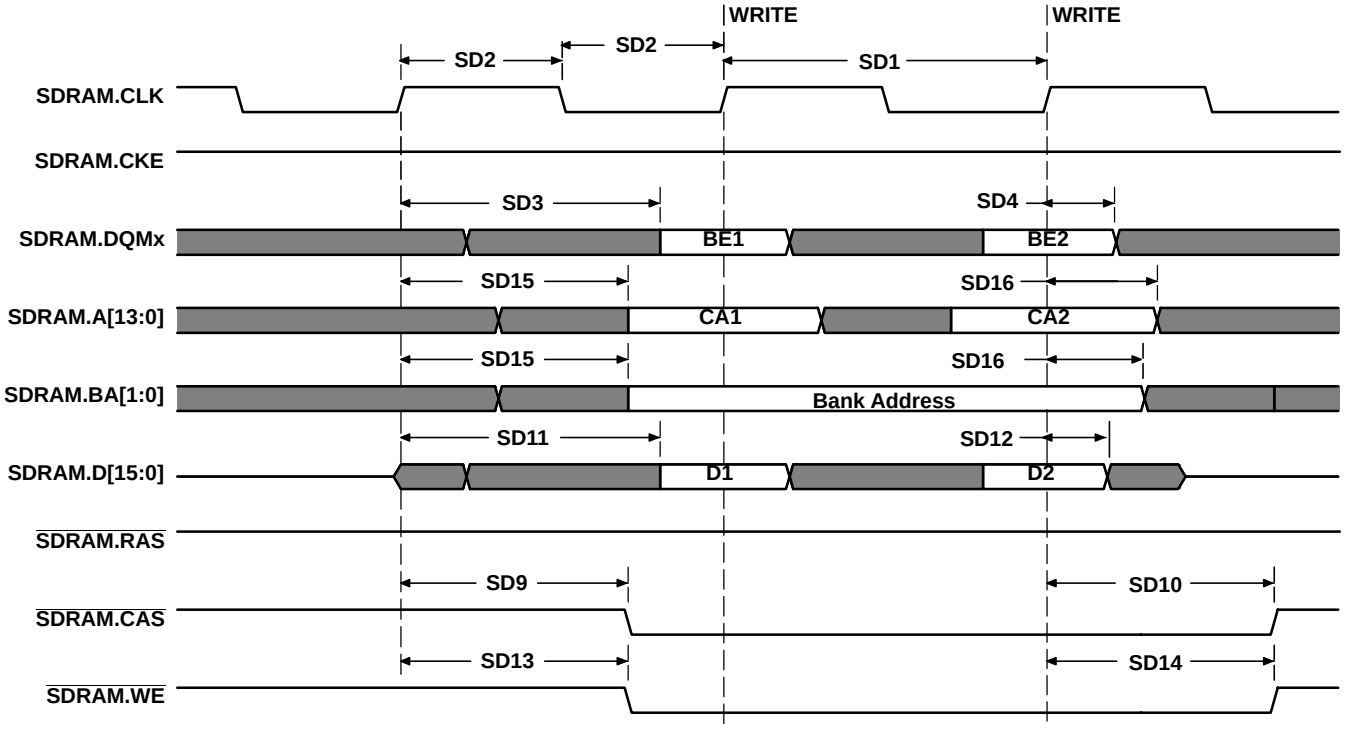


Figure 5−26. EMIFF/SDR Two SDRAM WRT (Write) Commands (Active Row)

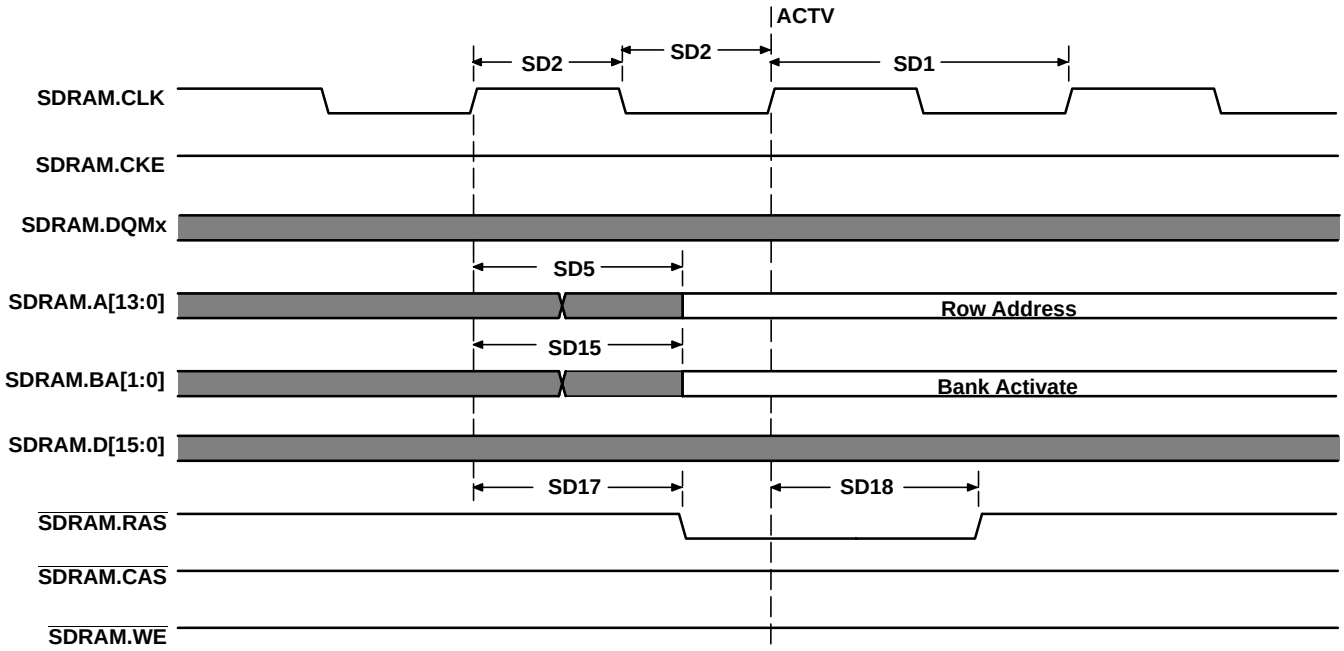


Figure 5−27. EMIFF/SDR SDRAM ACTV (Activate Row) Command

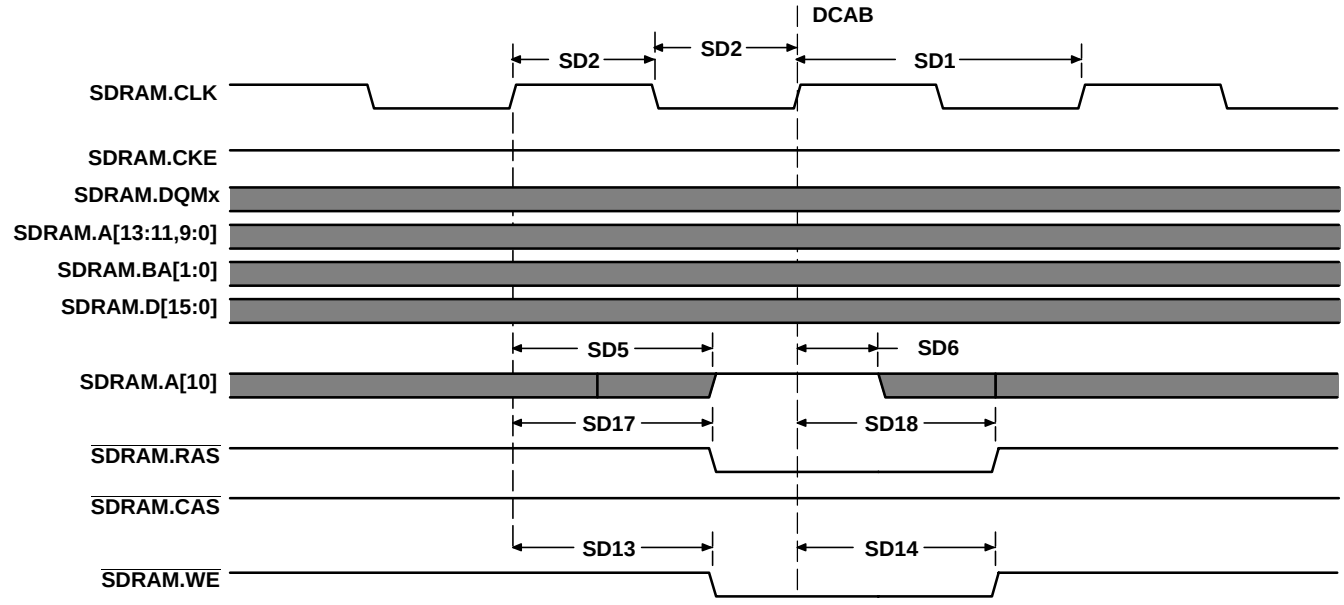


Figure 5−28. EMIFF/SDR SDRAM DCAB (Precharge/Deactivate Row) Command

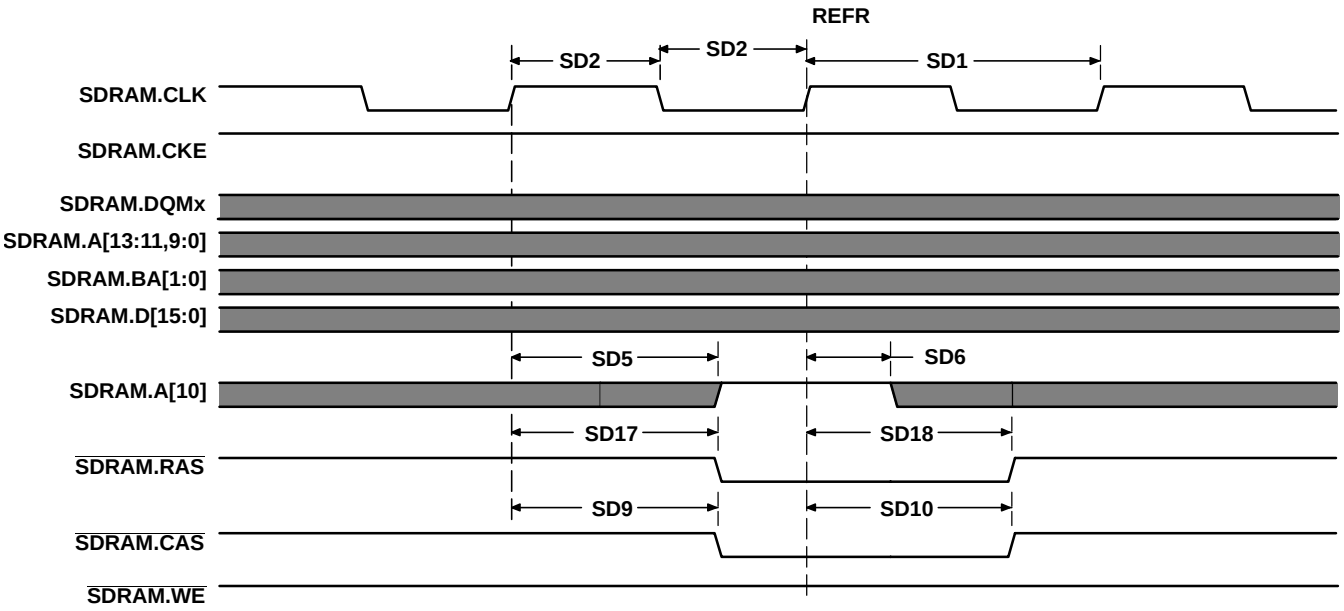


Figure 5−29. EMIFF/SDR SDRAM REFR (Refresh) Command

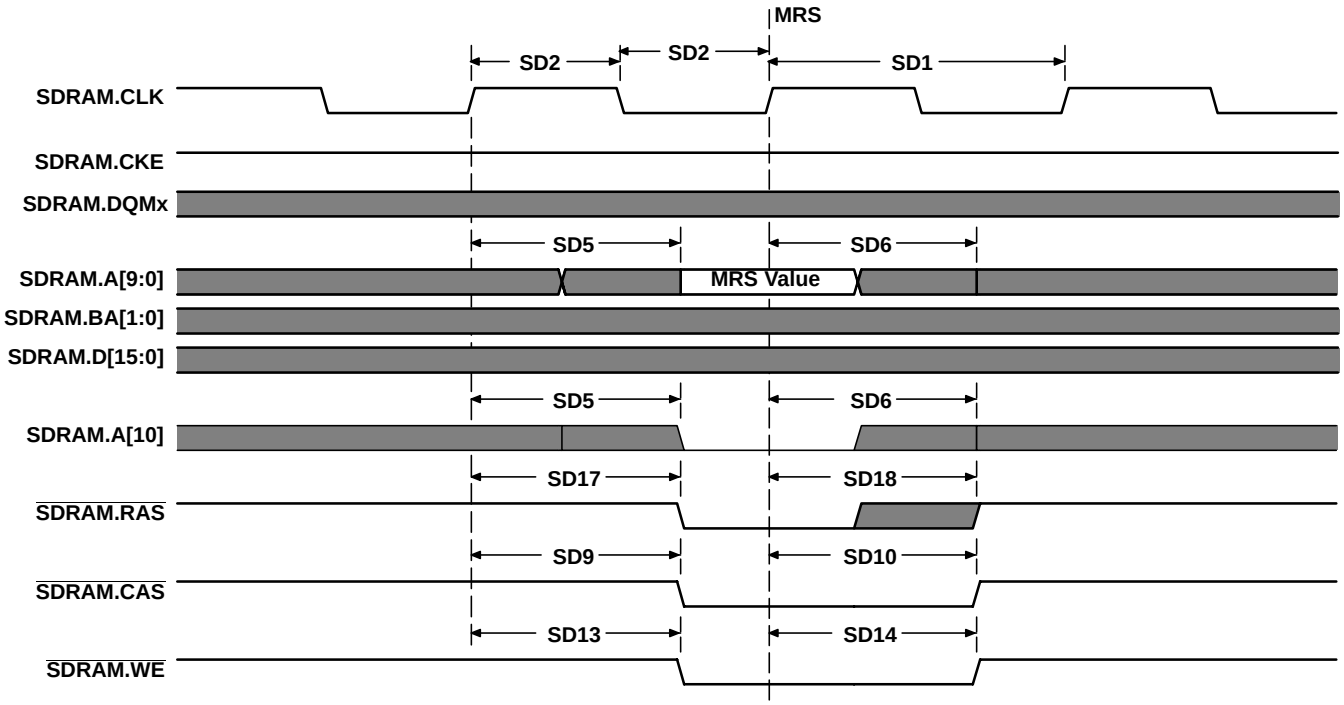


Figure 5−30. EMIFF/SDR SDRAM MRS (Mode Register Set) Command

5.9 EMIFF/Mobile DDR SDRAM Timing

Table 5−17 and Table 5−18 assume testing over recommended operating conditions (see Figure 5−31 through Figure 5−33).

Table 5−17. EMIFF/Mobile DDR SDRAM Timing Requirements

NO				DV_{DD4} = 1.8 V NOMINAL†		UNIT
				MIN	MAX	
DD17	$t_{su(DV-DQSL/H)}$	Setup time, SDRAM.D[15:0] input data valid to SDRAM.DQSL/H input high or low	DLL phase‡ = 72°	−1.32		ns
DD18	$t_{h(DQSL/H-DV)}$	Hold time, SDRAM.DQSL/H input high or low to SDRAM.D[15:0] input data valid before SDRAM.D[15:0] expires	DLL phase‡ = 72°	2.88		ns

† The control bit CONF_VOLTAGE_SDRAM_R of the register VOLTAGE_CTRL_0 must be set to 1 regardless of the DV_{DD4} voltage level.
‡ DLL phase value is defined in the EMIFF DLL read control register (DLL_PHASE bit). The delay time assume that WRITE_OFFSET bits value = 0 (in DLL_URD_CONTROL and DLL_LRD_CONTROL registers).

Table 5−18. EMIFF/Mobile DDR SDRAM Switching Characteristics§

NO	PARAMETER			DV_{DD4} = 1.8 V NOMINAL†		UNIT
				MIN	MAX	
DD1	$t_{c(CLK)}$	Cycle time, SDRAM.CLK/SDRAM.DDR-CLK		10.42		ns
DD3	$t_{osu(CLKH-CSL)}$	Output setup time, SDRAM.CLK high to $\overline{\text{SDRAM.CS}}$ low		2.00		ns
DD4	$t_{oh(CLKH-CSH)}$	Output hold time, SDRAM.CLK high to $\overline{\text{SDRAM.CS}}$ high		2.00		ns
DD5	$t_{osu(CLKH-RASL)}$	Output setup time, SDRAM.CLK high to $\overline{\text{SDRAM.RAS}}$ low		2.00	5.21	ns
DD5A	$t_{osu(CLKH-CASL)}$	Output setup time, SDRAM.CLK high to $\overline{\text{SDRAM.CAS}}$ low		2.00	5.40	ns
DD6	$t_{oh(CLKH-RASH)}$	Output hold time, SDRAM.CLK high to $\overline{\text{SDRAM.RAS}}$ high		2.00	6.88	ns
DD6A	$t_{oh(CLKH-CASH)}$	Output hold time, SDRAM.CLK high to $\overline{\text{SDRAM.CAS}}$ high		2.00	8.83	ns
DD7	$t_{osu(CLKH-BAV)}$	Output setup time, SDRAM.CLK high to SDRAM.BA[1:0] bank select valid		2.00		ns
DD8	$t_{oh(CLKH-BAIV)}$	Output hold time, SDRAM.CLK high to SDRAM.BA[1:0] bank select invalid		2.00		ns
DD9	$t_{osu(CLKH-AV)}$	Output setup time, SDRAM.CLK high to SDRAM.A[13:0] address valid		1.50		ns
DD10	$t_{oh(CLKH-AIV)}$	Output hold time, SDRAM.CLK high to SDRAM.A[13:0] address invalid		1.50		ns
DD11	$t_{osu(CLKH-WEL)}$	Output setup time, SDRAM.CLK high to $\overline{\text{SDRAM.WE}}$ low		2.00	5.37	ns
DD12	$t_{oh(CLKH-WEH)}$	Output hold time, SDRAM.CLK high to $\overline{\text{SDRAM.WE}}$ high		2.00	6.47	ns
DD13	$t_{osu(DQSL/H-DV)}$	Output setup time, SDRAM.DQSL/H (DQML/U) high/low to SDRAM.D[15:0] valid	DLL phase‡ = 72°	1.00		ns
DD14	$t_{oh(DQSL/H-DIV)}$	Output hold time, SDRAM.DQSL/H high or low (DQML/U) to SDRAM.D[15:0] invalid	DLL phase‡ = 72°	1.01		ns

† The control bit CONF_VOLTAGE_SDRAM_R of the register VOLTAGE_CTRL_0 must be set to 1 regardless of the DV_{DD4} voltage level.
‡ DLL phase value is defined in the EMIFF DLL read control register (DLL_PHASE bit). The delay time assume that WRITE_OFFSET bits value = 0 (in DLL_URD_CONTROL and DLL_LRD_CONTROL registers).
§ Delay time assumes that WRITE_OFFSET bits value = 0 (in DLL_URD_CONTROL and DLL_LRD_CONTROL registers).

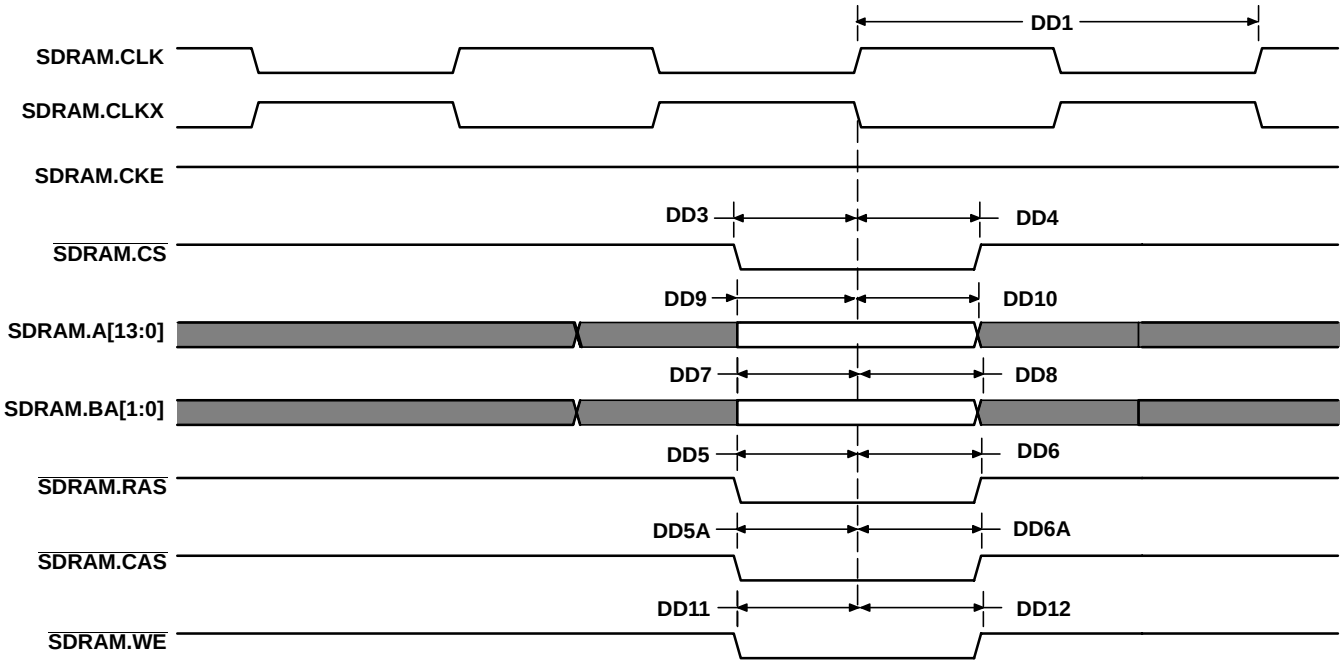
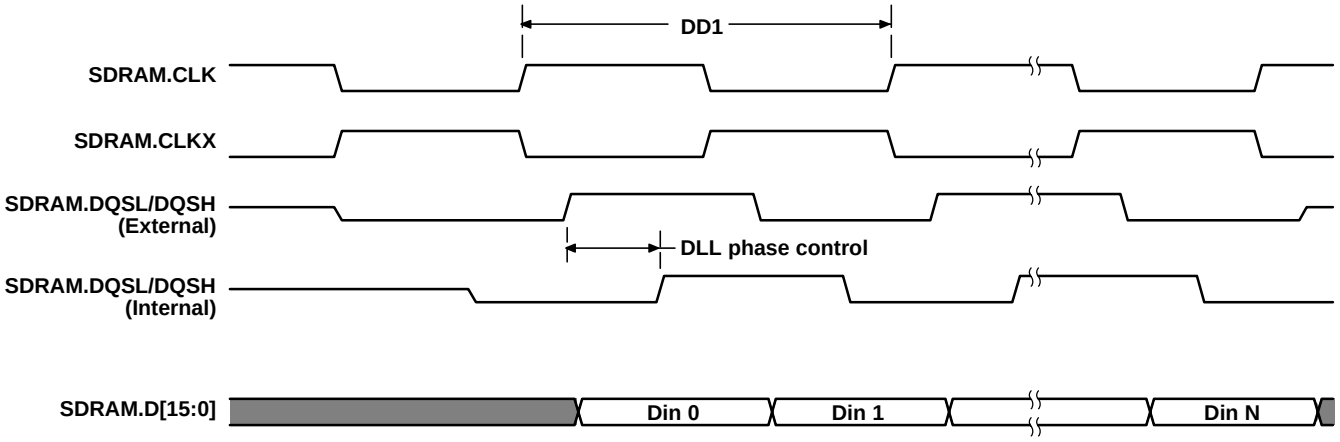
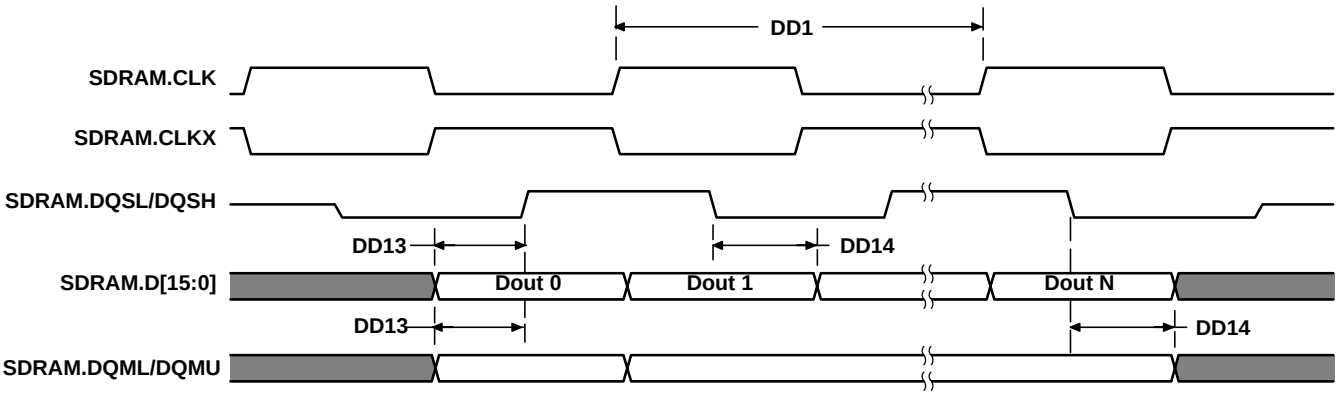


Figure 5−31. EMIFF/Mobile DDR SDRAM—Command and Address Output Timing Definition



NOTE: DQSL and DQSH internal delays are programmable in the EMIFF DLL_URD/LRD_CONTROL Register (72°)

Figure 5−32. EMIFF/Mobile DDR SDRAM—Memory Read Timing



NOTE: These timing includes the DLL phase effect on data, programmable in the EMIFF DLL write control register (72°), plus the device delay time (uncertainty).

Figure 5−33. EMIFF/Mobile DDR SDRAM—Memory Write Timing

5.10 Multichannel Buffered Serial Port (McBSP) Timing

5.10.1 McBSP Transmit and Receive Timing

Table 5−19 and Table 5−20 assume testing over recommended operating conditions (see Figure 5−34 and Figure 5−35). In Table 5−19 and Table 5−20, *ext* indicates that the device pin is configured as an input (slave) driven by an external device and int indicates that the pin is configured as an output (master).

Table 5−19. McBSP Timing Requirements†‡

NO.					MIN	MAX	UNIT
M11	$t_{c(CKRX)}$	Cycle time, CLKR/X		CLKR/X ext	2P		ns
M12	$t_{w(CKRX)}$	Pulse duration, CLKR/X high or CLKR/X low		CLKR/X ext	0.45P		ns
M13	t_r	Rise time, CLKR/X, MCBSP2.FSR/X	McBSP1	CLKR/X ext		18	ns
			McBSP2	CLKR/X ext MCBSP2.FSR/X ext		18	
			McBSP3	CLKR/X ext		9	
M14	t_f	Fall time, CLKR/X, MCBSP2.FSR/X	McBSP1	CLKR/X ext		18	ns
			McBSP2	CLKR/X ext MCBSP2.FSR/X ext		18	
			McBSP3	CLKR/X ext		9	
M15	$t_{su(FRH-CKRL)}$	Setup time, external receiver frame sync (FSR/X) high before CLKR/X low	McBSP1 (FSX)	CLKX int§	34		ns
				CLKX ext§	1		
			McBSP2 (FSR)	CLKR int	25		
				CLKR ext	0		
			McBSP3 (FSX)	CLKX int§	33		
				CLKX ext§	1		
M16	$t_{h(CKRL-FRH)}$	Hold time, external receiver frame sync (FSR/X) high after CLKR/X low	McBSP1 (FSX)	CLKX int§	−1.5		ns
				CLKX ext§	7.5		
			McBSP2 (FSR)	CLKR int	−1		
				CLKR ext	8.5		
			McBSP3 (FSX)	CLKX int§	−1.25		
				CLKX ext§	9		
M17	$t_{su(DRV-CKRL)}$	Setup time, DR valid before CLKR/X low	McBSP1	CLKX int§	33		ns
				CLKX ext§	0		
			McBSP2	CLKR int	27.75		
				CLKR ext	1		
			McBSP3	CLKX int§	32		
				CLKX ext§	1		
M18	$t_{h(CKRL-DRV)}$	Hold time, DR valid after CLKR/X low	McBSP1	CLKX int§	−1.5		ns
				CLKX ext§	8		
			McBSP2	CLKR int	−1		
				CLKR ext	8.25		
			McBSP3	CLKX int§	−1.25		
				CLKX ext§	9.75		

† Polarity bits CLKRP = CLKXP = FSRP = FSXP = 0. If the polarity of any of the signals is inverted, the timing references of that signal are also inverted.

‡ P = 1/(DSPPER_CK or DSPXOR_CK) for McBSP 1 and 3, or 1/(ARMPER_CK clock frequency) in nanoseconds (ns) for McBSP 2.

§ For McBSP1 and McBSP3, the receiver clock and frame sync inputs are driven by FSX and CLKX via internal loopback connections enabled via software configuration.

Table 5−19. McBSP Timing Requirements†‡ (Continued)

NO.					MIN	MAX	UNIT
M19	$t_{su(FXH-CKXL)}$	Setup time, external transmit frame sync (FSX) high before CLKX low	McBSP1	CLKX int§	33.5		ns
				CLKX ext§	1		
			McBSP2	CLKX int	25.25		
				CLKX ext	0		
			McBSP3	CLKX int§	33.25		
				CLKX ext§	1		
M20	$t_{h(CKXL-FXH)}$	Hold time, external transmit frame sync (FSX) high after CLKX low	McBSP1	CLKX int§	−1.5		ns
				CLKX ext§	7.5		
			McBSP2	CLKR int	−1		
				CLKR ext	7.75		
			McBSP3	CLKX int§	−1.25		
				CLKX ext§	9.25		

† Polarity bits CLKRP = CLKXP = FSRP = FSXP = 0. If the polarity of any of the signals is inverted, the timing references of that signal are also inverted.

‡ P = 1/(DSPPER_CK or DSPXOR_CK) for McBSP 1 and 3, or 1/(ARMPER_CK clock frequency) in nanoseconds (ns) for McBSP 2.

§ For McBSP1 and McBSP3, the receiver clock and frame sync inputs are driven by FSX and CLKX via internal loopback connections enabled via software configuration.

Table 5−20. McBSP Switching Characteristics†‡§

NO.	PARAMETER				MIN	MAX	UNIT
M0	$t_{d(CKSH-CKRXH)}$	Delay time, CLKS high to CLKR/X high for internal CLKR/X generated from CLKS input	McBSP1	CLKR/X int	3.5	31.5	ns
M1	$t_{d(CKRX)}$	Cycle time, CLKR/X		CLKR/X int	2P		
M2	$t_{d(CKRXH)}$	Pulse duration, CLKR/X high		CLKR/X int	0.90D	1.10D	ns
M3	$t_{d(CKRXL)}$	Pulse duration, CLKR/X low		CLKR/X int	0.90C	1.10C	ns
M4	$t_{d(CKRH-FRV)}$	Delay time, CLKR high to internal FSR valid	McBSP2	CLKR int	−7.5	5.5	ns
				CLKR ext	3	24	
M5	$t_{d(CKXH-FXV)}$	Delay time, CLKX high to internal FSX valid	McBSP1	CLKX int	−8	7.5	ns
				CLKX ext	3.5	32	
			McBSP2	CLKX int	−6.5	7	
				CLKX ext	3	24	
			McBSP3	CLKX int	−10.5	8.5	
				CLKX ext	3.25	37.75	

† Polarity bits CLKRP = CLKXP = FSRP = FSXP = 0. If the polarity of any of the signals is inverted, the timing references of that signal are also inverted.

‡ P = 1/(DSPPER_CK or DSPXOR_CK) for McBSP 1 and 3, or 1/(ARMPER_CK clock frequency) in nanoseconds (ns) for McBSP2.

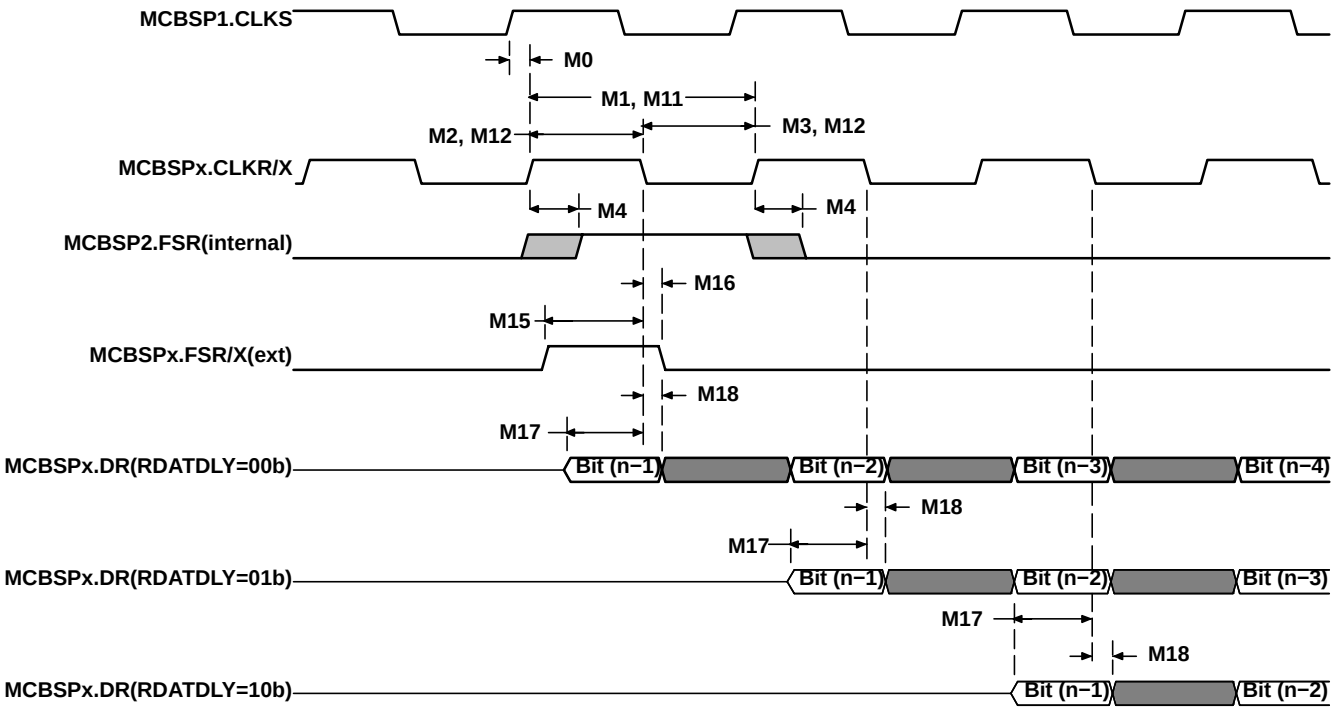
§ T = CLKRX period = (1 + CLKGDV) * P
C = CLKRX low pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2) * P when CLKGDV is even
D = CLKRX high pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2 + 1) * P when CLKGDV is even

¶ Only DXENA = 0 is supported for all OMAP5912 McBSPs.

Table 5−20. McBSP Switching Characteristics[†‡§] (Continued)

NO.	PARAMETER				MIN	MAX	UNIT
M7	$t_{d(CKXH-DXV)}$	Delay time, CLKX high to DX valid. This applies to all bits except the first bit transmitted when in data delay 0 (XDATDLY = 00b) mode.	McBSP1	CLKX int	−8	10.25	ns
				CLKX ext	3.5	34.75	
			McBSP2	CLKX int	−6.75	9.75	
				CLKX ext	2.75	26.75	
			McBSP3	CLKX int	−9.75	9.75	
				CLKX ext	3	39	
M9	$t_{d(FXH-DXV)}$	Delay time, FSX high to DX valid[¶] Only applies to first bit transmitted when in data delay 0 (XDATDLY = 00b) mode.	McBSP1	FSX int		29.5	ns
				FSX ext		35.75	
			McBSP2	FSX int		19.75	
				FSX ext		24.25	
			McBSP3	FSX int		15	
				FSX ext		18	

[†] Polarity bits CLKRP = CLKXP = FSRP = FSXP = 0. If the polarity of any of the signals is inverted, the timing references of that signal are also inverted.
[‡] P = 1/(DSPPER_CK or DSPXOR_CK) for McBSP 1 and 3, or 1/(ARMPER_CK clock frequency) in nanoseconds (ns) for McBSP2.
[§] T = CLKRX period = (1 + CLKGDV) * P
C = CLKRX low pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2) * P when CLKGDV is even
D = CLKRX high pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2 + 1) * P when CLKGDV is even
[¶] Only DXENA = 0 is supported for all OMAP5912 McBSPs.



NOTE: For McBSP1 and McBSP3, the receiver clock and frame sync inputs are driven by FSX and CLKX via internal loopback connections enabled via software configuration.

Figure 5−34. McBSP Receive Timing

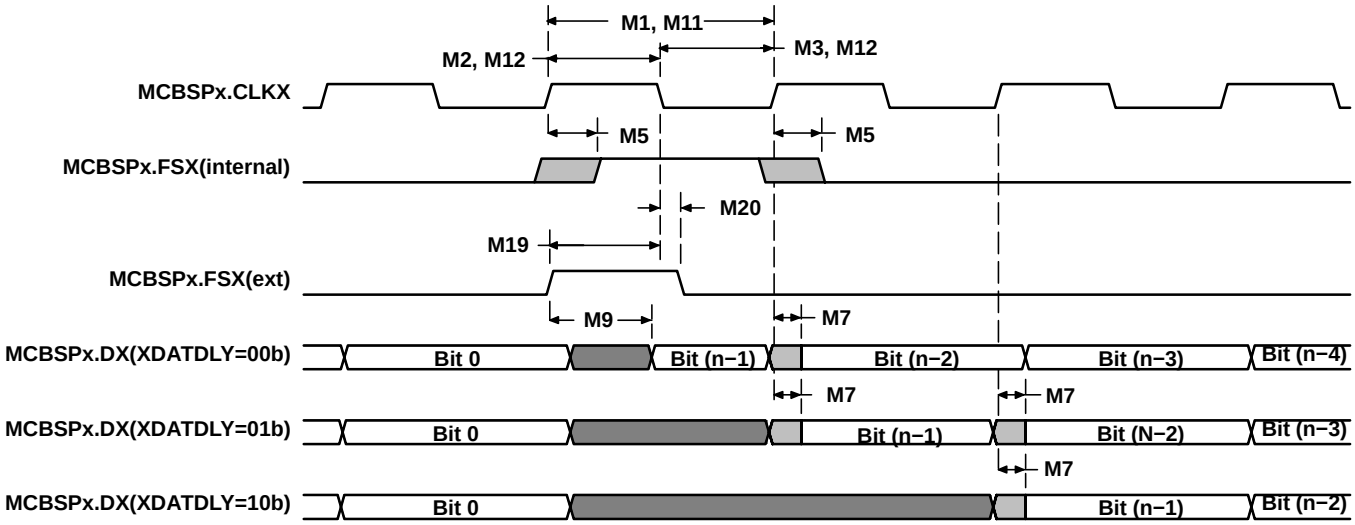


Figure 5−35. McBSP Transmit Timing

5.10.2 McBSP as SPI Master or Slave Timing

Table 5−21 to Table 5−28 assume testing over recommended operating conditions (see Figure 5−36 to Figure 5−39).

Table 5−21. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 10b, CLKXP = 0)†‡

NO.				MASTER		SLAVE		UNIT
				MIN	MAX	MIN	MAX	
M30	$t_{su(DRV-CKXL)}$	Setup time, MCBSPx.DR valid before MCBSPx.CLKX low		33.25		0		ns
M31	$t_{h(CKXL-DRV)}$	Hold time, MCBSPx.DR valid after MCBSPx.CLKX low		−1		6P + 9		ns
M32	$t_{su(BFXL-CKXH)}$	Setup time, MCBSPx.FSX low before MCBSPx.CLKX high	McBSP1			5		ns
			McBSP2			5		
			McBSP3			6		
M33	$t_{c(CKX)}$	Cycle time, MCBSPx.CLKX		2P		16P		ns

† P =1/(DSPPER_CK or DSPXOR_CK) for McBSP1 and McBSP3, or 1/(ARMPER_CK clock frequency) in nanoseconds (ns) for McBSP2.
‡ For all SPI slave modes, CLKG is programmed as 1/2 of the internal reference clock by setting CLKSM = CLKGDV = 1.

Table 5−22. McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 10b, CLKXP = 0)†‡

NO.	PARAMETER		MASTER		SLAVE		UNIT
			MIN	MAX	MIN	MAX	
M24	$t_{h(CKXL-FXL)}$	Hold time, MCBSPx.FSX low after MCBSPx.CLKX low§¶	C − 10.5	P + 8.25			ns
M25	$t_{d(FXL-CKXH)}$	Delay time, MCBSPx.FSX low to MCBSPx.CLKX high§#	2C − 10.5	P + 8.25			ns
M26	$t_{d(CKXH-DXV)}$	Delay time, MCBSPx.CLKX high to MCBSPx.DX valid	−9.75	10.25	2.75	5P + 34.5	ns

† P =1/(DSPPER_CK or DSPXOR_CK) for McBSP1 and McBSP3, or 1/(ARMPER_CK clock frequency) in nanoseconds (ns) for McBSP2.
‡ For all SPI slave modes, CLKG is programmed as 1/2 of the internal reference clock by setting CLKSM = CLKGDV = 1.
§ T = CLKX period = (1 + CLKGDV) * P
C = CLKX low pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2) * P when CLKGDV is even.
¶ FSRP = FSXP = 1. As a SPI master, MCBSPx.FSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on MCBSPx.FSX and MCBSPx.FSR is inverted before being used internally.
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP
CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP
# MCBSPx.FSX must be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (MCBSPx.CLKX).

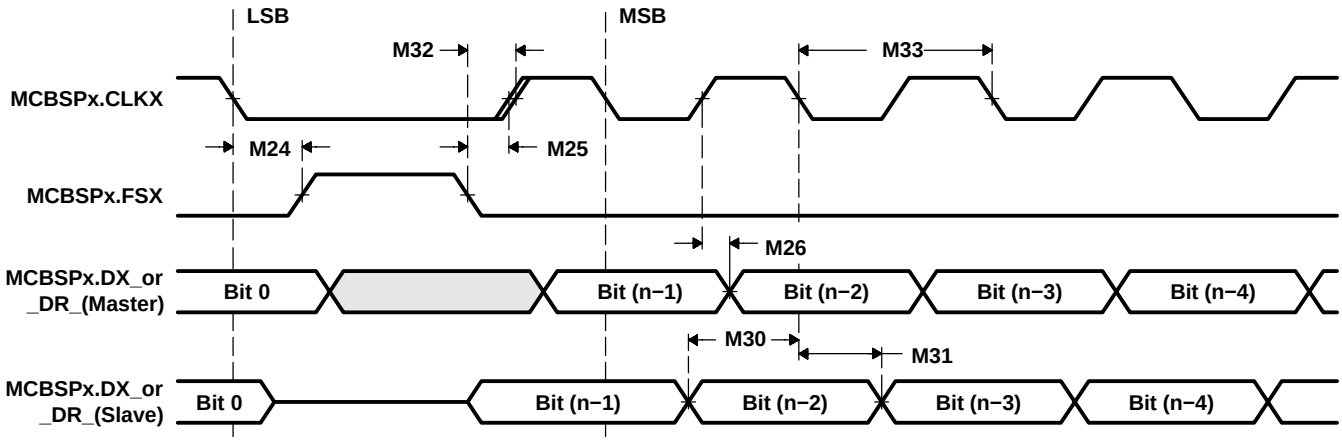


Figure 5−36. McBSP Timings as SPI Master or Slave: CLKSTP = 10b, CLKXP = 0

Table 5−23. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 11b, CLKXP = 0)†‡

NO.				MASTER		SLAVE		UNIT
				MIN	MAX	MIN	MAX	
M39	$t_{su(DRV-CKXH)}$	Setup time, MCBSPx.DR valid before MCBSPx.CLKX high		33.25		0		ns
M40	$t_{h(CKXH-DRV)}$	Hold time, MCBSPx.DR valid after MCBSPx.CLKX high		−1		6P + 9		ns
M41	$t_{su(FXL-CKXH)}$	Setup time, MCBSPx.FSX low before MCBSPx.CLKX high	McBSP1			5		ns
			McBSP2			5		
			McBSP3			6		
M42	$t_{c(CKX)}$	Cycle time, MCBSPx.CLKX		2P		16P		ns

† P =1/(DSPPER_CK or DSPXOR_CK) for McBSP1 and McBSP3, or 1/(ARMPER_CK clock frequency) in nanoseconds (ns) for McBSP2.
‡ For all SPI slave modes, CLKG is programmed as 1/2 of the internal reference clock by setting CLKSM = CLKGDV = 1.

Table 5−24. McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 11b, CLKXP = 0)†‡

NO.	PARAMETER		MASTER		SLAVE		UNIT
			MIN	MAX	MIN	MAX	
M34	$t_{h(CKXL-FXL)}$	Hold time, MCBSPx.FSX low after MCBSPx.CLKX low§¶	2C − 10.5	P + 8.25			ns
M35	$t_{d(FXL-CKXH)}$	Delay time, MCBSPx.FSX low to MCBSPx.CLKX high§#	C − 10.5	P + 8.25			ns
M36	$t_{d(CKXL-DXV)}$	Delay time, MCBSPx.CLKX low to MCBSPx.DX valid	−9.75	10.25	2.75	5P + 34.5	ns

† P =1/(DSPPER_CK or DSPXOR_CK) for McBSP1 and McBSP3, or 1/(ARMPER_CK clock frequency) in nanoseconds (ns) for McBSP2.
‡ For all SPI slave modes, CLKG is programmed as 1/2 of the internal reference clock by setting CLKSM = CLKGDV = 1.
§ T = CLKX period = (1 + CLKGDV) * P
C = CLKX low pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2) * P when CLKGDV is even.
¶ FSRP = FSXP = 1. As a SPI master, MCBSPx.FSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on MCBSPx.FSX and MCBSPx.FSR is inverted before being used internally.
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP
CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP
# MCBSPx.FSX must be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (MCBSPx.CLKX).

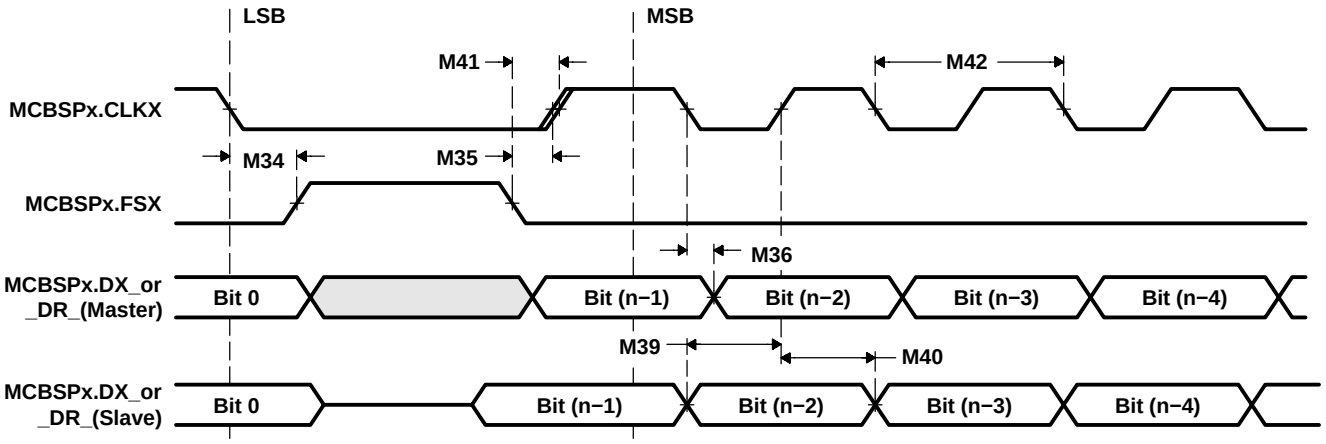


Figure 5−37. McBSP Timings as SPI Master or Slave: CLKSTP = 11b, CLKXP = 0

Table 5−25. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 10b, CLKXP = 1)†‡

NO.				MASTER		SLAVE		UNIT
				MIN	MAX	MIN	MAX	
M49	$t_{su(DRV-CKXH)}$	Setup time, MCBSPx.DR valid before MCBSPx.CLKX high		33.25		0		ns
M50	$t_{h(CKXH-DRV)}$	Hold time, MCBSPx.DR valid after MCBSPx.CLKX high		−1		6P + 9		ns
M51	$t_{su(FXL-CKXL)}$	Setup time, MCBSPx.FSX low before MCBSPx.CLKX low	McBSP1			5		ns
			McBSP2			5		
			McBSP3			6		
M52	$t_{c(CKX)}$	Cycle time, MCBSPx.CLKX		2P		16P		ns

† P =1/(DSPPER_CK or DSPXOR_CK) for McBSP1 and McBSP3, or 1/(ARMPER_CK clock frequency) in nanoseconds (ns) for McBSP2.
‡ For all SPI slave modes, CLKG is programmed as 1/2 of the internal reference clock by setting CLKSM = CLKGDV = 1.

Table 5−26. McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 10b, CLKXP = 1)†‡

NO.	PARAMETER		MASTER		SLAVE		UNIT
			MIN	MAX	MIN	MAX	
M43	$t_{h(CKXH-FXL)}$	Hold time, MCBSPx.FSX low after MCBSPx.CLKX high§¶	C − 10.5	P + 8.25			ns
M44	$t_{d(FXL-CKXL)}$	Delay time, MCBSPx.FSX low to MCBSPx.CLKX low§#	2C − 10.5	P + 8.25			ns
M45	$t_{d(CKXL-DXV)}$	Delay time, MCBSPx.CLKX low to MCBSPx.DX valid	−9.75	10.25	2.75	5P + 34.5	ns

† P =1/(DSPPER_CK or DSPXOR_CK) for McBSP1 and McBSP3, or 1/(ARMPER_CK clock frequency) in nanoseconds (ns) for McBSP2.
‡ For all SPI slave modes, CLKG is programmed as 1/2 of the internal reference clock by setting CLKSM = CLKGDV = 1.
§ T = CLKX period = (1 + CLKGDV) * P
C = CLKX low pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2) * P when CLKGDV is even.
¶ FSRP = FSXP = 1. As a SPI master, MCBSPx.FSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on MCBSPx.FSX and MCBSPx.FSR is inverted before being used internally.
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP
CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP
# MCBSPx.FSX must be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (MCBSPx.CLKX).

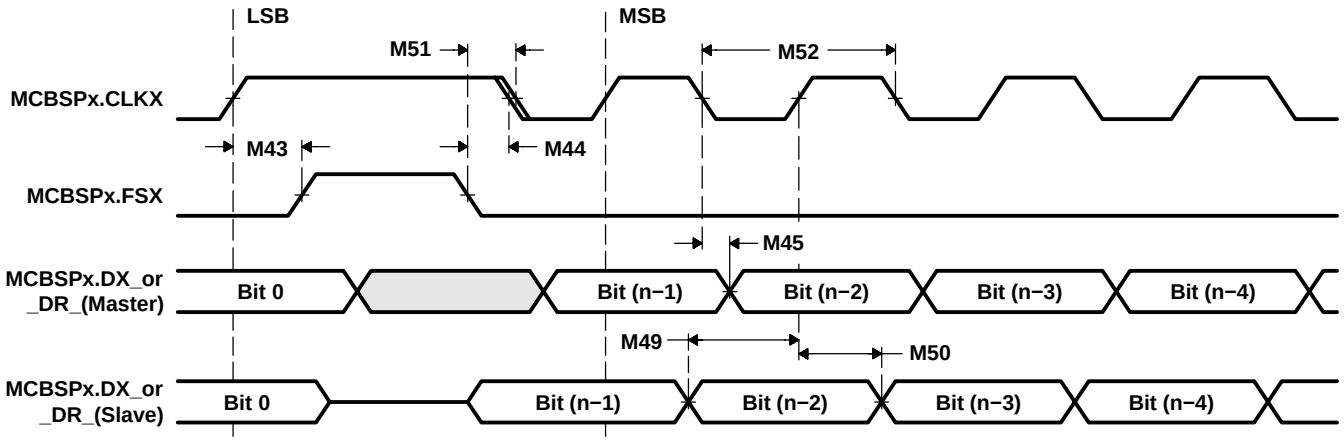


Figure 5−38. McBSP Timings as SPI Master or Slave: CLKSTP = 10b, CLKXP = 1

Table 5−27. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 11b, CLKXP = 1)†‡

NO.				MASTER		SLAVE		UNIT
				MIN	MAX	MIN	MAX	
M58	$t_{su(DRV-CKXL)}$	Setup time, MCBSPx.DR valid before MCBSPx.CLKX low		33.25		0		ns
M59	$t_{h(CKXL-DRV)}$	Hold time, MCBSPx.DR valid after MCBSPx.CLKX low		−1		6P + 9		ns
M60	$t_{su(FXL-CKXL)}$	Setup time, MCBSPx.FSX low before MCBSPx.CLKX low	McBSP1			5		ns
			McBSP2			5		
			McBSP3			6		
M61	$t_{c(CKX)}$	Cycle time, MCBSPx.CLKX		2P		16P		ns

† P =1/(DSPPER_CK or DSPXOR_CK) for McBSP1 and McBSP3, or 1/(ARMPER_CK clock frequency) in nanoseconds (ns) for McBSP2.
‡ For all SPI slave modes, CLKG is programmed as 1/2 of the internal reference clock by setting CLKSM = CLKGDV = 1.

Table 5−28. McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 11b, CLKXP = 1)†‡

NO.	PARAMETER		MASTER		SLAVE		UNIT
			MIN	MAX	MIN	MAX	
M53	$t_{h(CKXH-FXL)}$	Hold time, MCBSPx.FSX low after MCBSPx.CLKX high§¶	2C − 10.5	P + 8.25			ns
M54	$t_{d(FXL-CKXL)}$	Delay time, MCBSPx.FSX low to MCBSPx.CLKX low§#	C − 10.5	P + 8.25			ns
M55	$t_{d(CKXH-DXV)}$	Delay time, MCBSPx.CLKX high to MCBSPx.DX valid	−9.75	10.25	2.75	5P + 34.5	ns

† P =1/(DSPPER_CK or DSPXOR_CK) for McBSP1 and McBSP3, or 1/(ARMPER_CK clock frequency) in nanoseconds (ns) for McBSP2.
‡ For all SPI slave modes, CLKG is programmed as 1/2 of the internal reference clock by setting CLKSM = CLKGDV = 1.
§ T = CLKX period = (1 + CLKGDV) * P
C = CLKX low pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2) * P when CLKGDV is even.
¶ FSRP = FSXP = 1. As a SPI master, MCBSPx.FSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on MCBSPx.FSX and MCBSPx.FSR is inverted before being used internally.
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP
CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP
# MCBSPx.FSX must be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (MCBSPx.CLKX).

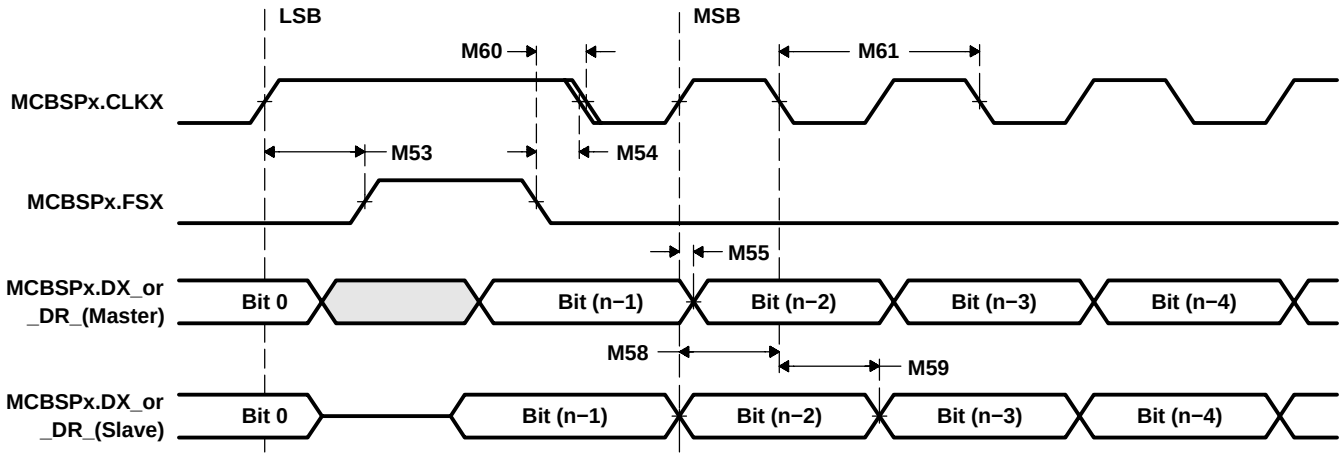


Figure 5−39. McBSP Timings as SPI Master or Slave: CLKSTP = 11b, CLKXP = 1

5.11 Multichannel Serial Interface (MCSI) Timing

Table 5−29 and Table 5−30 assume testing over recommended operating conditions (see Figure 5−40 and Figure 5−41).

Table 5−29. MCSI Timing Requirements

NO.				MIN	MAX	UNIT
MC5	$1/[t_{c(CLK)}]$	Operating frequency, MCSIx.CLK†	Slave		B‡	MHz
MC6	$t_{w(CLK)}$	Pulse duration, MCSIx.CLK high or low	Slave	0.45P§	0.55P§	ns
MC7	$t_{r(CLK)}$	Rise time, MCSIx.CLK	Slave		18	ns
MC8	$t_{f(CLK)}$	Fall time, MCSIx.CLK	Slave		18	ns
MC9	$t_{su(FSH-CLKL)}$	Setup time, external MCSIx.SYNC high before MCSIx.CLK low¶	Slave	12		ns
MC10	$t_{h(CLKL-FSH)}$	Hold time, external MCSIx.SYNC high after MCSIx.CLK low¶	Slave	5		ns
MC11	$t_{su(DIV-CLKL)}$	Setup time, MCSIx.DIN valid before MCSIx.CLK low	Master	18		ns
			Slave	12		
MC12	$t_{h(CLKL-DIV)}$	Hold time, MCSIx.DIN valid after MCSIx.CLK low	Master	0		ns
			Slave	5.8		

† The clock polarity can be configured by software (bit CLOCK_POLARITY of MAIN_PARAMETERS_REG register).
‡ B = System clock frequency of OMAP5912 (12, 13, or 19.2 MHz)
§ P = MCSIx.CLK period $t_{c(CLK)}$ in nanoseconds
¶ The frame synchro polarity can be configured by software (bit FRAME_POLARITY of MAIN_PARAMETERS_REG register).

Table 5−30. MCSI Switching Characteristics

NO.	PARAMETER			MIN	MAX	UNIT
MC1	$1/[t_{c(CLK)}]$	Operating frequency, MCSIx.CLK†	Master		0.5B‡	MHz
MC2	$t_{w(CLK)}$	Pulse duration, MCSIx.CLK high or low	Master	0.45P§	0.55P§	ns
MC3	$t_{d(CLKH-FS)}$	Delay time, MCSIx.CLK high to MCSIx.SYNC transition¶	Master	−2.5	4	ns
MC4	$t_{d(CLKH-DOV)}$	Delay time, MCSIx.CLK high to MCSIx.DOUT valid	Master	−2.5	3	ns
			Slave	2.5	24	

† The clock polarity can be configured by software (bit CLOCK_POLARITY of MAIN_PARAMETERS_REG register).
‡ B = System clock frequency of OMAP5912 (12, 13, or 19.2 MHz)
§ P = MCSIx.CLK period $t_{c(CLK)}$ in nanoseconds
¶ The frame synchro polarity can be configured by software (bit FRAME_POLARITY of MAIN_PARAMETERS_REG register).

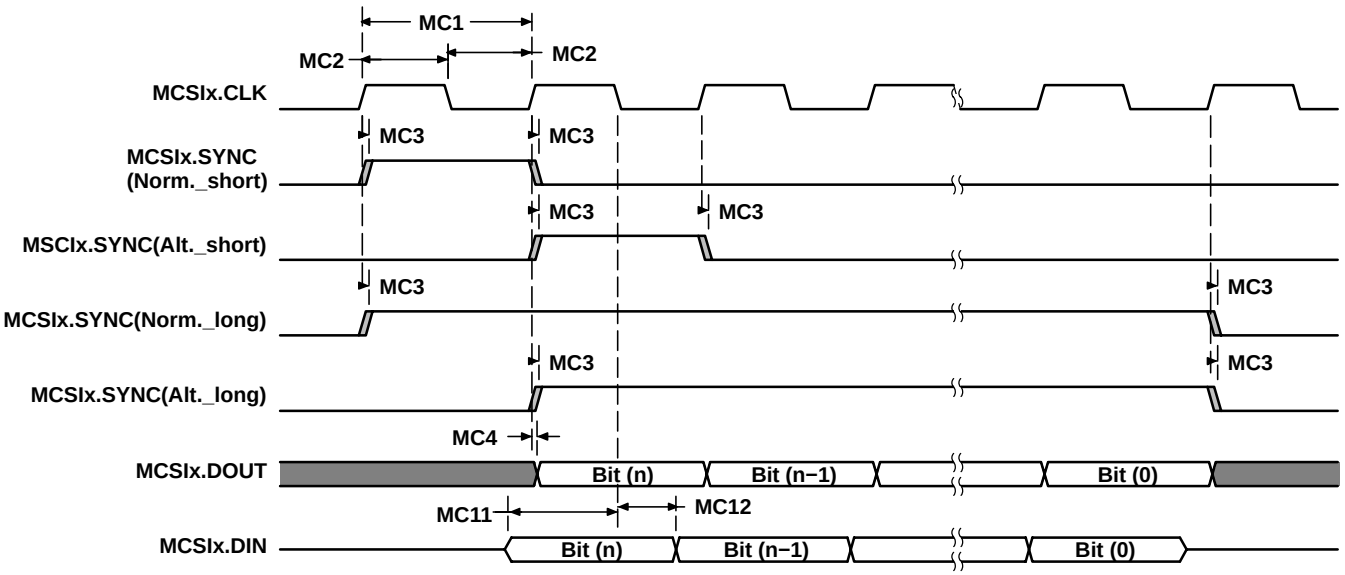


Figure 5−40. MCSI Master Mode Timing

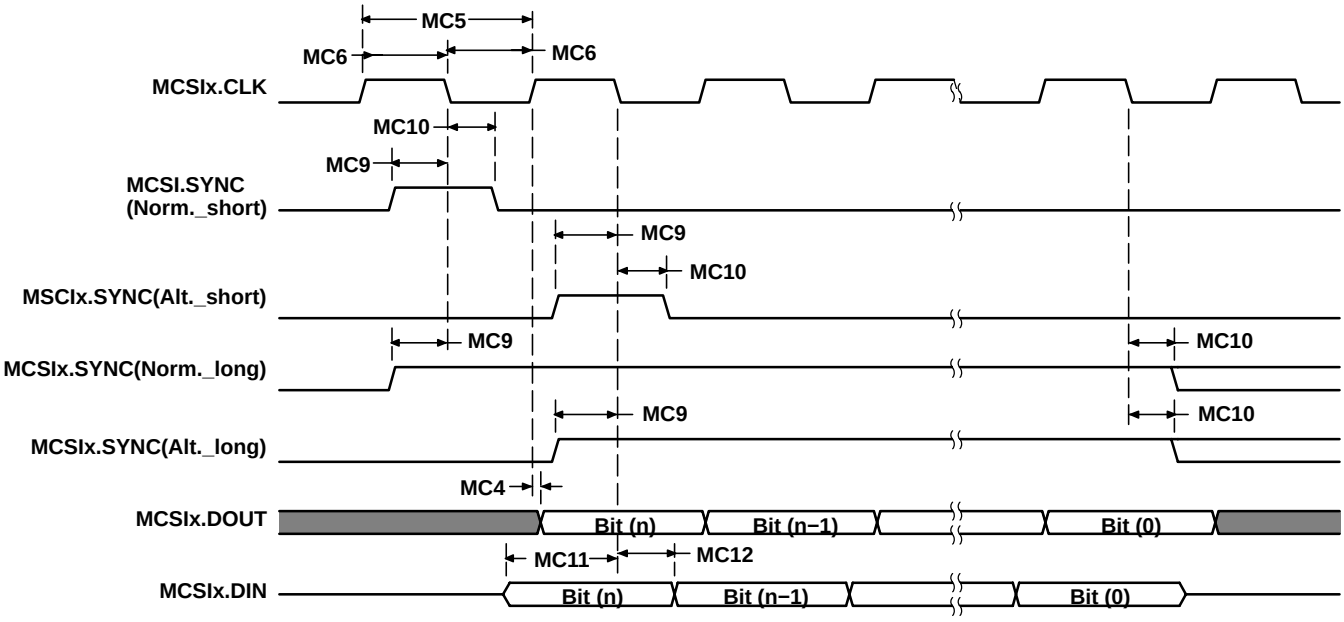


Figure 5−41. MCSI Slave Mode Timing

5.12 Serial Port Interface (SPI) Timing

Table 5−31 and Table 5−32 assume testing over recommended operating conditions (see Figure 5−42)

Table 5−31. SPI Interface Timing Requirements

NO.				MIN	MAX	UNIT
SPI1	$1/t_{c(SCLK)}$	Operating frequency, SPIF.SCK	Slave mode		B†	MHz
SPI2	$t_{w(SCLKH)}$	Pulse duration, SPIF.SCK high or low	Slave mode	0.45P‡	0.55P‡	ns
SPI5	$t_{su(DV-CLKH)}$	Setup time, SPIF.DIN valid before SPIF.SCK active edge§	Master mode	15		ns
			Slave mode	1		
SPI6	$t_{h(CLKH-DV)}$	Hold time, SPIF.DIN valid after SPIF.SCK active edge§	Master mode	−3		ns
			Slave mode	1		

† B = System clock frequency of OMAP5912 (12, 13, or 19.2 MHz)
‡ P = SPIF.SCK period $t_{c(CLK)}$ in nanoseconds
§ The polarity of SPIF.SCK and the active clock edge (rising or falling) on which DOUT is driven and DIN data is latched is all software configurable. These timing applies to all configurations regardless of SPIF.SCK polarity and which clock edges are used to drive output data and capture input data.

Table 5−32. SPI Interface Switching Characteristics

NO.	PARAMETER			MIN	MAX	UNIT
SPI1	$1/t_{c(SCLK)}$	Operating frequency, SPIF.SCK	Master mode		B†	MHz
SPI2	$t_{w(SCLKH)}$	Pulse duration, SPIF.SCK high or low	Master mode	0.45P‡	0.55P‡	ns
SPI3	$t_{d(CS-SCLK)}$	Delay time, $\overline{\text{SPIF.CSx}}$ active to SPIF.SCK active	Master mode	P‡	P + 5‡	ns
SPI4	$t_{d(SCLK-DOUT)}$	Delay time, SPIF.SCK active edge to SPIF.DOUT transition	Master mode	1	6	ns
			Slave mode	5	17	

† B = System clock frequency of OMAP5912 (12, 13, or 19.2 MHz)
‡ P = SPIF.SCK period $t_{c(CLK)}$ in nanoseconds

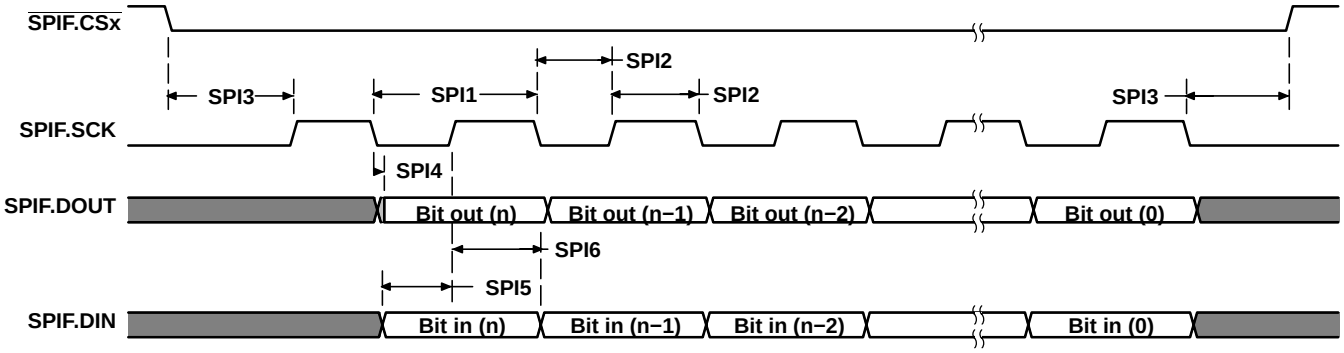


Figure 5−42. SPI Interface—Transmit and Receive in Master or Slave Timing

5.13 Parallel Camera Interface Timing

Table 5−33 assumes testing over recommended operating conditions (see Figure 5−43).

Table 5−33. Camera Interface Timing Requirements

NO.			MIN	MAX	UNIT
C1	$1/[t_{c(LCLK)}]$	Operating frequency, CAM.LCLK		80	MHz
C3	$t_{w(LCLK)}$	Pulse duration, CAM.LCLK high or low	0.45P1†	0.55P1†	ns
C5	$t_{r(LCLK)}$	Rise time, CAM.LCLK‡		0.25P1†	ns
C6	$t_{f(LCLK)}$	Fall time, CAM.LCLK‡		0.25P1†	ns
C9	$t_{su(DV-LCLKH)}$	Setup time, CAM.D[7:0] data valid before CAM.LCLK high	1§		ns
C10	$t_{h(LCLKH-DV)}$	Hold time, CAM.D[7:0] data valid after CAM.LCLK high	6§		ns
C11	$t_{su(CAM.VS/HS-LCLKH)}$	Setup time, CAM.VS/CAM.HS active before CAM.LCLK high	1§		ns
C12	$t_{h(LCLKH-CAM.VS/HS)}$	Hold time, CAM.VS/CAM.HS active after CAM.LCLK high	6§		ns

† P1 = Period of CAM.LCLK in nanoseconds (ns).

‡ In this table, the timing values of parameters C5 and C6 (CAM.LCLK) are given by considering the CMOS thresholds: $0.3DV_{DD}$ to $0.7DV_{DD}$. By considering t_r and t_f time from 10% to 90% of DV_{DD}, t_r and t_f = 0.45P1 for parameters C5 and C6.

§ The polarity of CAM.LCLK is selectable via the POLCLK bit in the CTRLCLOCK register. Although data is latched on rising CAM.LCLK in the timing diagrams, these timing parameters also apply to falling CAM.LCLK when POLCLK = 1.

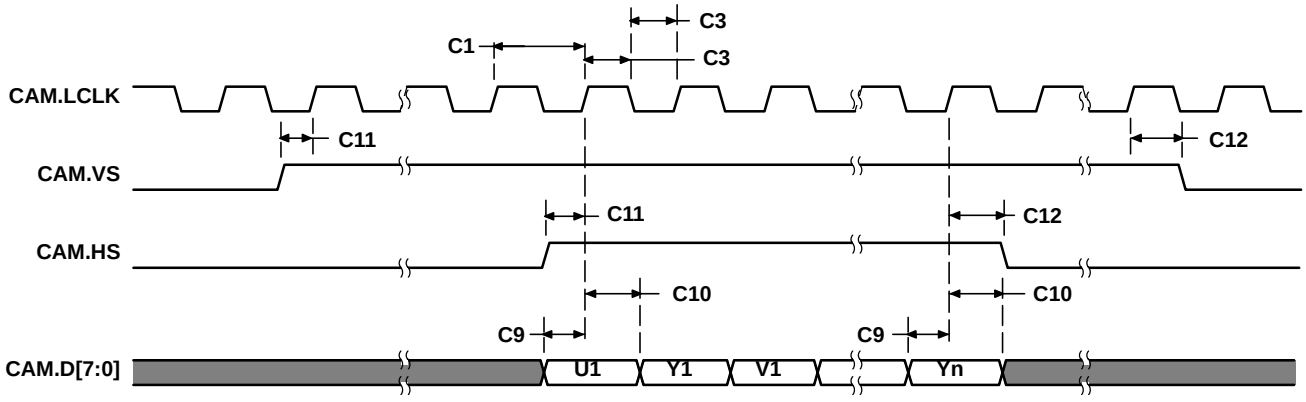


Figure 5−43. Camera Interface Timing

5.14 LCD Controller and LCDCONV Interfaces Timing

Table 5−34 assumes testing over recommended operating conditions (see Figure 5−44 and Figure 5−45).

Table 5−34. LCD Controller and LCDCONV Switching Characteristics†

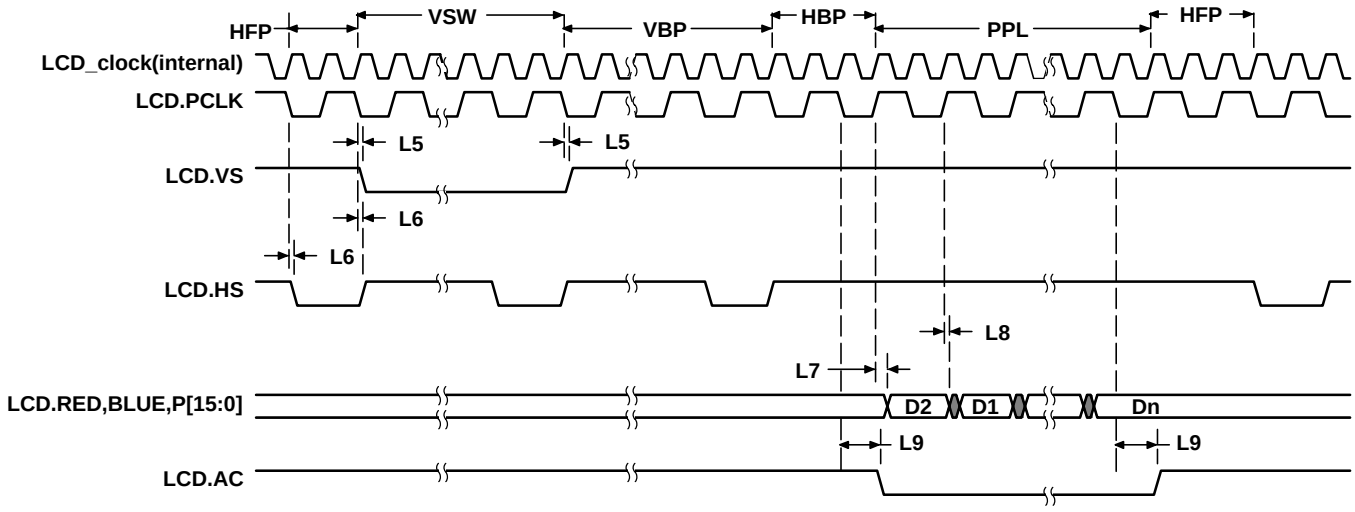
NO.	PARAMETER			MIN	MAX	UNIT
L1	$1/[t_{c(PCLK)}]$	Operating frequency, LCD.PCLK			20	MHz
L2	$t_{w(PCLK)}$	Pulse duration, LCD.PCLK high or low		0.4P‡§	0.6P‡§	ns
L3	$t_{r(PCLK)}$	Rise time, LCD.PCLK			15	ns
L4	$t_{f(PCLK)}$	Fall time, LCD.PCLK			15	ns
L5	$t_{d(CLK-VS)}$	Delay time, LCD.PCLK to LCD.VS transition		−1	1.5	ns
L6	$t_{d(CLK-HS)}$	Delay time, LCD.PCLK to LCD.HS transition		−1	1.5	ns
L7	$t_{d(CLK-PV)}$	Delay time, LCD.PCLK to pixel data valid (LCD.P[15:0])	LCD 16-bit mode (LCDCONV bypassed)		2	ns
			LCD 18-bit mode through LCDCONV (LCD.RED0 and LCD.BLUE0)		7	
L8	$t_{d(CLK-PIV)}$	Delay time, LCD.PCLK to pixel data invalid (LCD.P[15:0])	LCD 16-bit mode (LCDCONV bypassed)	−1		ns
			LCD 18-bit mode through LCDCONV (LCD.RED0 and LCD.BLUE0)	−3.5		
L9	$t_{d(CLK-AC)}$	Delay time, LCD.PCLK to LCD.AC transition		B − 2¶	B + 1¶	ns

† Although timing diagrams illustrate the logical function of the TFT mode, static timing applies to all supported modes of operation. Likewise, LCD.HS, LCD.VS, and LCD.AC are shown as active-low, but each can optionally be configured as active-high.

‡ P = Period of the LCD pixel clock

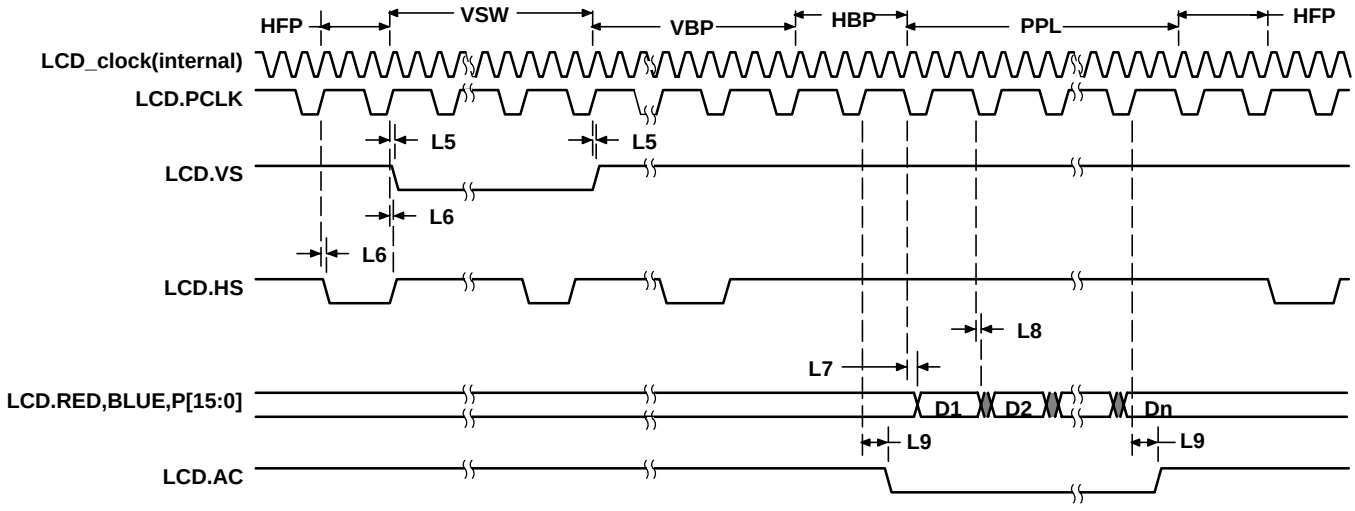
§ The pixel clock is created in a divider that may also be programmed to divide by odd numbers. In such case, the duty cycle at the output of the divider is influenced by the division ratio.

¶ B = Period of internal undivided pixel clock



NOTES: A. Different combinations of LCD signals behaviors can be attained by programming the LCD_TIMING_2 register. This figure corresponds to bits combination: PHSVSRF = 0, IEO = 1, IPC = 0, IHS = 1, IVS = 1, and PCD = 2.
B. Delays for HSW (LCD.HS width), VSW (LCD.VS width), VBP (vertical back porch), HFP (horizontal front porch), HBP (horizontal back porch), and PPL (pixels per line) are programmable in number of LCD.PCLK cycles via the LCD configuration registers.
C. Pins LCD.RED0 and LCD.BLUE0 have the same behavior than LCD.P[15:0] signals. They are only available in 18-bit LCD mode (through LCDCONV interface).

Figure 5−44. TFT Mode (LCD.HS/LCD.VS on Falling and LCD.Px on Rising LCD.PCLK—PCD = 2)



NOTES: A. Different combinations of LCD signals behavior are available by programming the LCD_TIMING_2 register. This figure corresponds to bits combination: PHSVSRF = 1, IEO = 1, IPC = 1, IHS = 1, IVS = 1, and PCD = 3.
B. Delays for HSW (LCD.HS width), VSW (LCD.VS width), VBP (vertical back porch), HFP (horizontal front porch), HBP (horizontal back porch), and PPL (pixels per line) are programmable in number of LCD.PCLK cycles via the LCD configuration registers.
C. Pins LCD.RED0 and LCD.BLUE0 have the same behavior as the LCD.P[15:0] signals. They are only available in 18-bit LCD mode (through LCDCONV interface).

Figure 5−45. TFT Mode (LCD.HS/LCD.VS on Rising and LCD.Px on Falling LCD.PCLK—PCD = 3)

5.15 Multimedia Card/Secure Digital (MMC/SD) Timing

Table 5−35 and Table 5−36 assume testing over recommended operating conditions (see Figure 5−46 through Figure 5−49).

Table 5−35. MMC/SD Timing Requirements

NO.			MIN	MAX	UNIT
M1	$t_{su(CMDV-CLKH)}$	Setup time, MMC.CMD valid before MMC.CLK high	10		ns
M2	$t_{h(CLKH-CMDV)}$	Hold time, MMC.CMD valid after MMC.CLK high	2		ns
M3	$t_{su(DATV-CLKH)}$	Setup time, MMC.DATx valid before MMC.CLK high	10		ns
M4	$t_{h(CLKH-DATV)}$	Hold time, MMC.DATx valid after MMC.CLK high	2		ns

Table 5−36. MMC/SD Switching Characteristics

NO.	PARAMETER			MIN	MAX	UNIT
M7	$1/[t_{c(CLK)}]$	Operating frequency, MMC.CLK	MMC Card		20	MHz
			SD Card		25	ns
M8	$t_{w(CLKH)}$	Pulse Duration, MMC.CLK low		0.45P†	0.55P†	ns
M9	$t_{w(CLKL)}$	Pulse Duration, MMC.CLK high		0.45P†	0.55P†	ns
M10	$t_{d(CLKL-CMD)}$	Delay time, MMC.CLK low to MMC.CMD transition		−1	5	ns
M11	$t_{d(CLKL-DAT)}$	Delay time, MMC.CLK low to MMC.DATx transition		−1	5	ns

† P is the period of the MMC.CLK clock.

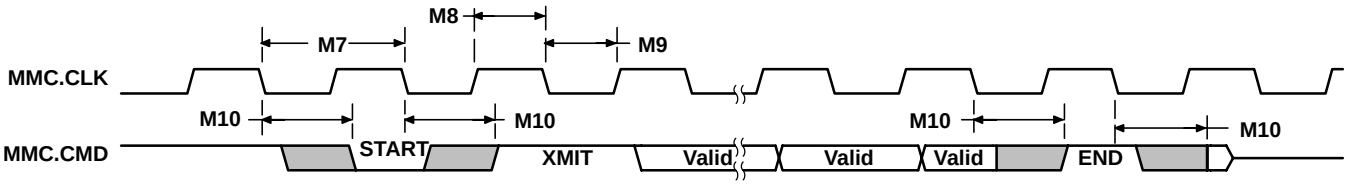


Figure 5−46. MMC/SD Host Command Timing

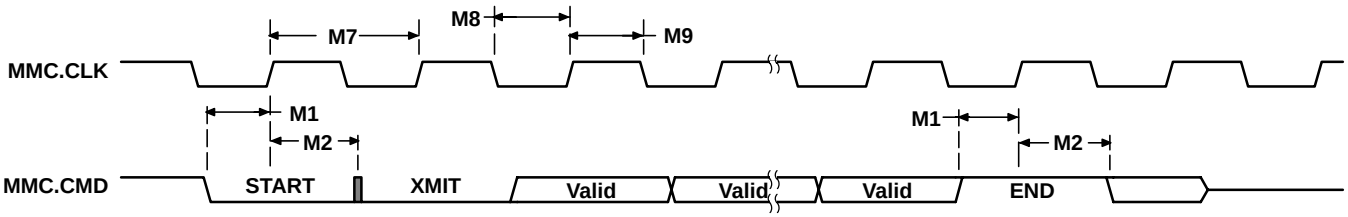


Figure 5−47. MMC/SD Card Response Timing

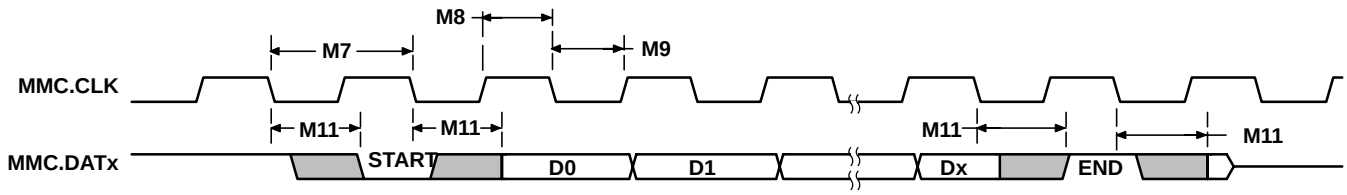


Figure 5−48. MMC/SD Host Write Timing

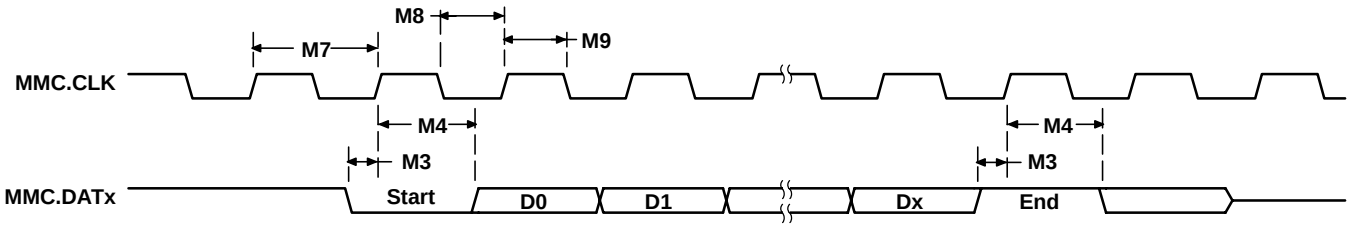


Figure 5−49. MMC/SD Host Read and Card CRC Status Timing

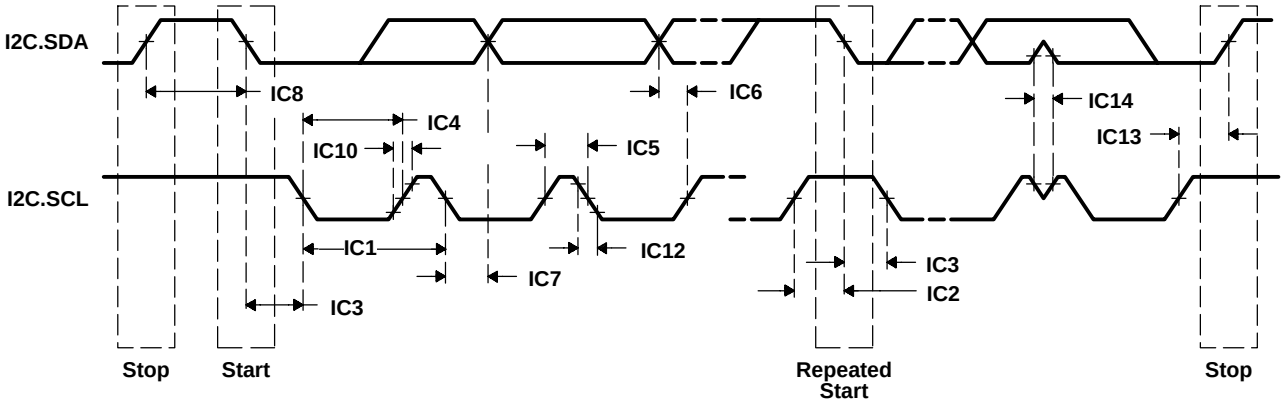
5.16 Inter-Integrated Circuit (I^2C) Timing

Table 5−37 assumes testing over recommended operating conditions (see Figure 5−50).

Table 5−37. I^2C Signals (I2C.SDA and I2C.SCL) Switching Characteristics

NO.	PARAMETER		STANDARD MODE		FAST MODE		UNIT
			MIN	MAX	MIN	MAX	
IC1	$t_{c(SCL)}$	Cycle time, I2C.SCL	10†		2.5		µs
IC2	$t_{su(SCLH-SDAL)}$	Setup time, I2C.SCL high before I2C.SDA low (for a repeated START condition)	4.7		0.6		µs
IC3	$t_{h(SCLL-SDAL)}$	Hold time, I2C.SCL low after I2C.SDA low (for a repeated START condition)	4		0.6		µs
IC4	$t_{w(SCLL)}$	Pulse duration, I2C.SCL low	4.7		1.3		µs
IC5	$t_{w(SCLH)}$	Pulse duration, I2C.SCL high	4		0.6		µs
IC6	$t_{su(SDA-SDLH)}$	Setup time, I2C.SDA valid before I2C.SCL high	250	‡	100		ns
IC7	$t_{h(SDA-SDLL)}$	Hold time, I2C.SDA valid after I2C.SCL low (for I^2C bus devices)	0		0	0.9	µs
IC8	$t_{w(SDAH)}$	Pulse duration, I2C.SDA high between STOP and START conditions	4.7		1.3		µs
IC9	$t_{r(SDA)}$	Rise time, I2C.SDA		1000§		300§	ns
IC10	$t_{r(SCL)}$	Rise time, I2C.SCL		1000§		300§	ns
IC11	$t_{f(SDA)}$	Fall time, I2C.SDA		300§		300§	ns
IC12	$t_{f(SCL)}$	Fall time, I2C.SCL		300§		300§	ns
IC13	$t_{su(SCLH-SDAH)}$	Setup time, I2C.SCL high before I2C.SDA high (for STOP condition)	4.0		0.6		µs
IC14	$t_{w(SP)}$	Pulse duration, spike (must be suppressed)			0	50	ns
IC15	C_b¶	Capacitive load for each bus line		400		400	pF

† In the master-only I^2C operating mode of OMAP5912, minimum cycle time for I2C.SCL is 12 µs.
‡ The maximum $t_{h(SCLL-SDAL)}$ has only to be met if the device does not stretch the low period ($t_{w(SCLL)}$) of the I2C.SCL signal.
§ Max of fall and rise times were measured while considering an internal pullup value of 520 Ω.
¶ C_b = The total capacitance of one bus line in pF.



NOTES: A. A device must internally provide a hold time of at least 300 ns for the I2C.SDA signal (referred to the V_{IHmin} of the I2C.SCL signal) to bridge the undefined region of the falling edge of I2C.SCL.
B. The maximum $t_{h(SCLL−SDAL)}$ has only to be met if the device does not stretch the LOW period ($t_{w(SCLL)}$) of the I2C.SCL signal.
C. A Fast-mode I^2C-bus device can be used in a Standard-mode I^2C-bus system, but the requirement $t_{su(SDA−SDLH)}$ • 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the I2C.SCL signal. If such a device does stretch the LOW period of the I2C.SCL signal, it must output the next data bit to the I2C.SDA line t_r max + $t_{su(SDA−SDLH)}$ = 1000 + 250 = 1250 ns (according to the standard-mode I^2C-bus specification) before the I2C.SCL line is released.
D. C_b = total capacitance of one bus line in pF. If mixed with fast-mode devices, faster fall times are allowed.

Figure 5−50. I^2C Timings

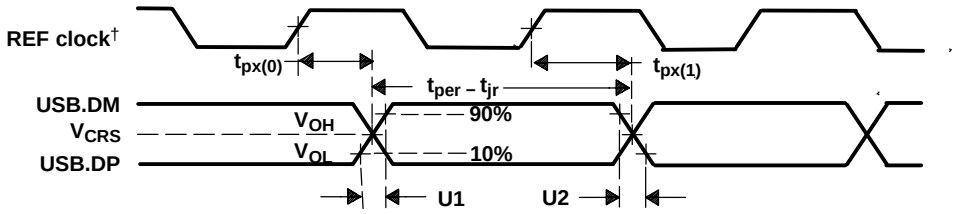
5.17 Universal Serial Bus (USB) Timing

All OMAP5912 USB interfaces are compliant with Universal Serial Bus Specifications, Revision 1.1. Table 5−38 assumes testing over recommended operating conditions (see Figure 5−51).

Table 5−38. USB Integrated Transceiver Interface Switching Characteristics

NO.	PARAMETER		LOW SPEED 1.5 Mbsp		FULL SPEED 12 Mbsp		UNIT
			MIN	MAX	MIN	MAX	
U1	t_r	Rise time, USB.DP and USB.DM signals†	75†	300†	4†	20†	ns
U2	t_f	Fall time, USB.DP and USB.DM signals†	75†	300†	4†	20†	ns
U3	t_{RFM}	Rise/Fall time matching‡	80‡	125‡	90‡	111.11‡	%
U4	V_{CRS}	Output signal cross-over voltage†	1.3†	2†	1.3†	2†	V
U5	t_{jr}	Differential propagation jitter§	−25§	25§	−2§	2§	ns
U6	f_{op}	Operating frequency¶		1.5		12	MHz

† Low speed: C_L = 200 pF. High speed: C_L = 50 pF.
‡ $t_{RFM} = (t_r/t_f) \times 100$
§ $t_{jr} = t_{px(1)} - t_{px(0)}$
¶ $f_{op} = 1/t_{per}$



† "REF clock" is not an actual device signal, but an ideal reference clock against which relative timings are specified. REF clock is assumed to be 12 MHz for full-speed mode or 1.5 MHz for low-speed mode.

Figure 5−51. USB Integrated Transceiver Interface Timings

5.18 MICROWIRE Interface Timing

Table 5−39 and Table 5−40 assume testing over recommended operating conditions (see Figure 5−52).

Table 5−39. MICROWIRE Timing Requirements

NO.			MIN	MAX	UNIT
W5	$t_{su(SDI-SCLK)}$	Setup time, UWIRE.SDI valid before UWIRE.SCLK active edge†	16		ns
W6	$t_{h(SCLK-SDI)}$	Hold time, UWIRE.SDI invalid after UWIRE.SCLK active edge†	1		ns

† Polarity of UWIRE.SCLK and the active clock edge (rising or falling) on which SDO data is driven and SDI data is latched is all software-configurable. These timings apply to all configurations regardless of UWIRE.SCLK polarity and which clock edges are used to drive output data and capture input data.

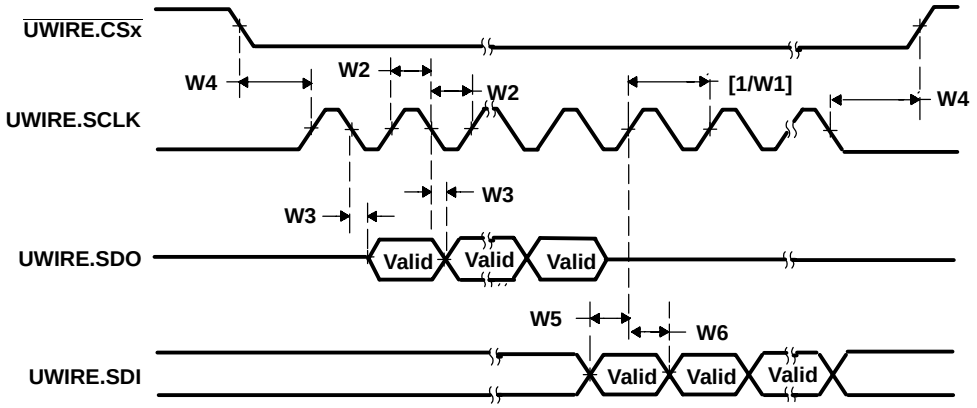
Table 5−40. MICROWIRE Switching Characteristics

NO.	PARAMETER		MIN	MAX	UNIT
W1	$f_{op(SCLK)}$	Operating frequency, UWIRE.SCLK		0.25B‡	MHz
W2	$t_{w(SCLK)}$	Pulse duration, UWIRE.SCLK high/low	0.45P§	0.55P§	ns
W3	$t_{d(SCLK-SDO)}$	Delay time, UWIRE.SCLK active edge to UWIRE.SDO transition†	−2	6	ns
W4	$t_{d(CS-SCLK)}$	Delay time, $\overline{\text{UWIRE.CSx}}$ active to UWIRE.SCLK active†	1.5P§		ns

† Polarity of UWIRE.SCLK and the active clock edge (rising or falling) on which SDO data is driven and SDI data is latched is all software-configurable. These timings apply to all configurations regardless of UWIRE.SCLK polarity and which clock edges are used to drive output data and capture input data.

‡ B = system clock of the OMAP5912 (12, 13, or 19.2 MHz).

§ P = UWIRE.SCLK cycle time in nanoseconds (ns).



NOTE: The polarities of $\overline{\text{UWIRE.CSx}}$ and UWIRE.SCLK and the active UWIRE.SCLK edges on which SDO is driven and SDI is sampled are all software-configurable.

Figure 5−52. MICROWIRE Timings

5.19 HDQ/1-Wire Interface Timing

Table 5−41 and Table 5−42 assume testing over recommended operating conditions (see Figure 5−53 through Figure 5−59).

Table 5−41. HDQ/1-Wire Timing Requirements†

NO.			SYSTEM CLOCK = 12 MHz		SYSTEM CLOCK = 13 MHz		SYSTEM CLOCK = 19.2 MHz		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
H1	$t_{(CYCH)}$	Read bit windows timing	253		234		158		µs
H2	$t_{(HW1)}$	Read bit−one time		68		63		42	µs
H3	$t_{(HW0)}$	Read bit−zero time	180		166		112		µs
W2	$t_{(PDH)}$	Presence pulse delay		68		63		42	µs
W3	$t_{(PDL)}$	Presence pulse low	68 – W2		63 − W2		42 – W2		µs
W6	$t_{(RDV)} + t_{(REL)}$	Read bit cycle time		102		94		63	µs

† HDQ timing is OMAP5912 default. 1-Wire timing is selectable through software.

Table 5−42. HDQ/1-Wire Switching Characteristics

NO.	PARAMETER		SYSTEM CLOCK = 12 MHz	SYSTEM CLOCK = 13 MHz	SYSTEM CLOCK = 19.2 MHz	UNIT
H5	$t_{(CYCD)}$	Write bit windows timing	232	214	145	µs
H6	$t_{(DW1)}$	Write bit-one time	1.3	1.2	0.81	µs
H7	$t_{(DW0)}$	Write bit-zero time	101	93	63	µs
H8	$t_{(B)}$	Break timing	192	178	120	µs
H9	$t_{(BR)}$	Break recovery time	63	58	39	µs
W1	$t_{(RSTL)}$	Reset time low	484	447	302	µs
W4	$t_{(RSTH)}$	Reset time high	484	447	302	µs
W5	$t_{(LOWR)}$	Read bit strobe time	13	12	8	µs
W7	$t_{(REC)}$	Recovery time	134	124	83	µs
W8	$t_{(LOW1)}$	Write bit-one time	1.3	1.2	0.8	µs
W9	$t_{(LOW0)}$	Write bit-zero time	101	93	63	µs
W10	$t_{(SLOT)}$	Write bit cycle time	102	94	63	µs

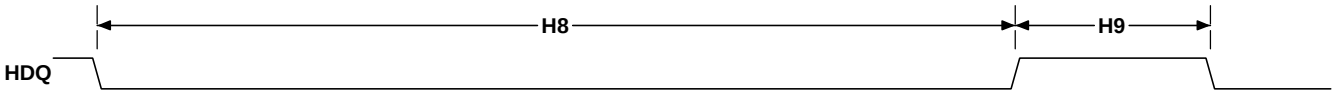


Figure 5−53. HDQ Break (Reset) Timing

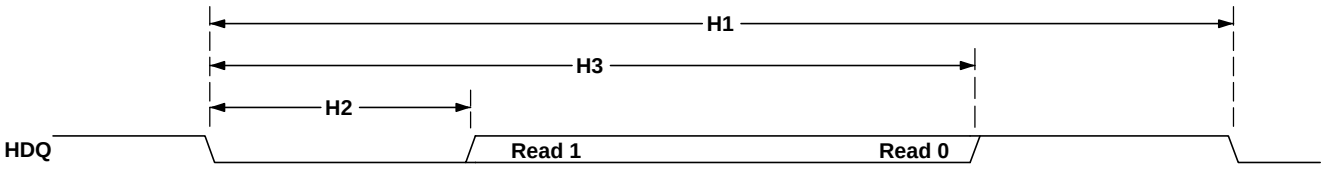


Figure 5−54. HDQ Interface Reading From HDQ Slave Device

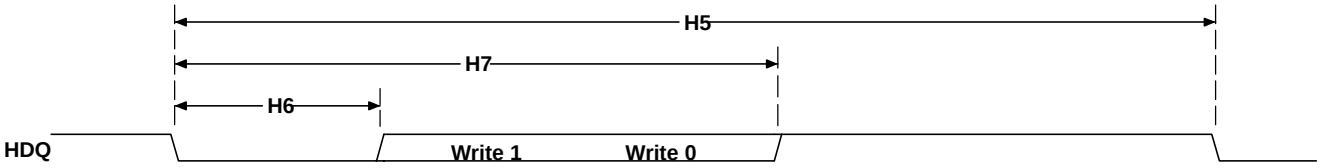


Figure 5−55. HDQ Interface Writing to HDQ Slave Device

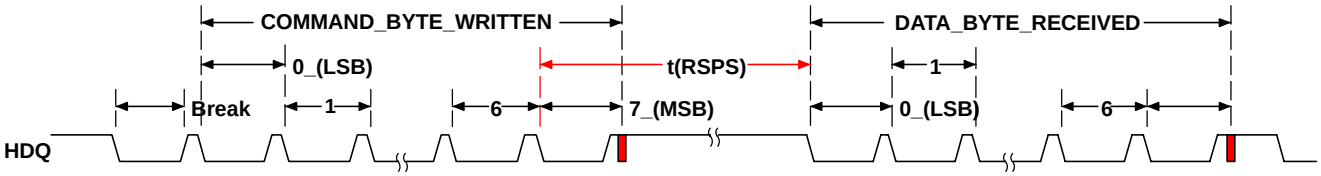


Figure 5−56. Typical Communication Between OMAP5912 HDQ and HDQ Slave

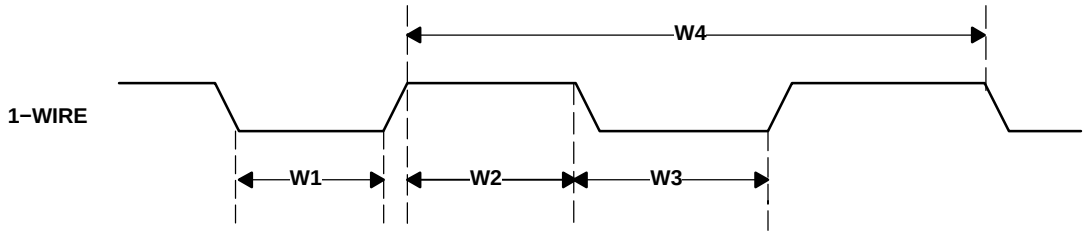


Figure 5−57. HDQ/1-Wire Break (Reset) Timing

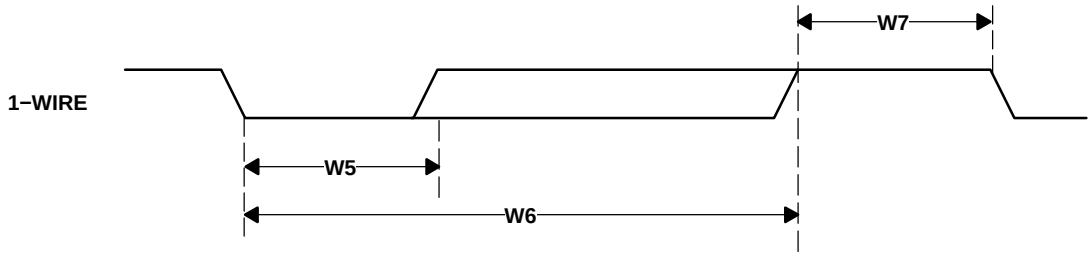


Figure 5−58. 1-Wire Interface Reading from 1-Wire Slave Device

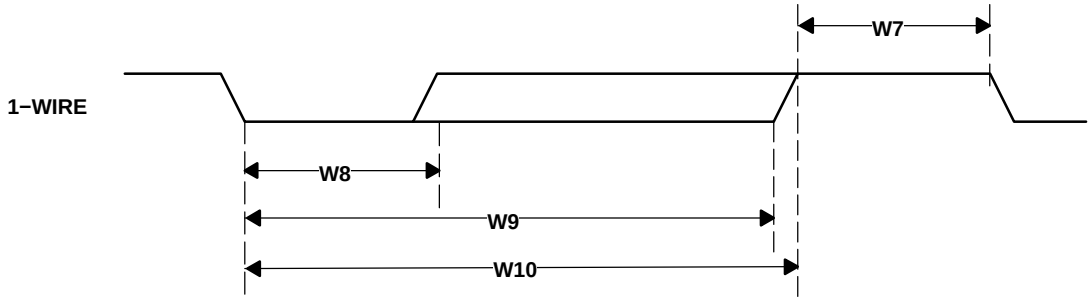


Figure 5−59. 1-Wire Interface Writing to 1-Wire Slave Device

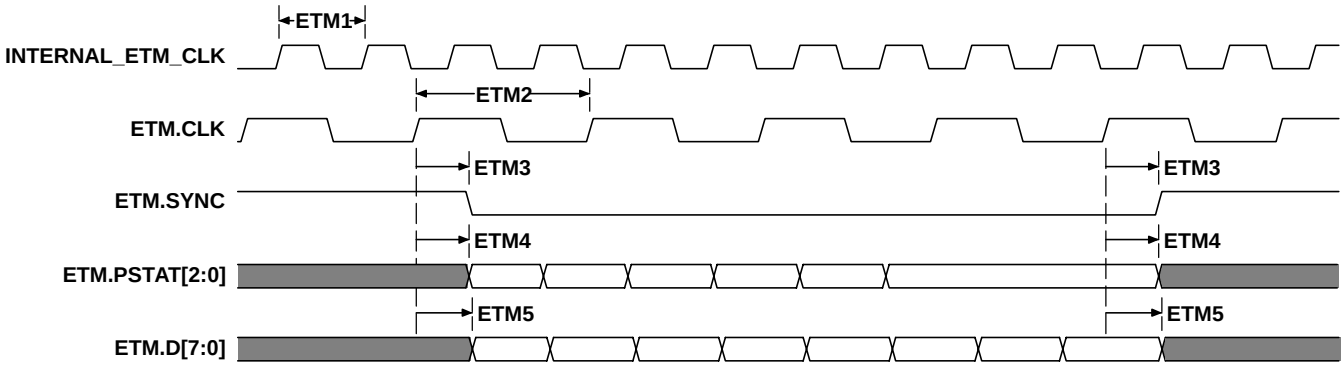
5.20 Embedded Trace Macrocell (ETM) Interface Timing

Table 5−43 assumes testing over recommended operating operations (see Figure 5−60 through Figure 5−61).

Table 5−43. ETM Interface Switching Characteristics

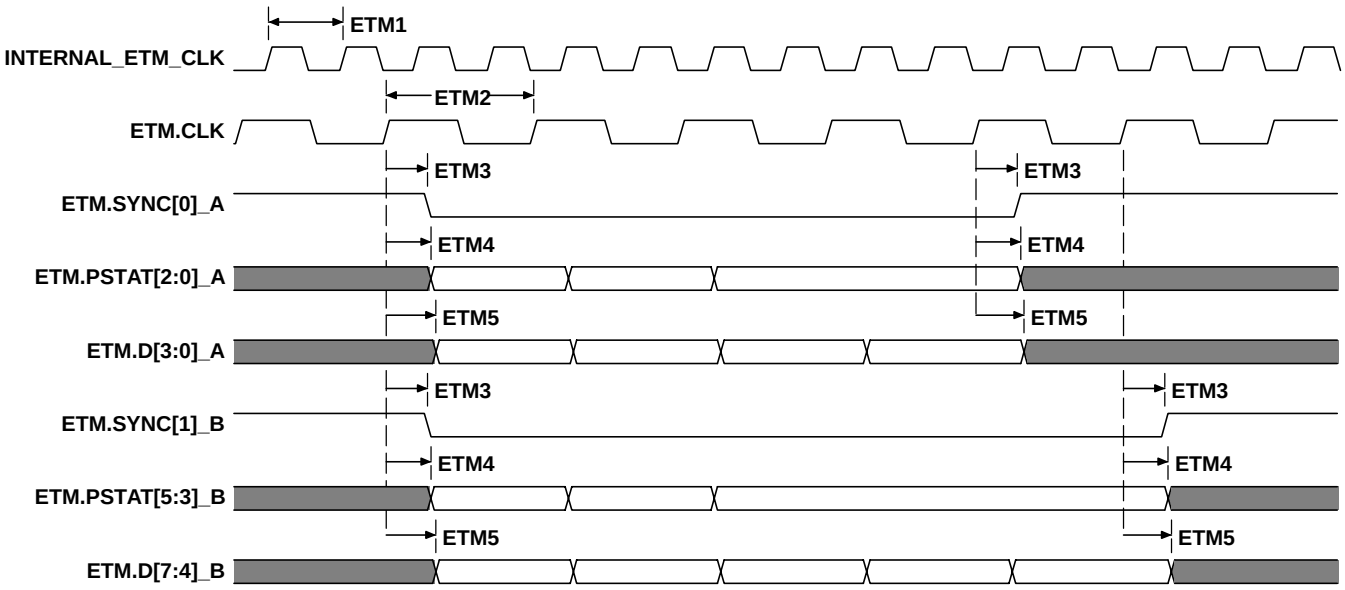
NO.	PARAMETER		MIN	MAX	UNIT
ETM1	$1/t_{c(CLKI)}$	Operating frequency, ETM internal clock		192	MHz
ETM2	$1/t_{c(CLK)}$	Operating frequency, ETM.CLK (external) clock		96	MHz
ETM3	$t_{d(CLKIH-SYNCV)}$	Delay time, ETM clock high to ETM.SYNCx valid		0.5P + 0.7†	ns
	$t_{d(CLKIH-SYNCIV)}$	Delay time, ETM clock high to ETM.SYNCx invalid	0.5P − 0.8†		ns
ETM4	$t_{d(CLKH-PSTATV)}$	Delay time, ETM clock high to ETM.PSTATx valid		0.5P + 0.82†	ns
	$t_{d(CLKH-PSTATIV)}$	Delay time, ETM clock high to ETM.PSTATx invalid	0.5P − 1.75†		ns
ETM5	$t_{d(CLKH-DV)}$	Delay time, ETM clock high to ETM.Dx valid		0.5P + 1.6†	ns
	$t_{d(CLKH-DIV)}$	Delay time, ETM clock high to ETM.Dx invalid	0.5P − 1.8†		ns

† P = Internal clock period



NOTE: Internal_ETM_CLK signal represents the internal ETM clock signal given as reference to express delay time.

Figure 5−60. Normal Mode—Half Rate Clock, Rising and Falling Clock Edge



NOTE: Internal_ETM_CLK signal represents the internal ETM clock signal given as reference to express delay time.

Figure 5−61. Demultiplexed Mode of Full Rate Clock—Rising Clock Edge

6 Glossary

ACRONYM	DEFINITION
3DES	triple data encryption security
AAC	Advanced Audio Coding (standard) (ISO/IEC 13818-7)
AC97	Interface Standard for Codecs
ALE	address latch enable
ALU	arithmetic/logic unit
AMR	adaptive multi-rate
APE	application chip
APLL	analog phase-locked loop
ASRAM	asynchronous static random-access memory
AU	address unit
BCD	binary coded decimal
BGA	ball grid array
BIST	built-in self-test
CBC	cipher block chaining
CE	chip enable
CFB	cipher feedback
CLE	common latch enable
CMOS	complementary metal oxide semiconductor
CMT	cellular mobile telephone
CP15	coprocessor 15
CPU	central processing unit
CRC	cyclic redundancy check
CS	chip select
CSL	Chip Support Library
CTS	clear-to-send
DARAM	dual-access random-access memory
DCDL	digitally controlled delay element
DCT	discrete cosine transform
DDR	dual data rate
DES	data encryption security
DMA	direct memory access
DPLL	digital phase-locked loop
DSP	digital signal processor
DSPLIB	DSP Library
DSR	data-set-ready
DTR	data-terminal-ready
DU	data unit
ECB	electronic codebook

ACRONYM	DEFINITION
EEPROM	electrically erasable programmable read-only memory
EMIFF	external memory interface fast
EMIFS	external memory interface slow
EOF	end of file
EP	endpoint
ESD	electrostatic discharge
ETM	Embedded Trace Macrocell
FAC	frame adjustment counter
FFT	Fast Fourier Transform
FIFO	first-in first out
FIQ	fast interrupt request
FIR	fast infrared
GP	general-purpose
GPIO	general-purpose input/output
GPRS	General Packet Radio Service
GSM	Global System for Mobile Communications
H.26x	an ITU-TSS standard
HBM	Human Body Model
HC	host controller
HCI	host controller interface
HOM	host-only mode
HS	high-speed
I-cache	instruction cache
I^2C	Inter-integrated circuit
I^2S	Inter-IC Sound (specification)
iDCT	Inverse Discrete Cosine Transform
IDE	integrated development environment
I/F	interface
IFR	Interrupt Flag Register
IMGLIB	Image/Video Processing Library
IMR	Interrupt Mask Register
IO	input/output
IOM-2	ISDN Oriented Modular Interface Revision 2
IrDA	infrared data adapter
IRQ	interrupt request
IU	instruction unit
IV	initialization vector
JPEG	Joint Photographic Experts Group
JTAG	Joint Test Action Group, IEEE 1149.1 standard

ACRONYM	DEFINITION
LB	local bus
LCD	liquid-crystal display
LH	local host
LPG	LED pulse generator light pulse generation
LSB	least significant bit
LVCMOS	low-voltage CMOS
MAC	multiply-accumulate
McBSP	multichannel buffered serial port
MCSI	multichannel serial interface
MD5	Message-Digest Algorithm developed by R. Rivest
MIR	medium infrared
MMC	multimedia card
MMC/SD	multimedia card/secure digital multimedia card/secure data
MMU	memory management unit
MPEG	Moving Picture Experts Group
MPU	microprocessor unit
MPUI	microprocessor unit interface
MPUIO	microprocessor unit I/O
MSB	most significant bit
MVIP	multi-vendor integration protocol
OCP	open core protocol
ODM	original design manufacturer
OEM	original equipment manufacturer
OFB	output feedback
OHCI	open host controller interface
OS	operating system
OTG	on-the-go
PCM	pulse code modulation
PI	pixel interpolation
PU	program unit
PWL	pulse-width light pulse width length
PWM	pulse width modulation
PWT	pulse-width tone pulse width time
R/B	read/busy
RAM	random-access memory
RE	read enable

ACRONYM	DEFINITION
RGB	red green blue
RISC	reduced instruction set computer
RNG	random number generator
ROM	read-only memory
RTC	real-time clock
RTS	request-to-send
RX	receive
SAM	shared-access mode
SARAM	single-access random-access memory
SD	secure digital
SDR	single data rate
SDRAM	synchronous dynamic random-access memory
SDW	short distance wireless
SIR	slow infrared
SPI	serial port interface serial peripheral interface
SRAM	static random-access memory
SRG	Sample Rate Generator
STN	super twisted nematic
T1/E1	T1 is a digital transmission link with a capacity of 1.544 Mbps. It uses two pairs of normal twisted-wires and can handle 24-voice conversations, each digitized using mu-law coding at 64 kbps. T1 is used in USA, Canada, Hong Kong, and Japan. E1 is a digital transmission link with a capacity of 2.048 Mbps. It is the European equivalent of T1. It can handle 30-voice conversations, each digitized using A-law coding at 64 kbps.
TAP	test access port
TC	traffic controller
TDES	triple data encryption security
TFT	thin-film transistor
TI	Texas Instruments
TIPB	TI peripheral bus
TLB	Translation Look-Aside Buffer
TTB	Translation Table Base
TX	transmit
UART	universal asynchronous receiver/transmitter
ULPD	ultra low-power device
URL	uniform resource locator
USB	universal serial bus
VIA	versatile interconnection architecture
VIVT	virtual index virtual tag
WB	write buffer

ACRONYM	DEFINITION
WDT	watchdog timer
WE	write enable
WMA	Windows Media Audio
WMV	Windows Media Video
WP	write protect

7 Mechanical Data

7.1 Package Thermal Resistance Characteristics

Table 7−1 and Table 7−2 provide the thermal resistance characteristics for the recommended package types used on the OMAP5912 device.

Table 7−1. OMAP5912 Thermal Resistance Characteristics (ZZG)

$R_{\Theta JA}$ (°C/W)	$R_{\Theta JB}$ (°C/W)	$R_{\Theta JC}$ (°C/W)	BOARD TYPE†
32.2	10.9	10.4	High-K

† Board types are as defined by JEDEC. Reference JEDEC Standard JESD51−2, Test Boards for Area Array Surface-Mount Package Thermal Measurements.

Table 7−2. OMAP5912 Thermal Resistance Characteristics (ZDY/GDY)

$R_{\Theta JA}$ (°C/W)	$R_{\Theta JB}$ (°C/W)	$R_{\Theta JC}$ (°C/W)	BOARD TYPE†
24.6	14.1	12.6	High-K

† Board types are as defined by JEDEC. Reference JEDEC Standard JESD51−2, Test Boards for Area Array Surface-Mount Package Thermal Measurements.

7.2 Packaging Information

The following packaging information reflects the most current released data available for the designated device(s). This data is subject to change without notice and without revision of this document.

PACKAGING INFORMATION

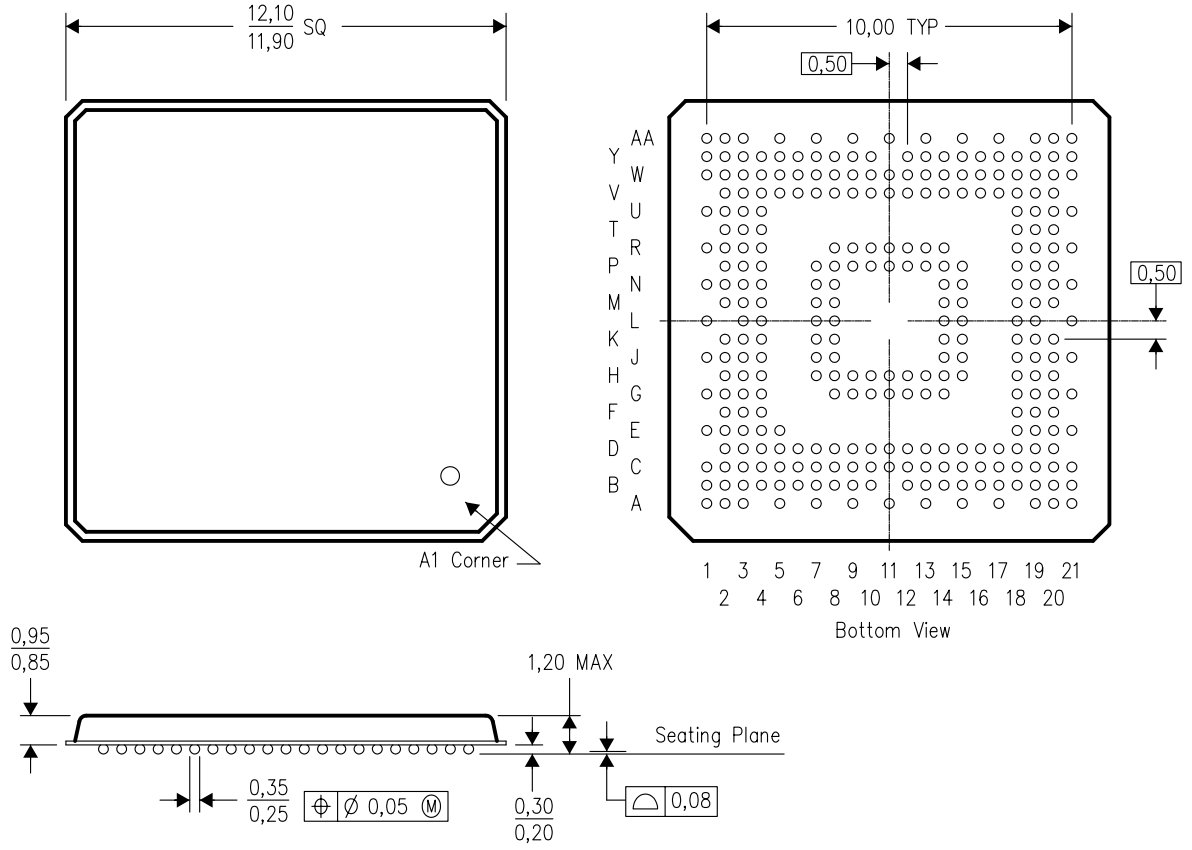
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
OMAP5912ZDY	NRND	BGA	ZDY	289	84	Pb-Free (RoHS)	SNAGCU	Level-3-260C-168 HR	
OMAP5912ZDYA	OBSOLETE	BGA	ZDY	289		TBD	Call TI	Call TI	
OMAP5912ZZG	NRND	BGA MICROSTAR	ZZG	289	160	Green (RoHS & no Sb/Br)	SNAGCU	Level-4-260C-72 HR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

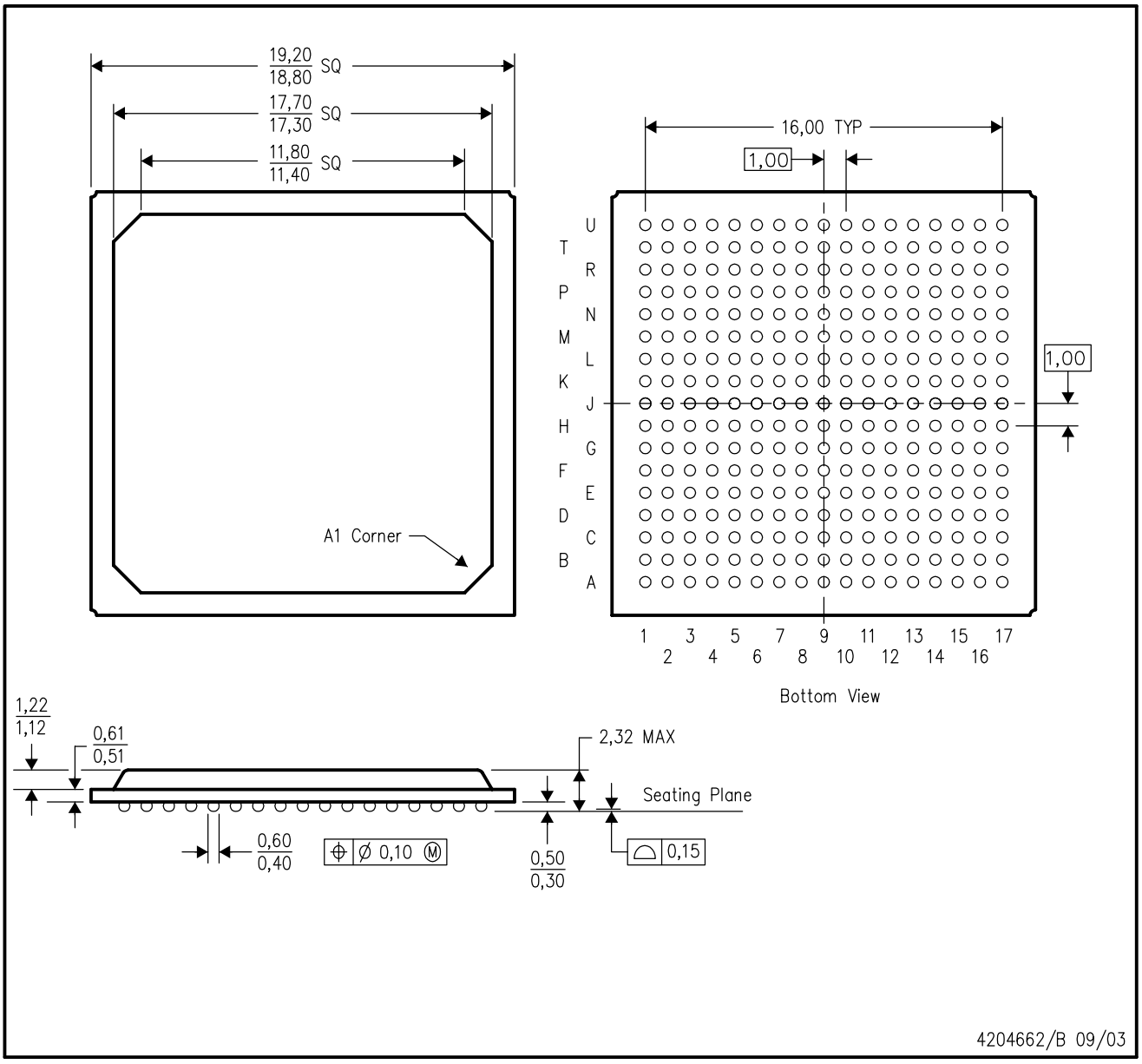
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

ZZG (S–PBGA–N289) PLASTIC BALL GRID ARRAY



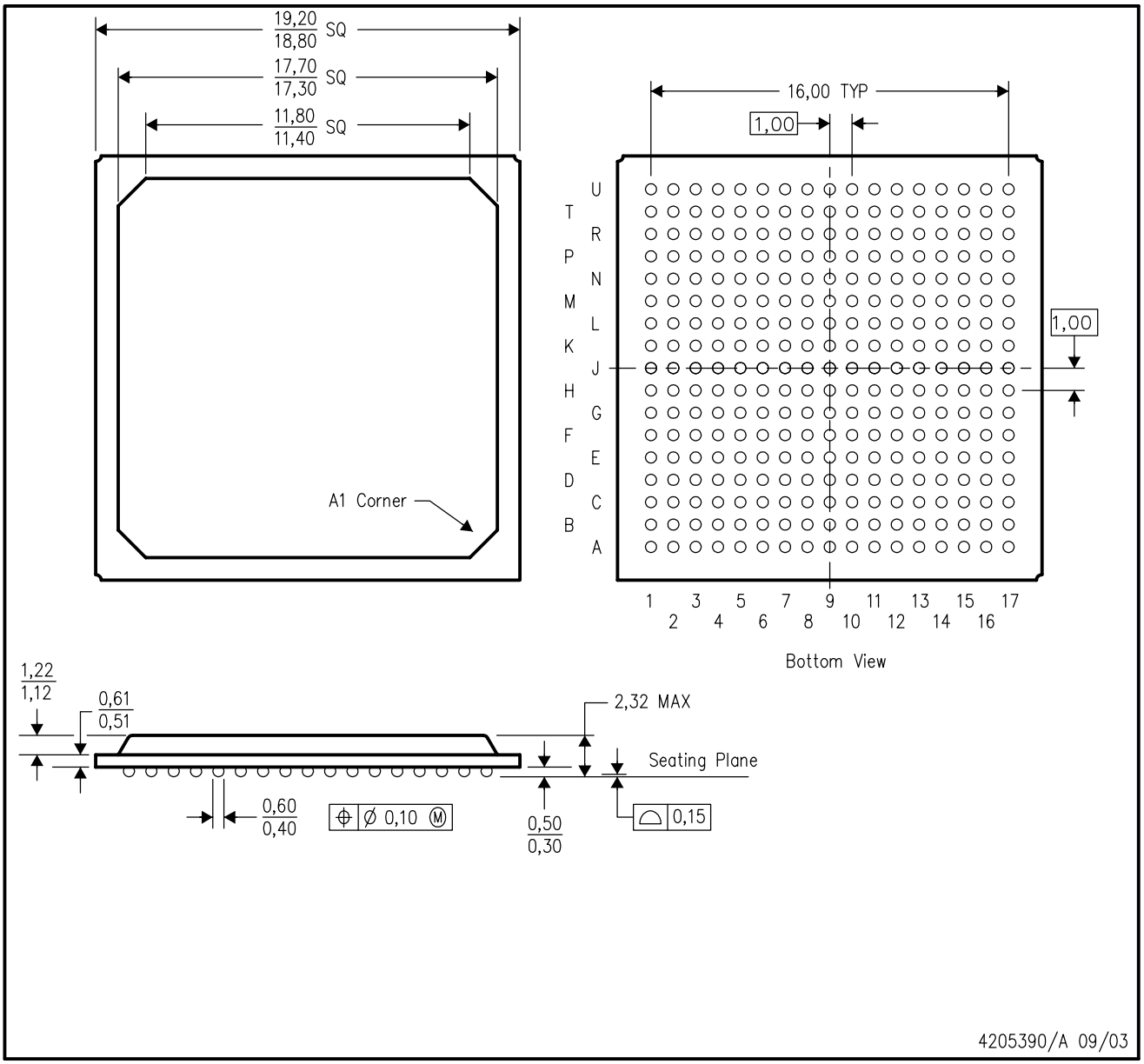
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar BGA configuration
D. This package is lead–free.

GDY (S–PBGA–N289) PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

ZDY (S–PBGA–N289) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is lead free.

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