

CDCLVP111

SCAS859E - JANUARY 2009-REVISED JULY 2011

Low-Voltage 1:10 LVPECL with Selectable Input Clock Driver

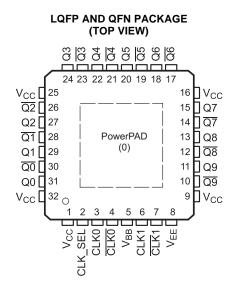
Check for Samples: CDCLVP111

FEATURES

- **Distributes One Differential Clock Input Pair** LVPECL to 10 Differential LVPECL
- Fully Compatible With LVECL/LVPECL
- Supports a Wide Supply Voltage Range From 2.375 V to 3.8 V
- Selectable Clock Input Through CLK_SEL
- Low-Output Skew (Typ 15 ps) for **Clock-Distribution Applications**
 - Additive Jitter Less Than 1 ps
 - Propagation Delay Less Than 350 ps
 - Open Input Default State
 - LVDS, CML, SSTL input compatible
- **V**_{BB} Reference Voltage Output for Single-Ended Clocking
- Available in a 32-Pin LQFP and QFN Package
- Frequency Range From DC to 3.5 GHz
- Pin-to-Pin Compatible With MC100 Series EP111, ES6111, LVEP111, PTN1111

APPLICATIONS

- Designed for Driving 50 Ω Transmission Lines
- **High Performance Clock Distribution**



DESCRIPTION

The CDCLVP111 clock driver distributes one differential clock pair of LVPECL input, (CLK0, CLK1) to ten pairs of differential LVPECL clock (Q0, Q9) outputs with minimum skew for clock distribution. The CDCLVP111 can accept two clock sources into an input multiplexer. The CDCLVP111 is specifically designed for driving 50- Ω transmission lines. When an output pin is not used, leaving it open is recommended to reduce power consumption. If only one of the output pins from a differential pair is used, the other output pin must be identically terminated to 50 Ω .

The V_{BB} reference voltage output is used if single-ended input operation is required. In this case, the V_{BB} pin should be connected to CLK0 and bypassed to GND via a 10-nF capacitor.

However, for high-speed performance up to 3.5 GHz, the differential mode is strongly recommended.

The CDCLVP111 is characterized for operation from -40°C to 85°C.

CLK_SEL	ACTIVE CLOCK INPUT					
0	CLK0, CLK0					
1	CLK1, CLK1					

Table 1. FUNCTION TABLE



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet. PowerPAD is a trademark of Texas Instruments.

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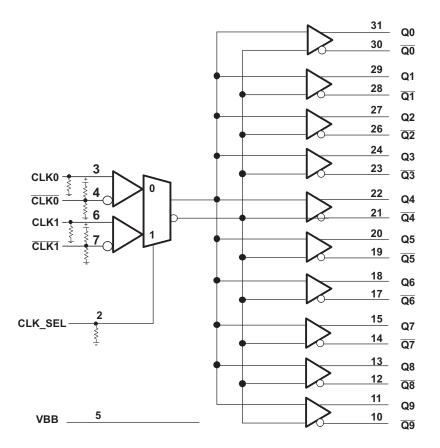
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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DEVICE INFORMATION



PIN FUNCTIONS⁽¹⁾

PIN NAME NO.		DESCRIPTION
		DESCRIPTION
CLK_SEL	2	Clock select. Used to select between CLK0 and CLK1 input pairs. LVTTL/LVCMOS functionality compatible.
CLK0, CLK0	3, 4	
CLK1, CLK1	6, 7	Differential LVECL/LVPECL input pair
Q [9:0]	11, 13, 15, 18, 20, 22, 24, 27, 29, 31	LVECL/LVPECL clock outputs, these outputs provide low-skew copies of CLKn.
<u>Q</u> [9:0]	10, 12, 14, 17, 19, 21,23, 26, 28, 30	LVECL/LVPECL complementary clock outputs, these outputs provide copies of CLKn.
V _{BB}	5	Reference voltage output for single-ended input operation
V _{CC}	1, 9, 16, 25, 32	Supply voltage
V _{EE}	8	Device ground or negative supply voltage in ECL mode
PowerPAD™	0	The PowerPAD of the QFN32 is thermally connected to the die to improve the heat transfer out of the package. The pad of the QFN32 with PowerPAD must be connected to V_{EE} .

(1) CLKn, CLK_SEL pull down resistor = 75 k Ω ; \overline{CLKn} pull up resistor = 37.5 k Ω ; \overline{CLKn} pull down resistor = 50 k Ω .

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ABSOLUTE MAXIMUM RATINGS⁽¹⁾

		VALUE	UNIT
V_{CC}	Supply voltage (Relative to V _{EE})	-0.3 to 4.6	V
VI	Input voltage	–0.3 to V _{CC} + 0.5	V
Vo	Output voltage	–0.3 to V _{CC} + 0.5	V
I _{IN}	Input current	±20	mA
V_{EE}	Negative supply voltage (Relative to V_{CC})	-4.6 to 0.3	V
I _{BB}	Sink/source current	-1 to 1	mA
I _O	DC output current	-50	mA
T _{stg}	Storage temperature range	-65 to 150	°C
TJ	Maximum operating junction temperature	125	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage (relative to V _{EE})	2.375	2.5/3.3	3.8	V
T _A	Operating free-air temperature	-40		85	°C/W
TJ	Operating junction temperature			110	°C

PACKAGE THERMAL IMPEDANCE, VF (LQFP)

		TEST CONDITION	VALUE	UNIT
θ _{JA}		0 LFM	74	°C/W
	Thermal resistance junction to embient ⁽¹⁾	150 LFM	66	°C/W
	Thermal resistance junction to ambient ⁽¹⁾	250 LFM	64	°C/W
		500 LFM	61	°C/W
θ_{JC}	Thermal resistance junction to case		39	°C/W

(1) According to JESD 51-7 standard.

PACKAGE THERMAL IMPEDANCE, RHB (QFN)

		TEST CONDITION	VALUE	UNIT
θ _{JA}		0 LFM	49	°C/W
	Thermal resistance junction to ambient ⁽¹⁾	150 LFM	37	°C/W
	merman resistance junction to ambient ^(*)	250 LFM	36	°C/W
		500 LFM	32	°C/W
θ_{JC}	Thermal resistance junction to case		19	°C/W

(1) According to JESD 51-7 standard.

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TRUMENTS

EXAS

LVECL DC ELECTRICAL CHARACTERISTICS

Vsupply: $V_{CC} = 0 \text{ V}$, $V_{EE} = -2.375 \text{ V}$ to -3.8 V over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
I _{EE}	Supply internal current	Absolute value of current	–40°C, 25°C, 85°C	40		85	mA
			-40°C			354	
I _{CC}	Output and internal supply current	All outputs terminated 50 Ω to V_{CC} – 2 V	25°C			380	mA
			85°C			405	
I _{IN}	Input current	Includes pullup/pulldown resistors, $V_{IH} = V_{CC}$, $V_{IL} = V_{CC}$ - 2 V	–40°C, 25°C, 85°C	-150		150	μA
V _{BB}	Internally generated	For $V_{EE} = -3$ to -3.8 V, $I_{BB} = -0.2$ mA	–40°C, 25°C, 85°C	-1.45	-1.3	-1.15	V
vвв	bias voltage	$V_{EE} = -2.375 \text{ to } -2.75 \text{ V},$ $I_{BB} = -0.2 \text{ mA}$	–40°C, 25°C, 85°C	-1.4	-1.25	-1.1	v
V _{IH}	High-level input voltage (CLK_SEL)		–40°C, 25°C, 85°C	-1.165		-0.88	V
VIL	Low-level input voltage (CLK_SEL)		–40°C, 25°C, 85°C	-1.81		-1.475	V
V _{ID}	Input amplitude (CLKn, CLKn)	Difference of input, See $^{(1)} \left V_{IH} - V_{IL} \right $	–40°C, 25°C, 85°C	0.5		1.3	V
V _{CM}	Common-modevoltage (CLKn, CLKn)	DC offset relative to $V_{\rm EE}$	–40°C, 25°C, 85°C	V _{EE} + 1		-0.3	V
			-40°C	-1.26		-0.85	
/ _{он}	High-level output voltage	$I_{OH} = -21 \text{ mA}$	25°C	-1.2		-0.85	V
			85°C	-1.15		-0.85	
			-40°C	-1.85		-1.5	
V _{OL}	Low-level output voltage	$I_{OL} = -5 \text{ mA}$	25°C	-1.85		-1.45	V
			85°C	-1.85		-1.4	
V _{OD}	Differential output voltage swing	Terminated with 50 Ω to V _{CC} –2 V, See Figure 4	–40°C, 25°C, 85°C	600			mV

(1) V_{ID} minimum and maximum is required to maintain ac specifications, actual device function tolerates a minimum V_{ID} of 100 mV.



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LVPECL DC ELECTRICAL CHARACTERISTICS

Vsupply: V_{CC} = 2.375 V to 3.8 V, V_{EE}= 0 V over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	ТҮР	МАХ	UNIT	
I_{EE}	Supply internal current	Absolute value of current	–40°C, 25°C, 85°C	40		85	mA
	Output and internal supply current		-40°C			354	
I _{CC}		All outputs terminated 50 Ω to V _{CC} – 2 V	25°C			380	mA
	Supply current		85°C			405	
I _{IN}	Input current	Includes pullup/pulldown resistors $V_{IH}=V_{CC}, V_{IL}=V_{CC}-2V$	–40°C, 25°C, 85°C	-150		150	μA
	Internelly, generated	V_{CC} = 3 to 3.8 V, I_{BB} = -0.2 mA	–40°C, 25°C, 85°C	V _{CC} – 1.45	V _{CC} – 1.3	V _{CC} – 1.15	
V_{BB}	Internally generated bias voltage	$V_{CC} = 2.375$ to 2.75 V, $I_{BB} = -0.2$ mA	–40°C, 25°C, 85°C	V _{CC} – 1.4	V _{CC} – 1.25	V _{CC} – 1.1	V
V _{IH}	High-level input voltage (CLK_SEL)		–40°C, 25°C, 85°C	V _{CC} – 1.165		V _{CC} – 0.88	V
V_{IL}	Low-level input voltage (CLK_SEL)		–40°C, 25°C, 85°C	V _{CC} – 1.81		V _{CC} – 1.475	V
V_{ID}	Input amplitude (CLKn, CLKn)	Difference of inpu, see $^{(1)},\left V_{IH}-V_{IL}\right $	–40°C, 25°C, 85°C	0.5		1.3	V
V_{CM}	Common-mode voltage (CLKn, CLKn)	DC offset relative to V_{EE}	–40°C, 25°C, 85°C	1		$V_{CC} - 0.3$	V
			-40°C	V _{CC} – 1.26		$V_{CC} - 0.85$	
V _{OH}	High-level output voltage	I _{OH} = -21 mA	25°C	V _{CC} – 1.2		V _{CC} – 0.85	V
	renage		85°C	V _{CC} – 1.15		$V_{CC} - 0.85$	
			-40°C	V _{CC} – 1.85		V _{CC} – 1.5	
V_{OL}	Low-level output voltage	$I_{OL} = -5 \text{ mA}$	25°C	V _{CC} – 1.85		V _{CC} – 1.45	V
			85°C	V _{CC} – 1.85		V _{CC} – 1.4	
V _{OD}	Differential output voltage swing	Terminated with 50 Ω to V _{CC} - 2 V, See Figure 4	–40°C, 25°C, 85°C	600			mV

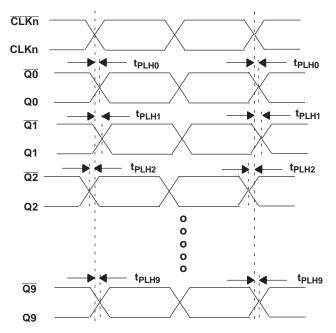
(1) V_{ID} minimum and maximum is required to maintain ac specifications, actual device function tolerates a minimum V_{ID} of 100 mV.

AC ELECTRICAL CHARACTERISTICS

Vsupply: $V_{CC} = 2.375$ V to 3.8 V, $V_{EE} = 0$ V or LVECL/LVPECL input $V_{CC} = 0$ V, $V_{EE} = -2.375$ V to -3.8 V over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{pd}	Differential propagation delay CLKn, CLKn to all Q0, Q0 Q9, Q9	See	200		350	ps
t _{sk(o)}	Output-to-output skew	See , and Figure 1		15	30	ps
t _{sk(pp)}	Part-to-part skew	See , and Figure 1			70	ps
t _{aj}	Additive phase jitter	Integration bandwidth of 20 kHz to 20 MHz, fout = 125 MHz at 25°C		0.04	< 0.8	ps
f _(max)	Maximum frequency	Functional up to 3.5 GHz, see Figure 4			3500	MHz
t _r /t _f	Output rise and fall time (20%, 80%)	See Note D in Figure 1	90		200	ps





- A. Output skew is calculated as the greater of: The difference between the fastest and the slowest t_{PLHn} (n = 0, 1,...9) or the difference between the fastest and the slowest t_{PHLn} (n = 0, 1,...9).
- B. Part-to-part skew, is calculated as the greater of: The difference between the fastest and the slowest t_{PLHn} (n = 0, 1,...9) across multiple devices or the difference between the fastest and the slowest t_{PHLn} (n = 0, 1,...9) across multiple devices.
- C. Typical value measured at ambient when clock input is 155.52MHz for an integration bandwidth of 20 kHz to 5 MHz.
- D. Input conditions: V_{CM} = 1 V, V_{ID} = 0.5 V and F_{IN} = 1GHz.

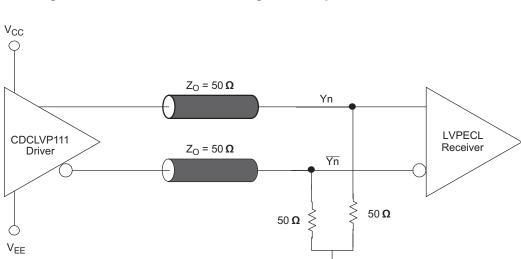


Figure 1. Waveform for Calculating Both Output and Part-to-Part Skew

Figure 2. Typical Termination for Output Driver (See the Interfacing Between LVPECL, LVDS, and CML Application Note, Literature Number SCAA056)

 $VT = V_{CC} - 2 V$



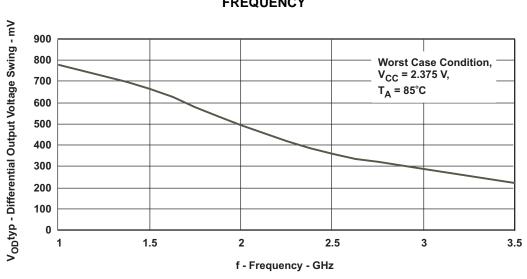


Figure 3. DIFFERENTIAL OUTPUT VOLTAGE SWING vs FREQUENCY





REVISION HISTORY

Cł	nanges from Original (January 2009) to Revision A Page
•	Changed note referneces within the AC ELECTRICAL CHARACTERISTICS table
•	Added a Typ value of 0.04ps to the Additive phase jitter in the AC ELECTRICAL CHARACTERISTICS
Cł	nanges from Revision A (March 2009) to Revision B Page
•	Added LVTTL/LVCMOS functionality compatible
Cł	nanges from Revision B (April 2009) to Revision C Page
•	Changed PowerPAD information to the Pinout Package 1
•	Added PowerPAD information to the Pin Functions table
Cł	nanges from Revision C (November 2009) to Revision D Page
•	Changed the PowerPAD description in the PIN FUNCTIONS table to include the LQFP package information
•	Deleted duplicate information covering the PowerPAD from Note 1 of the Pin Functions table
Cł	nanges from Revision D (March 2010) to Revision E Page
•	Changed the PowerPAD Pin Function Description
•	Added text "See Note D in Figure 1" to the t_r/t_f Test Conditions in the AC ELECTRICAL CHARACTERITICS table



PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
CDCLVP111RHBR	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
CDCLVP111RHBT	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
CDCLVP111VF	ACTIVE	LQFP	VF	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CDCLVP111VFR	ACTIVE	LQFP	VF	32	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION

REEL DIMENSIONS

TEXAS INSTRUMENTS





TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCLVP111RHBR	QFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
CDCLVP111RHBT	QFN	RHB	32	250	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
CDCLVP111VFR	LQFP	VF	32	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2

TEXAS INSTRUMENTS

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PACKAGE MATERIALS INFORMATION

3-Mar-2012



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCLVP111RHBR	QFN	RHB	32	3000	338.1	338.1	20.6
CDCLVP111RHBT	QFN	RHB	32	250	338.1	338.1	20.6
CDCLVP111VFR	LQFP	VF	32	1000	333.2	345.9	28.6



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) Package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO-220.



RHB (S-PVQFN-N32)

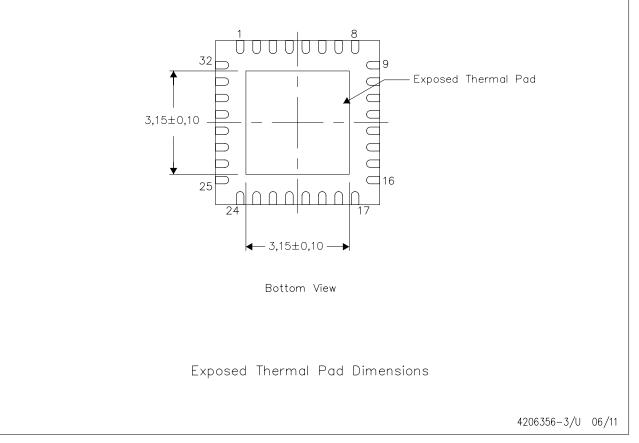
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

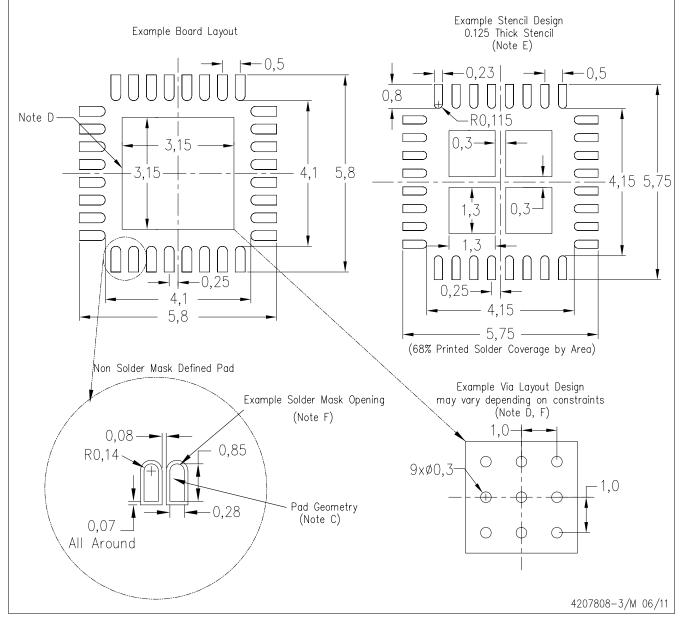


NOTE: A. All linear dimensions are in millimeters





PLASTIC QUAD FLATPACK NO-LEAD



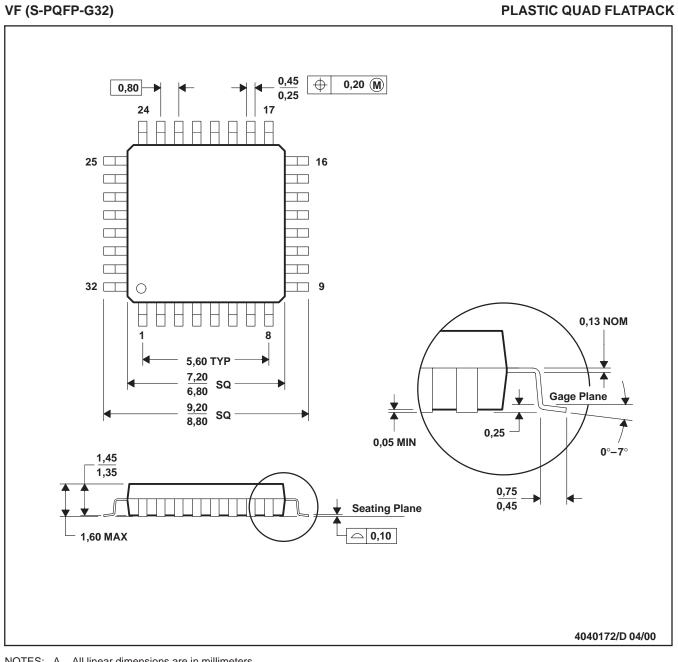
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com http://www.ti.com.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.



MECHANICAL DATA

MTQF002B - JANUARY 1995 - REVISED MAY 2000



NOTES: A. All linear dimensions are in millimeters. B. This drawing is subject to change without notice.



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Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers		
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps		
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