

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X

16-bit Microcontrollers and Digital Signal Controllers (up to 256 KB Flash and 32 KB SRAM) with High-Speed PWM, Op amps, and Advanced Analog

Operating Conditions

- 3.0V to 3.6V, -40°C to +85°C, DC to 70 MIPS
- 3.0V to 3.6V, -40°C to +125°C, DC to 60 MIPS

Core: 16-bit dsPIC33E/PIC24E CPU

- · Code-efficient (C and Assembly) architecture
- · Two 40-bit wide accumulators
- · Single-cycle (MAC/MPY) with dual data fetch
- · Single-cycle mixed-sign MUL plus hardware divide
- · 32-bit multiply support

Clock Management

- · 0.9% internal oscillator
- · Programmable PLLs and oscillator clock sources
- Fail-Safe Clock Monitor (FSCM)
- · Independent Watchdog Timer (WDT)
- · Fast wake-up and start-up

Power Management

- · Low-power management modes (Sleep, Idle, Doze)
- · Integrated Power-on Reset and Brown-out Reset
- 0.6 mA/MHz dynamic current (typical)
- 30 µA IPD current (typical)

High-Speed PWM

- · Up to three PWM pairs with independent timing
- Dead time for rising and falling edges
- 7.14 ns PWM resolution
- PWM support for:
 - DC/DC, AC/DC, Inverters, PFC, Lighting
- BLDC, PMSM, ACIM, SRM
- · Programmable Fault inputs
- · Flexible trigger configurations for ADC conversions

Advanced Analog Features

- · ADC module:
 - Configurable as 10-bit, 1.1 Msps with four S&H or 12-bit. 500 ksps with one S&H
 - Six analog inputs on 28-pin devices and up to 16 analog inputs on 64-pin devices
- · Flexible and independent ADC trigger sources
- Up to three Op amp/Comparators with direct connection to the ADC module:
 - Additional dedicated comparator
 - Programmable references with 32 voltage points
- Charge Time Measurement Unit (CTMU):
 - Supports mTouch™ capacitive touch sensing
 - Provides high-resolution time measurement (1 ns)
 - On-chip temperature measurement

Timers/Output Compare/Input Capture

- · 12 general purpose timers:
 - Five 16-bit and up to two 32-bit timers/counters
 - Four OC modules configurable as timers/counters
 - PTG module with two configurable timers/counters
 - 32-bit Quadrature Encoder Interface (QEI) module configurable as a timer/counter
- · Four IC modules
- · Peripheral Pin Select (PPS) to allow function remap
- Peripheral Trigger Generator (PTG) for scheduling complex sequences

Communication Interfaces

- Two UART modules (17.5 Mbps)
 - With support for LIN 2.0 protocols and IrDA®
- Two 4-wire SPI modules (15 Mbps)
- ECAN™ module (1 Mbaud) CAN 2.0B support
- Two I²C[™] modules (up to 1 Mbaud) with SMBus support
- · PPS to allow function remap
- Programmable Cyclic Redundancy Check (CRC)

Direct Memory Access (DMA)

- · 4-channel DMA with user-selectable priority arbitration
- · UART, SPI, ADC, ECAN, IC, OC, and Timers

Input/Output

- Sink/Source 15 mA or 10 mA, pin-specific for standard VOH/VOL, up to 22 or 14 mA, respectively for non-standard VOH1
- 5V-tolerant pins
- Selectable open drain, pull-ups, and pull-downs
- Up to 5 mA overvoltage clamp current
- · External interrupts on all I/O pins

Qualification and Class B Support

- AEC-Q100 REVG (Grade 1 -40°C to +125°C) planned
- AEC-Q100 REVG (Grade 0 -40°C to +150°C) planned
- Class B Safety Library, IEC 60730

Debugger Development Support

- · In-circuit and in-application programming
- · Two program and two complex data breakpoints
- IEEE 1149.2-compatible (JTAG) boundary scan
- · Trace and run-time watch

Packages

_										
Type	SPDIP	SOIC	SSOP	QFN-S	QI	FN	VT	LA	TC	(FP
Pin Count	28	28	28	28	44	64	36	44	44	64
I/O Pins	21	21	21	21	35	53	25	35	35	53
Contact Lead/Pitch	.100"	1.27	0.65	0.65	0.65	0.50	0.	50	0.	50
Dimensions	1.365x.240x.120"	17.9x7.50x2.05	10.50x7.80x2	6x6x0.9	8x8x0.9	9x9x.9	5x5x0.5	6x6x0.5	10x	10x1

Note: All dimensions are in millimeters (mm) unless specified.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, AND PIC24EPXXXGP/MC20X PRODUCT FAMILIES

The device names, pin counts, memory sizes, and peripheral availability of each device are listed in Table 1 (General Purpose Families) and Table 2 (Motor Control Families). Their pinout diagrams appear on the following pages.

TABLE 1: dsPIC33EPXXXGP50X and PIC24EPXXXGP20X GENERAL PURPOSE FAMILIES

	(S)	es)			Ren	nappa	ble Pe	eriphe	rals				ũ							
Device	Page Erase Size (Instructions)	Program Flash Memory (Kbytes)	RAM (Kbyte)	16-bit/32-bit Timer	Input Capture	Output Compare	UART	(₂)IdS	ECAN™ Technology	External Interrupts ⁽³⁾	I ² Стм	CRC Generator	10-bit/12-bit ADC (Channels)	Analog Comparator	Op amp/Comparator	СТМО	PTG	I/O Pins	Pins	Packages
PIC24EP32GP202	512	32	4																	SPDIP.
PIC24EP64GP202	1024	64	8	5	4	4	2	2		3	2	1	6	1 ⁽¹⁾	2	Yes	Yes	21	28	SOIC,
PIC24EP128GP202	1024	128	16	5	4	4	_	_	_	3	2	'	0	1, ,	_	res	res	21	20	SSOP,
PIC24EP256GP202	1024	256	32																	QFN-S
PIC24EP32GP203	512	32	4	5	4	4	2	2		3	2	1	8	1	3	Vaa	Vaa	25	26	\/TL
PIC24EP64GP203	1024	64	8	5	4	4	2	2	_	3	2	1	8	1	3	Yes	Yes	25	36	VTLA
PIC24EP32GP204	512	32	4		4	4	2	2					9	1	3	Yes		35	44	VTLA, TQFP,
PIC24EP64GP204	1024	64	8	_						_	0	,					Yes			
PIC24EP128GP204	1024	128	16	5		4	2	2	_	3	2	1	9		3	res	res			QFN
PIC24EP256GP204	1024	256	32																	
PIC24EP64GP206	1024	64	8																	
PIC24EP128GP206	1024	128	16	5	4	4	2	2	_	3	2	1	16	1	3	Yes	Yes	53	64	TQFP, QFN
PIC24EP256GP206	1024	256	32																	QIIV
dsPIC33EP32GP502	512	32	4																	SPDIP.
dsPIC33EP64GP502	1024	64	8	5	4	4	2	2	1	3	2	1	6	1 ⁽¹⁾	2	Voo	Vaa	24	28	SOIC,
dsPIC33EP128GP502	1024	128	16	5	4	4	_	_	'	3	2		0	1, ,		Yes	Yes	21	20	SSOP,
dsPIC33EP256GP502	1024	256	32																	QFN-S
dsPIC33EP32GP503	512	32	4	5	4	4	2	2	1	3	2	1	8	1	3	Vaa	Vaa	25	36	VTLA
dsPIC33EP64GP503	1024	64	8	5	4	4	_	_	'	3	2	'	٥	'	3	Yes	Yes	25	30	VILA
dsPIC33EP32GP504	512	32	4																	
dsPIC33EP64GP504	1024	64	8	5	4	4	2	2	1	3	2	1	9	1	3	Voc	Voc	35	44	VTLA,
dsPIC33EP128GP504	1024	128	16	Э	4	4	~	~	'	3		'	9	'	٥	Yes	Yes	ან	44	TQFP, QFN
dsPIC33EP256GP504	1024	256	32																	
dsPIC33EP64GP506	1024	64	8																	
dsPIC33EP128GP506	1024	128	16	5	4	4	2	2	1	3	2	1	16	1	3	Yes	Yes	53	64	TQFP, QFN
dsPIC33EP256GP506	1024	256	32																	Q() (

Note 1: On 28-pin devices, Comparator 4 does not have external connections. Refer to Section 25.0 "Op amp/Comparator Module" for details.

^{2:} Only SPI2 is remappable.

^{3:} INT0 is not remappable.

TABLE 2: dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X MOTOR CONTROL FAMILIES

		(Si				Re	mappa	ble Pe	eripho	erals												
Device	Page Erase Size (Instructions)	Program Flash Memory (Kbytes)	RAM (Kbytes)	16-bit/32-bit Timer	Input Capture	Output Compare	Motor Control PWM ⁽⁴⁾ (Channels)	Quadrature Encoder Interface	UART	SPI ⁽²⁾	ECAN™ Technology	External Interrupts ⁽³⁾	12С™	CRC Generator	10-bit/12-bit ADC (Channels)	Analog Comparator	Op amp/Comparator	СТМО	PTG	I/O Pins	Pins	Packages
PIC24EP32MC202	512	32	4																			SPDIP,
PIC24EP64MC202	1024	64	8	5	4	4	6	1	2	2	_	3	2	1	6	1(1)	2	Yes	Yes	21	28	SOIC,
PIC24EP128MC202	1024	128	16			ľ		·	_	_			_	•			_		100			SSOP, QFN-S
PIC24EP256MC202	1024	256	32																			QINO
PIC24EP32MC203	512	32	4	5	4	4	6	1	2	2		3	2	1	8	1	3	Yes	Yes	25	36	VTLA
PIC24EP64MC203	1024	64	8	J	7		Ů					,			Ü	'	٥	103	103	23	30	VILA
PIC24EP32MC204	512	32	4																			
PIC24EP64MC204	1024	64	8	5	4	4	6	1	2	2		3	2	1	9	1	3	Yes	Yes	35	44	VTLA, TQFP,
PIC24EP128MC204	1024	128	16	5	4	4	0	'		_		3	_	'	9	'	3	165	165	33	44	QFN
PIC24EP256MC204	1024	256	32																			
PIC24EP64MC206	1024	64	8																			
PIC24EP128MC206	1024	128	16	5	4	4	6	1	2	2	_	3	2	1	16	1	3	Yes	Yes	53	64	TQFP, QFN
PIC24EP256MC206	1024	256	32																			QIIV
dsPIC33EP32MC202	512	32	4																			
dsPIC33EP64MC202	1024	64	8	_									_		_	. (1)				l		SPDIP, SOIC,
dsPIC33EP128MC202	1024	128	16	5	4	4	6	1	2	2	_	3	2	1	6	1 ⁽¹⁾	2	Yes `	Yes	21	28	SSOP,
dsPIC33EP256MC202	1024	256	32																			QFN-S
dsPIC33EP32MC203	512	32	4									_	_	_								
dsPIC33EP64MC203	1024	64	8	5	4	4	6	1	2	2	_	3	2	1	8	1	3	Yes	Yes	25	36	VTLA
dsPIC33EP32MC204	512	32	4																			
dsPIC33EP64MC204	1024	64	8																			VTLA,
dsPIC33EP128MC204	1024	128	16	5	4	4	6	1	2	2	-	3	2	1	9	1	3	Yes	Yes	35	44	TQFP, QFN
dsPIC33EP256MC204	1024	256	32																			QIII
dsPIC33EP64MC206	1024	64	8																			
dsPIC33EP128MC206	1024	128	16	5	4	4	6	1	2	2	_	3	2	1	16	1	3	Yes	Yes	53	64	TQFP,
dsPIC33EP256MC206	1024	256	32				-							•	•							QFN
dsPIC33EP32MC502	512	32	4																			
dsPIC33EP64MC502	1024	64	8													,						SPDIP, SOIC,
dsPIC33EP128MC502	1024	128	16	5	4	4	6	1	2	2	1	3	2	1	6	1 ⁽¹⁾	2	Yes	Yes	21	28	SSOP,
dsPIC33EP256MC502	1024	256	32																			QFN-S
dsPIC33EP32MC503	512	32	4																			VTLA
dsPIC33EP64MC503	1024	64	8	5	4	4	6	1	2	2	1	3	2	1	8	1	3	Yes	Yes	25	36	
dsPIC33EP32MC504	512	32	4																			VTLA,
dsPIC33EP64MC504	1024	64	8																			TQFP,
dsPIC33EP128MC504	1024	128	16	5	4	4	6	1	2	2	1	3	2	1	9	1	3	Yes	Yes	35	44	QFN
dsPIC33EP256MC504	1024	256	32																			
dsPIC33EP64MC506	1024	64	8																			
dsPIC33EP128MC506	1024	128	16	5	4	4	6	1	2	2	1	3	2	1	16	1	3	Yes	Yes	53	64	TQFP,
dsPIC33EP256MC506	1024	256	32	,	-	-		'			'	,	_	'	'0	'	,	163	100	33	"	QFN
Note 1: On 29 pin	1024	200	52		L	1	1			Щ.	L		I		<u> </u>		L	<u> </u>				

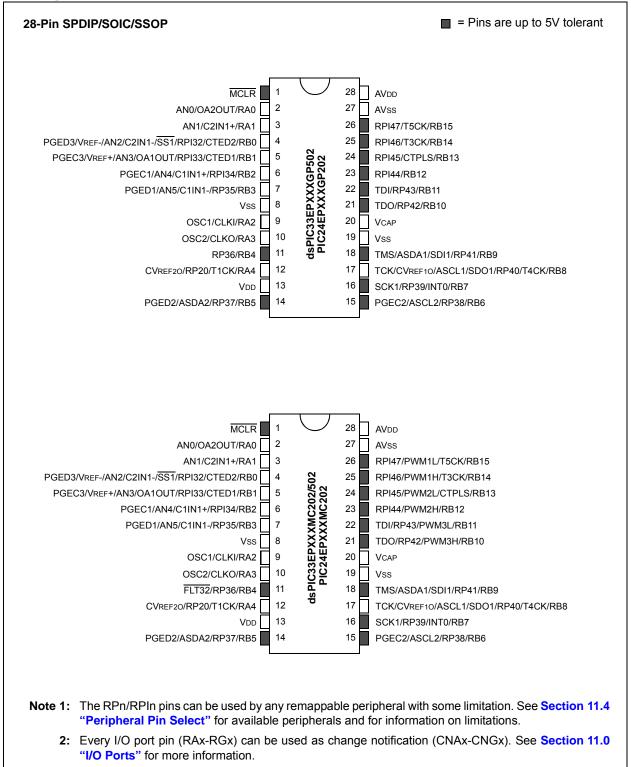
1: On 28-pin devices, Comparator 4 does not have external connections. Refer to Section 25.0 "Op amp/Comparator Module" for details. Note

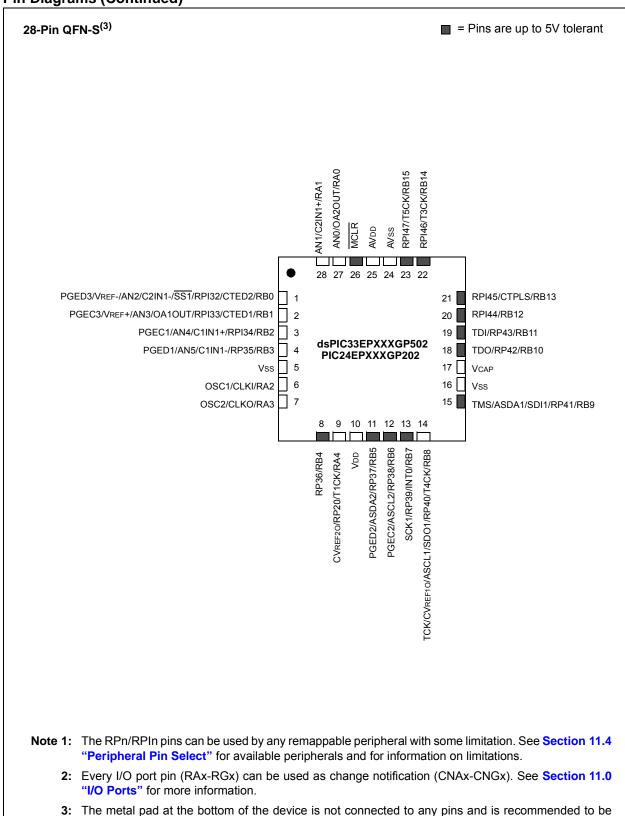
^{2:} Only SPI2 is remappable.

INT0 is not remappable. 3:

Only the PWM Faults are remappable.

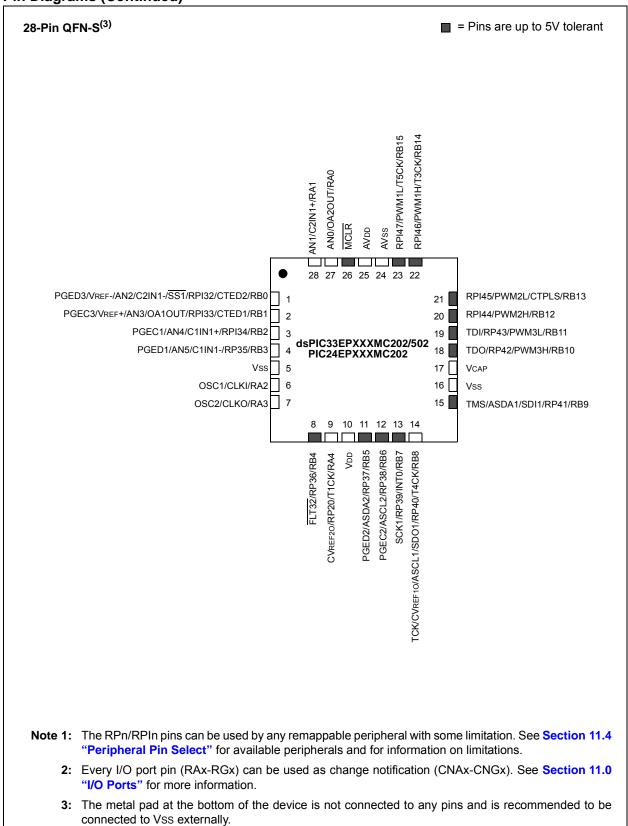


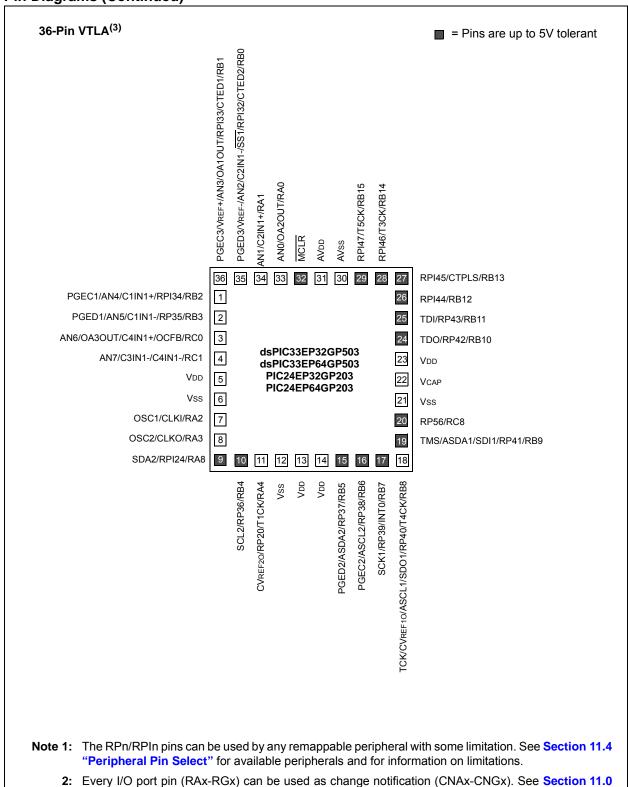




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connected to Vss externally.



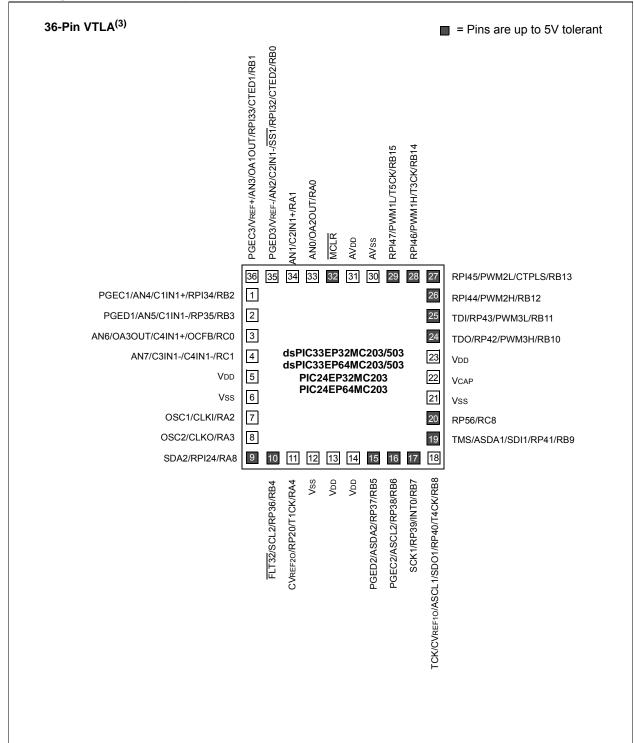


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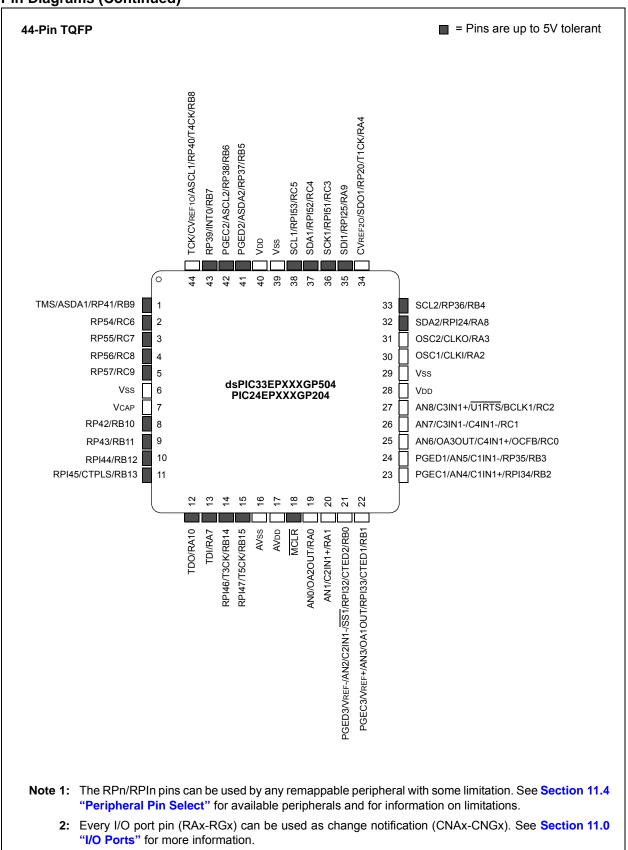
3: The metal pad at the bottom of the device is not connected to any pins and is recommended to be

"I/O Ports" for more information.

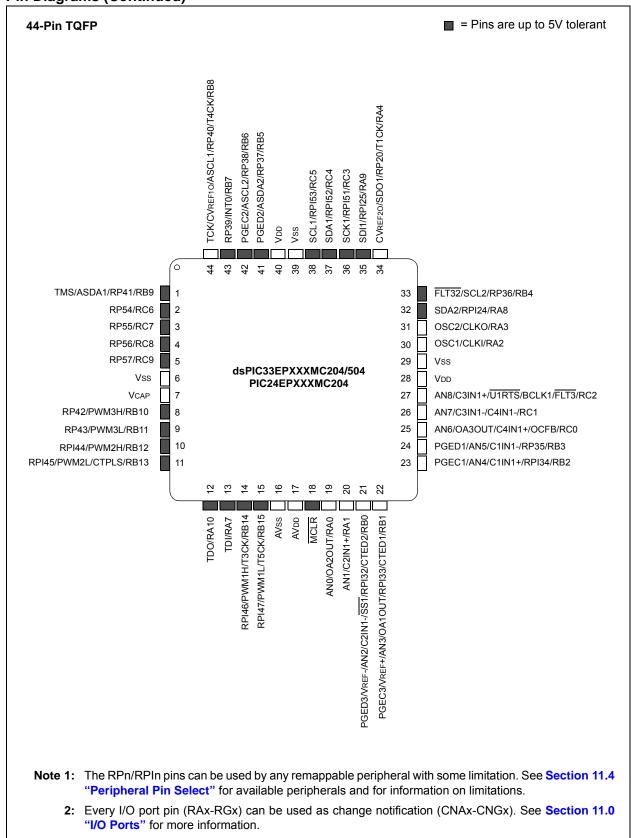
connected to Vss externally.

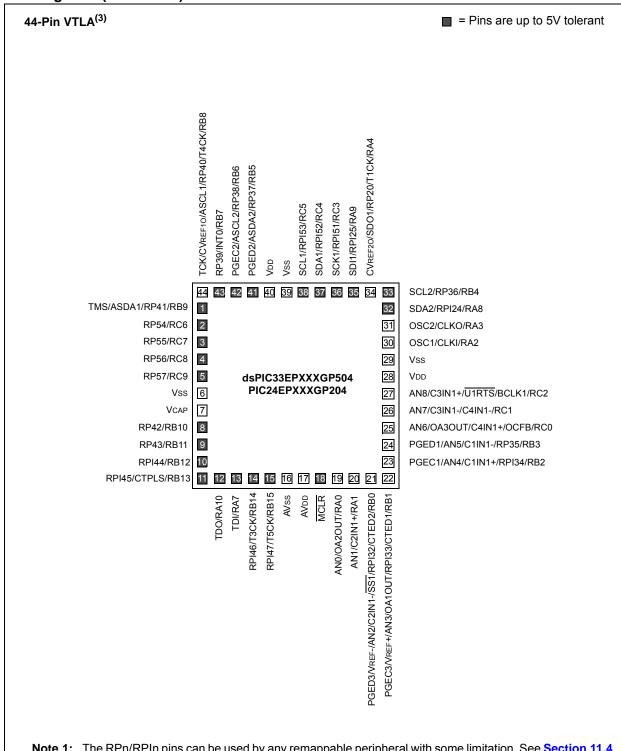


- **Note 1:** The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4** "**Peripheral Pin Select**" for available peripherals and for information on limitations.
 - 2: Every I/O port pin (RAx-RGx) can be used as change notification (CNAx-CNGx). See Section 11.0 "I/O Ports" for more information.
 - **3:** The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.



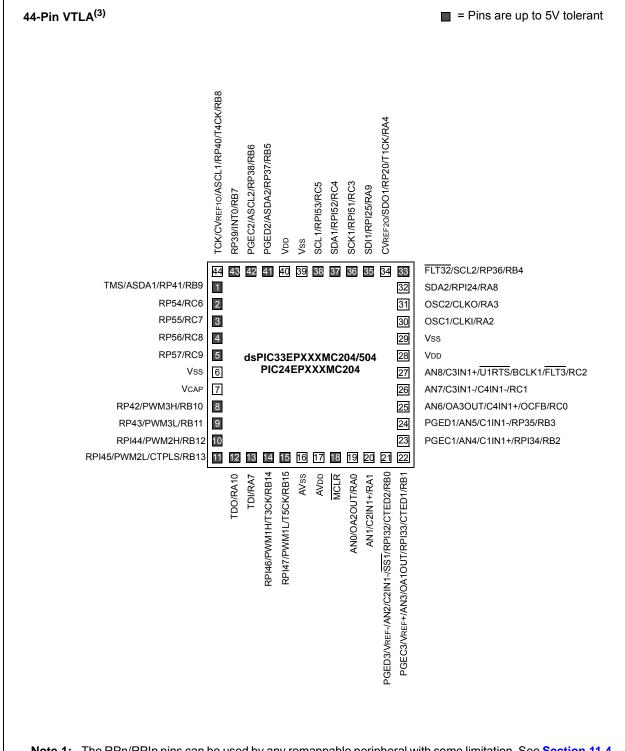
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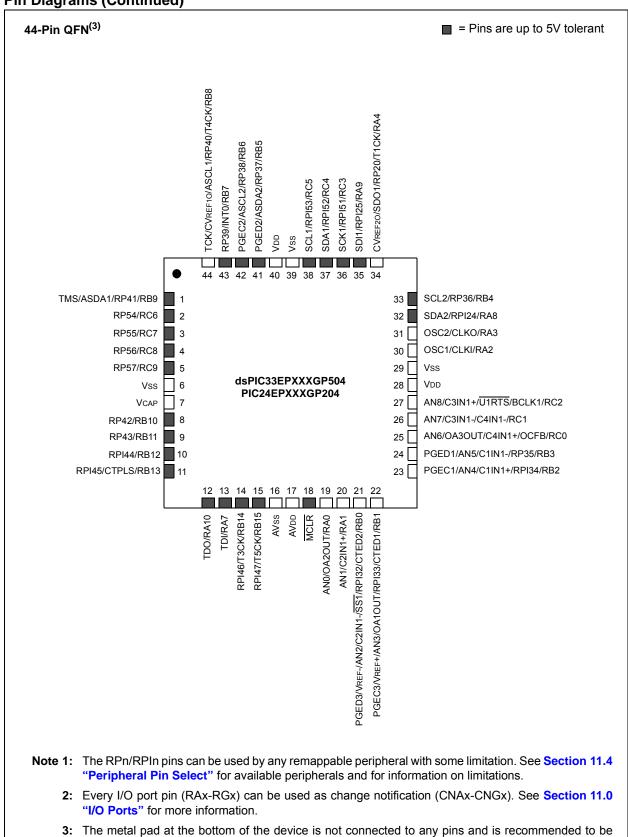


- **Note 1:** The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4** "**Peripheral Pin Select**" for available peripherals and for information on limitations.
 - 2: Every I/O port pin (RAx-RGx) can be used as change notification (CNAx-CNGx). See Section 11.0 "I/O Ports" for more information.
 - **3:** The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.

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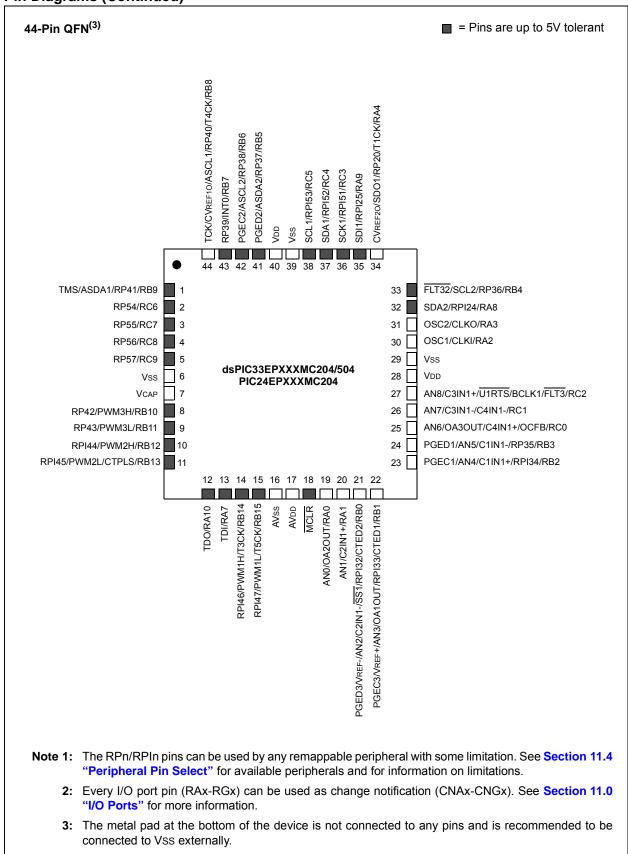
- **Note 1:** The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4** "**Peripheral Pin Select**" for available peripherals and for information on limitations.
 - 2: Every I/O port pin (RAx-RGx) can be used as change notification (CNAx-CNGx). See Section 11.0 "I/O Ports" for more information.
 - **3:** The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.

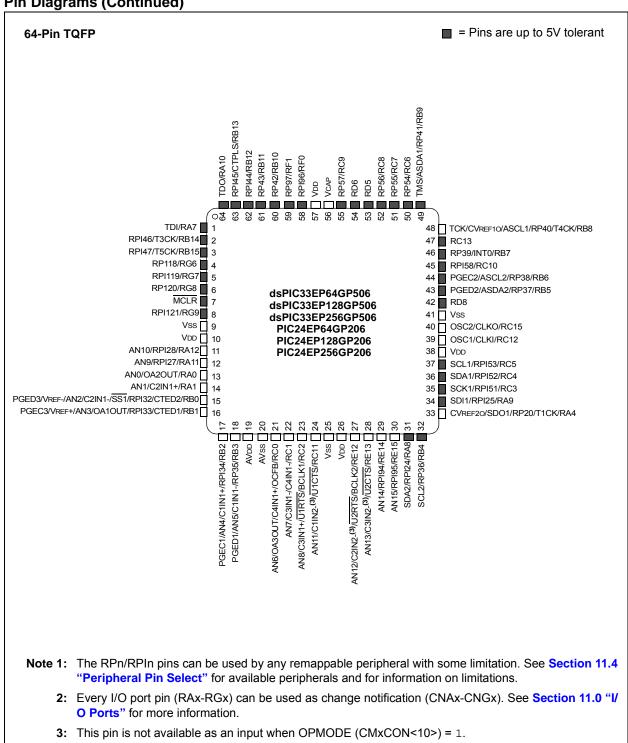


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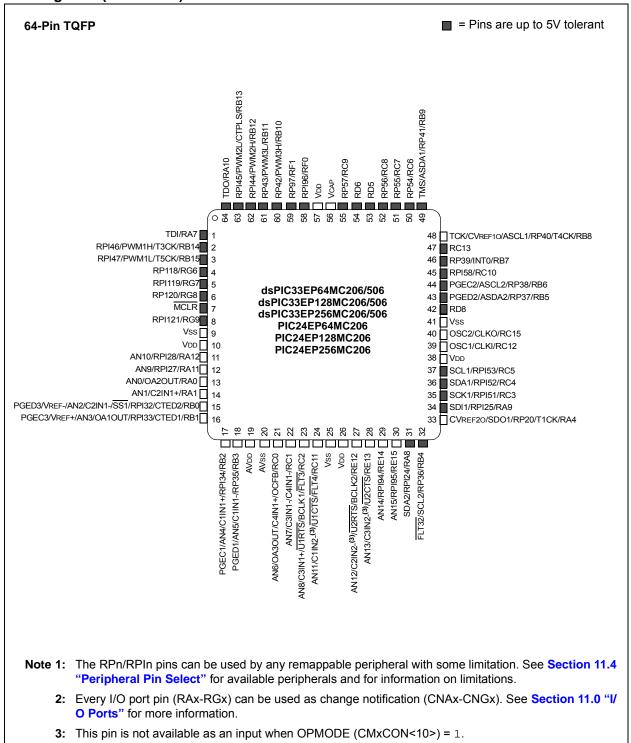
connected to Vss externally.

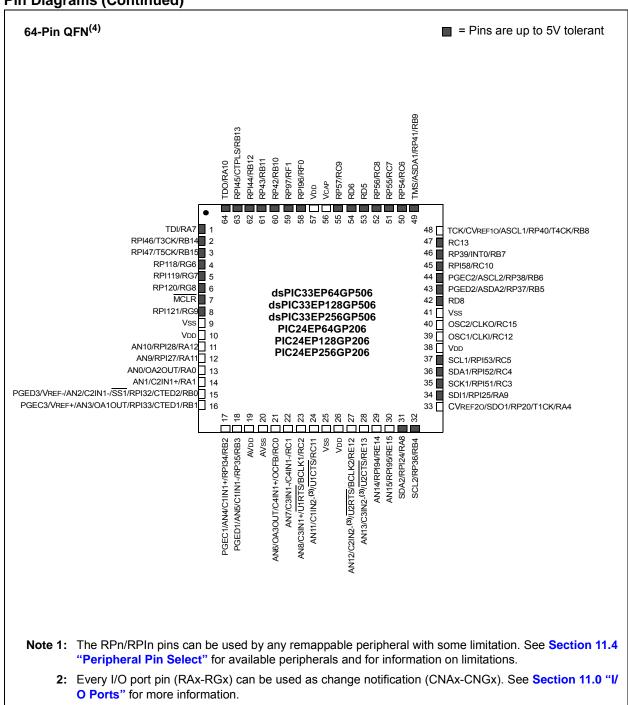






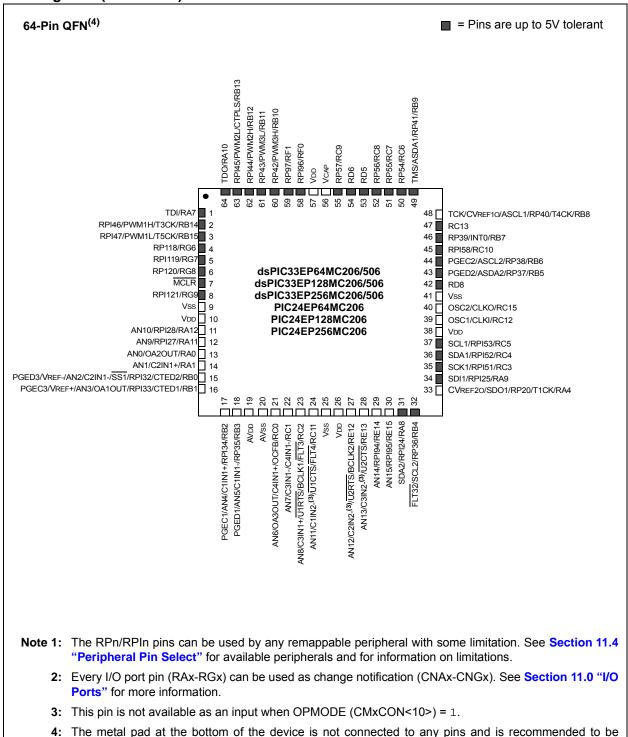
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- 3: This pin is not available as an input when OPMODE (CMxCON<10>) = 1.
- 4: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.

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connected to Vss externally.

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An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

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Referenced Sources

This device data sheet is based on the following individual chapters of the "dsPIC33E/PIC24E Family Reference Manual". These documents should be considered as the general reference for the operation of a particular module or device feature.

Note 1: To access the documents listed below, browse to the documentation section of the dsPIC33EP64MC506 product page of the Microchip web site (www.microchip.com) or select a family reference manual section from the following list.

In addition to parameters, features, and other documentation, the resulting page provides links to the related family reference manual sections.

- Section 1. "Introduction" (DS70573)
- Section 2. "CPU" (DS70359)
- Section 3. "Data Memory" (DS70595)
- Section 4. "Program Memory" (DS70613)
- Section 5. "Flash Programming" (DS70609)
- Section 6. "Interrupts" (DS70600)
- Section 7. "Oscillator" (DS70580)
- Section 8. "Reset" (DS70602)
- Section 9. "Watchdog Timer and Power-Saving Modes" (DS70615)
- Section 10. "I/O Ports" (DS70598)
- Section 11. "Timers" (DS70362)
- Section 12. "Input Capture" (DS70352)
- Section 13. "Output Compare" (DS70358)
- Section 14. "High-Speed PWM" (DS70645)
- Section 15. "Quadrature Encoder Interface (QEI)" (DS70601)
- Section 16. "Analog-to-Digital Converter (ADC)" (DS70621)
- Section 17. "UART" (DS70582)
- Section 18. "Serial Peripheral Interface (SPI)" (DS70569)
- Section 19. "Inter-Integrated Circuit (I²C™)" (DS70330)
- Section 21. "Enhanced Controller Area Network (ECAN™)" (DS70353)
- Section 22. "Direct Memory Access (DMA)" (DS70348)
- Section 23. "CodeGuard™ Security" (DS70634)
- Section 24. "Programming and Diagnostics" (DS70608)
- Section 26. "Op amp/Comparator" (DS70357)
- Section 27. "Programmable Cyclic Redundancy Check (CRC)" (DS70346)
- Section 30. "Device Configuration" (DS70618)
- Section 32. "Peripheral Trigger Generator (PTG)" (DS70669)
- Section 33. "Charge Time Measurement Unit (CTMU)" (DS70661)

1.0 DEVICE OVERVIEW

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive resource. To complement the information in this data sheet, refer to the related section of the "dsPIC33E/PIC24E Family Reference Manual", which is available from the Microchip web site (www.microchip.com)

2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

This document contains device-specific information for the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X, and PIC24EPXXXGP/MC20X Digital Signal Controller (DSC) and Microcontroller (MCU) devices.

the dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices contain extensive Digital Signal Processor (DSP) functionality with a high-performance 16-bit MCU architecture.

Figure 1-1 shows a general block diagram of the core and peripheral modules. Table 1-1 lists the functions of the various pins shown in the pinout diagrams.

FIGURE 1-1: dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, AND PIC24EPXXXGP/MC20X BLOCK DIAGRAM

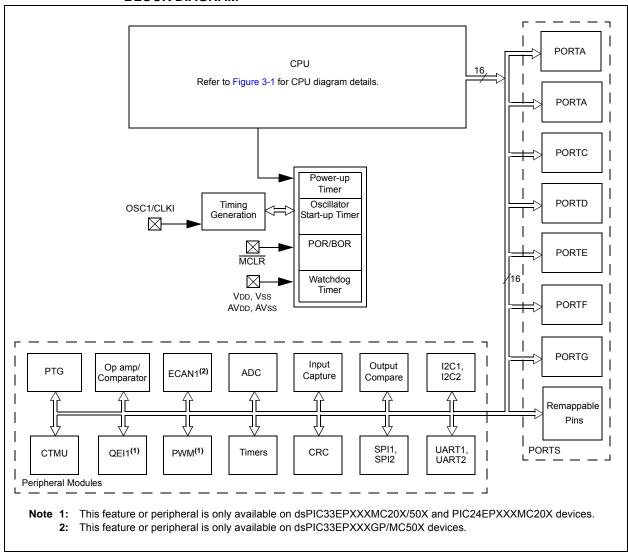


TABLE 1-1: PINOUT I/O DESCRIPTIONS

Pin Name ⁽⁴⁾	Pin Type	Buffer Type	PPS	Description
AN0-AN15	I	Analog	No	Analog input channels.
CLKI	0	ST/ CMOS	No	External clock source input. Always associated with OSC1 pin function. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
CLKO OSC1	-	ST/	No	Always associated with OSC2 pin function.
OSC2	I/O	CMOS	No No	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
REFCLKO	0	_	Yes	Reference clock output.
IC1-IC4	I	ST	Yes	Capture inputs 1 through 4.
OCFA OCFB OC1-OC4	- - 0	ST ST —	Yes No Yes	Compare Fault A input (for Compare channels). Compare Fault B input (for Compare channels). Compare outputs 1 through 4.
INTO INT1 INT2	 	ST ST ST	No Yes Yes	External interrupt 0. External interrupt 1. External interrupt 2.
RA0-RA4, RA7-RA12	I/O	ST	No	PORTA is a bidirectional I/O port.
RB0-RB15	I/O	ST	No	PORTB is a bidirectional I/O port.
RC0-RC13, RC15	I/O	ST	No	PORTC is a bidirectional I/O port.
RD5, RD6, RD8	I/O	ST	No	PORTD is a bidirectional I/O port.
RE12-RE15	I/O	ST	No	PORTE is a bidirectional I/O port.
RF0, RF1	I/O	ST	No	PORTF is a bidirectional I/O port.
RG6-RG9	I/O	ST	No	PORTG is a bidirectional I/O port.
T1CK T2CK T3CK T4CK T5CK		ST ST ST ST ST	No Yes No No No	Timer1 external clock input. Timer2 external clock input. Timer3 external clock input. Timer4 external clock input. Timer5 external clock input.
CTPLS CTED1 CTED2	0 	ST ST ST	No No No	CTMU pulse output. CTMU external edge input 1. CTMU external edge input 2.
U1CTS U1RTS U1RX U1TX BCLK1	- 0 - 0 0	ST — ST — ST	No No Yes Yes No	UART1 clear to send. UART1 ready to send. UART1 receive. UART1 transmit. UART1 IrDA baud clock output.

 Legend:
 CMOS = CMOS compatible input or output
 Analog = Analog input
 P = Power

 ST = Schmitt Trigger input with CMOS levels
 O = Output
 I = Input

 PPS = Peripheral Pin Select
 TTL = TTL input buffer

PPS = Peripheral Pin Select TTL = TTL input buffer

Note 1: This pin is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

2: This pin is available on dsPIC33EPXXXGP/MC50X devices only.

3: This is the default Fault on Reset for dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices. See Section 16.0 "High-Speed PWM Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)" for more information.

4: Not all pins are available in all packages variants. See the "Pin Diagrams" section for pin availability.

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name ⁽⁴⁾	Pin Type	Buffer Type	PPS	Description
U2CTS	1	ST	No	UART2 clear to send.
U2RTS	0	_	No	UART2 ready to send.
U2RX	ı	ST	Yes	UART2 receive.
U2TX	0	_	Yes	UART2 transmit.
BCLK2	0	ST	No	UART2 IrDA baud clock output.
SCK1	I/O	ST	No	Synchronous serial clock input/output for SPI1.
SDI1	I	ST	No	SPI1 data in.
SDO1	0	_	No	SPI1 data out.
SS1	I/O	ST	No	SPI1 slave synchronization or frame pulse I/O.
SCK2	I/O	ST	Yes	Synchronous serial clock input/output for SPI2.
SDI2	I	ST	Yes	SPI2 data in.
SDO2	0	_	Yes	SPI2 data out.
SS2	I/O	ST	Yes	SPI2 slave synchronization or frame pulse I/O.
SCL1	I/O	ST	No	Synchronous serial clock input/output for I2C1.
SDA1	I/O	ST	No	Synchronous serial data input/output for I2C1.
ASCL1	I/O	ST	No	Alternate synchronous serial clock input/output for I2C1.
ASDA1	I/O	ST	No	Alternate synchronous serial data input/output for I2C1.
SCL2	I/O	ST	No	Synchronous serial clock input/output for I2C2.
SDA2	I/O	ST	No	Synchronous serial data input/output for I2C2.
ASCL2	I/O	ST	No	Alternate synchronous serial clock input/output for I2C2.
ASDA2	I/O	ST	No	Alternate synchronous serial data input/output for I2C2.
TMS	I	ST	No	JTAG Test mode select pin.
TCK	I	ST	No	JTAG test clock input pin.
TDI	I	ST	No	JTAG test data input pin.
TDO	0	_	No	JTAG test data output pin.
C1RX ⁽²⁾	I	ST	Yes	ECAN1 bus receive pin.
C1TX ⁽²⁾	0		Yes	ECAN1 bus transmit pin.
FLT1 ⁽¹⁾ , FLT2 ⁽¹⁾	ı	ST	Yes	PWM Fault input 1 and 2.
FLT3 ⁽¹⁾ , FLT4 ⁽¹⁾	I	ST	No	PWM Fault input 3 and 4.
FLT32 ^(1,3)	I	ST	No	PWM Fault input 32 (Class B Fault).
DTCMP1-DTCMP3 ⁽¹⁾	I	ST	Yes	PWM Dead Time Compensation Input 1 through 3.
PWM1L-PWM3L ⁽¹⁾	0	_	No	PWM Low Output 1 through 3.
PWM1H-PWM3H ⁽¹⁾	0	_	No	PWM High Output 1 through 3.
SYNCI1 ⁽¹⁾	I	ST	Yes	PWM Synchronization Input 1.
SYNCO1 ⁽¹⁾	0		Yes	PWM Synchronization Output 1.
INDX1 ⁽¹⁾	I	ST	Yes	Quadrature Encoder Index1 Pulse input.
HOME1 ⁽¹⁾	I	ST	Yes	Quadrature Encoder Home1 Pulse input.
QEA1 ⁽¹⁾	I	ST	Yes	Quadrature Encoder Phase A input in QEI1 mode. Auxiliary Timer
(4)				External Clock/Gate input in Timer mode.
QEB1 ⁽¹⁾	I	ST	Yes	Quadrature Encoder Phase B input in QEI1 mode. Auxiliary Timer
CNTCMP1 ⁽¹⁾			Voo	External Clock/Gate input in Timer mode.
CIVI CIVIP IV.	0		Yes	Quadrature Encoder Compare Output 1.

Legend:CMOS = CMOS compatible input or outputAnalog = Analog inputP = PowerST = Schmitt Trigger input with CMOS levelsO = OutputI = InputPPS = Peripheral Pin SelectTTL = TTL input buffer

Note 1: This pin is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

- 2: This pin is available on dsPIC33EPXXXGP/MC50X devices only.
- 3: This is the default Fault on Reset for dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices. See Section 16.0 "High-Speed PWM Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)" for more information.
- 4: Not all pins are available in all packages variants. See the "Pin Diagrams" section for pin availability.

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

C1IN1- C1IN2-		Type		Description
CAINIO	ı	Analog	No	Op amp/Comparator 1 Negative Input 1.
	ı	Analog	No	Comparator 1 Negative Input 2.
C1IN1+	ı	Analog	No	Op amp/Comparator 1 Positive Input 1.
OA1OUT	0	Analog	No	Op amp 1 Output.
C1OUT	0	_	Yes	Comparator 1 Output.
C2IN1-	-	Analog	No	Op amp/Comparator 2 Negative Input 1.
C2IN2-	- 1	Analog	No	Comparator 2 Negative Input 2.
C2IN1+	ı	Analog	No	Op amp/Comparator 2 Positive Input 1.
OA2OUT	0	Analog	No	Op amp 2 Output.
C2OUT	0	_	Yes	Comparator 2 Output.
C3IN1-	I	Analog	No	Op amp/Comparator 3 Negative Input 1.
C3IN2-	- 1	Analog	No	Comparator 3 Negative Input 2.
C3IN1+	- 1	Analog	No	Op amp/Comparator 3 Positive Input 1.
OA3OUT	0	Analog	No	Op amp 3 Output.
C3OUT	0	_	Yes	Comparator 3 Output.
C4IN1-	ı	Analog	No	Comparator 4 Negative Input 1.
C4IN1+	ı	Analog	No	Comparator 4 Positive Input 1.
C4OUT	0	_	Yes	Comparator 4 Output.
CVREF10	0	Analog	No	Op amp/Comparator Voltage Reference Output.
CVREF2O	0	Analog	No	Op amp/Comparator Voltage Reference divided by 2 Output.
PGED1	I/O	ST	No	Data I/O pin for programming/debugging communication channel 1.
PGEC1	-1	ST	No	Clock input pin for programming/debugging communication channel 1.
PGED2	I/O	ST	No	Data I/O pin for programming/debugging communication channel 2.
PGEC2	ı	ST	No	Clock input pin for programming/debugging communication channel 2.
PGED3	I/O	ST	No	Data I/O pin for programming/debugging communication channel 3.
PGEC3	ı	ST	No	Clock input pin for programming/debugging communication channel 3.
MCLR	I/P	ST	No	Master Clear (Reset) input. This pin is an active-low Reset to the device.
AVDD	Р	Р	No	Positive supply for analog modules. This pin must be connected at all times.
AVss	Р	Р	No	Ground reference for analog modules. This pin must be connected at all times.
VDD	Р	_	No	Positive supply for peripheral logic and I/O pins.
VCAP	Р	_	No	CPU logic filter capacitor connection.
Vss	Р	_	No	Ground reference for logic and I/O pins.
VREF+	I	Analog	No	Analog voltage reference (high) input.
VREF-	ı	Analog	No	Analog voltage reference (low) input.

Legend:CMOS = CMOS compatible input or outputAnalog = Analog inputP = PowerST = Schmitt Trigger input with CMOS levelsO = OutputI = InputPPS = Peripheral Pin SelectTTL = TTL input buffer

Note 1: This pin is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

2: This pin is available on dsPIC33EPXXXGP/MC50X devices only.

3: This is the default Fault on Reset for dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices. See Section 16.0 "High-Speed PWM Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)" for more information.

4: Not all pins are available in all packages variants. See the "Pin Diagrams" section for pin availability.

2.0 GUIDELINES FOR GETTING STARTED WITH 16-BIT DIGITAL SIGNAL CONTROLLERS AND MICROCONTROLLERS

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the "dsPIC33E/PIC24E Family Reference Manual", which is available from the Microchip web site (www.microchip.com)
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

2.1 Basic Connection Requirements

Getting started with the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X families requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and Vss pins (see Section 2.2 "Decoupling Capacitors")
- All AVDD and AVss pins (regardless if ADC module is not used) (see Section 2.2 "Decoupling Capacitors")
- VCAP
 (see Section 2.3 "CPU Logic Filter Capacitor Connection (VCAP)")
- MCLR pin (see Section 2.4 "Master Clear (MCLR) Pin")
- PGECx/PGEDx pins used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes (see Section 2.5 "ICSP Pins")
- OSC1 and OSC2 pins when external oscillator source is used (see Section 2.6 "External Oscillator Pins")

Additionally, the following pins may be required:

 VREF+/VREF- pins are used when external voltage reference for ADC module is implemented

Note: The AVDD and AVSS pins must be connected independent of the ADC voltage reference source.

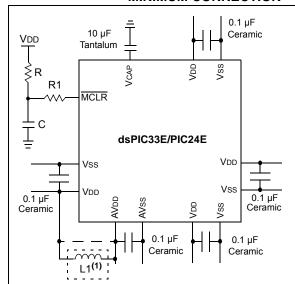
2.2 Decoupling Capacitors

The use of decoupling capacitors on every pair of power supply pins, such as VDD, VSS, AVDD and AVSS is required.

Consider the following criteria when using decoupling capacitors:

- Value and type of capacitor: Recommendation of 0.1 μF (100 nF), 10-20V. This capacitor should be a low-ESR and have resonance frequency in the range of 20 MHz and higher. It is recommended to use ceramic capacitors.
- Placement on the printed circuit board: The
 decoupling capacitors should be placed as close
 to the pins as possible. It is recommended to
 place the capacitors on the same side of the
 board as the device. If space is constricted, the
 capacitor can be placed on another layer on the
 PCB using a via; however, ensure that the trace
 length from the pin to the capacitor is within
 one-quarter inch (6 mm) in length.
- Handling high frequency noise: If the board is experiencing high frequency noise, above tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 μF to 0.001 μF. Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1 μF in parallel with 0.001 μF.
- Maximizing performance: On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB track inductance.

FIGURE 2-1: RECOMMENDED MINIMUM CONNECTION



Note 1: As an option, instead of a hard-wired connection, an inductor (L1) can be substituted between VDD and AVDD to improve ADC noise rejection. The inductor impedance should be less than 1Ω and the inductor capacity greater than 10 mA.

Where

$$f=rac{FCNV}{2}$$
 (i.e., ADC conversion rate/2)
$$f=rac{1}{(2\pi\sqrt{LC})}$$
 $L=\left(rac{1}{(2\pi f\sqrt{C})}
ight)^2$

2.2.1 TANK CAPACITORS

On boards with power traces running longer than six inches in length, it is suggested to use a tank capacitor for integrated circuits including DSCs to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device, and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 μF to 47 μF .

2.3 CPU Logic Filter Capacitor Connection (VCAP)

A low-ESR (< 1 Ohms) capacitor is required on the VCAP pin, which is used to stabilize the voltage regulator output voltage. The VCAP pin must not be connected to VDD, and must have a capacitor greater than 4.7 μ F (10 μ F is recommended), 16V connected to ground. The type can be ceramic or tantalum. See Section 30.0 "Electrical Characteristics" for additional information.

The placement of this capacitor should be close to the VCAP pin. It is recommended that the trace length not exceeds one-quarter inch (6 mm). See Section 27.3 "On-Chip Voltage Regulator" for details.

2.4 Master Clear (MCLR) Pin

The $\overline{\text{MCLR}}$ pin provides two specific device functions:

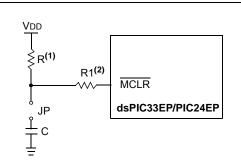
- · Device Reset
- · Device Programming and Debugging.

During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the $\overline{\text{MCLR}}$ pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as shown in Figure 2-2, it is recommended that the capacitor C, be isolated from the $\overline{\text{MCLR}}$ pin during programming and debugging operations.

Place the components as shown in Figure 2-2 within one-quarter inch (6 mm) from the $\overline{\text{MCLR}}$ pin.

FIGURE 2-2: EXAMPLE OF MCLR PIN CONNECTIONS



- Note 1: $R \le 10 \text{ k}\Omega$ is recommended. A suggested starting value is $10 \text{ k}\Omega$. Ensure that the MCLR pin VIH and VIL specifications are met.
 - 2: $R1 \le 470\Omega$ will limit any current flowing into \overline{MCLR} from the external capacitor C, in the event of \overline{MCLR} pin breakdown, due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS). Ensure that the \overline{MCLR} pin VIH and VIL specifications are met.

2.5 ICSP Pins

The PGECx and PGEDx pins are used for ICSP and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high (VIH) and input low (VIL) requirements.

Ensure that the "Communication Channel Select" (i.e., PGECx/PGEDx pins) programmed into the device matches the physical connections for the ICSP to MPLAB® PICkit™ 3, MPLAB ICD 3, or MPLAB REAL ICF™.

For more information on ICD 2, ICD 3 and REAL ICE connection requirements, refer to the following documents that are available on the Microchip web site

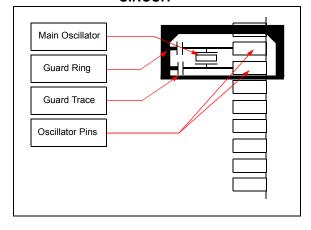
- "Using MPLAB® ICD 3" (poster) DS51765
- "MPLAB[®] ICD 3 Design Advisory" DS51764
- "MPLAB[®] REAL ICE™ In-Circuit Emulator User's Guide" DS51616
- "Using MPLAB[®] REAL ICE™ In-Circuit Emulator" (poster) DS51749

2.6 External Oscillator Pins

Many DSCs have options for at least two oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator. For details, see **Section 9.0** "Oscillator Configuration" for details.

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is shown in Figure 2-3.

FIGURE 2-3: SUGGESTED PLACEMENT
OF THE OSCILLATOR
CIRCUIT



2.7 Oscillator Value Conditions on Device Start-up

If the PLL of the target device is enabled and configured for the device start-up oscillator, the maximum oscillator source frequency must be limited to 3 MHz < FIN < 5.5 MHz to comply with device PLL start-up conditions. This means that if the external oscillator frequency is outside this range, the application must start-up in the FRC mode first. The default PLL settings after a POR with an oscillator frequency outside this range will violate the device operating speed.

Once the device powers up, the application firmware can initialize the PLL SFRs, CLKDIV and PLLDBF to a suitable value, and then perform a clock switch to the Oscillator + PLL clock source. Note that clock switching must be enabled in the device Configuration Word.

2.8 Unused I/Os

Unused I/O pins should be configured as outputs and driven to a logic-low state.

Alternatively, connect a 1k to 10k resistor between Vss and unused pins and drive the output to logic low.

2.9 Application Examples

- · Induction heating
- Uninterruptable Power Supplies (UPS)
- · DC/AC inverters
- · Compressor motor control
- · Washing machine 3-phase motor control
- · BLDC motor control
- · Automotive HVAC, cooling fans, fuel pumps
- · Stepper motor control
- · Audio and fluid sensor monitoring
- · Camera lens focus and stability control
- Speech (playback, hands-free kits, answering machines, VoIP)
- · Consumer audio
- Industrial and building control (security systems and access control)
- · Barcode reading
- Networking: LAN switches, gateways
- · Data storage device management
- · Smart cards and smart card readers

Examples of typical application connections are shown in Figure 2-4 through Figure 2-8.

FIGURE 2-4: BOOST CONVERTER IMPLEMENTATION

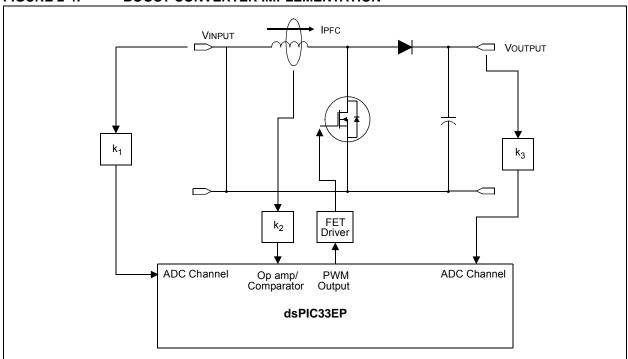


FIGURE 2-5: SINGLE-PHASE SYNCHRONOUS BUCK CONVERTER

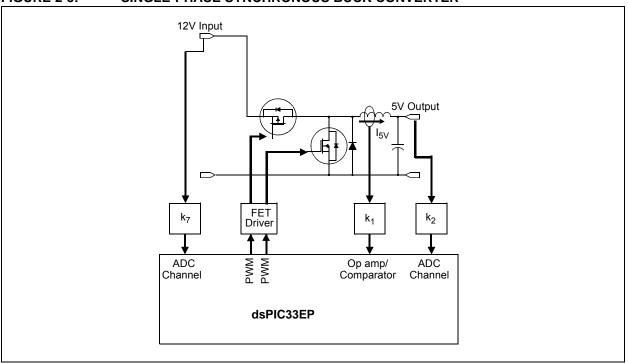
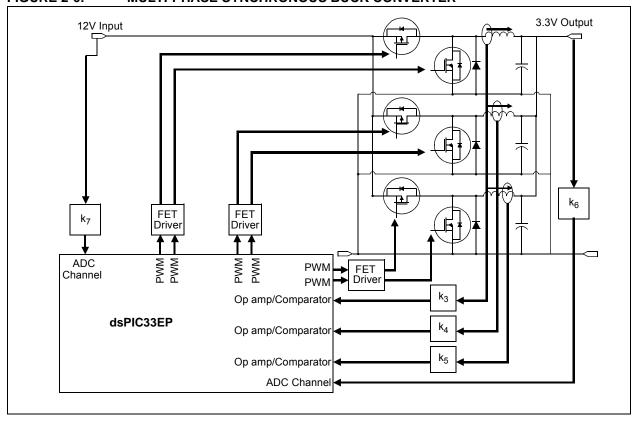


FIGURE 2-6: MULTI-PHASE SYNCHRONOUS BUCK CONVERTER



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FIGURE 2-7: INTERLEAVED PFC

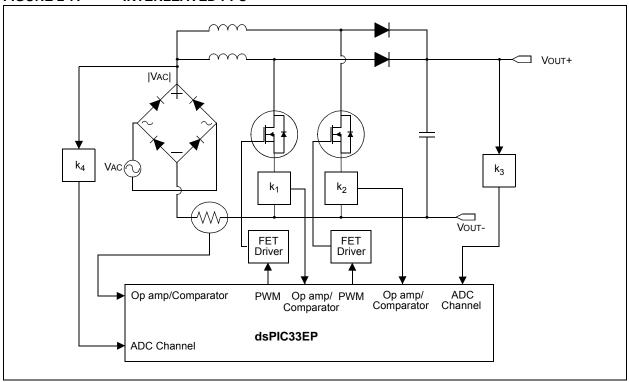
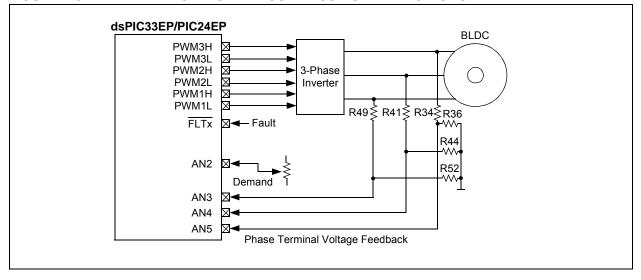


FIGURE 2-8: BEMF VOLTAGE MEASURED USING THE ADC MODULE



3.0 CPU

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 2. "CPU" (DS70359) in the "dsPIC33E/PIC24E Family Reference Manual", which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X CPU have a 16-bit (data) modified Harvard architecture with an enhanced instruction set, including significant support for digital signal processing. The CPU has a 24-bit instruction word, with a variable length opcode field. The Program Counter (PC) is 23 bits wide and addresses up to 4M x 24 bits of user program memory space.

An instruction prefetch mechanism helps maintain throughput and provides predictable execution. Most instructions execute in a single-cycle effective execution rate, with the exception of instructions that change the program flow, the double-word move (MOV.D) instruction, PSV accesses, and the table instructions. Overhead free program loop constructs are supported using the DO and REPEAT instructions, both of which are interruptible at any point.

3.1 Registers

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X devices have sixteen 16-bit Working registers in the programmer's model. Each of the Working registers can act as a data, address or address offset register. The 16th Working register (W15) operates as a software Stack Pointer for interrupts and calls.

3.2 Instruction Set

The instruction set for dsPIC33EPXXXGP50X and dsPIC33EPXXXMC20X/50X devices has two classes of instructions: the MCU class of instructions and the DSP class of instructions. The instruction set for PIC24EPXXXGP/MC20X devices has the MCU class of instructions only and does not support DSP instructions. These two instruction classes are seamlessly integrated into the architecture and execute from a single execution unit. The instruction set includes many addressing modes and was designed for optimum C compiler efficiency.

3.3 Data Space Addressing

The base data space can be addressed as 4K words or 8 Kbytes and is split into two blocks, referred to as X and Y data memory. Each memory block has its own independent Address Generation Unit (AGU). The MCU class of instructions operate solely through the X memory AGU, which accesses the entire memory map as one linear data space. On dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices, certain DSP instructions operate through the X and Y AGUs to support dual operand reads, which splits the data address space into two parts. The X and Y data space boundary is device specific.

The upper 4 Kbytes of the data space memory map can optionally be mapped into program space at any 16K program word boundary. The program-to-data-space mapping feature, known as Program Space Visibility (PSV), lets any instruction access program space as if it were data space. Moreover, the Base Data Space address is used in conjunction with a read or write page register (DSRPAG or DSWPAG) to form an Extended Data Space (EDS) address. The EDS can be addressed as 8 Mwords or 16 Mbytes. Refer to Section 3. "Data Memory" (DS70595) and Section 4. "Program Memory" (DS70613) in the "dsPIC33E/PIC24E Family Reference Manual" for more details on EDS, PSV and table accesses.

On dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices, overhead-free circular buffers (Modulo Addressing) are supported in both X and Y address spaces. The Modulo Addressing removes the software boundary-checking overhead for DSP algorithms. The X AGU circular addressing can be used with any of the MCU class of instructions. The X AGU also supports Bit-Reverse Addressing to greatly simplify input or output data reordering for radix-2 FFT algorithms. PIC24EPXXXGP/MC20X devices do not support Modulo and Bit-Reverse Addressing.

3.4 Addressing Modes

The CPU supports these addressing modes:

- · Inherent (no operand)
- Relative
- Literal
- · Memory Direct
- · Register Direct
- · Register Indirect

Each instruction is associated with a predefined Addressing mode group, depending upon its functional requirements. As many as six Addressing modes are supported for each instruction.

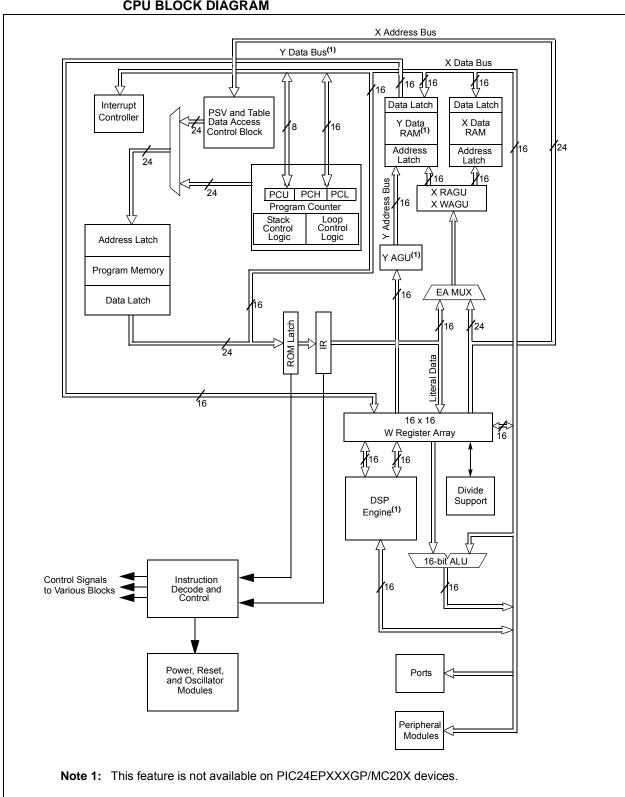


FIGURE 3-1: dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, AND PIC24EPXXXGP/MC20X CPU BLOCK DIAGRAM

3.5 Programmer's Model

The programmer's model for the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X is shown in Figure 3-2. All registers in the programmer's model are memory mapped and can be manipulated directly by instructions. Table 3-1 lists a description of each register.

In addition to the registers contained in the programmer's model, the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X devices contain control registers for Modulo Addressing (dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only), Bit-Reversed Addressing (dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only) and interrupts. These registers are described in subsequent sections of this document.

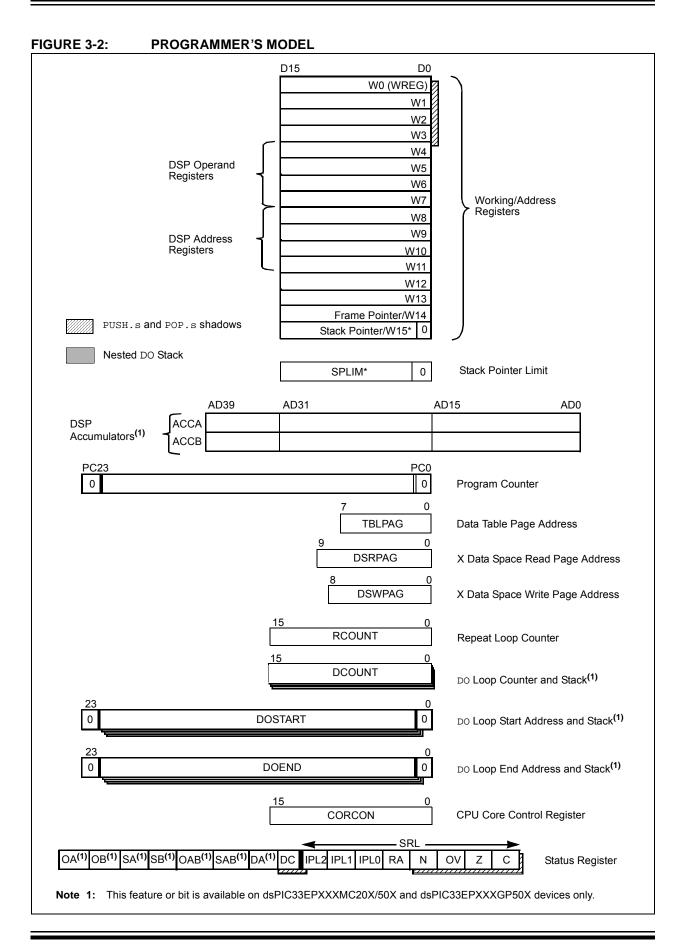
All registers associated with the programmer's model are memory mapped, as shown in Table 4-1.

TABLE 3-1: PROGRAMMER'S MODEL REGISTER DESCRIPTIONS

Description
Working register array
40-bit DSP Accumulators
23-bit Program Counter
ALU and DSP Engine Status register
Stack Pointer Limit Value register
Table Memory Page Address register
Extended Data Space (EDS) Read Page register
Extended Data Space (EDS) Write Page register
REPEAT Loop Count register
DO Loop Count register
DO Loop Start Address register (High and Low)
DO Loop End Address register (High and Low)
Contains DSP Engine, DO Loop control and trap status bits

Note 1: This register is available on dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only.

2: The DOSTARTH and DOSTARTL registers are read-only.



3.6 CPU Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:

In the event you are not able to access the product page using the link above, enter this URL in your browser:

http://www.microchip.com/wwwproducts/ Devices.aspx?dDocName=en555464

3.6.1 KEY RESOURCES

- Section 2. "CPU" (DS70359)
- · Code Samples
- · Application Notes
- · Software Libraries
- Webinars
- All related dsPIC33E/PIC24E Family Reference Manuals Sections
- · Development Tools

3.7 **CPU Control Registers**

REGISTER 3-1: SR: CPU STATUS REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/C-0	R/C-0	R -0	R/W-0
OA ⁽¹⁾	OB ⁽¹⁾	SA ^(1,4)	SB ^(1,4)	OAB ⁽¹⁾	SAB ⁽¹⁾	DA ⁽¹⁾	DC
bit 15							bit 8

R/W-0 ^(2,3)	R/W-0 ^(2,3)	R/W-0 ^(2,3)	R-0	R/W-0	R/W-0	R/W-0	R/W-0
	IPL<2:0>		RA	N	OV	Z	С
bit 7							bit 0

Legend:		U = Unimplemented bit, read	as '0'
R = Readable bit	W = Writable bit	C = Clearable bit	
-n = Value at POR	'1'= Bit is set	'0' = Bit is cleared	x = Bit is unknown

OA: Accumulator A Overflow Status bit(1) bit 15 1 = Accumulator A has overflowed 0 = Accumulator A has not overflowed **OB:** Accumulator B Overflow Status bit⁽¹⁾ bit 14 1 = Accumulator B has overflowed 0 = Accumulator B has not overflowed SA: Accumulator A Saturation 'Sticky' Status bit (1,4) bit 13 1 = Accumulator A is saturated or has been saturated at some time 0 = Accumulator A is not saturated bit 12 SB: Accumulator B Saturation 'Sticky' Status bit (1,4) 1 = Accumulator B is saturated or has been saturated at some time

0 = Accumulator B is not saturated

OAB: OA || OB Combined Accumulator Overflow Status bit(1) bit 11

1 = Accumulators A or B have overflowed

0 = Neither Accumulators A or B have overflowed

SAB: SA | SB Combined Accumulator 'Sticky' Status bit (1) bit 10

1 = Accumulators A or B are saturated or have been saturated at some time

0 = Neither Accumulator A or B are saturated

DA: DO Loop Active bit⁽¹⁾ bit 9 1 = DO loop in progress

0 = DO loop not in progress

DC: MCU ALU Half Carry/Borrow bit bit 8

> 1 = A carry-out from the 4th low order bit (for byte-sized data) or 8th low order bit (for word-sized data) of the result occurred

> 0 = No carry-out from the 4th low order bit (for byte-sized data) or 8th low order bit (for word-sized data) of the result occurred

Note 1: This bit is available on dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only.

2: The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL, if IPL<3> = 1. User interrupts are disabled when IPL<3> = 1.

3: The IPL<2:0> Status bits are read only when the NSTDIS bit (INTCON1<15>) = 1.

4: A data write to the SR register can modify the SA and SB bits by either a data write to SA and SB or by clearing the SAB bit. To avoid a possible SA or SB bit write race condition, the SA and SB bits should not be modified using bit operations.

REGISTER 3-1: SR: CPU STATUS REGISTER (CONTINUED)

IPL<2:0>: CPU Interrupt Priority Level Status bits(1,2) bit 7-5 111 = CPU Interrupt Priority Level is 7 (15). User interrupts disabled 110 = CPU Interrupt Priority Level is 6 (14) 101 = CPU Interrupt Priority Level is 5 (13) 100 = CPU Interrupt Priority Level is 4 (12) 011 = CPU Interrupt Priority Level is 3 (11) 010 = CPU Interrupt Priority Level is 2 (10) 001 = CPU Interrupt Priority Level is 1 (9) 000 = CPU Interrupt Priority Level is 0 (8) bit 4 RA: REPEAT Loop Active bit 1 = REPEAT loop in progress 0 = REPEAT loop not in progress N: MCU ALU Negative bit bit 3 1 = Result was negative 0 = Result was non-negative (zero or positive) bit 2 OV: MCU ALU Overflow bit This bit is used for signed arithmetic (2's complement). It indicates an overflow of the magnitude that causes the sign bit to change state. 1 = Overflow occurred for signed arithmetic (in this arithmetic operation) 0 = No overflow occurred Z: MCU ALU Zero bit bit 1 1 = An operation that affects the Z bit has set it at some time in the past 0 = The most recent operation that affects the Z bit has cleared it (i.e., a non-zero result)

1 = A carry-out from the Most Significant bit of the result occurred

C: MCU ALU Carry/Borrow bit

bit 0

- 0 = No carry-out from the Most Significant bit of the result occurred
- Note 1: This bit is available on dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only.
 - The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL, if IPL<3> = 1. User interrupts are disabled when IPL<3> = 1.
 - 3: The IPL<2:0> Status bits are read only when the NSTDIS bit (INTCON1<15>) = 1.
 - A data write to the SR register can modify the SA and SB bits by either a data write to SA and SB or by clearing the SAB bit. To avoid a possible SA or SB bit write race condition, the SA and SB bits should not be modified using bit operations.

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REGISTER 3-2: CORCON: CORE CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0
VAR	_	US<1	:0> ⁽¹⁾	EDT ^(1,2)		DL<2:0> ⁽¹⁾	
bit 15							bit 8

R/W-0	R/W-0	R/W-1	R/W-0	R/C-0	R-0	R/W-0	R/W-0
SATA ⁽¹⁾	SATB ⁽¹⁾	SATDW ⁽¹⁾	ACCSAT ⁽¹⁾	IPL3 ⁽³⁾	SFA	RND ⁽¹⁾	IF ⁽¹⁾
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15 VAR: Variable Exception Processing Latency Control bit

1 = Variable exception processing enabled 0 = Fixed exception processing enabled

bit 14 **Unimplemented:** Read as '0'

bit 13-12 US<1:0>: DSP Multiply Unsigned/Signed Control bits⁽¹⁾

11 = Reserved

10 = DSP engine multiplies are mixed-sign

01 = DSP engine multiplies are unsigned

00 = DSP engine multiplies are signed

bit 11 EDT: Early DO Loop Termination Control bit (1,2)

1 = Terminate executing DO loop at end of current loop iteration

0 = No effect

bit 10-8 **DL<2:0>**: DO Loop Nesting Level Status bits⁽¹⁾

111 = 7 DO loops active

•

.

001 = 1 DO loop active

000 = 0 DO loops active

bit 7 SATA: ACCA Saturation Enable bit(1)

1 = Accumulator A saturation enabled

0 = Accumulator A saturation disabled

bit 6 SATB: ACCB Saturation Enable bit⁽¹⁾

1 = Accumulator B saturation enabled

0 = Accumulator B saturation disabled

bit 5 SATDW: Data Space Write from DSP Engine Saturation Enable bit⁽¹⁾

1 = Data space write saturation enabled

0 = Data space write saturation disabled

bit 4 ACCSAT: Accumulator Saturation Mode Select bit⁽¹⁾

1 = 9.31 saturation (super saturation)

0 = 1.31 saturation (normal saturation)

bit 3 **IPL3:** CPU Interrupt Priority Level Status bit 3⁽³⁾

1 = CPU interrupt priority level is greater than 7

0 = CPU interrupt priority level is 7 or less

Note 1: This bit is available on dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only.

This bit is always read as '0'.

3: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU interrupt priority level.

REGISTER 3-2: CORCON: CORE CONTROL REGISTER (CONTINUED)

bit 2 SFA: Stack Frame Active Status bit

1 = Stack frame is active. W14 and W15 address 0x0000 to 0xFFFF, regardless of DSRPAG and DSW-PAG values

0 = Stack frame is not active. W14 and W15 address of EDS or Base Data Space

bit 1 RND: Rounding Mode Select bit⁽¹⁾

1 = Biased (conventional) rounding enabled0 = Unbiased (convergent) rounding enabled

bit 0 IF: Integer or Fractional Multiplier Mode Select bit⁽¹⁾

1 = Integer mode enabled for DSP multiply0 = Fractional mode enabled for DSP multiply

Note 1: This bit is available on dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only.

2: This bit is always read as '0'.

3: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU interrupt priority level.

3.8 Arithmetic Logic Unit (ALU)

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X ALU is 16 bits wide and is capable of addition, subtraction, bit shifts and logic operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. Depending on the operation, the ALU can affect the values of the Carry (C), Zero (Z), Negative (N), Overflow (OV) and Digit Carry (DC) Status bits in the SR register. The C and DC Status bits operate as Borrow and Digit Borrow bits, respectively, for subtraction operations.

The ALU can perform 8-bit or 16-bit operations, depending on the mode of the instruction that is used. Data for the ALU operation can come from the W register array or data memory, depending on the addressing mode of the instruction. Likewise, output data from the ALU can be written to the W register array or a data memory location.

Refer to the "16-bit MCU and DSC Programmer's Reference Manual" (DS70157) for information on the SR bits affected by each instruction.

The core CPU incorporates hardware support for both multiplication and division. This includes a dedicated hardware multiplier and support hardware for 16-bit divisor division.

3.8.1 MULTIPLIER

Using the high-speed 17-bit x 17-bit multiplier, the ALU supports unsigned, signed, or mixed-sign operation in several MCU multiplication modes:

- 16-bit x 16-bit signed
- 16-bit x 16-bit unsigned
- 16-bit signed x 5-bit (literal) unsigned
- 16-bit signed x 16-bit unsigned
- · 16-bit unsigned x 5-bit (literal) unsigned
- 16-bit unsigned x 16-bit signed
- · 8-bit unsigned x 8-bit unsigned

3.8.2 DIVIDER

The divide block supports 32-bit/16-bit and 16-bit/16-bit signed and unsigned integer divide operations with the following data sizes:

- · 32-bit signed/16-bit signed divide
- · 32-bit unsigned/16-bit unsigned divide
- · 16-bit signed/16-bit signed divide
- 16-bit unsigned/16-bit unsigned divide

The quotient for all divide instructions ends up in W0 and the remainder in W1. 16-bit signed and unsigned DIV instructions can specify any W register for both the 16-bit divisor (Wn) and any W register (aligned) pair (W(m + 1):Wm) for the 32-bit dividend. The divide algorithm takes one cycle per bit of divisor, so both 32-bit/16-bit and 16-bit/16-bit instructions take the same number of cycles to execute.

3.9 DSP Engine (dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X Devices Only)

The DSP engine consists of a high-speed 17-bit x 17-bit multiplier, a 40-bit barrel shifter and a 40-bit adder/subtracter (with two target accumulators, round and saturation logic).

The DSP engine can also perform inherent accumulator-to-accumulator operations that require no additional data. These instructions are ADD, SUB and NEG.

The DSP engine has options selected through bits in the CPU Core Control register (CORCON), as listed below:

- Fractional or integer DSP multiply (IF)
- Signed, unsigned, or mixed-sign DSP multiply (US)
- Conventional or convergent rounding (RND)
- · Automatic saturation on/off for ACCA (SATA)
- · Automatic saturation on/off for ACCB (SATB)
- Automatic saturation on/off for writes to data memory (SATDW)
- Accumulator Saturation mode selection (ACCSAT)

TABLE 3-2: DSP INSTRUCTIONS SUMMARY

Instruction	Algebraic Operation	ACC Write Back
CLR	A = 0	Yes
ED	$A = (x - y)^2$	No
EDAC	$A = A + (x - y)^2$	No
MAC	$A = A + (x \bullet y)$	Yes
MAC	$A = A + x^2$	No
MOVSAC	No change in A	Yes
MPY	$A = x \cdot y$	No
MPY	$A = x^2$	No
MPY.N	$A = -x \bullet y$	No
MSC	$A = A - x \bullet y$	Yes

4.0 MEMORY ORGANIZATION

Note:

This data sheet summarizes the features dsPIC33EPXXXGP50X. of the dsPIC33EPXXXMC20X/50X. and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to 4. "Program Memory" Section (DS70613) of the "dsPIC33E/PIC24E Family Reference Manual', which is available from the Microchip web site (www.microchip.com).

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X architecture features separate program and data memory spaces and buses. This architecture also allows the direct access of program memory from the data space during code execution.

4.1 Program Address Space

The program address memory space of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X devices is 4M instructions. The space is addressable by a 24-bit value derived either from the 23-bit PC during program execution, or from table operation or data space remapping as described in Section 4.8 "Interfacing Program and Data Memory Spaces".

User application access to the program memory space is restricted to the lower half of the address range (0x0000000 to 0x7FFFFF). The exception is the use of TBLRD operations, which use TBLPAG<7> to read Device ID sections of the configuration memory space.

The program memory maps, which are presented by device family and memory size, are shown in Figure 4-1 through Figure 4-4.

FIGURE 4-1: PROGRAM MEMORY MAP FOR dsPIC33EP32GP50X, dsPIC33EP32MC20X/50X, AND PIC24EP32GP/MC20X DEVICES⁽¹⁾

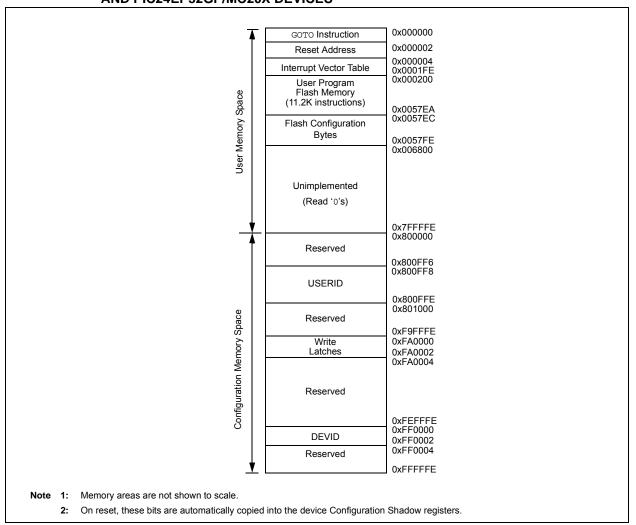


FIGURE 4-2: PROGRAM MEMORY MAP FOR dsPIC33EP64GP50X, dsPIC33EP64MC20X/50X, AND PIC24EP64GP/MC20X DEVICES⁽¹⁾

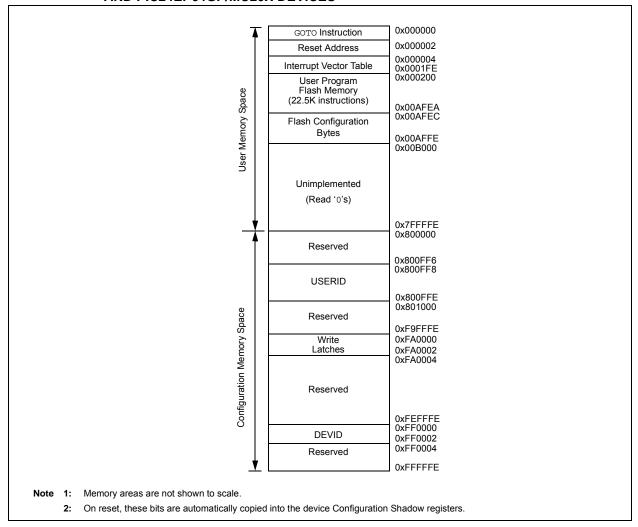


FIGURE 4-3: PROGRAM MEMORY MAP FOR dsPIC33EP128GP50X, dsPIC33EP128MC20X/50X, AND PIC24EP128GP/MC20X DEVICES⁽¹⁾

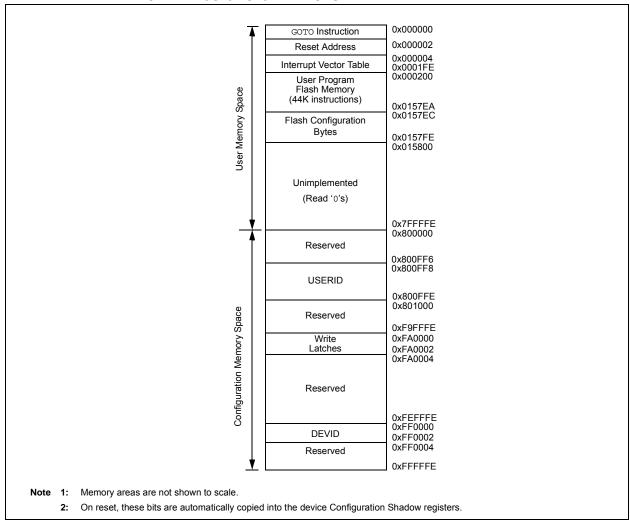
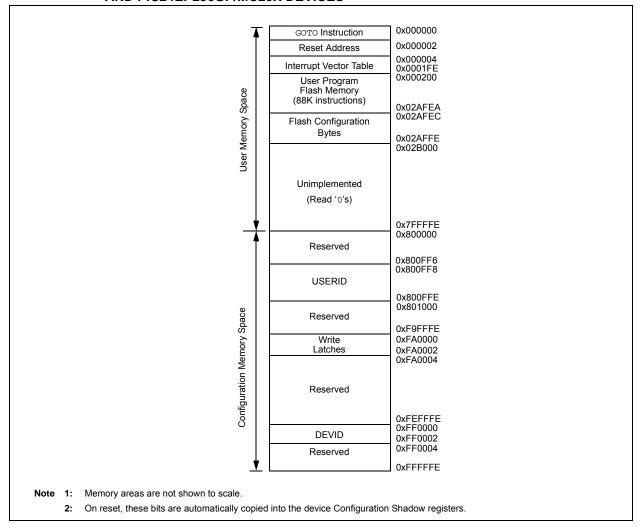


FIGURE 4-4: PROGRAM MEMORY MAP FOR dsPIC33EP256GP50X, dsPIC33EP256MC20X/50X, AND PIC24EP256GP/MC20X DEVICES⁽¹⁾



4.1.1 PROGRAM MEMORY ORGANIZATION

The program memory space is organized in word-addressable blocks. Although it is treated as 24 bits wide, it is more appropriate to think of each address of the program memory as a lower and upper word, with the upper byte of the upper word being unimplemented. The lower word always has an even address, while the upper word has an odd address (Figure 4-5).

Program memory addresses are always word-aligned on the lower word, and addresses are incremented or decremented by two during code execution. This arrangement provides compatibility with data memory space addressing and makes data in the program memory space accessible.

4.1.2 INTERRUPT AND TRAP VECTORS

All dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X devices reserve the addresses between 0x00000 and 0x000200 for hard-coded program execution vectors. A hardware Reset vector is provided to redirect code execution from the default value of the PC on device Reset to the actual start of code. A GOTO instruction is programmed by the user application at address 0x000000 of Flash memory, with the actual address for the start of code at address 0x0000002 of Flash memory.

A more detailed discussion of the interrupt vector tables is provided in **Section 7.1** "Interrupt Vector Table".

FIGURE 4-5: PROGRAM MEMORY ORGANIZATION

msw	most significant wo	rd l	east significant wor	
Address				(Isw Address)
	23	16	88	<u> </u>
0x000001	0000000			0x000000
0x000003	0000000			0x000002
0x000005	00000000			0x000004
0x000007	00000000			0x000006
		<u>.</u>	·	
	Program Memory 'Phantom' Byte (read as '0')	Instruc	tion Width	

4.2 Data Address Space

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X CPU has a separate 16-bit wide data memory space. The data space is accessed using separate Address Generation Units (AGUs) for read and write operations. The data memory maps, which are presented by device family and memory size, are shown in Figure 4-6 through Figure 4-13.

All Effective Addresses (EAs) in the data memory space are 16 bits wide and point to bytes within the data space. This arrangement gives a base data space address range of 8 Kbytes or 4K words.

The base data space address is used in conjunction with a read or write page register (DSRPAG or DSWPAG) to form an extended data space, which has a total address range of 16 MB.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X devices implement up to 56 Kbytes of data memory. If an EA point to a location outside of this area, an all-zero word or byte is returned.

4.2.1 DATA SPACE WIDTH

The data memory space is organized in byte addressable, 16-bit wide blocks. Data is aligned in data memory and registers as 16-bit words, but all data space EAs resolve to bytes. The Least Significant Bytes (LSBs) of each word have even addresses, while the Most Significant Bytes (MSBs) have odd addresses.

4.2.2 DATA MEMORY ORGANIZATION AND ALIGNMENT

To maintain backward compatibility with PIC® MCU devices and improve data space memory usage efficiency, the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X instruction set supports both word and byte operations. As a consequence of byte accessibility, all effective address calculations are internally scaled to step through word-aligned memory. For example, the core recognizes that Post-Modified Register Indirect Addressing mode [Ws++] results in a value of Ws + 1 for byte operations and Ws + 2 for word operations.

A data byte read, reads the complete word that contains the byte, using the LSb of any EA to determine which byte to select. The selected byte is placed onto the LSB of the data path. That is, data memory and registers are organized as two parallel byte-wide entities with shared (word) address decode but separate write lines. Data byte writes only write to the corresponding side of the array or register that matches the byte address.

All word accesses must be aligned to an even address. Misaligned word data fetches are not supported, so care must be taken when mixing byte and word operations, or translating from 8-bit MCU code. If a misaligned read or write is attempted, an address error trap is generated. If the error occurred on a read, the instruction underway is completed. If the error occurred on a write, the instruction is executed but the write does not occur. In either case, a trap is then executed, allowing the system and/or user application to examine the machine state prior to execution of the address Fault.

All byte loads into any W register are loaded into the LSB. The MSB is not modified.

A Sign-Extend instruction (SE) is provided to allow user applications to translate 8-bit signed data to 16-bit signed values. Alternatively, for 16-bit unsigned data, user applications can clear the MSB of any W register by executing a Zero-Extend (ZE) instruction on the appropriate address.

4.2.3 SFR SPACE

The first 4 Kbytes of the Near Data Space, from 0x0000 to 0x0FFF, is primarily occupied by Special Function Registers (SFRs). These are used by the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X core and peripheral modules for controlling the operation of the device.

SFRs are distributed among the modules that they control, and are generally grouped together by module. Much of the SFR space contains unused addresses; these are read as '0'.

Note: The actual set of peripheral features and interrupts varies by the device. Refer to the corresponding device tables and pinout diagrams for device-specific information.

4.2.4 NEAR DATA SPACE

The 8 Kbyte area between 0x0000 and 0x1FFF is referred to as the near data space. Locations in this space are directly addressable through a 13-bit absolute address field within all memory direct instructions. Additionally, the whole data space is addressable using MoV instructions, which support Memory Direct Addressing mode with a 16-bit address field, or by using Indirect Addressing mode using a working register as an Address Pointer.

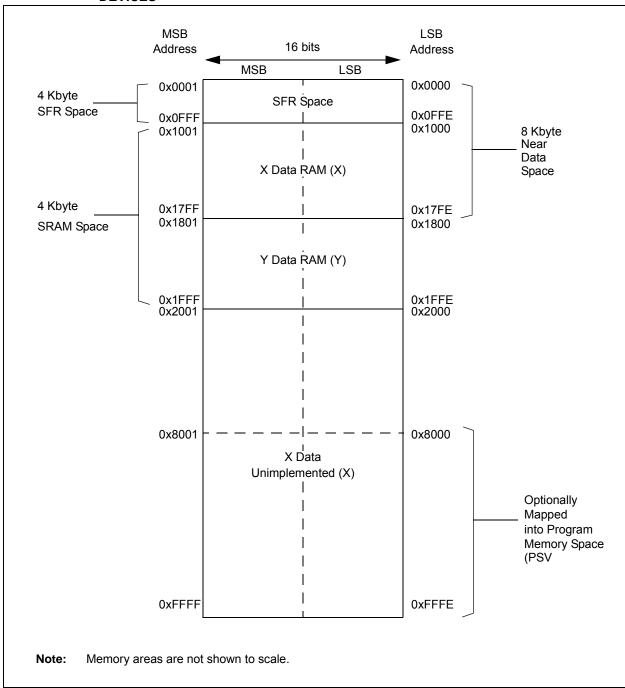


FIGURE 4-6: DATA MEMORY MAP FOR dsPIC33EP32MC20X/50X AND dsPIC33EP32GP50X DEVICES

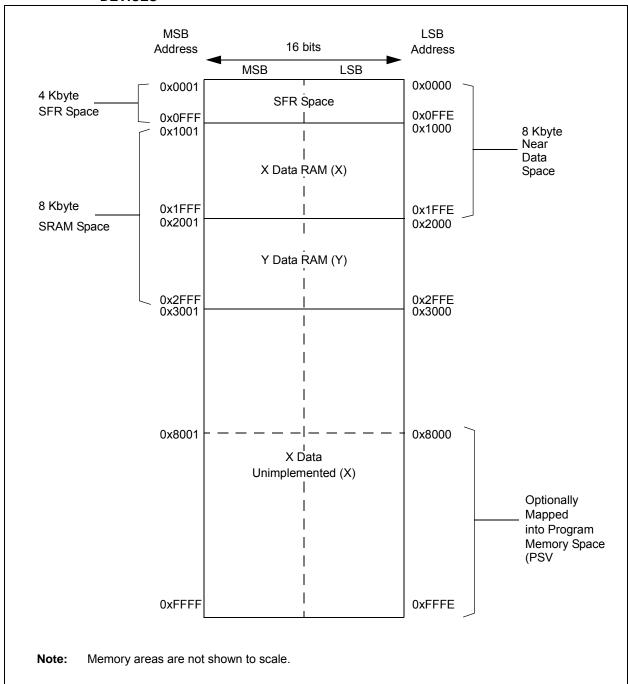


FIGURE 4-7: DATA MEMORY MAP FOR dsPIC33EP64MC20X/50X AND dsPIC33EP64GP50X DEVICES

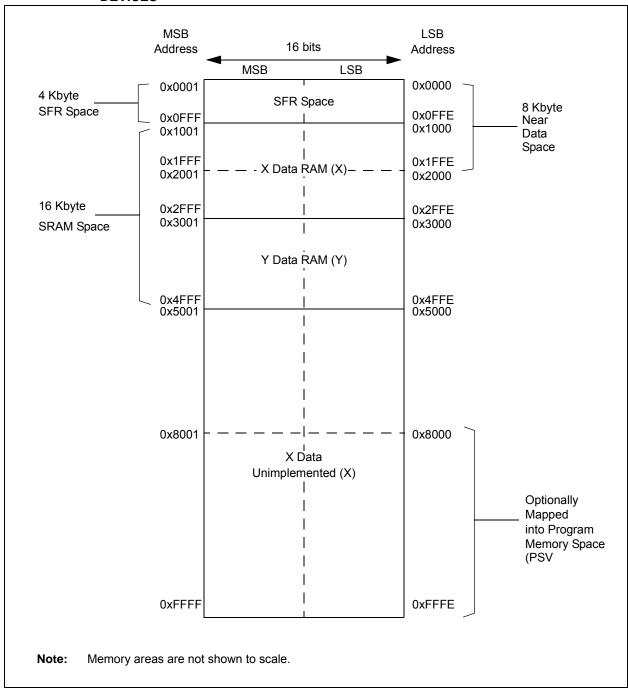


FIGURE 4-8: DATA MEMORY MAP FOR dsPIC33EP128MC20X/50X AND dsPIC33EP128GP50X DEVICES

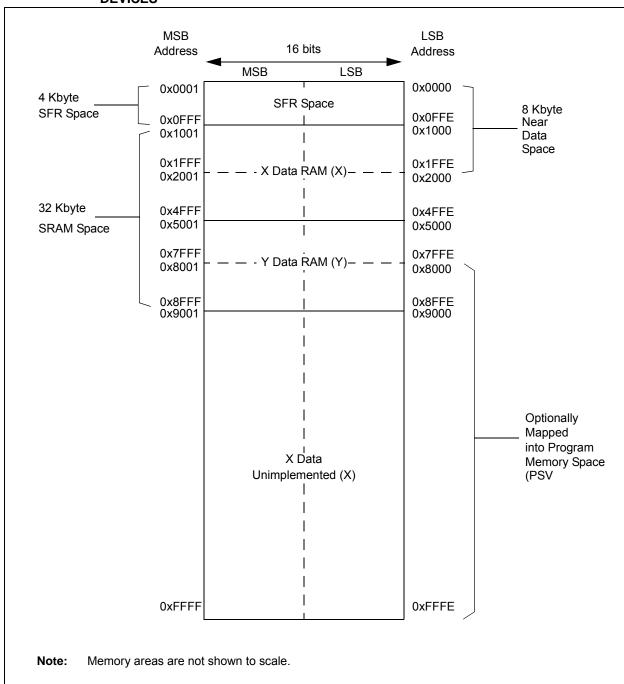


FIGURE 4-9: DATA MEMORY MAP FOR dsPIC33EP256MC20X/50X AND dsPIC33EP256GP50X DEVICES

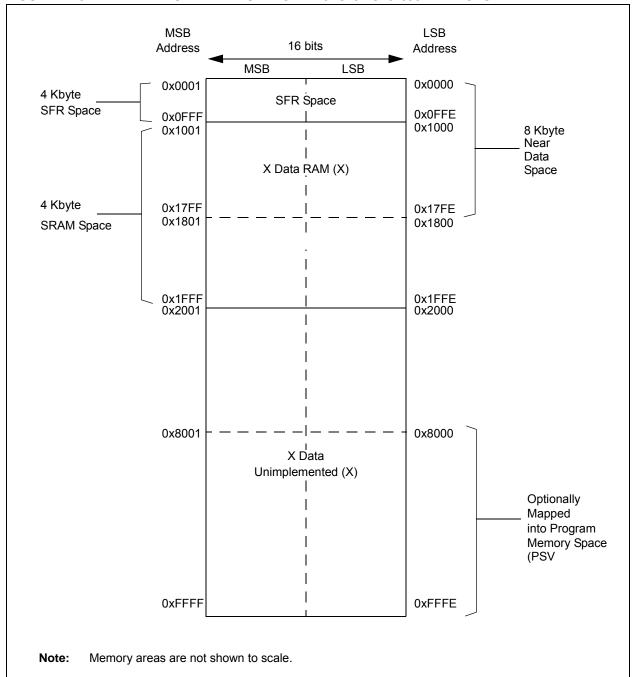


FIGURE 4-10: DATA MEMORY MAP FOR PIC24EP32GP/MC20X/50X DEVICES

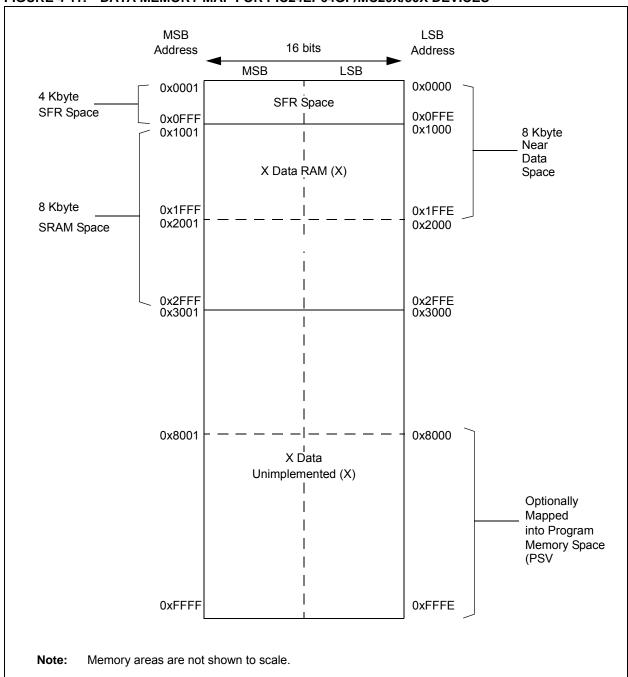


FIGURE 4-11: DATA MEMORY MAP FOR PIC24EP64GP/MC20X/50X DEVICES

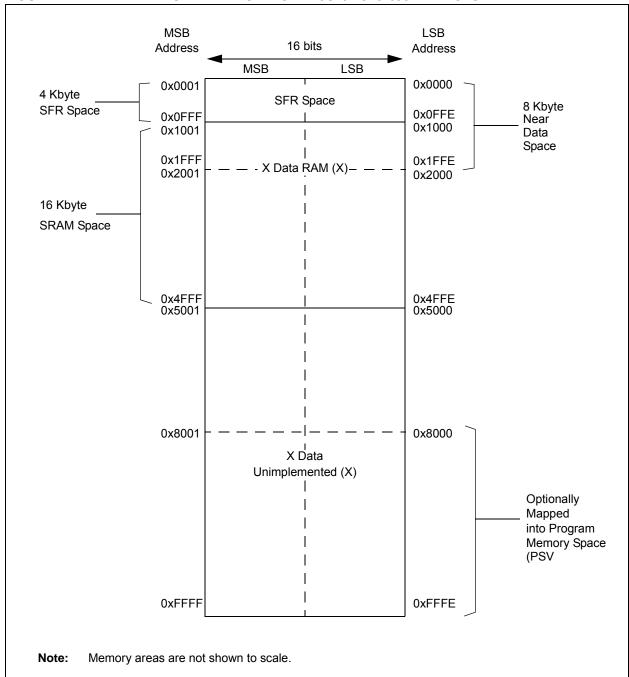


FIGURE 4-12: DATA MEMORY MAP FOR PIC24128GP/MC20X/50X DEVICES

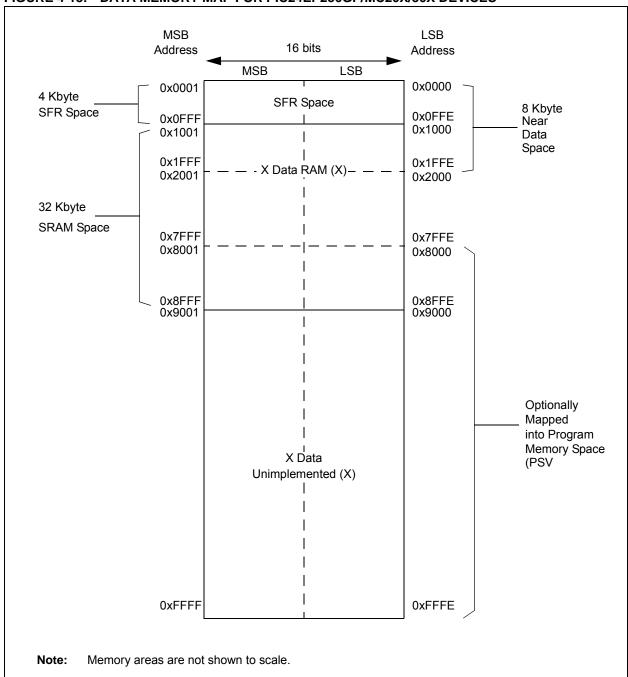


FIGURE 4-13: DATA MEMORY MAP FOR PIC24EP256GP/MC20X/50X DEVICES

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4.2.5 X AND Y DATA SPACES

The dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X core has two data spaces, X and Y. These data spaces can be considered either separate (for some DSP instructions), or as one unified linear address range (for MCU instructions). The data spaces are accessed using two Address Generation Units (AGUs) and separate data paths. This feature allows certain instructions to concurrently fetch two words from RAM, thereby enabling efficient execution of DSP algorithms such as Finite Impulse Response (FIR) filtering and Fast Fourier Transform (FFT).

The X data space is used by all instructions and supports all addressing modes. X data space has separate read and write data buses. The X read data bus is the read data path for all instructions that view data space as combined X and Y address space. It is also the X data prefetch path for the dual operand DSP instructions (MAC class).

The Y data space is used in concert with the X data space by the MAC class of instructions (CLR, ED, EDAC, MAC, MOVSAC, MPY, MPY.N and MSC) to provide two concurrent data read paths.

Both the X and Y data spaces support Modulo Addressing mode for all instructions, subject to addressing mode restrictions. Bit-Reversed Addressing mode is only supported for writes to X data space. Modulo Addressing and Bit-Reversed Addressing are not present in PIC24EPXXXGP/MC20X devices.

All data memory writes, including in DSP instructions, view data space as combined X and Y address space. The boundary between the X and Y data spaces is device-dependent and is not user-programmable.

4.3 Memory Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:

In the event you are not able to access the product page using the link above, enter this URL in your browser:

http://www.microchip.com/wwwproducts/ Devices.aspx?dDocName=en555464

4.3.1 KEY RESOURCES

- Section 4. "Program Memory" (DS70613)
- · Code Samples
- · Application Notes
- · Software Libraries
- Webinars
- All related dsPIC33E/PIC24E Family Reference Manuals Sections
- · Development Tools

4.4 Special Function Register Maps

TABLE 4-1: CPU CORE REGISTER MAP FOR dsPIC33EPXXXMC20X/50X AND dsPIC33EPXXXGP50X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	AII Resets
W0	0000								W0 (WF	EG)								xxxx
W1	0002								W1									xxxx
W2	0004								W2									xxxx
W3	0006								W3									xxxx
W4	8000								W4									xxxx
W5	000A								W5									xxxx
W6	000C								W6									xxxx
W7	000E								W7									xxxx
W8	0010								W8									xxxx
W9	0012								W9									xxxx
W10	0014								W10)								xxxx
W11	0016		W11 W12															xxxx
W12	0018																	xxxx
W13	001A		W13															xxxx
W14	001C		W14															xxxx
W15	001E								W15	5								xxxx
SPLIM	0020								SPLI	М								0000
ACCAL	0022								ACCA	NL								0000
ACCAH	0024								ACCA	Н								0000
ACCAU	0026			Si	gn-extensio	n of ACCA<	39>						AC	CAU				0000
ACCBL	0028								ACCE	BL								0000
ACCBH	002A								ACCE	BH								0000
ACCBU	002C			Si	gn-extensio	n of ACCB<	39>						AC	CBU				0000
PCL	002E								PCL								_	0000
PCH	0030	_	_	_	_	_	_	_	_	_				PCH				0000
DSRPAG	0032	_	_	_	_	_	_					DSRF	PAG					0001
DSWPAG	0034		_	_	_	_	_	_					DSWPAG					0001
RCOUNT	0036								RCOU	NT								0000
DCOUNT	0038								DCOU	NT								0000
DOSTARTL	003A							D	OSTARTL								_	0000
DOSTARTH	003C	_	_	_	_	_	_	_	_	_	_			DOS	TARTH			0000
DOENDL	003E								DOENDL					·			_	0000
DOENDH	0040	_	_	_	_	_	_	_	_	_	_			DO	ENDH			0000

TABLE 4-1: CPU CORE REGISTER MAP FOR dsPIC33EPXXXMC20X/50X AND dsPIC33EPXXXGP50X DEVICES ONLY (CONTINUED)

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
SR	0042	OA	ОВ	SA	SB	OAB	SAB	DA	DC	IPL2	IPL1	IPL0	RA	N	OV	Z	С	0000	
CORCON	0044	VAR	_	US<	1:0>	EDT		DL<2:0>		SATA	SATB	SATDW	ACCSAT	IPL3	SFA	RND	IF	0020	
MODCON	0046	XMODEN	YMODEN	-	-	BWM<3:0> YWM<3:0> XWM<3:0>												0000	
XMODSRT	0048					XMODSRT<15:0>													
XMODEND	004A					XMODER1<15:0> XMODEND<15:0>													
YMODSRT	004C							YMO	DSRT<15:0	>							_	0000	
YMODEND	004E							YMO	DEND<15:0	>							_	0001	
XBREV	0050	BREN							XBF	REV<14:0>								0000	
DISICNT	0052	_	_							DISICNT<	13:0>							0000	
TBLPAG	0054	_	_		-			_	I			•	TBLPA	G<7:0>	•			0000	
MSTRPR	0058			•	•	•			MSTRPR<	15:0>		•			•			0000	

TABLE 4-2: CPU CORE REGISTER MAP FOR PIC24EPXXXGP/MC20X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
W0	0000								W0 (WRI	EG)								xxxx
W1	0002								W1									xxxx
W2	0004								W2									xxxx
W3	0006								W3									xxxx
W4	8000								W4									xxxx
W5	000A								W5									xxxx
W6	000C								W6									xxxx
W7	000E								W7									xxxx
W8	0010		W8 W9 W10															xxxx
W9	0012		W9 W10															xxxx
W10	0014																	xxxx
W11	0016		W10 W11															xxxx
W12	0018								W12									xxxx
W13	001A								W13									xxxx
W14	001C								W14									xxxx
W15	001E								W15									xxxx
SPLIM	0020								SPLIM	1								0000
PCL	002E								PCL								_	0000
PCH	0030	_	_	_	_	_	_	_	_	_				PCH				0000
DSRPAG	0032	_	_	_	_	_	_					DSR	PAG					0001
DSWPAG	0034	_	_	_	_	_	_	_					DSWPAG					0001
RCOUNT	0036								RCOUN	NT .								0000
SR	0042	_	_	_	_	_	_	_	DC	IPL2	IPL1	IPL0	RA	N	OV	Z	С	0000
CORCON	0044	VAR	_	_	_	_	_	_	_	_	_	_	_	IPL3	SFA	_	_	0020
DISICNT	0052	_	_							DISICNT<	<13:0>	·				·		0000
TBLPAG	0054	_	_	_	_	_	_	_	_			·	TBLPAG	G<7:0>		·		0000
MSTRPR	0058								MSTRPR<	15:0>								0000

TABLE 4-3: INTERRUPT CONTROLLER REGISTER MAP FOR PIC24EPXXXGP20X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IFS0	0800	_	DMA1IF	AD1IF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF	T2IF	OC2IF	IC2IF	DMA0IF	T1IF	OC1IF	IC1IF	INT0IF	0000
IFS1	0802	U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	DMA2IF	1	_	1	INT1IF	CNIF	CMIF	MI2C1IF	SI2C1IF	0000
IFS2	0804	_	_	1	1	1	_	1	1	1	IC4IF	IC3IF	DMA3IF	_	_	SPI2IF	SPI2EIF	0000
IFS3	0806	_	_	_	_	-	_	-	_	ı	_	_	-	_	MI2C2IF	SI2C2IF	_	0000
IFS4	8080	_	_	CTMUIF	_	-	_	-	_	1	_	_	1	CRCIF	U2EIF	U1EIF	_	0000
IFS8	0810	JTAGIF	ICDIF	_	_	_	_	_	_	_	_	_	_	_	_	_		0000
IFS9	0812		_	_	_	_	_	_	_	_	PTG3IF	PTG2IF	PTG1IF	PTG0IF	PTGWDTIF	PTGSTEPIF		0000
IEC0	0820	_	DMA1IE	AD1IE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE	T2IE	OC2IE	IC2IE	DMA0IE	T1IE	OC1IE	IC1IE	INT0IE	0000
IEC1	0822	U2TXIE	U2RXIE	INT2IE	T5IE	T4IE	OC4IE	OC3IE	DMA2IE	_	_	_	INT1IE	CNIE	CMIE	MI2C1IE	SI2C1IE	0000
IEC2	0824		_	_	_	_	_	_	_	_	IC4IE	IC3IE	DMA3IE	_	_	SPI2IE	SPI2EIE	0000
IEC3	0826		_	_	_	_	_	_	_	_	_	_	_	_	MI2C2IE	SI2C2IE		0000
IEC4	0828		_	CTMUIE	_	_	_	_	_	_	_	_	_	CRCIE	U2EIE	U1EIE		0000
IEC8	0830	JTAGIE	ICDIE	_	_	_	_	_	_	_	_	_	_	_	_	_		0000
IEC9	0832	_	_	_	_	_			_	PTG3IE	PTG2IE	PTG1IE	PTG0IE	PTGWDTIE	PTGSTEPIE	_	0000	
IPC0	0840			T1IP<2:0>			(OC1IP<2:0	>			IC1IP<2:0>		_		INT0IP<2:0>		4444
IPC1	0842			T2IP<2:0>		_	(OC2IP<2:0)>	_		IC2IP<2:0>		_	[OMA0IP<2:0>		4444
IPC2	0844		ι	J1RXIP<2:0	>	_	5	SPI1IP<2:0)>	_	5	SPI1EIP<2:0	>	_		T3IP<2:0>		4444
IPC3	0846		_	_	_	_	D	MA1IP<2:	0>	_		AD1IP<2:0>		_	ı	J1TXIP<2:0>		0444
IPC4	0848			CNIP<2:0>		_		CMIP<2:0:	>	_	N	/II2C1IP<2:0	>	_	5	SI2C1IP<2:0>		4444
IPC5	084A	_	_	_	_	-	_	-	_	ı	_	_	-	_		INT1IP<2:0>		0004
IPC6	084C	_		T4IP<2:0>		-	(OC4IP<2:0)>	1		OC3IP<2:0>		_	[OMA2IP<2:0>		4444
IPC7	084E	_	ι	J2TXIP<2:0	>	-	L	2RXIP<2:	0>	1		INT2IP<2:0>	•	_		T5IP<2:0>		4444
IPC8	0850	_	_	1	1	-	_	1	1	1		SPI2IP<2:0>	•	_	5	SPI2EIP<2:0>		0044
IPC9	0852	_	_	_	_	-		IC4IP<2:0	>	1		IC3IP<2:0>		_	[OMA3IP<2:0>		0444
IPC12	0858	_	_	_	-	l	M	12C2IP<2:	0>	1	5	SI2C2IP<2:0	>	_	_	_	_	0440
IPC16	0860	_	(CRCIP<2:0>	>	1	MI2C2IP<2:0> U2EIP<2:0>		1		U1EIP<2:0>		_	_	_	_	4440	
IPC19	0866	_		I	ı	1	U2EIP<2:0>			I	(CTMUIP<2:0	>	_	_	_	_	0040
IPC35	0886	_	J	ITAGID<2:0	>	1		ICDIP<2:0	>	1	_	_	1	_	_	_	_	4400
IPC36	0888	_	F	PTG0IP<2:0	>	1	PC	GWDTIP<2	2:0>	I	PT	GSTEPIP<2	:0>	_	_	_		4440
IPC37	A880	_	_	_	_	_	F	TG3IP<2:0	0>	_		PTG2IP<2:0	>	_	-	PTG1IP<2:0>		0444

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TABLE 4-3: INTERRUPT CONTROLLER REGISTER MAP FOR PIC24EPXXXGP20X DEVICES ONLY (CONTINUED)

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	AII Resets
INTCON1	08C0	NSTDIS	OVAERR	OVBERR	_	_	_	_	1	-	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL	_	0000
INTCON2	08C2	GIE	DISI	SWTRAP	_		_	1	1	1	_	1	_	_	INT2EP	INT1EP	INT0EP	8000
INTCON3	08C4	-	1		_		_	1	1	1	_	DAE	DOOVR	_	1	1	1	0000
INTCON4	08C6	1		_	_		_	-	1	1	_	1	_	_	-	1	SGHT	0000
INTTREG	08C8	-	1		_		ILR<	3:0>					VECN	JM<7:0>				0000

TABLE 4-4: INTERRUPT CONTROLLER REGISTER MAP FOR PIC24EPXXXMC20X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IFS0	0800	_	DMA1IF	AD1IF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF	T2IF	OC2IF	IC2IF	DMA0IF	T1IF	OC1IF	IC1IF	INT0IF	0000
IFS1	0802	U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	DMA2IF	1	_	1	INT1IF	CNIF	CMIF	MI2C1IF	SI2C1IF	0000
IFS2	0804		1		1	1		1		1	IC4IF	IC3IF	DMA3IF	_	-	SPI2IF	SPI2EIF	0000
IFS3	0806	_	1	_	1	1	QEI1IF	PSEMIF	_	1	_	1	_	_	MI2C2IF	SI2C2IF	1	0000
IFS4	8080	_	-	CTMUIF	-	_	_	_	_	1	_	_	_	CRCIF	U2EIF	U1EIF	_	0000
IFS5	080A	PWM2IF	PWM1IF	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
IFS6	080C	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	PWM3IF	0000
IFS8	0810	JTAGIF	ICDIF	_	-	_	_	_	_	1	_	_	_	_	_	_	_	0000
IFS9	0812	_	1	_	1	1	_	1	_	1	PTG3IF	PTG2IF	PTG1IF	PTG0IF	PTGWDTIF	PTGSTEPIF	1	0000
IEC0	0820	_	DMA1IE	AD1IE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE	T2IE	OC2IE	IC2IE	DMA0IE	T1IE	OC1IE	IC1IE	INT0IE	0000
IEC1	0822	U2TXIE	U2RXIE	INT2IE	T5IE	T4IE	OC4IE	OC3IE	DMA2IE	1	_	_	INT1IE	CNIE	CMIE	MI2C1IE	SI2C1IE	0000
IEC2	0824	_	-	_	-	_	_	_	_	1	IC4IE	IC3IE	DMA3IE	_	_	SPI2IE	SPI2EIE	0000
IEC3	0826		1		1	1	QEI1IE	PSEMIE	_	1	_	1	_	_	MI2C2IE	SI2C2IE	1	0000
IEC4	0828	_	1	CTMUIE	1	1	_	1	_	1	_	1	_	CRCIE	U2EIE	U1EIE	1	0000
IEC5	082A	PWM2IE	PWM1IE	_	ı	1	_	1	_	1	_	1	_	_	_	_	-	0000
IEC6	082C	_	1	_	1	1	_	1	_	1	_	1	_	_	_	_	PWM3IE	0000
IEC8	0830	JTAGIE	ICDIE	_	1	1		1		1	_	1	_	_	-	_	1	0000
IEC9	0832		1		1	1		1		1	PTG3IE	PTG2IE	PTG1IE	PTG0IE	PTGWDTIE	PTGSTEPIE	1	0000
IPC0	0840	_		T1IP<2:0>		1	(OC1IP<2:0)>	1		IC1IP<2:0>		_		INT0IP<2:0>		4444
IPC1	0842	_		T2IP<2:0>		1	(OC2IP<2:0)>	1		IC2IP<2:0>		_	[OMA0IP<2:0>		4444
IPC2	0844		J	J1RXIP<2:0	>	1	9	SPI1IP<2:0)>	1	9	SPI1EIP<2:0	>	_		T3IP<2:0>		4444
IPC3	0846		1		1	1	D	MA1IP<2:	0>	1		AD1IP<2:0>	•	_		U1TXIP<2:0>		0444
IPC4	0848			CNIP<2:0>		1		CMIP<2:0	>	1	N	/II2C1IP<2:0	>	_		SI2C1IP<2:0>		4444
IPC5	084A	_	1	_	ı	1	_	1	_	1	_	1	_	_		INT1IP<2:0>		0004
IPC6	084C	_		T4IP<2:0>		1	(OC4IP<2:0)>	1		OC3IP<2:0>	•	_	[OMA2IP<2:0>		4444
IPC7	084E		ι	J2TXIP<2:0	>	1	l	J2RXIP<2:	0>	1		INT2IP<2:0>	>	_		T5IP<2:0>		4444
IPC8	0850		1		1	1		1		1		SPI2IP<2:0>	>	_		SPI2EIP<2:0>		0044
IPC9	0852	_	1	_	1	1		IC4IP<2:0	>	1		IC3IP<2:0>		_	[DMA3IP<2:0>		0444
IPC12	0858	_	1	_	1	1	M	II2C2IP<2:	0>	1	5	SI2C2IP<2:0	>	_	_	_	1	0440
IPC14	085C	_	1	_	1	-	(QEI1IP<2:0)>	1	F	PSEMIP<2:0	>	_	_	_	1	0440
IPC16	0860			CRCIP<2:0>	>	1	ı	J2EIP<2:0	>	1		U1EIP<2:0>	•	_	-	_	1	4440
IPC19	0866	_	1	_	1	-	_	_	_	1	(CTMUIP<2:0	>	_	_	_	1	0040
IPC23	086E	_	P	WM2IP<2:0)>		Р	WM1IP<2:	:0>	1	_	_	_	_	_		1	4400
IPC24	0870	_	1	_	-	_		_	_	1	_	_	_	_	F	PWM3IP<2:0>		4004
IPC35	0886	_	J	JTAGID<2:0	>	1		ICDIP<2:0	>	1	_	1	_	_	_	_		4400

TABLE 4-4: INTERRUPT CONTROLLER REGISTER MAP FOR PIC24EPXXXMC20X DEVICES ONLY (CONTINUED)

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	AII Resets
IPC36	0888	_	F	TG0IP<2:0	>	_	PC	GWDTIP<2	:0>	_	PT	GSTEPIP<2	:0>	_	_	_	_	4440
IPC37	088A	1		_	_	_	F	TG3IP<2:)>	_	F	PTG2IP<2:0	>		F	PTG1IP<2:0>		0444
INTCON1	08C0	NSTDIS	OVAERR	OVBERR	_	_	1	1	1	_	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL	_	0000
INTCON2	08C2	GIE	DISI	SWTRAP	_	_	1	1	1	_		_	_		INT2EP	INT1EP	INT0EP	8000
INTCON3	08C4	1		_	_	_	1	1	1	_		DAE	DOOVR		_	_	_	0000
INTCON4	08C6	-		_	_	_	1	1	I	_		_	-	-	_	-	SGHT	0000
INTTREG	08C8	_	_	_	_		ILR<	3:0>	·	·			VECNU	JM<7:0>		<u>'</u>		0000

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TABLE 4-5: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXGP50X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IFS0	0800	_	DMA1IF	AD1IF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF	T2IF	OC2IF	IC2IF	DMA0IF	T1IF	OC1IF	IC1IF	INT0IF	0000
IFS1	0802	U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	DMA2IF	1	_	1	INT1IF	CNIF	CMIF	MI2C1IF	SI2C1IF	0000
IFS2	0804	1	1	_	_	1	_	1		1	IC4IF	IC3IF	DMA3IF	C1IF	C1RXIF	SPI2IF	SPI2EIF	0000
IFS3	0806	_	1	_	_	I	_	1	_	1	_	1	1	1	MI2C2IF	SI2C2IF	ı	0000
IFS4	0808	_	_	CTMUIF	_	I	_	_	_	1	C1TXIF	_	_	CRCIF	U2EIF	U1EIF	ı	0000
IFS6	080C	_	_	_	_	I	_	_	_	1	_	_	_	-	_	_	PWM3IF	0000
IFS8	0810	JTAGIF	ICDIF	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
IFS9	0812	_	_	_	_	_	_	_	_	_	PTG3IF	PTG2IF	PTG1IF	PTG0IF	PTGWDTIF	PTGSTEPIF	_	0000
IEC0	0820	_	DMA1IE	AD1IE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE	T2IE	OC2IE	IC2IE	DMA0IE	T1IE	OC1IE	IC1IE	INT0IE	0000
IEC1	0822	U2TXIE	U2RXIE	INT2IE	T5IE	T4IE	OC4IE	OC3IE	DMA2IE	_	_	_	INT1IE	CNIE	CMIE	MI2C1IE	SI2C1IE	0000
IEC2	0824	_	_	_	_	_	_	_	_	_	IC4IE	IC3IE	DMA3IE	C1IE	C1RXIE	SPI2IE	SPI2EIE	0000
IEC3	0826	_	_	_	_	_	_	_	_	_	_	_	_	_	MI2C2IE	SI2C2IE	_	0000
IEC4	0828	_	_	CTMUIE	_		_	_	_	_	C1TXIE	_	_	CRCIE	U2EIE	U1EIE	_	0000
IEC8	0830	JTAGIE	ICDIE	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
IEC9	0832	_	_	_	_	_	_	_	_	_	PTG3IE	PTG2IE	PTG1IE	PTG0IE	PTGWDTIE	PTGSTEPIE	_	0000
IPC0	0840	_		T1IP<2:0>		_	(OC1IP<2:0)>	_		IC1IP<2:0>		_		INT0IP<2:0>		4444
IPC1	0842	_		T2IP<2:0>		I	(OC2IP<2:0)>	1		IC2IP<2:0>		-	[OMA0IP<2:0>		4444
IPC2	0844	_	ι	J1RXIP<2:0	>		5	SPI1IP<2:0)>	_	5	SPI1EIP<2:0	>	_		T3IP<2:0>		4444
IPC3	0846	_	_	_	_	I	D	MA1IP<2:	0>	1		AD1IP<2:0>		-	ı	J1TXIP<2:0>		0444
IPC4	0848	_		CNIP<2:0>		I		CMIP<2:0	>	1	N	/II2C1IP<2:0	>	-	5	SI2C1IP<2:0>		4444
IPC5	084A	_	_	_	_	I	_	_	_	1	_	_	_	-		INT1IP<2:0>		0004
IPC6	084C	1		T4IP<2:0>		1	(OC4IP<2:0)>	1		OC3IP<2:0>		1	[OMA2IP<2:0>		4444
IPC7	084E	_	Į	J2TXIP<2:0	>	I	L	J2RXIP<2:0	0>	1		INT2IP<2:0>	•	1		T5IP<2:0>		4444
IPC8	0850	_		C1IP<2:0>		I	C	1RXIP<2:0	0>	1		SPI2IP<2:0>	•	-	5	SPI2EIP<2:0>		4444
IPC9	0852	_	1	_	_	l		IC4IP<2:0	>	1		IC3IP<2:0>		1	[OMA3IP<2:0>		0444
IPC11	0856	1	1	_	_	1	_	1		1	_	1	1	1	_	_	1	0000
IPC12	0858	_	1	_	_	1	M	II2C2IP<2:	0>	1	9	SI2C2IP<2:0	>	1	_	_	1	0440
IPC16	0860	_		CRCIP<2:0>	•	l	ı	J2EIP<2:0	>	1		U1EIP<2:0>		1	_	_	ı	4440
IPC17	0862	1	1	_	_	1	C	:1TXIP<2:0)>	1	_	1	1	1	_	_	1	0400
IPC19	0866	_	1	_	_	1	_	_	_	1	(CTMUIP<2:0	>	-	_	_	_	0040
IPC35	0886	_		JTAGID<2:0	>			ICDIP<2:0	>	_				_	_	_		4400
IPC36	0888	_	F	PTG0IP<2:0	>	_	PC	GWDTIP<2	2:0>	_	PT	GSTEPIP<2	:0>		_	_	_	4440
IPC37	088A	_	1	_	_	1	F	TG3IP<2:0	0>	1	-	PTG2IP<2:0	>	-		PTG1IP<2:0>		0444

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TABLE 4-5: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXGP50X DEVICES ONLY (CONTINUED)

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	AII Resets
INTCON1	08C0	NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE	COVTE	SFTACERR	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL	1	0000
INTCON2	08C2	GIE	DISI	SWTRAP	_	1	_	1	1	_	1	-	_	_	INT2EP	INT1EP	INT0EP	8000
INTCON3	08C4	-	_	_	_	-	_	-	_	_	_	DAE	DOOVR	_	-	-	_	0000
INTCON4	08C6	1	1	-	_	_	_	-	1	_	1	1	_	_	-	1	SGHT	0000
INTTREG	08C8	-	_	_	_		ILR<	3:0>	•		•	•	VECNU	JM<7:0>	•	•	•	0000

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	INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXMC20X DEVICES ONLY	
TABLE 4-6:		

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	AII Resets
IFS0	0800	_	DMA1IF	AD1IF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF	T2IF	OC2IF	IC2IF	DMA0IF	T1IF	OC1IF	IC1IF	INT0IF	0000
IFS1	0802	U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	DMA2IF	1	_	1	INT1IF	CNIF	CMIF	MI2C1IF	SI2C1IF	0000
IFS2	0804	1	1		1	1	_	1		1	IC4IF	IC3IF	DMA3IF	1	_	SPI2IF	SPI2EIF	0000
IFS3	0806	1	ı	_	-	ı	QEI1IF	PSEMIF	_	1	_	1	_	1	MI2C2IF	SI2C2IF	_	0000
IFS4	0808	_	_	CTMUIF	_	_	_	_	_	_	_	_	_	CRCIF	U2EIF	U1EIF	_	0000
IFS5	080A	PWM2IF	PWM1IF	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
IFS6	080C	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	PWM3IF	0000
IFS8	0810	JTAGIF	ICDIF	_	_	_	_	_	_	-	_	_	_	_	_	_	_	0000
IFS9	0812	_	_	_	_	_	_	_	_	_	PTG3IF	PTG2IF	PTG1IF	PTG0IF	PTGWDTIF	PTGSTEPIF	_	0000
IEC0	0820	_	DMA1IE	AD1IE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE	T2IE	OC2IE	IC2IE	DMA0IE	T1IE	OC1IE	IC1IE	INT0IE	0000
IEC1	0822	U2TXIE	U2RXIE	INT2IE	T5IE	T4IE	OC4IE	OC3IE	DMA2IE	1	_	1	INT1IE	CNIE	CMIE	MI2C1IE	SI2C1IE	0000
IEC2	0824	1	1		1	1	_	1		1	IC4IE	IC3IE	DMA3IE	1	_	SPI2IE	SPI2EIE	0000
IEC3	0826	1	1		1	1	QEI1IE PSEMIE —		1	_	1	_	1	MI2C2IE	SI2C2IE	_	0000	
IEC4	0828	1	1	CTMUIE	1	1			1	_	1	_	CRCIE	U2EIE	U1EIE	_	0000	
IEC5	082A	PWM2IE	PWM1IE	_	1	1	_	1		1	_	1	_	1	_	_	_	0000
IEC6	082C	1	1		1	1	_	1		1	_	1	_	1	_	_	PWM3IE	0000
IEC8	0830	JTAGIE	ICDIE	_	1	1	_	1		1	_	1	_	1	_	_	_	0000
IEC9	0832	1	1	_	1	1	_	-	-	1	PTG3IE	PTG2IE	PTG1IE	PTG0IE	PTGWDTIE	PTGSTEPIE	_	0000
IPC0	0840	1		T1IP<2:0>		1	(OC1IP<2:0)>	1		IC1IP<2:0>		1		INT0IP<2:0>		4444
IPC1	0842	1		T2IP<2:0>		1	(OC2IP<2:0)>	1		IC2IP<2:0>		1	[OMA0IP<2:0>		4444
IPC2	0844	1	l	J1RXIP<2:0	>	-	Ş	SPI1IP<2:0)>	1	9	SPI1EIP<2:0	>	-		T3IP<2:0>		4444
IPC3	0846	_	_	_	_	_	С	MA1IP<2:	0>	_		AD1IP<2:0>	•	_		U1TXIP<2:0>		0444
IPC4	0848	1		CNIP<2:0>		1		CMIP<2:0	>	1	N	/II2C1IP<2:0)>	1	9	SI2C1IP<2:0>		4444
IPC5	084A	1	1		1	1	_	1		1	_	1	_	1		INT1IP<2:0>		0004
IPC6	084C	1		T4IP<2:0>		1	(OC4IP<2:0)>	1		OC3IP<2:0>	>	1	[OMA2IP<2:0>		4444
IPC7	084E	1	ı	J2TXIP<2:0	>	-	L	I2RXIP<2:	<0>	1		INT2IP<2:0	>	-		T5IP<2:0>		4444
IPC8	0850	1	-	_	_	_	C	1RXIP<2:	0>	1		SPI2IP<2:0>	>	-	9	SPI2EIP<2:0>		0444
IPC9	0852	1	-		-	-		IC4IP<2:0	^	1		IC3IP<2:0>		-	[OMA3IP<2:0>		0444
IPC12	0858	_	_	_	_	_	N	II2C2IP<2:	0>	_		SI2C2IP<2:0	>	_	_	_	_	0440
IPC14	085C	_	_	_	_	_	(QEI1IP<2:0)>	_	F	PSEMIP<2:0	 >	_	_	_	_	0440
IPC16	0860	_		CRCIP<2:0>	>	_		U2EIP<2:0	>	_		U1EIP<2:0>	•	_	_	_	_	4440
IPC19	0866	I	I	_	_		_		_		(CTMUIP<2:0)>			_		0040
IPC23	086E	1	P	WM2IP<2:0)>		Р	WM1IP<2:	:0>	1	_	_	_	_	_			4400
IPC24	0870	1		_			_			_		_		_	F	PWM3IP<2:0>		0004
IPC35	0886	_		JTAGID<2:0	>	_		ICDIP<2:0	>	_		_		_			_	4400

TABLE 4-6: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXMC20X DEVICES ONLY (CONTINUED)

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IPC36	0888	_	Р	TG0IP<2:0	>		PC	GWDTIP<2	:0>	-	PT	GSTEPIP<2	:0>	_		I	I	4440
IPC37	088A	-		_	1	1	F	TG3IP<2:)>	1	ı	PTG2IP<2:0>	>	_	F	PTG1IP<2:0>		0444
INTCON1	08C0	NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE	COVTE	SFTACERR	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL	1	0000
INTCON2	08C2	GIE	DISI	SWTRAP	-	1	-	1	ı	-	1	_	_	_	INT2EP	INT1EP	INT0EP	8000
INTCON3	08C4	-		_	1	1	1	1	1	1	1	DAE	DOOVR	_	1	I	1	0000
INTCON4	08C6	-		_	1	1	1	1	1	1	1	-	_	_	1	I	SGHT	0000
INTTREG	08C8	_	_	_	_		ILR<	3:0>			·		VECNU	JM<7:0>			·	0000

TABLE 4-7: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXMC50X DEVICES ONLY

IADLL	. 4-7.		LIVINOR		NOLLL		J . L		JIV USE	.0001.	.,,,,,,,,,,,,,,,	U/ D_ 1	CL3 OI	· - ·				
File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IFS0	0800	_	DMA1IF	AD1IF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF	T2IF	OC2IF	IC2IF	DMA0IF	T1IF	OC1IF	IC1IF	INT0IF	0000
IFS1	0802	U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	DMA2IF	_	_	_	INT1IF	CNIF	CMIF	MI2C1IF	SI2C1IF	0000
IFS2	0804	1	_	_	-	-	_	_	_	_	IC4IF	IC3IF	DMA3IF	C1IF	C1RXIF	SPI2IF	SPI2EIF	0000
IFS3	0806	1	_	_	1	1	QEI1IF	PSEMIF	_	_	_	1	_	_	MI2C2IF	SI2C2IF	_	0000
IFS4	0808	1	_	CTMUIF	1	1	_	1		_	C1TXIF	1	_	CRCIF	U2EIF	U1EIF	_	0000
IFS5	080A	PWM2IF	PWM1IF	_	1	1	_	-	-	_	_	1	_	_	_	_	_	0000
IFS6	080C	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	PWM3IF	0000
IFS8	0810	JTAGIF	ICDIF	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
IFS9	0812	1	_	_	1	1	_	1	_	_	PTG3IF	PTG2IF	PTG1IF	PTG0IF	PTGWDTIF	PTGSTEPIF	_	0000
IEC0	0820	-	DMA1IE	AD1IE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE	T2IE	OC2IE	IC2IE	DMA0IE	T1IE	OC1IE	IC1IE	INT0IE	0000
IEC1	0822	U2TXIE	U2RXIE	INT2IE	T5IE	T4IE	OC4IE	OC3IE	DMA2IE	_	_	_	INT1IE	CNIE	CMIE	MI2C1IE	SI2C1IE	0000
IEC2	0824	1	_	_	1	1	_	1	_	_	IC4IE	IC3IE	DMA3IE	C1IE	C1RXIE	SPI2IE	SPI2EIE	0000
IEC3	0826	_	_	_	_	_	QEI1IE	QEI1IE PSEMIE —		_	_	_	_	_	MI2C2IE	SI2C2IE	_	0000
IEC4	0828	_	_	CTMUIE	_	_			_	C1TXIE	_	_	CRCIE	U2EIE	U1EIE	_	0000	
IEC5	082A	PWM2IE	PWM1IE	_	_	_	_				_	_	_	_	_	_	_	0000
IEC6	082C	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	PWM3IE	0000
IEC7	082E	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
IEC8	0830	JTAGIE	ICDIE	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
IEC9	0832	-	_	_	1	1	_	-	-	_	PTG3IE	PTG2IE	PTG1IE	PTG0IE	PTGWDTIE	PTGSTEPIE	_	0000
IPC0	0840	_		T1IP<2:0>		_	(OC1IP<2:0)>	_		IC1IP<2:0>		_		INT0IP<2:0>		4444
IPC1	0842	_		T2IP<2:0>		_	(OC2IP<2:0)>	_		IC2IP<2:0>		_	[OMA0IP<2:0>		4444
IPC2	0844	1	ι	J1RXIP<2:0	>	1	9	SPI1IP<2:0)>	_	9	SPI1EIP<2:0	>	_		T3IP<2:0>		4444
IPC3	0846	1	_	_	1	1	D	MA1IP<2:	0>	_		AD1IP<2:0>	•	_	ı	U1TXIP<2:0>		0444
IPC4	0848	-		CNIP<2:0>		1		CMIP<2:0	>	_	N	/II2C1IP<2:0	>	_	5	SI2C1IP<2:0>		4444
IPC5	084A	_	_	_	_	_	_	_	_	_	_	_	_	_		INT1IP<2:0>		0004
IPC6	084C	_		T4IP<2:0>		_	(OC4IP<2:0)>	_		OC3IP<2:0>	•	_	[OMA2IP<2:0>		4444
IPC7	084E	1	l	J2TXIP<2:0	>	1	L	J2RXIP<2:	0>	_		INT2IP<2:0>	>	_		T5IP<2:0>		4444
IPC8	0850	-		C1IP<2:0>		1	C	1RXIP<2:	0>	_		SPI2IP<2:0>	>	_	9	SPI2EIP<2:0>		4444
IPC9	0852	_	_	_	_	_		IC4IP<2:0	>	_		IC3IP<2:0>		_	[OMA3IP<2:0>		0444
IPC12	0858	1	_	_	1	1	M	II2C2IP<2:	0>	_	5	SI2C2IP<2:0	>	_	_	_	_	0440
IPC14	085C	1	_	_	_	_	(QEI1IP<2:0)>	_	F	PSEMIP<2:0	>	_	_	_	_	0440
IPC16	0860	_		CRCIP<2:0	>		ı	U2EIP<2:0)>			U1EIP<2:0>		_	_	_		4440
IPC17	0862	-	_		_		C	C1TXIP<2:	0>					_	_			0400
IPC19	0866	-	_	_				_	_	_	(CTMUIP<2:0	>	_	_	_	_	0040
IPC23	086E	1	P	PWM2IP<2:0)>		Р	WM1IP<2:	:0>	_	_		_	_	_	_	_	4400

TABLE 4-7: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXMC50X DEVICES ONLY (CONTINUED)

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IPC24	0870	_	_	_	_	_	_	_	_	_	_	_	_	_	F	PWM3IP<2:0>		0004
IPC35	0886	1	J	ITAGID<2:0	>	_		ICDIP<2:0	>	_	1	_	-	_	I	-	1	4400
IPC36	0888	1	F	PTG0IP<2:0	>	-	PC	GWDTIP<2	2:0>	1	PT	GSTEPIP<2	:0>	_	1	1	1	4440
IPC37	A880	1	_	1	1	-	P	TG3IP<2:0								0444		
INTCON1	08C0	NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE	COVTE	SFTACERR	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL	_	0000
INTCON2	08C2	GIE	DISI	SWTRAP	1		1	1	-	1	1	_	-	_	INT2EP	INT1EP	INT0EP	8000
INTCON3	08C4	-	_	_	_	_	_	-	_	_	-	DAE	DOOVR	_	-	_	_	0000
INTCON4	08C6	1	_	1	-	_	1	1	-		1	_	1	_	I	-	SGHT	0000
INTTREG	08C8	_	_	_	_		ILR<	3:0>	·		·		VECNU	JM<7:0>	·	<u>'</u>		0000

TABLE 4-8: TIMER1 THROUGH TIMER5 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TMR1	0100								Timer1	Register								xxxx
PR1	0102								Period F	Register 1								FFFF
T1CON	0104	TON	_	TSIDL	_	_	_	_	_	_	TGATE	TCKPS	S<1:0>	_	TSYNC	TCS	_	0000
TMR2	0106								Timer2	Register								xxxx
TMR3HLD	0108						Time	r3 Holding F	Register (fo	r 32-bit time	r operations	only)						xxxx
TMR3	010A	9												xxxx				
PR2	010C														FFFF			
PR3	010E								Period F	Register 3								FFFF
T2CON	0110	TON	_	TSIDL	_	-	_	_	_	_	TGATE	TCKPS	S<1:0>	T32	_	TCS	_	0000
T3CON	0112	TON	_	TSIDL	_	_	_	_	_	_	TGATE	TCKP	S<1:0>	_	_	TCS	_	0000
TMR4	0114								Timer4	Register								xxxx
TMR5HLD	0116						Ti	mer5 Holdir	ıg Register	(for 32-bit o	perations or	nly)						xxxx
TMR5	0118								Timer5	Register								xxxx
PR4	011A								Period F	Register 4								FFFF
PR5	011C								Period F	Register 5								FFFF
T4CON	011E	TON	_	TSIDL	_	_	_	_	_	_	TGATE	TCKP	S<1:0>	T32	_	TCS	_	0000
T5CON	0120	TON	_	TSIDL	_	_	_	_	_	_	TGATE	TCKPS	S<1:0>	_	_	TCS	_	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-9: INPUT CAPTURE 1 THROUGH INPUT CAPTURE 4 REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	AII Resets	
IC1CON1	0140	_	_	ICSIDL	10	CTSEL<2:0	>	_	_	_	ICI<1	1:0>	ICOV	ICBNE		ICM<2:0>		0000	
IC1CON2	0142	1	_	_	_	_	_	_	IC32	ICTRIG	TRIGSTAT	_		S۱	/NCSEL<4:	0>		000D	
IC1BUF	0144							Inpu	ut Capture 1	Buffer Reg	jister							xxxx	
IC1TMR	0146								Input Capt	ure 1 Timer								0000	
IC2CON1	0148	_	_	ICSIDL	10	CTSEL<2:0	>	_	_	_	ICI<1	1:0>	ICOV	ICBNE		ICM<2:0>		0000	
IC2CON2	014A	_	_	_	_	_	_	_	IC32	ICTRIG	TRIGSTAT	_		S۱				000D	
IC2BUF	014C							Inpu	ıt Capture 2	Buffer Reg	jister					ICM<2:0> ICSEL<4:0> ICM<2:0>			
IC2TMR	014E								Input Capt	ure 2 Timer				SYNCSEL<4:0>				0000	
IC3CON1	0150	_	_	ICSIDL	10	CTSEL<2:0	>	_	_	_	ICI<1	1:0>	ICOV	ICBNE		ICM<2:0>		0000	
IC3CON2	0152	_	_	_	_	_	_	_	IC32	ICTRIG	TRIGSTAT	_		S۱	/NCSEL<4:	0>		000D	
IC3BUF	0154							Inpu	ut Capture 3	Buffer Reg	jister					ICM<2:0> ICM<2:0> ICM<2:0>			
IC3TMR	0156								Input Capt	ure 3 Timer								0000	
IC4CON1	0158	_	_	ICSIDL	10	CTSEL<2:0	>	_	_	-	ICI<1	1:0>	ICOV	ICBNE		ICM<2:0>		0000	
IC4CON2	015A	1	_	_	_	_	_	_	IC32	ICTRIG	TRIGSTAT	_		S۱	/NCSEL<4:	0>		000D	
IC4BUF	015C							Inpu	ut Capture 4	Buffer Reg	ister					ICM<2:0> ICM<2:0> ICM<2:0> ICM<2:0> ICM<2:0> ICM<2:0>			
IC4TMR	015E								Input Capt	ure 4 Timer						ICM<2:0> SEL<4:0> ICM<2:0> SEL<4:0> ICM<2:0> ICM<2:0> ICM<2:0> ICM<2:0>			

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-10: OUTPUT COMPARE 1 THROUGH OUTPUT COMPARE 4 REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets			
OC1CON1	0900		_	OCSIDL	С	CTSEL<2:0	>	_	ENFLTB	ENFLTA	_	OCFLTB	OCFLTA	TRIGMODE		OCM<2:0>		0000			
OC1CON2	0902	FLTMD	FLTOUT	FLTTRIEN	OCINV	_		_	OC32	OCTRIG	TRIGSTAT	OCTRIS		SY	NCSEL<4:0	>		000C			
OC1RS	0904							Out	put Compare	1 Seconda	ry Register							xxxx			
OC1R	0906								Output Co	mpare 1 Re	gister							xxxx			
OC1TMR	0908								Timer Va	alue 1 Regis	ter							xxxx			
OC2CON1	090A	1	_	OCSIDL	C	CTSEL<2:0	>	_	ENFLTB	ENFLTA	_	OCFLTB	OCFLTA	TRIGMODE		OCM<2:0>		0000			
OC2CON2	090C	FLTMD	FLTOUT	FLTTRIEN	OCINV	_	_	_	OC32	OCTRIG	TRIGSTAT	OCTRIS		SY	NCSEL<4:0	000C					
OC2RS	090E							Out	put Compare	e 2 Seconda	ry Register					xxxx					
OC2R	0910								Output Co	mpare 2 Re	gister										
OC2TMR	0912								Timer Va	alue 2 Regis	ter							xxxx			
OC3CON1	0914	1	_	OCSIDL	C	CTSEL<2:0	>	_	ENFLTB	ENFLTA	_	OCFLTB	OCFLTA	TRIGMODE		OCM<2:0>		0000			
OC3CON2	0916	FLTMD	FLTOUT	FLTTRIEN	OCINV	_	_	_	OC32	OCTRIG	TRIGSTAT	OCTRIS		SY	NCSEL<4:0	>		000C			
OC3RS	0918							Out	put Compare	e 3 Seconda	ry Register							xxxx			
OC3R	091A								Output Co	mpare 3 Re	gister							xxxx			
OC3TMR	091C								Timer Va	alue 3 Regis	ter							xxxx			
OC4CON1	091E	1	_	OCSIDL	C	CTSEL<2:0	>	ENFLTC	ENFLTB	ENFLTA	OCFLTC	OCFLTB	OCFLTA	TRIGMODE		OCM<2:0>		0000			
OC4CON2	0920	FLTMD	FLTOUT	FLTTRIEN	OCINV	_	_	_	OC32	OCTRIG	TRIGSTAT	OCTRIS		SY	NCSEL<4:0	>		000C			
OC4RS	0922							Out	put Compare	e 4 Seconda	ry Register							xxxx			
OC4R	0924								Output Co	mpare 4 Re	gister							xxxx			
OC4TMR	0926		•	•		•			Timer Va	alue 4 Regis	ter		•		•			xxxx			

TABLE 4-11: PTG REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PTGCST	0AC0	PTGEN	_	PTGSIDL	PTGTOGL	_	PTGSWT	_	PTGIVIS	PTGSTRT	PTGWTO	-	_	_	_	PTGITI	M<1:0>	0000
PTGCON	0AC2	F	PTGCLK<2	:0>		Р	TGDIV<4:0>	•			PTGPWI	0<3:0>		_	PT	GWDT<2:	0>	0000
PTGBTE	0AC4								PTGBTE<	:15:0>								0000
PTGHOLD	0AC6								PTGHOLD	<15:0>								0000
PTGT0LIM	0AC8								PTGT0LIM	<15:0>								0000
PTGT1LIM	0ACA								PTGT1LIM	<15:0>								0000
PTGSDLIM	0ACC		PTGSDLIM<15:0> PTGC0LIM<15:0>														0000	
PTGC0LIM	0ACE		PTGC0LIM<15:0>														0000	
PTGC1LIM	0AD0		PTGC0LIM<15:0> PTGC1LIM<15:0>														0000	
PTGADJ	0AD2								PTGADJ<	15:0>								0000
PTGL0	0AD4								PTGL0<1	15:0>								0000
PTGQPTR	0AD6	_	_	_	_	_	_	_	_	_	_	_		PT	GQPTR<4	0>		0000
PTGQUE0	0AD8				STEF	21<7:0>							STEP0<	7:0>				0000
PTGQUE1	0ADA				STEF	23<7:0>							STEP2<	7:0>				0000
PTGQUE2	0ADC				STER	P5<7:0>							STEP4<	7:0>				0000
PTGQUE3	0ADE				STER	27<7:0>							STEP6<	7:0>				0000
PTGQUE4	0AE0				STEF	9<7:0>			·				STEP8<	7:0>				0000
PTGQUE5	0AE2				STEP	11<7:0>							STEP10<	÷7:0>				0000
PTGQUE6	0AE4		•		STEP	13<7:0>		•			•	•	STEP12<	÷7:0>	•	•	•	0000
PTGQUE7	0AE6				STEP	15<7:0>							STEP14<	:7:0>				0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-12: PWM REGISTER MAP FOR dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	AII Resets
PTCON	0C00	PTEN		PTSIDL	SESTAT	SEIEN	EIPU	SYNCPOL	SYNCOEN	SYNCEN	SYI	NCSRC<2	2:0>		SEV	TPS<3:0>		0000
PTCON2	0C02	_	_	_	_	_	_	_	_	_	_	_	_	_	F	PCLKDIV<2:0)>	0000
PTPER	0C04								PTPER<15	:0>								00F8
SEVTCMP	0C06								SEVTCMP<1	5:0>								0000
MDC	0C0A								MDC<15:0)>								0000
CHOP	0C1A	CHPCLKEN	_	_	_	_	_					CHOPCL	.K<9:0>					0000
PWMKEY	0C1E								PWMKEY<1	5:0>								0000

TABLE 4-13: PWM GENERATOR 1 REGISTER MAP FOR dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PWMCON1	0C20	FLTSTAT	CLSTAT	TRGSTAT	FLTIEN	CLIEN	TRGIEN	ITB	MDCS	DTC<	1:0>	DTCP	_	MTBS	CAM	XPRES	IUE	0000
IOCON1	0C22	PENH	PENL	POLH	POLL	PMOD	<1:0>	OVRENH	OVRENL	OVRDA	T<1:0>	FLTDA	\T<1:0>	CLDA	T<1:0>	SWAP	OSYNC	0000
FCLCON1	0C24	_		(0000	
PDC1	0C26				PDC1<15:0>													FFF8
PHASE1	0C28																	0000
DTR1	0C2A	_	_							DTR1<13:	0>							0000
ALTDTR1	0C2C	_	_						Α	LTDTR1<1	3:0>							0000
TRIG1	0C32								TRGCMP<15	5:0>								0000
TRGCON1	0C34		TRGDI	V<3:0>		_	_	_	_	_	_			TRG	STRT<5:0	>		0000
LEBCON1	0C3A	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	_	_	_	_	BCH	BCL	BPHH	BPHL	BPLH	BPLL	0000
LEBDLY1	0C3C	_	_	_	_						LEB<11	:0>						0000
AUXCON1	0C3E	_	_	_	_		BLANKS	EL<3:0>		_	_		CHOPC	LK<3:0>		CHOPHEN	CHOPLEN	0000

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, AND PIC24EPXXXGP/MC20X

TABLE 4-14: PWM GENERATOR 2 REGISTER MAP FOR dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PWMCON2	0C40	FLTSTAT	CLSTAT	TRGSTAT	FLTIEN	CLIEN	TRGIEN	ITB	MDCS	DTC<	1:0>	DTCP	_	MTBS	CAM	XPRES	IUE	0000
IOCON2	0C42	PENH	PENL	POLH	POLL	PMOD	<1:0>	OVRENH	OVRENL	OVRDA	T<1:0>	FLTDA	\T<1:0>	CLDA	\T<1:0>	SWAP	OSYNC	0000
FCLCON2	0C44	_															00F8	
PDC2	0C46			PDC2<15:0> 00													0000	
PHASE2	0C48															0000		
DTR2	0C4A	_	_							TR2<13:0>	•							0000
ALTDTR2	0C4C	_	_						AL ⁻	ΓDTR2<13:	0>							0000
TRIG2	0C52							TF	RGCMP<15:0	>								0000
TRGCON2	0C54		TRGDI	/<3:0>		_	_	_	_	_	_			TRO	STRT<5:0)>		0000
LEBCON2	0C5A	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	_	_	_	_	BCH	BCL	BPHH	BPHL	BPLH	BPLL	0000
LEBDLY2	0C5C	_	_	_	_						LEB<11:0)>						0000
AUXCON2	0C5E	_	_	_	_		BLANK	SEL<3:0>		_	_		CHOPS	EL<3:0>		CHOPHEN	CHOPLEN	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-15: PWM GENERATOR 3 REGISTER MAP FOR dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PWMCON3	0C60	FLTSTAT	CLSTAT	TRGSTAT	FLTIEN	CLIEN	TRGIEN	ITB	MDCS	DTC<	<1:0>	DTCP	_	MTBS	CAM	XPRES	IUE	0000
IOCON3	0C62	PENH	PENL	POLH	POLL	PMOD	<1:0>	OVRENH	OVRENL	OVRDA	T<1:0>	FLTDA	T<1:0>	CLDA	AT<1:0>	SWAP	OSYNC	0000
FCLCON3	0C64	_		C	CLSRC<4:0> CLPOL CLMOD FLTSRC<4:0> FLTPOL FLTMOD<1:0>													00F8
PDC3	0C66				PDC3<15:0>													0000
PHASE3	0C68				PDC3<15:0> PHASE3<15:0>													0000
DTR3	0C6A	_	_							TR3<13:0	>							0000
ALTDTR3	0C6C	_	_						AL	TDTR3<13:	:0>							0000
TRIG3	0C72							TI	RGCMP<15:0)>								0000
TRGCON3	0C74		TRGDI	V<3:0>		_	_	_	_	_	_			TRO	GSTRT<5:0)>		0000
LEBCON3	0C7A	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	_	_	_	_	BCH	BCL	BPHH	BPHL	BPLH	BPLL	0000
LEBDLY3	0C7C	_	_	_	_						LEB<11:0)>						0000
AUXCON3	0C7E	_	_	_	_		BLANK	SEL<3:0>		_	_		CHOPS	SEL<3:0>		CHOPHEN	CHOPLEN	0000

TABLE 4-16: QEI1 REGISTER MAP FOR dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
QEI1CON	01C0	QEIEN	_	QEISIDL	I	PIMOD<2:0>		IMV<	:1:0>	_		INTDIV<2:0	>	CNTPOL	GATEN	CCM-	<1:0>	0000
QEI1IOC	01C2	QCAPEN	FLTREN		QFDIV<2:0>		OUTFN	IC<1:0>	SWPAB	HOMPOL	IDXPOL	QEBPOL	QEAPOL	HOME	INDEX	QEB	QEA	000x
QEI1STAT	01C4	-	_	PCHEQIRQ	PCHEQIEN	PCLEQIRQ	PCLEQIEN	POSOVIRQ	POSOVIEN	PCIIRQ	PCIIEN	VELOVIRQ	VELOVIEN	HOMIRQ	HOMIEN	IDXIRQ	IDXIEN	0000
POS1CNTL	01C6							F	POSCNT<15	:0>								0000
POS1CNTH	01C8							P	OSCNT<31:	16>								0000
POS1HLD	01CA															0000		
VEL1CNT	01CC		VELCNT<15:0>													0000		
INT1TMRL	01CE		INTTMR<15:0>													0000		
INT1TMRH	01D0							I	NTTMR<31:	16>								0000
INT1HLDL	01D2								INTHLD<15:	0>								0000
INT1HLDH	01D4							I	NTHLD<31:	16>								0000
INDX1CNTL	01D6							II.	NDXCNT<15	:0>								0000
INDX1CNTH	01D8							II	NDXCNT<31	:16>								0000
INDX1HLD	01DA							1	NDXHLD<15	:0>								0000
QEI1GECL	01DC							(QEIGEC<15	0>								0000
QEI1ICL	01DC								QEIIC<15:0	>								0000
QEI1GECH	01DE							(QEIGEC<31:	16>								0000
QEI1ICH	01DE								QEIIC<31:10	3>								0000
QEI1LECL	01E0								QEILEC<15:	0>								0000
QEI1LECH	01E2							(QEILEC<31:	16>								0000

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, AND PIC24EPXXXGP/MC20X

TABLE 4-17: I2C1 and I2C2 REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets		
I2C1RCV	0200	_	_	_	_	_	_	_	_				Receive	Register				0000		
I2C1TRN	0202	_	_	1	-	_	_	_	_				Transmit	t Register				00FF		
I2C1BRG	0204	_	_	_	_	_	_	_				Bau	d Rate Gen	erator				0000		
I2C1CON	0206	I2CEN	_	I2CSIDL	SCLREL	IPMIEN	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000		
I2C1STAT	0208	ACKSTAT	TRSTAT	_	_	_	BCL	GCSTAT	ADD10											
I2C1ADD	020A	_	_	1	-	_	_			Address Register										
I2C1MSK	020C	_	_	_	_	_	_					Addre	ss Mask					0000		
I2C2RCV	0210	_	_	1	1	-	_	-	_				Receive	Register				0000		
I2C2TRN	0212	_	_	_	_	_	_	_	_				Transmit	t Register				00FF		
I2C2BRG	0214	_	_	_	_	_	_	_				Bau	d Rate Gen	erator				0000		
I2C2CON	0216	I2CEN	_	I2CSIDL	SCLREL	IPMIEN	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000		
I2C2STAT	0218	ACKSTAT	TRSTAT	_	_	_	BCL	GCSTAT	ADD10	110 IWCOL I2COV D_A P S R_W RBF TBF										
I2C2ADD	021A	_	_	_	_	_	_			Address Register										
I2C2MSK	021C	_	_	_	_	_	_			Address Mask										

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-18: UART1 and UART2 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
U1MODE	0220	UARTEN	_	USIDL	IREN	RTSMD	_	UEN<	:1:0>	WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSE	L<1:0>	STSEL	0000
U1STA	0222	UTXISEL1	UTXINV	UTXISEL0	_	UTXBRK	UTXEN	UTXBF	TRMT	URXIS	SEL<1:0>	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U1TXREG	0224	_	_	Transmit Register												xxxx		
U1RXREG	0226	_	_	_													0000	
U1BRG	0228							Baud	Rate Gen	erator Pre	scaler							0000
U2MODE	0230	UARTEN	1	USIDL	IREN	RTSMD	1	UEN<	:1:0>	WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSE	L<1:0>	STSEL	0000
U2STA	0232	UTXISEL1	UTXINV	UTXISEL0	_	UTXBRK	UTXEN	UTXBF	TRMT	URXIS	SEL<1:0>	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U2TXREG	0234	_	_	_	_	_	_	_				Tra	nsmit Regi	ster				xxxx
U2RXREG	0236	_	-	_	_	_	— — Receive Register											
U2BRG	0238	Baud Rate Generator Prescaler												0000				

TABLE 4-19: SPI1 and SPI2 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
SPI1STAT	0240	SPIEN	_	SPISIDL		I	9	SPIBEC<2:0	>	SRMPT	SPIROV	SRXMPT		SISEL<2:0>		SPITBF	SPIRBF	0000
SPI1CON1	0242	1	_		DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN		SPRE<2:0>		PPRE	<1:0>	0000
SPI1CON2	0244	FRMEN	SPIFSD	FRMPOL	1	1	_	_	ı	_			_		_	FRMDLY	SPIBEN	0000
SPI1BUF	0248							SPI1 Tra	nsmit and R	eceive Buff	er Register	r						0000
SPI2STAT	0260	SPIEN	-	SPISIDL	-		9	SPIBEC<2:0	>	SRMPT	SPIROV	SRXMPT		SISEL<2:0>		SPITBF	SPIRBF	0000
SPI2CON1	0262	_	_	_	DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN		SPRE<2:0>		PPRE	<1:0>	0000
SPI2CON2	0264	FRMEN	SPIFSD	FRMPOL	_		_	_	_	_		_	_	_	_	FRMDLY	SPIBEN	0000
SPI2BUF	0268														0000			

TABLE 4-20: ADC1 REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
ADC1BUF0	0300								ADC1 Data B	uffer 0								xxxx
ADC1BUF1	0302								ADC1 Data B	uffer 1								xxxx
ADC1BUF2	0304								ADC1 Data B	uffer 2								xxxx
ADC1BUF3	0306								ADC1 Data B	uffer 3								xxxx
ADC1BUF4	0308								ADC1 Data B	uffer 4								xxxx
ADC1BUF5	030A								ADC1 Data B	uffer 5								xxxx
ADC1BUF6	030C								ADC1 Data B	uffer 6								xxxx
ADC1BUF7	030E					12012 1 2 %												xxxx
ADC1BUF8	0310																	xxxx
ADC1BUF9	0312					ADC1 Data Buffer 9 xxx												xxxx
ADC1BUFA	0314					10010 1 0 % 10												xxxx
ADC1BUFB	0316								ADC1 Data B	uffer 11								xxxx
ADC1BUFC	0318								ADC1 Data Bu	uffer 12								xxxx
ADC1BUFD	031A								ADC1 Data Bu	uffer 13								xxxx
ADC1BUFE	031C								ADC1 Data Bu	uffer 14								xxxx
ADC1BUFF	031E								ADC1 Data Bu	ıffer 15								xxxx
AD1CON1	0320	ADON	_	ADSIDL	ADDMABM	_	AD12B	FOR	M<1:0>		SSRC<2:0	>	SSRCG	SIMSAM	ASAM	SAMP	DONE	0000
AD1CON2	0322	\	/CFG<2:0>	>	_	_	CSCNA	CHP	S<1:0>	BUFS			SMPI<4:0	>		BUFM	ALTS	0000
AD1CON3	0324	ADRC	_	_			SAMC<4:0	>					ADCS	S<7:0>				0000
AD1CHS123	0326	_	_	_	_	_	CH123N	NB<1:0>	CH123SB	_	_	_	_	_	CH123N	A<1:0>	CH123SA	0000
AD1CHS0	0328	CH0NB	_	_		CH0SB<4:0>											0000	
AD1CSSH	032E	CSS31	CSS30	_	_	_	CSS26	CSS25	CSS24	_	_	_	_	_	_	_	_	0000
AD1CSSL	0330	CSS15	CSS14	CSS13	CSS12	CSS11	CSS10	CSS9	CSS8	CSS7	CSS6	CSS5	CSS4	CSS3	CSS2	CSS1	CSS0	0000
AD1CON4	0332	_	_	_	_	_	_	_	ADDMAEN	-	_	_	_	_	D	MABL<2:0)>	0000

TABLE 4-21: ECAN1 REGISTER MAP WHEN WIN (C1CTRL<0>) = 0 OR 1 FOR dsPIC33EPXXXMC/GP50X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
C1CTRL1	0400	1	_	CSIDL	ABAT	CANCKS	RI	EQOP<2:0	>	OPM	MODE<2:0	>	_	CANCAP		_	WIN	0480
C1CTRL2	0402	_	_	_	_	_	_	_	_	_	_	_		D	NCNT<4:0	>	3	0000
C1VEC	0404	_	_	_		F	ILHIT<4:0>		•	_		•	I	CODE<6:0	>			0040
C1FCTRL	0406		MABS<2:0	^	FSA<4:0>									0000				
C1FIFO	0408	_	_			FBP<	5:0>	•	,	_	_			FNRB	<5:0>			0000
C1INTF	040A	_	_	TXBO	TXBP	RXBP	TXWAR	RXWAR	EWARN	IVRIF	WAKIF	ERRIF	_	FIFOIF	RBOVIF	RBIF	TBIF	0000
C1INTE	040C	_	_	1	_	_	_	_	_	IVRIE	WAKIE	ERRIE	_	FIFOIE	RBOVIE	RBIE	TBIE	0000
C1EC	040E				TERRON	T<7:0>			,				RERRCN	T<7:0>				0000
C1CFG1	0410	_	_	_	_	_	_	_	_	SJW<1	:0>			BRP<	<5:0>			0000
C1CFG2	0412	_	WAKFIL	1	_	_	SE	G2PH<2:0)>	SEG2PHTS	SAM	S	EG1PH<2:	0>	Р	RSEG<2:0)>	0000
C1FEN1	0414	FLTEN15	FLTEN14	FLTEN13	EN13 FLTEN12 FLTEN11 FLTEN10 FLTEN9 FLTEN8 FLTEN7 FLTEN6 FLTEN5 FLTEN4 FLTEN3 FLTEN2 FLTEN1 FLTEN0									FFFF				
C1FMSKSEL1	0418	F7MSł	<<1:0>	F6MSk	<<1:0>	F5MSI	K<1:0>	F4MSI	K<1:0>	F3MSK<	<1:0>	F2MSł	<<1:0>	F1MSK	<1:0>	F0MSI	K<1:0>	0000
C1FMSKSEL2	041A	F15MS	K<1:0>	F14MS	K<1:0>	F13MS	K<1:0>	F12MS	K<1:0>	F11MSK	<1:0>	F10MS	K<1:0>	F9MSK	<1:0>	F8MSI	K<1:0>	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-22: ECAN1 REGISTER MAP WHEN WIN (C1CTRL<0>) = 0 FOR dsPIC33EPXXXMC/GP50X DEVICES ONLY

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
	0400- 041E							See	definition v	when WIN =	×							
C1RXFUL1	0420	RXFUL15	RXFUL14	RXFUL13	RXFUL12	RXFUL11	RXFUL10	RXFUL9	RXFUL8	RXFUL7	RXFUL6	RXFUL5	RXFUL4	RXFUL3	RXFUL2	RXFUL1	RXFUL0	0000
C1RXFUL2	0422	RXFUL31	.15 RXFUL14 RXFUL13 RXFUL12 RXFUL11 RXFUL10 RXFUL9 RXFUL8 RXFUL7 RXFUL6 RXFUL5 RXFUL4 RXFUL4 RXFUL3 RXFUL2 RXFUL1 RXFUL1 RXFUL0 RXFUL1 RXFUL10													0000		
C1RXOVF1	0428	RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF9	RXOVF8	RXOVF7	RXOVF6	RXOVF5	RXOVF4	RXOVF3	RXOVF2	RXOVF1	RXOVF0	0000
C1RXOVF2	042A	RXOVF31	RXOVF30	RXOVF29	RXOVF28	RXOVF27	RXOVF26	RXOVF25	RXOVF24	RXOVF23	RXOVF22	RXOVF21	RXOVF20	RXOVF19	RXOVF18	RXOVF17	RXOVF16	0000
C1TR01CON	0430	TXEN1	TXABT1	TXLARB1	TXERR1	TXREQ1	RTREN1	TX1PR	I<1:0>	TXEN0	TXABAT0	TXLARB0	TXERR0	TXREQ0	RTREN0	TX0PF	RI<1:0>	0000
C1TR23CON	0432	TXEN3	TXABT3	TXLARB3	TXERR3	TXREQ3	RTREN3	TX3PR	I<1:0>	TXEN2	TXABAT2	TXLARB2	TXERR2	TXREQ2	RTREN2	TX2PF	RI<1:0>	0000
C1TR45CON	0434	TXEN5	TXABT5	TXLARB5	TXERR5	TXREQ5	RTREN5	TX5PR	I<1:0>	TXEN4	TXABAT4	TXLARB4	TXERR4	TXREQ4	RTREN4	TX4PF	RI<1:0>	0000
C1TR67CON	0436	TXEN7	TXABT7	TXLARB7	TXERR7	TXREQ7	RTREN7	TX7PR	I<1:0>	TXEN6	TXABAT6	TXLARB6	TXERR6	TXREQ6	RTREN6	TX6PF	RI<1:0>	xxxx
C1RXD	0440								Received [Data Word								xxxx
C1TXD	0442								Transmit D	ata Word								xxxx

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, AND PIC24EPXXXGP/MC20X

TABLE 4-23: ECAN1 REGISTER MAP WHEN WIN (C1CTRL<0>) = 1 FOR dsPIC33EPXXXMC/GP50X DEVICES ONLY

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
	0400- 041E								See definit	ion when W	IN = x							
C1BUFPNT1	0420		F3BF	P<3:0>			F2BF	P<3:0>			F1BP	<3:0>			F0BP	<3:0>		0000
C1BUFPNT2	0422		F7BF	P<3:0>			F6BF	P<3:0>			F5BP	<3:0>			F4BP	<3:0>		0000
C1BUFPNT3	0424		F11BI	P<3:0>			F10BI	P<3:0>			F9BP	<3:0>			F8BP	<3:0>		0000
C1BUFPNT4	0426		F15B	P<3:0>			F14BI	P<3:0>			F13BP	<3:0>			F12BP	<3:0>		0000
C1RXM0SID	0430				SID<	:10:3>					SID<2:0>		_	MIDE	_	EID<1	17:16>	xxxx
C1RXM0EID	0432				EID<	:15:8>							EID<	7:0>	•	,		xxxx
C1RXM1SID	0434				SID<	:10:3>					SID<2:0>		_	MIDE	_	EID<1	17:16>	xxxx
C1RXM1EID	0436				EID<	:15:8>							EID<	7:0>				xxxx
C1RXM2SID	0438				SID<	:10:3>					SID<2:0>		_	MIDE	_	EID<1	17:16>	xxxx
C1RXM2EID	043A				EID<	:15:8>							EID<	7:0>		•		xxxx
C1RXF0SID	0440				SID<	:10:3>					SID<2:0>		_	EXIDE	_	EID<1	17:16>	xxxx
C1RXF0EID	0442				EID<	:15:8>							EID<	7:0>	•	,		xxxx
C1RXF1SID	0444				SID<	:10:3>					SID<2:0>		_	EXIDE	_	EID<1	17:16>	xxxx
C1RXF1EID	0446				EID<	:15:8>							EID<	7:0>		•		xxxx
C1RXF2SID	0448				SID<	:10:3>					SID<2:0>		_	EXIDE	_	EID<1	17:16>	xxxx
C1RXF2EID	044A				EID<	:15:8>							EID<	7:0>				xxxx
C1RXF3SID	044C				SID<	:10:3>					SID<2:0>		_	EXIDE	_	EID<1	17:16>	xxxx
C1RXF3EID	044E				EID<	:15:8>							EID<	7:0>				xxxx
C1RXF4SID	0450				SID<	:10:3>					SID<2:0>		_	EXIDE	_	EID<1	17:16>	xxxx
C1RXF4EID	0452				EID<	:15:8>							EID<	7:0>				xxxx
C1RXF5SID	0454				SID<	:10:3>					SID<2:0>		_	EXIDE	_	EID<1	17:16>	xxxx
C1RXF5EID	0456				EID<	:15:8>							EID<	7:0>				xxxx
C1RXF6SID	0458				SID<	:10:3>					SID<2:0>		_	EXIDE	_	EID<1	17:16>	xxxx
C1RXF6EID	045A				EID<	:15:8>							EID<	7:0>				xxxx
C1RXF7SID	045C				SID<	:10:3>					SID<2:0>		_	EXIDE	_	EID<1	17:16>	xxxx
C1RXF7EID	045E				EID<	:15:8>							EID<	7:0>				xxxx
C1RXF8SID	0460				SID<	:10:3>					SID<2:0>		_	EXIDE	_	EID<1	17:16>	xxxx
C1RXF8EID	0462				EID<	:15:8>							EID<	7:0>				xxxx
C1RXF9SID	0464				SID<	:10:3>					SID<2:0>		_	EXIDE	_	EID<1	17:16>	xxxx
C1RXF9EID	0466				EID<	:15:8>							EID<	7:0>				xxxx
C1RXF10SID	0468				SID<	:10:3>					SID<2:0>		_	EXIDE	_	EID<1	17:16>	xxxx
C1RXF10EID	046A				EID<	:15:8>							EID<	7:0>				xxxx
C1RXF11SID	046C				SID<	:10:3>					SID<2:0>		_	EXIDE		EID<1	17:16>	xxxx
C1RXF11EID	046E				EID<	:15:8>							EID<	7:0>				xxxx
C1RXF12SID	0470				SID<	:10:3>					SID<2:0>		_	EXIDE	_	EID<1	17:16>	xxxx
C1RXF12EID	0472				EID<	:15:8>							EID<	7:0>				xxxx

TABLE 4-23: ECAN1 REGISTER MAP WHEN WIN (C1CTRL<0>) = 1 FOR dsPIC33EPXXXMC/GP50X DEVICES ONLY (CONTINUED)

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
C1RXF13SID	0474				SID<	10:3>					SID<2:0>		_	EXIDE	_	EID<1	7:16>	xxxx
C1RXF13EID	0476				EID<	15:8>							EID<	7:0>				xxxx
C1RXF14SID	0478				SID<	10:3>					SID<2:0>		_	EXIDE	_	EID<1	7:16>	xxxx
C1RXF14EID	047A				EID<	15:8>							EID<	7:0>				xxxx
C1RXF15SID	047C				SID<	10:3>					SID<2:0>		_	EXIDE	_	EID<1	7:16>	xxxx
C1RXF15EID	047E				EID<	15:8>							EID<	7:0>				xxxx

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, AND PIC24EPXXXGP/MC20X

TABLE 4-24: CRC REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
CRCCON1	0640	CRCEN	_	CSIDL		V	WORD<4:0)>		CRCFUL	CRCMPT	CRCISEL	CRCGO	LENDIAN	_	_	_	0000	
CRCCON2	0642	_	_	_		DWIDTH<4:0>													
CRCXORL	0644					X<15:1>													
CRCXORH	0646					X<15:1>													
CRCDATL	0648								CRC Data	Input Low V	Nord							0000	
CRCDATH	064A								CRC Data	Input High \	Word							0000	
CRCWDATL	064C								CRC Re	sult Low Wo	ord							0000	
CRCWDATH	064E								CRC Res	sult High Wo	ord					·	·	0000	

Legend: — = unimplemented, read as '0'. Shaded bits are not used in the operation of the programmable CRC module.

TABLE 4-25: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EPXXXGP/MC202/502 AND PIC24EPXXXGP/MC202 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	AII Resets
RPOR0	0680	_	_			RP35F	R<5:0>			_	_			RP20F	R<5:0>			0000
RPOR1	0682	_	_			RP37F	R<5:0>			_	_			RP36F	R<5:0>			0000
RPOR2	0684	_	_			RP39F	R<5:0>			_	_			RP38F	R<5:0>			0000
RPOR3	0686	_	_			RP41F	R<5:0>			_	_			RP40F	R<5:0>			0000
RPOR4	0688	_	_			RP43F	R<5:0>			_	_			RP42F	R<5:0>			0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-26: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EPXXXGP/MC203/503 AND PIC24EPXXXGP/MC203 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPOR0	0680	I			RP35R<5:0> — — RP20R<5:0>										0000			
RPOR1	0682	1	_													0000		
RPOR2	0684	_	_			RP39F	R<5:0>			_	_			RP38F	R<5:0>			0000
RPOR3	0686	1	_			RP41F	R<5:0>			_	_			RP40F	R<5:0>			0000
RPOR4	0688	_	_			RP43F	R<5:0>			_	_			RP42F	R<5:0>			0000
RPOR5	068A	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
RPOR6	068C	-	_											0000				

TABLE 4-27: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EPXXXGP/MC204/504 AND PIC24EPXXXGP/MC204 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPOR0	0680	_	_			RP35F	R<5:0>			_	_			RP20F	R<5:0>			0000
RPOR1	0682	-	_			RP37F	R<5:0>			_	_			RP36F	R<5:0>			0000
RPOR2	0684	-	_			RP39F	R<5:0>			_	_			RP38F	R<5:0>			0000
RPOR3	0686	1				RP41F	R<5:0>			_	_			RP40F	R<5:0>			0000
RPOR4	0688	-	_			RP43F	R<5:0>			_	_			RP42F	R<5:0>			0000
RPOR5	068A	-	_			RP55F	R<5:0>			_	_			RP54F	R<5:0>			0000
RPOR6	068C	_	_			RP57F	R<5:0>			_	_			RP56F	R<5:0>			0000

TABLE 4-28: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EPXXXGP/MC206/506 AND PIC24EPXXXGP/MC206 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPOR0	0680		_			RP35F	R<5:0>			_	_			RP20F	R<5:0>			0000
RPOR1	0682	_	_			RP37F	R<5:0>			_	_			RP36F	R<5:0>			0000
RPOR2	0684	-	_			RP39F	R<5:0>			_	_			RP38F	R<5:0>			0000
RPOR3	0686	_	_			RP41F	R<5:0>			_	_			RP40F	R<5:0>			0000
RPOR4	0688	_	_			RP43F	R<5:0>			_	_			RP42F	R<5:0>			0000
RPOR5	068A		-			RP55F	R<5:0>			_	_			RP54F	R<5:0>			0000
RPOR6	068C	-	_			RP57F	R<5:0>			_	_			RP56F	R<5:0>			0000
RPOR7	068E	_	_			RP97F	R<5:0>			_	_	_	_	_	_	_	_	0000
RPOR8	0690	_	_			RP118	R<5:0>			_	_	_	_	_	_	_	_	0000
RPOR9	0692	_	_	_	_	_	_	_	_	_	_			RP120	R<5:0>			0000

TABLE 4-29: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR PIC24EPXXXMC20X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPINR0	06A0	_				INT1R<6:0>				_		_	_	_	1		_	0000
RPINR1	06A2	_	_	_	_	_	_	_	_	_				INT2R<6:0>				0000
RPINR3	06A6	_	_	_	_	_	_	_	_	_				T2CKR<6:0>	>			0000
RPINR7	06AE	_				IC2R<6:0>				-				IC1R<6:0>				0000
RPINR8	06B0	_				IC4R<6:0>				_				IC3R<6:0>				0000
RPINR11	06B6	_	_	_	_	_	_	_	_	_			(OCFAR<6:0	>			0000
RPINR12	06B8	_				FLT2R<6:0>	•			-				FLT1R<6:0>	•			0000
RPINR14	06BC	_			(QEB1R<6:0>	>			_			(QEA1R<6:0	>			0000
RPINR15	06BE	_			Н	OME1R<6:0)>			_			I	NDX1R<6:0	>			0000
RPINR18	06C4	_	_	_	_	_	_	_	_	_			ı	J1RXR<6:0	>			0000
RPINR19	06C6	_	1	_	_	_	_	-	1	_			ı	J2RXR<6:0	>			0000
RPINR22	06CC	_			S	CK2INR<6:0)>			_				SDI2R<6:0>	•			0000
RPINR23	06CE	_	_	_	_	_	_	_	_	_				SS2R<6:0>				0000
RPINR26	06D4	_	-	_	_	_	_	_	-	_	_	_	_	_	_	_	_	0000
RPINR37	06EA	_			S	YNCI1R<6:0)>			_	_	_	_	_			_	0000
RPINR38	06EC	_			D	CMP1R<6:	0>			_	_	_	_	_	-	_	_	0000
RPINR39	06EE	_			D	CMP3R<6:	0>						D ⁻	TCMP2R<6:	0>			0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-30: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR PIC24EPXXXGP20X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPINR0	06A0	_				INT1R<6:0>				_	_	_	_	_	_	_	_	0000
RPINR1	06A2	_	_	_	_	_	_	_	_	_				INT2R<6:0>	•			0000
RPINR3	06A6	-	_	_	_	_	_	_	_	_				T2CKR<6:0>	>			0000
RPINR7	06AE	_				IC2R<6:0>				_				IC1R<6:0>				0000
RPINR8	06B0	_				IC4R<6:0>				_				IC3R<6:0>				0000
RPINR11	06B6	-	_	_	_	_	_	_	_	_			(OCFAR<6:0	>			0000
RPINR18	06C4	_	_	_	_	_	_	_	_	_				J1RXR<6:0	>			0000
RPINR19	06C6	_	_	_	_	_	_	_	_	_				J2RXR<6:0	>			0000
RPINR22	06CC	1			S	CK2INR<6:0)>			_				SDI2R<6:0>	•			0000
RPINR23	06CE	_	_	_	_	_	_	_	_	_				SS2R<6:0>				0000

TABLE 4-31: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR dsPIC33EPXXXGP50X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPINR0	06A0	_				NT1R<6:0>				_	_	_	_	_	_	_	_	0000
RPINR1	06A2	_	_	_	_	_	_	_	_	_				INT2R<6:0>				0000
RPINR3	06A6	_	_	_	_	_	_	_	_	_			-	Γ2CKR<6:0>	>			0000
RPINR7	06AE	-				IC2R<6:0>				-				IC1R<6:0>				0000
RPINR8	06B0	_				IC4R<6:0>				_				IC3R<6:0>				0000
RPINR11	06B6	_	_	_	_	_	_	_	_	_			(OCFAR<6:0	>			0000
RPINR18	06C4	-	-	_	-	-	_	_	_	-			Į	J1RXR<6:0	>			0000
RPINR19	06C6	_	_	_	_	_	_	_	_	_			l	J2RXR<6:0	>			0000
RPINR22	06CC	_			S	CK2INR<6:0)>			_				SDI2R<6:0>				0000
RPINR23	06CE	-	-	_	-	-	_	_	_	-				SS2R<6:0>				0000
RPINR26	06D4	_	_	_	_	_	_	_	_	_			(C1RXR<6:0	>			0000

TABLE 4-32: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR dsPIC33EPXXXMC50X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPINR0	06A0	_				INT1R<6:0>				_	_	_	_	_	_	_	_	0000
RPINR1	06A2	_	_	_	_	_	_	_	_	_				INT2R<6:0>				0000
RPINR3	06A6	_	_	_	_	_	_	_	_	_			-	T2CKR<6:0>	>			0000
RPINR7	06AE	_				IC2R<6:0>				_				IC1R<6:0>				0000
RPINR8	06B0	_				IC4R<6:0>				_				IC3R<6:0>				0000
RPINR11	06B6	_	_	_	_	_	_	_	_	_			(OCFAR<6:0	>			0000
RPINR12	06B8	_			•	FLT2R<6:0>				_				FLT1R<6:0>				0000
RPINR14	06BC	_			(QEB1R<6:0	>			_			(QEA1R<6:0>	>			0000
RPINR15	06BE	_			Н	OME1R<6:0)>			_			I	NDX1R<6:0	>			0000
RPINR18	06C4	_	_	_	_	_	_	_	_	_			l	J1RXR<6:0>	>			0000
RPINR19	06C6	_	_	_	_	_	_	_	_	_			l	J2RXR<6:0>	>			0000
RPINR22	06CC	_			S	CK2INR<6:0)>			_				SDI2R<6:0>				0000
RPINR23	06CE	_	_	_	_	_	_	_	_	_				SS2R<6:0>				0000
RPINR26	06D4	_	_	_	_	_	_	_	_	_			(C1RXR<6:0>	>			0000
RPINR37	06EA	_			S	YNCI1R<6:0)>			_	_	_	_	_	_	_	_	0000
RPINR38	06EC	_			D ⁻	TCMP1R<6:	0>			_	_	_	_	_	-	_	_	0000
RPINR39	06EE	_			D ⁻	TCMP3R<6:	0>			_			D	CMP2R<6:	0>			0000

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, AND PIC24EPXXXGP/MC20X

TABLE 4-33: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR dsPIC33EPXXXMC20X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPINR0	06A0	_				INT1R<6:0>				_	_	_	_	_	_	_	_	0000
RPINR1	06A2	_	_	_	_	_	_	_	_	_				INT2R<6:0>				0000
RPINR3	06A6	_	_	_	_	_	_	_	_	_				T2CKR<6:0>	>			0000
RPINR7	06AE	_				IC2R<6:0>				_				IC1R<6:0>				0000
RPINR8	06B0	_				IC4R<6:0>				_				IC3R<6:0>				0000
RPINR11	06B6	_	_	_	_	_	_	_	_	_			(OCFAR<6:0	>			0000
RPINR12	06B8	_				FLT2R<6:0>	•			_				FLT1R<6:0>	•			0000
RPINR14	06BC	_			(QEB1R<6:0	>			_			(QEA1R<6:0	>			0000
RPINR15	06BE	_			Н	OME1R<6:0)>			_			I	NDX1R<6:0	>			0000
RPINR18	06C4	_	-	_	_	_	_	_	_	_			l	J1RXR<6:0	>			0000
RPINR19	06C6	_	_	_	_	_	_	_	_	_			l	J2RXR<6:0	>			0000
RPINR22	06CC	_			S	CK2INR<6:0)>			_				SDI2R<6:0>	•			0000
RPINR23	06CE	_	-	_	_	_	_	_	_	_				SS2R<6:0>				0000
RPINR37	06EA	_			S	YNCI1R<6:0)>			_	_	_	_	_	_	_	_	0000
RPINR38	06EC	_			D	CMP1R<6:	0>			_	_	_	_	_	_	_	_	0000
RPINR39	06EE	_	·	•	D	CMP3R<6:	0>		•	_		•	D	TCMP2R<6:	0>	•		0000

TABLE 4-34: NVM REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
NVMCON	0728	WR	WREN	WRERR	NVMSIDL	_	_	_	_	_	_	_	_		NVMC	P<3:0>		0000
NVMADR	072A								NVMA	DR<15:0>								0000
NVMADRU	072C	_	_	_	_	_	_	_	_				NVMADI	R<23:16>				0000
NVMKEY	072E	1	1	-	_	-	-	_	_				NVMKE	EY<7:0>				0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-35: SYSTEM CONTROL REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	AII Resets
RCON	0740	TRAPR	IOPUWR	_	_	VREGSF	_	CM	VREGS	EXTR	SWR	SWDTEN	WDTO	SLEEP	IDLE	BOR	POR	Note 1
OSCCON	0742	_	(COSC<2:0>		_		NOSC<2:0>		CLKLOCK	IOLOCK	LOCK	_	CF	-	_	OSWEN	Note 2
CLKDIV	0744	ROI]	OOZE<2:0>		DOZEN	F	RCDIV<2:0	>	PLLPOS	T<1:0>	_		F	PLLPRE	E<4:0>		0030
PLLFBD	0746	_	_	_	_	_	_	_				PLLDI	V<8:0>					0030
OSCTUN	0748	_	_	_	_	_	_	_	_	_	_			TUN	<5:0>			0000

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, AND PIC24EPXXXGP/MC20X

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: RCON register reset values dependent on type of reset.

2: OSCCON register reset values dependent on configuration fuses, and by type of reset.

TABLE 4-36: REFERENCE CLOCK REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
REFOCON	074E	ROON	_	ROSSLP	ROSEL		RODI	V<3:0>		-	_	1	1	1	_	1	_	0000

TABLE 4-37: PMD REGISTER MAP FOR PIC24EPXXXGP20X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	AII Resets
PMD1	0760	T5MD	T4MD	T3MD	T2MD	T1MD	_	_	_	I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	_	_	AD1MD	0000
PMD2	0762	_	_	_	_	IC4MD	IC3MD	IC2MD	IC1MD	_	_	_	_	OC4MD	OC3MD	OC2MD	OC1MD	0000
PMD3	0764		_	-	-	_	CMPMD	_	_	CRCMD	_	_	_	_	-	I2C2MD	_	0000
PMD4	0766		_	_	_	_	_	_	_	_	_	_	_	REFOMD	CTMUMD	_	_	0000
PMD6	076A	_	_	_	-	_	ı	-	-	-	_	ı	_	ı		_	-	0000
													DMA0MD					
PMD7	076C	_	_	_	_	_	_	_	_	_	_	_	DMA1MD	PTGMD	_	_	_	0000
	3.50												DMA2MD	511115				0000
													DMA3MD					

TABLE 4-38: PMD REGISTER MAP FOR PIC24EPXXXMC20X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	0760	T5MD	T4MD	T3MD	T2MD	T1MD	QEI1MD	PWMMD	-	I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	_	1	AD1MD	0000
PMD2	0762	_	_	_		IC4MD	IC3MD	IC2MD	IC1MD	_	_	_	_	OC4MD	OC3MD	OC2MD	OC1MD	0000
PMD3	0764	1	_	1	1	-	CMPMD	_	1	CRCMD	-	_	_	_	_	I2C2MD	_	0000
PMD4	0766	_	_	_	_	_	_	_	_	_	_	_	_	REFOMD	CTMUMD	_	_	0000
PMD6	076A	-	_	-	ı	ı	PWM3MD	PWM2MD	PWM1MD	-	-	-	_	_	_	ı	ı	0000
PMD7	076C		_		ı	ı	ı	_	ı	_	ı	_	DMA0MD DMA1MD DMA2MD DMA3MD	PTGMD	_	ı	ı	0000

TABLE 4-39: PMD REGISTER MAP FOR dsPIC33EPXXXGP50X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	0760	T5MD	T4MD	T3MD	T2MD	T1MD	ı	-	_	I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	_	C1MD	AD1MD	0000
PMD2	0762	_	_	_	_	IC4MD	IC3MD	IC2MD	IC1MD	_	_	_	_	OC4MD	OC3MD	OC2MD	OC1MD	0000
PMD3	0764	_	_	_	_	_	CMPMD	_	_	CRCMD	_	_	_	_	_	I2C2MD	_	0000
PMD4	0766	_	_	_	_	_	-	_	_	_	_	_	_	REFOMD	CTMUMD	_	_	0000
PMD6	076A	_	_	_	_	_	-	_	_	_	_	_	_	_	_	_	_	0000
PMD7	076C	-	-	1	1	ı	_	-	_	_	1	_	DMA0MD DMA1MD DMA2MD DMA3MD	PTGMD	ı	1	_	0000

TABLE 4-40: PMD REGISTER MAP FOR dsPIC33EPXXXMC50X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	0760	T5MD	T4MD	T3MD	T2MD	T1MD	QEI1MD	PWMMD	_	I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	_	C1MD	AD1MD	0000
PMD2	0762	_	_	_	_	IC4MD	IC3MD	IC2MD	IC1MD	_	_	_	_	OC4MD	OC3MD	OC2MD	OC1MD	0000
PMD3	0764	_	_	_	_	_	CMPMD	_	_	CRCMD	_	_	_	_	_	I2C2MD	_	0000
PMD4	0766	_	_	_	_	_	_	_	_	_	_	_	_	REFOMD	CTMUMD	_	_	0000
PMD6	076A	1	_	1	-	_	PWM3MD	PWM2MD	PWM1MD	-	-	_	-	-	-	_	_	0000
													DMA0MD					
PMD7	076C	_	_	_	_	_	_	_	_	_	_	_	DMA1MD DMA2MD	PTGMD	_	_	_	0000
													DMA3MD					

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, AND PIC24EPXXXGP/MC20X

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-41: PMD REGISTER MAP FOR dsPIC33EPXXXMC20X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	0760	T5MD	T4MD	T3MD	T2MD	T1MD	QEI1MD	PWMMD	_	I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	_	_	AD1MD	0000
PMD2	0762	_	_	_	_	IC4MD	IC3MD	IC2MD	IC1MD	_	_	_	_	OC4MD	OC3MD	OC2MD	OC1MD	0000
PMD3	0764	1	_		-	-	CMPMD	_	-	CRCMD	-	-	_	_	_	I2C2MD	_	0000
PMD4	0766		_		-	_	_	_		_	1	_	_	REFOMD	CTMUMD	_	_	0000
PMD6	076A	1	_		-	-	PWM3MD	PWM2MD	PWM1MD	_	-	-	_	_	_	_	_	0000
													DMA0MD					
PMD7	076C	_	_	_	_	_	_	_	_	_	_	_	DMA1MD DMA2MD	PTGMD	_	_	_	0000
													DMA3MD					

TABLE 4-42: OP AMP/COMPARATOR REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CMSTAT	0A80	PSIDL	_	-	_	C4EVT	C3EVT	C2EVT	C1EVT	_	_	_	_	C4OUT	C3OUT	C2OUT	C1OUT	0000
CVRCON	0A82	_	CVR2OE	_	_	_	VREFSEL	_	_	CVREN	CVR10E	CVRR	CVRSS		CVR<	3:0>		0000
CM1CON	0A84	CON	COE	CPOL	_	-	OPMODE	CEVT	COUT	EVPOL	<1:0>	ı	CREF	ı	ı	CCH	<1:0>	0000
CM1MSKSRC	0A86	ı	_	ı	_		SELSR	CC<3:0>			SELSRO	B<3:0>			SELSRC	A<3:0>		0000
CM1MSKCON	0A88	HLMS	_	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
CM1FLTR	0A8A	ı	_	ı	_	_	_	ı	_	_	C	FSEL<2:0)>	CFLTREN	(CFDIV<2:0	>	0000
CM2CON	0A8C	CON	COE	CPOL	_	_	OPMODE	CEVT	COUT	EVPOL	<1:0>	1	CREF	ı	ı	CCH	<1:0>	0000
CM2MSKSRC	0A8E	ı	_	ı	_		SELSR	CC<3:0>			SELSRO	B<3:0>			SELSRC	A<3:0>		0000
CM2MSKCON	0A90	HLMS	_	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
CM2FLTR	0A92	ı	_	ı	_	_	_	ı	_	_	C	FSEL<2:0)>	CFLTREN	(CFDIV<2:0	>	0000
CM3CON	0A94	CON	COE	CPOL	_	_	OPMODE	CEVT	COUT	EVPOL	<1:0>	1	CREF	ı	ı	CCH	<1:0>	0000
CM3MSKSRC	0A96	ı	_	ı	_		SELSR	CC<3:0>			SELSRO	B<3:0>			SELSRC	A<3:0>		0000
CM3MSKCON	0A98	HLMS	_	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
CM3FLTR	0A9A	ı	_	ı	_	_	_	ı	_	_	C	FSEL<2:0)>	CFLTREN	(CFDIV<2:0	>	0000
CM4CON	0A9C	CON	COE	CPOL	_	_	_	CEVT	COUT	EVPOL	<1:0>	1	CREF	ı	ı	CCH	<1:0>	0000
CM4MSKSRC	0A9E	ı	_	ı	_		SELSR	CC<3:0>			SELSRO	B<3:0>		SELSRCA<3:0>			0000	
CM4MSKCON	0AA0	HLMS	_	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
CM4FLTR	0AA2		_	-	_	_	_	-	_	_	C	FSEL<2:0)>	CFLTREN	(CFDIV<2:0	>	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-43: CTMU REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CTMUCON1	033A	CTMUEN	_	CTMUSIDL	TGEN	EDGEN	EDGSEQEN	IDISSEN	CTTRIG	_	_	_	_	_	_	_	_	0000
CTMUCON2	033C	EDG1MOD	EDG1POL	_	_	EDG1	SEL<1:0>	EDG2STAT	EDG1STAT	EDG2MOD	EDG2POL	_	_	EDG2S	EL<1:0>	_	_	0000
CTMUICON	033E			ITRIM<	5:0>			IRNG	<1:0>	_	_	_	_	_	_	_	_	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-44: JTAG INTERFACE REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
JDATAH	0FF0	_	_	_	_						JDATAH	<27:16>						xxxx
JDATAL	0FF2	•	•	•	•	•		•	JDATAL	_<15:0>	•					•	•	0000

TABLE 4-45: DMAC REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
DMA0CON	0B00	CHEN	SIZE	DIR	HALF	NULLW	_	_	_	_	_	AMOD	E<1:0>	_	_	MODI	E<1:0>	0000	
DMA0REQ	0B02	FORCE	_	_	-	_	_	_	_				IRQSEI	L<7:0>		•		00FF	
DMA0STAL	0B04							•	STA<1	5:0>								0000	
DMA0STAH	0B06	_	_	_	_	_	_	_	_				STA<2	3:16>				0000	
DMA0STBL	0B08							•	STB<1	5:0>								0000	
DMA0STBH	0B0A	_	_	_	_	_	_	_	_				STB<2	:3:16>				0000	
DMA0PAD	0B0C								PAD<1	5:0>								0000	
DMA0CNT	0B0E	-	_							CNT<1	3:0>							0000	
DMA1CON	0B10	CHEN	SIZE	DIR	HALF	NULLW	_	_	_	_	_	AMOD	E<1:0>	_	_	MODI	E<1:0>	0000	
DMA1REQ	0B12	FORCE	_	_	-	_	_	_	_				IRQSEL	L<7:0>	•			00FF	
DMA1STAL	0B14							•	STA<1	5:0>								0000	
DMA1STAH	0B16	_	_	_	_	_	_	_	_	- STA<23:16> 0									
DMA1STBL	0B18								STB<1	STB<15:0> 0									
DMA1STBH	0B1A	_	_	_	_	_	_	_	_	STB<15:0> 00 - STB<23:16> 00									
DMA1PAD	0B1C					•		•	PAD<1	5:0>								0000	
DMA1CNT	0B1E	_	_							CNT<1	3:0>							0000	
DMA2CON	0B20	CHEN	SIZE	DIR	HALF	NULLW	_	_	_	_	_	AMOD	E<1:0>	_	_	MODI	E<1:0>	0000	
DMA2REQ	0B22	FORCE	_	_	-	_	_	_	_				IRQSEL	L<7:0>	•			00FF	
DMA2STAL	0B24								STA<1	5:0>								0000	
DMA2STAH	0B26	_	_	_	_	_	_	_	_				STA<2	3:16>				0000	
DMA2STBL	0B28								STB<1	5:0>								0000	
DMA2STBH	0B2A	1	_	_	_	_	_	_	_				STB<2	3:16>				0000	
DMA2PAD	0B2C								PAD<1	5:0>								0000	
DMA2CNT	0B2E	-	_							CNT<1	3:0>							0000	
DMA3CON	0B30	CHEN	SIZE	DIR	HALF	NULLW	_	_	_	_	_	AMOD	E<1:0>	_	_	MODI	E<1:0>	0000	
DMA3REQ	0B32	FORCE	_	_	_	_	_	_	_				IRQSEL	L<7:0>				00FF	
DMA3STAL	0B34								STA<1	5:0>								0000	
DMA3STAH	0B36	_	_	_	_	_	_	_	_				STA<2	3:16>				0000	
DMA3STBL	0B38								STB<1	5:0>								0000	
DMA3STBH	0B3A	_	_	_	_	_	_	_	_				STB<2	3:16>				0000	
DMA3PAD	0B3C					•		•	PAD<1	PAD<15:0> 0									
DMA3CNT	0B3E	_	_							CNT<13:0>									
DMAPWC	0BF0	_	_	_	_	_	_	_	_	_	_	_	_	PWCOL3	PWCOL2	PWCOL1	PWCOL0	0000	
DMARQC	0BF2	_	_	_		_	_	_	_	_	_	_	_	RQCOL3	RQCOL2	RQCOL1	RQCOL0	0000	
DMAPPS	0BF4	_	_	_	_	_	_	_	_	_	_	_	_	PPST3	PPST2	PPST1	PPST0	0000	
DMALCA	0BF6	_	-	_	1	_	_	_	_	_	_	_	_		LSTCH	l<3:0>		000F	
DSADRL	0BF8								DSADR<	15:0>								0000	
DSADRH	0BFA	_	_	_	_	_	_	_	_				DSADR<	<23:16>				0000	

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, AND PIC24EPXXXGP/MC20X

TABLE 4-46: PORTA REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	0E00	_	_	_	TRISA12	TRISA11	TRISA10	TRISA9	TRISA8	TRISA7	_	_	TRISA4	_	_	TRISA1	TRISA0	1F93
PORTA	0E02	_	_	_	RA12	RA11	RA10	RA9	RA8	RA7	_	_	RA4	_	_	RA1	RA0	0000
LATA	0E04	-	_	_	LATA12	LATA11	LATA10	LATA9	LATA8	LATA7	_	_	LATA4	1	_	LA1TA1	LA0TA0	0000
ODCA	0E06	_	_	_	ODCA12	ODCA11	ODCA10	ODCA9	ODCA8	ODCA7	_	_	ODCA4	-	_	ODCA1	ODCA0	0000
CNENA	0E08	-	_	_	CNIEA12	CNIEA11	CNIEA10	CNIEA9	CNIEA8	CNIEA7	_	_	CNIEA4	1	_	CNIEA1	CNIEA0	0000
CNPUA	0E0A	_	_	_	CNPUA12	CNPUA11	CNPUA10	CNPUA9	CNPUA8	CNPUA7	_	_	CNPUA4	_	_	CNPUA1	CNPUA0	0000
CNPDA	0E0C	_	_	_	CNPDA12	CNPDA11	CNPDA10	CNPDA9	CNPDA8	CNPDA7	_	_	CNPDA4	-	_	CNPDA1	CNPDA0	0000
ANSELA	0E0E	_		_	ANSA12	ANSA11	1	_	_	_	_	_	ANSA4		_	ANSA1	ANSA0	1813

TABLE 4-47: PORTB REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	0E10	TRISB15	TRISB14	TRISB13	TRISB12	TRISB11	TRISB10	TRISB9	TRISB8	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	FFFF
PORTB	0E12	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx
LATB	0E14	LATB15	LATB14	LATB13	LATB12	LATB11	LATB10	LATB9	LATB8	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	xxxx
ODCB	0E16	ODCB15	ODCB14	ODCB13	ODCB12	ODCB11	ODCB10	ODCB9	ODCB8	ODCB7	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCB0	0000
CNENB	0E18	CNIEB15	CNIEB14	CNIEB13	CNIEB12	CNIEB11	CNIEB10	CNIEB9	CNIEB8	CNIEB7	CNIEB6	CNIEB5	CNIEB4	CNIEB3	CNIEB2	CNIEB1	CNIEB0	0000
CNPUB	0E1A	CNPUB15	CNPUB14	CNPUB13	CNPUB12	CNPUB11	CNPUB10	CNPUB9	CNPUB8	CNPUB7	CNPUB6	CNPUB5	CNPUB4	CNPUB3	CNPUB2	CNPUB1	CNPUB0	0000
CNPDB	0E1C	CNPDB15	CNPDB14	CNPDB13	CNPDB12	CNPDB11	CNPDB10	CNPDB9	CNPDB8	CNPDB7	CNPDB6	CNPDB5	CNPDB4	CNPDB3	CNPDB2	CNPDB1	CNPDB0	0000
ANSELB	0E1E	_	_	_	_	_	_	_	ANSB8	_	_	_	_	ANSB3	ANSB2	ANSB1	ANSB0	010F

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-48: PORTC REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISC	0E20	TRISC15	_	TRISC13	TRISC12	TRISC11	TRISC10	TRISC9	TRISC8	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	BFFF
PORTC	0E22	RC15		RC13	RC12	RC11	RC10	RC9	RC8	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx
LATC	0E24	LATC15	ı	LATC13	LATC12	LATC11	LATC10	LATC9	LATC8	LATC7	LATC6	LATC5	LATC4	LATC3	LATC2	LATC1	LATC0	xxxx
ODCC	0E26	ODCC15	_	ODCC13	ODCC12	ODCC11	ODCC10	ODCC9	ODCC8	ODCC7	ODCC6	ODCC5	ODCC4	ODCC3	ODCC2	ODCC1	ODCC0	0000
CNENC	0E28	CNIEC15	_	CNIEC13	CNIEC12	CNIEC11	CNIEC10	CNIEC9	CNIEC8	CNIEC7	CNIEC6	CNIEC5	CNIEC4	CNIEC3	CNIEC2	CNIEC1	CNIEC0	0000
CNPUC	0E2A	CNPUC15	_	CNPUC13	CNPUC12	CNPUC11	CNPUC10	CNPUC9	CNPUC8	CNPUC7	CNPUC6	CNPUC5	CNPUC4	CNPUC3	CNPUC2	CNPUC1	CNPUC0	0000
CNPDC	0E2C	CNPDC15	_	CNPDC13	CNPDC12	CNPDC11	CNPDC10	CNPDC9	CNPDC8	CNPDC7	CNPDC6	CNPDC5	CNPDC4	CNPDC3	CNPDC2	CNPDC1	CNPDC0	0000
ANSELC	0E2E	-	_	_	_	ANSC11	_	_	_	_	_	_	_	_	ANSC2	ANSC1	ANSC0	0807

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TABLE 4-49: PORTD REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISD	0E30	_	_	_	_	_	_	_	TRISD8		TRISD6	TRISD5	_	_	_	_	_	0160
PORTD	0E32	_	_	_	_	_	_	_	RD8	_	RD6	RD5	_	_	_	_	_	xxxx
LATD	0E34	_	_	_	_	_	_	_	LATD8	_	LATD6	LATD5		_	_	-	_	xxxx
ODCD	0E36	_	_	_	_	_	_	_	ODCD8	_	ODCD6	ODCD5	-	_	_	_	_	0000
CNEND	0E38	_	_	_	_	_	_	_	CNIED8	_	CNIED6	CNIED5	-	_	_	_	_	0000
CNPUD	0E3A	_	_	_	_	_	_	_	CNPUD8	_	CNPUD6	CNPUD5		_	_	_	_	0000
CNPDD	0E3C	_	_	_	_	_	_		CNPDD8		CNPDD6	CNPDD5	_		_		_	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-50: PORTE REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISE	0E40	TRISE15	TRISE14	TRISE13	TRISE12	_	_	_	_	_	_	_	_	_	_	_	_	F000
PORTE	0E42	RE15	RE14	RE13	RE12	_	_	_	_	_	_	_	_	_	_	_	_	xxxx
LATE	0E44	LATE15	LATE14	LATE13	LATE12	_	_	_	_	_	_	_	_	_	_	_	_	xxxx
ODCE	0E46	ODCE15	ODCE14	ODCE13	ODCE12	-	1	1	_	-	1	_		_	1		1	0000
CNENE	0E48	CNIEE15	CNIEE14	CNIEE13	CNIEE12		_	_	_		_	_	_	_			1	0000
CNPUE	0E4A	CNPUE15	CNPUE14	CNPUE13	CNPUE12	_	_	_	_	_	_	_	_	_	-	_	-	0000
CNPDE	0E4C	CNPDE15	CNPDE14	CNPDE13	CNPDE12	_	_	_	_	_	_	_	_	_	_	_	_	0000
ANSELE	0E4E	ANSE15	ANSE14	ANSE13	ANSE12	_	_	_	_	_	_	_	_	_	_	_	_	0000

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, AND PIC24EPXXXGP/MC20X

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-51: PORTF REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISF	0E50	_	_	_	_	_	_	_	_	_	_	_	_	_	_	TRISF1	TRISF0	0173
PORTF	0E52	_	_	_	_	_	_	_	_	_	_	_	_	_	_	RF1	RF0	xxxx
LATF	0E54	_	_	_	_	_	_	_	_	_	_	_	_	_	_	LATF1	LATF0	xxxx
ODCF	0E56	_	_	_	_	_	_	_	_	_	_	_	_	_	_	ODCF1	ODCF0	0000
CNENF	0E58	_	_	_	_	_	_	_	_	_	_	_	_	_	_	CNIEF1	CNIEF0	0000
CNPUF	0E5A	_	_	_	_	_	_	_	_	_	_	_	_	_	_	CNPUF1	CNPUF0	0000
CNPDF	0E5C	_	_	_	_		_	_	_	_	_	_	_	_	_	CNPDF1	CNPDF0	0000

TABLE 4-52: PORTG REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISG	0E60	_	_	_	_	_	_	TRISG9	TRISG8	TRISG7	TRISG6	_	_	_	_	_	_	03C0
PORTG	0E62	_	_	_	_	_	_	RG9	RG8	RG7	RG6	_	_	_	_	_	_	xxxx
LATG	0E64	_	_	_	_	_	_	LATG9	LATG8	LATG7	LATG6	_	_	_	_	_	_	xxxx
ODCG	0E66	_	_	_	_	_	_	ODCG9	ODCG8	ODCG7	ODCG6	_	_	_	_	_	_	0000
CNENG	0E68	_	_	_	_	_	_	CNIEG9	CNIEG8	CNIEG7	CNIEG6	_	_	_	_	_	_	0000
CNPUG	0E6A	_	_	_	_	_	_	CNPUG9	CNPUG8	CNPUG7	CNPUG6	_	_	_	_	_	_	0000
CNPDG	0E6C	_	_	-	_	_	_	CNPDG9	CNPDG8	CNPDG7	CNPDG6	_	_	_	_	_	_	0000

TABLE 4-53: PORTA REGISTER MAP FOR PIC24EPXXXGP/MC204 AND dsPIC33EPXXXGP/MC204/504 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	0E00	_	_	_	_	_	TRISA10	TRISA9	TRISA8	TRISA7	_	_	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	079F
PORTA	0E02	_	_	_	_	_	RA10	RA9	RA8	RA7	_	_	RA4	RA3	RA2	RA1	RA0	0000
LATA	0E04		_	_	-	_	LATA10	LATA9	LATA8	LATA7	_	_	LATA4	LATA3	LATA2	LA1TA1	LA0TA0	0000
ODCA	0E06	_	_	_	_	_	ODCA10	ODCA9	ODCA8	ODCA7	_	_	ODCA4	ODCA3	ODCA2	ODCA1	ODCA0	0000
CNENA	0E08		_	_	-	_	CNIEA10	CNIEA9	CNIEA8	CNIEA7	_	_	CNIEA4	CNIEA3	CNIEA2	CNIEA1	CNIEA0	0000
CNPUA	0E0A	_	_	_	_	_	CNPUA10	CNPUA9	CNPUA8	CNPUA7	_	_	CNPUA4	CNPUA3	CNPUA2	CNPUA1	CNPUA0	0000
CNPDA	0E0C		_	_	_	1	CNPDA10	CNPDA9	CNPDA8	CNPDA7			CNPDA4	CNPDA3	CNPDA2	CNPDA1	CNPDA0	0000
ANSELA	0E0E	_	_	_	_		_	_	_	_			ANSA4		_	ANSA1	ANSA0	0013

TABLE 4-54: PORTB REGISTER MAP FOR PIC24EPXXXGP/MC204 AND dsPIC33EPXXXGP/MC204/504 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	0E10	TRISB15	TRISB14	TRISB13	TRISB12	TRISB11	TRISB10	TRISB9	TRISB8	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	FFFF
PORTB	0E12	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx
LATB	0E14	LATB15	LATB14	LATB13	LATB12	LATB11	LATB10	LATB9	LATB8	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	xxxx
ODCB	0E16	ODCB15	ODCB14	ODCB13	ODCB12	ODCB11	ODCB10	ODCB9	ODCB8	ODCB7	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCB0	0000
CNENB	0E18	CNIEB15	CNIEB14	CNIEB13	CNIEB12	CNIEB11	CNIEB10	CNIEB9	CNIEB8	CNIEB7	CNIEB6	CNIEB5	CNIEB4	CNIEB3	CNIEB2	CNIEB1	CNIEB0	0000
CNPUB	0E1A	CNPUB15	CNPUB14	CNPUB13	CNPUB12	CNPUB11	CNPUB10	CNPUB9	CNPUB8	CNPUB7	CNPUB6	CNPUB5	CNPUB4	CNPUB3	CNPUB2	CNPUB1	CNPUB0	0000
CNPDB	0E1C	CNPDB15	CNPDB14	CNPDB13	CNPDB12	CNPDB11	CNPDB10	CNPDB9	CNPDB8	CNPDB7	CNPDB6	CNPDB5	CNPDB4	CNPDB3	CNPDB2	CNPDB1	CNPDB0	0000
ANSELB	0E1E	-	_	_	-	_	_	_	ANSB8	_	_	_	-	ANSB3	ANSB2	ANSB1	ANSB0	010F

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, AND PIC24EPXXXGP/MC20X

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-55: PORTC REGISTER MAP FOR PIC24EPXXXGP/MC204 AND dsPIC33EPXXXGP/MC204/504 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISC	0E20	_	_	_	_	ı	_	TRISC9	TRISC8	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	03FF
PORTC	0E22	_	-	_	_	ı	-	RC9	RC8	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx
LATC	0E24	_	_	-	_	-	1	LATC9	LATC8	LATC7	LATC6	LATC5	LATC4	LATC3	LATC2	LATC1	LATC0	xxxx
ODCC	0E26	_	-	_	_	ı	-	ODCC9	ODCC8	ODCC7	ODCC6	ODCC5	ODCC4	ODCC3	ODCC2	ODCC1	ODCC0	0000
CNENC	0E28	_	-	_	_	_	_	CNIEC9	CNIEC8	CNIEC7	CNIEC6	CNIEC5	CNIEC4	CNIEC3	CNIEC2	CNIEC1	CNIEC0	0000
CNPUC	0E2A	_	-	_	_	_	_	CNPUC9	CNPUC8	CNPUC7	CNPUC6	CNPUC5	CNPUC4	CNPUC3	CNPUC2	CNPUC1	CNPUC0	0000
CNPDC	0E2C	_	-	_	_	_	_	CNPDC9	CNPDC8	CNPDC7	CNPDC6	CNPDC5	CNPDC4	CNPDC3	CNPDC2	CNPDC1	CNPDC0	0000
ANSELC	0E2E	_	_	_	_	_	_	_	_	_	_	_	_	_	ANSC2	ANSC1	ANSC0	0007

TABLE 4-56: PORTA REGISTER MAP FOR PIC24EPXXXGP/MC203 AND dsPIC33EPXXXGP/MC203/503 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	0E00	_	_	_	_	_	_	_	TRISA8	_	_	_	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	011F
PORTA	0E02			_	ı	_	ı	I	RA8	_	_	_	RA4	RA3	RA2	RA1	RA0	0000
LATA	0E04		_	_	_	_	_	_	LATA8	_	_	_	LATA4	LATA3	LATA2	LA1TA1	LA0TA0	0000
ODCA	0E06			_	ı	_	ı	I	ODCA8	_	_	_	ODCA4	ODCA3	ODCA2	ODCA1	ODCA0	0000
CNENA	0E08		_	_	_	_	_	_	CNIEA8	_	_	_	CNIEA4	CNIEA3	CNIEA2	CNIEA1	CNIEA0	0000
CNPUA	0E0A	_	_	_	_	_	_	_	CNPUA8	_	_	_	CNPUA4	CNPUA3	CNPUA2	CNPUA1	CNPUA0	0000
CNPDA	0E0C		_	_		_	ı	I	CNPDA8	_	_	_	CNPDA4	CNPDA3	CNPDA2	CNPDA1	CNPDA0	0000
ANSELA	0E0E	_	_	_	-	_	_		_	_	_	_	ANSA4			ANSA1	ANSA0	0013

TABLE 4-57: PORTB REGISTER MAP FOR PIC24EPXXXGP/MC203 AND dsPIC33EPXXXGP/MC203/503 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	0E10	TRISB15	TRISB14	TRISB13	TRISB12	TRISB11	TRISB10	TRISB9	TRISB8	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	FFFF
PORTB	0E12	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx
LATB	0E14	LATB15	LATB14	LATB13	LATB12	LATB11	LATB10	LATB9	LATB8	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	xxxx
ODCB	0E16	ODCB15	ODCB14	ODCB13	ODCB12	ODCB11	ODCB10	ODCB9	ODCB8	ODCB7	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCB0	0000
CNENB	0E18	CNIEB15	CNIEB14	CNIEB13	CNIEB12	CNIEB11	CNIEB10	CNIEB9	CNIEB8	CNIEB7	CNIEB6	CNIEB5	CNIEB4	CNIEB3	CNIEB2	CNIEB1	CNIEB0	0000
CNPUB	0E1A	CNPUB15	CNPUB14	CNPUB13	CNPUB12	CNPUB11	CNPUB10	CNPUB9	CNPUB8	CNPUB7	CNPUB6	CNPUB5	CNPUB4	CNPUB3	CNPUB2	CNPUB1	CNPUB0	0000
CNPDB	0E1C	CNPDB15	CNPDB14	CNPDB13	CNPDB12	CNPDB11	CNPDB10	CNPDB9	CNPDB8	CNPDB7	CNPDB6	CNPDB5	CNPDB4	CNPDB3	CNPDB2	CNPDB1	CNPDB0	0000
ANSELB	0E1E	_				_		_	ANSB8		_	_		ANSB3	ANSB2	ANSB1	ANSB0	010F

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-58: PORTC REGISTER MAP FOR PIC24EPXXXGP/MC203 AND dsPIC33EPXXXGP/MC203/503 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISC	0E20	_		ı		_	-	_	TRISC8	I	_	_	_	_	_	TRISC1	TRISC0	0107
PORTC	0E22	1	-	1	-	1	-	_	RC8	1	_	_	_	_	_	RC1	RC0	xxxx
LATC	0E24	1	-	-	-	-	_	_	LATC8	1	_	_	_	_	_	LATC1	LATC0	xxxx
ODCC	0E26	1	-	-	-	-	_	_	ODCC8	1	_	_	_	_	_	ODCC1	ODCC0	0000
CNENC	0E28	1	-	-	-	-	_	_	CNIEC8	1	_	_	_	_	_	CNIEC1	CNIEC0	0000
CNPUC	0E2A	1	-	-	-	-	_	_	CNPUC8	1	_	_	_	_	_	CNPUC1	CNPUC0	0000
CNPDC	0E2C	_	_	_	_	_	_	_	CNPDC8	_	_	_	_	_	_	CNPDC1	CNPDC0	0000
ANSELC	0E2E	_	_	_	_	_	_	_	_	_	_	_	_	_	_	ANSC1	ANSC0	0007

TABLE 4-59: PORTA REGISTER MAP FOR PIC24EPXXXGP/MC202 AND dsPIC33EPXXXGP/MC202/502 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	0E00	_	_	_	_	_	_	_	_	_	_	_	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	001C
PORTA	0E02	_	_	_	_	_	_	_	_	_	_	_	RA4	RA3	RA2	RA1	RA0	0000
LATA	0E04	-	_	_	_	_	_	_	_	_	_	_	LATA4	LATA3	LATA2	LA1TA1	LA0TA0	0000
ODCA	0E06	_	_	_	_	_	_	_	_	_	_	_	ODCA4	ODCA3	ODCA2	ODCA1	ODCA0	0000
CNENA	0E08	-	_	_	_	_	_	_	_	_	_	_	CNIEA4	CNIEA3	CNIEA2	CNIEA1	CNIEA0	0000
CNPUA	0E0A	_	_	_	_	_	_	_	_	_	_	_	CNPUA4	CNPUA3	CNPUA2	CNPUA1	CNPUA0	0000
CNPDA	0E0C	_	_	_	_	_	_	_	_	_	_	_	CNPDA4	CNPDA3	CNPDA2	CNPDA1	CNPDA0	0000
ANSELA	0E0E	-	-	_	-		_	1	_	_	_	_	ANSA4	-		ANSA1	ANSA0	0013

TABLE 4-60: PORTB REGISTER MAP FOR PIC24EPXXXGP/MC202 AND dsPIC33EPXXXGP/MC202/502 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	0E10	TRISB15	TRISB14	TRISB13	TRISB12	TRISB11	TRISB10	TRISB9	TRISB8	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	FFFF
PORTB	0E12	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx
LATB	0E14	LATB15	LATB14	LATB13	LATB12	LATB11	LATB10	LATB9	LATB8	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	xxxx
ODCB	0E16	ODCB15	ODCB14	ODCB13	ODCB12	ODCB11	ODCB10	ODCB9	ODCB8	ODCB7	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCB0	0000
CNENB	0E18	CNIEB15	CNIEB14	CNIEB13	CNIEB12	CNIEB11	CNIEB10	CNIEB9	CNIEB8	CNIEB7	CNIEB6	CNIEB5	CNIEB4	CNIEB3	CNIEB2	CNIEB1	CNIEB0	0000
CNPUB	0E1A	CNPUB15	CNPUB14	CNPUB13	CNPUB12	CNPUB11	CNPUB10	CNPUB9	CNPUB8	CNPUB7	CNPUB6	CNPUB5	CNPUB4	CNPUB3	CNPUB2	CNPUB1	CNPUB0	0000
CNPDB	0E1C	CNPDB15	CNPDB14	CNPDB13	CNPDB12	CNPDB11	CNPDB10	CNPDB9	CNPDB8	CNPDB7	CNPDB6	CNPDB5	CNPDB4	CNPDB3	CNPDB2	CNPDB1	CNPDB0	0000
ANSELB	0E1E	_	_	_	_	_	_	_	ANSB8	_	_	_	_	ANSB3	ANSB2	ANSB1	ANSB0	010F

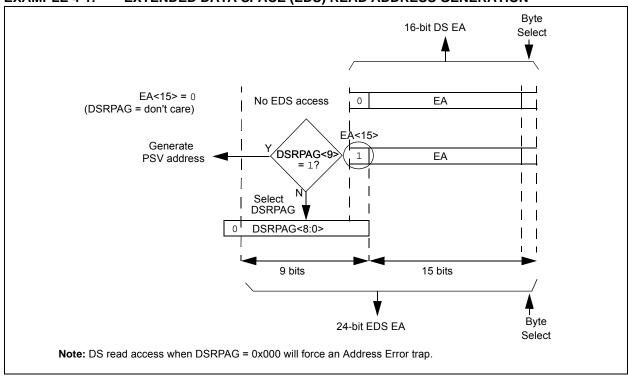
dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, AND PIC24EPXXXGP/MC20X

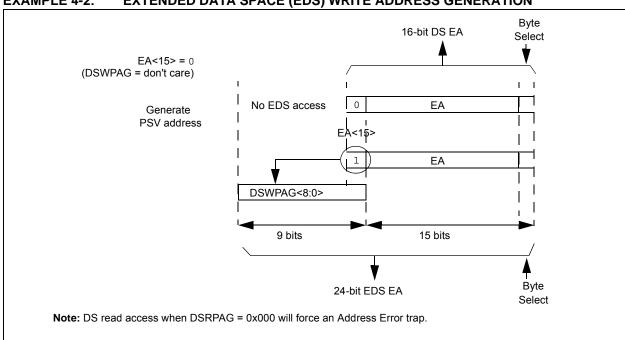
4.4.1 PAGED MEMORY SCHEME

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X architecture extends the available data space through a paging scheme, which allows the available data space to be accessed using MOV instructions in a linear fashion for pre- and post-modified effective addresses (EA). The upper half of base data space address is used in conjunction with the data space page registers, the 10-bit read page register (DSRPAG) or the 9-bit write page register (DSWPAG), to form an extended data space (EDS) address or Program Space Visibility (PSV) address. The data space page registers are located in the SFR space.

Construction of the EDS address is shown in Figure 4-1. When DSRPAG<9> = 0 and base address bit EA<15> = 1, DSRPAG<8:0> is concatenated onto EA<14:0> to form the 24-bit EDS read address. Similarly when base address bit EA<15> =1, DSWPAG<8:0> is concatenated onto EA<14:0> to form the 24-bit EDS write address.

EXAMPLE 4-1: EXTENDED DATA SPACE (EDS) READ ADDRESS GENERATION



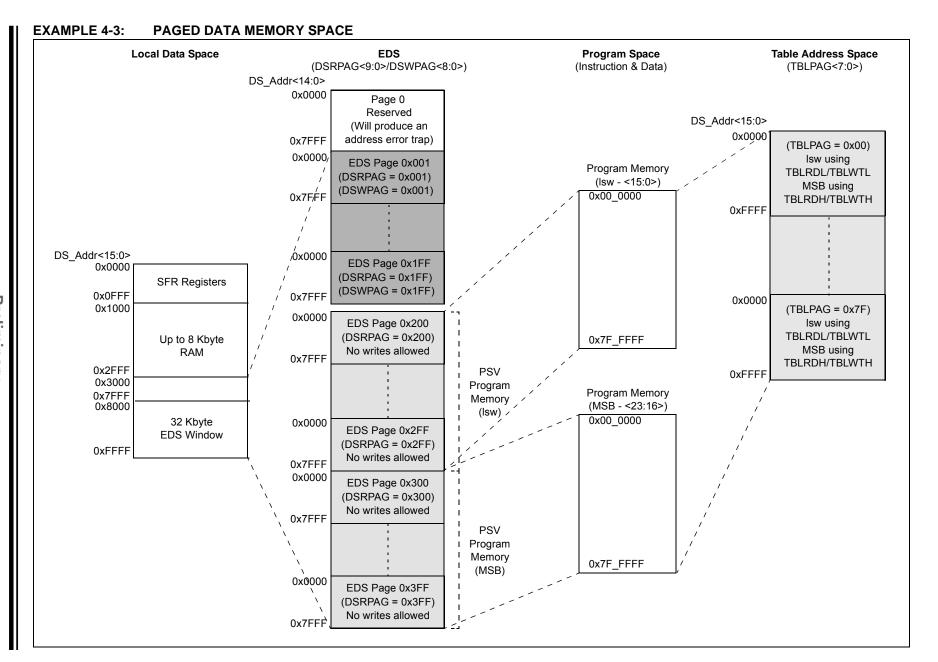


EXAMPLE 4-2: EXTENDED DATA SPACE (EDS) WRITE ADDRESS GENERATION

The paged memory scheme provides access to multiple 32-Kbyte windows in the EDS and PSV memory. The data space page registers DSxPAG, in combination with the upper half of data space address can provide up to 16 Mbytes of additional address space in the EDS and 8 Mbytes (DSRPAG only) of PSV address space. The paged data memory space is shown in Example 4-3.

The program space (PS) can be accessed with DSRPAG of 0x200 or greater. Only reads from PS are supported using the DSRPAG. Writes to PS are not supported, so DSWPAG is dedicated to DS, including EDS, only. The data space and EDS can be read from and written to using DSRPAG and DSWPAG, respectively.

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Allocating different page registers for read and write access allows the architecture to support data movement between different pages in data memory. This is accomplished by setting the DSRPAG register value to the page from which you want to read, and configuring the DSWPAG register to the page to which it needs to be written. Data can also be moved from different PSV to EDS pages, by configuring the DSRPAG and DSWPAG registers to address PSV and EDS space, respectively. The data can be moved between pages by a single instruction.

When an EDS or PSV page overflow or underflow occurs, EA<15> is cleared as a result of the register indirect EA calculation. An overflow or underflow of the EA in the EDS or PSV pages can occur at the page boundaries when:

- The initial address prior to modification addresses an EDS or PSV page
- The EA calculation uses pre- or post-modified register indirect addressing. However, this does not include register offset addressing

In general, when an overflow is detected, the DSxPAG register is incremented, and the EA<15> bit is set to keep the base address within the EDS or PSV window. When an underflow is detected, the DSxPAG register is decremented, and the EA<15> bit is set to keep the base address within the EDS or PSV window. This creates a linear EDS and PSV address space, but only when using Register Indirect Addressing modes.

Exceptions to the operation described above arise when entering and exiting the boundaries of page 0, EDS, and PSV spaces. Table 4-61 lists the effects of overflow and underflow scenarios at different boundaries.

In the following cases, when overflow or underflow occurs, the EA<15> bit is set and the DSxPAG is not modified; therefore, the EA will wrap to the beginning of the current page:

- · Register indirect with register offset addressing
- · Modulo Addressing
- · Bit-reversed addressing

TABLE 4-61: OVERFLOW AND UNDERFLOW SCENARIOS AT PAGE 0, EDS, and PSV SPACE BOUNDARIES

O/U.			Before		After				
R/W	Operation	DSxPAG	DS EA<15>	Page Description	DSxPAG	DS EA<15>	Page Description		
O, Read		DSRPAG = 0x1FF	1	EDS: Last page	DSRPAG = 0x1FF	0	See Note 1		
O, Read	[++Wn] or	DSRPAG = 0x2FF	1	PSV: Last Isw page	DSRPAG = 0x300	1	PSV: First MSB page		
O, Read	[Wn++]	DSRPAG = 0x3FF	1	PSV: Last MSB page	DSRPAG = 0x3FF	0	See Note 1		
O, Write		DSWPAG = 0x1FF	1	EDS: Last page	DSWPAG = 0x1FF	0	See Note 1		
U, Read		DSRPAG = 0x001	1	PSV page	DSRPAG = 0x001	0	See Note 1		
U, Read	[Wn] or [Wn]	DSRPAG = 0x200	1	PSV: First Isw page	DSRPAG = 0x200	0	See Note 1		
U, Read	[MII -]	DSRPAG = 0x300	1	PSV: First MSB page	DSRPAG = 0x2FF	1	PSV: Last Isw page		

Legend: O = Overflow, U = Underflow, R = Read, W = Write

- Note 1: The register indirect address now addresses a location in the base data space (0x0000-0x8000).
 - 2: An EDS access with DSxPAG = 0x000 will generate an address error trap.
 - **3:** Only reads from PS are supported using DSRPAG. An attempt to write to PS using DSWPAG will generate an address error trap.
 - **4:** Pseudo-linear addressing is not supported for large offsets.

4.4.2 EXTENDED X DATA SPACE

The lower portion of the base address space range between 0x0000 and 0x2FFF is always accessible regardless of the contents of the data space page registers. It is indirectly addressable through the register indirect instructions. It can be regarded as being located in the default EDS page 0 (i.e., EDS address range of 0x000000 to 0x002FFF with the base address bit EA<15> = 0 for this address range). However, page 0 cannot be accessed through upper 32 Kbytes, 0x8000 to 0xFFFF, of base data space in combination with DSRPAG = 0x00 or DSWPAG = 0x00. Consequently, DSRPAG and DSWPAG are initialized to 0x001 at Reset.

Note 1: DSxPAG should not be used to access page 0. An EDS access with DSxPAG set to 0x000 will generate an Address Error trap.

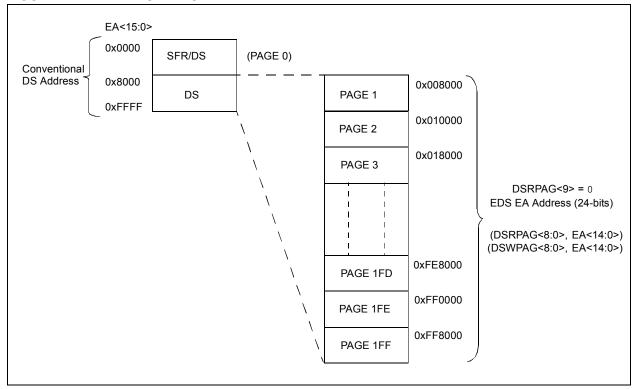
2: Clearing the DSxPAG in software has no effect.

The remaining pages including both EDS and PSV pages are only accessible using the DSRPAG or DSWPAG registers in combination with the upper 32 Kbytes, 0x8000 to 0xFFFF, of the base address, where base address bit EA<15> = 1.

For example, when DSRPAG = 0x01 or DSWPAG = 0x01, accesses to the upper 32 Kbytes, 0x8000 to 0xFFFF, of the data space will map to the EDS address range of 0x008000 to 0x00FFFF. When DSRPAG = 0x02 or DSWPAG = 0x02, accesses to the upper 32 Kbytes of the data space will map to the EDS address range of 0x010000 to 0x017FFF and so on, as shown in the EDS memory map in Figure 4-14.

For more information of the PSV page access using data space page registers refer to **4.5** "**Program Space Visibility from Data Space**" in **Section 4.** "**Program Memory**" (DS70613) of the "dsPIC33E/PIC24E Family Reference Manual".

FIGURE 4-14: EDS MEMORY MAP



4.4.3 DATA MEMORY ARBITRATION AND BUS MASTER PRIORITY

EDS accesses from bus masters in the system are arbitrated.

The arbiter for data memory (including EDS) arbitrates between the CPU, the DMA, and the ICD module. In the event of coincidental access to a bus by the bus masters, the arbiter determines which bus master access has the highest priority. The other bus masters are suspended and processed after the access of the bus by the bus master with the highest priority.

By default, the CPU is bus master 0 (M0) with the highest priority, and the ICD is bus master 4 (M4) with the lowest priority. The remaining bus masters (DMA Controllers) are allocated to M2 and M3, respectively

(M1 is reserved and cannot be used). The user application may raise or lower the priority of the masters to be above that of the CPU by setting the appropriate bits in the EDS Bus Master Priority Control (MSTRPR) register. All bus masters with raised priorities will maintain the same priority relationship relative to each other (i.e., M1 being highest and M3 being lowest with M2 in between). Also, all the bus masters with priorities below that of the CPU maintain the same priority relationship relative to each other. The priority schemes for bus masters with different MSTRPR values are tabulated in Table 4-62.

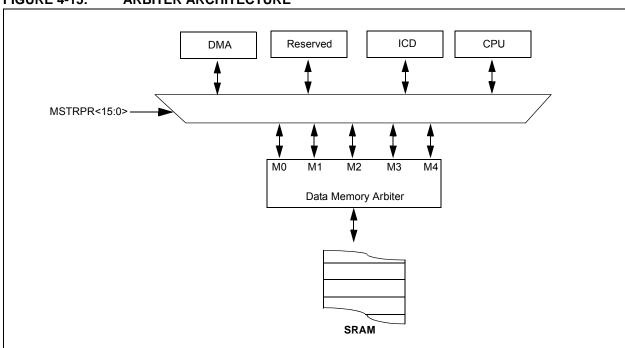
This bus master priority control allows the user application to manipulate the real-time response of the system, either statically during initialization, or dynamically in response to real-time events.

TABLE 4-62: DATA MEMORY BUS ARBITER PRIORITY

Priority	MSTRPR<15:0> Bit Setting ⁽¹⁾								
Filolity	0x0000	0x0008	0x0020	0x0028					
M0 (highest)	CPU	Reserved	DMA	Reserved					
M1	Reserved	CPU	CPU	DMA					
M2	Reserved	Reserved	Reserved	CPU					
M3	DMA	DMA	Reserved	Reserved					
M4 (lowest)	ICD	ICD	ICD	ICD					

Note 1: All other values of MSTRPR<15:0> are Reserved.

FIGURE 4-15: ARBITER ARCHITECTURE



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4.4.4 SOFTWARE STACK

The W15 register serves as a dedicated software Stack Pointer (SP) and is automatically modified by exception processing, subroutine calls and returns; however, W15 can be referenced by any instruction in the same manner as all other W registers. This simplifies reading, writing and manipulating of the Stack Pointer (for example, creating stack frames).

Note: To protect against misaligned stack accesses, W15<0> is fixed to '0' by the hardware.

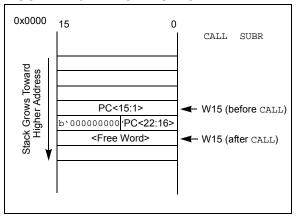
W15 is initialized to 0x1000 during all Resets. This address ensures that the SP points to valid RAM in all dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X devices and permits stack availability for non-maskable trap exceptions. These can occur before the SP is initialized by the user software. You can reprogram the SP during initialization to any location within data space.

The Stack Pointer always points to the first available free word and fills the software stack working from lower toward higher addresses. Figure 4-16 illustrates how it pre-decrements for a stack pop (read) and post-increments for a stack push (writes).

When the PC is pushed onto the stack, PC<15:0> is pushed onto the first available stack word, then PC<22:16> is pushed into the second available stack location. For a PC push during any CALL instruction, the MSB of the PC is zero-extended before the push, as shown in Figure 4-16. During exception processing, the MSB of the PC is concatenated with the lower 8 bits of the CPU STATUS register, SR. This allows the contents of SRL to be preserved automatically during interrupt processing.

- Note 1: To maintain system stack pointer (W15) coherency, W15 is never subject to (EDS) paging, and is therefore restricted to an address range of 0x0000 to 0xFFFF. The same applies to the W14 when used as a Stack Frame Pointer (SFA = 1).
 - 2: As the stack can be placed in, and can access, X and Y spaces, care must be taken regarding its use, particularly with regard to local automatic variables in a C development environment

FIGURE 4-16: CALL STACK FRAME



4.5 Instruction Addressing Modes

The addressing modes shown in Table 4-63 form the basis of the addressing modes optimized to support the specific features of individual instructions. The addressing modes provided in the MAC class of instructions differ from those in the other instruction types.

4.5.1 FILE REGISTER INSTRUCTIONS

Most file register instructions use a 13-bit address field (f) to directly address data present in the first 8192 bytes of data memory (near data space). Most file register instructions employ a working register, W0, which is denoted as WREG in these instructions. The destination is typically either the same file register or WREG (with the exception of the MUL instruction), which writes the result to a register or register pair. The MOV instruction allows additional flexibility and can access the entire data space.

4.5.2 MCU INSTRUCTIONS

The three-operand MCU instructions are of the form:

Operand 3 = Operand 1 < function > Operand 2

where Operand 1 is always a working register (that is, the addressing mode can only be Register Direct), which is referred to as Wb. Operand 2 can be a W register, fetched from data memory, or a 5-bit literal. The result location can be either a W register or a data memory location. The following addressing modes are supported by MCU instructions:

- · Register Direct
- · Register Indirect
- Register Indirect Post-Modified
- · Register Indirect Pre-Modified
- 5-bit or 10-bit Literal

Note: Not all instructions support all the addressing modes given above. Individual instructions can support different subsets of these addressing modes.

TABLE 4-63: FUNDAMENTAL ADDRESSING MODES SUPPORTED

Addressing Mode	Description
File Register Direct	The address of the file register is specified explicitly.
Register Direct	The contents of a register are accessed directly.
Register Indirect	The contents of Wn forms the Effective Address (EA).
Register Indirect Post-Modified	The contents of Wn forms the EA. Wn is post-modified (incremented or decremented) by a constant value.
Register Indirect Pre-Modified	Wn is pre-modified (incremented or decremented) by a signed constant value to form the EA.
Register Indirect with Register Offset (Register Indexed)	The sum of Wn and Wb forms the EA.
Register Indirect with Literal Offset	The sum of Wn and a literal forms the EA.

4.5.3 MOVE AND ACCUMULATOR INSTRUCTIONS

Move instructions, which apply to dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X devices, and the DSP accumulator class of instructions, which apply to the dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices, provide a greater degree of addressing flexibility than other instructions. In addition to the addressing modes supported by most MCU instructions, move and accumulator instructions also support Register Indirect with Register Offset Addressing mode, also referred to as Register Indexed mode.

Note: For the MOV instructions, the addressing mode specified in the instruction can differ for the source and destination EA. However, the 4-bit Wb (Register Offset) field is shared by both source and destination (but typically only used by one).

In summary, the following addressing modes are supported by move and accumulator instructions:

- · Register Direct
- · Register Indirect
- · Register Indirect Post-modified
- · Register Indirect Pre-modified
- · Register Indirect with Register Offset (Indexed)
- · Register Indirect with Literal Offset
- 8-bit Literal
- 16-bit Literal

Note: Not all instructions support all the addressing modes given above. Individual instructions may support different subsets of these addressing modes.

4.5.4 MAC INSTRUCTIONS (dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X DEVICES ONLY)

The dual source operand DSP instructions (CLR, ED, EDAC, MAC, MPY, MPY.N, MOVSAC and MSC), also referred to as MAC instructions, use a simplified set of addressing modes to allow the user application to effectively manipulate the data pointers through register indirect tables.

The two-source operand prefetch registers must be members of the set {W8, W9, W10, W11}. For data reads, W8 and W9 are always directed to the X RAGU, and W10 and W11 are always directed to the Y AGU. The effective addresses generated (before and after modification) must, therefore, be valid addresses within X data space for W8 and W9 and Y data space for W10 and W11.

Note: Register Indirect with Register Offset Addressing mode is available only for W9 (in X space) and W11 (in Y space).

In summary, the following addressing modes are supported by the ${\tt MAC}$ class of instructions:

- · Register Indirect
- Register Indirect Post-Modified by 2
- · Register Indirect Post-Modified by 4
- · Register Indirect Post-Modified by 6
- Register Indirect with Register Offset (Indexed)

4.5.5 OTHER INSTRUCTIONS

Besides the addressing modes outlined previously, some instructions use literal constants of various sizes. For example, BRA (branch) instructions use 16-bit signed literals to specify the branch destination directly, whereas the DISI instruction uses a 14-bit unsigned literal field. In some instructions, such as ULNK, the source of an operand or result is implied by the opcode itself. Certain operations, such as NOP, do not have any operands.

4.6 Modulo Addressing (dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X Devices Only)

Modulo Addressing mode is a method of providing an automated means to support circular data buffers using hardware. The objective is to remove the need for software to perform data address boundary checks when executing tightly looped code, as is typical in many DSP algorithms.

Modulo Addressing can operate in either data or program space (since the data pointer mechanism is essentially the same for both). One circular buffer can be supported in each of the X (which also provides the pointers into program space) and Y data spaces. Modulo Addressing can operate on any W register pointer. However, it is not advisable to use W14 or W15 for Modulo Addressing since these two registers are used as the Stack Frame Pointer and Stack Pointer, respectively.

In general, any particular circular buffer can be configured to operate in only one direction as there are certain restrictions on the buffer start address (for incrementing buffers), or end address (for decrementing buffers), based upon the direction of the buffer.

The only exception to the usage restrictions is for buffers that have a power-of-two length. As these buffers satisfy the start and end address criteria, they can operate in a bidirectional mode (that is, address boundary checks are performed on both the lower and upper address boundaries).

4.6.1 START AND END ADDRESS

The Modulo Addressing scheme requires that a starting and ending address be specified and loaded into the 16-bit Modulo Buffer Address registers: XMODSRT, XMODEND, YMODSRT and YMODEND (see Table 4-1).

Note: Y space Modulo Addressing EA calculations assume word-sized data (LSb of every EA is always clear).

The length of a circular buffer is not directly specified. It is determined by the difference between the corresponding start and end addresses. The maximum possible length of the circular buffer is 32K words (64 Kbytes).

4.6.2 W ADDRESS REGISTER SELECTION

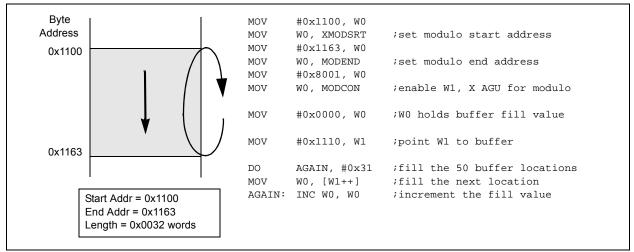
The Modulo and Bit-Reversed Addressing Control register, MODCON<15:0>, contains enable flags as well as a W register field to specify the W Address registers. The XWM and YWM fields select the registers that operate with Modulo Addressing:

- If XWM = 1111, X RAGU and X WAGU Modulo Addressing is disabled
- If YWM = 1111, Y AGU Modulo Addressing is disabled

The X Address Space Pointer W register (XWM), to which Modulo Addressing is to be applied, is stored in MODCON<3:0> (see Table 4-1). Modulo Addressing is enabled for X data space when XWM is set to any value other than '1111' and the XMODEN bit is set at MODCON<15>.

The Y Address Space Pointer W register (YWM) to which Modulo Addressing is to be applied is stored in MODCON<7:4>. Modulo Addressing is enabled for Y data space when YWM is set to any value other than '1111' and the YMODEN bit is set at MODCON<14>.

FIGURE 4-17: MODULO ADDRESSING OPERATION EXAMPLE



4.6.3 MODULO ADDRESSING APPLICABILITY

Modulo Addressing can be applied to the Effective Address (EA) calculation associated with any W register. Address boundaries check for addresses equal to:

- The upper boundary addresses for incrementing buffers
- The lower boundary addresses for decrementing buffers

It is important to realize that the address boundaries check for addresses less than or greater than the upper (for incrementing buffers) and lower (for decrementing buffers) boundary addresses (not just equal to). Address changes can, therefore, jump beyond boundaries and still be adjusted correctly.

Note:

The modulo corrected effective address is written back to the register only when Pre-Modify or Post-Modify Addressing mode is used to compute the effective address. When an address offset (such as [W7 + W2]) is used, Modulo Address correction is performed but the contents of the register remain unchanged.

4.7 Bit-Reversed Addressing (dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X Devices Only)

Bit-Reversed Addressing mode is intended to simplify data reordering for radix-2 FFT algorithms. It is supported by the X AGU for data writes only.

The modifier, which can be a constant value or register contents, is regarded as having its bit order reversed. The address source and destination are kept in normal order. Thus, the only operand requiring reversal is the modifier.

4.7.1 BIT-REVERSED ADDRESSING IMPLEMENTATION

Bit-Reversed Addressing mode is enabled in any of these situations:

- BWM bits (W register selection) in the MODCON register are any value other than '1111' (the stack cannot be accessed using Bit-Reversed Addressing)
- The BREN bit is set in the XBREV register
- The addressing mode used is Register Indirect with Pre-Increment or Post-Increment

If the length of a bit-reversed buffer is $M = 2^N$ bytes, the last 'N' bits of the data buffer start address must be zeros.

XB<14:0> is the Bit-Reversed Address modifier, or 'pivot point,' which is typically a constant. In the case of an FFT computation, its value is equal to half of the FFT data buffer size.

Note:

All bit-reversed EA calculations assume word-sized data (LSb of every EA is always clear). The XB value is scaled accordingly to generate compatible (byte) addresses.

When enabled, Bit-Reversed Addressing is executed only for Register Indirect with Pre-Increment or Post-Increment Addressing and word-sized data writes. It does not function for any other addressing mode or for byte-sized data, and normal addresses are generated instead. When Bit-Reversed Addressing is active, the W Address Pointer is always added to the address modifier (XB), and the offset associated with the Register Indirect Addressing mode is ignored. In addition, as word-sized data is a requirement, the LSb of the EA is ignored (and always clear).

Note:

Modulo addressing and bit-reversed addressing can be enabled simultaneously using the same W register, but bit-reversed addressing operation will always take precedence for data writes when enabled.

If Bit-Reversed Addressing has already been enabled by setting the BREN (XBREV<15>) bit, a write to the XBREV register should not be immediately followed by an indirect read operation using the W register that has been designated as the bit-reversed pointer.

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FIGURE 4-18: BIT-REVERSED ADDRESS EXAMPLE

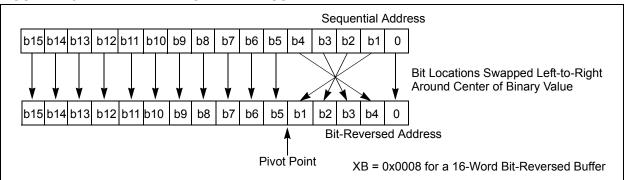


TABLE 4-64: BIT-REVERSED ADDRESS SEQUENCE (16-ENTRY)

		Norma	al Addres	ss	Bit-Reversed Address							
А3	A2	A 1	Α0	Decimal	А3	A2	A 1	Α0	Decimal			
0	0	0	0	0	0	0	0	0	0			
0	0	0	1	1	1	0	0	0	8			
0	0	1	0	2	0	1	0	0	4			
0	0	1	1	3	1	1	0	0	12			
0	1	0	0	4	0	0	1	0	2			
0	1	0	1	5	1	0	1	0	10			
0	1	1	0	6	0	1	1	0	6			
0	1	1	1	7	1	1	1	0	14			
1	0	0	0	8	0	0	0	1	1			
1	0	0	1	9	1	0	0	1	9			
1	0	1	0	10	0	1	0	1	5			
1	0	1	1	11	1	1	0	1	13			
1	1	0	0	12	0	0	1	1	3			
1	1	0	1	13	1	0	1	1	11			
1	1	1	0	14	0	1	1	1	7			
1	1	1	1	15	1	1	1	1	15			

4.8 Interfacing Program and Data Memory Spaces

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X architecture uses a 24-bit-wide program space and a 16-bit-wide data space. The architecture is also a modified Harvard scheme, meaning that data can also be present in the program space. To use this data successfully, it must be accessed in a way that preserves the alignment of information in both spaces.

Aside from normal execution, the architecture of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X devices provides two methods by which program space can be accessed during operation:

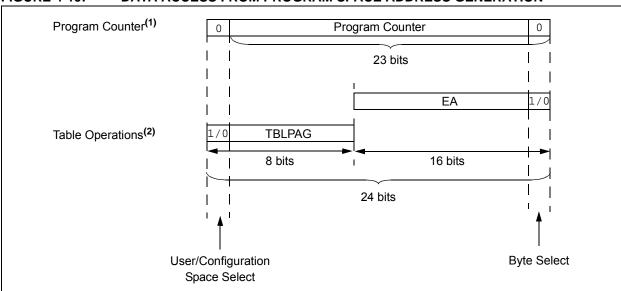
- Using table instructions to access individual bytes or words anywhere in the program space
- Remapping a portion of the program space into the data space (Program Space Visibility)

Table instructions allow an application to read or write to small areas of the program memory. This capability makes the method ideal for accessing data tables that need to be updated periodically. It also allows access to all bytes of the program word. The remapping method allows an application to access a large block of data on a read-only basis, which is ideal for look-ups from a large table of static data. The application can only access the least significant word of the program word.

TABLE 4-65: PROGRAM SPACE ADDRESS CONSTRUCTION

A T	Access	Program Space Address						
Access Type	Space	<23>	<22:16>	<15>	<14:1>	<0>		
Instruction Access	User	0 PC<22:1>						
(Code Execution)			0xx xxxx	xxx xxx	x xxxx xxx0			
TBLRD/TBLWT	User	TB	TBLPAG<7:0> Data EA					
(Byte/Word Read/Write)		0xxx xxxx xxxx xxxx xxxx						
	Configuration	TB	TBLPAG<7:0>		Data EA<15:0>			
		1	xxx xxxx	xxxx x	xxx xxxx xxxx			

FIGURE 4-19: DATA ACCESS FROM PROGRAM SPACE ADDRESS GENERATION



- **Note 1:** The Least Significant bit (LSb) of program space addresses is always fixed as '0' to maintain word alignment of data in the program and data spaces.
 - 2: Table operations are not required to be word aligned. Table read operations are permitted in the configuration memory space.

4.8.1 DATA ACCESS FROM PROGRAM MEMORY USING TABLE INSTRUCTIONS

The TBLRDL and TBLWTL instructions offer a direct method of reading or writing the lower word of any address within the program space without going through data space. The TBLRDH and TBLWTH instructions are the only method to read or write the upper 8 bits of a program space word as data.

The PC is incremented by two for each successive 24-bit program word. This allows program memory addresses to directly map to data space addresses. Program memory can thus be regarded as two 16-bit-wide word address spaces, residing side by side, each with the same address range. TBLRDL and TBLWTL access the space that contains the least significant data word. TBLRDH and TBLWTH access the space that contains the upper data byte.

Two table instructions are provided to move byte or word-sized (16-bit) data to and from program space. Both function as either byte or word operations.

- TBLRDL (Table Read Low):
 - In Word mode, this instruction maps the lower word of the program space location (P<15:0>) to a data address (D<15:0>)

- In Byte mode, either the upper or lower byte
 of the lower program word is mapped to the
 lower byte of a data address. The upper byte
 is selected when Byte Select is '1'; the lower
 byte is selected when it is '0'.
- TBLRDH (Table Read High):
 - In Word mode, this instruction maps the entire upper word of a program address (P<23:16>) to a data address. The 'phantom' byte (D<15:8>), is always '0'.
 - In Byte mode, this instruction maps the upper or lower byte of the program word to D<7:0> of the data address, in the TBLRDL instruction. The data is always '0' when the upper 'phantom' byte is selected (Byte Select = 1).

In a similar fashion, two table instructions, TBLWTH and TBLWTL, are used to write individual bytes or words to a program space address. The details of their operation are explained in **Section 5.0** "Flash Program Memory".

For all table operations, the area of program memory space to be accessed is determined by the Table Page register (TBLPAG). TBLPAG covers the entire program memory space of the device, including user application and configuration spaces. When TBLPAG<7> = 0, the table page is located in the user memory space. When TBLPAG<7> = 1, the page is located in configuration space.

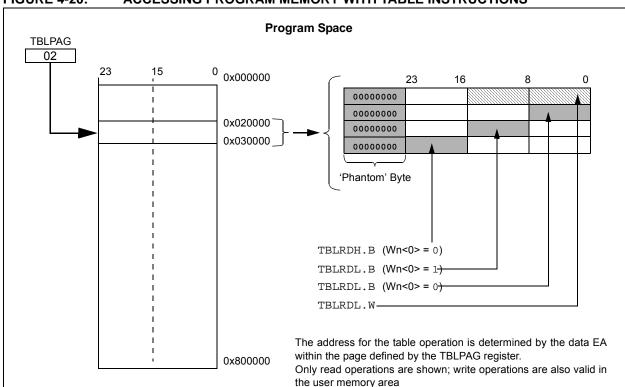


FIGURE 4-20: ACCESSING PROGRAM MEMORY WITH TABLE INSTRUCTIONS

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5.0 FLASH PROGRAM MEMORY

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 5. "Flash Programming" (DS70609) of the "dsPIC33E/PIC24E Family Reference Manual", which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X devices contain internal Flash program memory for storing and executing application code. The memory is readable, writable and erasable during normal operation over the entire VDD range.

Flash memory can be programmed in two ways:

- In-Circuit Serial Programming[™] (ICSP[™]) programming capability
- Run-Time Self-Programming (RTSP)

ICSP allows for a dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X device to be serially programmed while in the end application circuit. This is done with two lines for

programming clock and programming data (one of the alternate programming pin pairs: PGECx/PGEDx), and three other lines for power (VDD), ground (VSS) and Master Clear (MCLR). This allows customers to manufacture boards with unprogrammed devices and then program the device just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

RTSP is accomplished using TBLRD (table read) and TBLWT (table write) instructions. With RTSP, the user application can write program memory data a single program memory word, and erase program memory in blocks or 'pages' of 1024 instructions (3072 bytes) at a time.

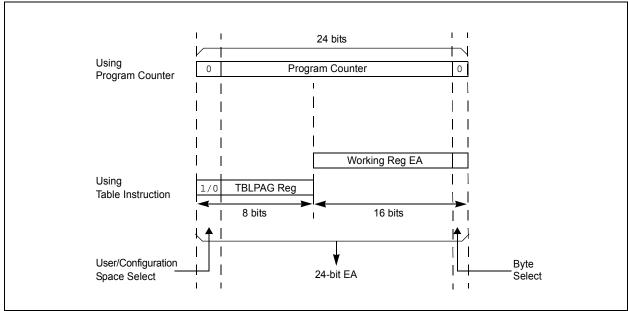
5.1 Table Instructions and Flash Programming

Regardless of the method used, all programming of Flash memory is done with the table read and table write instructions. These allow direct read and write access to the program memory space from the data memory while the device is in normal operating mode. The 24-bit target address in the program memory is formed using bits <7:0> of the TBLPAG register and the Effective Address (EA) from a W register specified in the table instruction, as shown in Figure 5-1.

The TBLRDL and the TBLWTL instructions are used to read or write to bits <15:0> of program memory. TBLRDL and TBLWTL can access program memory in both Word and Byte modes.

The TBLRDH and TBLWTH instructions are used to read or write to bits <23:16> of program memory. TBLRDH and TBLWTH can also access program memory in Word or Byte mode.

FIGURE 5-1: ADDRESSING FOR TABLE REGISTERS



5.2 RTSP Operation

RTSP allows the user application to erase a single page of memory, and to program two instruction words at a time. See the General Purpose and Motor Control Family tables (Table 1 and Table 2, respectively) for the page sizes of each device.

For more information on erasing and programming Flash memory, refer to **Section 5.** "Flash Programming" (DS70609) in the "dsPIC33E/PIC24E Family Reference Manual".

5.3 Programming Operations

A complete programming sequence is necessary for programming or erasing the internal Flash in RTSP mode. The processor stalls (waits) until the programming operation is finished.

For erase and program times, refer to parameters DI37a and DI37b (Page Erase Time), and DI38a and DI38b (Word Write Cycle Time), in Table 30-13: "DC Characteristics: Program Memory".

Setting the WR bit (NVMCON<15>) starts the operation, and the WR bit is automatically cleared when the operation is finished.

5.3.1 PROGRAMMING ALGORITHM FOR FLASH PROGRAM MEMORY

Programmers can program two adjacent words (24 bits x 2) of program Flash memory at a time on every other word address boundary (0x000002, 0x000006, 0x000000A, etc.). To do this, it is necessary to erase page that contains the desired address of the location the user wants to change.

For protection against accidental operations, the write initiate sequence for NVMKEY must be used to allow any erase or program operation to proceed. After the programming command has been executed, the user application must wait for the programming time until programming is complete. The two instructions following the start of the programming sequence should be

Refer to **Section 5. "Flash Programming"** (DS70609) in the "dsPIC33E/PIC24E Family Reference Manual" for details and codes examples on programming using RTSP.

5.4 Flash Memory Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter this URL in your browser:

http://www.microchip.com/wwwproducts/ Devices.aspx?dDocName=en555464

5.4.1 KEY RESOURCES

- Section 5. "Flash Programming" (DS70609)
- · Code Samples
- · Application Notes
- · Software Libraries
- Webinars
- All related dsPIC33E/PIC24E Family Reference Manuals Sections
- · Development Tools

5.5 Control Registers

Four SFRs are used to read and write the program Flash memory: NVMCON, NVMKEY, NVMADRU, and NVMADR.

The NVMCON register (Register 5-1) controls which blocks are to be erased, which memory type is to be programmed and the start of the programming cycle.

NVMKEY (Register 5-4) is a write-only register that is used for write protection. To start a programming or erase sequence, the user application must consecutively write 0x55 and 0xAA to the NVMKEY register.

There are two NVM address registers: NVMADRU and NVMADR. These two registers, when concatenated, form the 24-bit effective address (EA) of the selected row or word for programming operations, or the selected page for erase operations.

The NVMADRU register is used to hold the upper 8 bits of the EA, while the NVMADR register is used to hold the lower 16 bits of the EA.

REGISTER 5-1: NVMCON: NONVOLATILE MEMORY (NVM) CONTROL REGISTER

R/SO-0 ⁽¹⁾	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾	R/W-0	U-0	U-0	U-0	U-0
WR	WREN	WRERR	NVMSIDL ⁽²⁾	_	_	_	_
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾
_	_	_	_		NVMOP	<3:0> ^(3,4)	
bit 7							bit 0

Legend:	SO = Settable only bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15 WR: Write Control bit
 - 1 = Initiates a Flash memory program or erase operation. The operation is self-timed and the bit is cleared by hardware once operation is complete
 - 0 = Program or erase operation is complete and inactive
- bit 14 WREN: Write Enable bit
 - 1 = Enable Flash program/erase operations
 - 0 = Inhibit Flash program/erase operations
- bit 13 WRERR: Write Sequence Error Flag bit
 - 1 = An improper program or erase sequence attempt or termination has occurred (bit is set automatically on any set attempt of the WR bit)
 - 0 = The program or erase operation completed normally
- bit 12 **NVMSIDL:** NVM Stop-in-Idle Control bit⁽²⁾
 - 1 = Discontinue Flash operation when the device enters Idle mode
 - 0 = Continue Flash operation when the device enters Idle mode
- bit 11-4 Unimplemented: Read as '0'
- bit 3-0 **NVMOP<3:0>:** NVM Operation Select bits^(3,4)
 - 1111 = Reserved
 - 1110 = Reserved
 - 1101 = Reserved
 - 1100 = Reserved
 - 1011 = Reserved
 - 1010 = Reserved
 - 0011 = Memory page erase operation
 - 0010 = Reserved
 - 0001 = Memory double-word program operation⁽⁵⁾
 - 0000 = Reserved
- Note 1: These bits can only be reset on POR.
 - 2: If this bit is set, there will be minimal power savings (IIDLE), and upon exiting Idle mode there is a delay (TVREG) before Flash memory becomes operational.
 - 3: All other combinations of NVMOP<3:0> are unimplemented.
 - 4: Execution of the PWRSAV instruction is ignored while any of the NVM operations are in progress.
 - 5: Two adjacent words on a 4-word boundary are programmed during execution of this operation.

REGISTER 5-2: NVMADRU: NONVOLATILE MEMORY UPPER ADDRESS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	_	_	_	_	_	_	_
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x		
NVMADRU<7:0>									
bit 7							bit 0		

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **NVMADRU<7:0>:** Non-volatile Memory Upper Write Address bits

Selects the upper 8 bits of the location to program or erase in program Flash memory. This register

may be read or written by the user application.

REGISTER 5-3: NVMADR: NONVOLATILE MEMORY LOWER ADDRESS REGISTER

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
NVMADR<15:8>								
bit 15							bit 8	

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x		
NVMADR<7:0>									
bit 7							bit 0		

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **NVMADR<15:0>:** Non-volatile Memory Lower Write Address bits

Selects the lower 16 bits of the location to program or erase in program Flash memory. This register may be read or written by the user application.

REGISTER 5-4: NVMKEY: NONVOLATILE MEMORY KEY REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	_	_	_	_	_	_	_
bit 15							bit 8

W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0		
NVMKEY<7:0>									
bit 7 bit 0									

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-8 Unimplemented: Read as '0'

bit 7-0 **NVMKEY<7:0>:** Key Register (write-only) bits

6.0 RESETS

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 8. "Reset" (DS70602) of the "dsPIC33E/PIC24E Family Reference Manual", which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The Reset module combines all reset sources and controls the device Master Reset Signal, SYSRST. The following is a list of device Reset sources:

POR: Power-on Reset

· BOR: Brown-out Reset

MCLR: Master Clear Pin Reset

SWR: RESET Instruction

· WDTO: Watchdog Timer Reset

· CM: Configuration Mismatch Reset

· TRAPR: Trap Conflict Reset

· IOPUWR: Illegal Condition Device Reset

- Illegal Opcode Reset

- Uninitialized W Register Reset

- Security Reset

A simplified block diagram of the Reset module is shown in Figure 6-1.

Any active source of Reset will make the SYSRST signal active. On system Reset, some of the registers associated with the CPU and peripherals are forced to a known Reset state and some are unaffected.

Note: Refer to the specific peripheral section or **Section 4.0 "Memory Organization"** of this manual for register Reset states.

All types of device Reset sets a corresponding status bit in the RCON register to indicate the type of Reset (see Register 6-1).

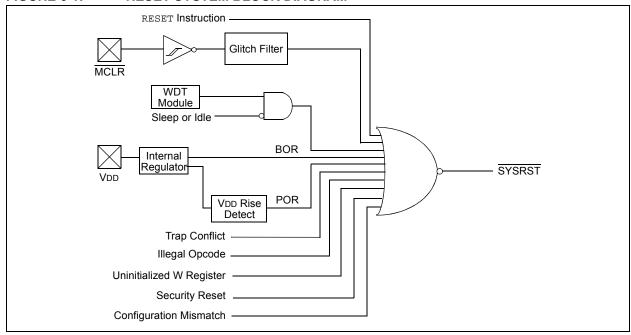
A POR clears all the bits, except for the POR and BOR bits (RCON<1:0>), that are set. The user application can set or clear any bit at any time during code execution. The RCON bits only serve as status bits. Setting a particular Reset status bit in software does not cause a device Reset to occur.

The RCON register also has other bits associated with the Watchdog Timer and device power-saving states. The function of these bits is discussed in other sections of this manual.

Note: The status bits in the RCON register should be cleared after they are read so that the next RCON register value after a device Reset is meaningful.

There are two types of Reset, a cold Reset and a warm Reset. A cold Reset is the result of a POR or BOR and the FNOSC Configuration bits in the FOSC device Configuration register select the device clock source. A warm Reset is the result of all other Resets including the RESET instruction and the Current Oscillator Selection bits (COSC<2:0>) in the Oscillator Control register (OSCCON<14:12>) select the clock source.

FIGURE 6-1: RESET SYSTEM BLOCK DIAGRAM



6.1 Reset Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:

In the event you are not able to access the product page using the link above, enter this URL in your browser:

http://www.microchip.com/wwwproducts/ Devices.aspx?dDocName=en555464

6.1.1 KEY RESOURCES

- Section 8. "Reset" (DS70602)
- · Code Samples
- · Application Notes
- · Software Libraries
- · Webinars
- All related dsPIC33E/PIC24E Family Reference Manuals Sections
- · Development Tools

REGISTER 6-1: RCON: RESET CONTROL REGISTER (1)

R/W-0	R/W-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0
TRAPR	IOPUWR	_	_	VREGSF	_	CM	VREGS
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1
EXTR	SWR	SWDTEN ⁽²⁾	WDTO	SLEEP	IDLE	BOR	POR
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15 **TRAPR:** Trap Reset Flag bit

1 = A Trap Conflict Reset has occurred

0 = A Trap Conflict Reset has not occurred

bit 14 IOPUWR: Illegal Opcode or Uninitialized W Access Reset Flag bit

1 = An illegal opcode detection, an illegal address mode or uninitialized W register used as an

Address Pointer caused a Reset

0 = An illegal opcode or uninitialized W Reset has not occurred

bit 13-12 **Unimplemented:** Read as '0'

bit 11 VREGSF: Flash Voltage Regulator Standby During Sleep bit

1 = Flash Voltage regulator is active during Sleep

0 = Flash Voltage regulator goes into Standby mode during Sleep

bit 10 **Unimplemented:** Read as '0'

bit 9 **CM:** Configuration Mismatch Flag bit

1 = A configuration mismatch Reset has occurred.0 = A configuration mismatch Reset has NOT occurred

bit 8 VREGS: Voltage Regulator Standby During Sleep bit

1 = Voltage regulator is active during Sleep

0 = Voltage regulator goes into Standby mode during Sleep

bit 7 **EXTR:** External Reset (MCLR) Pin bit

1 = A Master Clear (pin) Reset has occurred 0 = A Master Clear (pin) Reset has not occurred

bit 6 **SWR:** Software Reset (Instruction) Flag bit

1 = A RESET instruction has been executed 0 = A RESET instruction has not been executed

bit 5 **SWDTEN:** Software Enable/Disable of WDT bit⁽²⁾

1 = WDT is enabled

0 = WDT is disabled

bit 4 WDTO: Watchdog Timer Time-out Flag bit

1 = WDT time-out has occurred

0 = WDT time-out has not occurred

Note 1: All of the Reset status bits can be set or cleared in software. Setting one of these bits in software does not cause a device Reset.

2: If the FWDTEN Configuration bit is '1' (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.

REGISTER 6-1: RCON: RESET CONTROL REGISTER⁽¹⁾ (CONTINUED)

bit 3 SLEEP: Wake-up from Sleep Flag bit 1 = Device has been in Sleep mode

0 = Device has not been in Sleep mode

bit 2 IDLE: Wake-up from Idle Flag bit

1 = Device was in Idle mode0 = Device was not in Idle mode

bit 1 BOR: Brown-out Reset Flag bit

1 = A Brown-out Reset has occurred 0 = A Brown-out Reset has not occurred

bit 0 POR: Power-on Reset Flag bit

1 = A Power-on Reset has occurred 0 = A Power-on Reset has not occurred

Note 1: All of the Reset status bits can be set or cleared in software. Setting one of these bits in software does not cause a device Reset.

2: If the FWDTEN Configuration bit is '1' (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.

7.0 INTERRUPT CONTROLLER

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 6. "Interrupts" (DS70600) of the "dsPIC33E/PIC24E Family Reference Manual", which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X interrupt controller reduces the numerous peripheral interrupt request signals to a single interrupt request signal to the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X CPU.

The interrupt controller has the following features:

- Up to eight processor exceptions and software traps
- · Eight user-selectable priority levels
- Interrupt Vector Table (IVT) with a unique vector for each interrupt or exception source
- · Fixed priority within a specified user priority level
- · Fixed interrupt entry and return latencies

7.1 Interrupt Vector Table

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X Interrupt Vector Table (IVT), shown in Figure 7-1, resides in program memory, starting at location 000004h. The IVT contains seven non-maskable trap vectors and up to 114 sources of interrupt. In general, each interrupt source has its own vector. Each interrupt vector contains a 24-bit-wide address. The value programmed into each interrupt vector location is the starting address of the associated Interrupt Service Routine (ISR).

Interrupt vectors are prioritized in terms of their natural priority. This priority is linked to their position in the vector table. Lower addresses generally have a higher natural priority. For example, the interrupt associated with vector 0 takes priority over interrupts at any other vector address.

7.2 Reset Sequence

A device Reset is not a true exception because the interrupt controller is not involved in the Reset process. The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X devices clear their registers in response to a Reset, which forces the PC to zero. The device then begins program execution at location 0x000000. A GOTO instruction at the Reset address can redirect program execution to the appropriate start-up routine.

Note: Any unimplemented or unused vector locations in the IVT should be programmed with the address of a default interrupt handler routine that contains a RESET instruction.

FIGURE 7-1: dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, AND PIC24EPXXXGP/MC20X INTERRUPT VECTOR TABLE

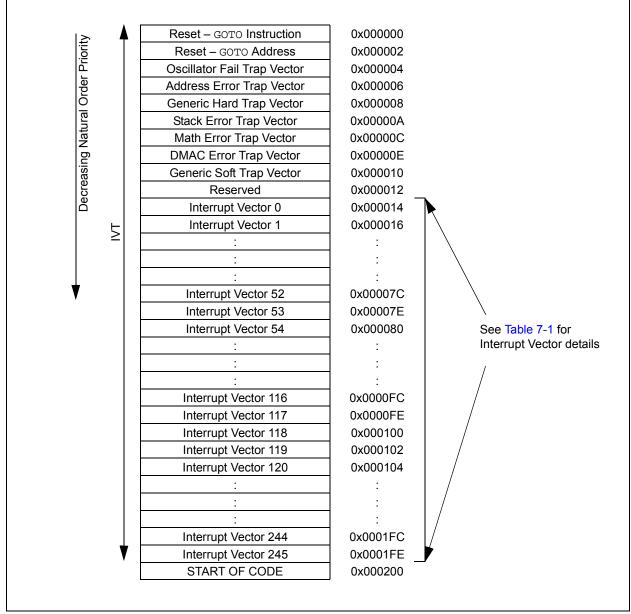


TABLE 7-1: INTERRUPT VECTOR DETAILS

Intervient Service	Vector	IDO	IVT	Inte	errupt Bit Lo	cation
Interrupt Source	Number	IRQ	Address	Flag	Enable	Priority
	Highes	t Natural O	der Priority		•	<u> </u>
INT0 – External Interrupt 0	8	0	0x000014	IFS0<0>	IEC0<0>	IPC0<2:0>
IC1 – Input Capture 1	9	1	0x000016	IFS0<1>	IEC0<1>	IPC0<6:4>
OC1 – Output Compare 1	10	2	0x000018	IFS0<2>	IEC0<2>	IPC0<10:8>
T1 – Timer1	11	3	0x00001A	IFS0<3>	IEC0<3>	IPC0<14:12>
DMA0 – DMA Channel 0	12	4	0x00001C	IFS0<4>	IEC0<4>	IPC1<2:0>
IC2 – Input Capture 2	13	5	0x00001E	IFS0<5>	IEC0<5>	IPC1<6:4>
OC2 – Output Compare 2	14	6	0x000020	IFS0<6>	IEC0<6>	IPC1<10:8>
T2 – Timer2	15	7	0x000022	IFS0<7>	IEC0<7>	IPC1<14:12>
T3 – Timer3	16	8	0x000024	IFS0<8>	IEC0<8>	IPC2<2:0>
SPI1E – SPI1 Error	17	9	0x000026	IFS0<9>	IEC0<9>	IPC2<6:4>
SPI1 – SPI1 Transfer Done	18	10	0x000028	IFS0<10>	IEC0<10>	IPC2<10:8>
U1RX – UART1 Receiver	19	11	0x00002A	IFS0<11>	IEC0<11>	IPC2<14:12>
U1TX – UART1 Transmitter	20	12	0x00002C	IFS0<12>	IEC0<12>	IPC3<2:0>
AD1 – ADC1 Convert Done	21	13	0x00002E	IFS0<13>	IEC0<13>	IPC3<6:4>
DMA1 – DMA Channel 1	22	14	0x000030	IFS0<14>	IEC0<14>	IPC3<10:8>
Reserved	23	15	0x000032	_	_	_
SI2C1 – I2C1 Slave Event	24	16	0x000034	IFS1<0>	IEC1<0>	IPC4<2:0>
MI2C1 – I2C1 Master Event	25	17	0x000036	IFS1<1>	IEC1<1>	IPC4<6:4>
CM – Comparator Combined Event	26	18	0x000038	IFS1<2>	IEC1<2>	IPC4<10:8>
CN – Input Change Interrupt	27	19	0x00003A	IFS1<3>	IEC1<3>	IPC4<14:12>
INT1 – External Interrupt 1	28	20	0x00003C	IFS1<4>	IEC1<4>	IPC5<2:0>
Reserved	29-31	21-23	0x00003E- 0x00042	_	_	_
DMA2 – DMA Channel 2	32	24	0x000044	IFS1<8>	IEC1<8>	IPC6<2:0>
OC3 – Output Compare 3	33	25	0x000046	IFS1<9>	IEC1<9>	IPC6<6:4>
OC4 – Output Compare 4	34	26	0x000048	IFS1<10>	IEC1<10>	IPC6<10:8>
T4 – Timer4	35	27	0x00004A	IFS1<11>	IEC1<11>	IPC6<14:12>
T5 – Timer5	36	28	0x00004C	IFS1<12>	IEC1<12>	IPC7<2:0>
INT2 – External Interrupt 2	37	29	0x00004E	IFS1<13>	IEC1<13>	IPC7<6:4>
U2RX – UART2 Receiver	38	30	0x000050	IFS1<14>	IEC1<14>	IPC7<10:8>
U2TX – UART2 Transmitter	39	31	0x000052	IFS1<15>	IEC1<15>	IPC7<14:12>
SPI2E – SPI2 Error	40	32	0x000054	IFS2<0>	IEC2<0>	IPC8<2:0>
SPI2 – SPI2 Transfer Done	41	33	0x000056	IFS2<1>	IEC2<1>	IPC8<6:4>
C1RX – CAN1 RX Data Ready ⁽¹⁾	42	34	0x000058	IFS2<2>	IEC2<2>	IPC8<10:8>
C1 – CAN1 Event ⁽¹⁾	43	35	0x00005A	IFS2<3>	IEC2<3>	IPC8<14:12>
DMA3 – DMA Channel 3	44	36	0x00005C	IFS2<4>	IEC2<4>	IPC9<2:0>
IC3 – Input Capture 3	45	37	0x00005E	IFS2<5>	IEC2<5>	IPC9<6:4>
IC4 – Input Capture 4	46	38	0x000060	IFS2<6>	IEC2<6>	IPC9<10:8>
Reserved	47-56	39-48	0x000062- 0x000074	_	_	_
SI2C2 – I2C2 Slave Event	57	49	0x000076	IFS3<1>	IEC3<1>	IPC12<6:4>
MI2C2 – I2C2 Master Event	58	50	0x000078	IFS3<2>	IEC3<2>	IPC12<10:8>

Note 1: This interrupt source is available on dsPIC33EPXXXGP50X and dsPIC33EPXXXMC50X devices only.

^{2:} This interrupt source is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

TABLE 7-1: INTERRUPT VECTOR DETAILS (CONTINUED)

Intermed Course	Vector	IDO	IVT	Into	errupt Bit Lo	cation
Interrupt Source	Number	IRQ	Address	Flag	Enable	Priority
Reserved	59-64	51-56	0x00007A- 0x000084	_	_	_
PSEM – PWM Special Event Match ⁽²⁾	65	57	0x000086	IFS3<9>	IEC3<9>	IPC14<6:4>
QEI1 – QEI1 Position Counter Compare ⁽²⁾	66	58	0x000088	IFS3<10>	IEC3<10>	IPC14<10:8>
Reserved	67-72	59-64	0x00008A- 0x000094	_	_	_
U1E – UART1 Error Interrupt	73	65	0x000096	IFS4<1>	IEC4<1>	IPC16<6:4>
U2E – UART2 Error Interrupt	74	66	0x000098	IFS4<2>	IEC4<2>	IPC16<10:8>
CRC – CRC Generator Interrupt	75	67	0x00009A	IFS4<3>	IEC4<3>	IPC16<14:12>
Reserved	76-77	68-69	0x00009C- 0x00009E	_	_	_
C1TX – CAN1 TX Data Request ⁽¹⁾	78	70	0x000A0	IFS4<6>	IEC4<6>	IPC17<10:8>
Reserved	79-84	71-76	0x0000A2 - 0x0000AC	-	_	
CTMU – CTMU Interrupt	85	77	0x0000AE	IFS5<13>	IEC4<13>	IPC19<6:4>
Reserved	86-101	78-93	0x0000B0- 0x0000CE	_	_	_
PWM1 – PWM Generator 1 ⁽²⁾	102	94	0x0000D0	IFS5<14>	IEC5<14>	IPC23<10:8>
PWM2 – PWM Generator 2 ⁽²⁾	103	95	0x0000D2	IFS5<15>	IEC5<15>	IPC23<14:12>
PWM3 – PWM Generator 3 ⁽²⁾	104	96	0x0000D4	IFS6<0>	IEC6<0>	IPC24<2:0>
Reserved	105-149	97-141	0x0001D6 - 0x00012E	_	_	_
ICD – ICD Application	150	142	0x000142	IFS8<14>	IEC8<14>	IPC35<10:8>
JTAG – JTAG Programming	151	143	0x000130	IFS8<15>	IEC8<15>	IPC35<14:12>
Reserved	152	144	0x000134	_	_	_
PTGSTEP – PTG Step	153	145	0x000136	IFS9<1>	IEC9<1>	IPC36<6:4>
PTGWDT – PTG Watchdog Time-out	154	146	0x000138	IFS9<2>	IEC9<2>	IPC36<10:8>
PTG0 – PTG Interrupt 0	155	147	0x00013A	IFS9<3>	IEC9<3>	IPC36<14:12>
PTG1 – PTG Interrupt 1	156	148	0x00013C	IFS9<4>	IEC9<4>	IPC37<2:0>
PTG2 – PTG Interrupt 2	157	149	0x00013E	IFS9<5>	IEC9<5>	IPC37<6:4>
PTG3 – PTG Interrupt 3	158	150	0x000140	IFS9<6>	IEC9<6>	IPC37<10:8>
Reserved	159-245	151-245	0x000142- 0x0001FE	_	_	_
	Lowes	t Natural Or	der Priority			

Note 1: This interrupt source is available on dsPIC33EPXXXGP50X and dsPIC33EPXXXMC50X devices only.

^{2:} This interrupt source is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

7.3 Interrupt Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:

In the event you are not able to access the product page using the link above, enter this URL in your browser:

http://www.microchip.com/wwwproducts/ Devices.aspx?dDocName=en555464

7.3.1 KEY RESOURCES

- Section 6. "Interrupts" (DS70600)
- · Code Samples
- · Application Notes
- · Software Libraries
- Webinars
- All related dsPIC33E/PIC24E Family Reference Manuals Sections
- · Development Tools

7.4 Interrupt Control and Status Registers

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X devices implement the following registers for the interrupt controller:

- INTCON1
- INTCON2
- INTCON3
- INTCON4
- INTTREG

7.4.1 INTCON1 THROUGH INTCON4

Global interrupt control functions are controlled from INTCON1, INTCON2, INTCON3 and INTCON4.

INTCON1 contains the Interrupt Nesting Disable bit (NSTDIS) as well as the control and status flags for the processor trap sources.

The INTCON2 register controls external interrupt request signal behavior and the use of the alternate vector table. This register also contains the General Interrupt Enable bit (GIE).

INTCON3 contains the status flags for the DMA, and DO stack overflow status trap sources.

The INTCON4 register contains the software generated hard trap status bit (SGHT).

7.4.2 IFSx

The IFS registers maintain all of the interrupt request flags. Each source of interrupt has a status bit, which is set by the respective peripherals or external signal and is cleared via software.

7.4.3 IECx

The IEC registers maintain all of the interrupt enable bits. These control bits are used to individually enable interrupts from the peripherals or external signals.

7.4.4 IPCx

The IPC registers are used to set the interrupt priority level for each source of interrupt. Each user interrupt source can be assigned to one of eight priority levels.

7.4.5 INTTREG

The INTTREG register contains the associated interrupt vector number and the new CPU interrupt priority level, which are latched into vector number (VECNUM<6:0>) and Interrupt level bit (ILR<3:0>) fields in the INTTREG register. The new interrupt priority level is the priority of the pending interrupt.

The interrupt sources are assigned to the IFSx, IECx and IPCx registers in the same sequence as they are listed in Table 7-1. For example, the INT0 (External Interrupt 0) is shown as having vector number 8 and a natural order priority of 0. Thus, the INT0IF bit is found in IFS0<0>, the INT0IE bit in IEC0<0> and the INT0IP bits in the first position of IPC0 (IPC0<2:0>).

7.4.6 STATUS/CONTROL REGISTERS

Although these registers are not specifically part of the interrupt control hardware, two of the CPU Control registers contain bits that control interrupt functionality. For more information on these registers refer to **Section 2.** "CPU" (DS70359) in the "dsPIC33E/PIC24E Family Reference Manual".

- The CPU STATUS register, SR, contains the IPL<2:0> bits (SR<7:5>). These bits indicate the current CPU interrupt priority level. The user software can change the current CPU priority level by writing to the IPL bits.
- The CORCON register contains the IPL3 bit which, together with IPL<2:0>, also indicates the current CPU priority level. IPL3 is a read-only bit so that trap events cannot be masked by the user software.

All Interrupt registers are described in Register 7-3 through Register 7-7 in the following pages.

REGISTER 7-1: SR: CPU STATUS REGISTER⁽¹⁾

R/W-0	R/W-0	R/W-0	R/W-0	R/C-0	R/C-0	R -0	R/W-0
OA	ОВ	SA	SB	OAB	SAB	DA	DC
bit 15							bit 8

R/W-0 ⁽³⁾	R/W-0 ⁽³⁾	R/W-0 ⁽³⁾	R-0	R/W-0	R/W-0	R/W-0	R/W-0
	IPL<2:0> ⁽²⁾		RA	N	OV	Z	С
bit 7							bit 0

Legend:		U = Unimplemented bit	U = Unimplemented bit, read as '0'			
R = Readable bit	W = Writable bit	C = Clearable bit				
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown			

bit 7-5 IPL<2:0>: CPU Interrupt Priority Level Status bits^(2,3)

111 = CPU Interrupt Priority Level is 7 (15). User interrupts disabled

110 = CPU Interrupt Priority Level is 6 (14)

101 = CPU Interrupt Priority Level is 5 (13)

100 = CPU Interrupt Priority Level is 4 (12)

011 = CPU Interrupt Priority Level is 3 (11)

010 = CPU Interrupt Priority Level is 2 (10)

001 = CPU Interrupt Priority Level is 1 (9)

000 = CPU Interrupt Priority Level is 0 (8)

Note 1: For complete register details, see Register 3-1.

- 2: The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL, if IPL<3> = 1. User interrupts are disabled when IPL<3> = 1.
- 3: The IPL<2:0> Status bits are read-only when the NSTDIS bit (INTCON1<15>) = 1.

REGISTER 7-2: CORCON: CORE CONTROL REGISTER⁽¹⁾

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0
VAR	_	US<	1:0>	EDT		DL<2:0>	
bit 15							bit 8

R/W-0	R/W-0	R/W-1	R/W-0	R/C-0	R-0	R/W-0	R/W-0
SATA	SATB	SATDW	ACCSAT	IPL3 ⁽²⁾	SFA	RND	IF
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15 VAR: Variable Exception Processing Latency Control bit

1 = Variable exception processing enabled0 = Fixed exception processing enabled

bit 3 IPL3: CPU Interrupt Priority Level Status bit 3⁽²⁾

1 = CPU interrupt priority level is greater than 7

0 = CPU interrupt priority level is 7 or less

Note 1: For complete register details, see Register 3-2.

2: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

REGISTER 7-3: INTCON1: INTERRUPT CONTROL REGISTER 1

W = Writable bit

'1' = Bit is set

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NSTDIS	OVAERR ⁽¹⁾	OVBERR ⁽¹⁾	COVAERR ⁽¹⁾	COVBERR ⁽¹⁾	OVATE ⁽¹⁾	OVBTE ⁽¹⁾	COVTE ⁽¹⁾
bit 15	•						bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
SFTACERR ⁽¹⁾	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL	_
bit 7							bit 0

U = Unimplemented bit, read as '0'

x = Bit is unknown

'0' = Bit is cleared

bit 15	NSTDIS: Interrupt Nesting Disable bit 1 = Interrupt nesting is disabled 0 = Interrupt nesting is enabled
bit 14	OVAERR: Accumulator A Overflow Trap Flag bit ⁽¹⁾ 1 = Trap was caused by overflow of Accumulator A 0 = Trap was not caused by overflow of Accumulator A
bit 13	OVBERR: Accumulator B Overflow Trap Flag bit ⁽¹⁾ 1 = Trap was caused by overflow of Accumulator B 0 = Trap was not caused by overflow of Accumulator B
bit 12	COVAERR: Accumulator A Catastrophic Overflow Trap Flag bit ⁽¹⁾ 1 = Trap was caused by catastrophic overflow of Accumulator A 0 = Trap was not caused by catastrophic overflow of Accumulator A
bit 11	COVBERR: Accumulator B Catastrophic Overflow Trap Flag bit ⁽¹⁾ 1 = Trap was caused by catastrophic overflow of Accumulator B 0 = Trap was not caused by catastrophic overflow of Accumulator B
bit 10	OVATE: Accumulator A Overflow Trap Enable bit ⁽¹⁾ 1 = Trap overflow of Accumulator A 0 = Trap is disabled
bit 9	OVBTE: Accumulator B Overflow Trap Enable bit ⁽¹⁾ 1 = Trap overflow of Accumulator B 0 = Trap is disabled
bit 8	COVTE: Catastrophic Overflow Trap Enable bit ⁽¹⁾ 1 = Trap on catastrophic overflow of Accumulator A or B enabled 0 = Trap is disabled
bit 7	SFTACERR: Shift Accumulator Error Status bit ⁽¹⁾ 1 = Math error trap was caused by an invalid accumulator shift 0 = Math error trap was not caused by an invalid accumulator shift
bit 6	DIV0ERR: Divide-by-zero Error Status bit 1 = Math error trap was caused by a divide by zero 0 = Math error trap was not caused by a divide by zero

DMACERR: DMAC Trap Flag bit 1 = DMAC trap has occurred 0 = DMAC trap has not occurred

MATHERR: Math Error Status bit 1 = Math error trap has occurred 0 = Math error trap has not occurred

Note 1: This bit is available on dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only.

bit 5

bit 4

Legend:

R = Readable bit

-n = Value at POR

REGISTER 7-3: INTCON1: INTERRUPT CONTROL REGISTER 1 (CONTINUED)

bit 3 ADDRERR: Address Error Trap Status bit 1 = Address error trap has occurred 0 = Address error trap has not occurred bit 2 STKERR: Stack Error Trap Status bit 1 = Stack error trap has occurred 0 = Stack error trap has not occurred bit 1 **OSCFAIL:** Oscillator Failure Trap Status bit 1 = Oscillator failure trap has occurred 0 = Oscillator failure trap has not occurred Unimplemented: Read as '0'

bit 0

Note 1: This bit is available on dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only.

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REGISTER 7-4: INTCON2: INTERRUPT CONTROL REGISTER 2

R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
GIE	DISI	SWTRAP	_	_	_	_	_
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
_	_	_	_	_	INT2EP	INT1EP	INT0EP
bit 7							bit 0

Legena:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15 GIE: Global Interrupt Enable bit

1 = Interrupts and Associated IE bits are enabled

0 = Interrupts are disabled, but traps are still enabled

bit 14 DISI: DISI Instruction Status bit

1 = DISI instruction is active 0 = DISI instruction is not active

bit 13 SWTRAP: Software Trap Status bit

1 = Software trap is enabled

0 = Software trap is disabled

bit 12-3 **Unimplemented:** Read as '0'

bit 2 INT2EP: External Interrupt 2 Edge Detect Polarity Select bit

1 = Interrupt on negative edge0 = Interrupt on positive edge

bit 1 INT1EP: External Interrupt 1 Edge Detect Polarity Select bit

1 = Interrupt on negative edge0 = Interrupt on positive edge

bit 0 INT0EP: External Interrupt 0 Edge Detect Polarity Select bit

1 = Interrupt on negative edge0 = Interrupt on positive edge

REGISTER 7-5: INTCON3: INTERRUPT CONTROL REGISTER 3

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	_	_	_	_	_	_	_
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
_	_	DAE	DOOVR	_	_	_	_
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-6 **Unimplemented:** Read as '0'

bit 5 DAE: DMA Address Error Soft Trap Status bit

1 = DMA Address error soft trap has occurred

0 = DMA Address error soft trap has not occurred

bit 4 DOOVR: Do Stack Overflow Soft Trap Status bit

1 = Do stack overflow soft trap has occurred

0 = Do stack overflow soft trap has not occurred

bit 3-0 **Unimplemented:** Read as '0'

REGISTER 7-6: INTCON4: INTERRUPT CONTROL REGISTER 4

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	_	_	_	_	_	_	_
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
_	_	_	_	_	_	_	SGHT
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-1 **Unimplemented:** Read as '0'

bit 0 SGHT: Software Generated Hard Trap Status bit

1 = Software generated hard trap has occurred

0 = Software generated hard trap has not occurred

REGISTER 7-7: INTTREG: INTERRUPT CONTROL AND STATUS REGISTER

U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
_	_	_	_		ILR<	3:0>	
bit 15							bit 8

U-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
_				VECNUM<7:0	>		
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-12 **Unimplemented:** Read as '0'

bit 11-8 ILR<3:0>: New CPU Interrupt Priority Level bits

1111 = CPU Interrupt Priority Level is 15

•

0001 = CPU Interrupt Priority Level is 1 0000 = CPU Interrupt Priority Level is 0

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **VECNUM<6:0>:** Vector Number of Pending Interrupt bits

1111111 = Interrupt vector pending is number 127

•

.

0000001 = Interrupt vector pending is number 9 0000000 = Interrupt vector pending is number 8

8.0 DIRECT MEMORY ACCESS (DMA)

Note 1: This data sheet summarizes the features dsPIC33EPXXXGP50X. the dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 22. "Direct Memory Access (DMA)" (DS70348) of the "dsPIC33E/PIC24E Family Reference Manual', which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The DMA controller transfers data between peripheral data registers and data space SRAM

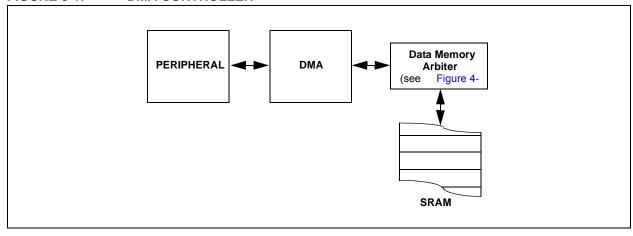
In addition, DMA can access the entire data memory space. The Data Memory Bus Arbiter is utilized when either the CPU or DMA attempt to access SRAM, resulting in potential DMA or CPU stalls.

The DMA controller supports 4 independent channels. Each channel can be configured for transfers to or from selected peripherals. Some of the peripherals supported by the DMA controller include:

- ECAN™
- Analog-to-Digital Converter (ADC)
- · Serial Peripheral Interface (SPI)
- UART
- · Input Capture
- · Output Compare

Refer to Table 8-1 for a complete list of supported peripherals.

FIGURE 8-1: DMA CONTROLLER



In addition, DMA transfers can be triggered by Timers as well as external interrupts. Each DMA channel is unidirectional. Two DMA channels must be allocated to read and write to a peripheral. If more than one channel receive a request to transfer data, a simple fixed priority scheme, based on channel number, dictates which channel completes the transfer and which channel, or channels, are left pending. Each DMA channel moves a block of data, after which it generates an interrupt to the CPU to indicate that the block is available for processing.

The DMA controller provides these functional capabilities:

- · Four DMA channels
- Register Indirect With Post-increment Addressing mode
- Register Indirect Without Post-increment Addressing mode

- Peripheral Indirect Addressing mode (peripheral generates destination address)
- CPU interrupt after half or full-block transfer complete
- · Byte or word transfers
- · Fixed priority channel arbitration
- Manual (software) or Automatic (peripheral DMA requests) transfer initiation
- · One-Shot or Auto-Repeat block transfer modes
- Ping-Pong mode (automatic switch between two SRAM start addresses after each block transfer complete)
- DMA request for each channel can be selected from any supported interrupt source
- Debug support features

The peripherals that can utilize DMA are listed in Table 8-1.

TABLE 8-1: DMA CHANNEL TO PERIPHERAL ASSOCIATIONS

Peripheral to DMA Association	DMAxREQ Register IRQSEL<7:0> Bits	DMAxPAD Register (Values to Read from Peripheral)	DMAxPAD Register (Values to Write to Peripheral)
INT0 – External Interrupt 0	0000000	_	_
IC1 – Input Capture 1	0000001	0x0144 (IC1BUF)	_
IC2 – Input Capture 2	00000101	0x014C (IC2BUF)	
IC3 – Input Capture 3	00100101	0x0154 (IC3BUF)	_
IC4 – Input Capture 4	00100110	0x015C (IC4BUF)	_
OC1 – Output Compare 1	0000010	_	0x0906 (OC1R) 0x0904 (OC1RS)
OC2 – Output Compare 2	00000110	_	0x0910 (OC2R) 0x090E (OC2RS)
OC3 – Output Compare 3	00011001	_	0x091A (OC3R) 0x0918 (OC3RS)
OC4 – Output Compare 4	00011010	_	0x0924 (OC4R) 0x0922 (OC4RS)
TMR2 – Timer2	00000111	_	
TMR3 – Timer3	00001000	_	
TMR4 – Timer4	00011011	_	1
TMR5 – Timer5	00011100	_	
SPI1 Transfer Done	00001010	0x0248 (SPI1BUF)	0x0248 (SPI1BUF)
SPI2 Transfer Done	00100001	0x0268 (SPI2BUF)	0x0268 (SPI2BUF)
UART1RX – UART1 Receiver	00001011	0x0226 (U1RXREG)	
UART1TX – UART1 Transmitter	00001100	_	0x0224 (U1TXREG)
UART2RX – UART2 Receiver	00011110	0x0236 (U2RXREG)	
UART2TX – UART2 Transmitter	00011111	_	0x0234 (U2TXREG)
ECAN1 – RX Data Ready	00100010	0x0440 (C1RXD)	_
ECAN1 – TX Data Request	01000110	_	0x0442 (C1TXD)
ADC1 – ADC1 Convert Done	00001101	0x0300 (ADC1BUF0)	_

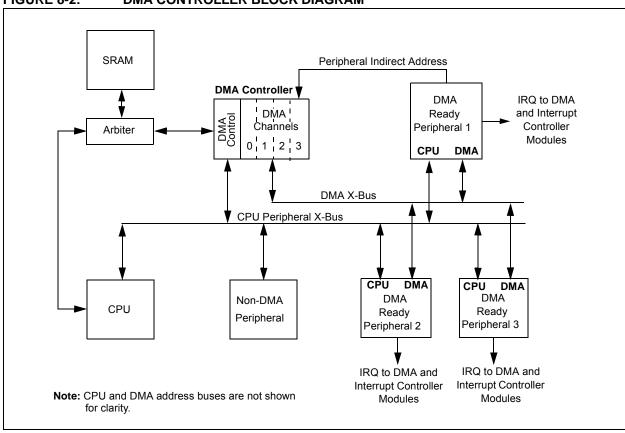


FIGURE 8-2: DMA CONTROLLER BLOCK DIAGRAM

8.1 DMA Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:

In the event you are not able to access the product page using the link above, enter this URL in your browser:

http://www.microchip.com/wwwproducts/ Devices.aspx?dDocName=en555464

8.1.1 KEY RESOURCES

- Section 22. "Direct Memory Access (DMA)" (DS70348)
- · Code Samples
- · Application Notes
- Software Libraries
- · Webinars
- All related dsPIC33E/PIC24E Family Reference Manuals Sections
- · Development Tools

8.2 DMAC Registers

Each DMAC Channel x (where x = 0 through 3) contains the following registers:

- 16-bit DMA Channel Control register (DMAxCON)
- 16-bit DMA Channel IRQ Select register (DMAxREQ)
- 32-bit DMA RAM Primary Start Address register (DMAxSTA)
- 32-bit DMA RAM Secondary Start Address register (DMAxSTB)
- 16-bit DMA Peripheral Address register (DMAxPAD)
- 14-bit DMA Transfer Count register (DMAxCNT)

Additional status registers (DMAPWC, DMARQC, DMAPPS, DMALCA, and DSADR) are common to all DMAC channels. These status registers provide information on write and request collisions, as well as on last address and channel access information.

The interrupt flags (DMAxIF) are located in an IFSx register in the interrupt controller. The corresponding interrupt enable control bits (DMAxIE) are located in an IECx register in the interrupt controller, and the corresponding interrupt priority control bits (DMAxIP) are located in an IPCx register in the interrupt controller.

REGISTER 8-1: DMAXCON: DMA CHANNEL x CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
CHEN	SIZE	DIR	HALF	NULLW	_	_	_
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
_	_	AMODI	E<1:0>	_	_	MODE<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	I as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CHEN:** Channel Enable bit

1 = Channel enabled0 = Channel disabled

SIZE: Data Transfer Size bit

1 = Byte0 = Word

bit 14

bit 13 **DIR:** Transfer Direction bit (source/destination bus select)

1 = Read from RAM address, write to peripheral address0 = Read from Peripheral address, write to RAM address

bit 12 HALF: Block Transfer Interrupt Select bit

1 = Initiate interrupt when half of the data has been moved

0 = Initiate interrupt when all of the data has been moved

bit 11 NULLW: Null Data Peripheral Write Mode Select bit

1 = Null data write to peripheral in addition to RAM write (DIR bit must also be clear)

0 = Normal operation

bit 10-6 **Unimplemented:** Read as '0'

bit 5-4 AMODE<1:0>: DMA Channel Addressing Mode Select bits

11 = Reserved

10 = Peripheral Indirect Addressing mode

01 = Register Indirect without Post-Increment mode

00 = Register Indirect with Post-Increment mode

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 MODE<1:0>: DMA Channel Operating Mode Select bits

11 = One-Shot, Ping-Pong modes enabled (one block transfer from/to each DMA buffer)

10 = Continuous, Ping-Pong modes enabled

01 = One-Shot, Ping-Pong modes disabled

00 = Continuous, Ping-Pong modes disabled

REGISTER 8-2: DMAXREQ: DMA CHANNEL x IRQ SELECT REGISTER

R/S-0	U-0						
FORCE ⁽¹⁾	_	_	_	_	_	_	_
bit 15	•						bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
IRQSEL<7:0>									
bit 7							bit 0		

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15 FORCE: Force DMA Transfer bit⁽¹⁾

1 = Force a single DMA transfer (Manual mode)

0 = Automatic DMA transfer initiation by DMA Request

bit 14-8 **Unimplemented:** Read as '0'

bit 7-0 IRQSEL<7:0>: DMA Peripheral IRQ Number Select bits

01000110 = ECAN1 - TX Data Reguest⁽²⁾

00100110 = IC4 - Input Capture 4

00100101 = IC3 – Input Capture 3

00100010 = ECAN1 - RX Data Ready(2)

00100001 = SPI2 Transfer Done

00011111 = UART2TX - UART2 Transmitter

00011110 = UART2RX - UART2 Receiver

00011100 = TMR5 - Timer5

00011011 = TMR4 - Timer4

00011010 = OC4 - Output Compare 4

00011001 = OC3 – Output Compare 3

00001101 = ADC1 - ADC1 Convert done

00001100 = UART1TX - UART1 Transmitter

00001011 = UART1RX - UART1 Receiver

00001010 = SPI1 - Transfer Done

00001000 = TMR3 - Timer3

00000111 = TMR2 - Timer2

00000110 = OC2 - Output Compare 2

00000101 = IC2 - Input Capture 2

00000010 = OC1 - Output Compare 1

00000001 = IC1 - Input Capture 1

00000000 = INT0 - External Interrupt 0

Note 1: The FORCE bit cannot be cleared by user software. The FORCE bit is cleared by hardware when the forced DMA transfer is complete or the channel is disabled (CHEN = 0).

2: This selection is available in dsPIC33EPXXXGP/MC50X devices only.

REGISTER 8-3: DMAXSTAH: DMA CHANNEL x START ADDRESS REGISTER A (HIGH)

U-0	U-0	U-0	U-0	R/W-0	U-0	U-0	U-0
_	_	_	_	_	_	_	_
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
STA<23:16>									
bit 7							bit 0		

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 STA<23:16>: Primary Start Address bits (source or destination)

REGISTER 8-4: DMAXSTAL: DMA CHANNEL x START ADDRESS REGISTER A (LOW)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
STA<15:8>									
bit 15							bit 8		

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
STA<7:0>									
bit 7							bit 0		

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 STA<15:0>: Primary Start Address bits (source or destination)

REGISTER 8-5: DMAXSTBH: DMA CHANNEL x START ADDRESS REGISTER B (HIGH)

U-0	U-0	U-0	U-0	R/W-0	U-0	U-0	U-0
_	_	_	_	_	_	_	_
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
STB<23:16>									
bit 7							bit 0		

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 STB<23:16>: Secondary Start Address bits (source or destination)

REGISTER 8-6: DMAXSTBL: DMA CHANNEL x START ADDRESS REGISTER B (LOW)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
STB<15:8>								
bit 15							bit 8	

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
STB<7:0>									
bit 7							bit 0		

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **STB<15:0>:** Secondary Start Address bits (source or destination)

REGISTER 8-7: DMAXPAD: DMA CHANNEL X PERIPHERAL ADDRESS REGISTER⁽¹⁾

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
PAD<15:8>									
bit 15							bit 8		

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
PAD<7:0>									
bit 7							bit 0		

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 PAD<15:0>: Peripheral Address Register bits

Note 1: If the channel is enabled (i.e., active), writes to this register may result in unpredictable behavior of the DMA channel and should be avoided.

REGISTER 8-8: DMAXCNT: DMA CHANNEL x TRANSFER COUNT REGISTER⁽¹⁾

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	_			CNT<	13:8> ⁽²⁾		
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			CNT<	7:0> ⁽²⁾			
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-14 Unimplemented: Read as '0'

bit 13-0 CNT<13:0>: DMA Transfer Count Register bits⁽²⁾

Note 1: If the channel is enabled (i.e., active), writes to this register may result in unpredictable behavior of the DMA channel and should be avoided.

2: The number of DMA transfers = CNT<13:0> + 1.

REGISTER 8-9: DSADRH: MOST RECENT RAM HIGH ADDRESS REGISTER

U-0	U-0	U-0	U-0	R/W-0	U-0	U-0	U-0
_		_	_		_	_	_
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	
DSADR<23:16>								
bit 7							bit 0	

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 DSADR<23:16>: Most Recent DMA Address Accessed by DMA bits

REGISTER 8-10: DSADRL: MOST RECENT RAM LOW ADDRESS REGISTER

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0		
DSADR<15:8>									
bit 15									

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0		
DSADR<7:0>									
bit 7							bit 0		

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 DSADR<15:0>: Most Recent DMA Address Accessed by DMA bits

REGISTER 8-11: DMAPWC: DMA PERIPHERAL WRITE COLLISION STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	_	_	_	_	_	_	_
bit 15							bit 8

U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
_	_	_	_	PWCOL3	PWCOL2	PWCOL1	PWCOL0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-4 Unimplemented: Read as '0'

bit 3 PWCOL3: Channel 3 Peripheral Write Collision Flag bit

1 = Write collision detected0 = No write collision detected

bit 2 **PWCOL2:** Channel 2 Peripheral Write Collision Flag bit

1 = Write collision detected0 = No write collision detected

bit 1 PWCOL1: Channel 1 Peripheral Write Collision Flag bit

1 = Write collision detected0 = No write collision detected

bit 0 PWCOL0: Channel 0 Peripheral Write Collision Flag bit

1 = Write collision detected0 = No write collision detected

REGISTER 8-12: DMARQC: DMA REQUEST COLLISION STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	_	_	_	_	_	_	_
bit 15							bit 8

U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
_	_	_	_	RQCOL3	RQCOL2	RQCOL1	RQCOL0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-4 **Unimplemented:** Read as '0'

bit 3 RQCOL3: Channel 3 Transfer Request Collision Flag bit

1 = User FORCE and Interrupt-based request collision detected

0 = No request collision detected

bit 2 RQCOL2: Channel 2 Transfer Request Collision Flag bit

1 = User FORCE and Interrupt-based request collision detected

0 = No request collision detected

bit 1 RQCOL1: Channel 1 Transfer Request Collision Flag bit

1 = User FORCE and Interrupt-based request collision detected

0 = No request collision detected

bit 0 RQCOL0: Channel 0 Transfer Request Collision Flag bit

1 = User FORCE and Interrupt-based request collision detected

0 = No request collision detected

REGISTER 8-13: DMALCA: DMA LAST CHANNEL ACTIVE DMA STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	_		_		_		_
bit 15							bit 8

U-0	U-0	U-0	U-0	R-1	R-1	R-1	R-1
_	_	_	_		LSTCH	1<3:0>	
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-4 Unimplemented: Read as '0'

bit 3-0 LSTCH<3:0>: Last DMAC Channel Active Status bits

1111 = No DMA transfer has occurred since system Reset

1110 = Reserved

.

•

0100 = Reserved

0011 = Last data transfer was handled by Channel 3

0010 = Last data transfer was handled by Channel 2

0001 = Last data transfer was handled by Channel 1

0000 = Last data transfer was handled by Channel 0

REGISTER 8-14: DMAPPS: DMA PING-PONG STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	_	_	_	_	_	_	_
bit 15							bit 8

U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
_	_	_	_	PPST3	PPST2	PPST1	PPST0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-4 **Unimplemented:** Read as '0'

bit 3 PPST3: Channel 3 Ping-Pong Mode Status Flag bit

1 = DMASTB3 register selected0 = DMASTA3 register selected

bit 2 PPST2: Channel 2 Ping-Pong Mode Status Flag bit

1 = DMASTB2 register selected0 = DMASTA2 register selected

bit 1 PPST1: Channel 1 Ping-Pong Mode Status Flag bit

1 = DMASTB1 register selected0 = DMASTA1 register selected

bit 0 PPST0: Channel 0 Ping-Pong Mode Status Flag bit

1 = DMASTB0 register selected0 = DMASTA0 register selected

9.0 OSCILLATOR CONFIGURATION

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 7. "Oscillator" (DS70580) of the "dsPIC33E/PIC24E Family Reference Manual", which is available from the Microchip web site (www.microchip.com).

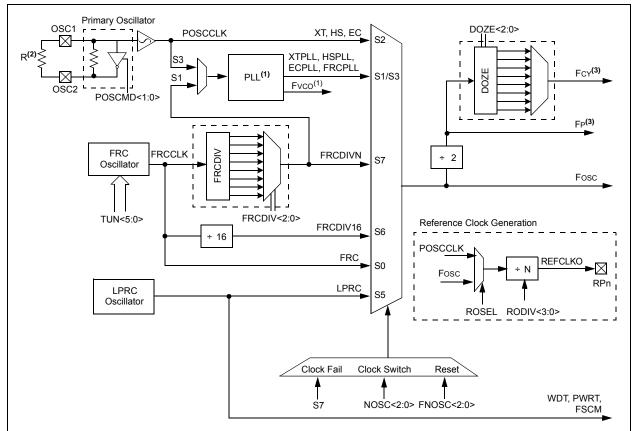
2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X oscillator system provides:

- On-chip Phase-Locked Loop (PLL) to boost internal operating frequency on select internal and external oscillator sources
- On-the-fly clock switching between various clock sources
- · Doze mode for system power savings
- Fail-Safe Clock Monitor (FSCM) that detects clock failure and permits safe application recovery or shutdown
- · Configuration bits for clock source selection

A simplified diagram of the oscillator system is shown in Figure 9-1.

FIGURE 9-1: OSCILLATOR SYSTEM DIAGRAM



Note 1: See Figure 9-2 for PLL and Fvco details.

- 2: If the Oscillator is used with XT or HS modes, an external parallel resistor with the value of 1 $M\Omega$ must be connected.
- 3: The term FP refers to the clock source for all peripherals, while FCY refers to the clock source for the CPU. Throughout this document, FCY and FP are used interchangeably, except in the case of DOZE mode. FP and FCY will be different when DOZE mode is used with a doze ratio of 1:2 or lower.

9.1 CPU Clocking System

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X family of devices provide seven system clock options:

- · Fast RC (FRC) Oscillator
- FRC Oscillator with Phase-Locked Loop (PLL)
- · FRC Oscillator with postscaler
- · Primary (XT, HS or EC) Oscillator
- · Primary Oscillator with PLL
- · Low-Power RC (LPRC) Oscillator

Instruction execution speed or device operating frequency, Fcy, is given by Equation 9-1.

EQUATION 9-1: DEVICE OPERATING FREQUENCY

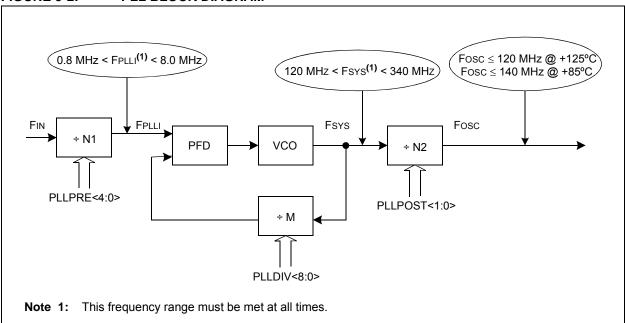
$$FCY = Fosc/2$$

Figure 9-2 is a block diagram of the PLL module.

Equation 9-2 provides the relation between input frequency (FIN) and output frequency (FOSC).

Equation 9-3 provides the relation between input frequency (FIN) and VCO frequency (FSYS).

FIGURE 9-2: PLL BLOCK DIAGRAM



EQUATION 9-2: Fosc CALCULATION

$$Fosc = Fin \times \left(\frac{M}{N1 \times N2}\right) = Fin \times \left(\frac{(PLLDIV + 2)}{(PLLPRE + 2) \times 2(PLLPOST + 1)}\right)$$

Where,

N1 = PLLPRE + 2

 $N2 = 2 \times (PLLPOST + 1)$

M = PLLDIV + 2

EQUATION 9-3: Fvco CALCULATION

$$Fsys = Fin \times \left(\frac{M}{N1}\right) = Fin \times \left(\frac{(PLLDIV + 2)}{(PLLPRE + 2)}\right)$$

TABLE 9-1: CONFIGURATION BIT VALUES FOR CLOCK SELECTION

Oscillator Mode	Oscillator Source	POSCMD<1:0>	FNOSC<2:0>	See Note
Fast RC Oscillator with Divide-by-N (FRCDIVN)	Internal	xx	111	1, 2
Low-Power RC Oscillator (LPRC)	Internal	xx	101	1
Primary Oscillator (HS) with PLL (HSPLL)	Primary	10	011	_
Primary Oscillator (XT) with PLL (XTPLL)	Primary	01	011	_
Primary Oscillator (EC) with PLL (ECPLL)	Primary	00	011	1
Primary Oscillator (HS)	Primary	10	010	_
Primary Oscillator (XT)	Primary	01	010	_
Primary Oscillator (EC)	Primary	00	010	1
Fast RC Oscillator (FRC) with divide-by-N and PLL (FRCPLL)	Internal	xx	001	1
Fast RC Oscillator (FRC)	Internal	xx	000	1

Note 1: OSC2 pin function is determined by the OSCIOFNC Configuration bit.

9.2 Oscillator Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:

In the event you are not able to access the product page using the link above, enter this URL in your browser:

http://www.microchip.com/wwwproducts/ Devices.aspx?dDocName=en555464

9.2.1 KEY RESOURCES

- Section 7. "Oscillator" (DS70580)
- · Code Samples
- · Application Notes
- · Software Libraries
- Webinars
- All related dsPIC33E/PIC24E Family Reference Manuals Sections
- · Development Tools

^{2:} This is the default oscillator mode for an unprogrammed (erased) device.

REGISTER 9-1: OSCCON: OSCILLATOR CONTROL REGISTER (1,3)

U-0	R-0	R-0	R-0	U-0	R/W-y	R/W-y	R/W-y
_		COSC<2:0>		_		NOSC<2:0> ⁽²⁾	
bit 15							bit 8

R/W-0	R/W-0	R-0	U-0	R/C-0	U-0	U-0	R/W-0
CLKLOCK	IOLOCK	LOCK	_	CF	_	_	OSWEN
bit 7							bit 0

Legend:	y = Value set from Configuration bits on POR				
R = Readable bit	W = Writable bit U = Unimplemented bit, read as '0'				
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **COSC<2:0>:** Current Oscillator Selection bits (read-only)

111 = Fast RC Oscillator (FRC) with Divide-by-n

110 = Fast RC Oscillator (FRC) with Divide-by-16 101 = Low-Power RC Oscillator (LPRC)

100 = Reserved

011 = Primary Oscillator (XT, HS, EC) with PLL

010 = Primary Oscillator (XT, HS, EC)

001 = Fast RC Oscillator (FRC) with divide-by-N and PLL (FRCPLL)

000 = Fast RC Oscillator (FRC)

bit 11 **Unimplemented:** Read as '0'

bit 10-8 NOSC<2:0>: New Oscillator Selection bits⁽²⁾

111 = Fast RC Oscillator (FRC) with Divide-by-n

110 = Fast RC Oscillator (FRC) with Divide-by-16

101 = Low-Power RC Oscillator (LPRC)

100 = Reserved

011 = Primary Oscillator (XT, HS, EC) with PLL

010 = Primary Oscillator (XT, HS, EC)

001 = Fast RC Oscillator (FRC) with divide-by-N and PLL (FRCPLL)

000 = Fast RC Oscillator (FRC)

bit 7 CLKLOCK: Clock Lock Enable bit

1 = If (FCKSM0 = 1), then clock and PLL configurations are locked

If (FCKSM0 = 0), then clock and PLL configurations may be modified

0 = Clock and PLL selections are not locked, configurations may be modified

bit 6 IOLOCK: I/O Lock Enable bit

1 = I/O Lock is active

0 = I/O Lock is not active

bit 5 LOCK: PLL Lock Status bit (read-only)

1 = Indicates that PLL is in lock, or PLL start-up timer is satisfied

0 = Indicates that PLL is out of lock, start-up timer is in progress or PLL is disabled

bit 4 Unimplemented: Read as '0'

Note 1: Writes to this register require an unlock sequence. Refer to **Section 7. "Oscillator"** (DS70580) in the "dsPIC33E/PIC24E Family Reference Manual" (available from the Microchip web site) for details.

- 2: Direct clock switches between any primary oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transition clock source between the two PLL modes.
- 3: This register resets only on a Power-on Reset (POR).

REGISTER 9-1: OSCCON: OSCILLATOR CONTROL REGISTER^(1,3) (CONTINUED)

bit 3 **CF:** Clock Fail Detect bit (read/clear by application)

1 = FSCM has detected clock failure0 = FSCM has not detected clock failure

bit 2-1 Unimplemented: Read as '0'

bit 0 **OSWEN:** Oscillator Switch Enable bit

1 = Request oscillator switch to selection specified by NOSC<2:0> bits

0 = Oscillator switch is complete

- **Note 1:** Writes to this register require an unlock sequence. Refer to **Section 7.** "**Oscillator**" (DS70580) in the "dsPIC33E/PIC24E Family Reference Manual" (available from the Microchip web site) for details.
 - 2: Direct clock switches between any primary oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transition clock source between the two PLL modes.
 - 3: This register resets only on a Power-on Reset (POR).

REGISTER 9-2: CLKDIV: CLOCK DIVISOR REGISTER(2)

R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
ROI		DOZE<2:0>(3)		DOZEN ^(1,4)		FRCDIV<2:0>	
bit 15							bit 8

R/W-0	R/W-1	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PLLPOS	ST<1:0>	_			PLLPRE<4:0>	>	
bit 7							bit 0

Legend:	y = Value set from Co	y = Value set from Configuration bits on POR					
R = Readable bit	W = Writable bit	W = Writable bit U = Unimplemented bit, read as '0'					
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown				

bit 15 ROI: Recover on Interrupt bit

1 = Interrupts will clear the DOZEN bit and the processor clock and peripheral clock ratio is set to 1:1

0 = Interrupts have no effect on the DOZEN bit

bit 14-12 **DOZE<2:0>:** Processor Clock Reduction Select bits⁽³⁾

111 = Fcy divided by 128

110 = FcY divided by 64

101 = Fcy divided by 32

100 = Fcy divided by 16

011 = Fcy divided by 8 (default)

010 = Fcy divided by 4

001 = Fcy divided by 2

000 = Fcy divided by 1

bit 11 **DOZEN:** Doze Mode Enable bit^(1,4)

1 = DOZE<2:0> field specifies the ratio between the peripheral clocks and the processor clocks

0 = Processor clock and peripheral clock ratio forced to 1:1

bit 10-8 FRCDIV<2:0>: Internal Fast RC Oscillator Postscaler bits

111 = FRC divided by 256

110 = FRC divided by 64

101 = FRC divided by 32

100 = FRC divided by 16

011 = FRC divided by 8

010 = FRC divided by 4

001 = FRC divided by 2

000 = FRC divided by 1 (default)

bit 7-6 PLLPOST<1:0>: PLL VCO Output Divider Select bits (also denoted as 'N2', PLL postscaler)

11 = Output divided by 8

10 = Reserved

01 = Output divided by 4 (default)

00 = Output divided by 2

bit 5 **Unimplemented:** Read as '0'

Note 1: This bit is cleared when the ROI bit is set and an interrupt occurs.

- 2: This register resets only on a Power-on Reset (POR).
- **3:** DOZE<2:0> bits can only be written to when the DOZEN bit is clear. If DOZEN = 1, any writes to DOZE<2:0> are ignored.
- **4:** The DOZEN bit cannot be set if DOZE<2:0> = 000. If DOZE<2:0> = 000, any attempt by user software to set the DOZEN bit is ignored.

REGISTER 9-2: CLKDIV: CLOCK DIVISOR REGISTER⁽²⁾ (CONTINUED)

- Note 1: This bit is cleared when the ROI bit is set and an interrupt occurs.
 - 2: This register resets only on a Power-on Reset (POR).
 - **3:** DOZE<2:0> bits can only be written to when the DOZEN bit is clear. If DOZEN = 1, any writes to DOZE<2:0> are ignored.
 - **4:** The DOZEN bit cannot be set if DOZE<2:0> = 000. If DOZE<2:0> = 000, any attempt by user software to set the DOZEN bit is ignored.

REGISTER 9-3: PLLFBD: PLL FEEDBACK DIVISOR REGISTER⁽¹⁾

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
_	_	_	_	_	_	_	PLLDIV<8>
bit 15							bit 8

R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
			PLLDI'	V<7:0>			
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-9 **Unimplemented:** Read as '0'

bit 8-0 PLLDIV<8:0>: PLL Feedback Divisor bits (also denoted as 'M', PLL multiplier)

111111111 = 513

•

•

•

000110000 = 50 (default)

•

•

•

00000010 = 4

000000001 = 3

000000000 = 2

Note 1: This register is reset only on a Power-on Reset (POR).

REGISTER 9-4: OSCTUN: FRC OSCILLATOR TUNING REGISTER⁽¹⁾

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	_	_	_	_	_	_	_
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	_			TUN	l<5:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-6	Unimplemented: Read as '0'
bit 5-0	TUN<5:0>: FRC Oscillator Tuning bits
	111111 = Center frequency -0.375% (7.345 MHz)
	•
	•
	•
	100001 = Center frequency -11.625% (6.52 MHz)
	100000 = Center frequency -12% (6.49 MHz)
	011111 = Center frequency + 11.625% (8.23 MHz) 011110 = Center frequency + 11.25% (8.20 MHz)
	• • • • • • • • • • • • • • • • • • •
	•
	•
	000001 = Center frequency 0.3759/ (7.40 MHz)
	000001 = Center frequency + 0.375% (7.40 MHz) 000000 = Center frequency (7.37 MHz nominal)

Note 1: This register resets only on a Power-on Reset (POR).

REGISTER 9-5: REFOCON: REFERENCE OSCILLATOR CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ROON	_	ROSSLP	ROSEL		RODIV	<3:0> ⁽¹⁾	
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	_	_	_	_	_	_	_
bit 7							bit 0

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15 ROON: Reference Oscillator Output Enable bit

1 = Reference oscillator output enabled on REFCLK⁽²⁾ pin

0 = Reference oscillator output disabled

bit 14 Unimplemented: Read as '0'

bit 13 ROSSLP: Reference Oscillator Run in Sleep bit

1 = Reference oscillator output continues to run in Sleep

0 = Reference oscillator output is disabled in Sleep

bit 12 ROSEL: Reference Oscillator Source Select bit

1 = Oscillator crystal used as the reference clock

0 = System clock used as the reference clock

bit 11-8 **RODIV<3:0>:** Reference Oscillator Divider bits⁽¹⁾

1111 = Reference clock divided by 32,768

1110 = Reference clock divided by 16,384

1101 = Reference clock divided by 8,192

1100 = Reference clock divided by 4,096

1011 = Reference clock divided by 2,048

1010 = Reference clock divided by 1,024

1001 = Reference clock divided by 512

1000 = Reference clock divided by 312

0111 = Reference clock divided by 128

0110 = Reference clock divided by 64

0101 = Reference clock divided by 32

0100 = Reference clock divided by 16

0011 = Reference clock divided by 8

0010 = Reference clock divided by 4

0001 = Reference clock divided by 2

0000 = Reference clock

bit 7-0 **Unimplemented:** Read as '0'

Note 1: The reference oscillator output must be disabled (ROON = 0) before writing to these bits.

2: This pin is remappable. See **Section 11.4 "Peripheral Pin Select"** for more information.

10.0 POWER-SAVING FEATURES

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 9. "Watchdog Timer and Power-Saving Modes" (DS70615) of the "dsPIC33E/PIC24E Family Reference Manual", which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X devices provide the ability to manage power consumption by selectively managing clocking to the CPU and the peripherals. In general, a lower clock frequency and a reduction in the number of peripherals being clocked constitutes lower consumed power.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X devices can manage power consumption in four ways:

- · Clock frequency
- · Instruction-based Sleep and Idle modes
- · Software-controlled Doze mode
- · Selective peripheral control in software

Combinations of these methods can be used to selectively tailor an application's power consumption while still maintaining critical application features, such as timing-sensitive communications.

10.1 Clock Frequency and Clock Switching

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X devices allow a wide range of clock frequencies to be selected under application control. If the system clock configuration is not locked, users can choose low-power or high-precision oscillators by simply changing the NOSC bits (OSCCON<10:8>). The process of changing a system clock during operation, as well as limitations to the process, are discussed in more detail in **Section 9.0** "Oscillator Configuration".

10.2 Instruction-Based Power-Saving Modes

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X devices have two special power-saving modes that are entered through the execution of a special PWRSAV instruction. Sleep mode stops clock operation and halts all code execution. Idle mode halts the CPU and code execution, but allows peripheral modules to continue operation. The assembler syntax of the PWRSAV instruction is shown in Example 10-1.

Note: SLEEP_MODE and IDLE_MODE are constants defined in the assembler include file for the selected device.

Sleep and Idle modes can be exited as a result of an enabled interrupt, WDT time-out or a device Reset. When the device exits these modes, it is said to "wake up".

EXAMPLE 10-1: PWRSAV INSTRUCTION SYNTAX

PWRSAV #SLEEP_MODE ; Put the device into Sleep mode
PWRSAV #IDLE_MODE ; Put the device into Idle mode

10.2.1 SLEEP MODE

The following occur in Sleep mode:

- The system clock source is shut down. If an on-chip oscillator is used, it is turned off.
- The device current consumption is reduced to a minimum, provided that no I/O pin is sourcing current
- The Fail-Safe Clock Monitor does not operate, since the system clock source is disabled
- The LPRC clock continues to run in Sleep mode if the WDT is enabled
- The WDT, if enabled, is automatically cleared prior to entering Sleep mode
- Some device features or peripherals can continue to operate. This includes items such as the input change notification on the I/O ports, or peripherals that use an external clock input.
- Any peripheral that requires the system clock source for its operation is disabled

The device wakes up from Sleep mode on any of the these events:

- · Any interrupt source that is individually enabled
- · Any form of device Reset
- · A WDT time-out

On wake-up from Sleep mode, the processor restarts with the same clock source that was active when Sleep mode was entered.

For optimal power savings, the internal regulator and the Flash regulator can be configured to go into Standby when Sleep mode is entered by clearing the VREGS (RCON<8>) and VREGSF (RCON<11>) bits (default configuration).

If the application requires a faster wake-up time, and can accept higher current requirements, the VREGS (RCON<8>) and VREGSF (RCON<11>) bits can be set to keep the internal regulator and the Flash regulator active during Sleep mode.

10.2.2 IDLE MODE

The following occur in Idle mode:

- · The CPU stops executing instructions
- · The WDT is automatically cleared
- The system clock source remains active. By default, all peripheral modules continue to operate normally from the system clock source, but can also be selectively disabled (see Section 10.4 "Peripheral Module Disable").
- If the WDT or FSCM is enabled, the LPRC also remains active.

The device wakes from Idle mode on any of these events:

- · Any interrupt that is individually enabled
- · Any device Reset
- A WDT time-out

On wake-up from Idle mode, the clock is reapplied to the CPU and instruction execution will begin (2-4 clock cycles later), starting with the instruction following the PWRSAV instruction, or the first instruction in the ISR.

All peripherals also have the option to discontinue operation when Idle mode is entered to allow for increased power savings. This option is selectable in the control register of each peripheral. For example, the TSIDL bit in the Timer1 Control register (T1CON<13>).

10.2.3 INTERRUPTS COINCIDENT WITH POWER SAVE INSTRUCTIONS

Any interrupt that coincides with the execution of a ${\tt PWRSAV}$ instruction is held off until entry into Sleep or Idle mode has completed. The device then wakes up from Sleep or Idle mode.

10.3 Doze Mode

The preferred strategies for reducing power consumption are changing clock speed and invoking one of the power-saving modes. In some circumstances, this cannot be practical. For example, it may be necessary for an application to maintain uninterrupted synchronous communication, even while it is doing nothing else. Reducing system clock speed can introduce communication errors, while using a power-saving mode can stop communications completely.

Doze mode is a simple and effective alternative method to reduce power consumption while the device is still executing code. In this mode, the system clock continues to operate from the same source and at the same speed. Peripheral modules continue to be clocked at the same speed, while the CPU clock speed is reduced. Synchronization between the two clock domains is maintained, allowing the peripherals to access the SFRs while the CPU executes code at a slower rate.

Doze mode is enabled by setting the DOZEN bit (CLKDIV<11>). The ratio between peripheral and core clock speed is determined by the DOZE<2:0> bits (CLKDIV<14:12>). There are eight possible configurations, from 1:1 to 1:128, with 1:1 being the default setting.

Programs can use Doze mode to selectively reduce power consumption in event-driven applications. This allows clock-sensitive functions, such as synchronous communications, to continue without interruption while the CPU idles, waiting for something to invoke an interrupt routine. An automatic return to full-speed CPU operation on interrupts can be enabled by setting the ROI bit (CLKDIV<15>). By default, interrupt events have no effect on Doze mode operation.

For example, suppose the device is operating at 20 MIPS and the ECAN module has been configured for 500 kbps based on this device operating speed. If the device is placed in Doze mode with a clock frequency ratio of 1:4, the ECAN module continues to communicate at the required bit rate of 500 kbps, but the CPU now starts executing instructions at a frequency of 5 MIPS.

10.4 Peripheral Module Disable

The Peripheral Module Disable (PMD) registers provide a method to disable a peripheral module by stopping all clock sources supplied to that module. When a peripheral is disabled using the appropriate PMD control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral are also disabled, so writes to those registers do not have effect and read values are invalid.

A peripheral module is enabled only if both the associated bit in the PMD register is cleared and the peripheral is supported by the specific dsPIC® DSC variant. If the peripheral is present in the device, it is enabled in the PMD register by default.

Note: If a PMD bit is set, the corresponding module is disabled after a delay of one instruction cycle. Similarly, if a PMD bit is cleared, the corresponding module is enabled after a delay of one instruction cycle (assuming the module control registers are already configured to enable module operation).

10.5 Power-Saving Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter this URL in your browser:

http://www.microchip.com/wwwproducts/
Devices.aspx?dDocName=en555464

10.5.1 KEY RESOURCES

- Section 9. "Watchdog Timer and Power-Saving Modes" (DS70615)
- · Code Samples
- Application Notes
- · Software Libraries
- · Webinars
- All related dsPIC33E/PIC24E Family Reference Manuals Sections
- · Development Tools

REGISTER 10-1: PMD1: PERIPHERAL MODULE DISABLE CONTROL REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
T5MD	T4MD	T3MD	T2MD	T1MD	QEI1MD ⁽¹⁾	PWMMD ⁽¹⁾	_
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	_	C1MD ⁽²⁾	AD1MD
bit 7							bit 0

ı	e	ae	n	d	•

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15	T5MD: Timer5 Module Disable bit
	1 = Timer5 module is disabled
	0 = Timer5 module is enabled
bit 14	T4MD: Timer4 Module Disable bit
	1 = Timer4 module is disabled
	0 = Timer4 module is enabled
bit 13	T3MD: Timer3 Module Disable bit
	1 = Timer3 module is disabled
	0 = Timer3 module is enabled
bit 12	T2MD: Timer2 Module Disable bit
	1 = Timer2 module is disabled
	0 = Timer2 module is enabled
bit 11	T1MD: Timer1 Module Disable bit
	1 = Timer1 module is disabled 0 = Timer1 module is enabled
bit 10	QEI1MD: QEI1 Module Disable bit ⁽¹⁾
DIL 10	1 = QEI1 module is disabled
	0 = QEI1 module is disabled
bit 9	PWMMD: PWM Module Disable bit ⁽¹⁾
	1 = PWM module is disabled
	0 = PWM module is enabled
bit 8	Unimplemented: Read as '0'
bit 7	I2C1MD: I2C1 Module Disable bit
	1 = I2C1 module is disabled
	0 = I2C1 module is enabled
bit 6	U2MD: UART2 Module Disable bit
	1 = UART2 module is disabled
	0 = UART2 module is enabled
bit 5	U1MD: UART1 Module Disable bit
	1 = UART1 module is disabled
	0 = UART1 module is enabled
bit 4	SPI2MD: SPI2 Module Disable bit
	1 = SPI2 module is disabled
	0 = SPI2 module is enabled

Note 1: This bit is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

2: This bit is available on dsPIC33EPXXXGP50X and dsPIC33EPXXXMC50X devices only.

REGISTER 10-1: PMD1: PERIPHERAL MODULE DISABLE CONTROL REGISTER 1 (CONTINUED)

bit 3 SPI1MD: SPI1 Module Disable bit

1 = SPI1 module is disabled

0 = SPI1 module is enabled

bit 2 **Unimplemented:** Read as '0'

bit 1 C1MD: ECAN1 Module Disable bit⁽²⁾

1 = ECAN1 module is disabled 0 = ECAN1 module is enabled

bit 0 AD1MD: ADC1 Module Disable bit

1 = ADC1 module is disabled 0 = ADC1 module is enabled

Note 1: This bit is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

2: This bit is available on dsPIC33EPXXXGP50X and dsPIC33EPXXXMC50X devices only.

REGISTER 10-2: PMD2: PERIPHERAL MODULE DISABLE CONTROL REGISTER 2

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
_	_	_	_	IC4MD	IC3MD	IC2MD	IC1MD
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
_	_	_	_	OC4MD	OC3MD	OC2MD	OC1MD
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-12 **Unimplemented:** Read as '0'

bit 11 IC4MD: Input Capture 4 Module Disable bit

1 = Input Capture 4 module is disabled0 = Input Capture 4 module is enabled

0 - Imput Gapture 4 module is chabled

bit 10 IC3MD: Input Capture 3 Module Disable bit

1 = Input Capture 3 module is disabled0 = Input Capture 3 module is enabled

bit 9 IC2MD: Input Capture 2 Module Disable bit

1 = Input Capture 2 module is disabled

0 = Input Capture 2 module is enabled

bit 8 IC1MD: Input Capture 1 Module Disable bit

1 = Input Capture 1 module is disabled

0 = Input Capture 1 module is enabled

bit 7-4 Unimplemented: Read as '0'

bit 3 OC4MD: Output Compare 4 Module Disable bit

1 = Output Compare 4 module is disabled

0 = Output Compare 4 module is enabled

bit 2 OC3MD: Output Compare 3 Module Disable bit

1 = Output Compare 3 module is disabled

0 = Output Compare 3 module is enabled

bit 1 OC2MD: Output Compare 2 Module Disable bit

1 = Output Compare 2 module is disabled

0 = Output Compare 2 module is enabled

bit 0 OC1MD: Output Compare 1 Module Disable bit

1 = Output Compare 1 module is disabled

0 = Output Compare 1 module is enabled

REGISTER 10-3: PMD3: PERIPHERAL MODULE DISABLE CONTROL REGISTER 3

U-0	U-0	U-0	U-0	U-0	R/W-0	U-0	U-0
_	_	_	_	_	CMPMD	_	_
bit 15							bit 8

R/W-0	U-0	U-0	U-0	U-0	U-0	R/W-0	U-0
CRCMD	_	_	_	_	_	I2C2MD	_
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-11 **Unimplemented:** Read as '0'

bit 10 **CMPMD:** Comparator Module Disable bit

1 = Comparator module is disabled0 = Comparator module is enabled

bit 9-8 **Unimplemented:** Read as '0'

bit 7 CRCMD: CRC Module Disable bit

1 = CRC module is disabled 0 = CRC module is enabled

bit 6-2 **Unimplemented:** Read as '0' bit 1 **I2C2MD:** I2C2 Module Disable bit

1 = I2C2 module is disabled

0 = I2C2 module is enabled

bit 0 **Unimplemented:** Read as '0'

REGISTER 10-4: PMD4: PERIPHERAL MODULE DISABLE CONTROL REGISTER 4

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	_	_	_	_	_	_	_
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0
_	_	_	_	REFOMD	CTMUMD	_	_
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-4 **Unimplemented:** Read as '0'

bit 3 REFOMD: Reference Clock Module Disable bit

1 = Reference Clock module is disabled0 = Reference Clock module is enabled

bit 2 CTMUMD: CTMU Module Disable bit

1 = CTMU module is disabled 0 = CTMU module is enabled

bit 1-0 **Unimplemented:** Read as '0'

REGISTER 10-5: PMD6: PERIPHERAL MODULE DISABLE CONTROL REGISTER 6

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
_	_	_	_	_	PWM3MD ⁽¹⁾	PWM2MD ⁽¹⁾	PWM1MD ⁽¹⁾
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	_	_	_	_	_	_	_
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-11 **Unimplemented:** Read as '0'

bit 10 **PWM3MD:** PWM3 Module Disable bit⁽¹⁾

1 = PWM3 module is disabled 0 = PWM3 module is enabled

bit 9 **PWM2MD:** PWM2 Module Disable bit⁽¹⁾

1 = PWM2 module is disabled 0 = PWM2 module is enabled

bit 8 **PWM1MD:** PWM1 Module Disable bit⁽¹⁾

1 = PWM1 module is disabled 0 = PWM1 module is enabled

bit 7-0 **Unimplemented:** Read as '0'

Note 1: This bit is available in dsPIC33EPXXXMC50X/20X and PIC24EPXXXMC20X devices only.

REGISTER 10-6: PMD7: PERIPHERAL MODULE DISABLE CONTROL REGISTER 7

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
_	_	_	_				_	
bit 15	bit 15 bit 8							

U-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0
		DMA0MD ⁽¹⁾					
			DMA1MD ⁽¹⁾	PTGMD			
_	_	_	DMA2MD ⁽¹⁾	FIGNID	_	_	_
		DMA3MD ⁽¹⁾					
bit 7							bit 0

Legend	:
--------	---

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-5 **Unimplemented:** Read as '0'

bit 4 DMA0MD: DMA0 Module Disable bit⁽¹⁾

1 = DMA0 module is disabled 0 = DMA0 module is enabled

DMA1MD: DMA1 Module Disable bit⁽¹⁾

1 = DMA1 module is disabled 0 = DMA1 module is enabled

DMA2MD: DMA2 Module Disable bit(1)

1 = DMA2 module is disabled0 = DMA2 module is enabled

DMA3MD: DMA3 Module Disable bit(1)

1 = DMA3 module is disabled 0 = DMA3 module is enabled

bit 3 **PTGMD:** PTG Module Disable bit

1 = PTG module is disabled 0 = PTG module is enabled

bit 2-0 **Unimplemented:** Read as '0'

Note 1: This single bit enables and disables all four DMA channels.

I/O PORTS 11.0

Note 1: This data sheet summarizes the features dsPIC33EPXXXGP50X, the dsPIC33EPXXXMC20X/50X. and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet. refer to Section 10. "I/O Ports" (DS70598) of the "dsPIC33E/PIC24E Family Reference Manual', which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

Many of the device pins are shared among the peripherals and the parallel I/O ports. All I/O input ports feature Schmitt Trigger inputs for improved noise immunity.

11.1 Parallel I/O (PIO) Ports

Generally, a parallel I/O port that shares a pin with a peripheral is subservient to the peripheral. The peripheral's output buffer data and control signals are provided to a pair of multiplexers. The multiplexers select whether the peripheral or the associated port has ownership of the output data and control signals of the I/O pin. The logic also prevents "loop through," in which a port's digital output can drive the input of a peripheral that shares the same pin. Figure 11-1 illustrates how ports are shared with other peripherals and the associated I/O pin to which they are connected.

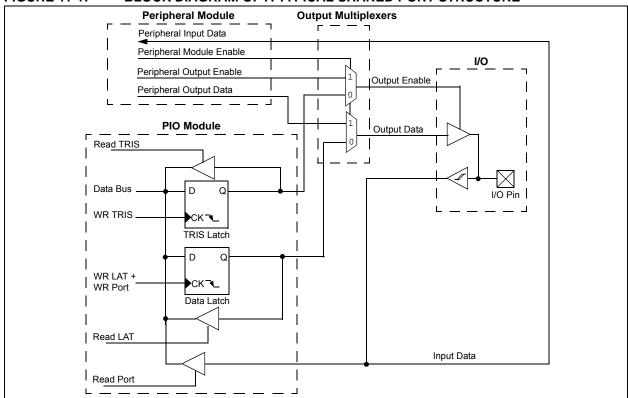
When a peripheral is enabled and the peripheral is actively driving an associated pin, the use of the pin as a general purpose output pin is disabled. The I/O pin can be read, but the output driver for the parallel port bit is disabled. If a peripheral is enabled, but the peripheral is not actively driving a pin, that pin can be driven by a

All port pins have eight registers directly associated with their operation as digital I/O. The data direction register (TRISx) determines whether the pin is an input or an output. If the data direction bit is a '1', then the pin is an input. All port pins are defined as inputs after a Reset. Reads from the latch (LATx) read the latch. Writes to the latch write the latch. Reads from the port (PORTx) read the port pins, while writes to the port pins write the latch.

Any bit and its associated data and control registers that are not valid for a particular device is disabled. This means the corresponding LATx and TRISx registers and the port pin are read as zeros.

When a pin is shared with another peripheral or function that is defined as an input only, it is nevertheless regarded as a dedicated port because there is no other competing source of outputs.

FIGURE 11-1: BLOCK DIAGRAM OF A TYPICAL SHARED PORT STRUCTURE Peripheral Module **Output Multiplexers**



11.1.1 OPEN-DRAIN CONFIGURATION

In addition to the PORT, LAT and TRIS registers for data control, port pins can also be individually configured for either digital or open-drain output. This is controlled by the Open-Drain Control register, ODCx, associated with each port. Setting any of the bits configures the corresponding pin to act as an open-drain output.

The open-drain feature allows the generation of outputs other than VDD by using external pull-up resistors. The maximum open-drain voltage allowed on any pin is the same as the maximum VIH specification for that particular pin.

See the "Pin Diagrams" section for the available 5V-tolerant pins and Table 30-10 for the maximum VIH specification for each pin.

11.2 Configuring Analog and Digital Port Pins

The ANSELx register controls the operation of the analog port pins. The port pins that are to function as analog inputs or outputs must have their corresponding ANSEL and TRIS bits set. In order to use port pins for I/O functionality with digital modules, such as Timers, UARTs, etc., the corresponding ANSELx bit must be cleared.

The ANSELx register has a default value of 0xFFFF; therefore, all pins that share analog functions are analog (not digital) by default.

Pins with analog functions affected by the ANSELx registers are listed with a buffer type of Analog in the Pinout I/O Descriptions (see Table 1-1).

If the TRIS bit is cleared (output) while the ANSELx bit is set, the digital output level (VOH or VOL) is converted by an analog peripheral, such as the ADC module or Comparator module.

When the PORT register is read, all pins configured as analog input channels are read as cleared (a low level).

Pins configured as digital inputs do not convert an analog input. Analog levels on any pin defined as a digital input (including the ANx pins) can cause the input buffer to consume current that exceeds the device specifications.

11.2.1 I/O PORT WRITE/READ TIMING

One instruction cycle is required between a port direction change or port write operation and a read operation of the same port. Typically this instruction would be an NOP, as shown in Example 11-1.

11.3 Input Change Notification

The input change notification function of the I/O ports allows devices to generate interrupt requests to the processor in response to a change-of-state on selected input pins. This feature can detect input change-of-states even in Sleep mode, when the clocks are disabled. Every I/O port pin can be selected (enabled) for generating an interrupt request on a change-of-state.

Three control registers are associated with the CN functionality of each I/O port. The CNENx registers contain the CN interrupt enable control bits for each of the input pins. Setting any of these bits enables a CN interrupt for the corresponding pins.

Each I/O pin also has a weak pull-up and a weak pull-down connected to it. The pull-ups and pull-downs act as a current source or sink source connected to the pin, and eliminate the need for external resistors when push-button or keypad devices are connected. The pull-ups and pull-downs are enabled separately using the CNPUx and the CNPDx registers, which contain the control bits for each of the pins. Setting any of the control bits enables the weak pull-ups and/or pull-downs for the corresponding pins.

Note: Pull-ups and pull-downs on change notification pins should always be disabled when the port pin is configured as a digital output.

EXAMPLE 11-1: PORT WRITE/READ EXAMPLE

```
MOV 0xFF00, W0 ; Configure PORTB<15:8>
; as inputs
MOV W0, TRISB ; and PORTB<7:0>
; as outputs
NOP ; Delay 1 cycle
BTSS PORTB, #13 ; Next Instruction
```

11.4 Peripheral Pin Select

A major challenge in general purpose devices is providing the largest possible set of peripheral features while minimizing the conflict of features on I/O pins. The challenge is even greater on low pin-count devices. In an application where more than one peripheral needs to be assigned to a single pin, inconvenient workarounds in application code or a complete redesign may be the only option.

Peripheral pin select configuration provides an alternative to these choices by enabling peripheral set selection and their placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, users can better tailor the device to their entire application, rather than trimming the application to fit the device.

The peripheral pin select configuration feature operates over a fixed subset of digital I/O pins. Users may independently map the input and/or output of most digital peripherals to any one of these I/O pins. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping once it has been established.

11.4.1 AVAILABLE PINS

The number of available pins is dependent on the particular device and its pin count. Pins that support the Peripheral Pin Select feature include the designation, "RPn" or "RPln", in their full pin designation, where "n" is the remappable pin number. "RP" is used to designate pins that support both remappable input and output functions, while "RPI" indicates pins that support remappable input functions only.

11.4.2 AVAILABLE PERIPHERALS

The peripherals managed by the peripheral pin select are all digital-only peripherals. These include general serial communications (UART and SPI), general purpose timer clock inputs, timer-related peripherals (input capture and output compare) and interrupt-on-change inputs.

In comparison, some digital-only peripheral modules are never included in the peripheral pin select feature. This is because the peripheral's function requires special I/O circuitry on a specific port and cannot be easily connected to multiple pins. These modules include $\rm I^2C$ and the PWM. A similar requirement excludes all modules with analog inputs, such as the A/D converter.

A key difference between remappable and non-remappable peripherals is that remappable peripherals are not associated with a default I/O pin. The peripheral must always be assigned to a specific I/O pin before it can be used. In contrast, non-remappable peripherals are always available on a default pin, assuming that the peripheral is active and not conflicting with another peripheral.

When a remappable peripheral is active on a given I/O pin, it takes priority over all other digital I/O and digital communication peripherals associated with the pin. Priority is given regardless of the type of peripheral that is mapped. Remappable peripherals never take priority over any analog functions associated with the pin.

11.4.3 CONTROLLING PERIPHERAL PIN SELECT

Peripheral pin select features are controlled through two sets of SFRs: one to map peripheral inputs, and one to map outputs. Because they are separately controlled, a particular peripheral's input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

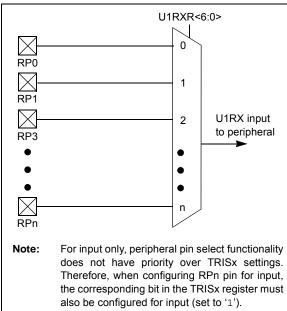
The association of a peripheral to a peripheral-selectable pin is handled in two different ways, depending on whether an input or output is being mapped.

11.4.4 INPUT MAPPING

The inputs of the peripheral pin select options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The RPINRx registers are used to configure peripheral input mapping (see Register 11-1 through Register 11-17). Each register contains sets of 7-bit fields, with each set associated with one of the remappable peripherals. Programming a given peripheral's bit field with an appropriate 7-bit value maps the RPn pin with the corresponding value to that peripheral. For any given device, the valid range of values for any bit field corresponds to the maximum number of peripheral pin selections supported by the device.

For example, Figure 11-2 illustrates remappable pin selection for the U1RX input.

FIGURE 11-2: REMAPPABLE INPUT FOR U1RX



11.4.4.1 Virtual Connections

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X devices support virtual (internal) connections to the output of the Op amp/Comparator module (see Figure 25-1 in Section 25.0 "Op amp/Comparator Module") and the PTG module (see Section 24.0 "Peripheral Trigger Generator (PTG) Module").

In addition, dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices support virtual connections to the filtered QEI module inputs FINDX1, FHOME1, FINDX2 and FHOME2 (see Figure 17-1 in Section 17.0 "Quadrature Encoder Interface (QEI) Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)".

Virtual connections provide a simple way of interperipheral connection without utilizing a physical pin. For example, by setting the FLT1R<6:0> bits of the RPINR12 register to the value of `b00000001, the output of the Analog Comparator C1OUT will be connected to the PWM Fault 1 input, which allows the Analog Comparator to trigger PWM faults without the use of an actual physical pin on the device.

Virtual connection to the QEI module allows peripherals to be connected to the QEI digital filter input. To utilize this filter, the QEI module must be enabled, and its inputs must be connected to a physical RPn pin. Example 11-2 illustrates how the input capture module can be connected to the QEI digital filter.

EXAMPLE 11-2: CONNECTING IC1 TO THE HOME1 QEI1 DIGITAL FILTER INPUT ON PIN 43 OF THE dsPIC33EPXXXMC206 DEVICE

```
RPINR15 = 0x2500; /* Connect the QEI1 HOME1 input to RP37 (pin 43) */
RPINR7 = 0x009; /* Connect the IC1 input to the digital filter on the FHOME1 input */
QEI1IOC = 0x4000; /* Enable the QEI digital filter */
QEI1CON = 0x8000; /* Enable the QEI module */
```

TABLE 11-1: SELECTABLE INPUT SOURCES (MAPS INPUT TO FUNCTION)

Input Name ⁽¹⁾	Function Name	Register	Configuration Bits
External Interrupt 1	INT1	RPINR0	INT1R<6:0>
External Interrupt 2	INT2	RPINR1	INT2R<6:0>
Timer2 External Clock	T2CK	RPINR3	T2CKR<6:0>
Input Capture 1	IC1	RPINR7	IC1R<6:0>
Input Capture 2	IC2	RPINR7	IC2R<6:0>
Input Capture 3	IC3	RPINR8	IC3R<6:0>
Input Capture 4	IC4	RPINR8	IC4R<6:0>
Output Compare Fault A	OCFA	RPINR11	OCFAR<6:0>
PWM Fault 1 ⁽³⁾	FLT1	RPINR12	FLT1R<6:0>
PWM Fault 2 ⁽³⁾	FLT2	RPINR12	FLT2R<6:0>
QEI1 Phase A ⁽³⁾	QEA1	RPINR14	QEA1R<6:0>
QEI1 Phase B ⁽³⁾	QEB1	RPINR14	QEB1R<6:0>
QEI1 Index ⁽³⁾	INDX1	RPINR15	INDX1R<6:0>
QEI1 Home ⁽³⁾	HOME1	RPINR15	HOM1R<6:0>
UART1 Receive	U1RX	RPINR18	U1RXR<6:0>
UART2 Receive	U2RX	RPINR19	U2RXR<6:0>
SPI2 Data Input	SDI2	RPINR22	SDI2R<6:0>
SPI2 Clock Input	SCK2	RPINR22	SCK2R<6:0>
SPI2 Slave Select	SS2	RPINR23	SS2R<6:0>
CAN1 Receive ⁽²⁾	C1RX	RPINR26	C1RXR<6:0>
PWM Synch Input 1 ⁽³⁾	SYNCI1	RPINR37	SYNCI1R<6:0>
PWM Dead Time Compensation 1 ⁽³⁾	DTCMP1	RPINR38	DTCMP1R<6:0>
PWM Dead Time Compensation 2 ⁽³⁾	DTCMP2	RPINR39	DTCMP2R<6:0>
PWM Dead Time Compensation 3 ⁽³⁾	DTCMP3	RPINR39	DTCMP3R<6:0>

- Note 1: Unless otherwise noted, all inputs use the Schmitt input buffers.
 - 2: This input source is available on dsPIC33EPXXXGP/MC50X devices only.
 - 3: This input source is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

TABLE 11-2: INPUT PIN SELECTION FOR SELECTABLE INPUT SOURCES

Peripheral Pin Select Input Register Value	Input/	Pin Assignment	Peripher Select Register
000 0000	I	Vss	010 1
000 0001	I	C1OUT ⁽¹⁾	010 1
000 0010	I	C2OUT ⁽¹⁾	010 1
000 0011	I	C3OUT ⁽¹⁾	011 0
000 0100	I	C4OUT ⁽¹⁾	011 0
000 0101	_	_	011 0
000 0110	I	PTGO30 ⁽¹⁾	011 0
000 0111	I	PTGO31 ⁽¹⁾	011 0
000 1000	I	FINDX1 ^(1,2)	011 0
000 1001	I	FHOME1 ^(1,2)	011 0
000 1010	_	_	011 0
000 1011	_	_	011 1
000 1100	_	_	011 1
000 1101		_	011 1
000 1110	_	_	011 1
000 1111	_	_	011 1
001 0000	_	_	011 1
001 0001	_	_	011 1
001 0010	_	_	011 1
001 0011	_	_	100 0
001 0100	I/O	RP20	100 0
001 0101	_	_	100 0
001 0110	_	_	100 0
001 0111	_	_	100 0
001 1000	I	RPI24	100 0
001 1001	I	RPI25	100 0
001 1010	_	_	100 0
001 1011	I	RPI27	100 1
001 1100	I	RPI28	100 1
001 1101	_	_	100 1
001 1110	_	_	100 1
001 1111	_	_	100 1
010 0000	I	RPI32	100 1
010 0001	I	RPI33	100 1
010 0010	I	RPI34	100 1
010 0011	I/O	RP35	101 0
010 0100	I/O	RP36	101 0
010 0101	I/O	RP37	101 0
010 0110	I/O	RP38	101 0
010 0111	I/O	RP39	101 0
010 1000	I/O	RP40	101 0
010 1001	I/O	RP41	101 0
010 1010	I/O	RP42	101 0
010 1011	I/O	RP43	101 1
		RPI44	_

Peripheral Pin Select Input Register Value	Input/ Output	Pin Assignment
010 1101	ı	RPI45
010 1110	I	RPI46
010 1111	ı	RPI47
011 0000	_	_
011 0001	_	_
011 0010	_	_
011 0011	I	RPI51
011 0100	ı	RPI52
011 0101	I	RPI53
011 0110	I/O	RP54
011 0111	I/O	RP55
011 1000	I/O	RP56
011 1001	I/O	RP57
011 1010	I	RPI58
011 1011	_	_
011 1100	_	_
011 1101	_	_
011 1110	_	_
011 1111	_	_
100 0000	_	_
100 0001	_	_
100 0010	_	_
100 0011	_	_
100 0100	_	_
100 0101	_	_
100 0110	_	_
100 0111	_	_
100 1000	_	_
100 1001	_	_
100 1010	_	_
100 1011	_	_
100 1100		_
100 1101		_
100 1110		_
100 1111	_	_
101 0000	_	_
101 0001		_
101 0010	_	_
101 0011	_	_
101 0100	_	_
101 0101	_	_
101 0110	_	_
101 0111	_	_
101 1000	_	_
101 1001	_	<u>—</u>

Note 1: See Section 11.4.4.1 "Virtual Connections" for more information on selecting this pin assignment.

2: These inputs are available on dsPIC33EPXXXGP/MC50X devices only.

TABLE 11-2: INPUT PIN SELECTION FOR SELECTABLE INPUT SOURCES (CONTINUED)

IABLE 11-2. IN OTT IN SELECTION ON SE						
Peripheral Pin Select Input Register Value	Input/ Output	Pin Assignment				
101 1010	<u> </u>	_				
101 1011	_	_				
101 1100	_	_				
101 1101	_	_				
101 1110	I	RPI94				
101 1111	I	RPI95				
110 0000	I	RPI96				
110 0001	I/O	RP97				
110 0010	_	_				
110 0011	_	_				
110 0100	_	_				
110 0101	_	_				
110 0110		_				
110 0111	_	_				
110 1000		_				
110 1001		_				
110 1010	_	_				
110 1011	_	_				
110 1100	_	_				

Peripheral Pin Select Input Register Value	Input/ Output	Pin Assignment
110 1101	_	_
110 1110	_	_
110 1111	_	_
111 0000	_	_
111 0001	_	_
111 0010	_	_
111 0011	_	_
111 0100	_	_
111 0101	_	_
111 0110	I/O	RP118
111 0111	ı	RPI119
111 1000	I/O	RP120
111 1001	I	RPI121
111 1010	_	_
111 1011	_	_
111 1100	_	_
111 1101	_	_
111 1110	_	_
111 1111	_	_

Note 1: See Section 11.4.4.1 "Virtual Connections" for more information on selecting this pin assignment.

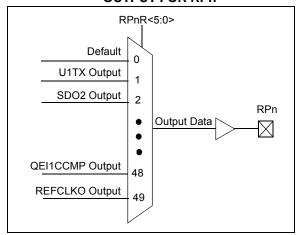
^{2:} These inputs are available on dsPIC33EPXXXGP/MC50X devices only.

11.4.4.2 Output Mapping

In contrast to inputs, the outputs of the peripheral pin select options are mapped on the basis of the pin. In this case, a control register associated with a particular pin dictates the peripheral output to be mapped. The RPORx registers are used to control output mapping. Like the RPINRx registers, each register contains sets of 6 bit fields, with each set associated with one RPn pin (see Register 11-18 through Register 11-27). The value of the bit field corresponds to one of the peripherals, and that peripheral's output is mapped to the pin (see Table 11-3 and Figure 11-3).

A null output is associated with the output register reset value of '0'. This is done to ensure that remappable outputs remain disconnected from all output pins by default.

FIGURE 11-3: MULTIPLEXING REMAPPABLE OUTPUT FOR RPn



11.4.4.3 Mapping Limitations

The control schema of the peripheral select pins is not limited to a small range of fixed peripheral configurations. There are no mutual or hardware-enforced lockouts between any of the peripheral mapping SFRs. Literally any combination of peripheral mappings across any or all of the RPn pins is possible. This includes both many-to-one and one-to-many mappings of peripheral inputs and outputs to pins. While such mappings may be technically possible from a configuration point of view, they may not be supportable from an electrical point of view.

TABLE 11-3: OUTPUT SELECTION FOR REMAPPABLE PINS (RPn)

Function	RPnR<5:0>	Output Name
DEFAULT PORT	000000	RPn tied to default pin
U1TX	000001	RPn tied to UART1 transmit
U2TX	000011	RPn tied to UART2 transmit
SDO2	001000	RPn tied to SPI2 data output
SCK2	001001	RPn tied to SPI2 clock output
SS2	001010	RPn tied to SPI2 slave select
C1TX ⁽²⁾	001110	RPn tied to CAN1 transmit
OC1	010000	RPn tied to Output Compare 1 output
OC2	010001	RPn tied to Output Compare 2 output
OC3	010010	RPn tied to Output Compare 3 output
OC4	010011	RPn tied to Output Compare 4 output
C1OUT	011000	RPn tied to Comparator Output 1
C2OUT	011001	RPn tied to Comparator Output 2
C3OUT	011010	RPn tied to Comparator Output 3
SYNCO1 ⁽¹⁾	101101	RPn tied to PWM primary time base sync output
QEI1CCMP ⁽¹⁾	101111	RPn tied to QEI 1 counter comparator output
REFCLKO	110001	RPn tied to Reference Clock output
C4OUT	110010	RPn tied to Comparator Output 4

Note 1: This function is available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

2: This function is available in dsPIC33EPXXXGP/MC50X devices only.

11.5 I/O Helpful Tips

- 1. In some cases, certain pins as defined in Table 30-10 under "Injection Current", have internal protection diodes to VDD and Vss. The term "Injection Current" is also referred to as "Clamp Current". On designated pins, with sufficient external current limiting precautions by the user, I/O pin input voltages are allowed to be greater or less than the data sheet absolute maximum ratings with respect to the Vss and VDD supplies. Note that when the user application forward biases either of the high or low side internal input clamp diodes, that the resulting current being injected into the device that is clamped internally by the VDD and Vss power rails, may affect the ADC accuracy by four to six counts.
- 2. I/O pins that are shared with any analog input pin, (i.e., ANx), are always analog pins by default after any reset. Consequently, configuring a pin as an analog input pin, automatically disables the digital input pin buffer and any attempt to read the digital input level by reading PORTx or LATx will always return a '0' regardless of the digital logic level on the pin. To use a pin as a digital I/O pin on a shared ANx pin, the user application needs to configure the analog pin configuration registers in the I/O Ports module, (i.e., ANSELx), by setting the appropriate bit that corresponds to that I/O port pin to a '1'.

Note: Although it is not possible to use a digital input pin when its analog function is enabled, it is possible to use the digital I/O output function, TRISx = 0x0, while the analog function is also enabled. However, this is not recommended, particularly if the

analog input is connected to an external analog voltage source, which would create signal contention between the analog signal and the output pin driver.

3. Most I/O pins have multiple functions. Referring to the device pin diagrams in the data sheet, the priorities of the functions allocated to any pins are indicated by reading the pin name from left-to-right. The left most function name takes precedence over any function to its right in the naming convention. For example: AN16/T2CK/T7CK/RC1. This indicates that AN16 is the highest priority in this example and will supersede all other functions to its right in the list. Those other functions to its right, even if enabled, would not work as long as any other function to its left was enabled. This rule applies to all of the functions listed for a given pin.

- 4. Each pin has an internal weak pull-up resistor and pull-down resistor that can be configured using the CNPUx and CNPDx registers, respectively. These resistors eliminate the need for external resistors in certain applications. The internal pull-up is up to ~(VDD-0.8), not VDD. This value is still above the minimum VIH of CMOS and TTL devices.
- 5. When driving LEDs directly, the I/O pin can source or sink more current than what is specified in the VOH/IOH and VOL/IOL DC characteristic specification. The respective IOH and IOL current rating only applies to maintaining the corresponding output at or above the VOH and at or below the VOL levels. However, for LEDs unlike digital inputs of an externally connected device, they are not governed by the same minimum VIH/VIL levels. An I/O pin output can safely sink or source any current less than that listed in the absolute maximum rating section of the data sheet. For example:

VOH = 2.4v @ IOH = -8 mA and VDD = 3.3V

The maximum output current sourced by any 8 mA I/O pin = 12 mA.

LED source current < 12 mA is technically permitted. Refer to the VOH/IOH graphs in Section 30.0 "Electrical Characteristics" for additional information.

11.6 I/O Ports Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:

In the event you are not able to access the product page using the link above, enter this URL in your browser:

http://www.microchip.com/wwwproducts/ Devices.aspx?dDocName=en555464

11.6.1 KEY RESOURCES

- Section 2. "I/O Ports" (DS70598)
- · Code Samples
- Application Notes
- · Software Libraries
- Webinars
- All related dsPIC33E/PIC24E Family Reference Manuals Sections
- · Development Tools

11.7 Peripheral Pin Select Registers

REGISTER 11-1: RPINR0: PERIPHERAL PIN SELECT INPUT REGISTER 0

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_				INT1R<6:0>	•		
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	_	_	_			_	_
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 INT1R<6:0>: Assign External Interrupt 1 (INT1) to the Corresponding RPn Pin bits

(see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121

.

0000001 = Input tied to CMP1 0000000 = Input tied to Vss

bit 7-0 **Unimplemented:** Read as '0'

REGISTER 11-2: RPINR1: PERIPHERAL PIN SELECT INPUT REGISTER 1

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	_	_	_	_	_	_	_
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_				INT2R<6:0>			
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'

bit 6-0 INT2R<6:0>: Assign External Interrupt 2 (INT2) to the Corresponding RPn Pin bits

(see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121

:

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

REGISTER 11-3: RPINR3: PERIPHERAL PIN SELECT INPUT REGISTER 3

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	_	_	_	_	_	_	_
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_				T2CKR<6:0>	•		
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'

bit 6-0 T2CKR<6:0>: Assign Timer2 External Clock (T2CK) to the Corresponding RPn pin bits

(see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121

:

0000001 = Input tied to CMP1 0000000 = Input tied to Vss

REGISTER 11-4: RPINR7: PERIPHERAL PIN SELECT INPUT REGISTER 7

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_				IC2R<6:0>			
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_				IC1R<6:0>			
bit 7					_	_	bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 IC2R<6:0>: Assign Input Capture 2 (IC2) to the Corresponding RPn Pin bits

(see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121

•

0000001 = Input tied to CMP1 0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 IC1R<6:0>: Assign Input Capture 1 (IC1) to the Corresponding RPn Pin bits

(see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121

.

0000001 = Input tied to CMP1 0000000 = Input tied to Vss

REGISTER 11-5: RPINR8: PERIPHERAL PIN SELECT INPUT REGISTER 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_				IC4R<6:0>			
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_				IC3R<6:0>			
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 IC4R<6:0>: Assign Input Capture 4 (IC4) to the Corresponding RPn Pin bits

(see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121

.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 IC3R<6:0>: Assign Input Capture 3 (IC3) to the Corresponding RPn Pin bits

(see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121

:

0000001 = Input tied to CMP1 0000000 = Input tied to Vss

REGISTER 11-6: RPINR11: PERIPHERAL PIN SELECT INPUT REGISTER 11

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	_	_	_	_	_	_	_
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_				OCFAR<6:0>	>		
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'

bit 6-0 OCFAR<6:0>: Assign Output Compare Fault A (OCFA) to the Corresponding RPn Pin bits

(see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121

.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

REGISTER 11-7: RPINR12: PERIPHERAL PIN SELECT INPUT REGISTER 12 (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_				FLT2R<6:0>	•		
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_				FLT1R<6:0>			
bit 7							bit 0

Legend:				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 15 **Unimplemented:** Read as '0'

bit 14-8 FLT2R<6:0>: Assign PWM Fault 2 (FLT2) to the Corresponding RPn Pin bits

(see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121

:

0000001 = Input tied to CMP1 0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 FLT1R<6:0>: Assign PWM Fault 1 (FLT1) to the Corresponding RPn Pin bits

(see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121

.

0000001 = Input tied to CMP1 0000000 = Input tied to Vss

REGISTER 11-8: RPINR14: PERIPHERAL PIN SELECT INPUT REGISTER 14 (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_				QEB1R<6:0>	>		
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_				QEA1R<6:0>	>		
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 QEB1R<6:0>: Assign B (QEB) to the Corresponding RPn Pin bits

(see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121

.

0000001 = Input tied to CMP1 0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **QEA1R<6:0>:** Assign A (QEA) to the Corresponding RPn Pin bits

(see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121

.

0000001 = Input tied to CMP1 0000000 = Input tied to Vss

REGISTER 11-9: RPINR15: PERIPHERAL PIN SELECT INPUT REGISTER 15 (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_				HOME1R<6:0	>		
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_				INDX1R<6:0>	>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 Unimplemented: Read as '0'
bit 14-8 HOME1R<6:0>: Assign QEI1 HOME1 (HOME1) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121
.

. 0000001 = Input tied to CMP1 0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 IND1XR<6:0>: Assign QEI1 INDEX1 (INDX1) to the Corresponding RPn Pin bits

(see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121

.

0000001 = Input tied to CMP1 0000000 = Input tied to Vss

REGISTER 11-10: RPINR18: PERIPHERAL PIN SELECT INPUT REGISTER 18

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	_	_	_	_	_	_	_
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_				U1RXR<6:0>	>		
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'

bit 6-0 U1RXR<6:0>: Assign UART1 Receive (U1RX) to the Corresponding RPn Pin bits

(see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121

.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

REGISTER 11-11: RPINR19: PERIPHERAL PIN SELECT INPUT REGISTER 19

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	_	_	_	_	_	_	_
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_				U2RXR<6:0>	>		
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'

bit 6-0 **U2RXR<6:0>:** Assign UART2 Receive (U2RX) to the Corresponding RPn Pin bits

(see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121

.

0000001 = Input tied to CMP1 0000000 = Input tied to Vss

REGISTER 11-12: RPINR22: PERIPHERAL PIN SELECT INPUT REGISTER 22

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_				SCK2<6:0>			
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_				SDI2<6:0>			
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 SCK2<6:0>: Assign SPI2 Clock Input (SCK2) to the Corresponding RPn Pin bits

(see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121

.

0000001 = Input tied to CMP1 0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 SDI2<6:0>: Assign SPI2 Data Input (SDI2) to the Corresponding RPn Pin bits

(see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121

.

0000001 = Input tied to CMP1 0000000 = Input tied to Vss

REGISTER 11-13: RPINR23: PERIPHERAL PIN SELECT INPUT REGISTER 23

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	_	_	_	_	_	_	_
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_				SS2<6:0>			
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 6-0 **SS2<6:0>:** Assign SPI2 Slave Select (SS2) to the Corresponding RPn Pin bits

(see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121

.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

REGISTER 11-14: RPINR26: PERIPHERAL PIN SELECT INPUT REGISTER 26 (dsPIC33EPXXXGP/MC50X DEVICES ONLY)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	_	_	_	_	_	_	_
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_				C1RXR<6:0>	>		
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'

bit 6-0 C1RXR<6:0>: Assign CAN1 RX Input (CRX1) to the Corresponding RPn Pin bits

(see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121

.

0000001 = Input tied to CMP1 0000000 = Input tied to Vss

REGISTER 11-15: RPINR37: PERIPHERAL PIN SELECT INPUT REGISTER 37 (dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_				SYNCI1R<6:0)>		
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	_	_	_	_	_	_	_
bit 7							bit 0

Legend

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 SYNCI1R<6:0>: Assign PWM Synchronization Input 1 to the Corresponding RPn Pin bits

(see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121

•

0000001 = Input tied to CMP1 0000000 = Input tied to Vss

bit 7-0 **Unimplemented:** Read as '0'

REGISTER 11-16: RPINR38: PERIPHERAL PIN SELECT INPUT REGISTER 38 (dsPIC33EPXXXMC02X AND PIC24EPXXXMC20X DEVICES ONLY)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_				DTCMP1R<6:0)>		
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	_	_	_	_	_	_	_
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **DTCMP1R<6:0>:** Assign PWM Dead Time Compensation Input 1 to the Corresponding RPn Pin bits

(see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121

.

0000001 = Input tied to CMP1 0000000 = Input tied to Vss

bit 7-0 **Unimplemented:** Read as '0'

REGISTER 11-17: RPINR39: PERIPHERAL PIN SELECT INPUT REGISTER 39 (dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_				DTCMP3R<6:0)>		
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_				DTCMP2R<6:0	0>		
bit 7							bit 0

Legend:					
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **DTCMP3R<6:0>:** Assign PWM Dead Time Compensation Input 3 to the Corresponding RPn Pin bits

(see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121

.

. 00000001 = Input tied to CMP1 00000000 = Input tied to Vss

bit 7 Unimplemented: Read as '0'

bit 6-0 **DTCMP2R<6:0>:** Assign PWM Dead Time Compensation Input 2 to the Corresponding RPn Pin bits

(see Table 11-2 for input pin selection numbers)
1111001 = Input tied to RPI121

:

0000001 = Input tied to CMP1 0000000 = Input tied to Vss

REGISTER 11-18: RPOR0: PERIPHERAL PIN SELECT OUTPUT REGISTER 0

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	_			RP35	R<5:0>		
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	_			RP20	R<5:0>		
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 RP35R<5:0>: Peripheral Output Function is Assigned to RP35 Output Pin bits (see Table 11-3 for

peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 RP20R<5:0>: Peripheral Output Function is Assigned to RP20 Output Pin bits (see Table 11-3 for

peripheral function numbers)

REGISTER 11-19: RPOR1: PERIPHERAL PIN SELECT OUTPUT REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	_			RP37	R<5:0>		
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	_			RP36	R<5:0>		
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 RP37R<5:0>: Peripheral Output Function is Assigned to RP37 Output Pin bits (see Table 11-3 for

peripheral function numbers)

bit 7-6 Unimplemented: Read as '0'

bit 5-0 RP36R<5:0>: Peripheral Output Function is Assigned to RP36 Output Pin bits (see Table 11-3 for

peripheral function numbers)

REGISTER 11-20: RPOR2: PERIPHERAL PIN SELECT OUTPUT REGISTER 2

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	_			RP39	R<5:0>		
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	_			RP38	R<5:0>		
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 RP39R<5:0>: Peripheral Output Function is Assigned to RP39 Output Pin bits (see Table 11-3 for

peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 RP38R<5:0>: Peripheral Output Function is Assigned to RP38 Output Pin bits (see Table 11-3 for

peripheral function numbers)

REGISTER 11-21: RPOR3: PERIPHERAL PIN SELECT OUTPUT REGISTER 3

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	_			RP41	R<5:0>		
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	_			RP40	R<5:0>		
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-14 Unimplemented: Read as '0'

bit 13-8 **RP41R<5:0>:** Peripheral Output Function is Assigned to RP41 Output Pin bits (see Table 11-3 for

peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 RP40R<5:0>: Peripheral Output Function is Assigned to RP40 Output Pin bits (see Table 11-3 for

peripheral function numbers)

REGISTER 11-22: RPOR4: PERIPHERAL PIN SELECT OUTPUT REGISTER 4

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	_			RP43	R<5:0>		
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	_			RP42	R<5:0>		
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 RP43R<5:0>: Peripheral Output Function is Assigned to RP43 Output Pin bits (see Table 11-3 for

peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 RP42R<5:0>: Peripheral Output Function is Assigned to RP42 Output Pin bits (see Table 11-3 for

peripheral function numbers)

REGISTER 11-23: RPOR5: PERIPHERAL PIN SELECT OUTPUT REGISTER 5

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	_			RP55	R<5:0>		
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	_			RP54	R<5:0>		
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-14 Unimplemented: Read as '0'

bit 13-8 RP55R<5:0>: Peripheral Output Function is Assigned to RP55 Output Pin bits (see Table 11-3 for

peripheral function numbers)

bit 7-6 Unimplemented: Read as '0'

bit 5-0 RP54R<5:0>: Peripheral Output Function is Assigned to RP54 Output Pin bits (see Table 11-3 for

peripheral function numbers)

REGISTER 11-24: RPOR6: PERIPHERAL PIN SELECT OUTPUT REGISTER 6

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	_			RP57	R<5:0>		
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	_			RP56	R<5:0>		
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 RP57R<5:0>: Peripheral Output Function is Assigned to RP57 Output Pin bits (see Table 11-3 for

peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 RP56R<5:0>: Peripheral Output Function is Assigned to RP56 Output Pin bits (see Table 11-3 for

peripheral function numbers)

REGISTER 11-25: RPOR7: PERIPHERAL PIN SELECT OUTPUT REGISTER 7

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	_			RP97	R<5:0>		
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_			-		-		_
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-14 Unimplemented: Read as '0'

bit 13-8 RP97R<5:0>: Peripheral Output Function is Assigned to RP97 Output Pin bits (see Table 11-3 for

peripheral function numbers)

bit 7-0 **Unimplemented:** Read as '0'

REGISTER 11-26: RPOR8: PERIPHERAL PIN SELECT OUTPUT REGISTER 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	_			RP118	3R<5:0>		
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	_	_	_	_	_	_	_
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-14 Unimplemented: Read as '0'

bit 13-8 RP118R<5:0>: Peripheral Output Function is Assigned to RP118 Output Pin bits (see Table 11-3 for

peripheral function numbers)

bit 7-0 **Unimplemented:** Read as '0'

REGISTER 11-27: RPOR9: PERIPHERAL PIN SELECT OUTPUT REGISTER 9

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	_	_	_	_	_	_	_
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	_			RP120	0R<5:0>		
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-6 Unimplemented: Read as '0'

bit 5-0 RP120R<5:0>: Peripheral Output Function is Assigned to RP120 Output Pin bits (see Table 11-3 for

peripheral function numbers)

12.0 TIMER1

This data sheet summarizes the features Note 1: dsPIC33EPXXXGP50X, the dsPIC33EPXXXMC20X/50X. and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 11. "Timers' (DS70362) of the "dsPIC33E/PIC24E Family Reference Manual', which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The Timer1 module is a 16-bit timer that can operate as a free-running interval timer/counter.

The Timer1 module has the following unique features over other timers:

- Can be operated in Asynchronous Counter mode from an external clock source
- The external clock input (T1CK) can optionally be synchronized to the internal device clock and the clock synchronization is performed after the prescaler

A block diagram of Timer1 is shown in Figure 12-1.

The Timer1 module can operate in one of the following modes:

- · Timer mode
- · Gated Timer mode
- · Synchronous Counter mode
- Asynchronous Counter mode

In Timer and Gated Timer modes, the input clock is derived from the internal instruction cycle clock (FcY). In Synchronous and Asynchronous Counter modes, the input clock is derived from the external clock input at the T1CK pin.

The Timer modes are determined by the following bits:

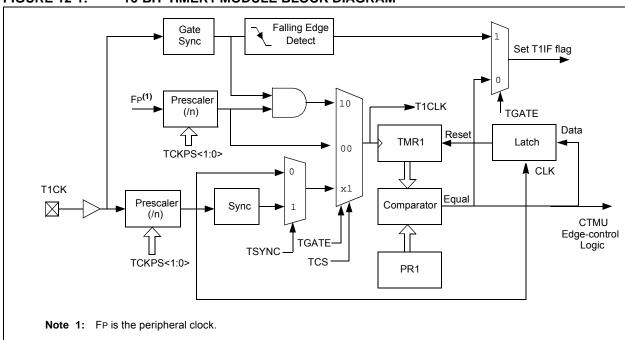
- Timer Clock Source Control bit (TCS): T1CON<1>
- Timer Synchronization Control bit (TSYNC): T1CON<2>
- Timer Gate Control bit (TGATE): T1CON<6>

Timer control bit setting for different operating modes are given in the Table 12-1.

TABLE 12-1: TIMER MODE SETTINGS

Mode	TCS	TGATE	TSYNC
Timer	0	0	х
Gated timer	0	1	х
Synchronous counter	1	х	1
Asynchronous counter	1	х	0

FIGURE 12-1: 16-BIT TIMER1 MODULE BLOCK DIAGRAM



12.1 Timer1 Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:

In the event you are not able to access the product page using the link above, enter this URL in your browser:

http://www.microchip.com/wwwproducts/ Devices.aspx?dDocName=en555464

12.1.1 KEY RESOURCES

- Section 11. "Timers" (DS70362)
- · Code Samples
- · Application Notes
- · Software Libraries
- Webinars
- All related dsPIC33E/PIC24E Family Reference Manuals Sections
- · Development Tools

12.2 Timer1 Control Register

REGISTER 12-1: T1CON: TIMER1 CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
TON ⁽¹⁾	_	TSIDL	_	_	_	_	_
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0
_	TGATE	TCKPS	S<1:0>	_	TSYNC ⁽¹⁾	TCS ⁽¹⁾	_
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15 TON: Timer1 On bit

1 = Starts 16-bit Timer1

0 = Stops 16-bit Timer1

bit 14 **Unimplemented:** Read as '0'

bit 13 TSIDL: Stop in Idle Mode bit

1 = Discontinue module operation when device enters Idle mode

0 = Continue module operation in Idle mode

bit 12-7 Unimplemented: Read as '0'

bit 6 TGATE: Timer1 Gated Time Accumulation Enable bit

When TCS = 1: This bit is ignored.

When TCS = 0:

1 = Gated time accumulation enabled0 = Gated time accumulation disabled

bit 5-4 TCKPS<1:0>: Timer1 Input Clock Prescale Select bits

11 = 1:256

10 = 1:64

01 = 1:8

00 = 1:1

bit 3 **Unimplemented:** Read as '0'

bit 2 TSYNC: Timer1 External Clock Input Synchronization Select bit

When TCS = 1:

1 = Synchronize external clock input

0 = Do not synchronize external clock input

When TCS = 0:

This bit is ignored.

bit 1 TCS: Timer1 Clock Source Select bit

1 = External clock from pin T1CK (on the rising edge)

0 = Internal clock (FP)

bit 0 Unimplemented: Read as '0'

Note 1: When Timer1 is enabled in external synchronous counter mode (TCS = 1, TSYNC = 1, TON = 1), any attempts by user software to write to the TMR1 register is ignored.

13.0 TIMER2/3 AND TIMER4/5

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 11. "Timers" (DS70362) of the "dsPIC33E/PIC24E Family Reference Manual", which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The Timer2/3 and Timer4/5 modules are 32-bit timers, which can also be configured as four independent 16-bit timers with selectable operating modes.

As a 32-bit timer, Timer2/3 and Timer4/5 operate in three modes:

- Two Independent 16-bit Timers (e.g., Timer2 and Timer3) with all 16-bit operating modes (except Asynchronous Counter mode)
- · Single 32-bit Timer
- · Single 32-bit Synchronous Counter

They also support these features:

- · Timer Gate Operation
- · Selectable Prescaler Settings
- · Timer Operation during Idle and Sleep modes
- Interrupt on a 32-bit Period Register Match
- Time Base for Input Capture and Output Compare Modules (Timer2 and Timer3 only)
- ADC1 Event Trigger (Timer2/3 only)

Individually, all four of the 16-bit timers can function as synchronous timers or counters. They also offer the features listed above, except for the event trigger; this is implemented only with Timer2/3. The operating modes and enabled features are determined by setting the appropriate bit(s) in the T2CON, T3CON, and T4CON, T5CON registers. T2CON and T4CON are shown in generic form in Register 13-1. T3CON and T5CON are shown in Register 13-2.

For 32-bit timer/counter operation, Timer2 and Timer4 are the least significant word (lsw); Timer3 and Timer5 are the most significant word (msw) of the 32-bit timers.

Note: For 32-bit operation, T3CON and T5CON control bits are ignored. Only T2CON and T4CON control bits are used for setup and control. Timer2 and Timer4 clock and gate inputs are utilized for the 32-bit timer modules, but an interrupt is generated with the Timer3 and Timer5 interrupt flags.

A block diagram for an example 32-bit timer pair (Timer2/3 and Timer4/5) is shown in Figure 13-3.

Note: Only Timer2, 3, 4 and 5 can trigger a DMA data transfer.

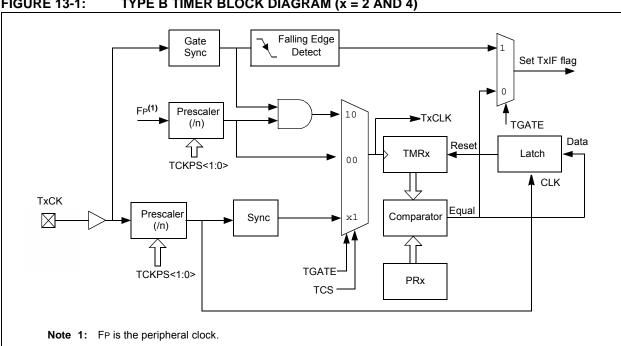
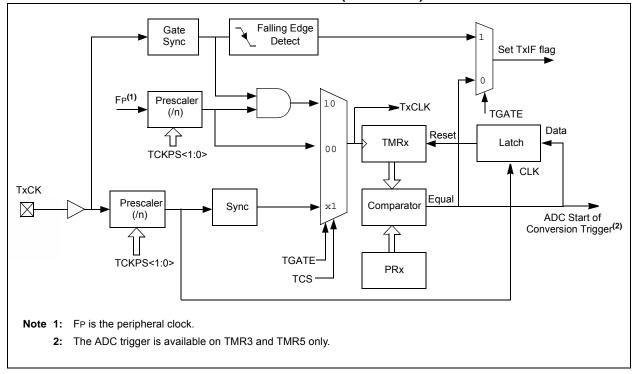


FIGURE 13-1: TYPE B TIMER BLOCK DIAGRAM (x = 2 AND 4)

FIGURE 13-2: TYPE C TIMER BLOCK DIAGRAM (x = 3 AND 5)



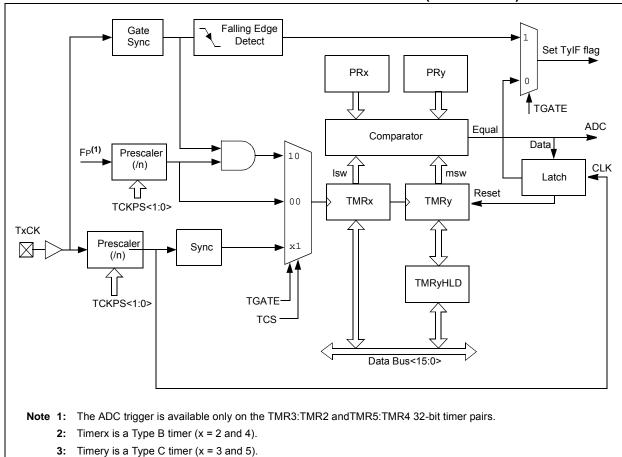


FIGURE 13-3: TYPE B/TYPE C TIMER PAIR BLOCK DIAGRAM (32-BIT TIMER)

13.1 Timer Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter this URL in your browser:
http://www.microchip.com/wwwprod-ucts/Devices.aspx?dDoc-Name=en555464

13.1.1 KEY RESOURCES

- Section 11. "Timers" (DS70362)
- · Code Samples
- · Application Notes
- · Software Libraries
- Webinars
- All related dsPIC33E/PIC24E Family Reference Manuals Sections
- · Development Tools

13.2 Timer Control Registers

REGISTER 13-1: TxCON (T2CON AND T4CON) CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
TON	_	TSIDL	_	_	_	_	_
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0
_	TGATE	TCKPS<1:0>		T32	_	TCS ⁽¹⁾	_
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15 TON: Timerx On bit

When T32 = 1:

1 = Starts 32-bit Timerx/y 0 = Stops 32-bit Timerx/y

When T32 = 0:

1 = Starts 16-bit Timerx

0 = Stops 16-bit Timerx

bit 14 **Unimplemented:** Read as '0'

bit 13 TSIDL: Stop in Idle Mode bit

1 = Discontinue module operation when device enters Idle mode

0 = Continue module operation in Idle mode

bit 12-7 Unimplemented: Read as '0'

bit 6 TGATE: Timerx Gated Time Accumulation Enable bit

When TCS = 1: This bit is ignored.

When TCS = 0:

1 = Gated time accumulation enabled0 = Gated time accumulation disabled

bit 5-4 TCKPS<1:0>: Timerx Input Clock Prescale Select bits

11 = 1:256

10 = 1:64

01 = 1:8

00 = 1:1

bit 3 T32: 32-bit Timer Mode Select bit

1 = Timerx and Timery form a single 32-bit timer

0 = Timerx and Timery act as two 16-bit timers

bit 2 **Unimplemented:** Read as '0'

bit 1 TCS: Timerx Clock Source Select bit⁽¹⁾

1 = External clock from pin TxCK (on the rising edge)

0 = Internal clock (FP)

bit 0 **Unimplemented:** Read as '0'

Note 1: The TxCK pin is not available on all timers. Refer to the "Pin Diagrams" section for the available pins.

REGISTER 13-2: TyCON (T3CON AND T5CON) CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
TON ⁽¹⁾	_	TSIDL ⁽²⁾	_	_	_	_	_
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	U-0
_	TGATE ⁽¹⁾	TCKPS<1:0>(1)		_	_	TCS ^(1,3)	_
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit,	read as '0'
-n = Value at POR	'1' = Rit is set	'0' = Rit is cleared	v = Rit is unknown

bit 15 **TON:** Timery On bit⁽¹⁾

1 = Starts 16-bit Timery
0 = Stops 16-bit Timery

bit 14 **Unimplemented:** Read as '0' bit 13 **TSIDL:** Stop in Idle Mode bit⁽²⁾

1 = Discontinue module operation when device enters Idle mode

0 = Continue module operation in Idle mode

bit 12-7 **Unimplemented:** Read as '0'

bit 6 **TGATE**: Timery Gated Time Accumulation Enable bit⁽¹⁾

 $\frac{\text{When TCS} = 1:}{\text{This bit is ignored.}}$

When TCS = 0:

1 = Gated time accumulation enabled 0 = Gated time accumulation disabled

bit 5-4 TCKPS<1:0>: Timery Input Clock Prescale Select bits⁽¹⁾

11 = 1:256 10 = 1:64 01 = 1:8 00 = 1:1

bit 3-2 **Unimplemented:** Read as '0'

bit 1 TCS: Timery Clock Source Select bit(1,3)

1 = External clock from pin TyCK (on the rising edge)

0 = Internal clock (FP)

bit 0 **Unimplemented:** Read as '0'

Note 1: When 32-bit operation is enabled (T2CON<3> = 1), these bits have no effect on Timery operation; all timer functions are set through TxCON.

- 2: When 32-bit timer operation is enabled (T32 = 1) in the Timer Control register (TxCON<3>), the TSIDL bit must be cleared to operate the 32-bit timer in Idle mode.
- 3: The TyCK pin is not available on all timers. See "Pin Diagrams" section for the available pins.

14.0 INPUT CAPTURE

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 12. "Input Capture" (DS70352) of the "dsPIC33E/PIC24E Family Reference Manual", which is available from the Microchip web site (www.microchip.com).

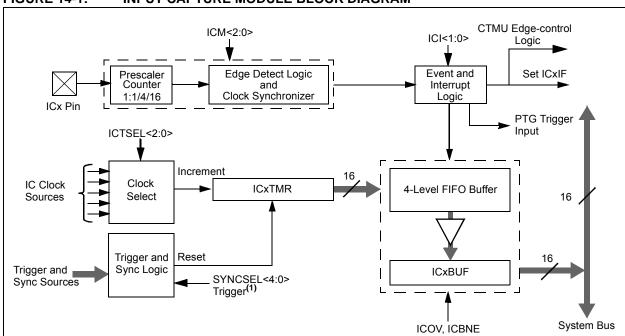
2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The Input Capture module is useful in applications requiring frequency (period) and pulse measurement. The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X devices support up to 4 input capture channels.

Key features of the Input Capture module include:

- Hardware-configurable for 32-bit operation in all modes by cascading two adjacent modules
- Synchronous and Trigger modes of output compare operation, with up to 31 user-selectable trigger/sync sources available
- A 4-level FIFO buffer for capturing and holding timer values for several events
- · Configurable interrupt generation
- Up to six clock sources available for each module, driving a separate internal 16-bit counter

FIGURE 14-1: INPUT CAPTURE MODULE BLOCK DIAGRAM



Note 1: The Trigger/Sync source is enabled by default and is set to Timer3 as a source. This timer must be enabled for proper ICx module operation or the Trigger/Sync source must be changed to another source option.

14.1 Input Capture Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:

In the event you are not able to access the product page using the link above, enter this URL in your browser:

http://www.microchip.com/wwwproducts/ Devices.aspx?dDocName=en555464

14.1.1 KEY RESOURCES

- Section 12. "Input Capture" (DS70352)
- · Code Samples
- · Application Notes
- · Software Libraries
- Webinars
- All related dsPIC33E/PIC24E Family Reference Manuals Sections
- · Development Tools

14.2 Input Capture Registers

REGISTER 14-1: ICxCON1: INPUT CAPTURE x CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
_	_	ICSIDL		ICTSEL<2:0>		_	_
bit 15	_		_				bit 8

U-0	R/W-0	R/W-0	R/HC/HS-0	R/HC/HS-0	R/W-0	R/W-0	R/W-0
_	ICI<	<1:0>	ICOV	ICBNE		ICM<2:0>	
bit 7							bit 0

Legend:

bit 15-14 Unimplemented: Read as '0'

bit 13 ICSIDL: Input Capture Stop in Idle Control bit

1 = Input capture will Halt in CPU Idle mode

0 = Input capture will continue to operate in CPU Idle mode

bit 12-10 ICTSEL<12:10>: Input Capture Timer Select bits

111 = Peripheral clock (FP) is the clock source of the ICx

110 = Reserved 101 = Reserved

100 = T1CLK is the clock source of the ICx (only the synchronous clock is supported)

011 = T5CLK is the clock source of the ICx 010 = T4CLK is the clock source of the ICx 001 = T2CLK is the clock source of the ICx

000 = T3CLK is the clock source of the ICx

bit 9-7 **Unimplemented:** Read as '0'

bit 6-5 **ICI<1:0>:** Number of Captures per Interrupt Select bits

(this field is not used if ICM<2:0> = 001 or 111) 11 = Interrupt on every fourth capture event

10 = Interrupt on every third capture event

01 = Interrupt on every second capture event

00 = Interrupt on every capture event

bit 4 ICOV: Input Capture Overflow Status Flag bit (read-only)

1 = Input capture buffer overflow occurred0 = No input capture buffer overflow occurred

bit 3 ICBNE: Input Capture Buffer Not Empty Status bit (read-only)

1 = Input capture buffer is not empty, at least one more capture value can be read

0 = Input capture buffer is empty

bit 2-0 ICM<2:0>: Input Capture Mode Select bits

111 = Input capture functions as interrupt pin only in CPU Sleep and Idle mode (rising edge detect only, all other control bits are not applicable)

110 = Unused (module disabled)

101 = Capture mode, every 16th rising edge (Prescaler Capture mode)

100 = Capture mode, every 4th rising edge (Prescaler Capture mode)

011 = Capture mode, every rising edge (Simple Capture mode)

010 = Capture mode, every falling edge (Simple Capture mode)

001 = Capture mode, every edge, rising and falling (Edge Detect mode (ICI<1:0>) is not used in this mode)

000 = Input Capture module is turned off

REGISTER 14-2: ICxCON2: INPUT CAPTURE x CONTROL REGISTER 2

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
_	_	_	_	_	_	_	IC32
bit 15							bit 8

R/W-0	R/W/HS-0	U-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-1
ICTRIG ⁽²⁾	TRIGSTAT ⁽³⁾	_		SY	YNCSEL<4:0>	•	
bit 7	•						bit 0

Legend:

R = Readable bit HS = Set by Hardware '0' = Bit is cleared

-n = Value at POR W = Writable bit U = Unimplemented bit, read as '0'

bit 15-9 **Unimplemented:** Read as '0'

bit 8 IC32: 32-bit Timer Mode Select bit (Cascade mode)

1 = ODD IC and EVEN IC form a single 32-bit Input Capture module⁽¹⁾

0 = Cascade module operation disabled

bit 7 ICTRIG: Trigger Operation Select bit⁽²⁾

1 = Input source used to trigger the input capture timer (Trigger mode)

0 = Input source used to synchronize input capture timer to timer of another module

(Synchronization mode)

bit 6 TRIGSTAT: Timer Trigger Status bit⁽³⁾

1 = ICxTMR has been triggered and is running

0 = ICxTMR has not been triggered and is being held clear

bit 5 **Unimplemented:** Read as '0'

Note 1: The IC32 bit in both the ODD and EVEN IC must be set to enable Cascade mode.

2: The input source is selected by the SYNCSEL<4:0> bits of the ICxCON2 register.

3: This bit is set by the selected input source (selected by SYNCSEL<4:0> bits). It can be read, set, and cleared in software.

4: Do not use the ICx module as its own sync or trigger source.

5: This option should only be selected as trigger source and not as a synchronization source.

6: Each Input Capture module (ICx) has one PTG input source. See Section 24.0 "Peripheral Trigger Generator (PTG) Module" for more information.

PTGO8 = IC1

PTGO9 = IC2

PTGO10 = IC3

PTGO11 = IC4

REGISTER 14-2: ICxCON2: INPUT CAPTURE x CONTROL REGISTER 2 (CONTINUED)

```
SYNCSEL<4:0>: Input Source Select for Synchronization and Trigger Operation bits<sup>(4)</sup>
bit 4-0
              11111 = No sync or trigger source for ICx
              11110 = Reserved
              11101 = Reserved
              11100 = CTMU module synchronizes or triggers ICx
              11011 = ADC1 module synchronizes or triggers ICx^{(5)}
              11010 = CMP3 module synchronizes or triggers ICx^{(5)}
              11001 = CMP2 module synchronizes or triggers ICx<sup>(5)</sup>
              11000 = CMP1 module synchronizes or triggers ICx<sup>(5)</sup>
              10111 = Reserved
              10110 = Reserved
              10101 = Reserved
              10100 = Reserved
              10011 = IC4 module synchronizes or triggers ICx
              10010 = IC3 module synchronizes or triggers ICx
              10001 = IC2 module synchronizes or triggers ICx
              10000 = IC1 module synchronizes or triggers ICx
              01111 = Timer5 synchronizes or triggers ICx
              01110 = Timer4 synchronizes or triggers ICx
               01101 = Timer3 synchronizes or triggers ICx (default)
              01100 = Timer2 synchronizes or triggers ICx
              01011 = Timer1 synchronizes or triggers ICx
              01010 = PTGOx module synchronizes or triggers ICx<sup>(6)</sup>
              01001 = Reserved
              01000 = Reserved
              00111 = Reserved
              00110 = Reserved
              00101 = Reserved
              00100 = OC4 module synchronizes or triggers ICx
              00011 = OC3 module synchronizes or triggers ICx
```

Note 1: The IC32 bit in both the ODD and EVEN IC must be set to enable Cascade mode.

00010 = OC2 module synchronizes or triggers ICx 00001 = OC1 module synchronizes or triggers ICx

- 2: The input source is selected by the SYNCSEL<4:0> bits of the ICxCON2 register.
- 3: This bit is set by the selected input source (selected by SYNCSEL<4:0> bits). It can be read, set, and cleared in software.
- 4: Do not use the ICx module as its own sync or trigger source.

00000 = No sync or trigger source for ICx

- **5:** This option should only be selected as trigger source and not as a synchronization source.
- 6: Each Input Capture module (ICx) has one PTG input source. See Section 24.0 "Peripheral Trigger Generator (PTG) Module" for more information.

PTGO8 = IC1 PTGO9 = IC2 PTGO10 = IC3 PTGO11 = IC4

15.0 OUTPUT COMPARE

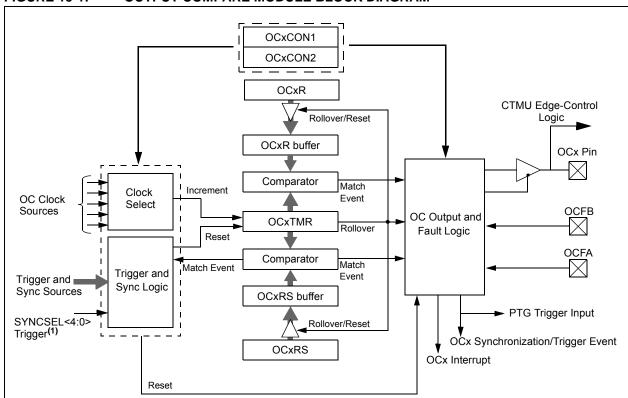
Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 13. "Output Compare" (DS70358) of the "dsPIC33E/PIC24E Family Reference Manual", which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The Output Compare module can select one of eight available clock sources for its time base. The module compares the value of the timer with the value of one or two compare registers depending on the operating mode selected. The state of the output pin changes when the timer value matches the compare register value. The output compare module generates either a single output pulse or a sequence of output pulses, by changing the state of the output pin on the compare match events. The output compare module can also generate interrupts on compare match events and trigger DMA data transfers.

Note: See Section 13. "Output Compare" (DS70358) in the "dsPIC33E/PIC24E Family Reference Manual" for OCxR and OCxRS register restrictions.

FIGURE 15-1: OUTPUT COMPARE MODULE BLOCK DIAGRAM



Note 1: The Trigger/Sync source is enabled by default and is set to Timer2 as a source. This timer must be enabled for proper OCx module operation or the Trigger/Sync source must be changed to another source option.

15.1 Output Compare Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:

In the event you are not able to access the product page using the link above, enter this URL in your browser:

http://www.microchip.com/wwwproducts/ Devices.aspx?dDocName=en555464

15.1.1 KEY RESOURCES

- Section 13. "Output Compare" (DS70358)
- · Code Samples
- · Application Notes
- · Software Libraries
- · Webinars
- All related dsPIC33E/PIC24E Family Reference Manuals Sections
- · Development Tools

15.2 Output Compare Control Registers

REGISTER 15-1: OCxCON1: OUTPUT COMPAREX CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
_	_	OCSIDL		OCTSEL<2:0>	>	_	ENFLTB
bit 15							bit 8

R/W-0	U-0	R/W-0 HCS	R/W-0 HCS	R/W-0	R/W-0	R/W-0	R/W-0
ENFLTA	_	OCFLTB	OCFLTA	TRIGMODE		OCM<2:0>	
bit 7							bit 0

Legend:	HCS = Hardware Clearable	HCS = Hardware Clearable/Settable bit				
R = Readable bit	W = Writable bit U = Unimplemented bit, read as '0'					
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown			

bit 15-14 **Unimplemented:** Read as '0'

bit 13 OCSIDL: Stop Output Compare x in Idle Mode Control bit

1 = Output Compare x halts in CPU Idle mode

0 = Output Compare x continues to operate in CPU Idle mode

bit 12-10 OCTSEL<2:0>: Output Compare x Clock Select bits

111 = Peripheral clock (FP)

110 = Reserved

101 = PTGOx clock⁽²⁾

100 = T1CLK is the clock source of the OCx (only the synchronous clock is supported)

011 = T5CLK is the clock source of the OCx

010 = T4CLK is the clock source of the OCx

001 = T3CLK is the clock source of the OCx

000 = T2CLK is the clock source of the OCx

bit 9 Unimplemented: Read as '0'

bit 8 **ENFLTB:** Fault B Input Enable bit

1 = Output Compare Fault B input (OCFB) is enabled

0 = Output Compare Fault B input (OCFB) is disabled

bit 7 ENFLTA: Fault A Input Enable bit

bit 6

1 = Output Compare Fault A input (OCFA) is enabled 0 = Output Compare Fault A input (OCFA) is disabled

Unimplemented: Read as '0'

bit 5 OCFLTB: PWM Fault B Condition Status bit

1 = PWM Fault B condition on OCFB pin has occurred

0 = No PWM Fault B condition on OCFB pin has occurred

bit 4 OCFLTA: PWM Fault A Condition Status bit

1 = PWM Fault A condition on OCFA pin has occurred

0 = No PWM Fault A condition on OCFA pin has occurred

bit 3 TRIGMODE: Trigger Status Mode Select bit

1 = TRIGSTAT (OCxCON2<6>) is cleared when OCxRS = OCxTMR or in software

0 = TRIGSTAT is cleared only by software

Note 1: OCxR and OCxRS are double-buffered in PWM mode only.

2: Each Output Compare module (OCx) has one PTG clock source. See Section 24.0 "Peripheral Trigger Generator (PTG) Module" for more information.

PTGO4 = OC1

PTGO5 = OC2

PTGO6 = OC3

PTG07 = 0C4

REGISTER 15-1: OCXCON1: OUTPUT COMPAREX CONTROL REGISTER 1 (CONTINUED)

- bit 2-0 OCM<2:0>: Output Compare Mode Select bits
 - 111 = Center-Aligned PWM mode: Output set high when OCxTMR = OCxR and set low when OCxTMR = OCxRS⁽¹⁾
 - 110 = Edge-Aligned PWM mode: Output set high when OCxTMR = 0 and set low when OCxTMR = OCxR⁽¹⁾
 - 101 = Double Compare Continuous Pulse mode: Initialize OCx pin low, toggle OCx state continuously on alternate matches of OCxR and OCxRS
 - 100 = Double Compare Single-Shot mode: Initialize OCx pin low, toggle OCx state on matches of OCxR and OCxRS for one cycle
 - 011 = Single Compare mode: Compare events with OCxR, continuously toggle OCx pin
 - 010 = Single Compare Single-Shot mode: Initialize OCx pin high, compare event with OCxR, forces OCx pin low
 - 001 = Single Compare Single-Shot mode: Initialize OCx pin low, compare event with OCxR, forces OCx pin high
 - 000 = Output compare channel is disabled
- Note 1: OCxR and OCxRS are double-buffered in PWM mode only.
 - 2: Each Output Compare module (OCx) has one PTG clock source. See Section 24.0 "Peripheral Trigger Generator (PTG) Module" for more information.

PTGO4 = OC1

PTGO5 = OC2

PTGO6 = OC3

PTG07 = 0C4

REGISTER 15-2: OCxCON2: OUTPUT COMPARE x CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0
FLTMD	FLTOUT	FLTTRIEN	OCINV	_	_	_	OC32
bit 15							bit 8

R/W-0	R/W-0 HS	R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0
OCTRIG	TRIGSTAT	OCTRIS		;	SYNCSEL<4:0	>	
bit 7							bit 0

Legend:	HS = Hardware Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 FLTMD: Fault Mode Select bit

1 = Fault mode is maintained until the Fault source is removed; the corresponding OCFLTx bit is cleared in software and a new PWM period starts

0 = Fault mode is maintained until the Fault source is removed and a new PWM period starts

bit 14 FLTOUT: Fault Out bit

1 = PWM output is driven high on a Fault

0 = PWM output is driven low on a Fault

bit 13 FLTTRIEN: Fault Output State Select bit

1 = OCx pin is tri-stated on Fault condition

0 = OCx pin I/O state defined by FLTOUT bit on Fault condition

bit 12 OCINV: OCMP Invert bit

1 = OCx output is inverted

0 = OCx output is not inverted

bit 11-9 **Unimplemented:** Read as '0'

bit 8 OC32: Cascade Two OCx Modules Enable bit (32-bit operation)

1 = Cascade module operation enabled

0 = Cascade module operation disabled

bit 7 OCTRIG: OCx Trigger/Sync Select bit

1 = Trigger OCx from source designated by SYNCSELx bits

0 = Synchronize OCx with source designated by SYNCSELx bits

bit 6 TRIGSTAT: Timer Trigger Status bit

1 = Timer source has been triggered and is running

0 = Timer source has not been triggered and is being held clear

bit 5 OCTRIS: OCx Output Pin Direction Select bit

1 = OCx is tri-stated

0 = Output compare module drives the OCx pin

Note 1: Do not use the OCx module as its own synchronization or trigger source.

2: When the OCy module is turned OFF, it sends a trigger out signal. If the OCx module use the OCy module as a trigger source, the OCy module must be unselected as a trigger source prior to disabling it.

3: Each Output Compare module (OCx) has one PTG Trigger/Synchronization source. See Section 24.0 "Peripheral Trigger Generator (PTG) Module" for more information.

PTGO0 = OC1

PTGO1 = OC2

PTGO2 = OC3

PTGO3 = OC4

REGISTER 15-2: OCxCON2: OUTPUT COMPARE x CONTROL REGISTER 2 (CONTINUED)

```
bit 4-0
              SYNCSEL<4:0>: Trigger/Synchronization Source Selection bits
```

```
11111 = No sync or trigger source for OCx
11110 = INT2 pin synchronizes or triggers OCx
11101 = INT1 pin synchronizes or triggers OCx
11100 = CTMU module synchronizes or triggers OCx
11011 = ADC1 module synchronizes or triggers OCx
11010 = CMP3 module synchronizes or triggers OCx
11001 = CMP2 module synchronizes or triggers OCx
11000 = CMP1 module synchronizes or triggers OCx
10111 = Reserved
10110 = Reserved
10101 = Reserved
10100 = Reserved
10011 = IC4 module synchronizes or triggers OCx
10010 = IC3 module synchronizes or triggers OCx
10001 = IC2 module synchronizes or triggers OCx
10000 = IC1 module synchronizes or triggers OCx
01111 = Timer5 synchronizes or triggers OCx
01110 = Timer4 synchronizes or triggers OCx
01101 = Timer3 synchronizes or triggers OCx
01100 = Timer2 synchronizes or triggers OCx (default)
01011 = Timer1 synchronizes or triggers OCx
```

01010 = PTGOx synchronizes or trigger $OCx^{(3)}$

01001 = Reserved

01000 = Reserved

00111 = Reserved

00110 = Reserved

00101 = Reserved

00100 = OC4 module synchronizes or triggers $OCx^{(1,2)}$

00011 = OC3 module synchronizes or triggers $OCx^{(1,2)}$

00010 = OC2 module synchronizes or triggers $OCx^{(1,2)}$

00001 = OC1 module synchronizes or triggers $OCx^{(1,2)}$

00000 = No sync or trigger source for OCx

Note 1: Do not use the OCx module as its own synchronization or trigger source.

- 2: When the OCy module is turned OFF, it sends a trigger out signal. If the OCx module use the OCy module as a trigger source, the OCy module must be unselected as a trigger source prior to disabling it.
- Each Output Compare module (OCx) has one PTG Trigger/Synchronization source. See Section 24.0 "Peripheral Trigger Generator (PTG) Module" for more information.

PTGO0 = OC1

PTGO1 = OC2

PTGO2 = OC3

PTGO3 = OC4

16.0 HIGH-SPEED PWM MODULE (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 14. "High-Speed PWM" (DS70645) of the "dsPIC33E/PIC24E Family Reference Manual", which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices support a dedicated Pulse-Width Modulation (PWM) module with up to 6 outputs.

The High-Speed PWM module consists of the following major features:

- · Three PWM generators
- Two PWM outputs per PWM generator
- · Individual period and duty cycle for each PWM pair
- Duty cycle, dead time, phase shift and frequency resolution of 8.32 ns
- Independent Fault and current-limit inputs for six PWM outputs
- Redundant output
- · Center-Aligned PWM mode
- · Output override control
- Chop mode (also known as Gated mode)
- · Special Event Trigger
- Prescaler for input clock
- · PWMxL and PWMxH output pin swapping
- Independent PWM frequency, duty cycle and phase shift changes for each PWM generator
- · Dead-time compensation
- Enhanced Leading-Edge Blanking (LEB) functionality
- · Frequency resolution enhancement
- PWM capture functionality

Note: In Edge-Aligned PWM mode, the duty cycle, dead-time, phase shift and frequency resolution are 8.32 ns.

The High-Speed PWM module contains up to three PWM generators. Each PWM generator provides two PWM outputs: PWMxH and PWMxL. The master time base generator provides a synchronous signal as a common time base to synchronize the various PWM outputs. The individual PWM outputs are available on the output pins of the device. The input Fault signals and current-limit signals, when enabled, can monitor and protect the system by placing the PWM outputs into a known "safe" state.

Each PWM can generate a trigger to the ADC module to sample the analog signal at a specific instance during the PWM period. In addition, the High-Speed PWM module also generates a Special Event Trigger to the ADC module based on either of the two master time bases.

The High-Speed PWM module can synchronize itself with an external signal or can act as a synchronizing source to any external device. The SYNCI1 input pin that utilizes PPS, can synchronize the High-Speed PWM module with an external signal. The SYNCO1 pin is an output pin that provides a synchronous signal to an external device.

Figure 16-1 illustrates an architectural overview of the High-Speed PWM module and its interconnection with the CPU and other peripherals.

16.1 PWM Faults

The PWM module incorporates multiple external Fault inputs to include $\overline{FLT1}$ and $\overline{FLT2}$, which are remappable using the PPS feature, $\overline{FLT3}$ and $\overline{FLT4}$, which are available only on the larger 44-pin and 64-pin packages, and $\overline{FLT32}$, which has been implemented with Class B safety features, and is available on a fixed pin on all dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

These faults provide a safe and reliable way to safely shut down the PWM outputs when the Fault input is asserted.

16.1.1 PWM FAULTS AT RESET

During any reset event, the <u>PWM</u> module maintains ownership of the Class B fault <u>FLT32</u>. At reset, this fault is enabled in latched mode to guarantee the fail-safe power-up of the application. The application software must clear the PWM fault before enabling the High-Speed Motor <u>Control PWM</u> module. To clear the fault condition, the <u>FLT32</u> pin must first be pulled high externally or the internal pull up resistor in the CNPUx register can be enabled.

Note: The Fault mode may be changed using the FLTMOD<1:0> bits (FCLCON<1:0>) regardless of the state of FLT32.

16.1.2 WRITE-PROTECTED REGISTERS

On dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices, write protection is implemented for the IOCONx and FCLCONx registers. The write protection feature prevents any inadvertent writes to these registers. This protection feature can be controlled by the PWMLOCK Configuration bit (FOSCSEL<6>). The default state of the write protection feature is enabled (PWMLOCK = 1). The write protection feature can be disabled by configuring PWMLOCK = 0.

To gain write access to these locked registers, the user application must write two consecutive values of (0xABCD and 0x4321) to the PWMKEY register to perform the unlock operation. The write access to the IOCONx or FCLCONx registers must be the next SFR access following the unlock process. There can be no other SFR accesses during the unlock process and subsequent write access. To write to both the IOCONx and FCLCONx registers requires two unlock operations.

The correct unlocking sequence is described in Example 16-1.

EXAMPLE 16-1: PWM WRITE-PROTECTED REGISTER UNLOCK SEQUENCE

```
; FLT32 pin must be pulled high externally in order to clear and disable the fault
; Writing to FCLCON1 register requires unlock sequence
mov #0xabcd,w10
                     ; Load first unlock key to w10 register
mov #0x4321,w11
                     ; Load second unlock key to wll register
mov #0x0000,w0
                     ; Load desired value of FCLCON1 register in w0
mov w10, PWMKEY
                     ; Write first unlock key to PWMKEY register
mov w11, PWMKEY
                     ; Write second unlock key to PWMKEY register
                    ; Write desired value to FCLCON1 register
mov w0,FCLCON1
; Set PWM ownership and polarity using the IOCON1 register
; Writing to IOCON1 register requires unlock sequence
mov #0xabcd,w10
                   ; Load first unlock key to w10 register
mov #0x4321,w11
                    ; Load second unlock key to wll register
mov #0xF000,w0
                     ; Load desired value of IOCON1 register in w0
mov w10, PWMKEY
                     ; Write first unlock key to PWMKEY register
mov w11, PWMKEY
                     ; Write second unlock key to PWMKEY register
                    ; Write desired value to IOCON1 register
mov w0.IOCON1
```

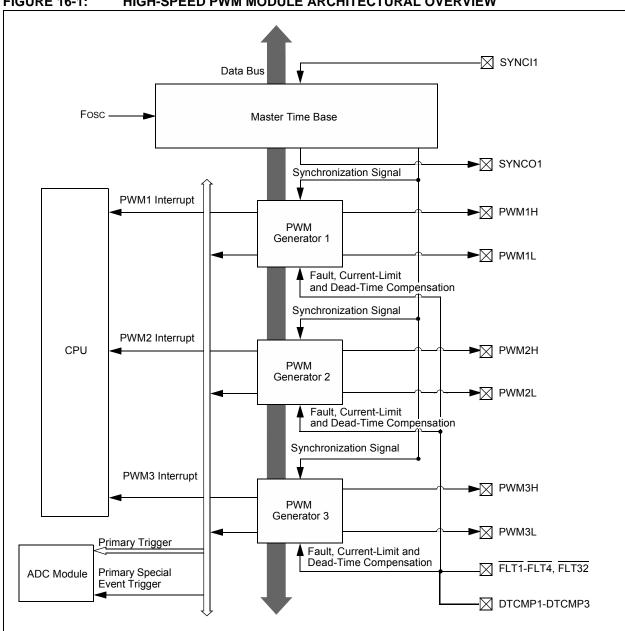
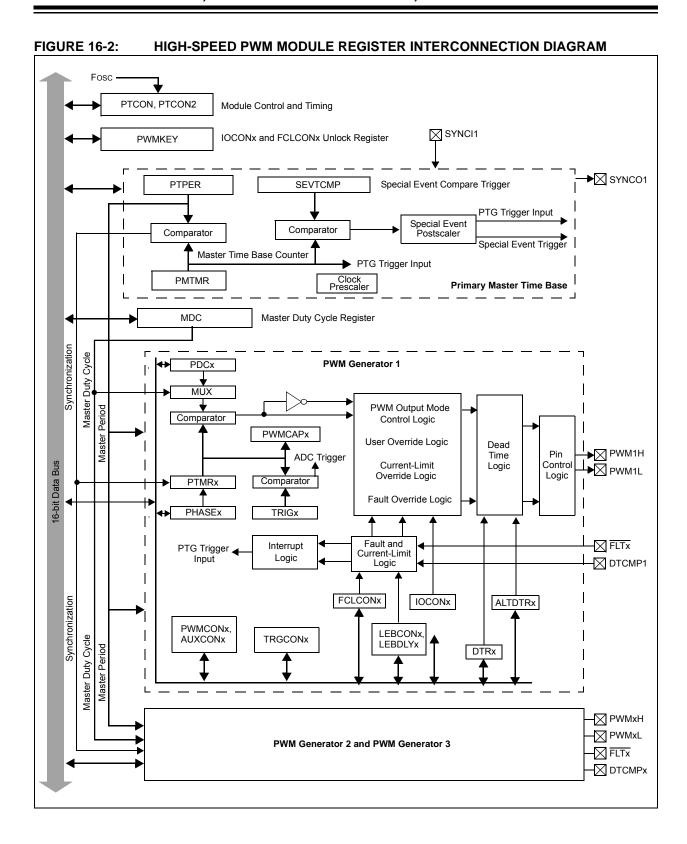


FIGURE 16-1: HIGH-SPEED PWM MODULE ARCHITECTURAL OVERVIEW

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16.2 **PWM Resources**

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:

In the event you are not able to access the product page using the link above, enter this URL in your browser:

http://www.microchip.com/wwwproducts/ Devices.aspx?dDocName=en555464

16.2.1 **KEY RESOURCES**

- Section 14. "High-Speed PWM" (DS70645)
- · Code Samples
- · Application Notes
- · Software Libraries
- Webinars
- · All related dsPIC33E/PIC24E Family Reference Manuals Sections
- · Development Tools

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16.3 PWM Control Registers

REGISTER 16-1: PTCON: PWM TIME BASE CONTROL REGISTER

R/W-0	U-0	R/W-0	HS/HC-0	R/W-0	R/W-0	R/W-0	R/W-0
PTEN	_	PTSIDL	SESTAT	SEIEN	EIPU ⁽¹⁾	SYNCPOL ⁽¹⁾	SYNCOEN ⁽¹⁾
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SYNCEN ⁽¹⁾	SYNCSRC<2:0> ⁽¹⁾			SEVTPS<3:0> ⁽¹⁾			
bit 7							bit 0

Legend:	HC = Cleared in Hardware	HS = Set in Hardware	
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15	PTEN: PWM Module Enable bit 1 = PWM module is enabled
hit 11	0 = PWM module is disabled
bit 14	Unimplemented: Read as '0'
bit 13	PTSIDL: PWM Time Base Stop in Idle Mode bit 1 = PWM time base halts in CPU Idle mode 0 = PWM time base runs in CPU Idle mode
bit 12	SESTAT: Special Event Interrupt Status bit 1 = Special Event Interrupt is pending 0 = Special Event Interrupt is not pending
bit 11	SEIEN: Special Event Interrupt Enable bit 1 = Special Event Interrupt is enabled 0 = Special Event Interrupt is disabled
bit 10	EIPU: Enable Immediate Period Updates bit ⁽¹⁾ 1 = Active Period register is updated immediately 0 = Active Period register updates occur on PWM cycle boundaries
bit 9	SYNCPOL: Synchronize Input and Output Polarity bit ⁽¹⁾ 1 = SYNCI1/SYNCO1 polarity is inverted (active-low) 0 = SYNCI1/SYNCO1 is active-high
bit 8	SYNCOEN: Primary Time Base Sync Enable bit ⁽¹⁾ 1 = SYNCO1 output is enabled 0 = SYNCO1 output is disabled
bit 7	SYNCEN: External Time Base Synchronization Enable bit ⁽¹⁾ 1 = External synchronization of primary time base is enabled 0 = External synchronization of primary time base is disabled
bit 6-4	SYNCSRC<2:0>: Synchronous Source Selection bits ⁽¹⁾ 111 = Reserved

- **Note 1:** These bits should be changed only when PTEN = 0. In addition, when using the SYNCI1 feature, the user application must program the period register with a value that is slightly larger than the expected period of the external synchronization input signal.
 - 2: See Section 24.0 "Peripheral Trigger Generator (PTG) Module" for information on this selection.

REGISTER 16-1: PTCON: PWM TIME BASE CONTROL REGISTER (CONTINUED)

- **Note 1:** These bits should be changed only when PTEN = 0. In addition, when using the SYNCI1 feature, the user application must program the period register with a value that is slightly larger than the expected period of the external synchronization input signal.
 - 2: See Section 24.0 "Peripheral Trigger Generator (PTG) Module" for information on this selection.

REGISTER 16-2: PTCON2: PWM PRIMARY MASTER CLOCK DIVIDER SELECT REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	_	_	_	_	_	_	_
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
_	_	_	_	_	P	CLKDIV<2:0> ⁽	1)
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-3 **Unimplemented:** Read as '0'

bit 2-0 PCLKDIV<2:0>: PWM Input Clock Prescaler (Divider) Select bits⁽¹⁾

111 = Reserved

110 = Divide by 64

101 = Divide by 32

100 = Divide by 16

011 **= Divide by 8**

010 = Divide by 4

001 = Divide by 2

000 = Divide by 1, maximum PWM timing resolution (power-on default)

Note 1: These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

REGISTER 16-3: PTPER: PRIMARY MASTER TIME BASE PERIOD REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1			
	PTPER<15:8>									
bit 15							bit 8			

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0		
PTPER<7:0>									
bit 7							bit 0		

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 PTPER<15:0>: Primary Master Time Base (PMTMR) Period Value bits

REGISTER 16-4: SEVTCMP: PWM PRIMARY SPECIAL EVENT COMPARE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
	SEVTCMP<15:8>									
bit 15							bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
	SEVTCMP<7:0>									
bit 7										

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **SEVTCMP<15:0>:** Special Event Compare Count Value bits

REGISTER 16-5: CHOP: PWM CHOP CLOCK GENERATOR REGISTER

R/W-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
CHPCLKEN	_	_	_	_	_	CHOP<9:8>	
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
CHOP<7:0>									
bit 7							bit 0		

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15 CHPCLKEN: Enable Chop Clock Generator bit

1 = Chop clock generator is enabled0 = Chop clock generator is disabled

bit 14-10 **Unimplemented:** Read as '0'

bit 9-0 CHOP<9:0>: Chop Clock Divider bits

The frequency of the chop clock signal is given by the following expression:

Chop Frequency = (FP/PCLKDIV<2:0)/(CHOP<9:0> + 1)

REGISTER 16-6: MDC: PWM MASTER DUTY CYCLE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
MDC<15:8>								
bit 15							bit 8	

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
MDC<7:0>										
bit 7							bit 0			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 MDC<15:0>: Master PWM Duty Cycle Value bits

REGISTER 16-7: PWMCONx: PWM CONTROL REGISTER

HS/HC-0	HS/HC-0	HS/HC-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FLTSTAT ⁽¹⁾	CLSTAT ⁽¹⁾	TRGSTAT	FLTIEN	CLIEN	TRGIEN	ITB ⁽²⁾	MDCS ⁽²⁾
bit 15							bit 8

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
DTC<	<1:0>	DTCP ⁽³⁾	_	MTBS	CAM ^(2,4)	XPRES ⁽⁵⁾	IUE ⁽²⁾
bit 7							bit 0

Legend:	HC = Cleared in Hardware	HS = Set in Hardware	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 FLTSTAT: Fault Interrupt Status bit⁽¹⁾

1 = Fault interrupt is pending

0 = No Fault interrupt is pending

This bit is cleared by setting FLTIEN = 0.

bit 14 CLSTAT: Current-Limit Interrupt Status bit⁽¹⁾

1 = Current-limit interrupt is pending

0 = No current-limit interrupt is pending

This bit is cleared by setting CLIEN = 0.

bit 13 TRGSTAT: Trigger Interrupt Status bit

1 = Trigger interrupt is pending

0 = No trigger interrupt is pending

This bit is cleared by setting TRGIEN = 0.

bit 12 **FLTIEN:** Fault Interrupt Enable bit

1 = Fault interrupt is enabled

0 = Fault interrupt is disabled and FLTSTAT bit is cleared

bit 11 CLIEN: Current-Limit Interrupt Enable bit

1 = Current-limit interrupt enabled

0 = Current-limit interrupt disabled and CLSTAT bit is cleared

bit 10 TRGIEN: Trigger Interrupt Enable bit

1 = A trigger event generates an interrupt request

0 = Trigger event interrupts are disabled and TRGSTAT bit is cleared

bit 9 **ITB:** Independent Time Base Mode bit⁽²⁾

1 = PHASEx register provides time base period for this PWM generator

0 = PTPER register provides timing for this PWM generator

bit 8 MDCS: Master Duty Cycle Register Select bit⁽²⁾

1 = MDC register provides duty cycle information for this PWM generator

0 = PDCx register provides duty cycle information for this PWM generator

Note 1: Software must clear the interrupt status here and in the corresponding IFS bit in the interrupt controller.

- 2: These bits should not be changed after the PWM is enabled (PTEN = 1).
- 3: DTC<1:0> = 11 for DTCP to be effective; otherwise, DTCP is ignored.
- **4:** The Independent Time Base (ITB = 1) mode must be enabled to use Center-Aligned mode. If ITB = 0, the CAM bit is ignored.
- 5: To operate in External Period Reset mode, the ITB bit must be '1' and the CLMOD bit in the FCLCONx register must be '0'.

REGISTER 16-7: PWMCONx: PWM CONTROL REGISTER (CONTINUED)

bit 7-6 DTC<1:0>: Dead-Time Control bits

11 = Dead-Time Compensation mode

10 = Dead-time function is disabled

01 = Negative dead time actively applied for Complementary Output mode

00 = Positive dead time actively applied for all output modes

bit 5 **DTCP:** Dead-Time Compensation Polarity bit⁽³⁾

When set to '1':

If DTCMPx = 0, PWMLx is shortened and PWMHx is lengthened. If DTCMPx = 1, PWMHx is shortened and PWMLx is lengthened.

When set to '0':

If DTCMPx = 0, PWMHx is shortened and PWMLx is lengthened. If DTCMPx = 1, PWMLx is shortened and PWMHx is lengthened.

bit 4 **Unimplemented:** Read as '0'

bit 3 MTBS: Master Time Base Select bit

- 1 = PWM generator uses the secondary master time base for synchronization and as the clock source for the PWM generation logic (if secondary time base is available)
- 0 = PWM generator uses the primary master time base for synchronization and as the clock source for the PWM generation logic
- bit 2 **CAM:** Center-Aligned Mode Enable bit^(2,4)
 - 1 = Center-Aligned mode is enabled
 - 0 = Edge-Aligned mode is enabled
- bit 1 XPRES: External PWM Reset Control bit (5)
 - 1 = Current-limit source resets the time base for this PWM generator if it is in Independent Time Base mode
 - 0 = External pins do not affect PWM time base
- bit 0 **IUE:** Immediate Update Enable bit
 - 1 = Updates to the active MDC/PDCx/DTx/ALTDTRx/PHASEx registers are immediate
 - 0 = Updates to the active MDC/PDCx/DTx/ALTDTRx/PHASEx registers are synchronized to the PWM time base
- Note 1: Software must clear the interrupt status here and in the corresponding IFS bit in the interrupt controller.
 - 2: These bits should not be changed after the PWM is enabled (PTEN = 1).
 - 3: DTC<1:0> = 11 for DTCP to be effective; otherwise, DTCP is ignored.
 - **4:** The Independent Time Base (ITB = 1) mode must be enabled to use Center-Aligned mode. If ITB = 0, the CAM bit is ignored.
 - 5: To operate in External Period Reset mode, the ITB bit must be '1' and the CLMOD bit in the FCLCONx register must be '0'.

REGISTER 16-8: PDCx: PWM GENERATOR DUTY CYCLE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
PDCx<15:8>									
bit 15							bit 8		

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
PDCx<7:0>									
bit 7							bit 0		

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 PDCx<15:0>: PWM Generator # Duty Cycle Value bits

REGISTER 16-9: PHASEx: PWM PRIMARY PHASE SHIFT REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
PHASEx<15:8>										
bit 15							bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
PHASEx<7:0>										
bit 7							bit 0			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 PHASEx<15:0>: PWM Phase Shift Value or Independent Time Base Period bits for the PWM Generator

Note 1: If ITB (PWMCONx<9>) = 0, the following applies based on the mode of operation:

Complementary, Redundant and Push-Pull Output mode (PMOD<1:0> (IOCON<11:10>) = 00, 01 or 10),

PHASEx<15:0> = Phase shift value for PWMxH and PWMxL outputs

2: If ITB (PWMCONx<9>) = 1, the following applies based on the mode of operation:
Complementary, Redundant and Push-Pull Output mode (PMOD<1:0> (IOCONx<11:10>) = 00, 01 or 10),
PHASEx<15:0> = Independent time base period value for PWMxH and PWMxL

REGISTER 16-10: DTRx: PWM DEAD-TIME REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	_			DTRx	<13:8>		
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
DTRx<7:0>									
bit 7							bit 0		

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-0 DTRx<13:0>: Unsigned 14-bit Dead-Time Value bits for PWMx Dead-Time Unit

REGISTER 16-11: ALTDTRx: PWM ALTERNATE DEAD-TIME REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	_			ALTDTI	Rx<13:8>		
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			ALTDT	Rx<7:0>			
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-0 ALTDTRx<13:0>: Unsigned 14-bit Dead-Time Value bits for PWMx Dead-Time Unit

REGISTER 16-12: TRGCONX: PWM TRIGGER CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
	TRGDI\	/<3:0>		_	_	_	_
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	_			TRGST	RT<5:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	t, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **TRGDIV<3:0>:** Trigger # Output Divider bits

1111 = Trigger output for every 16th trigger event

1110 = Trigger output for every 15th trigger event

1101 = Trigger output for every 14th trigger event

1100 = Trigger output for every 13th trigger event

1011 = Trigger output for every 12th trigger event

1010 = Trigger output for every 11th trigger event

1001 = Trigger output for every 10th trigger event

1000 = Trigger output for every 9th trigger event

0111 = Trigger output for every 8th trigger event

0110 = Trigger output for every 7th trigger event 0101 = Trigger output for every 6th trigger event

0100 = Trigger output for every 5th trigger event

0100 - Trigger output for every 4th trigger event

0011 = Trigger output for every 4th trigger event

0010 = Trigger output for every 3rd trigger event

0001 = Trigger output for every 2nd trigger event

0000 = Trigger output for every trigger event

bit 11-6 **Unimplemented:** Read as '0'

bit 5-0 TRGSTRT<5:0>: Trigger Postscaler Start Enable Select bits

111111 = Wait 63 PWM cycles before generating the first trigger event after the module is enabled

•

•

•

000010 = Wait 2 PWM cycles before generating the first trigger event after the module is enabled 000001 = Wait 1 PWM cycles before generating the first trigger event after the module is enabled 000000 = Wait 0 PWM cycles before generating the first trigger event after the module is enabled

Note 1: The secondary PWM generator cannot generate PWM trigger interrupts.

REGISTER 16-13: IOCONX: PWM I/O CONTROL REGISTER (2)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PENH	PENL	POLH	POLL	PMOD	<1:0> ⁽¹⁾	OVRENH	OVRENL
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OVRDA	T<1:0>	FLTDA	T<1:0>	CLDA	T<1:0>	SWAP	OSYNC
bit 7							bit 0

Leaend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15 PENH: PWMxH Output Pin Ownership bit

1 = PWM module controls PWMxH pin

0 = GPIO module controls PWMxH pin

bit 14 PENL: PWMxL Output Pin Ownership bit

1 = PWM module controls PWMxL pin

0 = GPIO module controls PWMxL pin

bit 13 POLH: PWMxH Output Pin Polarity bit

1 = PWMxH pin is active-low

0 = PWMxH pin is active-high

bit 12 POLL: PWMxL Output Pin Polarity bit

1 = PWMxL pin is active-low

0 = PWMxL pin is active-high

PMOD<1:0>: PWM # I/O Pin Mode bits(1) bit 11-10

11 = Reserved; do not use

10 = PWM I/O pin pair is in the Push-Pull Output mode

01 = PWM I/O pin pair is in the Redundant Output mode

00 = PWM I/O pin pair is in the Complementary Output mode

bit 9 **OVRENH:** Override Enable for PWMxH Pin bit

1 = OVRDAT<1> controls output on PWMxH pin

0 = PWM generator controls PWMxH pin

bit 8 **OVRENL:** Override Enable for PWMxL Pin bit

1 = OVRDAT<0> controls output on PWMxL pin

0 = PWM generator controls PWMxL pin

OVRDAT<1:0>: Data for PWMxH, PWMxL Pins if Override is Enabled bits bit 7-6

> If OVERENH = 1, PWMxH is driven to the state specified by OVRDAT<1>. If OVERENL = 1, PWMxL is driven to the state specified by OVRDAT<0>.

FLTDAT<1:0>: Data for PWMxH and PWMxL Pins if FLTMOD is Enabled bits

If Fault is active, PWMxH is driven to the state specified by FLTDAT<1>.

If Fault is active, PWMxL is driven to the state specified by FLTDAT<0>.

bit 3-2 CLDAT<1:0>: Data for PWMxH and PWMxL Pins if CLMOD is Enabled bits

> If current-limit is active, PWMxH is driven to the state specified by CLDAT<1>. If current-limit is active, PWMxL is driven to the state specified by CLDAT<0>.

Note 1: These bits should not be changed after the PWM module is enabled (PTEN = 1).

If the PWMLOCK Configuration bit (FOSCSEL<6>) is a '1', the IOCONx register can only be written after the unlock sequence has been executed.

bit 5-4

REGISTER 16-13: IOCONx: PWM I/O CONTROL REGISTER⁽²⁾ (CONTINUED)

bit 1 **SWAP:** SWAP PWMxH and PWMxL Pins bit

- 1 = PWMxH output signal is connected to PWMxL pins; PWMxL output signal is connected to PWMxH pins
- 0 = PWMxH and PWMxL pins are mapped to their respective pins
- bit 0 OSYNC: Output Override Synchronization bit
 - 1 = Output overrides via the OVRDAT<1:0> bits are synchronized to the PWM time base 0 = Output overrides via the OVDDAT<1:0> bits occur on the next CPU clock boundary
- **Note 1:** These bits should not be changed after the PWM module is enabled (PTEN = 1).
 - 2: If the PWMLOCK Configuration bit (FOSCSEL<6>) is a '1', the IOCONx register can only be written after the unlock sequence has been executed.

REGISTER 16-14: TRIGX: PWM PRIMARY TRIGGER COMPARE VALUE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TRGCMP<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			TRGCM	1P<7:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	t, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 TRGCMP<15:0>: Trigger Control Value bits

When the primary PWM functions in local time base, this register contains the compare values that can trigger the ADC module.

REGISTER 16-15: FCLCONx: PWM FAULT CURRENT-LIMIT CONTROL REGISTER⁽¹⁾

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_			CLSRC<4:0>	•		CLPOL ⁽²⁾	CLMOD
bit 15				bit 8			

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0
	F	LTSRC<4:0>			FLTPOL ⁽²⁾	FLTMO	D<1:0>
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	r, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 Unimplemented: Read as '0'

bit 14-10 **CLSRC<4:0>:** Current-Limit Control Signal Source Select bits for PWM Generator # These bits also specify the source for the dead-time compensation input signal, DTCMPx.

11111 = Fault 32 11110 = Reserved

•

01100 = Reserved

01011 = Comparator 4

01010 = Op amp/Comparator 3

01001 = Op amp/Comparator 2

01000 = Op amp/Comparator 1

00111 = Reserved

00110 = Reserved

00101 = Reserved

00100 = Reserved

00011 = Fault 4

00010 **= Fault 3**

00001 = Fault 2

00000 = Fault 1 (default)

bit 9 **CLPOL:** Current-Limit Polarity bit for PWM Generator #⁽²⁾

1 = The selected current-limit source is active-low

0 = The selected current-limit source is active-high

bit 8 CLMOD: Current-Limit Mode Enable bit for PWM Generator #

1 = Current-Limit mode is enabled

0 = Current-Limit mode is disabled

Note 1: If the PWMLOCK Configuration bit (FOSCSEL<6>) is a '1', the IOCONx register can only be written after the unlock sequence has been executed.

2: These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

REGISTER 16-15: FCLCONx: PWM FAULT CURRENT-LIMIT CONTROL REGISTER⁽¹⁾ (CONTINUED)

```
FLTSRC<4:0>: Fault Control Signal Source Select bits for PWM Generator #
bit 7-3
               11111 = Fault 32 (default)
               11110 = Reserved
               01100 = Reserved
               01011 = Comparator 4
               01010 = Op amp/Comparator 3
               01001 = Op amp/Comparator 2
               01000 = Op amp/Comparator 1
               00111 = Reserved
               00110 = Reserved
               00101 = Reserved
               00100 = Reserved
               00011 = Fault 4
               00010 = Fault 3
               00001 = Fault 2
               00000 = Fault 1
bit 2
               FLTPOL: Fault Polarity bit for PWM Generator #<sup>(2)</sup>
               1 = The selected Fault source is active-low
               0 = The selected Fault source is active-high
bit 1-0
               FLTMOD<1:0>: Fault Mode bits for PWM Generator #
               11 = Fault input is disabled
               10 = Reserved
               01 = The selected Fault source forces PWMxH, PWMxL pins to FLTDAT values (cycle)
               00 = The selected Fault source forces PWMxH, PWMxL pins to FLTDAT values (latched condition)
```

- Note 1: If the PWMLOCK Configuration bit (FOSCSEL<6>) is a '1', the IOCONx register can only be written after the unlock sequence has been executed.
 - 2: These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

REGISTER 16-16: LEBCONx: LEADING-EDGE BLANKING CONTROL REGISTER

Legend:

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	_	_
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	_	ВСН	BCL	BPHH	BPHL	BPLH	BPLL
bit 7							bit 0

R = Readable	bit W = Writab	le bit U =	Unimplemented bit, read	l as '0'
-n = Value at F	POR '1' = Bit is s	set '0'	= Bit is cleared	x = Bit is unknown
bit 15	PHR: PWMxH Rising Edg 1 = Rising edge of PWMx 0 = Leading-Edge Blankir	H will trigger Leading g ignores rising edg		
bit 14	PHF: PWMxH Falling Edg 1 = Falling edge of PWMx 0 = Leading-Edge Blankir	H will trigger Leadin		
bit 13	PLR: PWMxL Rising Edgu 1 = Rising edge of PWMx 0 = Leading-Edge Blankir	L will trigger Leading		
bit 12	PLF: PWMxL Falling Edg 1 = Falling edge of PWMx 0 = Leading-Edge Blankir	L will trigger Leading		
bit 11	FLTLEBEN: Fault Input L 1 = Leading-Edge Blankir 0 = Leading-Edge Blankir	g is applied to selec	ted Fault input	
bit 10	CLLEBEN: Current-Limit 1 = Leading-Edge Blankir 0 = Leading-Edge Blankir	g is applied to selec	ted current-limit input	
bit 9-6	Unimplemented: Read a	s '0'		
bit 5	BCH: Blanking in Selecter 1 = State blanking (of curr 0 = No blanking when selecters)	ent-limit and/or Faul	t input signals) when sele	cted blanking signal is high
bit 4	BCL: Blanking in Selected 1 = State blanking (of curron 0 = No blanking when selected	ent-limit and/or Faul	t input signals) when sele	cted blanking signal is low
bit 3	BPHH: Blanking in PWMx 1 = State blanking (of curr 0 = No blanking when PW	ent-limit and/or Faul	t input signals) when PWN	MxH output is high
bit 2	BPHL: Blanking in PWMx 1 = State blanking (of curr 0 = No blanking when PW	ent-limit and/or Faul	t input signals) when PWN	MxH output is low
bit 1	BPLH: Blanking in PWMx 1 = State blanking (of curr 0 = No blanking when PW	L High Enable bit ent-limit and/or Faul	t input signals) when PWN	/lxL output is high
bit 0	BPLL: Blanking in PWMx 1 = State blanking (of curr 0 = No blanking when PW	ent-limit and/or Faul	t input signals) when PWN	∕lxL output is low

Note 1: The blanking signal is selected via the BLANKSEL bits in the AUXCONx register.

REGISTER 16-17: LEBDLYx: LEADING-EDGE BLANKING DELAY REGISTER

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
_	_	_	_		LEB<	11:8>	
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
LEB<7:0>									
bit 7									

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-12 **Unimplemented:** Read as '0'

bit 11-0 LEB<11:0>: Leading-Edge Blanking Delay bits for Current-Limit and Fault Inputs

REGISTER 16-18: AUXCONX: PWM AUXILIARY CONTROL REGISTER

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
_	_	_	_		BLANKS	EL<3:0>	
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	_	CHOPSEL<3:0>				CHOPHEN	CHOPLEN
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-12 **Unimplemented:** Read as '0'

bit 11-8 BLANKSEL<3:0>: PWM State Blank Source Select bits

The selected state blank signal will block the current-limit and/or Fault input signals (if enabled via the BCH and BCL bits in the LEBCONx register).

1001 = Reserved

•

•

0100 = Reserved

0011 = PWM3H selected as state blank source

0010 = PWM2H selected as state blank source

0001 = PWM1H selected as state blank source

0000 = No state blanking

bit 7-6 **Unimplemented:** Read as '0'

bit 5-2 CHOPSEL<3:0>: PWM Chop Clock Source Select bits

The selected signal will enable and disable (CHOP) the selected PWM outputs.

1001 = Reserved

•

0100 = Reserved

0011 = PWM3H selected as CHOP clock source

0010 = PWM2H selected as CHOP clock source

0001 = PWM1H selected as CHOP clock source

0000 = Chop clock generator selected as CHOP clock source

bit 1 CHOPHEN: PWMxH Output Chopping Enable bit

1 = PWMxH chopping function is enabled

0 = PWMxH chopping function is disabled

bit 0 CHOPLEN: PWMxL Output Chopping Enable bit

1 = PWMxL chopping function is enabled

0 = PWMxL chopping function is disabled

17.0 QUADRATURE ENCODER INTERFACE (QEI) MODULE (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

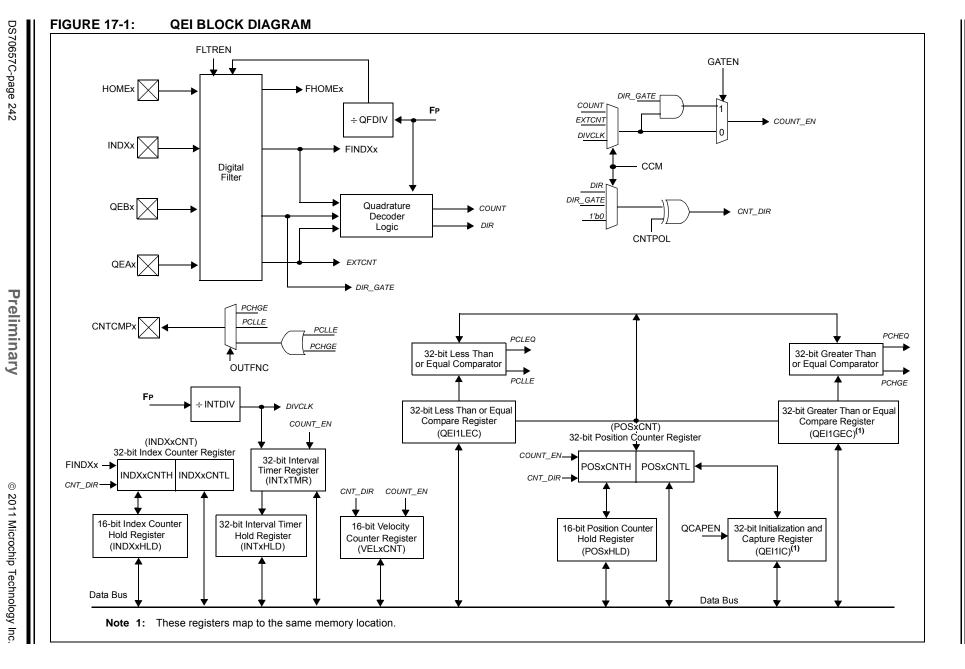
- Note 1: This data sheet summarizes the features dsPIC33EPXXXGP50X. the dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 15. "Quadrature Encoder Interface (QEI)" (DS70601) of "dsPIC33E/PIC24E Family Reference Manual', which is available from the Microchip (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

This chapter describes the Quadrature Encoder Interface (QEI) module and associated operational modes. The QEI module provides the interface to incremental encoders for obtaining mechanical position data.

The operational features of the QEI module include:

- · 32-bit position counter
- · 32-bit Index pulse counter
- · 32-bit Interval timer
- · 16-bit velocity counter
- 32-bit Position Initialization/Capture/Compare High register
- · 32-bit Position Compare Low register
- · x4 Quadrature Count mode
- · External Up/Down Count mode
- · External Gated Count mode
- · External Gated Timer mode
- · Internal Timer mode

Figure 17-1 illustrates the QEI block diagram.



17.1 QEI Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter

this URL in your browser:

http://www.microchip.com/wwwproducts/ Devices.aspx?dDocName=en555464

17.1.1 KEY RESOURCES

- Section 15. "Quadrature Encoder Interface" (DS70601)
- · Code Samples
- · Application Notes
- · Software Libraries
- Webinars
- All related dsPIC33E/PIC24E Family Reference Manuals Sections
- · Development Tools

17.2 QEI Control Registers

REGISTER 17-1: QEI1CON: QEI CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEIEN	_	QEISIDL		PIMOD<2:0>	IMV<	1:0> ⁽²⁾	
bit 15	•						bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	INTDIV<2:0>(3)			CNTPOL	GATEN	CCM<1:0>	
bit 7							bit 0

Legend:				
R = Readable bit	lable bit W = Writable bit U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 15 QEIEN: Quadrature Encoder Interface Module Counter Enable bit

1 = Module counters are enabled

0 = Module counters are disabled, but SFRs can be read or written to

bit 14 **Unimplemented:** Read as '0' bit 13 **QEISIDL:** Stop in Idle Mode bit

1 = Discontinue module operation when device enters Idle mode

0 = Continue module operation in Idle mode

bit 12-10 PIMOD<2:0>: Position Counter Initialization Mode Select bits⁽¹⁾

111 = Reserved

110 = Modulo count mode for position counter

101 = Resets the position counter when the position counter equals QEI1GEC register

100 = Second index event after home event initializes position counter with contents of QEI1IC register

011 = First index event after home event initializes position counter with contents of QEI1IC register

010 = Next index input event initializes the position counter with contents of QEI1IC register

001 = Every Index input event resets the position counter

000 = Index input event does not affect position counter

bit 9-8 IMV<1:0>: Index Match Value bits(2)

11 = Index match occurs when QEB = 1 and QEA = 1

10 = Index match occurs when QEB = 1 and QEA = 0

01 = Index match occurs when QEB = 0 and QEA = 1

00 = Index input event does not affect position counter

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **INTDIV<2:0>:** Timer Input Clock Prescale Select bits (interval timer, main timer (position counter), velocity counter and index counter internal clock divider select)⁽³⁾

111 = 1:256 prescale value

110 = 1:64 prescale value

101 = 1:32 prescale value

100 = 1:16 prescale value

011 = 1:8 prescale value

010 = 1:4 prescale value

001 = 1:2 prescale value

000 = 1:1 prescale value

Note 1: When CCM = 10 or CCM = 11, all of the QEI counters operate as timers and the PIMOD<2:0> bits are ignored.

- 2: When CCM = 00 and QEA and QEB values match Index Match Value (IMV), the POSCNTH and POSCNTL registers are reset.
- 3: The selected clock rate should be at least twice the expected maximum quadrature count rate.

REGISTER 17-1: QEI1CON: QEI CONTROL REGISTER (CONTINUED)

bit 3 CNTPOL: Position and Index Counter/Timer Direction Select bit

1 = Counter direction is negative unless modified by external Up/Down signal 0 = Counter direction is positive unless modified by external Up/Down signal

bit 2 GATEN: External Count Gate Enable bit

1 = External gate signal controls position counter operation

0 = External gate signal does not affect position counter/timer operation

bit 1-0 **CCM<1:0>:** Counter Control Mode Selection bits

11 = Internal timer mode with optional external count is selected10 = External clock count with optional external count is selected

01 = External clock count with external up/down direction is selected

00 = Quadrature Encoder Interface (x4 mode) count mode is selected

- Note 1: When CCM = 10 or CCM = 11, all of the QEI counters operate as timers and the PIMOD<2:0> bits are ignored.
 - 2: When CCM = 00 and QEA and QEB values match Index Match Value (IMV), the POSCNTH and POSCNTL registers are reset.
 - 3: The selected clock rate should be at least twice the expected maximum quadrature count rate.

REGISTER 17-2: QEI1IOC: QEI I/O CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QCAPEN	FLTREN	QFDIV<2:0>			OUTFNC<1:0>		SWPAB
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R-x	R-x	R-x	R-x
HOMPOL	IDXPOL	QEBPOL	QEAPOL	HOME	INDEX	QEB	QEA
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15 QCAPEN: Position Counter Input Capture Enable bit

1 = Positive edge detect of Home input triggers position capture function
 0 = HOMEx input event (positive edge) does not trigger a capture event

bit 14 FLTREN: QEAx/QEBx/INDXx/HOMEx Digital Filter Enable bit

1 = Input Pin Digital filter is enabled

0 = Input Pin Digital filter is disabled (bypassed)

bit 13-11 QFDIV<2:0>: QEAx/QEBx/INDXx/HOMEx Digital Input Filter Clock Divide Select bits

111 = 1:256 clock divide 110 = 1:64 clock divide 101 = 1:32 clock divide 100 = 1:16 clock divide 011 = 1:8 clock divide 010 = 1:4 clock divide

001 = 1:2 clock divide 000 = 1:1 clock divide

bit 10-9 OUTFNC<1:0>: QEI Module Output Function Mode Select bits

11 = The CTNCMPx pin goes high when QEI1LEC ≥ POSxCNT ≥ QEI1GEC

10 = The CTNCMPx pin goes high when POSxCNT \leq QEI1LEC 01 = The CTNCMPx pin goes high when POSxCNT \geq QEI1GEC

00 = Output is disabled

bit 8 SWPAB: Swap QEA and QEB Inputs bit

1 = QEAx and QEBx are swapped prior to quadrature decoder logic

0 = QEAx and QEBx are not swapped

bit 7 **HOMPOL:** HOMEx Input Polarity Select bit

1 = Input is inverted0 = Input is not inverted

bit 6 IDXPOL: HOMEx Input Polarity Select bit

1 = Input is inverted0 = Input is not inverted

bit 5 **QEBPOL:** QEBx Input Polarity Select bit

1 = Input is inverted0 = Input is not inverted

bit 4 QEAPOL: QEAx Input Polarity Select bit

1 = Input is inverted0 = Input is not inverted

bit 3 **HOME:** Status of HOMEx Input Pin After Polarity Control

1 = Pin is at logic '1' 0 = Pin is at logic '0'

REGISTER 17-2: QEI1IOC: QEI I/O CONTROL REGISTER (CONTINUED)

bit 2 INDEX: Status of INDXx Input Pin After Polarity Control

1 = Pin is at logic '1' 0 = Pin is at logic '0'

bit 1 QEB: Status of QEBx Input Pin After Polarity Control And SWPAB Pin Swapping

1 = Pin is at logic '1' 0 = Pin is at logic '0'

bit 0 QEA: Status of QEAx Input Pin After Polarity Control And SWPAB Pin Swapping

1 = Pin is at logic '1' 0 = Pin is at logic '0'

REGISTER 17-3: QEI1STAT: QEI STATUS REGISTER

U-0	U-0	HS, RC-0	R/W-0	HS, RC-0	R/W-0	HS, RC-0	R/W-0
_	_	PCHEQIRQ	PCHEQIEN	PCLEQIRQ	PCLEQIEN	POSOVIRQ	POSOVIEN
bit 15							bit 8

HS, RC-0	R/W-0	HS, RC-0	R/W-0	HS, RC-0	R/W-0	HS, RC-0	R/W-0
PCIIRQ ⁽¹⁾	PCIIEN	VELOVIRQ	VELOVIEN	HOMIRQ	HOMIEN	IDXIRQ	IDXIEN
bit 7							bit 0

Legend:	HS = Set by Hardware	C = Cleared by Software		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

E# 45 44	Harimalamantada Dandara (c)
bit 15-14	Unimplemented: Read as '0'
bit 13	PCHEQIRQ: Position Counter Greater Than or Equal Compare Status bit 1 = POSxCNT ≥ QEI1GEC
	0 = POSXCNT < QEITGEC
bit 12	PCHEQIEN: Position Counter Greater Than or Equal Compare Interrupt Enable bit
DIC 12	1 = Interrupt is enabled
	0 = Interrupt is disabled
bit 11	PCLEQIRQ: Position Counter Less Than or Equal Compare Status bit
	1 = POSxCNT ≤ QEI1LEC
	0 = POSxCNT > QEI1LEC
bit 10	PCLEQIEN: Position Counter Less Than or Equal Compare Interrupt Enable bit
	1 = Interrupt is enabled 0 = Interrupt is disabled
bit 9	POSOVIRQ: Position Counter Overflow Status bit
Dit 3	1 = Overflow has occurred
	0 = No overflow has occurred
bit 8	POSOVIEN: Position Counter Overflow Interrupt Enable bit
	1 = Interrupt is enabled
	0 = Interrupt is disabled
bit 7	PCIIRQ: Position Counter (Homing) Initialization Process Complete Status bit ⁽¹⁾
	1 = POSxCNT was reinitialized 0 = POSxCNT was not reinitialized
bit 6	PCIIEN: Position Counter (Homing) Initialization Process Complete interrupt Enable bit
DIL O	1 = Interrupt is enabled
	0 = Interrupt is disabled
bit 5	VELOVIRQ: Velocity Counter Overflow Status bit
	1 = Overflow has occurred
	0 = No overflow has not occurred
bit 4	VELOVIEN: Velocity Counter Overflow Interrupt Enable bit
	1 = Interrupt is enabled 0 = Interrupt is disabled
bit 3	HOMIRQ: Status Flag for Home Event Status bit
5.0	1 = Home event has occurred
	0 = No Home event has occurred
bit 2	HOMIEN: Home Input Event Interrupt Enable bit
	1 = Interrupt is enabled
	0 = Interrupt is disabled

Note 1: This status bit is only applicable to PIMOD<2:0> modes '011' and '100'.

REGISTER 17-3: QEI1STAT: QEI STATUS REGISTER (CONTINUED)

bit 1 IDXIRQ: Status Flag for Index Event Status bit

1 = Index event has occurred 0 = No Index event has occurred

bit 0 IDXIEN: Index Input Event Interrupt Enable bit

1 = Interrupt is enabled0 = Interrupt is disabled

Note 1: This status bit is only applicable to PIMOD<2:0> modes '011' and '100'.

REGISTER 17-4: POSxCNTH: POSITION COUNTER HIGH WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
	POSCNT<31:24>								
bit 15							bit 8		

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
	POSCNT<23:16>								
bit 7							bit 0		

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 POSCNT<31:16>: High word used to form 32-bit Position Counter Register (POSxCNT) bits

REGISTER 17-5: POSxCNTL: POSITION COUNTER LOW WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
POSCNT<15:8>								
bit 15							bit 8	

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
	POSCNT<7:0>								
bit 7							bit 0		

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **POSCNT<15:0>:** Low word used to form 32-bit Position Counter Register (POSxCNT) bits

REGISTER 17-6: POSxHLD: POSITION COUNTER HOLD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
	POSHLD<15:8>								
bit 15 bit									

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
	POSHLD<7:0>								
bit 7							bit 0		

Legend:

 $R = Readable \ bit \ W = Writable \ bit \ U = Unimplemented \ bit, read as '0'$

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **POSHLD<15:0>:** Hold register bits for reading and writing POSxCNTH

REGISTER 17-7: VELXCNT: VELOCITY COUNTER REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
	VELCNT<15:8>								
bit 15							bit 8		

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
VELCNT<7:0>							
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **VELCNT<15:0>:** Velocity Counter bits

REGISTER 17-8: INDXxCNTH: INDEX COUNTER HIGH WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			INDXCN	T<31:24>			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			INDXCN ⁻	T<23:16>			
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 INDXCNT<31:16>: High word used to form 32-bit Index Counter Register (INDXxCNT) bits

REGISTER 17-9: INDXxCNTL: INDEX COUNTER LOW WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			INDXCN	IT<15:8>			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			INDXCI	NT<7:0>			
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 INDXCNT<15:0>: Low word used to form 32-bit Index Counter Register (INDXxCNT) bits

REGISTER 17-10: INDXxHLD: INDEX COUNTER HOLD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			INDXHL	D<15:8>			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			INDXHL	_D<7:0>			
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **INDXHLD<15:0>:** Hold register for reading and writing INDXxCNTH bits

REGISTER 17-11: QEI1ICH: INITIALIZATION/CAPTURE HIGH WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			QEIIC<	31:24>			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			QEIIC<	:23:16>			
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 QEIIC<31:16>: High word used to form 32-bit Initialization/Capture Register (QEI1IC) bits

REGISTER 17-12: QEI1ICL: INITIALIZATION/CAPTURE LOW WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			QEIIC-	<15:8>			
bit 15							bit 8

| R/W-0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| | | | QEIIC | <7:0> | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

 $R = Readable \ bit \ W = Writable \ bit \ U = Unimplemented \ bit, read as '0'$

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 QEIIC<15:0>: Low word used to form 32-bit Initialization/Capture Register (QEI1IC) bits

REGISTER 17-13: QEI1LECH: LESS THAN OR EQUAL COMPARE HIGH WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			QEILEC	<31:24>			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			QEILEC	<23:16>			
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 QEILEC<31:16>: High word used to form 32-bit Less Than or Equal Compare Register (QEI1LEC) bits

REGISTER 17-14: QEI1LECL: LESS THAN OR EQUAL COMPARE LOW WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			QEILE	C<15:8>			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			QEILE	C<7:0>			
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 QEILEC<15:0>: Low word used to form 32-bit Less Than or Equal Compare Register (QEI1LEC) bits

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REGISTER 17-15: QEI1GECH: GREATER THAN OR EQUAL COMPARE HIGH WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEIGEC<31:24>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			QEIGEC	<23:16>			
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **QEIGEC<31:16>:** High word used to form 32-bit Greater Than or Equal Compare Register (QEI1GEC) bits

REGISTER 17-16: QEI1GECL: GREATER THAN OR EQUAL COMPARE LOW WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			QEIGE	C<15:8>			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			QEIGE	C<7:0>			
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **QEIGEC<15:0>:** Low word used to form 32-bit Greater Than or Equal Compare Register (QEI1GEC) bits

REGISTER 17-17: INTXTMRH: INTERVAL TIMER HIGH WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
INTTMR<31:24>								
bit 15							bit 8	

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
	INTTMR<23:16>								
bit 7							bit 0		

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 INTTMR<31:16>: High word used to form 32-bit Interval Timer Register (INTxTMR) bits

REGISTER 17-18: INTXTMRL: INTERVAL TIMER LOW WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
INTTMR<15:8>								
bit 15							bit 8	

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
INTTMR<7:0>								
bit 7							bit 0	

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 INTTMR<15:0>: Low word used to form 32-bit Interval Timer Register (INTxTMR) bits

REGISTER 17-19: INTxHLDH: INTERVAL TIMER HOLD HIGH WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
INTHLD<31:24>									
bit 15							bit 8		

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
INTHLD<23:16>										
bit 7										

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **INTHLD<31:16>:** Hold register for reading and writing INTxTMRH bits

REGISTER 17-20: INTxHLDL: INTERVAL TIMER HOLD LOW WORD REGISTER

Ī	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
	INTHLD<15:8>										
bit 15											

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
	INTHLD<7:0>										
bit 7											

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **INTHLD<15:0>:** Hold register for reading and writing INTxTMRL bits

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18.0 SERIAL PERIPHERAL INTERFACE (SPI)

Note 1: This data sheet summarizes the features the dsPIC33EPXXXGP50X. dsPIC33EPXXXMC20X/50X. PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 18. "Serial Peripheral Interface (SPI)" (DS70569) "dsPIC33E/PIC24E Family Reference Manual', which is available Microchip from the web (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The SPI module is a synchronous serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices can be serial EEPROMs, shift registers, display drivers, A/D converters, etc. The SPI module is compatible with Motorola's SPI and SIOP interfaces.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X device family offers two SPI modules on a single device. These modules, which are designated as SPI1 and SPI2, are functionally identical. Each SPI module includes an eight-word FIFO buffer and allows DMA bus connections. When using the SPI module with DMA, FIFO operation can be disabled.

Note: In this section, the SPI modules are referred to together as SPIx, or separately as SPI1 and SPI2. Special Function Registers follow a similar notation. For example, SPIxCON refers to the control register for the SPI1 and SPI2 module.

The SPI1 module uses dedicated pins which allow for a higher speed when using SPI1. The SPI2 module takes advantage of the Peripheral Pin Select (PPS) feature to allow for greater flexibility in pin configuration of the SPI2 module, but results in a lower maximum speed for SPI2. See Section 30.0 "Electrical Characteristics" for more information.

The SPIx serial interface consists of four pins, as follows:

- SDIx: Serial Data Input
- SDOx: Serial Data Output
- · SCKx: Shift Clock Input or Output
- SSx/FSYNCx: Active-Low Slave Select or Frame Synchronization I/O Pulse

The SPIx module can be configured to operate with two, three or four pins. In 3-pin mode, SSx is not used. In 2-pin mode, neither SDOx nor SSx is used.

Figure 18-1 illustrates the block diagram of the SPI module in Standard and Enhanced modes.

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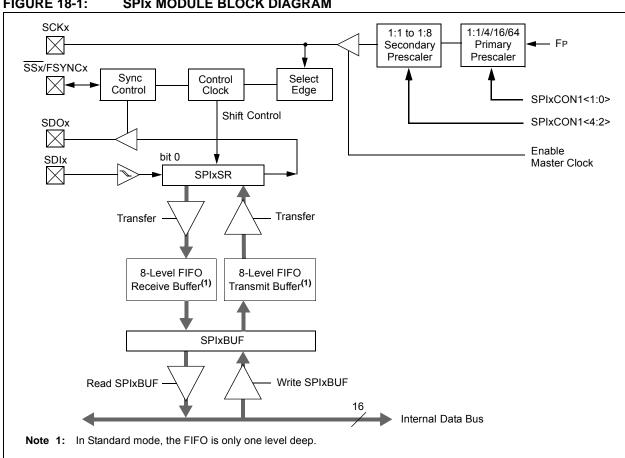


FIGURE 18-1: SPIX MODULE BLOCK DIAGRAM

18.1 SPI Helpful Tips

- In Frame mode, if there is a possibility that the master may not be initialized before the slave:
 - a) If FRMPOL (SPIxCON2<13>) = 1, use a pull-down resistor on SSx.
 - b) If FRMPOL = 0, use a pull-up resistor on \overline{SSx} .

Note: This insures that the first frame transmission after initialization is not shifted or corrupted.

- 2. In non-framed 3-wire mode, (i.e., not using SSx from a master):
 - a) If CKP (SPIxCON1<6>) = 1, always place a pull-up resistor on SSx.
 - b) If CKP = 0, always place a pull-down resistor on \overline{SSx} .

Note: This will insure that during power-up and initialization the master/slave will not lose sync due to an errant SCK transition that would cause the slave to accumulate data shift errors for both transmit and receive appearing as corrupted data.

3. FRMEN (SPIxCON2<15>) = 1 and SSEN (SPIxCON1<7>) = 1 are exclusive and invalid. In Frame mode, SCKx is continuous and the Frame sync pulse is active on the SSx pin, which indicates the start of a data frame.

Note: Not all third-party devices support Frame mode timing. Refer to the SPI electrical characteristics for details.

4. In Master mode only, set the SMP bit (SPIxCON1<9>) to a '1' for the fastest SPI data rate possible. The SMP bit can only be set at the same time or after the MSTEN bit (SPIxCON1<5>) is set.

To avoid invalid slave read data to the master, the user's master software must guarantee enough time for slave software to fill its write buffer before the user application initiates a master write/read cycle. It is always advisable to preload the SPIxBUF transmit register in advance of the next master transaction cycle. SPIxBUF is transferred to the SPI shift register and is empty once the data transmission begins.

18.2 SPI Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464

18.2.1 KEY RESOURCES

- Section 18. "Serial Peripheral Interface" (DS70569)
- · Code Samples
- · Application Notes
- · Software Libraries
- Webinars
- All related dsPIC33E/PIC24E Family Reference Manuals Sections
- · Development Tools

18.3 SPI Control Registers

REGISTER 18-1: SPIXSTAT: SPIX STATUS AND CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
SPIEN	_	SPISIDL	_	_		SPIBEC<2:0>	>
bit 15							bit 8

R/W-0	R/C-0, HS	R/W-0	R/W-0	R/W-0	R/W-0	R-0, HS, HC	R-0, HS, HC
SRMPT	SPIROV	SRXMPT		SISEL<2:0>		SPITBF	SPIRBF
bit 7							bit 0

Legend: C = Clearable bit

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

HS = Set in Hardware bit HC = Cleared in Hardware bit U = Unimplemented bit, read as '0'

bit 15 SPIEN: SPIx Enable bit

1 = Enables the module and configures SCKx, SDOx, SDIx and \overline{SSx} as serial port pins

0 = Disables the module

bit 14 **Unimplemented:** Read as '0' bit 13 **SPISIDL:** Stop in Idle Mode bit

1 = Discontinue the module operation when device enters Idle mode

0 = Continue the module operation in Idle mode

bit 12-11 Unimplemented: Read as '0'

bit 10-8 SPIBEC<2:0>: SPIx Buffer Element Count bits (valid in Enhanced Buffer mode)

Master mode:

Number of SPIx transfers are pending.

Slave mode:

Number of SPIx transfers are unread.

bit 7 SRMPT: Shift Register (SPIxSR) Empty bit (valid in Enhanced Buffer mode)

1 = SPIx Shift register is empty and ready to send or receive the data

0 = SPIx Shift register is not empty

bit 6 SPIROV: Receive Overflow Flag bit

1 = A new byte/word is completely received and discarded. The user application has not read the previous data in the SPIxBUF register

0 = No overflow has occurred

bit 5 SRXMPT: Receive FIFO Empty bit (valid in Enhanced Buffer mode)

1 = RX FIFO is empty

0 = RX FIFO is not empty

bit 4-2 SISEL<2:0>: SPIx Buffer Interrupt Mode bits (valid in Enhanced Buffer mode)

111 = Interrupt when the SPIx transmit buffer is full (SPIxTBF bit is set)

110 = Interrupt when last bit is shifted into SPIxSR, and as a result, the TX FIFO is empty

101 = Interrupt when the last bit is shifted out of SPIxSR, and the transmit is complete

100 = Interrupt when one data is shifted into the SPIxSR, and as a result, the TX FIFO has one open memory location

011 = Interrupt when the SPIx receive buffer is full (SPIxRBF bit set)

010 = Interrupt when the SPIx receive buffer is 3/4 or more full

001 = Interrupt when data is available in the receive buffer (SRMPT bit is set)

000 = Interrupt when the last data in the receive buffer is read, as a result, the buffer is empty (SRXMPT bit set)

Preliminary

REGISTER 18-1: SPIXSTAT: SPIX STATUS AND CONTROL REGISTER (CONTINUED)

bit 1 SPITBF: SPIx Transmit Buffer Full Status bit

1 = Transmit not yet started, SPIxTXB is full 0 = Transmit started, SPIxTXB is empty

Standard Buffer Mode:

Automatically set in hardware when core writes to the SPIxBUF location, loading SPIxTXB. Automatically cleared in hardware when SPIx module transfers data from SPIxTXB to SPIxSR.

Enhanced Buffer Mode:

Automatically set in hardware when CPU writes to the SPIxBUF location, loading the last available buffer location. Automatically cleared in hardware when a buffer location is available for a CPU write operation.

bit 0 SPIRBF: SPIx Receive Buffer Full Status bit

1 = Receive complete, SPIxRXB is full

0 = Receive is incomplete, SPIxRXB is empty

Standard Buffer Mode:

Automatically set in hardware when SPIx transfers data from SPIxSR to SPIxRXB. Automatically cleared in hardware when core reads the SPIxBUF location, reading SPIxRXB.

Enhanced Buffer Mode:

Automatically set in hardware when SPIx transfers data from SPIxSR to the buffer, filling the last unread buffer location. Automatically cleared in hardware when a buffer location is available for a transfer from SPIxSR.

REGISTER 18-2: SPIXCON1: SPIX CONTROL REGISTER 1

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	_	_	DISSCK	DISSDO	MODE16	SMP	CKE ⁽¹⁾
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SSEN ⁽²⁾	CKP	MSTEN		SPRE<2:0>(PPRE<	<1:0> ⁽³⁾	
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12 DISSCK: Disable SCKx Pin bit (SPI Master modes only)

1 = Internal SPI clock is disabled, pin functions as I/O

0 = Internal SPI clock is enabled

bit 11 DISSDO: Disable SDOx Pin bit

1 = SDOx pin is not used by the module; pin functions as I/O

0 = SDOx pin is controlled by the module

bit 10 MODE16: Word/Byte Communication Select bit

1 = Communication is word-wide (16 bits)0 = Communication is byte-wide (8 bits)

bit 9 SMP: SPIx Data Input Sample Phase bit

Master mode:

1 = Input data is sampled at end of data output time

0 = Input data is sampled at middle of data output time

Slave mode:

SMP must be cleared when SPIx is used in Slave mode.

bit 8 **CKE:** SPIx Clock Edge Select bit⁽¹⁾

1 = Serial output data changes on transition from active clock state to idle clock state (refer to bit 6)

0 = Serial output data changes on transition from idle clock state to active clock state (refer to bit 6)

bit 7 SSEN: Slave Select Enable bit (Slave mode)(2)

 $1 = \overline{SSx}$ pin is used for Slave mode

 $0 = \overline{SSx}$ pin is not used by module. Pin is controlled by port function

bit 6 **CKP:** Clock Polarity Select bit

1 = Idle state for clock is a high level; active state is a low level 0 = Idle state for clock is a low level; active state is a high level

bit 5 MSTEN: Master Mode Enable bit

1 = Master mode

0 = Slave mode

bit 4-2 SPRE<2:0>: Secondary Prescale bits (Master mode)(3)

111 = Secondary prescale 1:1

110 = Secondary prescale 2:1

•

000 = Secondary prescale 8:1

bit 1-0 **PPRE<1:0>:** Primary Prescale bits (Master mode)⁽³⁾

11 = Primary prescale 1:1

10 = Primary prescale 4:1

01 = Primary prescale 16:1

00 = Primary prescale 64:1

Note 1: The CKE bit is not used in Framed SPI modes. Program this bit to '0' for Framed SPI modes (FRMEN = 1).

2: This bit must be cleared when FRMEN = 1.

3: Do not set both Primary and Secondary prescalers to the value of 1:1.

SPIXCON2: SPIX CONTROL REGISTER 2 REGISTER 18-3:

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
FRMEN	SPIFSD	FRMPOL	_	_	_	_	_
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
_	_	_	_	_	_	FRMDLY	SPIBEN
bit 7							bit 0

R = Readable bit

Legend:

W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15 FRMEN: Framed SPIx Support bit

1 = Framed SPIx support is enabled (\overline{SSx} pin used as frame sync pulse input/output)

0 = Framed SPIx support is disabled

bit 14 SPIFSD: Frame Sync Pulse Direction Control bit

> 1 = Frame sync pulse input (slave) 0 = Frame sync pulse output (master)

bit 13 FRMPOL: Frame Sync Pulse Polarity bit

> 1 = Frame sync pulse is active-high 0 = Frame sync pulse is active-low

bit 12-2 Unimplemented: Read as '0'

bit 1 FRMDLY: Frame Sync Pulse Edge Select bit

> 1 = Frame sync pulse coincides with first bit clock 0 = Frame sync pulse precedes first bit clock

bit 0 SPIBEN: Enhanced Buffer Enable bit

1 = Enhanced Buffer is enabled

0 = Enhanced Buffer is disabled (Standard mode)

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19.0 INTER-INTEGRATED CIRCUIT™ (I²C™)

- Note 1: This data sheet summarizes the features dsPIC33EPXXXGP50X. the dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 19. "Inter-Integrated Circuit™ (I²C™)" (DS70330) of the "dsPIC33E/PIC24E Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X family of devices contain two Inter-Integrated Circuit (I²C) modules: I2C1 and I2C2.

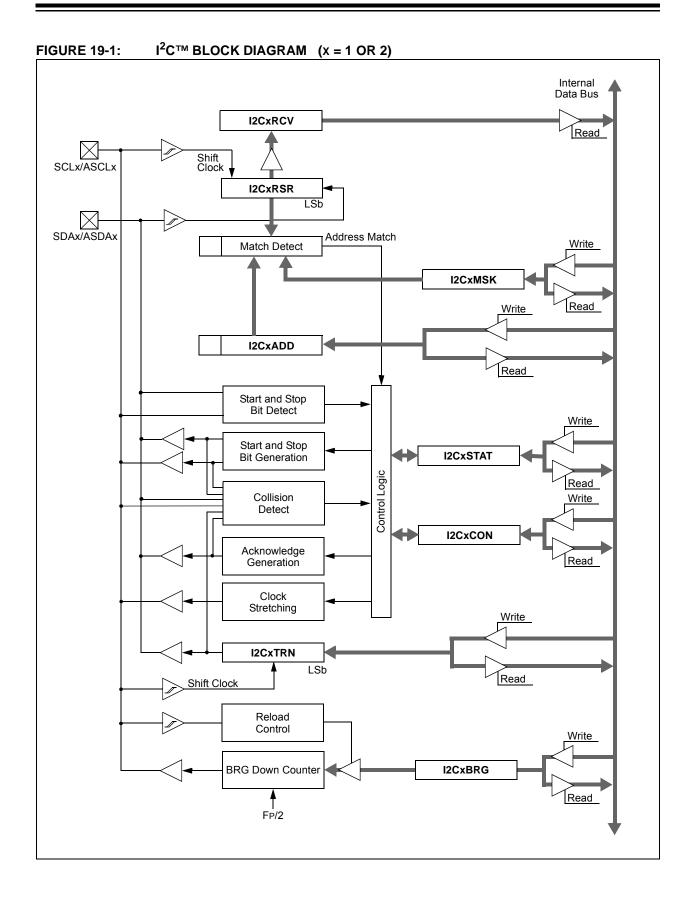
The I²C module provides complete hardware support for both Slave and Multi-Master modes of the I²C serial communication standard, with a 16-bit interface.

The I²C module has a 2-pin interface:

- · The SCLx pin is clock.
- · The SDAx pin is data.

The I²C module offers the following key features:

- I²C interface supporting both Master and Slave modes of operation.
- I²C Slave mode supports 7 and 10-bit address.
- I²C Master mode supports 7 and 10-bit address.
- I²C port allows bidirectional transfers between master and slaves.
- Serial clock synchronization for I²C port can be used as a handshake mechanism to suspend and resume serial transfer (SCLREL control).
- 1²C supports multi-master operation, detects bus collision and arbitrates accordingly.
- IPMI support
- · SMBus support



19.1 I²C Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter

this URL in your browser:

http://www.microchip.com/wwwproducts/ Devices.aspx?dDocName=en555464

19.1.1 KEY RESOURCES

- Section 19. "Inter-Integrated Circuit (I²C)" (DS70330)
- · Code Samples
- · Application Notes
- · Software Libraries
- Webinars
- All related dsPIC33E/PIC24E Family Reference Manuals Sections
- · Development Tools

19.2 I²C Control Registers

REGISTER 19-1: I2CxCON: I2Cx CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-1 HC	R/W-0	R/W-0	R/W-0	R/W-0
I2CEN	_	I2CSIDL	SCLREL	IPMIEN ⁽¹⁾	A10M	DISSLW	SMEN
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0 HC				
GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN
bit 7							bit 0

Legend:	U = Unimplemented bit, read as '0'					
R = Readable bit	W = Writable bit HS = Set in hardware HC = Cleared in hardware					
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown			

bit 15 I2CEN: I2Cx Enable bit

1 = Enables the I2Cx module and configures the SDAx and SCLx pins as serial port pins

0 = Disables the I2Cx module. All I²CTM pins are controlled by port functions

bit 14 **Unimplemented:** Read as '0' bit 13 **I2CSIDL:** Stop in Idle Mode bit

1 = Discontinue module operation when device enters an Idle mode

0 = Continue module operation in Idle mode

bit 12 **SCLREL:** SCLx Release Control bit (when operating as I²C slave)

1 = Release SCLx clock

0 = Hold SCLx clock low (clock stretch)

If STREN = 1:

Bit is R/W (i.e., software can write '0' to initiate stretch and write '1' to release clock). Hardware clear at beginning of every slave data byte transmission. Hardware clear at end of every slave address byte reception. Hardware clear at end of every slave data byte reception.

If STREN = 0

Bit is R/S (i.e., software can only write '1' to release clock). Hardware clear at beginning of every slave data byte transmission. Hardware clear at the end of every slave address byte reception.

bit 11 IPMIEN: Intelligent Peripheral Management Interface (IPMI) Enable bit⁽¹⁾

1 = IPMI mode is enabled; all addresses Acknowledged

0 = IPMI mode disabled

bit 10 **A10M:** 10-bit Slave Address bit

1 = I2CxADD is a 10-bit slave address0 = I2CxADD is a 7-bit slave address

bit 9 DISSLW: Disable Slew Rate Control bit

1 = Slew rate control disabled0 = Slew rate control enabled

bit 8 SMEN: SMBus Input Levels bit

1 = Enable I/O pin thresholds compliant with SMBus specification

0 = Disable SMBus input thresholds

bit 7 **GCEN:** General Call Enable bit (when operating as I²C slave)

1 = Enable interrupt when a general call address is received in the I2CxRSR (module is enabled for reception)

0 = General call address disabled

Note 1: When performing Master operations, ensure that the IPMIEN bit is '0'.

REGISTER 19-1: I2CxCON: I2Cx CONTROL REGISTER (CONTINUED)

bit 6 STREN: SCLx Clock Stretch Enable bit (when operating as I²C slave)

Used in conjunction with SCLREL bit.

1 = Enable software or receive clock stretching

0 = Disable software or receive clock stretching

bit 5 **ACKDT:** Acknowledge Data bit (when operating as I²C master, applicable during master receive)

Value that is transmitted when the software initiates an Acknowledge sequence.

1 = Send NACK during Acknowledge

0 = Send ACK during Acknowledge

bit 4 ACKEN: Acknowledge Sequence Enable bit

(when operating as I²C master, applicable during master receive)

1 = Initiate Acknowledge sequence on SDAx and SCLx pins and transmit ACKDT data bit.

Hardware clear at end of master Acknowledge sequence.

0 = Acknowledge sequence not in progress

bit 3 **RCEN:** Receive Enable bit (when operating as I²C master)

1 = Enables Receive mode for I^2C . Hardware clear at end of eighth bit of master receive data byte.

0 = Receive sequence not in progress

bit 2 **PEN:** Stop Condition Enable bit (when operating as I²C master)

1 = Initiate Stop condition on SDAx and SCLx pins. Hardware clear at end of master Stop sequence.

0 = Stop condition not in progress

bit 1 **RSEN:** Repeated Start Condition Enable bit (when operating as I²C master)

1 = Initiate Repeated Start condition on SDAx and SCLx pins. Hardware clear at end of

master Repeated Start sequence.

0 = Repeated Start condition not in progress

bit 0 **SEN:** Start Condition Enable bit (when operating as I²C master)

1 = Initiate Start condition on SDAx and SCLx pins. Hardware clear at end of master Start sequence.

0 = Start condition not in progress

Note 1: When performing Master operations, ensure that the IPMIEN bit is '0'.

REGISTER 19-2: I2CxSTAT: I2Cx STATUS REGISTER

R-0 HSC	R-0 HSC	U-0	U-0	U-0	R/C-0 HS	R-0 HSC	R-0 HSC
ACKSTAT	TRSTAT	_	_	_	BCL	GCSTAT	ADD10
bit 15							bit 8

R/C-0 HS	R/C-0 HS	R-0 HSC	R/C-0 HSC	R/C-0 HSC	R-0 HSC	R-0 HSC	R-0 HSC
IWCOL	I2COV	D_A	Р	S	R_W	RBF	TBF
bit 7							bit 0

Legend:	U = Unimplemented bit, read as '0'					
R = Readable bit	W = Writable bit HS = Set in hardware HSC = Hardware set/cleare					
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown			

bit 15 ACKSTAT: Acknowledge Status bit

(when operating as I²C[™] master, applicable to master transmit operation)

1 = NACK received from slave 0 = ACK received from slave

Hardware set or clear at end of slave Acknowledge.

bit 14 **TRSTAT:** Transmit Status bit (when operating as I²C master, applicable to master transmit operation)

1 = Master transmit is in progress (8 bits + ACK)

0 = Master transmit is not in progress

Hardware set at beginning of master transmission. Hardware clear at end of slave Acknowledge.

bit 13-11 Unimplemented: Read as '0'

bit 10 BCL: Master Bus Collision Detect bit

1 = A bus collision has been detected during a master operation

0 = No collision

Hardware set at detection of bus collision.

bit 9 GCSTAT: General Call Status bit

1 = General call address was received0 = General call address was not received

Hardware set when address matches general call address. Hardware clear at Stop detection.

bit 8 ADD10: 10-bit Address Status bit

1 = 10-bit address was matched 0 = 10-bit address was not matched

Hardware set at match of 2nd byte of matched 10-bit address. Hardware clear at Stop detection.

bit 7 IWCOL: Write Collision Detect bit

1 = An attempt to write the I2CxTRN register failed because the I²C module is busy

0 = No collision

Hardware set at occurrence of write to I2CxTRN while busy (cleared by software).

bit 6 I2COV: Receive Overflow Flag bit

1 = A byte was received while the I2CxRCV register is still holding the previous byte

0 = No overflow

Hardware set at attempt to transfer I2CxRSR to I2CxRCV (cleared by software).

bit 5 **D_A:** Data/Address bit (when operating as I²C slave)

1 = Indicates that the last byte received was data

0 = Indicates that the last byte received was device address

Hardware clear at device address match. Hardware set by reception of slave byte.

bit 4 **P:** Stop bit

1 = Indicates that a Stop bit has been detected last

0 = Stop bit was not detected last

Hardware set or clear when Start, Repeated Start or Stop detected.

REGISTER 19-2: I2CxSTAT: I2Cx STATUS REGISTER (CONTINUED)

bit 3 S: Start bit

bit 2

1 = Indicates that a Start (or Repeated Start) bit has been detected last

0 = Start bit was not detected last

Hardware set or clear when Start, Repeated Start or Stop detected.

R_W: Read/Write Information bit (when operating as I²C slave)

1 = Read – indicates data transfer is output from slave 0 = Write – indicates data transfer is input to slave

Hardware set or clear after reception of I²C device address byte.

bit 1 RBF: Receive Buffer Full Status bit

1 = Receive complete, I2CxRCV is full

0 = Receive not complete, I2CxRCV is empty

Hardware set when I2CxRCV is written with received byte. Hardware clear when software

reads I2CxRCV.

bit 0 TBF: Transmit Buffer Full Status bit

1 = Transmit in progress, I2CxTRN is full 0 = Transmit complete, I2CxTRN is empty

Hardware set when software writes I2CxTRN. Hardware clear at completion of data transmission.

REGISTER 19-3: I2CxMSK: I2Cx SLAVE MODE ADDRESS MASK REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
_	_	_	_	_	_	AMSK9	AMSK8
bit 15							bit 8

| R/W-0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| AMSK7 | AMSK6 | AMSK5 | AMSK4 | AMSK3 | AMSK2 | AMSK1 | AMSK0 |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-10 Unimplemented: Read as '0'

bit 9-0 AMSKx: Mask for Address bit x Select bit

For 10-bit Address:

1 = Enable masking for bit Ax of incoming message address; bit match is not required in this position

0 = Disable masking for bit Ax; bit match is required in this position

For 7-bit Address (I2CxMSK<6:0> only):

1 = Enable masking for bit Ax + 1 of incoming message address; bit match is not required in this position

0 =Disable masking for bit Ax + 1; bit match is required in this position

20.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 17. "UART" (DS70582) of the "dsPIC33E/PIC24E Family Reference Manual", which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X family of devices contain two UART modules.

The Universal Asynchronous Receiver Transmitter (UART) module is one of the serial I/O modules available in the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X device family. The UART is a full-duplex asynchronous system that can communicate with peripheral devices, such as personal computers, LIN, RS-232 and RS-485 interfaces. The module also supports a hardware flow control option with the UxCTS and UxRTS pins and also includes an IrDA® encoder and decoder.

Note: Hardware flow control using UxRTS and UxCTS is not available on all pin count devices. See the "Pin Diagrams" section for availability.

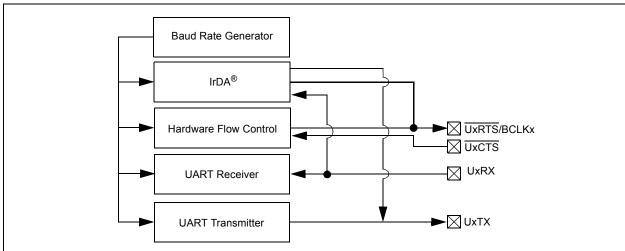
The primary features of the UART module are:

- Full-Duplex, 8- or 9-bit Data Transmission through the UxTX and UxRX pins
- Even, Odd or No Parity Options (for 8-bit data)
- · One or two stop bits
- Hardware flow control option with UxCTS and UxRTS pins
- Fully integrated Baud Rate Generator with 16-bit prescaler
- Baud rates ranging from 4.375 Mbps to 67 bps at 16x mode at 70 MIPS
- Baud rates ranging from 17.5 Mbps to 267 bps at 4x mode at 70 MIPS
- 4-deep First-In First-Out (FIFO) Transmit Data buffer
- · 4-deep FIFO Receive Data buffer
- · Parity, framing and buffer overrun error detection
- Support for 9-bit mode with Address Detect (9th bit = 1)
- · Transmit and Receive interrupts
- A separate interrupt for all UART error conditions
- · Loopback mode for diagnostic support
- · Support for Sync and Break characters
- · Support for automatic baud rate detection
- IrDA[®] encoder and decoder logic
- 16x baud clock output for IrDA[®] support

A simplified block diagram of the UART module is shown in Figure 20-1. The UART module consists of these key hardware elements:

- · Baud Rate Generator
- · Asynchronous Transmitter
- · Asynchronous Receiver





20.1 UART Helpful Tips

- 1. In multi-node direct-connect UART networks, receive inputs react to complementary logic level defined by the URXINV bit (UxMODE<4>), which defines the idle state, the default of which is logic high, (i.e., URXINV = 0). Because remote devices do not initialize at the same time, it is likely that one of the devices, because the RX line is floating, will trigger a start bit detection and will cause the first byte received after the device has been initialized to be invalid. To avoid this situation, the user should use a pull-up or pull-down resistor on the RX pin depending on the value of the URXINV bit.
 - a) If URXINV = 0, use a pull-up resistor on the RX pin.
 - b) If URXINV = 1, use a pull-down resistor on the RX pin.
- 2. The first character received on a wake-up from Sleep mode caused by activity on the UxRX pin of the UART module will be invalid. In Sleep mode, peripheral clocks are disabled. By the time the oscillator system has restarted and stabilized from Sleep mode, the baud rate bit sampling clock relative to the incoming UxRX bit timing is no longer synchronized, resulting in the first character being invalid. This is to be expected.

20.2 UART Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:

In the event you are not able to access the product page using the link above, enter this URL in your browser:

http://www.microchip.com/wwwproducts/ Devices.aspx?dDocName=en555464

20.2.1 KEY RESOURCES

- Section 17. "UART" (DS70582)
- Code Samples
- · Application Notes
- · Software Libraries
- Webinars
- All related dsPIC33E/PIC24E Family Reference Manuals Sections
- · Development Tools

20.3 UART Control Registers

REGISTER 20-1: UxMODE: UARTx MODE REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
UARTEN ⁽¹⁾	_	USIDL	IREN ⁽²⁾	RTSMD	_	UEN-	<1:0>
bit 15							bit 8

R/W-0 HC	R/W-0	R/W-0 HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL	.<1:0>	STSEL
bit 7							bit 0

Legend:	HC = Hardware cleared	HC = Hardware cleared			
R = Readable bit	W = Writable bit	U = Unimplemented bit,	read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 15 **UARTEN:** UARTx Enable bit

1 = UARTx is enabled; all UARTx pins are controlled by UARTx as defined by UEN<1:0>

0 = UARTx is disabled; all UARTx pins are controlled by PORT latches; UARTx power consumption

bit 14 **Unimplemented:** Read as '0'

bit 13 USIDL: Stop in Idle Mode bit

1 = Discontinue module operation when device enters Idle mode

0 = Continue module operation in Idle mode

bit 12 IREN: IrDA® Encoder and Decoder Enable bit(2)

1 = IrDA encoder and decoder enabled

0 = IrDA encoder and decoder disabled

bit 11 RTSMD: Mode Selection for UxRTS Pin bit

 $1 = \overline{\text{UxRTS}} \text{ pin in Simplex mode}$

 $0 = \overline{UxRTS}$ pin in Flow Control mode

bit 10 **Unimplemented:** Read as '0'

bit 9-8 **UEN<1:0>:** UARTx Pin Enable bits

11 = UxTX, UxRX and BCLKx pins are enabled and used; UxCTS pin controlled by PORT latches (3)

10 = UxTX, UxRX, $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins are enabled and used⁽⁴⁾

01 = UxTX, UxRX and UxRTS pins are enabled and used; UxCTS pin controlled by PORT latches (4)

00 = UxTX and UxRX pins are enabled and used; UxCTS and UxRTS/BCLKx pins controlled by PORT latches

bit 7 WAKE: Wake-up on Start bit Detect During Sleep Mode Enable bit

1 = UARTx continues to sample the UxRX pin; interrupt generated on falling edge; bit cleared in hardware on following rising edge

0 = No wake-up enabled

bit 6 LPBACK: UARTx Loopback Mode Select bit

1 = Enable Loopback mode

0 = Loopback mode is disabled

Note 1: Refer to Section 17. "UART" (DS70582) in the "dsPIC33E/PIC24E Family Reference Manual" for information on enabling the UART module for receive or transmit operation.

2: This feature is only available for the 16x BRG mode (BRGH = 0).

3: This feature is only available on 44-pin and 64-pin devices.

4: This feature is only available on 64-pin devices.

REGISTER 20-1: UXMODE: UARTX MODE REGISTER (CONTINUED)

bit 5 ABAUD: Auto-Baud Enable bit

1 = Enable baud rate measurement on the next character – requires reception of a Sync field (55h) before other data; cleared in hardware upon completion

0 = Baud rate measurement disabled or completed

bit 4 URXINV: Receive Polarity Inversion bit

1 = UxRX Idle state is '0' 0 = UxRX Idle state is '1'

bit 3 BRGH: High Baud Rate Enable bit

1 = BRG generates 4 clocks per bit period (4x baud clock, High-Speed mode)
 0 = BRG generates 16 clocks per bit period (16x baud clock, Standard mode)

bit 2-1 PDSEL<1:0>: Parity and Data Selection bits

11 = 9-bit data, no parity 10 = 8-bit data, odd parity 01 = 8-bit data, even parity 00 = 8-bit data, no parity

bit 0 STSEL: Stop Bit Selection bit

1 = Two Stop bits 0 = One Stop bit

Note 1: Refer to Section 17. "UART" (DS70582) in the "dsPIC33E/PIC24E Family Reference Manual" for information on enabling the UART module for receive or transmit operation.

- 2: This feature is only available for the 16x BRG mode (BRGH = 0).
- 3: This feature is only available on 44-pin and 64-pin devices.
- 4: This feature is only available on 64-pin devices.

REGISTER 20-2: UxSTA: UARTx STATUS AND CONTROL REGISTER

R/W-0	R/W-0	R/W-0	U-0	R/W-0 HC	R/W-0	R-0	R-1
UTXISEL1	UTXINV	UTXISEL0	_	UTXBRK	UTXEN ⁽¹⁾	UTXBF	TRMT
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R-1	R-0	R-0	R/C-0	R-0
URXISE	L<1:0>	ADDEN	RIDLE	PERR	FERR	OERR	URXDA
bit 7		•					bit 0

Legend:	HC = Hardware cleared		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15,13 UTXISEL<1:0>: Transmission Interrupt Mode Selection bits
 - 11 = Reserved; do not use
 - 10 = Interrupt when a character is transferred to the Transmit Shift Register, and as a result, the transmit buffer becomes empty
 - 01 = Interrupt when the last character is shifted out of the Transmit Shift Register; all transmit operations are completed
 - 00 = Interrupt when a character is transferred to the Transmit Shift Register (this implies there is at least one character open in the transmit buffer)
- bit 14 UTXINV: Transmit Polarity Inversion bit

If IREN = 0:

- 1 = UxTX Idle state is '0'
- 0 = UxTX Idle state is '1'

If IREN = 1:

- 1 = IrDA encoded UxTX Idle state is '1'
- 0 = IrDA encoded UxTX Idle state is '0'
- bit 12 **Unimplemented:** Read as '0'
- bit 11 UTXBRK: Transmit Break bit
 - 1 = Send Sync Break on next transmission Start bit, followed by twelve '0' bits, followed by Stop bit; cleared by hardware upon completion
 - 0 = Sync Break transmission disabled or completed
- bit 10 UTXEN: Transmit Enable bit⁽¹⁾
 - 1 = Transmit enabled, UxTX pin controlled by UARTx
 - 0 = Transmit disabled, any pending transmission is aborted and buffer is reset. UxTX pin controlled by port.
- bit 9 **UTXBF:** Transmit Buffer Full Status bit (read-only)
 - 1 = Transmit buffer is full
 - 0 = Transmit buffer is not full, at least one more character can be written
- bit 8 **TRMT:** Transmit Shift Register Empty bit (read-only)
 - 1 = Transmit Shift Register is empty and transmit buffer is empty (the last transmission has completed)
 - 0 = Transmit Shift Register is not empty, a transmission is in progress or queued
- bit 7-6 URXISEL<1:0>: Receive Interrupt Mode Selection bits
 - 11 = Interrupt is set on UxRSR transfer making the receive buffer full (i.e., has 4 data characters)
 - 10 = Interrupt is set on UxRSR transfer making the receive buffer 3/4 full (i.e., has 3 data characters)
 - 0x = Interrupt is set when any character is received and transferred from the UxRSR to the receive buffer. Receive buffer has one or more characters.
- Note 1: Refer to Section 17. "UART" (DS70582) in the "dsPIC33E/PIC24E Family Reference Manual" for information on enabling the UART module for transmit operation.

REGISTER 20-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)

- bit 5 ADDEN: Address Character Detect bit (bit 8 of received data = 1)
 - 1 = Address Detect mode enabled. If 9-bit mode is not selected, this does not take effect.
 - 0 = Address Detect mode disabled
- bit 4 RIDLE: Receiver Idle bit (read-only)
 - 1 = Receiver is Idle
 - 0 = Receiver is active
- bit 3 **PERR:** Parity Error Status bit (read-only)
 - 1 = Parity error has been detected for the current character (character at the top of the receive FIFO)
 - 0 = Parity error has not been detected
- bit 2 FERR: Framing Error Status bit (read-only)
 - 1 = Framing error has been detected for the current character (character at the top of the receive FIFO)
 - 0 = Framing error has not been detected
- bit 1 OERR: Receive Buffer Overrun Error Status bit (read/clear only)
 - 1 = Receive buffer has overflowed
 - 0 = Receive buffer has not overflowed. Clearing a previously set OERR bit (1 \rightarrow 0 transition) resets the receiver buffer and the UxRSR to the empty state.
- bit 0 **URXDA:** Receive Buffer Data Available bit (read-only)
 - 1 = Receive buffer has data, at least one more character can be read
 - 0 = Receive buffer is empty
- Note 1: Refer to Section 17. "UART" (DS70582) in the "dsPIC33E/PIC24E Family Reference Manual" for information on enabling the UART module for transmit operation.

21.0 ENHANCED CAN (ECAN™) MODULE (dsPIC33EPXXXGP/ MC50X DEVICES ONLY)

Note 1: This data sheet summarizes the features the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 21. "Enhanced Controller Area Network (ECAN™)" (DS70353) of the "dsPIC33E/PIC24E Family Reference Manual', which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

21.1 Overview

The Enhanced Controller Area Network (ECAN) module is a serial interface, useful for communicating with other CAN modules or microcontroller devices. This interface/protocol was designed to allow communications within noisy environments. The dsPIC33EPXXXGP/MC50X devices contain one FCAN module.

The ECAN module is a communication controller implementing the CAN 2.0 A/B protocol, as defined in the BOSCH CAN specification. The module supports CAN 1.2, CAN 2.0A, CAN 2.0B Passive and CAN 2.0B Active versions of the protocol. The module implementation is a full CAN system. The CAN specification is not covered within this data sheet. The reader can refer to the BOSCH CAN specification for further details.

The ECAN module features are as follows:

- Implementation of the CAN protocol, CAN 1.2, CAN 2.0A and CAN 2.0B
- · Standard and extended data frames
- · 0-8 bytes data length
- · Programmable bit rate up to 1 Mbit/sec
- Automatic response to remote transmission requests
- Up to eight transmit buffers with application specified prioritization and abort capability (each buffer can contain up to 8 bytes of data)
- Up to 32 receive buffers (each buffer can contain up to 8 bytes of data)
- Up to 16 full (standard/extended identifier) acceptance filters
- · Three full acceptance filter masks
- DeviceNet[™] addressing support
- Programmable wake-up functionality with integrated low-pass filter
- Programmable Loopback mode supports self-test operation
- Signaling via interrupt capabilities for all CAN receiver and transmitter error states
- · Programmable clock source
- Programmable link to Input Capture module (IC2) for time-stamping and network synchronization
- · Low-power Sleep and Idle mode

The CAN bus module consists of a protocol engine and message buffering/control. The CAN protocol engine handles all functions for receiving and transmitting messages on the CAN bus. Messages are transmitted by first loading the appropriate data registers. Status and errors can be checked by reading the appropriate registers. Any message detected on the CAN bus is checked for errors and then matched against filters to see if it should be received and stored in one of the receive registers.

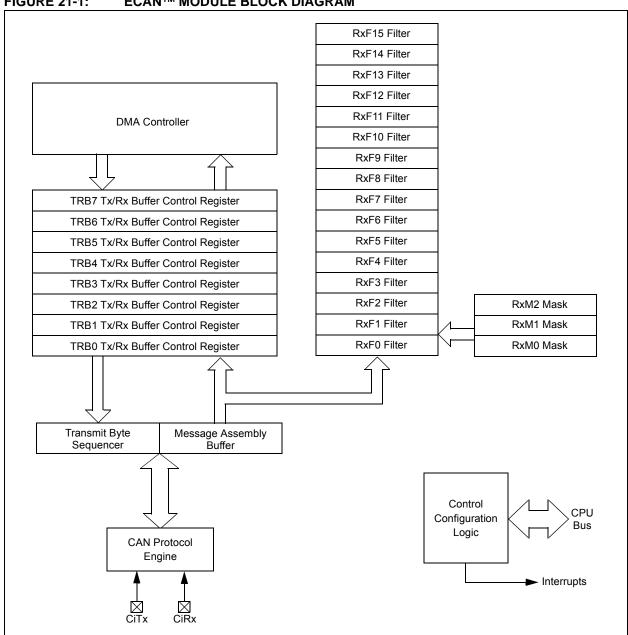


FIGURE 21-1: ECAN™ MODULE BLOCK DIAGRAM

21.2 Modes of Operation

The ECAN module can operate in one of several operation modes selected by the user. These modes include:

- · Initialization mode
- · Disable mode
- · Normal Operation mode
- · Listen Only mode
- · Listen All Messages mode
- · Loopback mode

Modes are requested by setting the REQOP<2:0> bits (CiCTRL1<10:8>). Entry into a mode is Acknowledged by monitoring the OPMODE<2:0> bits (CiCTRL1<7:5>). The module does not change the mode and the OPMODE bits until a change in mode is acceptable, generally during bus Idle time, which is defined as at least 11 consecutive recessive bits.

21.3 ECAN Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter this URL in your browser:
http://www.microchip.com/wwwproducts/
Devices.aspx?dDocName=en555464

21.3.1 KEY RESOURCES

- Section 21. "Enhanced Controller Area Network (ECAN™)" (DS70353)
- · Code Samples
- · Application Notes
- Software Libraries
- Webinars
- All related dsPIC33E/PIC24E Family Reference Manuals Sections
- · Development Tools

21.4 ECAN Control Registers

REGISTER 21-1: CICTRL1: ECAN™ CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0
_	_	CSIDL	ABAT	CANCKS		REQOP<2:0>	
bit 15							bit 8

R-1	R-0	R-0	U-0	R/W-0	U-0	U-0	R/W-0
	OPMODE<2:0>		_	CANCAP	-	_	WIN
bit 7							bit 0

Legend:	C = Writable bit, but only '0' can be written to clear the bit $r = Bit$ is Reserved					
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown			

bit 15-14 **Unimplemented:** Read as '0' bit 13 **CSIDL:** Stop in Idle Mode bit

1 = Discontinue module operation when device enters Idle mode

0 = Continue module operation in Idle mode

bit 12 ABAT: Abort All Pending Transmissions bit

1 = Signal all transmit buffers to abort transmission

0 = Module will clear this bit when all transmissions are aborted

bit 11 CANCKS: ECAN Module Clock (FCAN) Source Select bit

1 = FCAN is equal to FP 0 = FCAN is equal to 2 * FP

bit 10-8 **REQOP<2:0>:** Request Operation Mode bits

111 = Set Listen All Messages mode

110 = Reserved

101 = Reserved

100 = Set Configuration mode011 = Set Listen Only Mode

010 = Set Loopback mode 001 = Set Disable mode

000 = Set Normal Operation mode

bit 7-5 **OPMODE<2:0>**: Operation Mode bits

111 = Module is in Listen All Messages mode

110 = Reserved

101 = Reserved

100 = Module is in Configuration mode

011 = Module is in Listen Only mode 010 = Module is in Loopback mode

001 = Module is in Disable mode

000 = Module is in Normal Operation mode

bit 4 **Unimplemented:** Read as '0'

bit 3 CANCAP: CAN Message Receive Timer Capture Event Enable bit

1 = Enable input capture based on CAN message receive

0 = Disable CAN capture

bit 2-1 **Unimplemented:** Read as '0'

bit 0 WIN: SFR Map Window Select bit

1 = Use filter window

0 = Use buffer window

REGISTER 21-2: CICTRL2: ECAN™ CONTROL REGISTER 2

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	_	_	_	_	_	_	_
bit 15							bit 8

U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
_	_	_			DNCNT<4:0>		
bit 7							bit 0

 Legend:
 C = Writable bit, but only '0' can be written to clear the bit

 R = Readable bit
 W = Writable bit
 U = Unimplemented bit, read as '0'

 -n = Value at POR
 '1' = Bit is set
 '0' = Bit is cleared
 x = Bit is unknown

bit 15-5 **Unimplemented:** Read as '0'

bit 4-0 **DNCNT<4:0>:** DeviceNet™ Filter Bit Number bits

10010-11111 = Invalid selection

10001 = Compare up to data byte 3, bit 6 with EID<17>

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00001 = Compare up to data byte 1, bit 7 with EID<0>

00000 = Do not compare data bytes

REGISTER 21-3: CIVEC: ECAN™ INTERRUPT CODE REGISTER

U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
_	_	_			FILHIT<4:0>		
bit 15							bit 8

U-0	R-1	R-0	R-0	R-0	R-0	R-0	R-0
_				ICODE<6:0>	•		
bit 7							bit 0

 Legend:
 C = Writable bit, but only '0' can be written to clear the bit

 R = Readable bit
 W = Writable bit
 U = Unimplemented bit, read as '0'

 -n = Value at POR
 '1' = Bit is set
 '0' = Bit is cleared
 x = Bit is unknown

bit 15-13 Unimplemented: Read as '0' bit 12-8 FILHIT<4:0>: Filter Hit Number bits

10000-11111 = Reserved

01111 = Filter 15

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00001 = Filter 1 00000 = Filter 0

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **ICODE<6:0>:** Interrupt Flag Code bits

1000101-1111111 = Reserved

1000100 = FIFO almost full interrupt

1000011 = Receiver overflow interrupt

1000010 = Wake-up interrupt

1000001 = Error interrupt

1000000 = No interrupt

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0010000-0111111 = Reserved 0001111 = RB15 buffer Interrupt

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0001001 = RB9 buffer interrupt

0001000 = RB8 buffer interrupt

0000111 = TRB7 buffer interrupt

0000110 = TRB6 buffer interrupt

0000101 = TRB5 buffer interrupt

0000100 = TRB4 buffer interrupt

0000011 = TRB3 buffer interrupt

0000010 = TRB2 buffer interrupt

0000001 = TRB1 buffer interrupt

0000000 = TRB0 Buffer interrupt

REGISTER 21-4: CIFCTRL: ECAN™ FIFO CONTROL REGISTER

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	DMABS<2:0>		_	_	_	_	_
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	_	_			FSA<4:0>		
bit 7							bit 0

Legend:	C = Writable bit, but o	nly '0' can be written to clear th	ne bit
R = Readable bit	W = Writable bit	U = Unimplemented bit,	read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 DMABS<2:0>: DMA Buffer Size bits

111 = Reserved

110 = 32 buffers in RAM

101 = 24 buffers in RAM

100 = 16 buffers in RAM

011 = 12 buffers in RAM

010 = 8 buffers in RAM

001 = 6 buffers in RAM

000 = 4 buffers in RAM

bit 12-5 **Unimplemented:** Read as '0'

bit 4-0 FSA<4:0>: FIFO Area Starts with Buffer bits

11111 = Read buffer RB31

11110 = Read buffer RB30

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00001 = Tx/Rx buffer TRB1 00000 = Tx/Rx buffer TRB0

REGISTER 21-5: CiFIFO: ECAN™ FIFO STATUS REGISTER

U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
_	_			FBP	<5:0>		
bit 15	-	-			_		bit 8

U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
_	_			FNRI	B<5:0>		
bit 7							bit 0

Legend: C = Writable bit, but only '0' can be written to clear the bit

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-14 Unimplemented: Read as '0'

bit 13-8 **FBP<5:0>:** FIFO Buffer Pointer bits

011111 = RB31 buffer 011110 = RB30 buffer

•

•

000001 = TRB1 buffer

000000 = TRB0 buffer

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **FNRB<5:0>:** FIFO Next Read Buffer Pointer bits

011111 = RB31 buffer 011110 = RB30 buffer

•

•

000001 = TRB1 buffer 000000 = TRB0 buffer

REGISTER 21-6: CIINTF: ECAN™ INTERRUPT FLAG REGISTER

U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
_	_	TXBO	TXBP	RXBP	TXWAR	RXWAR	EWARN
bit 15							bit 8

R/C-0	R/C-0	R/C-0	U-0	R/C-0	R/C-0	R/C-0	R/C-0
IVRIF	WAKIF	ERRIF	_	FIFOIF	RBOVIF	RBIF	TBIF
bit 7							bit 0

Legend:	C = Writable bit, but only '0' can be written to clear the bit			
R = Readable bit	W = Writable bit	U = Unimplemented bit,	, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 15-14	Unimplemented: Read as '0'
bit 13	TXBO: Transmitter in Error State Bus Off bit
	1 = Transmitter is in Bus Off state
	0 = Transmitter is not in Bus Off state
bit 12	TXBP: Transmitter in Error State Bus Passive bit
	1 = Transmitter is in Bus Passive state
	0 = Transmitter is not in Bus Passive state
bit 11	RXBP: Receiver in Error State Bus Passive bit
	1 = Receiver is in Bus Passive state
	0 = Receiver is not in Bus Passive state
bit 10	TXWAR: Transmitter in Error State Warning bit
	1 = Transmitter is in Error Warning state
	0 = Transmitter is not in Error Warning state
bit 9	RXWAR: Receiver in Error State Warning bit
	1 = Receiver is in Error Warning state 0 = Receiver is not in Error Warning state
hit 0	
bit 8	EWARN: Transmitter or Receiver in Error State Warning bit 1 = Transmitter or Receiver is in Error State Warning state
	0 = Transmitter or Receiver is in Error State Warning state
bit 7	IVRIF: Invalid Message Interrupt Flag bit
DIC 1	1 = Interrupt Request has occurred
	0 = Interrupt Request has not occurred
bit 6	WAKIF: Bus Wake-up Activity Interrupt Flag bit
	1 = Interrupt Request has occurred
	0 = Interrupt Request has not occurred
bit 5	ERRIF : Error Interrupt Flag bit (multiple sources in CilNTF<13:8> register)
	1 = Interrupt Request has occurred
	0 = Interrupt Request has not occurred
bit 4	Unimplemented: Read as '0'
bit 3	FIFOIF: FIFO Almost Full Interrupt Flag bit
	1 = Interrupt Request has occurred
	0 = Interrupt Request has not occurred
bit 2	RBOVIF: RX Buffer Overflow Interrupt Flag bit
	1 = Interrupt Request has occurred
	0 = Interrupt Request has not occurred
bit 1	RBIF: RX Buffer Interrupt Flag bit
	1 = Interrupt Request has occurred
	0 = Interrupt Request has not occurred
bit 0	TBIF: TX Buffer Interrupt Flag bit
	1 = Interrupt Request has occurred
	0 = Interrupt Request has not occurred

REGISTER 21-7: CIINTE: ECAN™ INTERRUPT ENABLE REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	_	_	_	_	_	_	_
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IVRIE	WAKIE	ERRIE	_	FIFOIE	RBOVIE	RBIE	TBIE
bit 7							bit 0

Legend:	C = Writable bit, but o	nly '0' can be written to clear the	he bit
R = Readable bit	W = Writable bit	U = Unimplemented bit	, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8	Unimplemented: Read as '0'
bit 7	IVRIE: Invalid Message Interrupt Enable bit
	1 = Interrupt Request Enabled
	0 = Interrupt Request not enabled
bit 6	WAKIE: Bus Wake-up Activity Interrupt Enable bit
	1 = Interrupt Request Enabled
	0 = Interrupt Request not enabled
bit 5	ERRIE: Error Interrupt Enable bit
	1 = Interrupt Request Enabled
	0 = Interrupt Request not enabled
bit 4	Unimplemented: Read as '0'
bit 3	FIFOIE: FIFO Almost Full Interrupt Enable bit
	1 = Interrupt Request Enabled
	0 = Interrupt Request not enabled
bit 2	RBOVIE: RX Buffer Overflow Interrupt Enable bit
	1 = Interrupt Request Enabled
	0 = Interrupt Request not enabled
bit 1	RBIE: RX Buffer Interrupt Enable bit
	1 = Interrupt Request Enabled
	0 = Interrupt Request not enabled

TBIE: TX Buffer Interrupt Enable bit

1 = Interrupt Request Enabled0 = Interrupt Request not enabled

bit 0

REGISTER 21-8: CIEC: ECAN™ TRANSMIT/RECEIVE ERROR COUNT REGISTER

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0		
TERRCNT<7:0>									
bit 15							bit 8		

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0		
RERRCNT<7:0>									
bit 7							bit 0		

Legend:C = Writable bit, but only '0' can be written to clear the bitR = Readable bitW = Writable bitU = Unimplemented bit, read as '0'-n = Value at POR'1' = Bit is set'0' = Bit is clearedx = Bit is unknown

bit 15-8 **TERRCNT<7:0>:** Transmit Error Count bits bit 7-0 **RERRCNT<7:0>:** Receive Error Count bits

REGISTER 21-9: CICFG1: ECAN™ BAUD RATE CONFIGURATION REGISTER 1

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	_	_	_	_	_	_	_
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
SJW	<1:0>			BRP<5:0>				
bit 7							bit 0	

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-8 Unimplemented: Read as '0'

bit 7-6 **SJW<1:0>:** Synchronization Jump Width bits

11 = Length is 4 x TQ

10 = Length is 3 x TQ

01 = Length is 2 x TQ

00 = Length is 1 x TQ

bit 5-0 BRP<5:0>: Baud Rate Prescaler bits

11 1111 = TQ = 2 x 64 x 1/FCAN

•

00 0010 = $TQ = 2 \times 3 \times 1/FCAN$

00 0001 = TQ = 2 x 2 x 1/FCAN

00 0000 = TQ = 2 x 1 x 1/FCAN

REGISTER 21-10: CICFG2: ECAN™ BAUD RATE CONFIGURATION REGISTER 2

U-0	R/W-x	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x
_	WAKFIL	_	_	_	;	SEG2PH<2:0>	
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
SEG2PHTS	SAM	;	SEG1PH<2:0>	•		PRSEG<2:0>	
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15 Unimplemented: Read as '0'

bit 14 WAKFIL: Select CAN bus Line Filter for Wake-up bit

1 = Use CAN bus line filter for wake-up

0 = CAN bus line filter is not used for wake-up

bit 13-11 **Unimplemented:** Read as '0'

bit 10-8 **SEG2PH<2:0>:** Phase Segment 2 bits

111 = Length is 8 x TQ

•

.

000 = Length is 1 x TQ

bit 7 SEG2PHTS: Phase Segment 2 Time Select bit

1 = Freely programmable

0 = Maximum of SEG1PH bits or Information Processing Time (IPT), whichever is greater

bit 6 SAM: Sample of the CAN bus Line bit

 $\ensuremath{\mathtt{1}}$ = Bus line is sampled three times at the sample point

0 = Bus line is sampled once at the sample point

bit 5-3 **SEG1PH<2:0>:** Phase Segment 1 bits

111 = Length is 8 x TQ

•

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000 = Length is $1 \times TQ$

bit 2-0 PRSEG<2:0>: Propagation Time Segment bits

111 = Length is 8 x TQ

•

•

•

000 = Length is 1 x TQ

REGISTER 21-11: CIFEN1: ECAN™ ACCEPTANCE FILTER ENABLE REGISTER 1

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
FLTEN15	FLTEN14	FLTEN13	FLTEN12	FLTEN11	FLTEN10	FLTEN9	FLTEN8
bit 15							bit 8

| R/W-1 |
|--------|--------|--------|--------|--------|--------|--------|--------|
| FLTEN7 | FLTEN6 | FLTEN5 | FLTEN4 | FLTEN3 | FLTEN2 | FLTEN1 | FLTEN0 |
| bit 7 | | | | | | | bit 0 |

Legend: C = Writable bit, but only '0' can be written to clear the bit

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 FLTENn: Enable Filter n to Accept Messages bits

1 = Enable Filter n0 = Disable Filter n

REGISTER 21-12: CIBUFPNT1: ECAN™ FILTER 0-3 BUFFER POINTER REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
	F3BP<	<3:0>		F2BP<3:0>				
bit 15							bit 8	

| R/W-0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| | F1BP< | <3:0> | | | F0BP | | |
| bit 7 | | | | | | | bit 0 |

Legend:C = Writable bit, but only '0' can be written to clear the bitR = Readable bitW = Writable bitU = Unimplemented bit, read as '0'-n = Value at POR'1' = Bit is set'0' = Bit is clearedx = Bit is unknown

bit 15-12 **F3BP<3:0>:** RX Buffer mask for Filter 3 bits 1111 = Filter hits received in RX FIFO buffer

1111 - Filter hits received in RX FIFO bulle 1110 = Filter hits received in RX Buffer 14

•

•

0001 = Filter hits received in RX Buffer 1

0000 = Filter hits received in RX Buffer 0

bit 11-8 **F2BP<3:0>:** RX Buffer mask for Filter 2 bits (same values as bit 15-12) bit 7-4 **F1BP<3:0>:** RX Buffer mask for Filter 1 bits (same values as bit 15-12)

bit 3-0 **F0BP<3:0>:** RX Buffer mask for Filter 0 bits (same values as bit 15-12)

REGISTER 21-13: CIBUFPNT2: ECAN™ FILTER 4-7 BUFFER POINTER REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
	F7BP<	<3:0>		F6BP<3:0>				
bit 15							bit 8	

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
	F5BP<	<3:0>		F4BP<3:0>				
bit 7							bit 0	

Legend: C = Writable bit, but only '0' can be written to clear the bit

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-12 **F7BP<3:0>:** RX Buffer mask for Filter 7 bits

1111 = Filter hits received in RX FIFO buffer 1110 = Filter hits received in RX Buffer 14

•

.

0001 = Filter hits received in RX Buffer 1 0000 = Filter hits received in RX Buffer 0

bit 11-8 **F6BP<3:0>:** RX Buffer mask for Filter 6 bits (same values as bit 15-12) bit 7-4 **F5BP<3:0>:** RX Buffer mask for Filter 5 bits (same values as bit 15-12)

bit 3-0 **F4BP<3:0>:** RX Buffer mask for Filter 4 bits (same values as bit 15-12)

REGISTER 21-14: CIBUFPNT3: ECAN™ FILTER 8-11 BUFFER POINTER REGISTER 3

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
	F11BP<3:0>				F10BP<3:0>				
bit 15							bit 8		

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
	F9BP<3:0>				F8BP<3:0>				
bit 7							bit 0		

Legend:C = Writable bit, but only '0' can be written to clear the bitR = Readable bitW = Writable bitU = Unimplemented bit, read as '0'-n = Value at POR'1' = Bit is set'0' = Bit is clearedx = Bit is unknown

bit 15-12 F11BP<3:0>: RX Buffer mask for Filter 11 bits

1111 = Filter hits received in RX FIFO buffer

1110 = Filter hits received in RX Buffer 14

•

.

0001 = Filter hits received in RX Buffer 1 0000 = Filter hits received in RX Buffer 0

bit 11-8 **F10BP<3:0>:** RX Buffer mask for Filter 10 bits (same values as bit 15-12) bit 7-4 **F9BP<3:0>:** RX Buffer mask for Filter 9 bits (same values as bit 15-12)

bit 3-0 **F8BP<3:0>:** RX Buffer mask for Filter 8 bits (same values as bit 15-12)

REGISTER 21-15: CIBUFPNT4: ECAN™ FILTER 12-15 BUFFER POINTER REGISTER 4

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
	F15BP	<3:0>		F14BP<3:0>				
bit 15							bit 8	

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
	F13BP<3:0>				F12BP<3:0>				
bit 7							bit 0		

Legend:	C = Writable bit, but o	C = Writable bit, but only '0' can be written to clear the bit					
R = Readable bit	W = Writable bit	U = Unimplemented bit	U = Unimplemented bit, read as '0'				
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown				

bit 15-12 F15BP<3:0>: RX Buffer mask for Filter 15 bits

1111 = Filter hits received in RX FIFO buffer 1110 = Filter hits received in RX Buffer 14

•

•

0001 = Filter hits received in RX Buffer 1 0000 = Filter hits received in RX Buffer 0

bit 11-8 F14BP<3:0>: RX Buffer mask for Filter 14 bits (same values as bit 15-12) bit 7-4 F13BP<3:0>: RX Buffer mask for Filter 13 bits (same values as bit 15-12) bit 3-0 F12BP<3:0>: RX Buffer mask for Filter 12 bits (same values as bit 15-12)

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REGISTER 21-16: CIRXFnSID: ECAN™ ACCEPTANCE FILTER STANDARD IDENTIFIER REGISTER n (n = 0-15)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3
bit 15							bit 8

R/W-x	R/W-x	R/W-x	U-0	R/W-x	U-0	R/W-x	R/W-x
SID2	SID1	SID0	_	EXIDE	_	EID17	EID16
bit 7							bit 0

 Legend:
 C = Writable bit, but only '0' can be written to clear the bit

 R = Readable bit
 W = Writable bit
 U = Unimplemented bit, read as '0'

 -n = Value at POR
 '1' = Bit is set
 '0' = Bit is cleared
 x = Bit is unknown

bit 15-5 SID<10:0>: Standard Identifier bits

1 = Message address bit SIDx must be '1' to match filter 0 = Message address bit SIDx must be '0' to match filter

bit 4 **Unimplemented:** Read as '0'

bit 3 **EXIDE:** Extended Identifier Enable bit

If MIDE = 1:

1 = Match only messages with extended identifier addresses0 = Match only messages with standard identifier addresses

If MIDE = 0:
Ignore EXIDE bit.

bit 2 **Unimplemented:** Read as '0'

bit 1-0 **EID<17:16>:** Extended Identifier bits

1 = Message address bit EIDx must be '1' to match filter 0 = Message address bit EIDx must be '0' to match filter

REGISTER 21-17: CIRXFnEID: ECAN™ ACCEPTANCE FILTER EXTENDED IDENTIFIER REGISTER n (n = 0-15)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID15	EID14	EID13	EID12	EID11	EID10	EID9	EID8
bit 15							bit 8

| R/W-x |
|-------|-------|-------|-------|-------|-------|-------|-------|
| EID7 | EID6 | EID5 | EID4 | EID3 | EID2 | EID1 | EID0 |
| bit 7 | | | | | | | bit 0 |

Legend:	C = Writable bit, but only '0	C = Writable bit, but only '0' can be written to clear the bit					
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'					
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown				

bit 15-0 EID<15:0>: Extended Identifier bits

1 = Message address bit EIDx must be '1' to match filter 0 = Message address bit EIDx must be '0' to match filter

REGISTER 21-18: CIFMSKSEL1: ECAN™ FILTER 7-0 MASK SELECTION REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F7MSk	<<1:0>	F6MSk	<<1:0>	F5MS	K<1:0>	F4MSI	K<1:0>
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
F3MSK	<1:0>	F2MSł	ISK<1:0>		F1MSK<1:0>		F0MSK<1:0>	
bit 7							bit 0	

Legend:	C = Writable bit, but o	only '0' can be written to clear t	he bit
R = Readable bit	W = Writable bit	U = Unimplemented bit	, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14	F7MSK<1:0>: Mask Source for Filter 7 bit
	11 = Reserved
	10 = Acceptance Mask 2 registers contain mask
	01 = Acceptance Mask 1 registers contain mask
	00 = Acceptance Mask 0 registers contain mask
bit 13-12	F6MSK<1:0>: Mask Source for Filter 6 bit (same values as bit 15-14)
bit 11-10	F5MSK<1:0>: Mask Source for Filter 5 bit (same values as bit 15-14)
bit 9-8	F4MSK<1:0>: Mask Source for Filter 4 bit (same values as bit 15-14)
bit 7-6	F3MSK<1:0>: Mask Source for Filter 3 bit (same values as bit 15-14)
bit 5-4	F2MSK<1:0>: Mask Source for Filter 2 bit (same values as bit 15-14)
bit 3-2	F1MSK<1:0>: Mask Source for Filter 1 bit (same values as bit 15-14)
bit 1-0	F0MSK<1:0>: Mask Source for Filter 0 bit (same values as bit 15-14)

REGISTER 21-19: CIFMSKSEL2: ECAN™ FILTER 15-8 MASK SELECTION REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F15MSI	K<1:0>	F14MS	K<1:0>	F13MS	SK<1:0>	F12MS	K<1:0>
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F11MS	K<1:0>	F10MS	K<1:0>	F9MS	SK<1:0>	F8MSI	<<1:0>
bit 7							bit 0

Legend:	C = Writable bit, but o	C = Writable bit, but only '0' can be written to clear the bit						
R = Readable bit	W = Writable bit	U = Unimplemented bit	, read as '0'					
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown					

bit 15-14	F15MSK<1:0>: Mask Source for Filter 15 bit 11 = Reserved
	10 = Acceptance Mask 2 registers contain mask
	01 = Acceptance Mask 1 registers contain mask
	00 = Acceptance Mask 0 registers contain mask
bit 13-12	F14MSK<1:0>: Mask Source for Filter 14 bit (same values as bit 15-14)
bit 11-10	F13MSK<1:0>: Mask Source for Filter 13 bit (same values as bit 15-14)
bit 9-8	F12MSK<1:0>: Mask Source for Filter 12 bit (same values as bit 15-14)
bit 7-6	F11MSK<1:0>: Mask Source for Filter 11 bit (same values as bit 15-14)
bit 5-4	F10MSK<1:0>: Mask Source for Filter 10 bit (same values as bit 15-14)
bit 3-2	F9MSK<1:0>: Mask Source for Filter 9 bit (same values as bit 15-14)
bit 1-0	F8MSK<1:0>: Mask Source for Filter 8 bit (same values as bit 15-14)

REGISTER 21-20: CIRXMnSID: ECAN™ ACCEPTANCE FILTER MASK STANDARD IDENTIFIER REGISTER n (n = 0-2)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3
bit 15							bit 8

R/W-x	R/W-x	R/W-x	U-0	R/W-x	U-0	R/W-x	R/W-x
SID2	SID1	SID0	_	MIDE	_	EID17	EID16
bit 7							bit 0

Legend:C = Writable bit, but only '0' can be written to clear the bitR = Readable bitW = Writable bitU = Unimplemented bit, read as '0'-n = Value at POR'1' = Bit is set'0' = Bit is clearedx = Bit is unknown

bit 15-5 SID<10:0>: Standard Identifier bits

1 = Include bit SIDx in filter comparison0 = Bit SIDx is don't care in filter comparison

bit 4 **Unimplemented:** Read as '0' bit 3 **MIDE:** Identifier Receive Mode bit

1 = Match only message types (standard or extended address) that correspond to EXIDE bit in filter

0 = Match either standard or extended address message if filters match

(i.e., if (Filter SID) = (Message SID) or if (Filter SID/EID) = (Message SID/EID))

bit 2 **Unimplemented:** Read as '0'

bit 1-0 EID<17:16>: Extended Identifier bits

1 = Include bit EIDx in filter comparison

0 = Bit EIDx is don't care in filter comparison

REGISTER 21-21: CIRXMnEID: ECAN™ ACCEPTANCE FILTER MASK EXTENDED IDENTIFIER REGISTER n (n = 0-2)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID15	EID14	EID13	EID12	EID11	EID10	EID9	EID8
bit 15							bit 8

| R/W-x |
|-------|-------|-------|-------|-------|-------|-------|-------|
| EID7 | EID6 | EID5 | EID4 | EID3 | EID2 | EID1 | EID0 |
| bit 7 | | | | | | | bit 0 |

Legend:C = Writable bit, but only '0' can be written to clear the bitR = Readable bitW = Writable bitU = Unimplemented bit, read as '0'-n = Value at POR'1' = Bit is set'0' = Bit is clearedx = Bit is unknown

bit 15-0 **EID<15:0>:** Extended Identifier bits

1 = Include bit EIDx in filter comparison

0 = Bit EIDx is don't care in filter comparison

REGISTER 21-22: CIRXFUL1: ECAN™ RECEIVE BUFFER FULL REGISTER 1

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXFUL15	RXFUL14	RXFUL13	RXFUL12	RXFUL11	RXFUL10	RXFUL9	RXFUL8
bit 15							bit 8

| R/C-0 |
|--------|--------|--------|--------|--------|--------|--------|--------|
| RXFUL7 | RXFUL6 | RXFUL5 | RXFUL4 | RXFUL3 | RXFUL2 | RXFUL1 | RXFUL0 |
| bit 7 | | | | | | | bit 0 |

Legend: C = Writable bit, but only '0' can be written to clear the bit

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 RXFUL<15:0>: Receive Buffer n Full bits

1 = Buffer is full (set by module)

0 = Buffer is empty (cleared by user software)

REGISTER 21-23: CIRXFUL2: ECAN™ RECEIVE BUFFER FULL REGISTER 2

| R/C-0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| RXFUL31 | RXFUL30 | RXFUL29 | RXFUL28 | RXFUL27 | RXFUL26 | RXFUL25 | RXFUL24 |
| bit 15 | | | | | | | bit 8 |

| R/C-0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| RXFUL23 | RXFUL22 | RXFUL21 | RXFUL20 | RXFUL19 | RXFUL18 | RXFUL17 | RXFUL16 |
| bit 7 | | | | | | | bit 0 |

Legend: C = Writable bit, but only '0' can be written to clear the bit

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 RXFUL<31:16>: Receive Buffer n Full bits

1 = Buffer is full (set by module)

0 = Buffer is empty (cleared by user software)

REGISTER 21-24: CIRXOVF1: ECAN™ RECEIVE BUFFER OVERFLOW REGISTER 1

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF9	RXOVF8
bit 15	•	•	•				bit 8

| R/C-0 |
|--------|--------|--------|--------|--------|--------|--------|--------|
| RXOVF7 | RXOVF6 | RXOVF5 | RXOVF4 | RXOVF3 | RXOVF2 | RXOVF1 | RXOVF0 |
| bit 7 | | | | | | | bit 0 |

Legend:C = Writable bit, but only '0' can be written to clear the bitR = Readable bitW = Writable bitU = Unimplemented bit, read as '0'-n = Value at POR'1' = Bit is set'0' = Bit is clearedx = Bit is unknown

bit 15-0 **RXOVF<15:0>:** Receive Buffer n Overflow bits

1 = Module attempted to write to a full buffer (set by module)

0 = No overflow condition (cleared by user software)

REGISTER 21-25: CIRXOVF2: ECAN™ RECEIVE BUFFER OVERFLOW REGISTER 2

| R/C-0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| RXOVF31 | RXOVF30 | RXOVF29 | RXOVF28 | RXOVF27 | RXOVF26 | RXOVF25 | RXOVF24 |
| bit 15 | | | | | | | bit 8 |

| R/C-0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| RXOVF23 | RXOVF22 | RXOVF21 | RXOVF20 | RXOVF19 | RXOVF18 | RXOVF17 | RXOVF16 |
| bit 7 | | | | | | | bit 0 |

Legend:C = Writable bit, but only '0' can be written to clear the bitR = Readable bitW = Writable bitU = Unimplemented bit, read as '0'-n = Value at POR'1' = Bit is set'0' = Bit is clearedx = Bit is unknown

bit 15-0 RXOVF<31:16>: Receive Buffer n Overflow bits

1 = Module attempted to write to a full buffer (set by module)

0 = No overflow condition (cleared by user software)

REGISTER 21-26: CiTRmnCON: ECAN™ Tx/Rx BUFFER m CONTROL REGISTER (m = 0,2,4,6; n = 1,3,5,7)

R/W-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
TXENn	TXABTn	TXLARBn	TXERRn	TXREQn	RTRENn	TXnPRI<1:0>	
bit 15	•	•		•			bit 8

R/W-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
TXENm	TXABTm ⁽¹⁾	TXLARBm ⁽¹⁾	TXERRm ⁽¹⁾	TXREQm	RTRENm	TXmPF	RI<1:0>
bit 7							bit 0

Legend:	C = Writable bit, but o	C = Writable bit, but only '0' can be written to clear the bit					
R = Readable bit	W = Writable bit	U = Unimplemented bit	t, read as '0'				
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown				

bit 15-8	See Definition for Bits 7-0, Controls Buffer n
bit 7	TXENm: TX/RX Buffer Selection bit
	1 = Buffer TRBn is a transmit buffer
	0 = Buffer TRBn is a receive buffer
bit 6	TXABTm: Message Aborted bit ⁽¹⁾
	1 = Message was aborted
	0 = Message completed transmission successfully
bit 5	TXLARBm: Message Lost Arbitration bit ⁽¹⁾
	1 = Message lost arbitration while being sent
	0 = Message did not lose arbitration while being sent
bit 4	TXERRm: Error Detected During Transmission bit ⁽¹⁾
	1 = A bus error occurred while the message was being sent
	0 = A bus error did not occur while the message was being sent
bit 3	TXREQm: Message Send Request bit
	1 = Requests that a message be sent. The bit automatically clears when the message is successfully sent.
	0 = Clearing the bit to '0' while set requests a message abort.
bit 2	RTRENm: Auto-Remote Transmit Enable bit
	1 = When a remote transmit is received, TXREQ will be set
	0 = When a remote transmit is received, TXREQ will be unaffected
bit 1-0	TXmPRI<1:0>: Message Transmission Priority bits
	11 = Highest message priority

Note 1: This bit is cleared when TXREQ is set.

10 = High intermediate message priority01 = Low intermediate message priority

00 = Lowest message priority

Note: The buffers, SID, EID, DLC, Data Field and Receive Status registers are located in DMA RAM.

21.5 ECAN Message Buffers

ECAN Message Buffers are part of RAM Memory. They are not ECAN Special Function Registers. The user application must directly write into the RAM area that is configured for ECAN Message Buffers. The location and size of the buffer area is defined by the user application.

BUFFER 21-1: ECAN™ MESSAGE BUFFER WORD 0

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
_	_	_	SID10	SID9	SID8	SID7	SID6
bit 15							bit 8

| R/W-x |
|-------|-------|-------|-------|-------|-------|-------|-------|
| SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | SRR | IDE |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-13 Unimplemented: Read as '0'
bit 12-2 SID<10:0>: Standard Identifier bits
bit 1 SRR: Substitute Remote Request bit

When TXIDE = 0:

1 = Message will request remote transmission

0 = Normal messageWhen TXIDE = 1:

The SRR bit must be set to '1'

bit 0 **IDE:** Extended Identifier bit

1 = Message will transmit extended identifier0 = Message will transmit standard identifier

BUFFER 21-2: ECAN™ MESSAGE BUFFER WORD 1

U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x
_	_	_		EID17	EID16	EID15	EID14
bit 15							bit 8

| R/W-x |
|-------|-------|-------|-------|-------|-------|-------|-------|
| EID13 | EID12 | EID11 | EID10 | EID9 | EID8 | EID7 | EID6 |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-12 **Unimplemented:** Read as '0' bit 11-0 **EID<17:6>:** Extended Identifier bits

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BUFFER 21-3: ECAN™ MESSAGE BUFFER WORD 2

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID5	EID4	EID3	EID2	EID1	EID0	RTR	RB1
bit 15							bit 8

U-x	U-x	U-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
_	_	_	RB0	DLC3	DLC2	DLC1	DLC0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-10 **EID<5:0>:** Extended Identifier bits bit 9 **RTR:** Remote Transmission Request bit

When TXIDE = 1:

1 = Message will request remote transmission

0 = Normal message
When TXIDE = 0:
The RTR bit is ignored.

bit 8 RB1: Reserved Bit 1

User must set this bit to '0' per CAN protocol.

bit 7-5 **Unimplemented:** Read as '0'

bit 4 RB0: Reserved Bit 0

User must set this bit to '0' per CAN protocol.

bit 3-0 **DLC<3:0>:** Data Length Code bits

BUFFER 21-4: ECAN™ MESSAGE BUFFER WORD 3

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x			
	Byte 1									
bit 15							bit 8			

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x		
Byte 0									
bit 7							bit 0		

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-8 **Byte 1<15:8>:** ECAN™ Message byte 0 bit 7-0 **Byte 0<7:0>:** ECAN Message byte 1

BUFFER 21-5: ECAN™ MESSAGE BUFFER WORD 4

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x			
	Byte 3									
bit 15							bit 8			

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x			
	Byte 2									
bit 7							bit 0			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-8 **Byte 3<15:8>:** ECAN™ Message byte 3 bit 7-0 **Byte 2<7:0>:** ECAN Message byte 2

BUFFER 21-6: ECAN™ MESSAGE BUFFER WORD 5

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x		
Byte 5									
bit 15							bit 8		

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x			
	Byte 4									
bit 7							bit 0			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-8 **Byte 5<15:8>:** ECAN™ Message byte 5 bit 7-0 **Byte 4<7:0>:** ECAN Message byte 4

BUFFER 21-7: ECAN™ MESSAGE BUFFER WORD 6

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x			
	Byte 7									
bit 15							bit 8			

| R/W-x |
|-------|-------|-------|-------|-------|-------|-------|-------|
| | | | Byt | e 6 | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-8 **Byte 7<15:8>:** ECAN™ Message byte 7 bit 7-0 **Byte 6<7:0>:** ECAN Message byte 6

BUFFER 21-8: ECAN™ MESSAGE BUFFER WORD 7

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
_	_	_			FILHIT<4:0> ⁽¹)	
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	_	_	_	_	_	_	_
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0' bit 12-8 **FILHIT<4:0>:** Filter Hit Code bits⁽¹⁾

Encodes number of filter that resulted in writing this buffer.

bit 7-0 **Unimplemented:** Read as '0'

Note 1: Only written by module for receive buffers, unused for transmit buffers.

22.0 CHARGE TIME MEASUREMENT UNIT (CTMU)

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 33. "Charge Time Measurement Unit (CTMU)" (DS70661) in the "dsPIC33E/PIC24E Family Reference Manual", which is available on the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

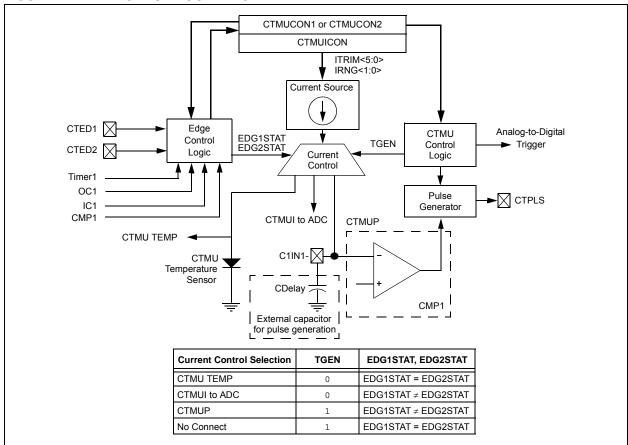
The Charge Time Measurement Unit is a flexible analog module that provides accurate differential time measurement between pulse sources, as well as asynchronous pulse generation. Its key features include:

- · Four edge input trigger sources
- · Polarity control for each edge source
- · Control of edge sequence
- · Control of response to edges
- · Precise time measurement resolution of 1 ns
- Accurate current source suitable for capacitive measurement
- On-chip temperature measurement using a built-in diode

Together with other on-chip analog modules, the CTMU can be used to precisely measure time, measure capacitance, measure relative changes in capacitance or generate output pulses that are independent of the system clock.

The CTMU module is ideal for interfacing with capacitive-based sensors. The CTMU is controlled through two registers: CTMUCON and CTMUICON. CTMUCON enables the module and controls edge source selection, edge source polarity selection and edge sequencing. The CTMUICON register controls the selection and trim of the current source.





22.1 CTMU Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter

this URL in your browser:

http://www.microchip.com/wwwprod-

ucts/Devices.aspx?dDoc-

Name=en555464

22.1.1 KEY RESOURCES

- Section 33. "Charge Time Measurement Unit (CTMU)" (DS70661)
- · Code Samples
- · Application Notes
- · Software Libraries
- · Webinars
- All related dsPIC33E/PIC24E Family Reference Manuals Sections
- · Development Tools

22.2 CTMU Control Registers

CTMUCON1: CTMU CONTROL REGISTER 1 **REGISTER 22-1:**

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CTMUEN	_	CTMUSIDL	TGEN	EDGEN	EDGSEQEN	IDISSEN ⁽¹⁾	CTTRIG
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	_	_	_	_	_	_	_
bit 7							bit 0

Legend:

R = Readable bit U = Unimplemented bit, read as '0' W = Writable bit

'0' = Bit is cleared -n = Value at POR '1' = Bit is set x = Bit is unknown

bit 15 CTMUEN: CTMU Enable bit

1 = Module is enabled

0 = Module is disabled

bit 14 Unimplemented: Read as '0'

bit 13 CTMUSIDL: Stop in Idle Mode bit

1 = Discontinue module operation when device enters Idle mode

0 = Continue module operation in Idle mode

bit 12 **TGEN:** Time Generation Enable bit

1 = Enables edge delay generation

0 = Disables edge delay generation

bit 11 EDGEN: Edge Enable bit

1 = Hardware modules are used to trigger edges (TMRx, CTEDx, etc.)

0 = Software is used to trigger edges (manual set of EDGxSTAT)

bit 10 **EDGSEQEN:** Edge Sequence Enable bit

1 = Edge 1 event must occur before Edge 2 event can occur

0 = No edge sequence is needed

bit 9 **IDISSEN:** Analog Current Source Control bit⁽¹⁾

1 = Analog current source output is grounded

0 = Analog current source output is not grounded

bit 8 CTTRIG: ADC Trigger Control bit

1 = CTMU triggers ADC start of conversion

0 = CTMU does not trigger ADC start of conversion

bit 7-0 Unimplemented: Read as '0'

The ADC module Sample and Hold capacitor is not automatically discharged between sample/conversion Note 1: cycles. Software using the ADC as part of a capacitance measurement, must discharge the ADC capacitor before conducting the measurement. The IDISSEN bit, when set to '1', performs this function. The ADC must be sampling while the IDISSEN bit is active to connect the discharge sink to the capacitor array.

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REGISTER 22-2: CTMUCON2: CTMU CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EDG1MOD	EDG1POL		EDG1SEL<3:0>				EDG1STAT
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
EDG2MOD	EDG2POL		EDG2SEL<3:0>				_
bit 7		bit 0					

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15 **EDG1MOD:** Edge 1 Edge Sampling Mode Selection bit

1 = Edge 1 is edge sensitive 0 = Edge 1 is level sensitive

bit 14 EDG1POL: Edge 1 Polarity Select bit

1 = Edge 1 programmed for a positive edge response 0 = Edge 1 programmed for a negative edge response

bit 13-10 EDG1SEL<3:0>: Edge 1 Source Select bits

1xxx = Reserved 01xx = Reserved 0011 = CTED1 pin 0010 = CTED2 pin 0001 = OC1 module 0000 = Timer1 module

bit 9 EDG2STAT: Edge 2 Status bit

Indicates the status of Edge 2 and can be written to control the edge source.

1 = Edge 2 has occurred 0 = Edge 2 has not occurred

bit 8 EDG1STAT: Edge 1 Status bit

Indicates the status of Edge 1 and can be written to control the edge source.

1 = Edge 1 has occurred 0 = Edge 1 has not occurred

bit 7 EDG2MOD: Edge 2 Edge Sampling Mode Selection bit

1 = Edge 2 is edge sensitive0 = Edge 2 is level sensitive

bit 6 EDG2POL: Edge 2 Polarity Select bit

1 = Edge 2 programmed for a positive edge response 0 = Edge 2 programmed for a negative edge response

bit 5-2 EDG2SEL<3:0>: Edge 2 Source Select bits

1111 = Reserved 01xx = Reserved 0100 = CMP1 module 0011 = CTED2 pin 0010 = CTED1 pin 0001 = OC1 module 0000 = IC1 module

bit 1-0 **Unimplemented:** Read as '0'

CTMUICON: CTMU CURRENT CONTROL REGISTER REGISTER 22-3:

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ITRIM<5:0>							<1:0>
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	_	_	_	_	_	_	_
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-10 ITRIM<5:0>: Current Source Trim bits

011111 = Maximum positive change from nominal current +62%

011110 = Maximum positive change from nominal current +60%

000010 = Minimum positive change from nominal current +4%

000001 = Minimum positive change from nominal current +2%

000000 = Nominal current output specified by IRNG<1:0>

111111 = Minimum negative change from nominal current -2%

111110 = Minimum negative change from nominal current -4%

100010 = Maximum negative change from nominal current -60% 100001 = Maximum negative change from nominal current -62%

bit 9-8 IRNG<1:0>: Current Source Range Select bits

11 = 100 × Base Current(2)

 $10 = 10 \times Base Current^{(2)}$

01 = Base Current Level(2)

00 = 1000 × Base Current^(1,2)

bit 7-0 Unimplemented: Read as '0'

Note 1: This current range is not available to be used with the internal temperature measurement diode.

2: Refer to the CTMU Current Source Specifications (Table 30-55) in Section 30.0 "Electrical Characteristics" for the current range selection values.

23.0 10-BIT/12-BIT ANALOG-TO-DIGITAL CONVERTER (ADC)

Note 1: This data sheet summarizes the features the dsPIC33EPXXXGP50X. dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 16. "Analog-to-Digital Converter (ADC)" (DS70621) of the "dsPIC33E/PIC24E Family Reference Manual', which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X devices have one ADC module. The ADC module supports up to 16 analog input channels.

On ADC1, the AD12B bit (AD1CON1<10>) allows each of the ADC modules to be configured by the user as either a 10-bit, 4-sample/hold ADC (default configuration) or a 12-bit, 1-sample/hold ADC.

Note: The ADC module needs to be disabled before modifying the AD12B bit.

23.1 Key Features

The 10-bit ADC configuration has the following key features:

- Successive Approximation (SAR) conversion
- · Conversion speeds of up to 1.1 Msps
- · Up to 16 analog input pins
- · External voltage reference input pins
- Simultaneous sampling of up to four analog input pins
- · Automatic Channel Scan mode
- · Selectable conversion trigger source
- · Selectable Buffer Fill modes
- Four result alignment options (signed/unsigned, fractional/integer)
- · Operation during CPU Sleep and Idle modes

The 12-bit ADC configuration supports all the above features, except:

- In the 12-bit configuration, conversion speeds of up to 500 ksps are supported
- There is only one sample/hold amplifier in the 12-bit configuration, so simultaneous sampling of multiple channels is not supported.

Depending on the particular device pinout, the ADC can have up to 16 analog input pins, designated AN0 through AN15. In addition, there are two analog input pins for external voltage reference connections. These voltage reference inputs can be shared with other analog input pins. The actual number of analog input pins and external voltage reference input configuration depends on the specific device.

A block diagram of the ADC module is shown in Figure 23-1. Figure 23-2 provides a diagram of the ADC conversion clock period.

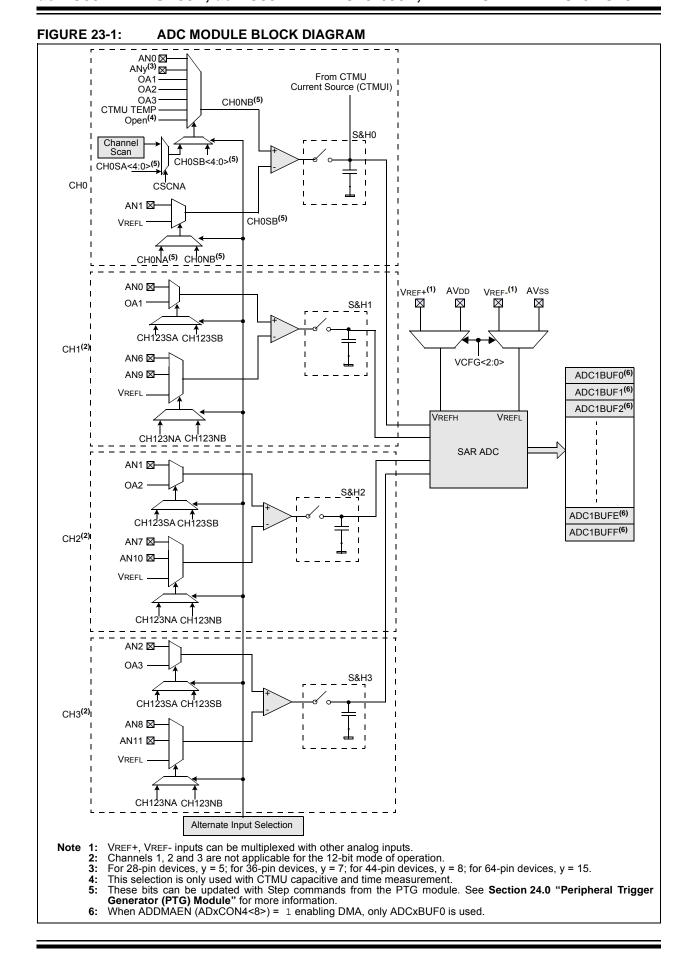
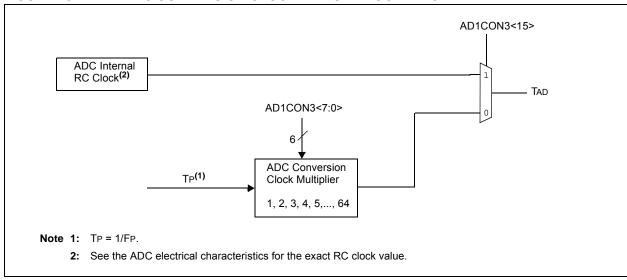


FIGURE 23-2: ADC CONVERSION CLOCK PERIOD BLOCK DIAGRAM



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23.2 ADC Helpful Tips

- 1. The SMPI control bits in the ADxCON2 registers:
 - Determine when the ADC interrupt flag is set and an interrupt is generated, if enabled.
 - b) When the CSCNA bit in the ADxCON2 registers is set to '1', this determines when the ADC analog scan channel list defined in the AD1CSSL/AD1CSSH registers starts over from the beginning.
 - c) When the DMA peripheral is not used (ADDMAEN = 0), this determines when the ADC result buffer pointer to ADC1BUF0-ADC1BUFF, gets reset back to the beginning at ADC1BUF0.
 - d) When the DMA peripheral is used (ADDMAEN = 1), this determines when the DMA address pointer is incremented after a sample/conversion operation. ADC1BUF0 is the only ADC buffer used in this mode. The ADC result buffer pointer to ADC1BUF0-ADC1BUFF gets reset back to the beginning at ADC1BUF0. The DMA address is incremented after completion of every 32nd sample/conversion operation. Conversion results are stored in the ADC1BUF0 register for transfer to RAM using DMA.
- 2. When the DMA module is disabled (ADDMAEN = 0), the ADC has 16 result buffers. ADC conversion results are stored sequentially in ADC1BUF0-ADC1BUFF regardless of which analog inputs are being used subject to the SMPI bits and the condition described in 1c above. There is no relationship between the ANx input being measured and which ADC buffer (ADC1BUF0-ADC1BUFF) that the conversion results will be placed in.
- 3. When the DMA module is enabled (ADDMAEN = 1), the ADC module has only 1 ADC result buffer, (i.e., ADC1BUF0), per ADC peripheral and the ADC conversion result must be read either by the CPU or DMA controller before the next ADC conversion is complete to avoid overwriting the previous value.
- 4. The DONE bit (ADxCON1<0>) is only cleared at the start of each conversion and is set at the completion of the conversion, but remains set indefinitely even through the next sample phase until the next conversion begins. If application code is monitoring the DONE bit in any kind of software loop, the user must consider this behavior because the CPU code execution is faster than the ADC. As a result, in manual sample mode, particularly where the users code is setting the SAMP bit (ADxCON1<1>), the DONE bit should also be cleared by the user application just before setting the SAMP bit.

23.3 ADC Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:

In the event you are not able to access the product page using the link above, enter this URL in your browser:

http://www.microchip.com/wwwproducts/ Devices.aspx?dDocName=en555464

23.3.1 KEY RESOURCES

- Section 4. "Analog-to-Digital Converter (ADC)" (DS70621)
- · Code Samples
- · Application Notes
- · Software Libraries
- Webinars
- All related dsPIC33E/PIC24E Family Reference Manuals Sections
- · Development Tools

23.4 ADC Control Registers

REGISTER 23-1: AD1CON1: ADC1 CONTROL REGISTER 1

R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
ADON	_	ADSIDL	ADDMABM	_	AD12B	FORM	l<1:0>
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/C-0
						HC,HS	HC, HS
	SSRC<2:0>		SSRCG	SIMSAM	ASAM	SAMP	DONE ⁽³⁾
bit 7							bit 0

Legend: HC = Cleared by hardware		HS = Set by hardware		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 15 ADON: ADC Operating Mode bit

1 = ADC module is operating

0 = ADC is off

bit 14 **Unimplemented:** Read as '0'

bit 13 ADSIDL: Stop in Idle Mode bit

1 = Discontinue module operation when device enters Idle mode

0 = Continue module operation in Idle mode

bit 12 ADDMABM: DMA Buffer Build Mode bit

1 = DMA buffers are written in the order of conversion. The module provides an address to the DMA channel that is the same as the address used for the non-DMA stand-alone buffer.

0 = DMA buffers are written in Scatter/Gather mode. The module provides a Scatter/Gather address to the DMA channel, based on the index of the analog input and the size of the DMA buffer.

bit 11 **Unimplemented:** Read as '0'

bit 10 AD12B: 10-bit or 12-bit Operation Mode bit

1 = 12-bit, 1-channel ADC operation 0 = 10-bit, 4-channel ADC operation

bit 9-8 **FORM<1:0>:** Data Output Format bits

For 10-bit operation:

11 = Signed fractional (Dout = sddd dddd dd00 0000, where s = .NOT.d<9>)

10 = Fractional (Dout = dddd dddd dd00 0000)

01 = Signed integer (Dout = ssss sssd dddd dddd, where s = .NOT.d<9>)

00 = Integer (Dout = 0000 00dd dddd dddd)

For 12-bit operation:

11 = Signed fractional (Dout = sddd dddd dddd 0000, where s = .NOT.d<11>)

10 = Fractional (Dout = dddd dddd dddd 0000)

01 = Signed Integer (Dout = ssss sddd dddd, where s = .NOT.d<11>)

00 = Integer (Dout = 0000 dddd dddd dddd)

Note 1: See Section 24.0 "Peripheral Trigger Generator (PTG) Module" for information on this selection.

2: This setting is available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

3: Do not clear the DONE bit in software if Auto-Sample is enabled (ASAM = 1).

REGISTER 23-1: AD1CON1: ADC1 CONTROL REGISTER 1 (CONTINUED)

bit 7-5 SSRC<2:0>: Sample Clock Source Select bits

If SSRCG = 1:

- 111 = Reserved
- 110 = PTGO15 primary trigger compare ends sampling and starts conversion⁽¹⁾
- 101 = PTGO14 primary trigger compare ends sampling and starts conversion⁽¹⁾
- 100 = PTGO13 primary trigger compare ends sampling and starts conversion⁽¹⁾
- 011 = PTGO12 primary trigger compare ends sampling and starts conversion⁽¹⁾
- 010 = PWM Generator 3 primary trigger compare ends sampling and starts conversion⁽²⁾
- 001 = PWM Generator 2 primary trigger compare ends sampling and starts conversion⁽²⁾
- 000 = PWM Generator 1 primary trigger compare ends sampling and starts conversion⁽²⁾

If SSRCG = 0:

- 111 = Internal counter ends sampling and starts conversion (auto-convert)
- 110 = CTMU ends sampling and starts conversion
- 101 = Reserved
- 100 = Timer5 compare ends sampling and starts conversion
- 011 = PWM primary Special Event Trigger ends sampling and starts conversion (2)
- 010 = Timer3 compare ends sampling and starts conversion
- 001 = Active transition on the INTO pin ends sampling and starts conversion
- 000 = Clearing the Sample bit (SAMP) ends sampling and starts conversion (Manual mode)
- bit 4 SSRCG: Sample Clock Source Group bit

See SSRC<2:0> for details.

bit 3 SIMSAM: Simultaneous Sample Select bit (only applicable when CHPS<1:0> = 01 or 1x)

When AD12B = 1, SIMSAM is: U-0, Unimplemented, Read as '0'

- 1 = Samples CH0, CH1, CH2, CH3 simultaneously (when CHPS<1:0> = 1x); or Samples CH0 and CH1 simultaneously (when CHPS<1:0> = 01)
- 0 = Samples multiple channels individually in sequence
- bit 2 ASAM: ADC Sample Auto-Start bit
 - 1 = Sampling begins immediately after last conversion. SAMP bit is auto-set.
 - 0 = Sampling begins when SAMP bit is set
- bit 1 SAMP: ADC Sample Enable bit
 - 1 = ADC Sample/Hold amplifiers are sampling
 - 0 = ADC Sample/Hold amplifiers are holding
 - If ASAM = 0, software can write '1' to begin sampling. Automatically set by hardware if ASAM = 1.
 - If SSRC = 000, software can write '0' to end sampling and start conversion. If SSRC \neq 000,

automatically cleared by hardware to end sampling and start conversion.

- bit 0 **DONE:** ADC Conversion Status bit⁽³⁾
 - 1 = ADC conversion cycle is completed.
 - 0 = ADC conversion not started or in progress

Automatically set by hardware when A/D conversion is complete. Software can write '0' to clear DONE status (software not allowed to write '1'). Clearing this bit does NOT affect any operation in progress. Automatically cleared by hardware at start of a new conversion.

- Note 1: See Section 24.0 "Peripheral Trigger Generator (PTG) Module" for information on this selection.
 - 2: This setting is available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.
 - **3:** Do not clear the DONE bit in software if Auto-Sample is enabled (ASAM = 1).

REGISTER 23-2: AD1CON2: ADC1 CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	VCFG<2:0>		_	_	CSCNA	CHPS	<1:0>
bit 15							bit 8

R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BUFS			SMPI<4:0>			BUFM	ALTS
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-13 VCFG<2:0>: Converter Voltage Reference Configuration bits

	VREFH	VREFL
000	Avdd	Avss
001	External VREF+	Avss
010	AVDD	External VREF-
011	External VREF+	External VREF-
1xx	AVDD	Avss

bit 12-11 **Unimplemented:** Read as '0'

bit 10 CSCNA: Input Scan Select bit

1 = Scan inputs for CH0+ during Sample A bit

0 = Do not scan inputs

bit 9-8 CHPS<1:0>: Channel Select bits

When AD12B = 1, CHPS<1:0> is: U-0, Unimplemented, Read as '0'

1x = Converts CH0, CH1, CH2 and CH3

01 = Converts CH0 and CH1

00 = Converts CH0

bit 7 **BUFS:** Buffer Fill Status bit (only valid when BUFM = 1)

- 1 = ADC is currently filling the second half of the buffer. The user application should access data in the first half of the buffer
- 0 = ADC is currently filling the first half of the buffer. The user application should access data in the second half of the buffer.

bit 6-2 **SMPI<4:0>:** Increment Rate bits

When ADDMAEN = 0:

x1111 = Generates interrupt after completion of every 16th sample/conversion operation

x1110 = Generates interrupt after completion of every 15th sample/conversion operation

.

x0001 = Generates interrupt after completion of every 2nd sample/conversion operation

x0000 = Generates interrupt after completion of every sample/conversion operation

When ADDMAEN = 1:

11111 = Increments the DMA address after completion of every 32nd sample/conversion operation 11110 = Increments the DMA address after completion of every 31st sample/conversion operation

•

00001 = Increments the DMA address after completion of every 2nd sample/conversion operation 00000 = Increments the DMA address after completion of every sample/conversion operation

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REGISTER 23-2: AD1CON2: ADC1 CONTROL REGISTER 2 (CONTINUED)

bit 1 **BUFM:** Buffer Fill Mode Select bit

1 = Starts buffer filling the first half of the buffer on the first interrupt and the second half of the buffer on next interrupt

0 = Always starts filling the buffer from the start address.

bit 0 ALTS: Alternate Input Sample Mode Select bit

1 = Uses channel input selects for Sample A on first sample and Sample B on next sample

0 = Always uses channel input selects for Sample A

REGISTER 23-3: AD1CON3: ADC1 CONTROL REGISTER 3

R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADRC	_	_			SAMC<4:0>(1)		
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			ADCS<	7:0> ⁽²⁾			
bit 7							bit 0

Legend:

R = Readable bit U = Unimplemented bit, read as '0' W = Writable bit

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15 ADRC: ADC Conversion Clock Source bit

1 = ADC Internal RC Clock

0 = Clock Derived From System Clock

Unimplemented: Read as '0' bit 14-13

SAMC<4:0>: Auto Sample Time bits⁽¹⁾ bit 12-8

11111 = 31 TAD

00001 = 1 TAD

00000 = 0 TAD

ADCS<7:0>: ADC Conversion Clock Select bits(2) bit 7-0

111111111 = $TP \cdot (ADCS < 7:0 > + 1) = TP \cdot 256 = TAD$

 $00000010 = \text{TP} \cdot (\text{ADCS} < 7:0 > + 1) = \text{TP} \cdot 3 = \text{TAD}$

 $00000001 = TP \cdot (ADCS < 7:0 > + 1) = TP \cdot 2 = TAD$

 $00000000 = \text{TP} \cdot (\text{ADCS} < 7:0 > + 1) = \text{TP} \cdot 1 = \text{TAD}$

Note 1: This bit is only used if AD1CON1<7:5> (SSRC<2:0>) = 111 and AD1CON1<4> (SSRCG) = 0.

2: This bit is not used if AD1CON3<15> (ADRC) = 1.

REGISTER 23-4: AD1CON4: ADC1 CONTROL REGISTER 4

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
_	_	_	_	_	_	_	ADDMAEN
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
_	_	_	_			DMABL<2:0>	
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0' bit 8 **ADDMAEN:** ADC DMA Enable bit

1 = Conversion results stored in ADC1BUF0 register, for transfer to RAM using DMA

0 = Conversion results stored in ADC1BUF0 through ADC1BUFF registers; DMA will not be used

bit 7-3 **Unimplemented:** Read as '0'

bit 2-0 DMABL<2:0>: Selects Number of DMA Buffer Locations per Analog Input bits

111 = Allocates 128 words of buffer to each analog input

110 = Allocates 64 words of buffer to each analog input

101 = Allocates 32 words of buffer to each analog input 100 = Allocates 16 words of buffer to each analog input

011 = Allocates 8 words of buffer to each analog input

010 = Allocates 4 words of buffer to each analog input

001 = Allocates 2 words of buffer to each analog input

000 = Allocates 1 word of buffer to each analog input

REGISTER 23-5: AD1CHS123: ADC1 INPUT CHANNEL 1, 2, 3 SELECT REGISTER

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
_	_	_	_	_	CH123N	IB<1:0>	CH123SB
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
_	_	_	_	_	CH123N	IA<1:0>	CH123SA
bit 7							bit 0

Legend	d:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-11 **Unimplemented:** Read as '0'

bit 10-9 CH123NB<1:0>: Channel 1, 2, 3 Negative Input Select for Sample B bits

When AD12B = 1, CHxNB is: U-0, Unimplemented, Read as '0'

11 = CH1 negative input is AN9, CH2 negative input is AN10, CH3 negative input is AN11 10 = CH1 negative input is AN6, CH2 negative input is AN7, CH3 negative input is AN8

0x = CH1, CH2, CH3 negative input is VREFL

bit 8 CH123SB: Channel 1, 2, 3 Positive Input Select for Sample B bit

When AD12B = 1, CHxSA is: U-0, Unimplemented, Read as '0'

1 = CH1 positive input is OA1, CH2 positive input is OA2, CH3 positive input is OA3 0 = CH1 positive input is AN0, CH2 positive input is AN1, CH3 positive input is AN2

bit 7-3 **Unimplemented:** Read as '0'

bit 2-1 CH123NA<1:0>: Channel 1, 2, 3 Negative Input Select for Sample A bits

When AD12B = 1, CHxNA is: U-0, Unimplemented, Read as '0'

11 = CH1 negative input is AN9, CH2 negative input is AN10, CH3 negative input is AN11 10 = CH1 negative input is AN6, CH2 negative input is AN7, CH3 negative input is AN8

0x = CH1, CH2, CH3 negative input is VREFL

bit 0 CH123SA: Channel 1, 2, 3 Positive Input Select for Sample A bit

When AD12B = 1, CHxSA is: U-0, Unimplemented, Read as '0'

1 = CH1 positive input is OA1, CH2 positive input is OA2, CH3 positive input is OA3 0 = CH1 positive input is AN0, CH2 positive input is AN1, CH3 positive input is AN2

REGISTER 23-6: AD1CHS0: ADC1 INPUT CHANNEL 0 SELECT REGISTER

R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH0NB	_	_			CH0SB<4:0>		
bit 15							bit 8

R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH0NA	_	_			CH0SA<4:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	t, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 CHONB: Channel 0 Negative Input Select for Sample B bit 1 = Channel 0 negative input is AN1 0 = Channel 0 negative input is VREFL bit 14-13 Unimplemented: Read as '0' bit 12-8 CH0SB<4:0>: Channel 0 Positive Input Select for Sample B bits 11111 = Open; use this selection with CTMU capacitive and time measurement 11110 = Channel 0 positive input is connected to CTMU temperature measurement diode (CTMU TEMP) 11101 = Reserved 11100 = Reserved 11011 = Reserved 11010 = Channel 0 positive input is output of CMP3 11001 = Channel 0 positive input is output of CMP2 11000 = Channel 0 positive input is output of CMP1 10110 = Reserved 10000 = Reserved 01111 = Channel 0 positive input is AN15⁽¹⁾ 01110 = Channel 0 positive input is AN14⁽¹⁾ 01101 = Channel 0 positive input is AN13⁽¹⁾ 00010 = Channel 0 positive input is AN2⁽¹⁾ 00001 = Channel 0 positive input is AN1⁽¹⁾ 00000 = Channel 0 positive input is ANO(1) bit 7 CHONA: Channel 0 Negative Input Select for Sample A bit

Note 1: See the "Pin Diagrams" section for the available analog channels for each device.

1 = Channel 0 negative input is AN10 = Channel 0 negative input is VREFL

Unimplemented: Read as '0'

bit 6-5

REGISTER 23-6: AD1CHS0: ADC1 INPUT CHANNEL 0 SELECT REGISTER

```
bit 4-0
                CH0SA<4:0>: Channel 0 Positive Input Select for Sample A bits
                11111 = Open; use this selection with CTMU capacitive and time measurement
                11110 = Channel 0 positive input is connected to CTMU temperature measurement diode
                         (CTMU TEMP)
                11101 = Reserved
                11100 = Reserved
                11011 = Reserved
                11010 = Channel 0 positive input is output of CMP3
                11001 = Channel 0 positive input is output of CMP2
                11000 = Channel 0 positive input is output of CMP1
                10110 = Reserved
                10000 = Reserved
                01111 = Channel 0 positive input is AN15<sup>(1)</sup>
                01110 = Channel 0 positive input is AN14<sup>(1)</sup>
                01101 = Channel 0 positive input is AN13(1)
                00010 = Channel 0 positive input is AN2<sup>(1)</sup>
                00001 = Channel 0 positive input is AN1(1)
                00000 = Channel 0 positive input is ANO<sup>(1)</sup>
```

Note 1: See the "Pin Diagrams" section for the available analog channels for each device.

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REGISTER 23-7: AD1CSSH: ADC1 INPUT SCAN SELECT REGISTER HIGH⁽¹⁾

R/W-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
CSS31	CSS30	_	_	_	CSS26	CSS25	CSS24
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	_	_	_	_	_	_	_
bit 7							bit 0

I ea	end:
	viiu.

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15 CSS31: ADC Input Scan Selection bits

1 = Select CTMU capacitive and time measurement for input scan (Open)0 = Skip CTMU capacitive and time measurement for input scan (Open)

bit 14 CSS30: ADC Input Scan Selection bits

1 = Select CTMU on-chip temperature measurement for input scan (CTMU TEMP)
 0 = Skip CTMU on-chip temperature measurement for input scan (CTMU TEMP)

bit 13-11 **Unimplemented:** Read as '0'

bit 10 CSS26: ADC Input Scan Selection bits

1 = Select CMP3 for input scan 0 = Skip CMP3 for input scan

bit 9 CSS25: ADC Input Scan Selection bits

1 = Select CMP2 for input scan0 = Skip CMP2 for input scan

bit 8 CSS24: ADC Input Scan Selection bits

1 = Select CMP1 for input scan 0 = Skip CMP1 for input scan

bit 7-0 **Unimplemented:** Read as '0'

Note 1: All ADxCSSH bits can be selected by user software. However, inputs selected for scan without a corresponding input on device convert VREFL.

REGISTER 23-8: AD1CSSL: ADC1 INPUT SCAN SELECT REGISTER LOW^(1,2)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CSS15	CSS14	CSS13	CSS12	CSS11	CSS10	CSS9	CSS8
bit 15							bit 8

| R/W-0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| CSS7 | CSS6 | CSS5 | CSS4 | CSS3 | CSS2 | CSS1 | CSS0 |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 CSS<15:0>: ADC Input Scan Selection bits

1 = Select ANx for input scan0 = Skip ANx for input scan

Note 1: On devices with less than 16 analog inputs, all AD1CSSL bits can be selected by the user. However, inputs selected for scan without a corresponding input on device convert VREFL.

2: CSSx = ANx, where x = 0-15.

24.0 PERIPHERAL TRIGGER GENERATOR (PTG) MODULE

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Section 32. Peripheral Trigger Generator (PTG)" (DS70669) of the "dsPIC33E/PIC24E Family Reference Manual", which is available from the Microchip web site (www.microchip.com).

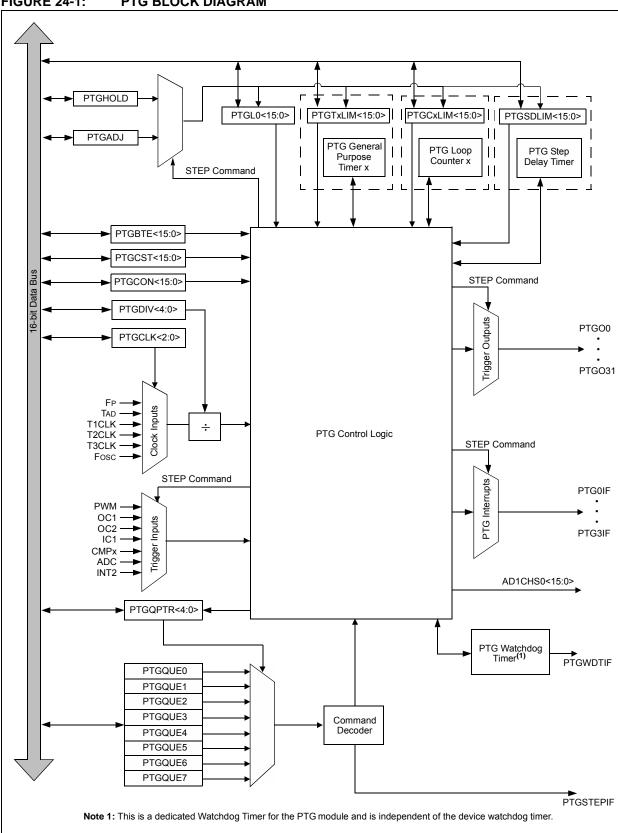
2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

24.1 Module Introduction

The Peripheral Trigger Generator (PTG) provides a means to schedule complex high-speed peripheral operations that would be difficult to achieve using software. The PTG module uses 8-bit commands called "steps" that the user writes to the PTG Queue register (PTGQUE0-PTQUE7), which performs operations such as wait for input signal, generate output trigger, and wait for timer.

The PTG module has the following major features:

- · Multiple clock sources
- Two 16-bit general purpose timers
- · Two 16-bit general limit counters
- · Configurable for rising or falling edge triggering
- · Generates processor interrupts to include:
 - Four configurable processor interrupts
 - Interrupt on a step event in Single-Step mode
 - Interrupt on a PTG Watchdog Timer time-out
- Able to receive trigger signals from these peripherals:
 - ADC
 - PWM
 - Output Compare
 - Input Capture
 - Op amp/Comparator
 - INT2
- Able to trigger or synchronize to these peripherals:
 - Watchdog Timer
 - Output Compare
 - Input Capture
- ADC
- PWM
- Op amp/Comparator



24.2 PTG Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter

this URL in your browser:

http://www.microchip.com/wwwproducts/ Devices.aspx?dDocName=en555464

24.2.1 KEY RESOURCES

- Section 32. "Peripheral Trigger Generator" (DS70669)
- · Code Samples
- · Application Notes
- · Software Libraries
- Webinars
- All related dsPIC33E/PIC24E Family Reference Manuals Sections
- · Development Tools

24.3 **PTG Control Registers**

PTGCST: PTG CONTROL/STATUS REGISTER REGISTER 24-1:

R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
PTGEN	_	PTGSIDL	PTGTOGL	_	PTGSWT ⁽²⁾	PTGSSEN	PTGIVIS
bit 15							bit 8

R/W-0	HS-0	U-0	U-0	U-0	U-0	R/W-0
PTGSTRT	PTGWDTO	_	_	_	_	PTGITM<1:0> ⁽¹⁾
bit 7						bit 0

Legend:		HS = Set by Hardware	HS = Set by Hardware			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'				
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown			

bit 15 PTGEN: Module Enable bit

1 = PTG module is enabled

0 = PTG module is disabled

bit 14 Unimplemented: Read as '0' bit 13

PTGSIDL: Stop in Idle Mode bit

1 = Discontinue module operation when device enters Idle mode

0 = Continue module operation in Idle mode

bit 12 **PTGTOGL:** TRIG Output Toggle Mode bit

1 = Toggle state of the PTGOx for each execution of the PTGTRIG command

0 = Each execution of PTGTRIG command will generate a single PTGOx pulse determined by value

in PTGPWD

bit 11 Unimplemented: Read as '0'

bit 10 PTGSWT: Software Trigger bit⁽²⁾

1 = Trigger the PTG module

0 = No action (clearing this bit will have no effect)

bit 9 PTGSSEN: Enable Single Step

1 = Enable Single Step mode

0 = Disable Single Step mode

bit 8 PTGIVIS: Counter/Timer Visibility Control bit

1 = Reads of the PTGSDLIM, PTGCxLIM or PTGTxLIM registers returns the current values of their

corresponding counter/timer registers (PTGSD, PTGCx, PTGTx)

0 = Reads of the PTGSDLIM, PTGCxLIM or PTGTxLIM registers returns the value previously written

to those limit registers

bit 7 PTGSTRT: Start PTG Sequencer bit

1 = Start to sequentially execute commands (Continuous mode)

0 = Stop executing commands

bit 6 PTGWDTO: PTG Watchdog Timer Time-out Status bit

1 = PTG watchdog timer has timed out

0 = PTG watchdog timer has not timed out.

bit 5-2 Unimplemented: Read as '0'

Note 1: These bit apply to the PTGWHI and PTGWLO commands only.

2: This bit is only used with the PTGCTRL step command software trigger option.

REGISTER 24-1: PTGCST: PTG CONTROL/STATUS REGISTER (CONTINUED)

- bit 1-0 **PTGITM<1:0>:** PTG Input Trigger Command Operating Mode bits⁽¹⁾
 - 11 = Single level detect with step delay not executed on exit of command (regardless of PTGCTRL command)
 - 10 = Single level detect with step delay executed on exit of command
 - 01 = Continuous edge detect with step delay not executed on exit of command (regardless of PTGCTRL command)
 - 00 = Continuous edge detect with step delay executed on exit of command
- Note 1: These bit apply to the PTGWHI and PTGWLO commands only.
 - 2: This bit is only used with the PTGCTRL step command software trigger option.

REGISTER 24-2: PTGCON: PTG CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PTGCLK<2:0>				PTGDIV<4:0>	•	
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGPWD<3:0>				_	PTGWDT<2:0>		
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-13 PTGCLK<2:0>: Select PTG Module Clock Source bits

111 = Reserved

110 = Reserved

101 = PTG module clock source will be T3CLK

100 = PTG module clock source will be T2CLK

011 = PTG module clock source will be T1CLK

010 = PTG module clock source will be TAD

001 = PTG module clock source will be Fosc

000 = PTG module clock source will be FP

bit 12-8 PTGDIV<4:0>: PTG Module Clock Prescaler (divider) bits

11111 = Divide by 32

11110 = Divide by 31

•

00001 = Divide by 2

00000 = Divide by 1

bit 7-4 **PTGPWD<3:0>:** PTG Trigger Output Pulse Width bits

1111 = All trigger outputs are 16 PTG clock cycles wide

1110 = All trigger outputs are 15 PTG clock cycles wide

.

.

•

0001 = All trigger outputs are 2 PTG clock cycles wide

0000 = All trigger outputs are 1 PTG clock cycle wide

bit 3 **Unimplemented:** Read as '0'

bit 2-0 PTGWDT<2:0>: Select PTG Watchdog Time-out Count Value bits

111 = Watchdog will time out after 512 PTG clocks

110 = Watchdog will time out after 256 PTG clocks

101 = Watchdog will time out after 128 PTG clocks

100 = Watchdog will time out after 64 PTG clocks

011 = Watchdog will time out after 32 PTG clocks

010 = Watchdog will time out after 16 PTG clocks

001 = Watchdog will time out after 8 PTG clocks

000 = Watchdog is disabled

REGISTER 24-3: PTGBTE: PTG BROADCAST TRIGGER ENABLE REGISTER^(1,2)

W = Writable bit

'1' = Bit is set

Legend:

bit 5

R = Readable bit

-n = Value at POR

| R/W-0 |
|--------|--------|--------|--------|--------|--------|--------|--------|
| ADCTS4 | ADCTS3 | ADCTS2 | ADCTS1 | IC4TSS | IC3TSS | IC2TSS | IC1TSS |
| bit 15 | | | | | | | bit 8 |

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OC4CS	OC3CS	OC2CS	OC1CS	OC4TSS	OC3TSS	OC2TSS	OC1TSS
bit 7							bit 0

U = Unimplemented bit, read as '0'

x = Bit is unknown

'0' = Bit is cleared

bit 15	ADCTS4: Sample Trigger PTGO15 for ADC bit
	1 = Generate trigger when the broadcast command is executed0 = Do not generate trigger when the broadcast command is executed
bit 14	ADCTS3: Sample Trigger PTGO14 for ADC bit
	1 = Generate trigger when the broadcast command is executed0 = Do not generate trigger when the broadcast command is executed
bit 13	ADCTS2: Sample Trigger PTGO13 for ADC bit
	1 = Generate trigger when the broadcast command is executed0 = Do not generate trigger when the broadcast command is executed
bit 12	ADCTS1: Sample Trigger PTGO12 for ADC bit
	1 = Generate trigger when the broadcast command is executed0 = Do not generate trigger when the broadcast command is executed
bit 11	IC4TSS: Trigger/Synchronization Source for IC4 bit
	1 = Generate trigger/synchronization when the broadcast command is executed0 = Do not generate trigger/synchronization when the broadcast command is executed
bit 10	IC3TSS: Trigger/Synchronization Source for IC3 bit
	1 = Generate trigger/synchronization when the broadcast command is executed0 = Do not generate trigger/synchronization when the broadcast command is executed
bit 9	IC2TSS: Trigger/Synchronization Source for IC2 bit
	1 = Generate trigger/synchronization when the broadcast command is executed0 = Do not generate trigger/synchronization when the broadcast command is executed
bit 8	IC1TSS: Trigger/Synchronization Source for IC1 bit
	1 = Generate trigger/synchronization when the broadcast command is executed0 = Do not generate trigger/synchronization when the broadcast command is executed
bit 7	OC4CS: Clock Source for OC4 bit
	1 = Generate clock pulse when the broadcast command is executed0 = Do not generate clock pulse when the broadcast command is executed
bit 6	OC3CS: Clock Source for OC3 bit
	1 = Generate clock pulse when the broadcast command is executed

Note 1: This register is read only when the PTG module is executing step commands (PTGEN = 1 and PTGSTRT = 1).

0 = Do not generate clock pulse when the broadcast command is executed

1 = Generate clock pulse when the broadcast command is executed 0 = Do not generate clock pulse when the broadcast command is executed

2: This register only used with the PTGCTRL OPTION = 1111 step command.

OC2CS: Clock Source for OC2 bit

REGISTER 24-3: PTGBTE: PTG BROADCAST TRIGGER ENABLE REGISTER^(1,2) (CONTINUED)

- bit 4 OC1CS: Clock Source for OC1 bit 1 = Generate clock pulse when the broadcast command is executed 0 = Do not generate clock pulse when the broadcast command is executed bit 3 OC4TSS: Trigger/Synchronization Source for OC4 bit 1 = Generate trigger/synchronization when the broadcast command is executed 0 = Do not generate trigger/synchronization when the broadcast command is executed bit 2 OC3TSS: Trigger/Synchronization Source for OC3 bit 1 = Generate trigger/synchronization when the broadcast command is executed 0 = Do not generate trigger/synchronization when the broadcast command is executed bit 1 OC2TSS: Trigger/Synchronization Source for OC2 bit 1 = Generate trigger/synchronization when the broadcast command is executed 0 = Do not generate trigger/synchronization when the broadcast command is executed bit 0 OC1TSS: Trigger/Synchronization Source for OC1 bit 1 = Generate trigger/synchronization when the broadcast command is executed 0 = Do not generate trigger/synchronization when the broadcast command is executed
- **Note 1:** This register is read only when the PTG module is executing step commands (PTGEN = 1 and PTGSTRT = 1).
 - 2: This register only used with the PTGCTRL OPTION = 1111 step command.

REGISTER 24-4: PTGT0LIM: PTG TIMER0 LIMIT REGISTER(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
	PTGT0LIM<15:8>									
bit 15							bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
PTGT0LIM<7:0>									
bit 7									

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **PTGT0LIM<15:0>:** PTG Timer0 Limit Register bits

General purpose Timer0 limit register (effective only with a PTGT0 step command).

Note 1: This register is read only when the PTG module is executing step commands (PTGEN = 1 and PTGSTRT = 1).

REGISTER 24-5: PTGT1LIM: PTG TIMER1 LIMIT REGISTER(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGT1L	IM<15:8>			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGT1L	.IM<7:0>			
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **PTGT1LIM<15:0>:** PTG Timer1 Limit Register bits

General purpose Timer1 limit register (effective only with a PTGT1 step command).

Note 1: This register is read only when the PTG module is executing step commands (PTGEN = 1 and PTGSTRT = 1).

REGISTER 24-6: PTGSDLIM: PTG STEP DELAY LIMIT REGISTER (1,2)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGSDL	IM<15:8>			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGSDL	_IM<7:0>			
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **PTGSDLIM<15:0>:** PTG Step Delay Limit Register bits

Holds a PTG Step Delay value representing the number of additional PTG clocks between the start of a step command, and the completion of the step command.

- Note 1: A base step delay of one PTG clock is added to any value written to the PTGSDLIM register (Step Delay = (PTGSDLIM) + 1).
 - 2: This register is read only when the PTG module is executing step commands (PTGEN = 1 and PTGSTRT = 1).

REGISTER 24-7: PTGC0LIM: PTG COUNTER 0 LIMIT REGISTER(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGC0L	IM<15:8>			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGC0L	-IM<7:0>			
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 PTGC0LIM<15:0>: PTG Counter 0 Limit Register bits

May be used to specify the loop count for the PTGJMPC0 step command, or as a limit register for the general purpose counter 0.

Note 1: This register is read only when the PTG module is executing step commands (PTGEN = 1 and PTGSTRT = 1).

REGISTER 24-8: PTGC1LIM: PTG COUNTER 1 LIMIT REGISTER⁽¹⁾

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGC1L	IM<15:8>			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGC1L	-IM<7:0>			
bit 7							bit 0

 Legend:
 R = Readable bit
 W = Writable bit
 U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **PTGC1LIM<15:0>:** PTG Counter 1 Limit Register bits

May be used to specify the loop count for the PTGJMPC1 step command, or as a limit register for the general purpose counter 1.

Note 1: This register is read only when the PTG module is executing step commands (PTGEN = 1 and PTGSTRT = 1).

REGISTER 24-9: PTGHOLD: PTG HOLD REGISTER⁽¹⁾

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
	PTGHOLD<15:8>									
bit 15							bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGHO	LD<7:0>			
bit 7							bit 0

 Legend:
 R = Readable bit
 W = Writable bit
 U = Unimplemented bit, read as '0'

 -n = Value at POR
 '1' = Bit is set
 '0' = Bit is cleared
 x = Bit is unknown

bit 15-0 **PTGHOLD<15:0>:** PTG General Purpose Hold Register bits

Holds user supplied data to be copied to the PTGTxLIM, PTGCxLIM, PTGSDLIM, or PTGL0 registers with the PTGCOPY command.

Note 1: This register is read only when the PTG module is executing step commands (PTGEN = 1 and PTGSTRT = 1).

REGISTER 24-10: PTGADJ: PTG ADJUST REGISTER(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGAD	J<15:8>			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGAE)J<7:0>			
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **PTGADJ<15:0>:** PTG Adjust Register bits

This register Holds user supplied data to be added to the PTGTxLIM, PTGCxLIM, PTGSDLIM, or PTGL0 registers with the PTGADD command.

Note 1: This register is read only when the PTG module is executing step commands (PTGEN = 1 and PTGSTRT = 1).

REGISTER 24-11: PTGL0: PTG LITERAL 0 REGISTER(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGL0	<15:8>			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGL	0<7:0>			
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **PTGL0<15:0>:** PTG Literal 0 Register bits

This register holds the 16-bit value to be written to the AD1CHS0 register with the PTGCTRL step command

Note 1: This register is read only when the PTG module is executing step commands (PTGEN = 1 and PTGSTRT = 1).

REGISTER 24-12: PTGQPTR: PTG STEP QUEUE POINTER REGISTER⁽¹⁾

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	_	_	_	_	_	_	_
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	_	_			PTGQPTR<4:0	 >	
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **Unimplemented:** Read as '0'

bit 4-0 PTGQPTR<4:0>: PTG Step Queue Pointer Register bits

This register points to the currently active step command in the step queue.

Note 1: This register is read only when the PTG module is executing step commands (PTGEN = 1 and PTGSTRT = 1).

REGISTER 24-13: PTGQUEx: PTG STEP QUEUE REGISTERS $(x = 0.7)^{(1,3)}$

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			STEP(2x -	+1)<7:0> ⁽²⁾			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			STEP(2x	()<7:0> ⁽²⁾			
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-8 STEP(2x +1)<7:0>: PTG Step Queue Pointer Register bits⁽²⁾

A queue location for storage of the STEP(2x +1) command byte.

bit 7-0 STEP(2x)<7:0>: PTG Step Queue Pointer Register bits(2)

A queue location for storage of the STEP(2x) command byte.

- **Note 1:** This register is read only when the PTG module is executing step commands (PTGEN = 1 and PTGSTRT = 1).
 - 2: Refer to Table 24-1 for the STEP command encoding.
 - 3: The step registers maintain their values on any type of reset.

24.4 STEP Commands and Format

TABLE 24-1: PTG STEP COMMAND FORMAT

STEP Command Byte:							
	STEPx	<7:0>					
CMD<3:0>		OPTION<3:0>					
bit 7	bit 4	bit 3	bit 0				

bit 7-4	CMD<3:0>	Step Command	Command Description
	0000	PTGCTRL	Execute control command as described by OPTION<3:0>
	0001	PTGADD	Add contents of PTGADJ register to target register as described by OPTION<3:0>
		PTGCOPY	Copy contents of PTGHOLD register to target register as described by OPTION<3:0>
	001x	PTGSTRB	Copy the value contained in CMD<0>:OPTION<3:0> to the CH0SA<4:0> bits (AD1CHS0<4:0>)
	0100	PTGWHI	Wait for a Low to High edge input from selected PTG trigger input as described by OPTION<3:0>
	0101	PTGWLO	Wait for a High to Low edge input from selected PTG trigger input as described by OPTION<3:0>
	0110	Reserved	Reserved
	0111	PTGIRQ	Generate individual interrupt request as described by OPTION3<:0>
	100x	PTGTRIG	Generate individual trigger output as described by < <cmd<0>:OPTION<3:0>></cmd<0>
	101x	PTGJMP	Copy the value indicated in < <cmd<0>:OPTION<3:0>> to the Queue Pointer (PTGQPTR) and jump to that step queue</cmd<0>
	110x	PTGJMPC0	PTGC0 = PTGC0LIM: Increment the Queue Pointer (PTGQPTR)
			PTGC0 ≠ PTGC0LIM: Increment Counter 0 (PTGC0) and copy the value indicated in < <cmd<0>:OPTION<3:0>> to the Queue Pointer (PTGQPTR) and jump to that step queue</cmd<0>
	111x	PTGJMPC1	PTGC1 = PTGC1LIM: Increment the queue pointer (PTGQPTR)
			PTGC1 \neq PTGC1LIM: Increment Counter 1 (PTGC1) and copy the value indicated in < <cmd<0>:OPTION<3:0>> to the Queue Pointer (PTGQPTR) and jump to that step queue</cmd<0>

Note 1: All reserved commands or options will execute but have no effect (i.e., execute as a NOP instruction).

^{2:} Refer to Table 24-2 for the trigger output descriptions.

^{3:} This feature is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

TABLE 24-1: PTG STEP COMMAND FORMAT (CONTINUED)

bit 3-0	Step Command	OPTION<3:0>	Option Description
	PTGCTRL ⁽¹⁾	0000	Reserved
		0001	Reserved
		0010	Disable Step Delay Timer (PTGSD)
		0011	Reserved
		0100	Reserved
		0101	Reserved
		0110	Enable Step Delay Timer (PTGSD)
		0111	Reserved
		1000	Start and wait for the PTG Timer 0 to match Timer 0 Limit Register
		1001	Start and wait for the PTG Timer 1 to match Timer 1 Limit Register
		1010	Reserved
		1011	Wait for software trigger bit transition from low to high before continuing (PTGSWT = 0 to 1)
		1100	Copy contents of the Counter 0 register to the AD1CHS0 register
		1101	Copy contents of the Counter 1 register to the AD1CHS0 register
		1110	Copy contents of the Literal 0 register to the AD1CHS0 register
		1111	Generate triggers indicated in the Broadcast Trigger Enable Register (PTGBTE)
	PTGADD(1)	0000	Add contents of PTGADJ register to the Counter 0 Limit register (PTGC0LIM)
		0001	Add contents of PTGADJ register to the Counter 1 Limit register (PTGC1LIM)
		0010	Add contents of PTGADJ register to the Timer 0 Limit register (PTGT0LIM)
		0011	Add contents of PTGADJ register to the Timer 1 Limit register (PTGT1LIM)
		0100	Add contents of PTGADJ register to the Step Delay Limit register (PTGSDLIM)
		0101	Add contents of PTGADJ register to the Literal 0 register (PTGL0)
		0110	Reserved
		0111	Reserved
	PTGCOPY ⁽¹⁾	1000	Copy contents of PTGHOLD register to the Counter 0 Limit register (PTGC0LIM)
		1001	Copy contents of PTGHOLD register to the Counter 1 Limit register (PTGC1LIM)
		1010	Copy contents of PTGHOLD register to the Timer 0 Limit register (PTGT0LIM)
		1011	Copy contents of PTGHOLD register to the Timer 1 Limit register (PTGT1LIM)
		1100	Copy contents of PTGHOLD register to the Step Delay Limit register (PTGSDLIM)
		1101	Copy contents of PTGHOLD register to the Literal 0 register (PTGL0)
		1110	Reserved
		1111	Reserved

Note 1: All reserved commands or options will execute but have no effect (i.e., execute as a NOP instruction).

^{2:} Refer to Table 24-2 for the trigger output descriptions.

^{3:} This feature is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

TABLE 24-1: PTG STEP COMMAND FORMAT (CONTINUED)

bit 3-0	Step Command	OPTION<3:0>	Option Description
	PTGWHI(1)	0000	PWM Special Event Trigger ⁽³⁾
	or PTGWLO ⁽¹⁾	0001	PWM Master Timebase Synchronization Output ⁽³⁾
	P.I.GMTO(.)	0010	PWM1 Interrupt ⁽³⁾
		0011	PWM2 Interrupt ⁽³⁾
		0100	PWM3 Interrupt ⁽³⁾
		0101	Reserved
		0110	Reserved
		0111	OC1 Trigger Event
		1000	OC2 Trigger Event
		1001	IC1 Trigger Event
		1010	CMP1 Trigger Event
		1011	CMP2 Trigger Event
		1100	CMP3 Trigger Event
		1101	CMP4 Trigger Event
		1110	ADC Conversion Done Interrupt
		1111	INT2 External Interrupt
	PTGIRQ(1)	0000	Generate PTG interrupt 0
		0001	Generate PTG interrupt 1
		0010	Generate PTG interrupt 2
		0011	Generate PTG interrupt 3
		0100	Reserved
		•	•
		•	•
		•	•
	(2)	1111	Reserved
	PTGTRIG ⁽²⁾	00000	PTG00
		00001	PTGO1
		•	•
		•	•
		•	PTO COO
		11110	PTGO30
		11111	PTGO31

Note 1: All reserved commands or options will execute but have no effect (i.e., execute as a NOP instruction).

^{2:} Refer to Table 24-2 for the trigger output descriptions.

^{3:} This feature is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

TABLE 24-2: PTG OUTPUT DESCRIPTIONS

PTG Output Number	PTG Output Description
PTGO0	Trigger/Synchronization Source for OC1
PTGO1	Trigger/Synchronization Source for OC2
PTGO2	Trigger/Synchronization Source for OC3
PTGO3	Trigger/Synchronization Source for OC4
PTGO4	Clock Source for OC1
PTGO5	Clock Source for OC2
PTGO6	Clock Source for OC3
PTGO7	Clock Source for OC4
PTGO8	Trigger/Synchronization Source for IC1
PTGO9	Trigger/Synchronization Source for IC2
PTGO10	Trigger/Synchronization Source for IC3
PTGO11	Trigger/Synchronization Source for IC4
PTGO12	Sample Trigger for ADC
PTGO13	Sample Trigger for ADC
PTGO14	Sample Trigger for ADC
PTGO15	Sample Trigger for ADC
PTGO16	PWM Time Base Synchronous Source for PWM ⁽¹⁾
PTGO17	PWM Time Base Synchronous Source for PWM ⁽¹⁾
PTGO18	Mask Input Select for Op Amp/Comparator
PTGO19	Mask Input Select for Op Amp/Comparator
PTGO20	Reserved
PTGO21	Reserved
PTGO22	Reserved
PTGO23	Reserved
PTGO24	Reserved
PTGO25	Reserved
PTGO26	Reserved
PTGO27	Reserved
PTGO28	Reserved
PTGO29	Reserved
PTGO30	PTG output to PPS input selection
PTGO31	PTG output to PPS input selection

Note 1: This feature is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

25.0 OP AMP/COMPARATOR MODULE

Note 1: This data sheet summarizes the features dsPIC33EPXXXGP50X, the dsPIC33EPXXXMC20X/50X, PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 26. "Op amp/ Comparator" (DS70357) of "dsPIC33E/PIC24E Family Reference Manual', which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

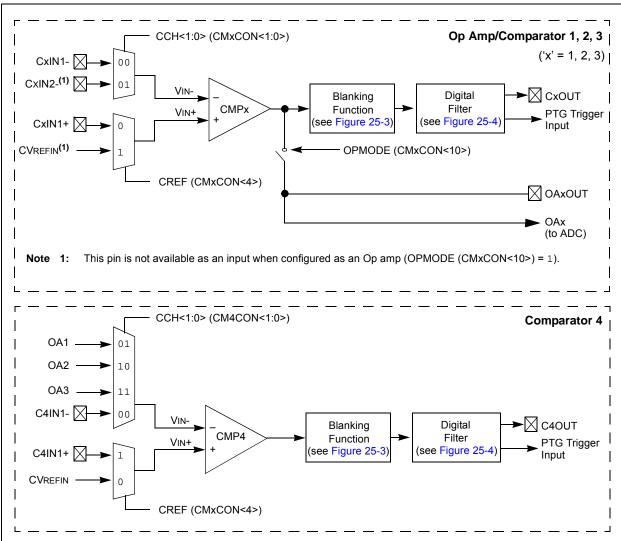
The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X devices contain up to four comparators which can be configured in various ways. Comparators CMP1, CMP2, and CMP3 also have the option to be configured as Op amps, with the output being brought to an external pin for gain/filtering connections. As shown in Figure 25-1, individual comparator options are specified by the Comparator module's Special Function Register (SFR) control bits.

These options allow users to:

- · Select the edge for trigger and interrupt generation
- · Configure the comparator voltage reference
- · Configure output blanking and masking
- Configure as a Comparator or Op amp (CMP1, CMP2, and CMP3 only)

Note: Not all Op amp/Comparator input/output connections are available on all devices. See the "Pin Diagrams" section for available connections.

FIGURE 25-1: OP AMP/COMPARATOR I/O OPERATING MODES



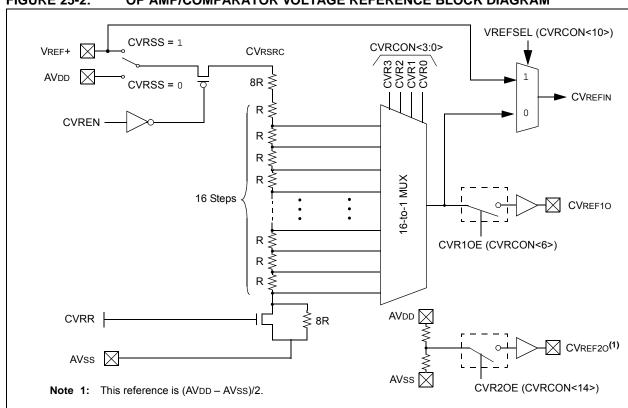


FIGURE 25-2: OP AMP/COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM

FIGURE 25-3: USER-PROGRAMMABLE BLANKING FUNCTION BLOCK DIAGRAM

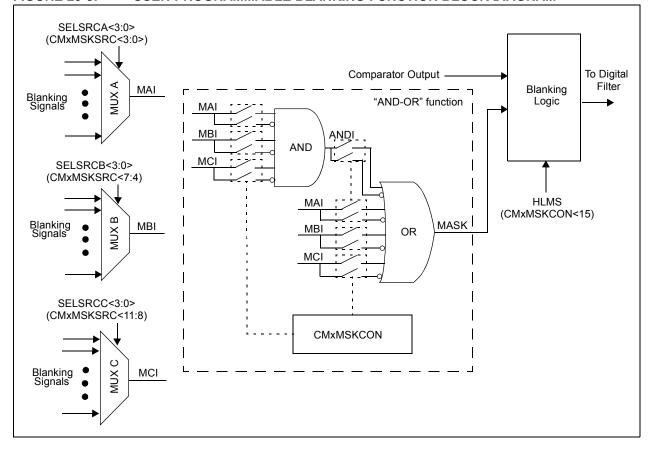
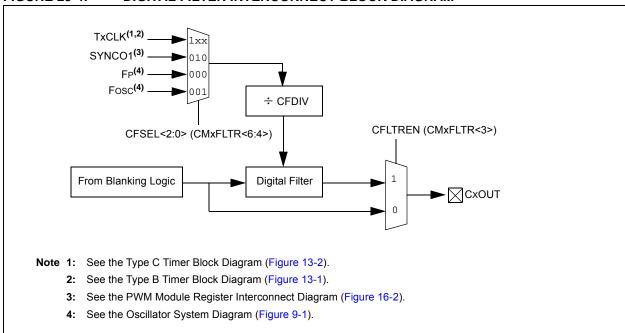


FIGURE 25-4: DIGITAL FILTER INTERCONNECT BLOCK DIAGRAM



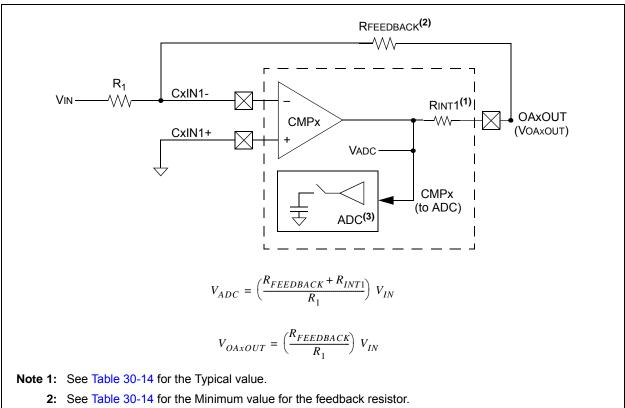
25.1 Op amp Application Considerations

There are two configurations to take into consideration when designing with the Op amp modules that are available in the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/ MC20X devices. Configuration A (see Figure 25-5) takes advantage of the internal connection to the ADC module to route the output of the Op amp directly to the ADC for measurement. Configuration B (see Figure 25-6) requires that the designer externally route the output of the Op amp (OAxOUT) to a separate analog input pin (ANx) on the device. Table 30-16 in Section 30.0 "Electrical Characteristics" describes the performance characteristics for the Op amps, distinguishing between the two configuration types where applicable.

25.1.1 OP AMP CONFIGURATION A

Figure 25-5 shows a typical inverting amplifier circuit taking advantage of the internal connections from the Op amp output to the input of the ADC. The advantage of this configuration is that the user does not need to consume another analog input (ANx) on the device, and allows the user to simultaneous sample all three Op amps with the ADC module, if needed. However, the presence of the internal resistance, RINT1, adds an error in the feedback path. Since RINT1 is an internal resistance, in relation to the Op amp output (VOAxOUT) and ADC internal connection (VADC), RINT1 must be included in the numerator term of the transfer function. See Table 30-14 in Section 30.0 "Electrical Characteristics" for the typical value of RINT1. Table 30-59 and Table 30-60 in Section 30.0 "Electrical Characteristics" describe the minimum sample time (TSAMP) requirements for the ADC module in this configuration. Figure 25-5 also defines the equations that should be used when calculating the expected voltages at points VADC and VOAXOUT.

FIGURE 25-5: OP AMP CONFIGURATION A



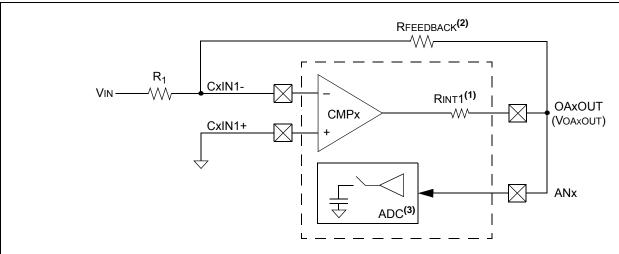
3: See Table 30-59 and Table 30-60 for the minimum sample time (TSAMP).

25.1.2 OP AMP CONFIGURATION B

Figure 25-6 shows a typical inverting amplifier circuit with the output of the Op amp (OAxOUT) externally routed to a separate analog input pin (ANx) on the device. This Op amp configuration is slightly different in terms of the Op amp output and the ADC input connection, therefore RINT1 is not included in the transfer function. However, this configuration requires the designer to externally route the Op amp output (OAxOUT) to another analog input pin (ANx). See Table 30-14 in Section 30.0 "Electrical Characteristics" for the typical value of RINT1. Table 30-59 and Table 30-60 in Section 30.0 "Electrical Characteristics" describe the minimum sample time (TSAMP) requirements for the ADC module in this configuration.

Figure 25-6 also defines the equation to be used to calculate the expected voltage at point VOAXOUT. This is the typical inverting amplifier equation.

FIGURE 25-6: OP AMP CONFIGURATION B



$$V_{OAxOUT} = \left(\frac{R_{FEEDBACK}}{R_1}\right) \, V_{IN}$$

Note 1: See Table 30-14 for the Typical value.

2: See Table 30-14 for the Minimum value for the feedback resistor.

3: See Table 30-59 and Table 30-60 for the minimum sample time (TSAMP).

25.2 Op amp/Comparator Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:

In the event you are not able to access the product page using the link above, enter this URL in your browser:

http://www.microchip.com/wwwproducts/ Devices.aspx?dDocName=en555464

25.2.1 KEY RESOURCES

- Section 26. "Op amp/Comparator" (DS70357)
- · Code Samples
- · Application Notes
- · Software Libraries
- Webinars
- All related dsPIC33E/PIC24E Family Reference Manuals Sections
- · Development Tools

25.3 Op amp/Comparator Registers

REGISTER 25-1: CMSTAT: OP AMP/COMPARATOR STATUS REGISTER

R/W-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
CMSIDL	_	_	_	C4EVT ⁽¹⁾	C3EVT ⁽¹⁾	C2EVT ⁽¹⁾	C1EVT ⁽¹⁾
bit 15							bit 8

U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
_	_	_	_	C4OUT ⁽²⁾	C3OUT ⁽²⁾	C2OUT ⁽²⁾	C1OUT ⁽²⁾
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15 CMSIDL: Stop in Idle Mode bit

1 = Discontinue operation of all comparators when device enters Idle mode

0 = Continue operation of all comparators in Idle mode

bit 14-12 **Unimplemented:** Read as '0'

bit 11 C4EVT: Op amp/Comparator 4 Event Status bit⁽¹⁾

1 = Op amp/Comparator event occurred

0 = Op amp/Comparator event did not occur

bit 10 **C3EVT:** Comparator 3 Event Status bit⁽¹⁾

1 = Comparator event occurred

0 = Comparator event did not occur

bit 9 **C2EVT:** Comparator 2 Event Status bit⁽¹⁾

1 = Comparator event occurred

0 = Comparator event did not occur

bit 8 C1EVT: Comparator 1 Event Status bit⁽¹⁾

1 = Comparator event occurred

0 = Comparator event did not occur

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **C4OUT:** Comparator 4 Output Status bit⁽²⁾

When CPOL = 0:

1 = VIN+ > VIN-

0 = VIN+ < VIN-

When CPOL = 1:

1 = VIN+ < VIN-

0 = VIN+ > VIN-

Note 1: Reflects the value of the CEVT bit in the respective Op amp/Comparator control register, CMxCON<9>.

2: Reflects the value of the COUT bit in the respective Op amp/Comparator control register, CMxCON<8>.

REGISTER 25-1: CMSTAT: OP AMP/COMPARATOR STATUS REGISTER (CONTINUED)

bit 2 C3OUT: Comparator 3 Output Status bit(2) When CPOL = 0: 1 = VIN+ > VIN-0 = VIN+ < VIN-When CPOL = 1: 1 = VIN+ < VIN-0 = VIN+ > VINbit 1 C2OUT: Comparator 2 Output Status bit(2) When CPOL = 0: 1 = VIN+ > VIN-0 = VIN+ < VIN-When CPOL = 1: 1 = VIN+ < VIN-0 = VIN+ > VINbit 0 C10UT: Comparator 1 Output Status bit(2) When CPOL = 0: 1 = VIN+ > VIN-0 = VIN+ < VIN-When CPOL = 1: 1 = VIN+ < VIN-0 = VIN+ > VIN-

- Note 1: Reflects the value of the CEVT bit in the respective Op amp/Comparator control register, CMxCON<9>.
 - 2: Reflects the value of the COUT bit in the respective Op amp/Comparator control register, CMxCON<8>.

REGISTER 25-2: CMxCON: COMPARATOR CONTROL REGISTER (x = 1, 2, OR 3)

R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
CON	COE	CPOL	_	_	OPMODE	CEVT	COUT
bit 15							bit 8

R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0
EVPOI	_<1:0>	_	CREF	_	_	CCH	<1:0>
bit 7							bit 0

Legend:

bit 8

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15 **CON:** Comparator Enable bit

1 = Comparator is enabled0 = Comparator is disabled

bit 14 COE: Comparator Output Enable bit

1 = Comparator output is present on the CxOUT pin

0 = Comparator output is internal only

bit 13 **CPOL:** Comparator Output Polarity Select bit

1 = Comparator output is inverted0 = Comparator output is not inverted

bit 12-11 Unimplemented: Read as '0'

bit 10 **OPMODE:** Op Amp/Comparator Operation Mode Select bit

1 = Circuit operates as an Op amp

0 = Circuit operates as a Comparator

bit 9 **CEVT:** Comparator Event bit

1 = Comparator event according to EVPOL<1:0> settings occurred; disables future triggers and

interrupts until the bit is cleared 0 = Comparator event did not occur

COUT: Comparator Output bit

When CPOL = 0 (non-inverted polarity):

1 = VIN+ > VIN-

0 = VIN+ < VIN-

When CPOL = 1 (inverted polarity):

1 = VIN+ < VIN-

0 = VIN+ > VIN-

Note 1: Inputs that are selected and not available will be tied to Vss. See the "Pin Diagrams" section for available inputs for each package.

2: This input is not available when OPMODE (CMxCON<10>) = 1.

REGISTER 25-2: CMxCON: COMPARATOR CONTROL REGISTER (x = 1, 2, OR 3) (CONTINUED)

bit 7-6 **EVPOL<1:0>:** Trigger/Event/Interrupt Polarity Select bits

11 = Trigger/Event/Interrupt generated on any change of the comparator output (while CEVT = 0)

10 = Trigger/Event/Interrupt generated only on high to low transition of the polarity-selected comparator output (while CEVT = 0)

If CPOL = 1 (inverted polarity):

Low-to-high transition of the comparator output

If CPOL = 0 (non-inverted polarity):

High-to-low transition of the comparator output

01 = Trigger/Event/Interrupt generated only on low to high transition of the polarity-selected comparator output (while CEVT = 0)

If CPOL = 1 (inverted polarity):

High-to-low transition of the comparator output

If CPOL = 0 (non-inverted polarity):

Low-to-high transition of the comparator output

00 = Trigger/Event/Interrupt generation is disabled

bit 5 **Unimplemented:** Read as '0'

bit 4 CREF: Comparator Reference Select bit (VIN+ input)⁽¹⁾

1 = VIN+ input connects to internal CVREFIN voltage(2)

0 = VIN+ input connects to CxIN1+ pin

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **CCH<1:0>:** Op amp/Comparator Channel Select bits⁽¹⁾

11 = Unimplemented

10 = Unimplemented

01 = Inverting input of Comparator connects to CxIN2- pin⁽²⁾

00 = Inverting input of Op amp/Comparator connects to CxIN1- pin

Note 1: Inputs that are selected and not available will be tied to Vss. See the "Pin Diagrams" section for available inputs for each package.

2: This input is not available when OPMODE (CMxCON<10>) = 1.

REGISTER 25-3: CM4CON: COMPARATOR CONTROL REGISTER

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
CON	COE	CPOL	_	_	_	CEVT	COUT
bit 15							bit 8

R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0
EVPOL	_<1:0>	_	CREF	_	_	CCH	<1:0>
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15 CON: Comparator Enable bit

1 = Comparator is enabled0 = Comparator is disabled

bit 14 **COE**: Comparator Output Enable bit

 ${\tt 1}$ = Comparator output is present on the CxOUT pin

0 = Comparator output is internal only

bit 13 CPOL: Comparator Output Polarity Select bit

1 = Comparator output is inverted0 = Comparator output is not inverted

bit 12-10 **Unimplemented:** Read as '0' bit 9 **CEVT:** Comparator Event bit

CEVT: Comparator Event bit 1 = Comparator event according to EVPOL<1:0> settings occurred; disables future triggers and

interrupts until the bit is cleared 0 = Comparator event did not occur

bit 8 **COUT:** Comparator Output bit

When CPOL = 0 (non-inverted polarity):

1 = VIN+ > VIN-

0 = VIN+ < VIN-

When CPOL = 1 (inverted polarity):

1 = VIN+ < VIN-

0 = VIN+ > VIN-

bit 7-6 **EVPOL<1:0>:** Trigger/Event/Interrupt Polarity Select bits

11 = Trigger/Event/Interrupt generated on any change of the comparator output (while CEVT = 0)

10 = Trigger/Event/Interrupt generated only on high to low transition of the polarity-selected comparator output (while CEVT = 0)

If CPOL = 1 (inverted polarity):

Low-to-high transition of the comparator output

If CPOL = 0 (non-inverted polarity):

High-to-low transition of the comparator output

01 = Trigger/Event/Interrupt generated only on low to high transition of the polarity-selected comparator output (while CEVT = 0)

If CPOL = 1 (inverted polarity):

High-to-low transition of the comparator output

If CPOL = 0 (non-inverted polarity):

Low-to-high transition of the comparator output

00 = Trigger/Event/Interrupt generation is disabled

Note 1: Inputs that are selected and not available will be tied to Vss. See the "Pin Diagrams" section for available inputs for each package.

REGISTER 25-3: CM4CON: COMPARATOR CONTROL REGISTER (CONTINUED)

bit 5 **Unimplemented:** Read as '0'

bit 4 CREF: Comparator Reference Select bit (VIN+ input)⁽¹⁾

1 = VIN+ input connects to internal CVREFIN voltage

0 = VIN+ input connects to C4IN1+ pin

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **CCH<1:0>:** Comparator Channel Select bits⁽¹⁾

11 = VIN- input of comparator connects to CMP3 10 = VIN- input of comparator connects to CMP2 01 = VIN- input of comparator connects to CMP1 00 = VIN- input of comparator connects to C4IN1-

Note 1: Inputs that are selected and not available will be tied to Vss. See the "Pin Diagrams" section for available inputs for each package.

REGISTER 25-4: CMxMSKSRC: COMPARATOR MASK SOURCE SELECT CONTROL REGISTER

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	RW-0
_	_	_	_		SELSRO	CC<3:0>	
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
	SELSRO	B<3:0>		SELSRCA<3:0>				
bit 7							bit 0	

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-12 **Unimplemented:** Read as '0'

bit 11-8 SELSRCC<3:0>: Mask C Input Select bits

1111 **= FLT4**

1110 **= FLT2**

1101 = PTGO19

1100 **= PTGO18**

1011 = Reserved

1010 = Reserved 1001 = Reserved

1000 = Reserved

0111 = Reserved

0110 = Reserved

0101 = PWM3H

0100 = PWM3L

0011 = PWM2H

0010 = PWM2L

0001 = PWM1H

0000 = PWM1L

bit 7-4 SELSRCB<3:0>: Mask B Input Select bits

1111 **= FLT4**

1110 = FLT2

1101 = PTGO19

1100 **= PTGO18**

1011 = Reserved

1010 = Reserved

1001 = Reserved

1000 = Reserved

0111 = Reserved

0110 = Reserved

0101 = PWM3H

0100 = PWM3L

0011 = PWM2H

0010 = PWM2L

0001 = PWM1H

0000 = PWM1L

REGISTER 25-4: CMxMSKSRC: COMPARATOR MASK SOURCE SELECT CONTROL REGISTER

bit 3-0 SELSRCA<3:0>: Mask A Input Select bits

1111 = FLT4

1110 = FLT2

1101 **= PTGO19**

1100 **= PTGO18**

1011 = Reserved

1010 = Reserved

1001 = Reserved

1000 = Reserved

0111 = Reserved

0110 = Reserved

0101 **= PWM3H**

0100 = PWM3L

0011 = PWM2H

0010 = PWM2L

0001 **= PWM1H**

0000 **= PWM1L**

REGISTER 25-5: CMxMSKCON: COMPARATOR MASK GATING CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
HLMS		OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN
bit 15							bit 8

| R/W-0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| NAGS | PAGS | ACEN | ACNEN | ABEN | ABNEN | AAEN | AANEN |
| bit 7 | | | | | | | bit 0 |

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit,	read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

-n = Value	at POR '1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
bit 15	HLMS: High or Low-Level Ma	•	
	G (G,		') comparator signal from propagating ') comparator signal from propagating
bit 14	Unimplemented: Read as '0	,	
bit 13	OCEN: OR Gate C Input Ena	ble bit	
	1 = MCI is connected to OR of the original origin	•	
bit 12	OCNEN: OR Gate C Input In	verted Enable bit	
	1 = Inverted MCI is connected 0 = Inverted MCI is not connected	. I _	
bit 11	OBEN: OR Gate B Input Ena	ble bit	
	1 = MBI is connected to OR of the OR of the Connected to OR of the OR of		
bit 10	OBNEN: OR Gate B Input Inv	verted Enable bit	
	1 = Inverted MBI is connected 0 = Inverted MBI is not connected materials.	•	
bit 9	OAEN: OR Gate A Input Ena	ble bit	
	1 = MAI is connected to OR g 0 = MAI is not connected to O		
bit 8	OANEN: OR Gate A Input Inv	verted Enable bit	
	1 = Inverted MAI is connected 0 = Inverted MAI is not connected 1	•	
bit 7	NAGS: AND Gate Output Inv 1 = Inverted ANDI is connected 0 = Inverted ANDI is not connected	ed to OR gate	
bit 6	PAGS: AND Gate Output Ena 1 = ANDI is connected to OR 0 = ANDI is not connected to	gate	
bit 5	ACEN: AND Gate C Input En	able bit	
	1 = MCI is connected to AND 0 = MCI is not connected to A	•	
bit 4	ACNEN: AND Gate C Input In	nverted Enable bit	
	1 = Inverted MCI is connected 0 = Inverted MCI is not connected materials.	d to AND gate	
bit 3	ABEN: AND Gate B Input En		
	1 = MBI is connected to AND		
	0 = MBI is not connected to A	ND gate	

REGISTER 25-5: CMxMSKCON: COMPARATOR MASK GATING CONTROL REGISTER

bit 2

ABNEN: AND Gate B Input Inverted Enable bit

1 = Inverted MBI is connected to AND gate

0 = Inverted MBI is not connected to AND gate

bit 1

AAEN: AND Gate A Input Enable bit

1 = MAI is connected to AND gate

0 = MAI is not connected to AND gateAANEN: AND Gate A Input Inverted Enable bit

bit 0

1 = Inverted MAI is connected to AND gate0 = Inverted MAI is not connected to AND gate

REGISTER 25-6: CMxFLTR: COMPARATOR FILTER CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	I-O
_	_	_	_	_	_	_	_
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_		CFSEL<2:0>		CFLTREN		CFDIV<2:0>	
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'

bit 6-4 CFSEL<2:0>: Comparator Filter Input Clock Select bits

111 = T5CLK⁽¹⁾

110 = T4CLK(2)

101 = T3CLK(1)

100 = T2CLK(2)

011 = Reserved 010 = SYNCO1⁽³⁾

010 = SYNCOT $001 = FOSC^{(4)}$

 $000 = FP^{(4)}$

bit 3 **CFLTREN:** Comparator Filter Enable bit

1 = Digital filter enabled

0 = Digital filter disabled

bit 2-0 CFDIV<2:0>: Comparator Filter Clock Divide Select bits

111 = Clock Divide 1:128

110 = Clock Divide 1:64

101 = Clock Divide 1:32

100 = Clock Divide 1:16

011 = Clock Divide 1:8

010 = Clock Divide 1:4

001 = Clock Divide 1:2

000 = Clock Divide 1:1

Note 1: See the Type C Timer Block Diagram (Figure 13-2).

2: See the Type B Timer Block Diagram (Figure 13-1).

3: See the PWM Module Register Interconnect Diagram (Figure 16-2).

4: See the Oscillator System Diagram (Figure 9-1).

REGISTER 25-7: CVRCON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER

U-0	R/W-0	U-0	U-0	U-0	R/W-0	U-0	U-0
_	CVR20E ⁽¹⁾	_	_	_	VREFSEL	_	_
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CVREN	CVR10E ⁽¹⁾	CVRR	CVRSS		CVR-	<3:0>	
bit 7							bit 0

L	е	g	е	n	d	

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14 **CVR20E**: Comparator Voltage Reference 2 Output Enable bit⁽¹⁾

1 = (AVDD – AVSS)/2 is connected to the CVREF2O pin

0 = (AVDD - AVSS)/2 is disconnected from the CVREF2O pin

bit 13-11 **Unimplemented:** Read as '0'

bit 10 VREFSEL: Voltage Reference Select bit

1 = CVREFIN = VREF+

0 = CVREFIN is generated by the resistor network

bit 9-8 **Unimplemented:** Read as '0'

bit 7 **CVREN:** Comparator Voltage Reference Enable bit

1 = Comparator voltage reference circuit powered on0 = Comparator voltage reference circuit powered down

bit 6 **CVR10E**: Comparator Voltage Reference 1 Output Enable bit⁽¹⁾

1 = Voltage level is output on CVREF10 pin

0 = Voltage level is disconnected from CVREF10 pin

bit 5 CVRR: Comparator Voltage Reference Range Selection bit

1 = CVRSRC/24 step size

0 = CVRSRC/32 step size

bit 4 CVRSS: Comparator Voltage Reference Source Selection bit

1 = Comparator voltage reference source, CVRSRC = (VREF+) – (AVSS)

CVR<3:0> Comparator Voltage Reference Value Selection 0 ≤ CVR<3:0> ≤ 15 bits

0 = Comparator voltage reference source, CVRSRC = AVDD – AVSS

When CVRR = 1:

CVREFIN = (CVR<3:0>/24) • (CVRSRC)

When CVRR = 0:

CVREFIN = (CVRSRC/4) + (CVR<3:0>/32) • (CVRSRC)

Note 1: CVRxOE overrides the TRISx and the ANSELx bit settings.

bit 3-0

26.0 PROGRAMMABLE CYCLIC REDUNDANCY CHECK (CRC) GENERATOR

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 27. "Programmable Cyclic Redundancy Check (CRC)" (DS70346) of the "dsPIC33E/PIC24E Family Reference Manual", which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The programmable CRC generator offers the following features:

- User-programmable (up to 32nd order) polynomial CRC equation
- · Interrupt output
- Data FIFO

The programmable CRC generator provides a hardware-implemented method of quickly generating checksums for various networking and security applications. It offers the following features:

- User-programmable CRC polynomial equation, up to 32 bits
- Programmable shift direction (little or big-endian)
- · Independent data and polynomial lengths
- · Configurable Interrupt output
- Data FIFO

A simplified block diagram of the CRC generator is shown in Figure 26-1. A simple version of the CRC shift engine is shown in Figure 26-2.

FIGURE 26-1: CRC BLOCK DIAGRAM

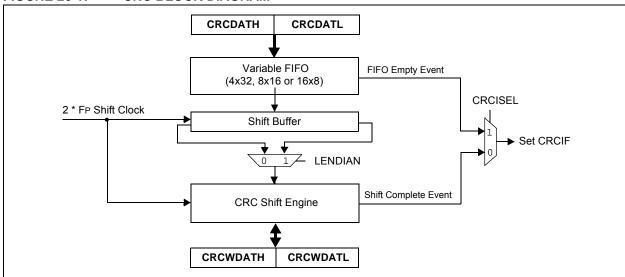
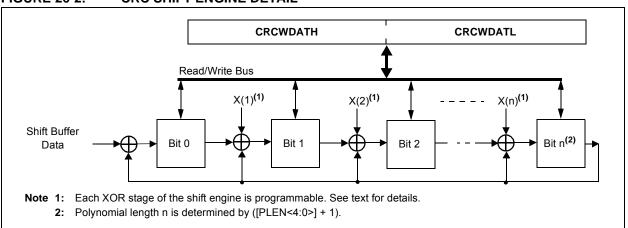


FIGURE 26-2: CRC SHIFT ENGINE DETAIL



26.1 Overview

The CRC module can be programmed for CRC polynomials of up to the 32nd order, using up to 32 bits. Polynomial length, which reflects the highest exponent in the equation, is selected by the PLEN<4:0> bits (CRCCON2<4:0>).

The CRCXORL and CRCXORH registers control which exponent terms are included in the equation. Setting a particular bit includes that exponent term in the equation; functionally, this includes an XOR operation on the corresponding bit in the CRC engine. Clearing the bit disables the XOR.

For example, consider two CRC polynomials, one a 16-bit equation and the other a 32-bit equation:

$$x16 + x12 + x5 + 1$$
 and
$$x32 + x26 + x23 + x22 + x16 + x12 + x11 + x10 + x8 + x7 + x5 + x4 + x2 + x + 1$$

To program these polynomials into the CRC generator, set the register bits as shown in Table 26-1.

Note that the appropriate positions are set to '1' to indicate that they are used in the equation (for example, X26 and X23). The 0 bit required by the equation is always XORed; thus, X0 is a don't care. For a polynomial of length N, it is assumed that the Nth bit will always be used, regardless of the bit setting. Therefore, for a polynomial length of 32, there is no 32nd bit in the CRCxOR register.

TABLE 26-1: CRC SETUP EXAMPLES FOR 16 AND 32-BIT POLYNOMIAL

CRC Control	Bit Va	Bit Values					
Bits	16-bit Polynomial	32-bit Polynomial					
PLEN<4:0>	01111	11111					
X<31:16>	0000 0000 0000 000x	0000 0100 1100 0001					
X<15:0>	0001 0000 0010 000x	0001 1101 1011 011x					

26.2 Programmable CRC Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter this URL in your browser:
http://www.microchip.com/wwwproducts/
Devices.aspx?dDocName=en555464

26.2.1 KEY RESOURCES

- Section 27. "Programmable Cyclic Redundancy Check (CRC)" (DS70346)
- · Code Samples
- Application Notes
- · Software Libraries
- Webinars
- All related dsPIC33E/PIC24E Family Reference Manuals Sections
- · Development Tools

26.3 Programmable CRC Registers

CRCCON1: CRC CONTROL REGISTER 1 REGISTER 26-1:

R/W-0	U-0	R/W-0	R-0	R-0	R-0	R-0	R-0
CRCEN	_	CSIDL			VWORD<4:0>	•	
bit 15							bit 8

R-0	R-1	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
CRCFUL	CRCMPT	CRCISEL	CRCGO	LENDIAN	_	_	_
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15 CRCEN: CRC Enable bit

1 = CRC module is enabled

0 = CRC module is disabled. All state machines, pointers, and CRCWDAT/CRCDAT are reset. Other SFRs are not reset.

Unimplemented: Read as '0' bit 14

CSIDL: CRC Stop in Idle Mode bit bit 13

1 = Discontinue module operation when device enters Idle mode

0 = Continue module operation in Idle mode

bit 12-8 VWORD<4:0>: Pointer Value bits

Indicates the number of valid words in the FIFO. Has a maximum value of 8 when PLEN<4:0>>7,

or 16 when PLEN<4:0> \leq 7.

bit 7 CRCFUL: FIFO Full bit

> 1 = FIFO is full 0 = FIFO is not full

bit 6 **CRCMPT:** FIFO Empty Bit

> 1 = FIFO is empty 0 = FIFO is not empty

bit 5 CRCISEL: CRC Interrupt Selection bit

1 = Interrupt on FIFO empty; final word of data is still shifting through CRC

0 = Interrupt on shift complete and CRCWDAT results ready

bit 4 CRCGO: Start CRC bit

1 = Start CRC serial shifter

0 = CRC serial shifter is turned off

bit 3 **LENDIAN:** Data Word Little-Endian Configuration bit

1 = Data word is shifted into the CRC starting with the LSb (little endian)

0 = Data word is shifted into the CRC starting with the MSb (big endian)

Unimplemented: Read as '0' bit 2-0

REGISTER 26-2: CRCCON2: CRC CONTROL REGISTER 2

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	_	_			DWIDTH<4:0>	•	
bit 15			_		_		bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	_	_			PLEN<4:0>		
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **DWIDTH<4:0>:** Data Width Select bits

These bits set the width of the data word (DWIDTH<4:0> + 1)

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 PLEN<4:0>: Polynomial Length Select bits

These bits set the length of the polynomial (Polynomial Length = PLEN<4:0> + 1)

REGISTER 26-3: CRCXORH: CRC XOR POLYNOMIAL HIGH REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
X<31:24>								
bit 15							bit 8	

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
X<23:16>									
bit 7							bit 0		

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 X<31:16>: XOR of Polynomial Term Xⁿ Enable bits

REGISTER 26-4: CRCXORL: CRC XOR POLYNOMIAL LOW REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
	X<15:8>										
bit 15							bit 8				

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
			X<7:1>				_
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-1 X<15:1>: XOR of Polynomial Term Xⁿ Enable bits

bit 0 Unimplemented: Read as '0'

27.0 SPECIAL FEATURES

Note: This data sheet summarizes the features of dsPIC33EPXXXGP50X. dsPIC33EPXXXMC20X/50X. and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the "dsPIC33E/PIC24E Family Reference Manual', which is available from the Microchip web site (www.microchip.com).

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X devices include several features intended to maximize application flexibility and reliability, and minimize cost through elimination of external components. These are:

- · Flexible configuration
- · Watchdog Timer (WDT)
- Code Protection and CodeGuard™ Security
- JTAG Boundary Scan Interface
- In-Circuit Serial Programming™ (ICSP™)
- In-Circuit Emulation

27.1 Configuration Bits

In dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X devices, the configuration bytes are implemented as volatile memory. This means that configuration data must be programmed each time the device is powered up. Configuration data is stored in at the top of the on-chip program memory space, known as the Flash Configuration Bytes. Their specific locations are shown in Table 27-1. The configuration data is automatically loaded from the Flash Configuration Bytes to the proper Configuration shadow registers during device Resets.

Note: Configuration data is reloaded on all types of device Resets.

When creating applications for these devices, users should always specifically allocate the location of the Flash Configuration Bytes for configuration data in their code for the compiler. This is to make certain that program code is not stored in this address when the code is compiled.

The upper 2 bytes of all Flash Configuration Words in program memory should always be '1111 1111 1111 1111 1111'. This makes them appear to be NOP instructions in the remote event that their locations are ever executed by accident. Since Configuration bits are not implemented in the corresponding locations, writing '1's to these locations has no effect on device operation.

Note: Performing a page erase operation on the last page of program memory clears the Flash Configuration Bytes, enabling code protection as a result. Therefore, users should avoid performing page erase operations on the last page of program memory.

The Configuration Flash Bytes map is shown in Table 27-1.

TABLE 27-1: CONFIGURATION BYTE REGISTER MAP

File Name	Address	Bit 23-8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	0057EC ⁽¹⁾									
	00AFEC ⁽²⁾					_	_	_		_
	0157EC ⁽³⁾	_	_	_	_				_	
	02AFEC ⁽⁴⁾									
Reserved	0057EE ⁽¹⁾									
	00AFEE ⁽²⁾									
	0157EE ⁽³⁾	_	_	_	_	_	_	_	_	_
	02AFEE ⁽⁴⁾									
FICD	0057F0 ⁽¹⁾									
	00AFF0 ⁽²⁾				ITAOFNI	D(6)	D		100	.4.0:
	0157F0 ⁽³⁾	_	Reserved ⁽⁷⁾	_	JTAGEN	Reserved ⁽⁶⁾	Reserved ⁽⁷⁾	_	ICS<	:1:0>
	02AFF0 ⁽⁴⁾									
FPOR	0057F2 ⁽¹⁾									
	00AFF2 ⁽²⁾		MOTA	/INI	ALTIOCO	A1 T1004	_			_
	0157F2 ⁽³⁾	_	WDIW	/IN<1:0>	ALTI2C2	ALTI2C1		_	_	
	02AFF2 ⁽⁴⁾									
FWDT	0057F4 ⁽¹⁾									
	00AFF4 ⁽²⁾		EMPTEN	MANDIO	DLLKEN	WOTODE		WDTDO	WDTPOST<3:0>	
	0157F4 ⁽³⁾	_	FWDTEN	WINDIS	PLLKEN	WDTPRE		WDTPO	51<3:0>	
	02AFF4 ⁽⁴⁾									
FOSC	0057F6 ⁽¹⁾									
	00AFF6 ⁽²⁾		FOKO	M 44.05	101 414/41/			OCCIOENO	DOCON	ID 44.05
	0157F6 ⁽³⁾	_	FCKS	M<1:0>	IOL1WAY	_	_	OSCIOFNC	POSCM	ID<1:0>
	02AFF6 ⁽⁴⁾									
FOSCSEL	0057F8 ⁽¹⁾									
	00AFF8 ⁽²⁾		IESO	DWM 00K(5)					ENOCO ZOIOS	
	0157F8 ⁽³⁾	_	IESO	PWMLOCK ⁽⁵⁾	_	_	_		FNOSC<2:0>	
	02AFF8 ⁽⁴⁾									
FGS	0057FA ⁽¹⁾									
	00AFFA ⁽²⁾								CCB	GWRP
	0157FA ⁽³⁾	_	_	_	_	_	_	_	GCP	GWKP
	02AFFA ⁽⁴⁾									
Reserved	0057FC ⁽¹⁾									
	00AFFC ⁽²⁾									
	0157FC ⁽³⁾	_	_	_	_	_	_	_	_	_
	02AFFC ⁽⁴⁾									
Reserved	057FFE ⁽¹⁾			_						
	00AFFE ⁽²⁾									
	0157FE ⁽³⁾	_	_	_	_	_	_	_	_	_
	02AFFE ⁽⁴⁾									

Legend:

- Note
- = unimplemented, read as '1'.

 Address for dsPIC33EP32GP/MC50X, dsPIC33EP32MC20X, and PIC24EP32GP/MC20X devices.

 Address for dsPIC33EP64GP/MC50X, dsPIC33EP64MC20X, and PIC24EP64GP/MC20X devices.
 - Address for dsPIC33EP128GP/MC50X, dsPIC33EP128MC20X, and PIC24EP128GP/MC20X devices.
 - Address for dsPIC33EP256GP/MC50X, dsPIC33EP256MC20X, and PIC24EP256GP/MC20X devices. These bits are only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.
 - This bit is reserved and must be programmed as '0'.
 - This bit is reserved and must be programmed as '1'.

TABLE 27-2: CONFIGURATION BITS DESCRIPTION

Bit Field	Description
GCP	General Segment Code-Protect bit
	1 = User program memory is not code-protected
	0 = Code protection is enabled for the entire program memory space
GWRP	General Segment Write-Protect bit
	1 = User program memory is not write-protected
	0 = User program memory is write-protected
IESO	Two-speed Oscillator Start-up Enable bit
	1 = Start-up device with FRC, then automatically switch to the
	user-selected oscillator source when ready
	0 = Start-up device with user-selected oscillator source
PWMLOCK ⁽¹⁾	PWM Lock Enable bit
	1 = Certain PWM registers may only be written after key sequence
	0 = PWM registers may be written without key
FNOSC<2:0>	Oscillator Selection bits
	111 = Fast RC Oscillator with divide-by-N (FRCDIVN)
	110 = Reserved; do not use
	101 = Low-Power RC Oscillator (LPRC)
	100 = Reserved; do not use
	011 = Primary Oscillator with PLL module (XT + PLL, HS + PLL, EC + PLL)
	010 = Primary Oscillator (XT, HS, EC)
	001 = Fast RC Oscillator with divide-by-N with PLL module (FRCPLL)
	000 = Fast RC Oscillator (FRC)
FCKSM<1:0>	Clock Switching Mode bits
	1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled
	01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled
	00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled
IOL1WAY	Peripheral pin select configuration
	1 = Allow only one reconfiguration
	0 = Allow multiple reconfigurations
OSCIOFNC	OSC2 Pin Function bit (except in XT and HS modes)
	1 = OSC2 is clock output
	0 = OSC2 is general purpose digital I/O pin
POSCMD<1:0>	Primary Oscillator Mode Select bits
	11 = Primary oscillator disabled
	10 = HS Crystal Oscillator mode
	01 = XT Crystal Oscillator mode
	00 = EC (External Clock) mode
FWDTEN	Watchdog Timer Enable bit
	1 = Watchdog Timer always enabled (LPRC oscillator cannot be disabled. Clearing the
	SWDTEN bit in the RCON register will have no effect.)
	0 = Watchdog Timer enabled/disabled by user software (LPRC can be disabled by clearing
	the SWDTEN bit in the RCON register)
WINDIS	Watchdog Timer Window Enable bit
	1 = Watchdog Timer in Non-Window mode
51117511	0 = Watchdog Timer in Window mode
PLLKEN	PLL Lock Enable bit
	1 = PLL lock enabled
	0 = PLL lock disabled
WDTPRE	Watchdog Timer Prescaler bit
	1 = 1:128
	0 = 1:32

Note 1: This bit is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

TABLE 27-2: CONFIGURATION BITS DESCRIPTION (CONTINUED)

Bit Field	Description
WDTPOST<3:0>	Watchdog Timer Postscaler bits 1111 = 1:32,768 1110 = 1:16,384
WDTWIN<1:0>	Watchdog Window Select bits 11 = WDT Window is 25% of WDT period 10 = WDT Window is 37.5% of WDT period 01 = WDT Window is 50% of WDT period 00 = WDT Window is 75% of WDT period
ALTI2C1	Alternate I^2C1 pins 1 = I^2C1 mapped to SDA1/SCL1 pins 0 = I^2C1 mapped to ASDA1/ASCL1 pins
ALTI2C2	Alternate I^2C2 pins 1 = I^2C2 mapped to SDA2/SCL2 pins 0 = I^2C2 mapped to ASDA2/ASCL2 pins
JTAGEN	JTAG Enable bit 1 = JTAG enabled 0 = JTAG disabled
ICS<1:0>	ICD Communication Channel Select bits 11 = Communicate on PGEC1 and PGED1 10 = Communicate on PGEC2 and PGED2 01 = Communicate on PGEC3 and PGED3 00 = Reserved, do not use

Note 1: This bit is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

REGISTER 27-1: DEVID: DEVICE ID REGISTER

R	R	R	R	R	R	R	R			
			DEVID-	<23:16>						
bit 23	bit 23 bit 16									
R	R	R	R	R	R	R	R			
			DEVID	<15:8>						
bit 15							bit 8			
R	R	R	R	R	R	R	R			
			DEVI	0<7:0>						
bit 7							bit 0			

Legend: R = Read-Only bit U = Unimplemented bit

bit 23-0 **DEVID<23:0>:** Device Identifier bits⁽¹⁾

Note 1: Refer to the "dsPIC33E/PIC24E Flash Programming Specification" (DS70619) for the list of device ID values.

REGISTER 27-2: DEVREV: DEVICE REVISION REGISTER

R	R	R	R	R	R	R	R				
			DEVREV	/<23:16>							
bit 23	bit 23 bit										
R	R	R	R	R	R	R	R				
			DEVRE'	V<15:8>							
bit 15							bit 8				
R	R	R	R	R	R	R	R				
	DEVREV<7:0>										
bit 7							bit 0				

Legend: R = Read-only bit U = Unimplemented bit

bit 23-0 **DEVREV<23:0>:** Device Revision bits⁽¹⁾

Note 1: Refer to the "dsPIC33E/PIC24E Flash Programming Specification" (DS70619) for the list of device revision values.

27.2 User ID Words

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X devices contain four User ID Words, located at addresses 0x800FF8 through 0x800FFE. The User ID Words can be used for storing product information such as serial numbers, system manufacturing dates, manufacturing lot numbers and other application-specific information.

The User ID Words register map is shown in Table 27-3.

TABLE 27-3: USER ID WORDS REGISTER MAP

File Name	Address	Bit 23-16	Bit 15-0
FUID0	0x800FF8	_	UID0
FUID1	0x800FFA	_	UID1
FUID2	0x800FFC	_	UID2
FUID3	0x800FFE	_	UID3

Legend: — = unimplemented, read as '1'.

27.3 On-Chip Voltage Regulator

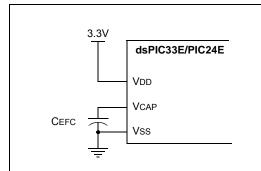
All of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X devices power their core digital logic at a nominal 1.8V. This can create a conflict for designs that are required to operate at a higher typical voltage, such as 3.3V. To simplify system design, all devices in the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X family incorporate an onchip regulator that allows the device to run its core logic from VDD.

The regulator provides power to the core from the other VDD pins. A low-ESR (less than 1 Ohm) capacitor (such as tantalum or ceramic) must be connected to the VCAP pin (Figure 27-1). This helps to maintain the stability of the regulator. The recommended value for the filter capacitor is provided in Table 30-5 located in Section 30.0 "Electrical Characteristics".

Note:

It is important for the low-ESR capacitor to be placed as close as possible to the VCAP pin.

FIGURE 27-1: CONNECTIONS FOR THE ON-CHIP VOLTAGE REGULATOR^(1,2,3)



- Note 1: These are typical operating voltages. Refer to Table 30-5 located in Section 30.1 "DC Characteristics" for the full operating ranges of VDD and VCAP.
 - 2: It is important for the low-ESR capacitor to be placed as close as possible to the VCAP pin.
 - **3:** Typical VCAP pin voltage = 1.8V when VDD ≥ VDDMIN.

27.4 Brown-out Reset (BOR)

The Brown-out Reset (BOR) module is based on an internal voltage reference circuit that monitors the regulated supply voltage VCAP. The main purpose of the BOR module is to generate a device Reset when a brown-out condition occurs. Brown-out conditions are generally caused by glitches on the AC mains (for example, missing portions of the AC cycle waveform due to bad power transmission lines, or voltage sags due to excessive current draw when a large inductive load is turned on).

A BOR generates a Reset pulse, which resets the device. The BOR selects the clock source, based on the device Configuration bit values (FNOSC<2:0> and POSCMD<1:0>).

If an oscillator mode is selected, the BOR activates the Oscillator Start-up Timer (OST). The system clock is held until OST expires. If the PLL is used, the clock is held until the LOCK bit (OSCCON<5>) is '1'.

Concurrently, the PWRT time-out (TPWRT) is applied before the internal Reset is released. If TPWRT = 0 and a crystal oscillator is being used, then a nominal delay of TFSCM is applied. The total delay in this case is TFSCM. Refer to parameter SY35 in Table 30-24 of Section 30.0 "Electrical Characteristics" for specific TFSCM values.

The BOR Status bit (RCON<1>) is set to indicate that a BOR has occurred. The BOR circuit, continues to operate while in Sleep or Idle modes and resets the device should VDD fall below the BOR threshold voltage.

27.5 Watchdog Timer (WDT)

For dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X devices, the WDT is driven by the LPRC oscillator. When the WDT is enabled, the clock source is also enabled.

27.5.1 PRESCALER/POSTSCALER

The nominal WDT clock source from LPRC is 32 kHz. This feeds a prescaler that can be configured for either 5-bit (divide-by-32) or 7-bit (divide-by-128) operation. The prescaler is set by the WDTPRE Configuration bit. With a 32 kHz input, the prescaler yields a WDT timeout period (TWDT), as shown in parameter SY12 in Table 30-24.

A variable postscaler divides down the WDT prescaler output and allows for a wide range of time-out periods. The postscaler is controlled by the WDTPOST<3:0> Configuration bits (FWDT<3:0>), which allow the selection of 16 settings, from 1:1 to 1:32,768. Using the prescaler and postscaler, time-out periods ranging from 1 ms to 131 seconds can be achieved.

The WDT, prescaler and postscaler are reset:

- · On any device Reset
- On the completion of a clock switch, whether invoked by software (i.e., setting the OSWEN bit after changing the NOSC bits) or by hardware (i.e., Fail-Safe Clock Monitor)
- When a PWRSAV instruction is executed (i.e., Sleep or Idle mode is entered)
- When the device exits Sleep or Idle mode to resume normal operation
- By a CLRWDT instruction during normal execution

Note: The CLRWDT and PWRSAV instructions clear the prescaler and postscaler counts when executed.

27.5.2 SLEEP AND IDLE MODES

If the WDT is enabled, it continues to run during Sleep or Idle modes. When the WDT time-out occurs, the device wakes the device and code execution continues from where the PWRSAV instruction was executed. The corresponding SLEEP or IDLE bits (RCON<3,2>) needs to be cleared in software after the device wakes up.

27.5.3 ENABLING WDT

The WDT is enabled or disabled by the FWDTEN Configuration bit in the FWDT Configuration register. When the FWDTEN Configuration bit is set, the WDT is always enabled.

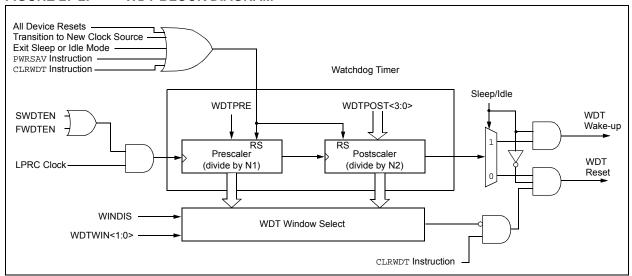
The WDT can be optionally controlled in software when the FWDTEN Configuration bit has been programmed to '0'. The WDT is enabled in software by setting the SWDTEN control bit (RCON<5>). The SWDTEN control bit is cleared on any device Reset. The software WDT option allows the user application to enable the WDT for critical code segments and disable the WDT during non-critical segments for maximum power savings.

The WDT flag bit, WDTO (RCON<4>), is not automatically cleared following a WDT time-out. To detect subsequent WDT events, the flag must be cleared in software.

27.5.4 WDT WINDOW

The Watchdog Timer has an optional Windowed mode enabled by programming the WINDIS bit in the WDT configuration register (FWDT<6>). In the Windowed mode (WINDIS = 0), the WDT should be cleared based on the settings in the programmable watchdog window select bits (WDTWIN<1:0>).

FIGURE 27-2: WDT BLOCK DIAGRAM



27.6 JTAG Interface

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X devices implement a JTAG interface, which supports boundary scan device testing. Detailed information on this interface is provided in future revisions of the document.

Note: Refer to Section 24. "Programming and Diagnostics" (DS70608) of the "dsPIC33E/PIC24E Family Reference Manual" for further information on usage, configuration and operation of the JTAG interface.

27.7 In-Circuit Serial Programming

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X devices can be serially programmed while in the end application circuit. This is done with two lines for clock and data and three other lines for power, ground and the programming sequence. Serial programming allows customers to manufacture boards with unprogrammed devices and then program the device just before shipping the product. Serial programming also allows the most recent firmware or a custom firmware to be programmed. Refer to the "dsPIC33E/PIC24E Flash Programming Specification" (DS70619) for details about In-Circuit Serial Programming (ICSP).

Any of the three pairs of programming clock/data pins can be used:

- PGEC1 and PGED1
- · PGEC2 and PGED2
- · PGEC3 and PGED3

27.8 In-Circuit Debugger

When MPLAB[®] ICD 3 or REAL ICE™ is selected as a debugger, the in-circuit debugging functionality is enabled. This function allows simple debugging functions when used with MPLAB IDE. Debugging functionality is controlled through the PGECx (Emulation/Debug Clock) and PGEDx (Emulation/Debug Data) pin functions.

Any of the three pairs of debugging clock/data pins can be used:

- PGEC1 and PGED1
- PGEC2 and PGED2
- · PGEC3 and PGED3

To use the in-circuit debugger function of the device, the design must implement ICSP connections to MCLR, VDD, VSS, and the PGECx/PGEDx pin pair. In addition, when the feature is enabled, some of the resources are not available for general use. These resources include the first 80 bytes of data RAM and two I/O pins (PGECx and PGEDx).

27.9 Code Protection and CodeGuard™ Security

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X devices offer basic implementation of CodeGuard Security that supports only General Segment (GS) security. This feature helps protect individual Intellectual Property.

Note: Refer to Section 23. "CodeGuard™ Security" (DS70634) of the "dsPlC33E/PlC24E Family Reference Manual" for further information on usage, configuration and operation of CodeGuard Security.

28.0 INSTRUCTION SET SUMMARY

Note: This data sheet summarizes the features of dsPIC33EPXXXGP50X. dsPIC33EPXXXMC20X/50X. and PIC24EPXXXGP/MC20X families οf devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the "dsPIC33E/PIC24E Family Reference Manual', which is available from the Microchip web site (www.microchip.com).

The dsPIC33EP instruction set is almost identical to that of the dsPIC30F and dsPIC33F. The PIC24EP instruction set is almost identical to that of the PIC24F and PIC24H.

Most instructions are a single program memory word (24 bits). Only three instructions require two program memory locations.

Each single-word instruction is a 24-bit word, divided into an 8-bit opcode, which specifies the instruction type and one or more operands, which further specify the operation of the instruction.

The instruction set is highly orthogonal and is grouped into five basic categories:

- · Word or byte-oriented operations
- · Bit-oriented operations
- · Literal operations
- · DSP operations
- · Control operations

Table 28-1 lists the general symbols used in describing the instructions.

The dsPIC33E instruction set summary in Table 28-2 lists all the instructions, along with the status flags affected by each instruction.

Most word or byte-oriented W register instructions (including barrel shift instructions) have three operands:

- The first source operand, which is typically a register 'Wb' without any address modifier
- The second source operand, which is typically a register 'Ws' with or without an address modifier
- The destination of the result, which is typically a register 'Wd' with or without an address modifier

However, word or byte-oriented file register instructions have two operands:

- · The file register specified by the value 'f'
- The destination, which could be either the file register 'f' or the W0 register, which is denoted as 'WREG'

Most bit-oriented instructions (including simple rotate/shift instructions) have two operands:

- The W register (with or without an address modifier) or file register (specified by the value of 'Ws' or 'f')
- The bit in the W register or file register (specified by a literal value or indirectly by the contents of register 'Wb')

The literal instructions that involve data movement can use some of the following operands:

- A literal value to be loaded into a W register or file register (specified by 'k')
- The W register or file register where the literal value is to be loaded (specified by 'Wb' or 'f')

However, literal instructions that involve arithmetic or logical operations use some of the following operands:

- The first source operand, which is a register 'Wb' without any address modifier
- The second source operand, which is a literal value
- The destination of the result (only if not the same as the first source operand), which is typically a register 'Wd' with or without an address modifier

The MAC class of DSP instructions can use some of the following operands:

- The accumulator (A or B) to be used (required operand)
- The W registers to be used as the two operands
- The X and Y address space prefetch operations
- The X and Y address space prefetch destinations
- · The accumulator write back destination

The other DSP instructions do not involve any multiplication and can include:

- · The accumulator to be used (required)
- The source or destination operand (designated as Wso or Wdo, respectively) with or without an address modifier
- The amount of shift specified by a W register 'Wn' or a literal value

The control instructions can use some of the following operands:

- · A program memory address
- The mode of the table read and table write instructions

Most instructions are a single word. Certain double-word instructions are designed to provide all the required information in these 48 bits. In the second word, the 8 MSbs are '0's. If this second word is executed as an instruction (by itself), it executes as a NOP.

The double-word instructions execute in two instruction cycles.

Most single-word instructions are executed in a single instruction cycle, unless a conditional test is true, or the program counter is changed as a result of the instruction, or a PSV or table read is performed. In these cases, the execution takes multiple instruction cycles

with the additional instruction cycle(s) executed as a NOP. Certain instructions that involve skipping over the subsequent instruction require either two or three cycles if the skip is performed, depending on whether the instruction being skipped is a single-word or two-word instruction. Moreover, double-word moves require two cycles.

Note: For more details on the instruction set, refer to the "16-bit MCU and DSC Programmer's Reference Manual" (DS70157).

TABLE 28-1: SYMBOLS USED IN OPCODE DESCRIPTIONS

Field	Description
#text	Means literal defined by "text"
(text)	Means "content of text"
[text]	Means "the location addressed by text"
{}	Optional field or operation
$a \in \{b, c, d\}$	a is selected from the set of values b, c, d
<n:m></n:m>	Register bit field
.b	Byte mode selection
.d	Double-Word mode selection
.S	Shadow register select
.W	Word mode selection (default)
Acc	One of two accumulators {A, B}
AWB	Accumulator write back destination address register ∈ {W13, [W13]+ = 2}
bit4	4-bit bit selection field (used in word addressed instructions) ∈ {015}
C, DC, N, OV, Z	MCU Status bits: Carry, Digit Carry, Negative, Overflow, Sticky Zero
Expr	Absolute address, label or expression (resolved by the linker)
f	File register address ∈ {0x00000x1FFF}
lit1	1-bit unsigned literal ∈ {0,1}
lit4	4-bit unsigned literal ∈ {015}
lit5	5-bit unsigned literal ∈ {031}
lit8	8-bit unsigned literal ∈ {0255}
lit10	10-bit unsigned literal ∈ {0255} for Byte mode, {0:1023} for Word mode
lit14	14-bit unsigned literal ∈ {016384}
lit16	16-bit unsigned literal ∈ {065535}
lit23	23-bit unsigned literal ∈ {08388608}; LSb must be '0'
None	Field does not require an entry, can be blank
OA, OB, SA, SB	DSP Status bits: ACCA Overflow, ACCB Overflow, ACCA Saturate, ACCB Saturate
PC	Program Counter
Slit10	10-bit signed literal ∈ {-512511}
Slit16	16-bit signed literal ∈ {-3276832767}
Slit6	6-bit signed literal ∈ {-1616}
Wb	Base W register ∈ {W0W15}
Wd	Destination W register ∈ { Wd, [Wd], [Wd++], [Wd], [++Wd], [Wd] }
Wdo	Destination W register ∈ { Wnd, [Wnd], [Wnd++], [Wnd], [++Wnd], [Wnd], [Wnd+Wb] }
Wm,Wn	Dividend, Divisor working register pair (direct addressing)

TABLE 28-1: SYMBOLS USED IN OPCODE DESCRIPTIONS (CONTINUED)

Field	Description
Wm*Wm	Multiplicand and Multiplier working register pair for Square instructions ∈ {W4 * W4,W5 * W5,W6 * W6,W7 * W7}
Wm*Wn	Multiplicand and Multiplier working register pair for DSP instructions ∈ {W4 * W5,W4 * W6,W4 * W7,W5 * W6,W5 * W7,W6 * W7}
Wn	One of 16 working registers ∈ {W0W15}
Wnd	One of 16 destination working registers ∈ {W0W15}
Wns	One of 16 source working registers ∈ {W0W15}
WREG	W0 (working register used in file register instructions)
Ws	Source W register ∈ { Ws, [Ws], [Ws++], [Ws], [++Ws], [Ws] }
Wso	Source W register ∈ { Wns, [Wns++], [Wns], [++Wns], [Wns], [Wns+Wb] }
Wx	X data space prefetch address register for DSP instructions ∈ {[W8] + = 6, [W8] + = 4, [W8] + = 2, [W8], [W8] - = 6, [W8] - = 4, [W8] - = 2, [W9] + = 6, [W9] + = 4, [W9] + = 2, [W9], [W9] - = 6, [W9] - = 4, [W9] - = 2, [W9 + W12], none}
Wxd	X data space prefetch destination register for DSP instructions ∈ {W4W7}
Wy	Y data space prefetch address register for DSP instructions ∈ {[W10] + = 6, [W10] + = 4, [W10] + = 2, [W10], [W10] - = 6, [W10] - = 4, [W10] - = 2, [W11] + = 6, [W11] + = 4, [W11] + = 2, [W11], [W11] - = 6, [W11] - = 4, [W11] - = 2, [W11 + W12], none}
Wyd	Y data space prefetch destination register for DSP instructions ∈ {W4W7}

TABLE 28-2: INSTRUCTION SET OVERVIEW

Base Instr	Assembly Mnemonic		Assembly Syntax	Description	# of Words	# of Cycles	Status Flags Affected
1	ADD	ADD	Acc ⁽¹⁾	Add Accumulators	1	1	OA,OB,SA,S B
		ADD	f	f = f + WREG	1	1	C,DC,N,OV,Z
		ADD	f,WREG	WREG = f + WREG	1	1	C,DC,N,OV,Z
		ADD	#lit10,Wn	Wd = lit10 + Wd	1	1	C,DC,N,OV,Z
		ADD	Wb, Ws, Wd	Wd = Wb + Ws	1	1	C,DC,N,OV,Z
		ADD	Wb,#lit5,Wd	Wd = Wb + lit5	1	1	C,DC,N,OV,Z
		ADD	Wso,#Slit4,Acc	16-bit Signed Add to Accumulator	1	1	OA,OB,SA,S B
2	ADDC	ADDC	f	f = f + WREG + (C)	1	1	C,DC,N,OV,Z
		ADDC	f,WREG	WREG = f + WREG + (C)	1	1	C,DC,N,OV,Z
		ADDC	#lit10,Wn	Wd = lit10 + Wd + (C)	1	1	C,DC,N,OV,Z
		ADDC	Wb, Ws, Wd	Wd = Wb + Ws + (C)	1	1	C,DC,N,OV,Z
		ADDC	Wb,#lit5,Wd	Wd = Wb + lit5 + (C)	1	1	C,DC,N,OV,Z
3	AND	AND	f	f = f.AND. WREG	1	1	N,Z
		AND	f,WREG	WREG = f .AND. WREG	1	1	N,Z
		AND	#lit10,Wn	Wd = lit10 .AND. Wd	1	1	N,Z
		AND	Wb, Ws, Wd	Wd = Wb .AND. Ws	1	1	N,Z
		AND	Wb,#lit5,Wd	Wd = Wb .AND. lit5	1	1	N,Z
4	ASR	ASR	f	f = Arithmetic Right Shift f	1	1	C,N,OV,Z
•	ribit	ASR	f,WREG	WREG = Arithmetic Right Shift f	1	1	C,N,OV,Z
		ASR	Ws, Wd	Wd = Arithmetic Right Shift Ws	1	1	C,N,OV,Z
		ASR	Wb, Wns, Wnd	Wnd = Arithmetic Right Shift Wb by Wns	1	1	N,Z
		ASR	Wb,#lit5,Wnd	Wnd = Arithmetic Right Shift Wb by lit5	1	1	N,Z
5	BCLR	BCLR	f,#bit4	Bit Clear f	1	1	None
	DCLIK	BCLR	Ws,#bit4	Bit Clear Ws	1	1	None
6	BRA	BRA	C,Expr	Branch if Carry	1	1 (4)	None
	DICA	BRA	GE, Expr	Branch if greater than or equal	1	1 (4)	None
		BRA	GEU, Expr	Branch if unsigned greater than or equal	1	1 (4)	None
		BRA	GT, Expr	Branch if greater than	1	1 (4)	None
		BRA	GTU, Expr	Branch if unsigned greater than	1	1 (4)	None
		BRA	LE, Expr	Branch if less than or equal	1	1 (4)	None
		BRA	LEU, Expr	Branch if unsigned less than or equal	1	1 (4)	None
		BRA	LT, Expr	Branch if less than	1	1 (4)	None
		BRA	LTU, Expr	Branch if unsigned less than	1	1 (4)	None
		BRA	N,Expr	Branch if Negative	1	1 (4)	None
		BRA	NC, Expr	Branch if Not Carry	1	1 (4)	None
		BRA	NN,Expr	Branch if Not Negative	1	1 (4)	None
		BRA		Branch if Not Overflow	1	1 (4)	None
		BRA	NOV, Expr	Branch if Not Zero	1	1 (4)	None
			NZ, Expr OA, Expr(1)	Branch if Accumulator A overflow	1	1 (4)	None
		BRA	OB, Expr(1)	Branch if Accumulator B overflow	1		None
		BRA	OV, Expr(1)	Branch if Overflow	1	1 (4)	
		BRA	SA, Expr ⁽¹⁾	Branch if Accumulator A saturated	1	1 (4)	None None
		BRA	SB, Expr(1)	Branch if Accumulator A saturated Branch if Accumulator B saturated	1	1 (4)	None
			Expr	Branch Unconditionally	1	4	None
		BRA		Branch if Zero	1	1 (4)	None
		BRA	Z,Expr	Computed Branch	1	4	None
7	BSET	BRA	Wn f #bi+4	Bit Set f	1	1	None
1	DOET	BSET	f,#bit4	Bit Set Ws	1	1	None
		L DO BILL	Ws,#bit4	חוו סבו אוס	1 1		None
8	BSW	BSW.C	Ws,Wb	Write C bit to Ws <wb></wb>	1	1	None

Note 1: This instruction is available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic		Assembly Syntax	Description	# of Words	# of Cycles	Status Flags Affected
9	BTG	BTG	f,#bit4	Bit Toggle f	1	1	None
		BTG	Ws,#bit4	Bit Toggle Ws	1	1	None
10	BTSC	BTSC	f,#bit4	Bit Test f, Skip if Clear	1	1 (2 or 3)	None
		BTSC	Ws,#bit4	Bit Test Ws, Skip if Clear	1	1 (2 or 3)	None
11	BTSS	BTSS	f,#bit4	Bit Test f, Skip if Set	1	1 (2 or 3)	None
		BTSS	Ws,#bit4	Bit Test Ws, Skip if Set	1	1 (2 or 3)	None
12	BTST	BTST	f,#bit4	Bit Test f	1	1	Z
		BTST.C	Ws,#bit4	Bit Test Ws to C	1	1	С
		BTST.Z	Ws,#bit4	Bit Test Ws to Z	1	1	Z
		BTST.C	Ws,Wb	Bit Test Ws <wb> to C</wb>	1	1	С
		BTST.Z	Ws,Wb	Bit Test Ws <wb> to Z</wb>	1	1	Z
13	BTSTS	BTSTS	f,#bit4	Bit Test then Set f	1	1	Z
		BTSTS.C	Ws,#bit4	Bit Test Ws to C, then Set	1	1	С
		BTSTS.Z	Ws,#bit4	Bit Test Ws to Z, then Set	1	1	Z
14	CALL	CALL	lit23	Call subroutine	2	4	SFA
		CALL	Wn	Call indirect subroutine	1	4	SFA
		CALL.L	Wn	Call indirect subroutine (long address)	1	4	SFA
15	CLR	CLR	f	f = 0x0000	1	1	None
		CLR	WREG	WREG = 0x0000	1	1	None
		CLR	Ws	Ws = 0x0000	1	1	None
		CLR	Acc, Wx, Wxd, Wy, Wyd, AWB ⁽¹⁾	Clear Accumulator	1	1	OA,OB,SA,S B
16	CLRWDT	CLRWDT		Clear Watchdog Timer	1	1	WDTO,Sleep
17	COM	COM	f	f = f	1	1	N,Z
		COM	f,WREG	WREG = f	1	1	N,Z
		COM	Ws,Wd	$Wd = \overline{Ws}$	1	1	N,Z
18	CP	CP	f	Compare f with WREG	1	1	C,DC,N,OV,Z
		CP	Wb,#lit8	Compare Wb with lit8	1	1	C,DC,N,OV,Z
		CP	Wb,Ws	Compare Wb with Ws (Wb – Ws)	1	1	C,DC,N,OV,Z
19	CP0	CP0	f	Compare f with 0x0000	1	1	C,DC,N,OV,Z
		CP0	Ws	Compare Ws with 0x0000	1	1	C,DC,N,OV,Z
20	CPB	CPB	f	Compare f with WREG, with Borrow	1	1	C,DC,N,OV,Z
		CPB	Wb,#lit8	Compare Wb with lit8, with Borrow	1	1	C,DC,N,OV,Z
		CPB	Wb,Ws	Compare Wb with Ws, with Borrow (Wb – Ws – \overline{C})	1	1	C,DC,N,OV,Z
21	CPSEQ	CPSEQ	Wb,Wn	Compare Wb with Wn, skip if =	1	1 (2 or 3)	None
	CPBEQ	CPBEQ	Wb,Wn,Expr	Compare Wb with Wn, branch if =	1	1 (5)	None
22	CPSGT	CPSGT	Wb,Wn	Compare Wb with Wn, skip if >	1	1 (2 or 3)	None
	CPBGT	CPBGT	Wb,Wn,Expr	Compare Wb with Wn, branch if >	1	1 (5)	None
23	CPSLT	CPSLT	Wb,Wn	Compare Wb with Wn, skip if <	1	1 (2 or 3)	None
	CPBLT	CPBLT	Wb,Wn,Expr	Compare Wb with Wn, branch if <	1	1 (5)	None
24	CPSNE	CPSNE	Wb,Wn	Compare Wb with Wn, skip if ≠	1	1 (2 or 3)	None
	CPBNE	CPBNE	Wb,Wn,Expr	Compare Wb with Wn, branch if ≠	1	1 (5)	None

Note 1: This instruction is available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic		Assembly Syntax	Description		# of Cycles	Status Flags Affected
25	DAW	DAW	Wn	Wn = decimal adjust Wn	1	1	С
26	DEC	DEC	f = f - 1		1	1	C,DC,N,OV,Z
		DEC	f,WREG	WREG = f - 1	1	1	C,DC,N,OV,Z
		DEC	Ws,Wd	Wd = Ws - 1	1	1	C,DC,N,OV,Z
27	DEC2	DEC2	f	f = f - 2	1	1	C,DC,N,OV,Z
		DEC2	f,WREG	WREG = f – 2	1	1	C,DC,N,OV,Z
		DEC2	Ws,Wd	Wd = Ws - 2	1	1	C,DC,N,OV,Z
28	DISI	DISI	#lit14	Disable Interrupts for k instruction cycles	1	1	None
29	DIV	DIV.S	Wm,Wn	Signed 16/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.SD	Wm,Wn	Signed 32/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.U	Wm,Wn	Unsigned 16/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.UD	Wm,Wn	Unsigned 32/16-bit Integer Divide	1	18	N,Z,C,OV
30	DIVF	DIVF	Wm, Wn ⁽¹⁾	Signed 16/16-bit Fractional Divide	1	18	N,Z,C,OV
31	DO	DO	#lit15,Expr ⁽¹⁾	Do code to PC + Expr, lit15 + 1 times	2	2	None
		DO	Wn, Expr ⁽¹⁾	Do code to PC + Expr, (Wn) + 1 times	2	2	None
32	ED	ED	Wm*Wm,Acc,Wx,Wy,Wxd ⁽¹⁾	Euclidean Distance (no accumulate)	1	1	OA,OB,OAB, SA,SB,SAB
33	EDAC	EDAC	Wm*Wm, Acc, Wx, Wy, Wxd ⁽¹⁾	Euclidean Distance	1	1	OA,OB,OAB, SA,SB,SAB
34	EXCH	EXCH	Wns, Wnd	Swap Wns with Wnd	1	1	None
35	FBCL	FBCL	Ws, Wnd	Find Bit Change from Left (MSb) Side		1	С
36	FF1L	FF1L	Ws, Wnd	Find First One from Left (MSb) Side		1	С
37	FF1R	FF1R	Ws, Wnd	Find First One from Right (LSb) Side	1	1	С
38	GOTO	GOTO	Expr	Go to address	2	4	None
		GOTO	Wn	Go to indirect	1	4	None
		GOTO.L	Wn	Go to indirect (long address)	1	4	None
39	INC	INC	f	f = f + 1	1	1	C,DC,N,OV,Z
		INC	f,WREG	WREG = f + 1	1	1	C,DC,N,OV,Z
		INC	Ws,Wd	Wd = Ws + 1	1	1	C,DC,N,OV,Z
40	INC2	INC2	f	f = f + 2	1	1	C,DC,N,OV,Z
		INC2	f,WREG	WREG = f + 2	1	1	C,DC,N,OV,Z
		INC2	Ws,Wd	Wd = Ws + 2	1	1	C,DC,N,OV,Z
41	IOR	IOR	f	f = f .IOR. WREG	1	1	N,Z
		IOR	f,WREG	WREG = f .IOR. WREG	1	1	N,Z
		IOR	#lit10,Wn	Wd = lit10 .IOR. Wd	1	1	N,Z
		IOR	Wb,Ws,Wd	Wd = Wb .IOR. Ws	1	1	N,Z
		IOR	Wb,#lit5,Wd	Wd = Wb .IOR. lit5	1	1	N,Z
42	LAC	LAC	Wso,#Slit4,Acc	Load Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
43	LNK	LNK	#lit14	Link Frame Pointer	1	1	SFA
44	LSR	LSR	f	f = Logical Right Shift f	1	1	C,N,OV,Z
		LSR	f,WREG	WREG = Logical Right Shift f	1	1	C,N,OV,Z
		LSR	Ws,Wd	Wd = Logical Right Shift Ws	1	1	C,N,OV,Z
		LSR	Wb, Wns, Wnd	Wnd = Logical Right Shift Wb by Wns	1	1	N,Z
		LSR	Wb,#lit5,Wnd	Wnd = Logical Right Shift Wb by lit5	1	1	N,Z
45	MAC	MAC	Wm*Wn, Acc, Wx, Wxd, Wy, Wyd, AWB ⁽¹⁾	Multiply and Accumulate	1	1	OA,OB,OAB, SA,SB,SAB
		MAC	Wm*Wm,Acc,Wx,Wxd,Wy,Wyd ⁽¹⁾	Square and Accumulate	1	1	OA,OB,OAB, SA,SB,SAB

Note 1: This instruction is available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic		Assembly Syntax Description		# of Words	# of Cycles	Status Flags Affected
46	MOV	MOV	f,Wn	Move f to Wn	1	1	None
		MOV	f	Move f to f	1	1	None
		MOV	f,WREG	Move f to WREG	1	1	None
		MOV	#lit16,Wn	Move 16-bit literal to Wn	1	1	None
		MOV.b	#lit8,Wn	Move 8-bit literal to Wn	1	1	None
		MOV	Wn,f	Move Wn to f	1	1	None
		MOV	Wso,Wdo	Move Ws to Wd	1	1	None
		MOV	WREG, f	Move WREG to f	1	1	None
		MOV.D	Wns,Wd	Move Double from W(ns):W(ns + 1) to Wd	1	2	None
		MOV.D	Ws, Wnd	Move Double from Ws to W(nd + 1):W(nd)	1	2	None
47	MOVPAG	MOVPAG	#lit10,DSRPAG	Move 10-bit literal to DSRPAG	1	1	None
		MOVPAG	#lit9,DSWPAG	Move 9-bit literal to DSWPAG	1	1	None
		MOVPAG	#lit8,TBLPAG	Move 8-bit literal to TBLPAG	1	1	None
		MOVPAGW	Ws, DSRPAG	Move Ws<9:0> to DSRPAG	1	1	None
		MOVPAGW	Ws, DSWPAG	Move Ws<8:0> to DSWPAG	1	1	None
		MOVPAGW	Ws, TBLPAG	Move Ws<7:0> to TBLPAG	1	1	None
48	MOVSAC	MOVSAC	Acc, Wx, Wxd, Wy, Wyd, AWB ⁽¹⁾	Prefetch and store accumulator	1	1	None
49	MPY	MPY	Wm*Wn,Acc,Wx,Wxd,Wy,Wyd ⁽¹⁾	Multiply Wm by Wn to Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
		MPY	Wm*Wm, Acc, Wx, Wxd, Wy, Wyd ⁽¹⁾	Square Wm to Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
50	MPY.N	MPY.N	Wm*Wn,Acc,Wx,Wxd,Wy,Wyd ⁽¹⁾	-(Multiply Wm by Wn) to Accumulator	1	1	None
51	MSC	MSC	Wm*Wm, Acc, Wx, Wxd, Wy, Wyd, AWB ⁽¹⁾	Multiply and Subtract from Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
52	MUL	MUL.SS	Wb, Ws, Wnd	{Wnd + 1, Wnd} = signed(Wb) * 1 signed(Ws)		1	None
		MUL.SS	Wb, Ws, Acc ⁽¹⁾	Accumulator = signed(Wb) * signed(Ws)	1	1	None
		MUL.SU	Wb, Ws, Wnd	{Wnd + 1, Wnd} = signed(Wb) * unsigned(Ws)	1	1	None
		MUL.SU	Wb, Ws, Acc ⁽¹⁾	Accumulator = signed(Wb) * unsigned(Ws)	1	1	None
		MUL.SU	Wb,#lit5,Acc ⁽¹⁾	Accumulator = signed(Wb) * unsigned(lit5)	1	1	None
		MUL.US	Wb,Ws,Wnd	{Wnd + 1, Wnd} = unsigned(Wb) * signed(Ws)	1	1	None
		MUL.US	Wb, Ws, Acc ⁽¹⁾	Accumulator = unsigned(Wb) * signed(Ws)	1	1	None
		MUL.UU	Wb, Ws, Wnd	{Wnd + 1, Wnd} = unsigned(Wb) * unsigned(Ws)	1	1	None
		MUL.UU	Wb,#lit5,Acc ⁽¹⁾	Accumulator = unsigned(Wb) * unsigned(lit5)	1	1	None
		MUL.UU	Wb, Ws, Acc ⁽¹⁾	Accumulator = unsigned(Wb) * unsigned(Ws)	1	1	None
		MULW.SS	Wb, Ws, Wnd	Wnd = signed(Wb) * signed(Ws)	1	1	None
		MULW.SU	Wb, Ws, Wnd	Wnd = signed(Wb) * unsigned(Ws)	1	1	None
		MULW.US	Wb, Ws, Wnd	Wnd = unsigned(Wb) * signed(Ws)	1	1	None
		MULW.UU	Wb, Ws, Wnd	Wnd = unsigned(Wb) * unsigned(Ws)	1	1	None
		MUL.SU	Wb,#lit5,Wnd	{Wnd + 1, Wnd} = signed(Wb) * unsigned(lit5)	1	1	None
		MUL.SU	Wb,#lit5,Wnd	Wnd = signed(Wb) * unsigned(lit5)	1	1	None
		MUL.UU	Wb,#lit5,Wnd	{Wnd + 1, Wnd} = unsigned(Wb) * unsigned(lit5)	1	1	None
		MUL.UU	Wb,#lit5,Wnd	Wnd = unsigned(Wb) * unsigned(lit5)	1	1	None
		MUL	f	W3:W2 = f * WREG	1	1	None

Note 1: This instruction is available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic		Assembly Syntax	Description	# of Words	# of Cycles	Status Flags Affected
53	NEG	NEG	Acc(1)	Negate Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
		NEG	f	$f = \overline{f} + 1$	1	1	C,DC,N,OV,Z
		NEG	f,WREG	WREG = f + 1	1	1	C,DC,N,OV,Z
		NEG	Ws,Wd	$Wd = \overline{Ws} + 1$	1	1	C,DC,N,OV,Z
54	NOP	NOP		No Operation	1	1	None
		NOPR		No Operation	1	1	None
55	POP	POP	f	Pop f from Top-of-Stack (TOS)	1	1	None
		POP	Wdo	Pop from Top-of-Stack (TOS) to Wdo	1	1	None
		POP.D	Wnd	Pop from Top-of-Stack (TOS) to W(nd):W(nd + 1)	1	2	None
		POP.S		Pop Shadow Registers	1	1	All
56	PUSH	PUSH	f	Push f to Top-of-Stack (TOS)	1	1	None
		PUSH	Wso	Push Wso to Top-of-Stack (TOS)	1	1	None
		PUSH.D	Wns	Push W(ns):W(ns + 1) to Top-of-Stack (TOS)	1	2	None
		PUSH.S		Push Shadow Registers	1	1	None
57	PWRSAV	PWRSAV	#lit1	Go into Sleep or Idle mode	1	1	WDTO,Sleep
58	RCALL	RCALL	Expr	Relative Call	1	4	SFA
		RCALL	Wn	Computed Call	1	4	SFA
59	REPEAT	REPEAT	#lit15	Repeat Next Instruction lit15 + 1 times	1	1	None
		REPEAT	Wn	Repeat Next Instruction (Wn) + 1 times	1	1	None
60	RESET	RESET		Software device Reset	1	1	None
61	RETFIE	RETFIE		Return from interrupt	1	6 (5)	SFA
62	RETLW	RETLW	#lit10,Wn	Return with literal in Wn	1	6 (5)	SFA
63	RETURN	RETURN		Return from Subroutine	1	6 (5)	SFA
64	RLC	RLC	f	f = Rotate Left through Carry f	1	1	C,N,Z
		RLC	f,WREG	WREG = Rotate Left through Carry f	1	1	C,N,Z
		RLC	Ws,Wd	Wd = Rotate Left through Carry Ws	1	1	C,N,Z
65	RLNC	RLNC	f	f = Rotate Left (No Carry) f	1	1	N,Z
		RLNC	f,WREG	WREG = Rotate Left (No Carry) f	1	1	N,Z
		RLNC	Ws,Wd	Wd = Rotate Left (No Carry) Ws	1	1	N,Z
66	RRC	RRC	f	f = Rotate Right through Carry f	1	1	C,N,Z
		RRC	f,WREG	WREG = Rotate Right through Carry f	1	1	C,N,Z
		RRC	Ws,Wd	Wd = Rotate Right through Carry Ws	1	1	C,N,Z
67	RRNC	RRNC	f	f = Rotate Right (No Carry) f	1	1	N,Z
		RRNC	f,WREG	WREG = Rotate Right (No Carry) f	1	1	N,Z
		RRNC	Ws,Wd	Wd = Rotate Right (No Carry) Ws	1	1	N,Z
68	SAC	SAC	Acc,#Slit4,Wdo ⁽¹⁾	Store Accumulator	1	1	None
		SAC.R	Acc,#Slit4,Wdo ⁽¹⁾	Store Rounded Accumulator	1	1	None
69	SE	SE	Ws, Wnd	Wnd = sign-extended Ws	1	1	C,N,Z
70	SETM	SETM	f	f = 0xFFFF	1	1	None
		SETM	WREG	WREG = 0xFFFF	1	1	None
		SETM	Ws	Ws = 0xFFFF	1	1	None
71	SFTAC	SFTAC	Acc, Wn ⁽¹⁾	Arithmetic Shift Accumulator by (Wn)	1	1	OA,OB,OAB, SA,SB,SAB
		SFTAC	Acc,#Slit6 ⁽¹⁾	Arithmetic Shift Accumulator by Slit6	1	1	OA,OB,OAB, SA,SB,SAB

Note 1: This instruction is available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax Description		# of Words	# of Cycles	Status Flags Affected	
72	SL	SL	f	f = Left Shift f	1	1	C,N,OV,Z
		SL	f,WREG	WREG = Left Shift f	1	1	C,N,OV,Z
		SL	Ws,Wd	Wd = Left Shift Ws	1	1	C,N,OV,Z
		SL	Wb, Wns, Wnd	Wnd = Left Shift Wb by Wns	1	1	N,Z
		SL	Wb,#lit5,Wnd	Wnd = Left Shift Wb by lit5	1	1	N,Z
73	SUB	SUB	_{Acc} (1)	Subtract Accumulators	1	1	OA,OB,OAB, SA,SB,SAB
		SUB	f	f = f – WREG	1	1	C,DC,N,OV,Z
		SUB	f,WREG	WREG = f – WREG	1	1	C,DC,N,OV,Z
		SUB	#lit10,Wn	Wn = Wn – lit10	1	1	C,DC,N,OV,Z
		SUB	Wb,Ws,Wd	Wd = Wb – Ws	1	1	C,DC,N,OV,Z
		SUB	Wb,#lit5,Wd	Wd = Wb – lit5	1	1	C,DC,N,OV,Z
74	SUBB	SUBB	f	$f = f - WREG - (\overline{C})$	1	1	C,DC,N,OV,Z
		SUBB	f,WREG	WREG = $f - WREG - (\overline{C})$	1	1	C,DC,N,OV,Z
		SUBB	#lit10,Wn	$Wn = Wn - lit10 - (\overline{C})$	1	1	C,DC,N,OV,Z
		SUBB	Wb,Ws,Wd	$Wd = Wb - Ws - (\overline{C})$	1	1	C,DC,N,OV,Z
		SUBB	Wb,#lit5,Wd	$Wd = Wb - lit5 - (\overline{C})$	1	1	C,DC,N,OV,Z
75	SUBR	SUBR	f	f = WREG – f	1	1	C,DC,N,OV,Z
		SUBR	f,WREG	WREG = WREG – f	1	1	C,DC,N,OV,Z
		SUBR	Wb,Ws,Wd	Wd = Ws - Wb	1	1	C,DC,N,OV,Z
		SUBR	Wb,#lit5,Wd	Wd = lit5 – Wb	1	1	C,DC,N,OV,Z
76	SUBBR	SUBBR	f	$f = WREG - f - (\overline{C})$	1	1	C,DC,N,OV,Z
		SUBBR	f,WREG	WREG = WREG – f – (\overline{C})	1	1	C,DC,N,OV,Z
		SUBBR	Wb,Ws,Wd	$Wd = Ws - Wb - (\overline{C})$	1	1	C,DC,N,OV,Z
		SUBBR	Wb,#lit5,Wd	$Wd = lit5 - Wb - (\overline{C})$	1	1	C,DC,N,OV,Z
77	SWAP	SWAP.b	Wn	Wn = nibble swap Wn	1	1	None
		SWAP	Wn	Wn = byte swap Wn	1	1	None
78	TBLRDH	TBLRDH	Ws,Wd	Read Prog<23:16> to Wd<7:0>	1	5	None
79	TBLRDL	TBLRDL	Ws,Wd	Read Prog<15:0> to Wd	1	5	None
80	TBLWTH	TBLWTH	Ws,Wd	Write Ws<7:0> to Prog<23:16>	1	2	None
81	TBLWTL	TBLWTL	Ws,Wd	Write Ws to Prog<15:0>	1	2	None
82	ULNK	ULNK		Unlink Frame Pointer	1	1	SFA
83	XOR	XOR f f=f.XOR. WREG		f = f .XOR. WREG	1	1	N,Z
		XOR	f,WREG	WREG = f .XOR. WREG	1	1	N,Z
		XOR	#lit10,Wn	Wd = lit10 .XOR. Wd	1	1	N,Z
		XOR	Wb,Ws,Wd	Wd = Wb .XOR. Ws	1	1	N,Z
		XOR	Wb,#lit5,Wd	Wd = Wb .XOR. lit5	1	1	N,Z
84	ZE	ZE	Ws,Wnd	Wnd = Zero-extend Ws	1	1	C,Z,N

Note 1: This instruction is available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

29.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers and dsPIC® digital signal controllers are supported with a full range of software and hardware development tools:

- · Integrated Development Environment
 - MPLAB® IDE Software
- · Compilers/Assemblers/Linkers
 - MPLAB C Compiler for Various Device Families
 - HI-TECH C® for Various Device Families
 - MPASM™ Assembler
 - MPLINK[™] Object Linker/ MPLIB[™] Object Librarian
 - MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
 - MPLAB SIM Software Simulator
- Emulators
 - MPLAB REAL ICE™ In-Circuit Emulator
- · In-Circuit Debuggers
 - MPLAB ICD 3
 - PICkit™ 3 Debug Express
- · Device Programmers
 - PICkit™ 2 Programmer
 - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits, and Starter Kits

29.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16/32-bit microcontroller market. The MPLAB IDE is a Windows® operating system-based application that contains:

- A single graphical interface to all debugging tools
 - Simulator
 - Programmer (sold separately)
 - In-Circuit Emulator (sold separately)
 - In-Circuit Debugger (sold separately)
- · A full-featured editor with color-coded context
- · A multiple project manager
- Customizable data windows with direct edit of contents
- · High-level source code debugging
- · Mouse over variable inspection
- Drag and drop variables from source to watch windows
- · Extensive on-line help
- Integration of select third party tools, such as IAR C Compilers

The MPLAB IDE allows you to:

- Edit your source files (either C or assembly)
- One-touch compile or assemble, and download to emulator and simulator tools (automatically updates all project information)
- · Debug using:
 - Source files (C or assembly)
 - Mixed C and assembly
 - Machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost-effective simulators, through low-cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increased flexibility and power.

29.2 MPLAB C Compilers for Various Device Families

The MPLAB C Compiler code development systems are complete ANSI C compilers for Microchip's PIC18, PIC24 and PIC32 families of microcontrollers and the dsPIC30 and dsPIC33 families of digital signal controllers. These compilers provide powerful integration capabilities, superior code optimization and ease of use.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

29.3 HI-TECH C for Various Device Families

The HI-TECH C Compiler code development systems are complete ANSI C compilers for Microchip's PIC family of microcontrollers and the dsPIC family of digital signal controllers. These compilers provide powerful integration capabilities, omniscient code generation and ease of use.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

The compilers include a macro assembler, linker, preprocessor, and one-step driver, and can run on multiple platforms.

29.4 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code and COFF files for debugging.

The MPASM Assembler features include:

- · Integration into MPLAB IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process

29.5 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler and the MPLAB C18 C Compiler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

29.6 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC devices. MPLAB C Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- · Support for fixed-point and floating-point data
- · Command line interface
- · Rich directive set
- · Flexible macro language
- · MPLAB IDE compatibility

29.7 MPLAB SIM Software Simulator

The MPLAB SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC® DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB SIM Software Simulator fully supports symbolic debugging using the MPLAB C Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

29.8 MPLAB REAL ICE In-Circuit Emulator System

MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs PIC[®] Flash MCUs and dsPIC[®] Flash DSCs with the easy-to-use, powerful graphical user interface of the MPLAB Integrated Development Environment (IDE), included with each kit.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with incircuit debugger systems (RJ11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB IDE. In upcoming releases of MPLAB IDE, new devices will be supported, and new features will be added. MPLAB REAL ICE offers significant advantages over competitive emulators including low-cost, full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, a ruggedized probe interface and long (up to three meters) interconnection cables.

29.9 MPLAB ICD 3 In-Circuit Debugger System

MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost effective high-speed hardware debugger/programmer for Microchip Flash Digital Signal Controller (DSC) and microcontroller (MCU) devices. It debugs and programs PIC® Flash microcontrollers and dsPIC® DSCs with the powerful, yet easy-to-use graphical user interface of MPLAB Integrated Development Environment (IDE).

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

29.10 PICkit 3 In-Circuit Debugger/ Programmer and PICkit 3 Debug Express

The MPLAB PICkit 3 allows debugging and programming of PIC[®] and dsPIC[®] Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB Integrated Development Environment (IDE). The MPLAB PICkit 3 is connected to the design engineer's PC using a full speed USB interface and can be connected to the target via an Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the reset line to implement in-circuit debugging and In-Circuit Serial Programming ™.

The PICkit 3 Debug Express include the PICkit 3, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

29.11 PICkit 2 Development Programmer/Debugger and PICkit 2 Debug Express

The PICkit™ 2 Development Programmer/Debugger is a low-cost development tool with an easy to use interface for programming and debugging Microchip's Flash families of microcontrollers. The full featured Windows® programming interface supports baseline (PIC10F, PIC12F5xx, PIC16F5xx), midrange (PIC12F6xx, PIC16F), PIC18F, PIC24, dsPIC30, dsPIC33, and PIC32 families of 8-bit, 16-bit, and 32-bit microcontrollers, and many Microchip Serial EEPROM products. With Microchip's powerful MPLAB Integrated Development Environment (IDE) the PICkit™ 2 enables in-circuit debugging on most PIC® microcontrollers. In-Circuit-Debugging runs, halts and single steps the program while the PIC microcontroller is embedded in the application. When halted at a breakpoint, the file registers can be examined and modified.

The PICkit 2 Debug Express include the PICkit 2, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

29.12 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages and a modular, detachable socket assembly to support various package types. The ICSP™ cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices and incorporates an MMC card for file storage and data applications.

29.13 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELoq® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

30.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X family are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied.

Absolute Maximum Ratings(1)

Ambient temperature under bias	40°C to +125°C
Storage temperature	65°C to +150°C
Voltage on VDD with respect to Vss	0.3V to +4.0V
Voltage on any pin that is not 5V tolerant, with respect to Vss ⁽³⁾	0.3V to (VDD + 0.3V)
Voltage on any 5V tolerant pin with respect to Vss when VDD ≥ 3.0V ⁽³⁾	0.3V to +5.5V
Voltage on any 5V tolerant pin with respect to Vss when VDD < 3.0V ⁽³⁾	0.3V to 3.6V
Maximum current out of Vss pin	300 mA
Maximum current into VDD pin ⁽²⁾	300 mA
Maximum current sunk/sourced by any 4x I/O pin	15 mA
Maximum current sunk/sourced by any 8x I/O pin	25 mA
Maximum current sunk by all ports ^(2,4)	200 mA

- **Note 1:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
 - 2: Maximum allowable current is a function of device maximum power dissipation (see Table 30-2).
 - 3: See the "Pin Diagrams" section for the 5V tolerant pins.
 - **4:** Exceptions are: dsPIC33EPXXXGP502, dsPIC33EPXXXMC202/502, and PIC24EPXXXGP/MC202 devices, which have a maximum sink/source capability of 130 mA.

30.1 DC Characteristics

TABLE 30-1: OPERATING MIPS VS. VOLTAGE

			Maximum MIPS		
Characteristic	V _{DD} Range (in Volts)	Temp Range (in °C)	dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X		
_	VBOR to 3.6V ⁽¹⁾	-40°C to +85°C	70		
_	VBOR to 3.6V ⁽¹⁾	-40°C to +125°C	60		

Note 1: Device is functional at VBOR < VDD < VDDMIN. Analog modules: ADC, Op amp/Comparator, and DAC will have degraded performance. Device functionality is tested but not characterized.

TABLE 30-2: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min.	Тур.	Max.	Unit
Industrial Temperature Devices					
Operating Junction Temperature Range	TJ	-40	_	+125	°C
Operating Ambient Temperature Range	TA	-40	_	+85	°C
Extended Temperature Devices					
Operating Junction Temperature Range	TJ	-40	_	+140	°C
Operating Ambient Temperature Range	TA	-40	_	+125	°C
Power Dissipation: Internal chip power dissipation: $PINT = VDD \ x \ (IDD - \Sigma \ IOH)$ I/O Pin Power Dissipation:	Po	PINT + PI/O			W
I/O = Σ ({VDD - VOH} x IOH) + Σ (VOL x IOL)					
Maximum Allowed Power Dissipation	PDMAX	(ΓJ − TA)/θJ	IA	W

TABLE 30-3: THERMAL PACKAGING CHARACTERISTICS

Characteristic	Symbol	Тур.	Max.	Unit	Notes
Package Thermal Resistance, 64-Pin QFN	θ JA	28.0	_	°C/W	1
Package Thermal Resistance, 64-Pin TQFP 10x10 mm	θ JA	48.3	_	°C/W	1
Package Thermal Resistance, 44-Pin QFN	θ JA	29.0	_	°C/W	1
Package Thermal Resistance, 44-Pin TQFP 10x10 mm	θ JA	49.8	_	°C/W	1
Package Thermal Resistance, 44-Pin VTLA 6x6 mm	θ JA	25.2	_	°C/W	1
Package Thermal Resistance, 36-Pin VTLA 5x5 mm	θ JA	28.5	_	°C/W	1
Package Thermal Resistance, 28-Pin QFN-S	θја	30.0	_	°C/W	1
Package Thermal Resistance, 28-Pin SSOP	θ JA	71.0	_	°C/W	1
Package Thermal Resistance, 28-Pin SOIC	θ JA	69.7	_	°C/W	1
Package Thermal Resistance, 28-Pin SPDIP	θја	60.0	_	°C/W	1

Note 1: Junction to ambient thermal resistance, Theta-JA (θ JA) numbers are achieved by package simulations.

TABLE 30-4: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS			(unless o	therwise	stated) ure -40	0°C≤ TA	ee Note3): 3.0V to 3.6V ≤ + 85°C for Industrial ≤ +125°C for Extended		
Param No.	Symbol	Characteristic	Min. Typ. ⁽¹⁾ Max. Units Conditions						
Operating Voltage									
DC10	VDD	Supply Voltage ⁽³⁾	VBOR	_	3.6	V	_		
DC12	VDR	RAM Data Retention Voltage ⁽²⁾	1.8	_	_	V	_		
DC16	VPOR	VDD Start Voltage to ensure internal Power-on Reset signal	_	_	Vss	V	_		
DC17	SVDD	VDD Rise Rate to ensure internal Power-on Reset signal	0.03	_	_	V/ms	0V-1V in 100 ms		

- **Note 1:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated.
 - 2: This is the limit to which VDD may be lowered without losing RAM data.
 - **3:** The device is functional at VBOR < VDD < VDDMIN. Analog modules: ADC, Op amp/Comparator, and DAC, will have degraded performance. Device functionality is tested but not characterized.

TABLE 30-5: FILTER CAPACITOR (CEFC) SPECIFICATIONS

	Standard Operating Conditions (unless otherwise stated): Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended											
Param No.	Param Symbol Characteristics Min Tyn Max Units Comments											
	CEFC	External Filter Capacitor Value ⁽¹⁾	4.7	10	_	μF	Capacitor must have a low series resistance (< 1 ohm)					

Note 1: Typical VCAP voltage = 1.8 volts when VDD ≥ VDDMIN.

TABLE 30-6: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

DC CHARACTI	ERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq \text{TA} \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq \text{TA} \leq +125^{\circ}\text{C}$ for Extended							
Parameter No.	Тур.	Max.	Units	Conditions						
Operating Curi	rent (IDD)									
DC20d	9	20	mA	-40°C						
DC20a	9	20	mA	+25°C	3.3V	10 MIPS				
DC20b	9	20	mA	+85°C	3.34	10 WIFS				
DC20c	9	20	mA	+125°C						
DC22d	16	40	mA	-40°C						
DC22a	16	40	mA	+25°C	3.3V	20 MIPS				
DC22b	16	40	mA	+85°C	3.3 v	20 WIFS				
DC22c	16	40	mA	+125°C						
DC24d	27	60	mA	-40°C						
DC24a	27	60	mA	+25°C	3.3V	40 MIPS				
DC24b	27	60	mA	+85°C	3.34	40 WIFS				
DC24c	27	60	mA	+125°C						
DC25d	36	80	mA	-40°C						
DC25a	36	80	mA	+25°C	3.3V	60 MIPS				
DC25b	36	80	mA	+85°C	3.34	00 WIFS				
DC25c	36	80	mA	+125°C						
DC26d	41	100	mA	-40°C						
DC26a	41	100	mA	+25°C	3.3V	70 MIPS				
DC26b	41	100	mA	+85°C						

- **Note 1:** IDD is primarily a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all IDD measurements are as follows:
 - Oscillator is configured in EC mode with PLL, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
 - CLKO is configured as an I/O input pin in the Configuration word
 - · All I/O pins are configured as inputs and pulled to Vss
 - MCLR = VDD, WDT and FSCM are disabled
 - · CPU, SRAM, program memory and data memory are operational
 - No peripheral modules are operating; however, every peripheral is being clocked (all PMDx bits are zeroed)
 - CPU executing while(1) statement
 - JTAG disabled

TABLE 30-7: DC CHARACTERISTICS: IDLE CURRENT (IIDLE)

DC CHARACTI	ERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +125^{\circ}\text{C}$ for Extended								
Parameter No.	Тур.	Max.	Units	Conditions							
Idle Current (III	e Current (IIDLE) ⁽¹⁾										
DC40d	3	5	mA	-40°C							
DC40a	3	5	mA	+25°C		10 MIPS					
DC40b	3	5	mA	+85°C	3.3V	10 WIFS					
DC40c	3	5	mA	+125°C							
DC42d	6	10	mA	-40°C							
DC42a	6	10	mA	+25°C	3.3V	20 MIPS					
DC42b	6	10	mA	+85°C	3.5 V	20 WIF 3					
DC42c	6	10	mA	+125°C							
DC44d	11	20	mA	-40°C							
DC44a	11	20	mA	+25°C	3.3V	40 MIPS					
DC44b	11	20	mA	+85°C	3.5 V	40 WIF 3					
DC44c	11	20	mA	+125°C							
DC45d	17	40	mA	-40°C							
DC45a	17	40	mA	+25°C	3.3V	60 MIPS					
DC45b	17	40	mA	+85°C	3.30 60 MIPS						
DC45c	17	40	mA	+125°C							
DC46d	20	60	mA	-40°C							
DC46a	20	60	mA	+25°C	3.3V	70 MIPS					
DC46b	20	60	mA	+85°C							

Note 1: Base Idle current (IIDLE) is measured as follows:

- CPU core is off, oscillator is configured in EC mode and external clock active, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- · CLKO is configured as an I/O input pin in the Configuration word
- All I/O pins are configured as inputs and pulled to Vss
- MCLR = VDD, WDT and FSCM are disabled
- No peripheral modules are operating; however, every peripheral is being clocked (all PMDx bits are zeroed)
- The NVMSIDL bit (NVMCON<12>) = 1 (i.e., Flash regulator is set to stand-by while the device is in Idle mode)
- The VREGSF bit (RCON<11>) = 0 (i.e., Flash regulator is set to stand-by while the device is in Sleep mode)
- JTAG disabled

TABLE 30-8: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD)

DC CHARACT	EDICTICS		Standard O		nditions: 3.0\ ed)	· · · · · · · · · · · · · · · · · · ·			
DC CHARACT	ERISTICS		Operating to	emperature		← + 85°C for Industrial ← +125°C for Extended			
Parameter No.	Тур.	Max.	Units	Conditions					
Power-Down (Current (IPD) ⁽	¹⁾ – dsPIC33	EP32GP50X,	, dsPIC33EP	32MC20X/50	X, and PIC24EP32GP/MC20X			
DC60d	30		μΑ	-40°C					
DC60a	35	1	μΑ	+25°C	3.3V	Base Power-Down Current			
DC60b	150		μΑ	+85°C	3.34	Base Fower-Down Current			
DC60c	250		μΑ	+125°C					
DC61d	8		μΑ	-40°C					
DC61a	10	_	μΑ	+25°C	3.3V	Watchdog Timer Current: ∆IwDT ⁽²⁾			
DC61b	12	_	μΑ	+85°C	J.5 V	Waterlady Timer Gurrent. AIWB1			
DC61c	13	_	μΑ	+125°C					
Power-Down (Current (IPD) ⁽	¹⁾ – dsPIC33	EP64GP50X,	dsPIC33EP	64MC20X/50	X, and PIC24EP64GP/MC20X			
DC60d	25	100	μΑ	-40°C					
DC60a	30	100	μΑ	+25°C	3.3V	Base Power-Down Current			
DC60b	150	300	μΑ	+85°C	0.0 V	Buse I owel Bown outlent			
DC60c	350	700	μΑ	+125°C					
DC61d	8	10	μΑ	-40°C					
DC61a	10	15	μΑ	+25°C	3.3V	Watchdog Timer Current: ∆IwDT ⁽²⁾			
DC61b	12	20	μΑ	+85°C	J.5 V	Waterlady Timer Gurrent. AIWB1			
DC61c	13	25	μΑ	+125°C					
Power-Down (Current (IPD) ^{(*}	¹⁾ – dsPIC33	EP128GP50X	, dsPIC33EI	P128MC20X/	50X, and PIC24EP128GP/MC20X			
DC60d	30	_	μΑ	-40°C					
DC60a	35	_	μΑ	+25°C	3.3V	Base Power-Down Current			
DC60b	150	_	μΑ	+85°C	0.0 V	Buse I owel Bown durient			
DC60c	550	_	μΑ	+125°C					
DC61d	8	_	μΑ	-40°C					
DC61a	10	_	μΑ	+25°C	3.3V	Watchdog Timer Current: ∆IwDT ⁽²⁾			
DC61b	12	_	μΑ	+85°C	J.5 v	Tracelled Times Current. ZiwD1**			
DC61c	13	_	μΑ	+125°C					

Note 1: IPD (Sleep) current is measured as follows:

- CPU core is off, oscillator is configured in EC mode and external clock active, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration word
- · All I/O pins are configured as inputs and pulled to Vss
- MCLR = VDD, WDT and FSCM are disabled
- All peripheral modules are disabled (PMDx bits are all ones)
- The VREGS bit (RCON<8>) = 0 (i.e., core regulator is set to stand-by while the device is in Sleep mode)
- The VREGSF bit (RCON<11>) = 0 (i.e., Flash regulator is set to stand-by while the device is in Sleep mode)
- · JTAG disabled
- 2: The Δ current is the additional current consumed when the module is enabled. This current should be added to the base IPD current.

TABLE 30-8: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD) (CONTINUED)

DC CHARACT	ERISTICS		(unless oth	Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +125^{\circ}\text{C}$ for Extended						
Parameter No.	Тур.	Max.	Units		(Conditions				
Power-Down (Current (IPD) ⁽	^{1,3)} – dsPIC3	3EP256GP50	X, dsPIC33E	P256MC20X	/50X, and PIC24EP256GP/MC20X				
DC60d	35		μΑ	-40°C						
DC60a	40	_	μΑ	+25°C	3.3V	Base Power-Down Current				
DC60b	250	_	μΑ	+85°C	3.3V	Base Fower-Down Current				
DC60c	1000	_	μΑ	+125°C						
DC61d	8	_	μΑ	-40°C						
DC61a	10	_	μΑ	+25°C	2 2V Watchdag Timer Current: Alive					
DC61b	12		μΑ	+85°C	3.3V	Watchdog Timer Current: ∆IwDT ⁽²⁾				
DC61c	13	_	μΑ	+125°C						

Note 1: IPD (Sleep) current is measured as follows:

- CPU core is off, oscillator is configured in EC mode and external clock active, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- · CLKO is configured as an I/O input pin in the Configuration word
- · All I/O pins are configured as inputs and pulled to Vss
- MCLR = VDD, WDT and FSCM are disabled
- All peripheral modules are disabled (PMDx bits are all ones)
- The VREGS bit (RCON<8>) = 0 (i.e., core regulator is set to stand-by while the device is in Sleep mode)
- The VREGSF bit (RCON<11>) = 0 (i.e., Flash regulator is set to stand-by while the device is in Sleep mode)
- · JTAG disabled
- 2: The Δ current is the additional current consumed when the module is enabled. This current should be added to the base IPD current.

TABLE 30-9: DC CHARACTERISTICS: DOZE CURRENT (IDOZE)

DC CHARACTER	ISTICS	Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{Ta} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{Ta} \le +125^{\circ}\text{C}$ for Extended						
Parameter No.	Тур.	Doze Ratio	Units		Conditions			
Doze Current (IDC)ZE) ⁽¹⁾							
DC73a	35	60	1:2	mA	-40°C	3.3V	Fosc = 140 MHz	
DC73g	20	30	1:128	mA	-40 C		FUSC = 140 WIHZ	
DC70a	35	60	1:2	mA	+25°C	3.3V	Fosc = 140 MHz	
DC70g	20	30	1:128	mA	+25 C	3.3 V	140 WI12	
DC71a	35	60	1:2	mA	+85°C	3.3V	Fosc = 140 MHz	
DC71g	20	30	1:128	mA	+65 C	3.3 V	FOSC = 140 MHZ	
DC72a	28	60	1:2	mA	+125°C	3.3V	Fosc = 120 MHz	
DC72g	15	30	1:128	mA	+125 C	3.31	FUSC - 120 WITZ	

- **Note 1:** IDOZE is primarily a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all IDOZE measurements are as follows:
 - Oscillator is configured in EC mode and external clock active, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
 - CLKO is configured as an I/O input pin in the Configuration word
 - · All I/O pins are configured as inputs and pulled to Vss
 - MCLR = VDD, WDT and FSCM are disabled
 - · CPU, SRAM, program memory and data memory are operational
 - No peripheral modules are operating; however, every peripheral is being clocked (all PMDx bits are zeroed)
 - CPU executing while(1) statement
 - JTAG disabled

TABLE 30-10: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Oper (unless otherw Operating temp	· ·			
Param No.	Symbol	Characteristic	Min.	Max.	Units	Conditions	
	VIL	Input Low Voltage					
DI10		Any I/O pin and MCLR	Vss	_	0.2 VDD	V	
DI18		I/O Pins with SDAx, SCLx	Vss	_	0.3 VDD	V	SMBus disabled
DI19		I/O Pins with SDAx, SCLx	Vss	_	8.0	V	SMBus enabled
	VIH	Input High Voltage					
DI20		I/O Pins Not 5V Tolerant I/O Pins 5V Tolerant and MCLR	0.7 VDD 0.7 VDD	_	VDD 5.3	V V	See Note 4 See Note 4
		I/O Pins with SDAx, SCLx	0.7 VDD	_	5.3	V	SMBus disabled
		I/O Pins with SDAx, SCLx	2.1		5.3	V	SMBus enabled
	ICNPU	Change Notification Pull-up Current					
DI30			50	250	400	μΑ	VDD = 3.3V, VPIN = VSS
	ICNPD	Change Notification Pull- down Current ⁽⁵⁾				_	
DI31			_	50	_	μΑ	VDD = 3.3V, VPIN = VDD

- Note 1: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.
 - 2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.
 - 3: Negative current is defined as current sourced by the pin.
 - 4: See "Pin Diagrams" for the 5V tolerant I/O pins.
 - 5: VIL source < (Vss 0.3). Characterized but not tested.
 - **6:** Non-5V tolerant pins VIH source > (VDD + 0.3), 5V tolerant pins VIH source > 5.5V. Characterized but not tested.
 - 7: Digital 5V tolerant pins cannot tolerate any "positive" input injection current from input sources > 5.5V.
 - 8: Injection currents > | 0 | can affect the ADC results by approximately 4-6 counts.
 - **9:** Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the mathematical "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

TABLE 30-10: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS (CONTINUED)

DC CH	DC CHARACTERISTICS			Standard Operating Co (unless otherwise state Operating temperature			3.6V 5°C for Industrial 25°C for Extended
Param No.	Symbol	Characteristic	Min. Typ. ⁽¹⁾		Max.	Units	Conditions
	lıL	Input Leakage Current ^(2,3)					
DI50		I/O pins 5V Tolerant ⁽⁴⁾	_	±1	_	μА	Vss ≤ Vpin ≤ Vdd, Pin at high-impedance
DI51		I/O Pins Not 5V Tolerant ⁽⁴⁾	_	±1	_	μА	$VSS \leq VPIN \leq VDD, \\ Pin at high-impedance, \\ -40^{\circ}C \leq TA \leq +85^{\circ}C$
DI51a		I/O Pins Not 5V Tolerant ⁽⁴⁾	_	±1	_	μА	Analog pins shared with external reference pins, $-40^{\circ}C \le TA \le +85^{\circ}C$
DI51b		I/O Pins Not 5V Tolerant ⁽⁴⁾	_	±1	_	μА	$Vss \leq VPIN \leq VDD, \ Pin$ at high-impedance, $-40^{\circ}C \leq TA \leq +125^{\circ}C$
DI51c		I/O Pins Not 5V Tolerant ⁽⁴⁾	_	±1	_	μА	Analog pins shared with external reference pins, $-40^{\circ}\text{C} \le \text{TA} \le +125^{\circ}\text{C}$
DI55		MCLR	_	±1	_	μΑ	$Vss \leq Vpin \leq Vdd$
DI56		OSC1	_	±1	<u> </u>	μА	$ \begin{array}{c} \text{VSS} \leq \text{VPIN} \leq \text{VDD,} \\ \text{XT and HS modes} \end{array} $

- **Note 1:** Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.
 - 2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.
 - **3:** Negative current is defined as current sourced by the pin.
 - 4: See "Pin Diagrams" for the 5V tolerant I/O pins.
 - 5: VIL source < (VSS 0.3). Characterized but not tested.
 - **6:** Non-5V tolerant pins VIH source > (VDD + 0.3), 5V tolerant pins VIH source > 5.5V. Characterized but not tested.
 - 7: Digital 5V tolerant pins cannot tolerate any "positive" input injection current from input sources > 5.5V.
 - 8: Injection currents > | 0 | can affect the ADC results by approximately 4-6 counts.
 - **9:** Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the mathematical "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

TABLE 30-10: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)					
Param No.	Symbol	Characteristic	Min.	Max.	Units	Conditions		
DI60a	lich	Input Low Injection Current Input High Injection Current	0	_	-5 ^(5,8)	mA mA	All pins except VDD, VSS, AVDD, AVSS, MCLR, VCAP, and RB7 All pins except VDD, VSS, AVDD, AVSS, MCLR, VCAP, RB7, and all 5V tolerant pins ⁽⁷⁾	
DI60c	∑lict	Total Input Injection Current (sum of all I/O and control pins)	₋₂₀ (9)	_	+20(9)	mA	Absolute instantaneous sum of all \pm input injection currents from all I/O pins (IICL + IICH) $\leq \Sigma$ IICT	

- **Note 1:** Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.
 - 2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.
 - **3:** Negative current is defined as current sourced by the pin.
 - 4: See "Pin Diagrams" for the 5V tolerant I/O pins.
 - 5: VIL source < (VSS 0.3). Characterized but not tested.
 - 6: Non-5V tolerant pins VIH source > (VDD + 0.3), 5V tolerant pins VIH source > 5.5V. Characterized but not tested
 - 7: Digital 5V tolerant pins cannot tolerate any "positive" input injection current from input sources > 5.5V.
 - 8: Injection currents > | 0 | can affect the ADC results by approximately 4-6 counts.
 - **9:** Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the mathematical "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

TABLE 30-11: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHA	RACTER	ISTICS	Standard (unless Operation	otherwi	se state	ed)	:: 3.0V to 3.6V ≤ TA ≤ +85°C for Industrial		
						$-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended			
Param.	Symbol	Characteristic	Min.	Тур.	Max.	Units	Conditions		
DO10	Voi	Output Low Voltage I/O Pins: 4x Sink Driver Pins - All I/O output pins not defined as 8x Sink Driver pins	_	_	0.4	٧	IOL ≤ 10 mA, VDD = 3.3V		
DO10 VOL	VOL	Output Low Voltage I/O Pins: 8x Sink Driver Pins - RA3, RA4, RA9, RB7-RB15, RC3, and RC15	1	_	0.4	>	$IOL \le 15 \text{ mA}, VDD = 3.3V$		
DO20	Vон	Output High Voltage I/O Pins: 4x Source Driver Pins - All I/O output pins not defined as 8x Source Driver pins	2.4	_	_	>	IOH ≥ -10 mA, VDD = 3.3V		
DO20	VOH	Output High Voltage I/O Pins: 8x Source Driver Pins - RA3, RA4, RA9, RB7-RB15, RC3, and RC15	2.4	_	_	V	IOH ≥ -15 mA, VDD = 3.3V		
		Output High Voltage	1.5 ⁽¹⁾		_		$IOH \ge -14 \text{ mA}, VDD = 3.3V$		
		4x Source Driver Pins - All I/O	2.0 ⁽¹⁾	_	_	V	IOH ≥ -12 mA, VDD = 3.3V		
DO20A	Voud	output pins not defined as 8x Sink Driver pins	3.0 ⁽¹⁾	_	_		IOH \geq -7 mA, VDD = 3.3V		
DOZUA	VOH I	Output High Voltage I/O Pins:	1.5 ⁽¹⁾	_	_		IOH ≥ -22 mA, VDD = 3.3V		
		8x Source Driver Pins - RA3,	2.0 ⁽¹⁾	_	_	V	IOH ≥ -18 mA, VDD = 3.3V		
		RA4, RA9, RB7-RB15, RC3, and RC15	3.0(1)	_	_		IOH ≥ -10 mA, VDD = 3.3V		

Note 1: Parameters are characterized, but not tested.

TABLE 30-12: ELECTRICAL CHARACTERISTICS: BOR

DC CHARACTERISTICS Standard Opera (unless otherwi Operating tempor			•					
Param No.	Symbol	Character	Characteristic			Max.	Units	Conditions
BO10	VBOR	BOR Event on VDD transition igh-to-low		2.7	_	2.95	V	See Note 2

- Note 1: Parameters are for design guidance only and are not tested in manufacturing.
 - 2: The device will operate as normal until the VDDMIN threshold is reached.
 - **3:** The device is functional at VBOR < VDD < VDDMIN. Analog modules: ADC, Op amp/Comparator, and DAC, will have degraded performance. Device functionality is tested but not characterized.

TABLE 30-13: DC CHARACTERISTICS: PROGRAM MEMORY

DC CHA	RACTER	ISTICS		-	ating Co	d)	s: 3.0V to 3.6V		
DO ONA				Operating temperature			≤ TA ≤ +85°C for Industrial ≤ TA ≤ +125°C for Extended		
Param No.	Symbol	Characteristic	Min.	Typ. ⁽¹⁾	Max.	Units Conditions			
		Program Flash Memory							
D130	EP	Cell Endurance	10,000	_	_	E/W	-40°C to +125°C		
D131	VPR	VDD for Read	3.0	_	3.6	V			
D132b	VPEW	VDD for Self-Timed Write	3.0	_	3.6	V			
D134	TRETD	Characteristic Retention	20	_	_	Year	Provided no other specifications are violated, -40°C to +125°C		
D135	IDDP	Supply Current during Programming	_	10	_	mA			
D136	IPEAK	Instantaneous Peak Current During Start-up	_	_	150	mA			
D137a	TPE	Page Erase Time	19.6	_	20.4	ms	TPE = 147400 FRC cycles, TA = +85°C, See Note 2		
D137b	TPE	Page Erase Time	19.5	_	21.0	ms	TPE = 149243 FRC cycles, TA = +125°C, See Note 2		
D138a	Tww	Word Write Cycle Time	46	_	47.9	μs	Tww = 346 FRC cycles, TA = +85°C, See Note 2		
D138b	Tww	Word Write Cycle Time	45.8	_	48.0	μs	Tww = 346 FRC cycles, TA = +125°C, See Note 2		

Note 1: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

^{2:} Other conditions: FRC = 7.37 MHz, TUN<5:0> = 'b011111 (for Minimum), TUN<5:0> = 'b100000 (for Maximum). This parameter depends on the FRC accuracy (see Table 30-22) and the value of the FRC Oscillator Tuning register (see Register 9-4). For complete details on calculating the Minimum and Maximum time see Section 5.3 "Programming Operations".

TABLE 30-14: AC/DC CHARACTERISTICS: OP AMP/COMPARATOR

DC CH	ARACTERIS	TICS	Standard Operating Conditions (see Note 3): 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +125^{\circ}\text{C}$ for Extended						
Param No.	Symbol	Characteristic	Min.	Typ. ⁽¹⁾	Max.	Units	Conditions		
Compa	rator AC Ch	aracteristics							
CM10	TRESP	Response Time	_	19	_	ns	V+ input step of 100 mV V- input held at VDD/2		
CM11	Тмс2о∨	Comparator Mode Change to Output Valid	_	_	10	μs	_		
Compa	rator DC Ch	aracteristics							
CM30	VOFFSET	Comparator Offset Voltage		±10	_	mV	_		
CM31	VHYST	Input Hysteresis Voltage		30	_	mV	_		
CM32	TRISE/ TFALL	Comparator Output Rise/Fall Time	_	20	_	ns	1 pF load capacitance on input		
CM33	VGAIN	Open Loop Voltage Gain	_	90	_	db	_		
Op am	AC Charac	cteristics							
CM20	SR	Slew Rate	_	9	_	V/µs	10 pF load		
CM21a	Рм	Phase Margin (Configuration A ⁽⁴⁾)	_	55	_	Degree	G = 100V/V; 10 pF load		
CM21b	Рм	Phase Margin (Configuration B ⁽⁵⁾)	_	40	_	Degree	G = 100V/V; 10 pF load		
CM22	Gм	Gain Margin	_	20	_	db	G = 100V/V; 10 pF load		
CM23a	GBW	Gain Bandwidth (Configuration A ⁽⁴⁾)	_	10	_	MHz	10 pF load		
CM23b	GBW	Gain Bandwidth (Configuration B ⁽⁵⁾)	1	6	_	MHz	10 pF load		
Op amp	DC Charac	eteristics							
CM40	VCMR	Common Mode Input Voltage Range	AVss	_	AVDD	V	_		
CM41	CMRR	Common Mode Rejection ratio	_	40	_	db	Vcm = AVDD/2		
CM42	VOFFSET	Op amp Offset Voltage	_	±5	_	mV	_		
CM43	VGAIN	Open Loop Voltage Gain	_	90		db	_		
CM44	los	Input Offset Current	_	_	_		See Pad leakage currents in Table 30-10		
CM45	lв	Input Bias Current	_	_	_	_	See Pad leakage currents in Table 30-10		
CM46	lout	Output Current	_	_	420	μA	With minimum value of RFEEDBACK (CM48)		
CM48		Feedback Resistance Value	8		_	kΩ	_		

Note 1: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated.

^{2:} Resistances can vary by ±10% between Op amps.

^{3:} Device is functional at VBOR < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized.

^{4:} See Figure 25-5 for configuration information.

^{5:} See Figure 25-6 for configuration information.

TABLE 30-14: AC/DC CHARACTERISTICS: OP AMP/COMPARATOR (CONTINUED)

DC CH	ARACTERIS	TICS	Standard Operating Conditions (see Note 3): 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +125^{\circ}\text{C}$ for Extended						
Param No.	Symbol	Characteristic	Min. Typ. ⁽¹⁾ Max. Units Conditions						
CM49a	Vol, Voh	Output Voltage Swing (Configuration A ⁽⁴⁾)	AVss + 0.075	_	AVDD - 0.075	V	_		
CM49b	Vol, Voh	Output Voltage Swing (Configuration B ⁽⁵⁾)	AVss + 0.100 — AVDD - 0.100 V —						
CM51	R _{INT} 1 ⁽²⁾	Internal Resistance 1 (Configuration A ⁽⁴⁾ and B ⁽⁵⁾)	198	264	317	Ω	Min = -40°C Typ = +25°C Max = +125°C		

- Note 1: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated.
 - 2: Resistances can vary by ±10% between Op amps.
 - **3:** Device is functional at VBOR < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized.
 - **4:** See Figure 25-5 for configuration information.
 - **5:** See Figure 25-6 for configuration information.

TABLE 30-15: OP AMP/COMPARATOR REFERENCE VOLTAGE SETTLING TIME SPECIFICATIONS

AC CHA	TICS	Standard Operating Conditions (see Note 2): 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +125^{\circ}\text{C}$ for Extended							
Param.	Symbol	Characteristic	Min. Typ. Max. Units Conditions						
VR310	TSET	Settling Time	_	1	10	μS	See Note 1		

Note 1: Settling time measured while CVRR = 1 and CVR<3:0> bits transition from '0000' to '1111'.

TABLE 30-16: OP AMP/COMPARATOR VOLTAGE REFERENCE DC SPECIFICATIONS

DC CHAP	RACTERIS	TICS	Standard Operating Conditions (see Note 1): 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +125^{\circ}\text{C}$ for Extended							
Param No.	Symbol	Characteristics	Min. Typ. Max. Units Conditions							
VRD310	CVRES	Resolution	CVRSRC/24	_	CVRSRC/32	LSb	_			
VRD311	CVRAA	Absolute Accuracy	_	±25	_	mV	CVRSRC = 3.3V			
VRD313	CVRSRC	Input Reference Voltage	0	_	AVDD + 0.3	V	_			
VRD314	CVRout	Buffer Output Resistance	_	1.5k	_	Ω	_			

Note 1: Device is functional at VBOR < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized.

^{2:} Device is functional at VBOR < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized.

30.2 AC Characteristics and Timing Parameters

This section defines dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X AC characteristics and timing parameters.

TABLE 30-17: TEMPERATURE AND VOLTAGE SPECIFICATIONS - AC

	Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)
AC CHARACTERISTICS	Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +125^{\circ}\text{C}$ for Extended
	Operating voltage VDD range as described in Section 30.1 "DC Characteristics" .

FIGURE 30-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

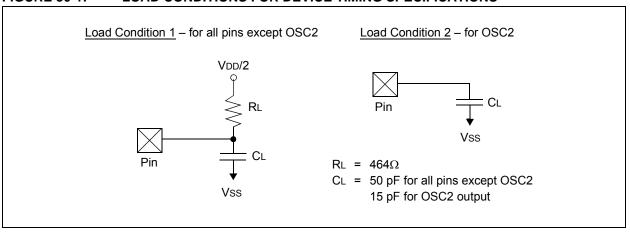


TABLE 30-18: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS

Param No.	Symbol	Characteristic	Min.	Тур.	Max.	Units	Conditions
DO50	Cosco	OSC2 pin	_	_	15	pF	In XT and HS modes when external clock is used to drive OSC1
DO56	Сю	All I/O pins and OSC2	_	_	50	pF	EC mode
DO58	Св	SCLx, SDAx	_	_	400	pF	In I ² C™ mode

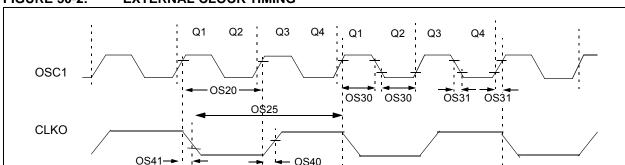


FIGURE 30-2: EXTERNAL CLOCK TIMING

TABLE 30-19: EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHA	RACTE	RISTICS	Standard Oper (unless otherway) Operating temp	vise state				
Param No.	Symb	Characteristic	Min.	Typ. ⁽¹⁾	Max.	Units	Conditions	
OS10	FIN	External CLKI Frequency (External clocks allowed only in EC and ECPLL modes)	DC	_	60	MHz	EC	
Oscilla		Oscillator Crystal Frequency	3.5 10	_	10 25	MHz MHz	XT HS	
OS20 Tosc Tosc = 1/Fosc		8.33	_	DC	ns	+125°C		
		Tosc = 1/Fosc	7.14	_	DC	ns	+85°C	
OS25	TCY	Instruction Cycle Time ⁽²⁾	16.67	_	DC	ns	+125°C	
		Instruction Cycle Time ⁽²⁾	14.28	_	DC	ns	+85°C	
OS30	TosL, TosH	External Clock in (OSC1) High or Low Time	0.375 x Tosc	_	0.625 x Tosc	ns	EC	
OS31	TosR, TosF	External Clock in (OSC1) Rise or Fall Time	_	_	20	ns	EC	
OS40	TckR	CLKO Rise Time ⁽³⁾	_	5.2	_	ns	_	
OS41	TckF	CLKO Fall Time ⁽³⁾	_	5.2	_	ns	_	
OS42	2 GM External Oscillator Transconductance ⁽⁴⁾			12	_	mA/V	HS, VDD = 3.3V TA = +25°C	
			_	- 6		mA/V	XT, VDD = 3.3V TA = +25°C	

Note 1: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

- 2: Instruction cycle period (TcY) equals two times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "Minimum" values with an external clock applied to the OSC1 pin. When an external clock input is used, the "Maximum" cycle time limit is "DC" (no clock) for all devices.
- 3: Measurements are taken in EC mode. The CLKO signal is measured on the OSC2 pin.
- 4: This parameter is characterized, but not tested in manufacturing.

TABLE 30-20: PLL CLOCK TIMING SPECIFICATIONS

AC CHA	RACTERIS	STICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended						
Param No.	Symbol	Characteris	Min.	Typ. ⁽¹⁾	Max.	Units	Conditions			
OS50	FPLLI	PLL Voltage Controll Oscillator (VCO) Inpo Frequency Range	0.8	_	8.0	MHz	ECPLL, XTPLL modes			
OS51	Fsys	On-Chip VCO System Frequency		120		340	MHz	_		
OS52	TLOCK	PLL Start-up Time (Lock Time)		0.9	1.5	3.1	ms	_		
OS53	DCLK	CLKO Stability (Jitter	·) ⁽²⁾	-3	0.5	3	%	_		

- **Note 1:** Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
 - 2: This jitter specification is based on clock cycle-by-clock cycle measurements. To get the effective jitter for individual time bases or communication clocks used by the application, use the following formula:

$$Effective Jitter = \frac{DCLK}{\sqrt{Fosc}}$$

$$\sqrt{Time Base or Communication Clock}$$

For example, if Fosc = 120 MHz and the SPI bit rate = 10 MHz, the effective jitter is as follows:

Effective Jitter =
$$\frac{DCLK}{\sqrt{\frac{120}{10}}}$$
 = $\frac{DCLK}{\sqrt{12}}$ = $\frac{DCLK}{3.464}$

TABLE 30-21: INTERNAL FRC ACCURACY

AC CHA	RACTERISTICS	Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{Ta} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{Ta} \le +125^{\circ}\text{C}$ for Extended							
Param No.	Characteristic	Min.	Тур.	Max.	Units	Jnits Conditions			
	Internal FRC Accuracy @	FRC Fr	equency	= 7.37 N	IHz ⁽¹⁾				
F20a	FRC	-0.9	0.5	+0.9	%	$-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ VDD = 3.0-3.6V			
F20b	FRC	-2	1	+2	%	-40°C ≤ TA ≤ +125°C VDD = 3.0-3.6V			

Note 1: Frequency calibrated at 25°C and 3.3V. TUN bits can be used to compensate for temperature drift.

TABLE 30-22: INTERNAL LPRC ACCURACY

AC CH	ARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +125^{\circ}\text{C}$ for Extended							
Param No.	Characteristic Min Tvn Max Units Conditions									
	LPRC @ 32.768 kHz ⁽¹⁾									
F21a	LPRC	-15	5	+15	%	-40°C ≤ TA ≤ +85°C	VDD = 3.0-3.6V			
F21b	LPRC	-30	10	+30	%	-40°C ≤ TA ≤ +125°C	VDD = 2.0.2.6V/			

Note 1: Change of LPRC frequency as VDD changes.

FIGURE 30-3: I/O TIMING CHARACTERISTICS

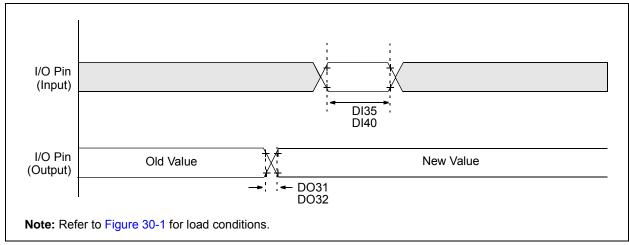


TABLE 30-23: I/O TIMING REQUIREMENTS

AC CHAPACTERISTICS (unless oth				perating Conditions: 3.0V to 3.6V erwise stated) mperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +125^{\circ}\text{C}$ for Extended					
Param No.	Symbol	Character	Min.	Typ. ⁽¹⁾	Max.	Units	Conditions		
DO31	TioR	Port Output Rise Tim	е	_	5	10	ns	_	
DO32	TioF	Port Output Fall Time	;	_	5	10	ns	_	
DI35	TINP	INTx Pin High or Low	20	_		ns			
DI40	TRBP	CNx High or Low Tim	2	_	_	Tcy	_		

Note 1: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

FIGURE 30-4: BOR AND MASTER CLEAR RESET TIMING CHARACTERISTICS

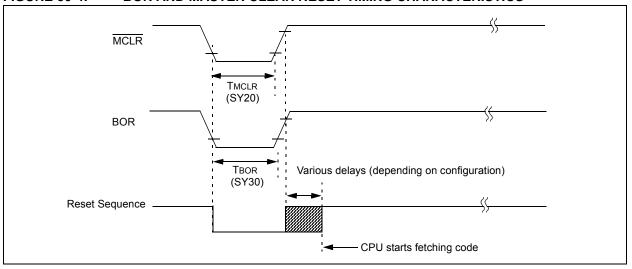


TABLE 30-24: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER TIMING REQUIREMENTS

AC CH	AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +125^{\circ}\text{C}$ for Extended							
Param No.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions				
SY00	Tpu	Power-up Period	_	400	600	μS	_				
SY10	Tost	Oscillator Start-up Time	_	1024 Tosc	_	_	Tosc = OSC1 period				
SY12	TWDT	Watchdog Timer Time-out Period	0.8	_	1.2	ms	WDTPRE = 0, WDTPOST = 0000, using LPRC tolerances indicated in F21 (see Table 30-22)				
			3.2	_	4.8	ms	WDTPRE = 1, WDTPOST = 0000, using LPRC tolerances indicated in F21 (see Table 30-22)				
SY13	Tioz	I/O High-Impedance from MCLR Low or Watchdog Timer Reset	0.68	0.72	1.2	μS	_				
SY20	TMCLR	MCLR Pulse Width (low)	2	_	_	μS	_				
SY30	TBOR	BOR Pulse Width (low)	1	_	_	μS	_				
SY35	TFSCM	Fail-Safe Clock Monitor Delay	_	500	900	μS	-40°C to +85°C				
SY36	TVREG	Voltage regulator standby-to-active mode transition time		_	30	μs	_				
SY37	Toscdfrc	FRC Oscillator start-up delay	46	48	54	μs	_				
SY38	Toscolprc	LPRC Oscillator start-up delay	_	_	70	μs	_				

Note 1: These parameters are characterized but not tested in manufacturing.

^{2:} Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

FIGURE 30-5: TIMER1-TIMER5 EXTERNAL CLOCK TIMING CHARACTERISTICS

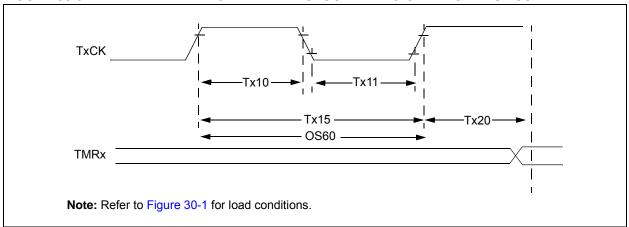


TABLE 30-25: TIMER1 EXTERNAL CLOCK TIMING REQUIREMENTS⁽¹⁾

AC CH	ARACTERIS	TICS	(unle	Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq \text{TA} \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq \text{TA} \leq +125^{\circ}\text{C}$ for Extended						
Param No.	Symbol	Charac	teristic ⁽²⁾	Min.	Тур.	Max.	Units	Conditions		
TA10	ТтхН	TxCK High Time	Synchronous mode	Greater of: 20 or (Tcy + 20)/N	_	_	ns	Must also meet parameter TA15 N = prescaler value (1, 8, 64, 256)		
			Asynchronou	35	_	_	ns	_		
TA11	TTXL	TxCK Low Time	Synchronous mode	Greater of: 20 or (Tcy + 20)/N	_	_	ns	Must also meet parameter TA15 N = prescaler value (1, 8, 64, 256)		
			Asynchronou	10	_	_	ns	_		
TA15	ТтхР	TxCK Input Period	Synchronous mode	Greater of: 40 or (2 Tcy + 40)/N	_	_	ns	N = prescale value (1, 8, 64, 256)		
OS60	Ft1		inge (oscillator etting bit TCS	DC	_	50	kHz	_		
TA20	TCKEXTMRL	Delay from E Clock Edge to	xternal TxCK o Timer	0.75 Tcy + 40	_	1.75 Tcy + 40	ns	_		

Note 1: Timer1 is a Type A.

Increment

2: These parameters are characterized, but are not tested in manufacturing.

TABLE 30-26: TIMER2 AND TIMER4 (TYPE B TIMER) EXTERNAL CLOCK TIMING REQUIREMENTS

AC CH	ARACTERIS	TICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +125^{\circ}\text{C}$ for Extended						
Param No.	Symbol	Charac	cteristic ⁽	1)	Min.	Тур.	Max.	Units	Conditions	
TB10	TtxH	TxCK High Time	Synchro mode	nous	Greater of: 20 or (Tcy + 20)/N	_	_	ns	Must also meet parameter TB15 N = prescale value (1, 8, 64, 256)	
TB11	TtxL	TxCK Low Time	Synchro mode	onous	Greater of: 20 or (Tcy + 20)/N		_	ns	Must also meet parameter TB15 N = prescale value (1, 8, 64, 256)	
TB15	TtxP	TxCK Input Period	Synchro mode	nous	Greater of: 40 or (2 Tcy + 40)/N	_	_	ns	N = prescale value (1, 8, 64, 256)	
TB20	TCKEXTMRL		m External TxCK ge to Timer		0.75 Tcy + 40	_	1.75 Tcy + 40	ns	_	

Note 1: These parameters are characterized, but are not tested in manufacturing.

TABLE 30-27: TIMER3 AND TIMER5 (TYPE C TIMER) EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS				dard Operating C ess otherwise sta rating temperature	ited) e -40°0		or Indus	
Param No.	Symbol	Charac	teristic ⁽¹⁾	Min.	Тур.	Max.	Units	Conditions
TC10	TtxH	TxCK High Time	Synchronous	Tcy + 20	_	_	ns	Must also meet parameter TC15
TC11	TtxL	TxCK Low Time	Synchronous	Tcy + 20	_	_	ns	Must also meet parameter TC15
TC15	TtxP	TxCK Input Period	Synchronous with prescale	<i>'</i>	_	_	ns	N = prescale value (1, 8, 64, 256)
TC20 TCKEXTMRL Delay from External Tx Clock Edge to Timer In ment					_	1.75 Tcy + 40	ns	_

Note 1: These parameters are characterized, but are not tested in manufacturing.

FIGURE 30-6: INPUT CAPTURE (ICx) TIMING CHARACTERISTICS

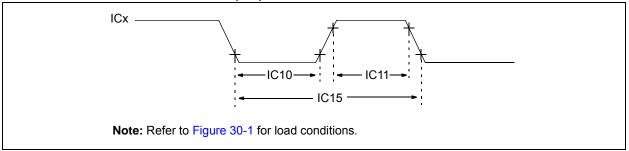


TABLE 30-28: INPUT CAPTURE MODULE TIMING REQUIREMENTS

AC CHA	Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +125^{\circ}\text{C}$ for Extended							
Param. No.	Symbol	Charac	cteristics ⁽¹⁾	Min.	Max.	Max. Units Conditions		
IC10	TccL	ICx Input	t Low Time	Greater of 12.5 + 25 or (0.5 Tcy/N) + 25	_	ns	Must also meet parameter IC15.	
IC11	TccH	ICx Input	t High Time	Greater of 12.5 + 25 or (0.5 Tcy/N) + 25	_	ns	Must also meet parameter IC15.	N = prescale value (1, 4, 16)
IC15	TccP	ICx Input	t Period	Greater of 25 + 50 or (1 Tcy/N) + 50	_	ns	_	

Note 1: These parameters are characterized, but not tested in manufacturing.

FIGURE 30-7: OUTPUT COMPARE MODULE (OCx) TIMING CHARACTERISTICS

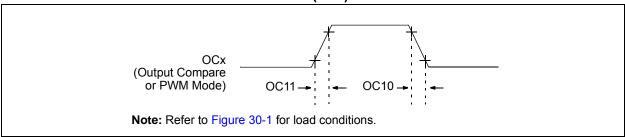


TABLE 30-29: OUTPUT COMPARE MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended						
Param No.	Symbol	Characteristic ⁽¹⁾	Min. Typ. Max. Units Conditions						
OC10	TccF	OCx Output Fall Time	_	_	_	ns	See parameter DO32		
OC11	TccR	OCx Output Rise Time	ns See parameter DO31						

Note 1: These parameters are characterized but not tested in manufacturing.

FIGURE 30-8: OC/PWM MODULE TIMING CHARACTERISTICS

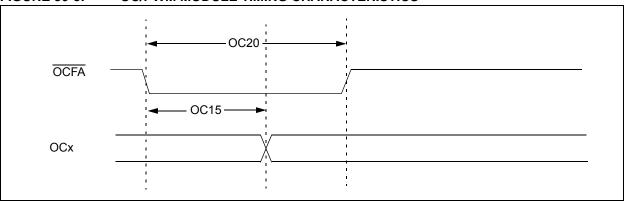


TABLE 30-30: OC/PWM MODE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{Ta} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{Ta} \le +125^{\circ}\text{C}$ for Extended					
Param No.	Symbol	Characteristic ⁽¹⁾	Min. Typ. Max. Units Conditions					
OC15	TFD	Fault Input to PWM I/O Change	_	_	Tcy + 20	ns		
OC20	TFLT	Fault Input Pulse Width	Tcy + 20 — ns —					

Note 1: These parameters are characterized but not tested in manufacturing.

FIGURE 30-9: HIGH-SPEED PWM MODULE FAULT TIMING CHARACTERISTICS (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

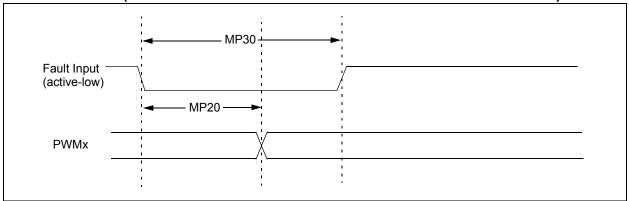


FIGURE 30-10: HIGH-SPEED PWM MODULE TIMING CHARACTERISTICS (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

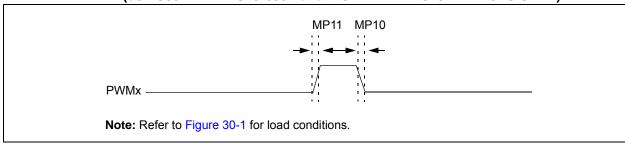


TABLE 30-31: HIGH-SPEED PWM MODULE TIMING REQUIREMENTS (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

AC CHARACTERISTICS				otherwis	se stated rature -) 40°C ≤ 1	3.0V to 3.6V $\Gamma A \leq +85^{\circ} C \text{ for Industrial}$ $\Gamma A \leq +125^{\circ} C \text{ for Extended}$		
Param No.	Symbol	Characteristic ⁽¹⁾	Min. Typ. Max. Units Conditions						
MP10	TFPWM	PWM Output Fall Time	_	_	_	ns	See parameter DO32		
MP11	TRPWM	PWM Output Rise Time	_	_	_	ns	See parameter DO31		
MP20	TFD	Fault Input ↓ to PWM I/O Change	15 ns						
MP30	TFH	Fault Input Pulse Width	15	_	_	ns	_		

Note 1: These parameters are characterized but not tested in manufacturing.

FIGURE 30-11: TIMERQ (QEI MODULE) EXTERNAL CLOCK TIMING CHARACTERISTICS (dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY)

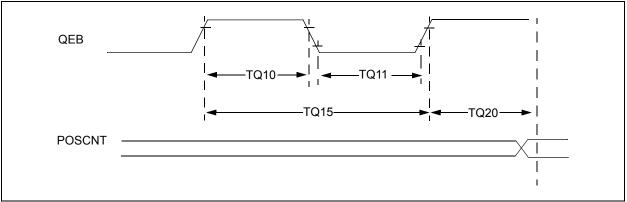


TABLE 30-32: QEI MODULE EXTERNAL CLOCK TIMING REQUIREMENTS (dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY)

AC CHARACTERISTICS Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +125^{\circ}\text{C}$ for Extended									
Param No.	Symbol	Charac	teristic ⁽¹⁾	Min. Typ. Max. Units Co					
TQ10	TtQH	TQCK High Time	Synchronous, with prescaler	Greater of 12.5 + 25 or (0.5 Tcy/N) + 25	_	_	ns	Must also meet parameter TQ15.	
TQ11	TtQL	TQCK Low Time	Synchronous, with prescaler	Greater of 12.5 + 25 or (0.5 Tcy/N) + 25	_	_	ns	Must also meet parameter TQ15.	
TQ15	TtQP	TQCP Input Period	Synchronous, with prescaler	Greater of 25 + 50 or (1 Tcy/N) + 50	_	_	ns	_	
TQ20	TCKEXTMRL	Delay from Ex Clock Edge to ment		_	1	Tcy	_	_	

Note 1: These parameters are characterized but not tested in manufacturing.



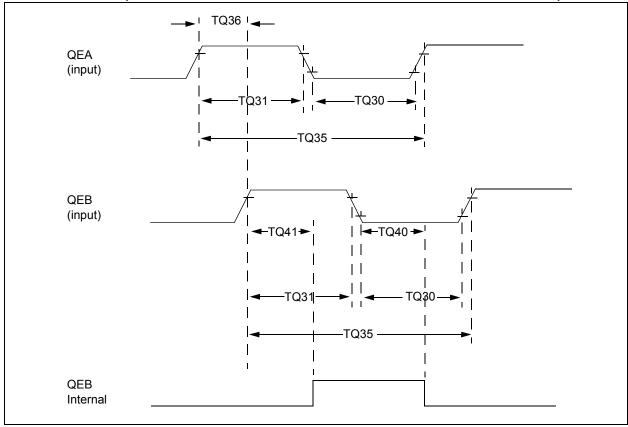
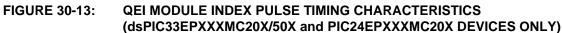


TABLE 30-33: QUADRATURE DECODER TIMING REQUIREMENTS (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended						
Param No.	Symbol Characteristic ⁽¹⁾ Typ. ⁽²⁾ Max. Units						Conditions		
TQ30	TquL	Quadrature Input Low Time		6 Tcy	_	ns	_		
TQ31	TquH	Quadrature Input High Time		6 Tcy	_	ns	_		
TQ35	TquIN	Quadrature Input Period		12 TcY	_	ns	_		
TQ36	TquP	Quadrature Phase Period		3 Tcy	_	ns	_		
TQ40	TQUFL	Filter Time to Recognize Low with Digital Filter	ν,	3 * N * Tcy	_	ns	N = 1, 2, 4, 16, 32, 64, 128 and 256 (Note 3)		
TQ41	TQUFH	Filter Time to Recognize Hig with Digital Filter	h,	3 * N * Tcy	_	ns	N = 1, 2, 4, 16, 32, 64, 128 and 256 (Note 3)		

- Note 1: These parameters are characterized but not tested in manufacturing.
 - 2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
 - 3: N = Index Channel Digital Filter Clock Divide Select bits. Refer to **Section 15. "Quadrature Encoder Interface (QEI)"** (DS70601) in the "dsPIC33E/PIC24E Family Reference Manual". Please see the Microchip web site for the latest family reference manual sections.



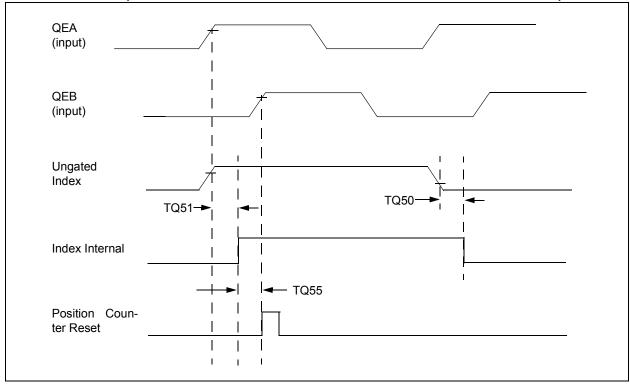


TABLE 30-34: QEI INDEX PULSE TIMING REQUIREMENTS
(dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

AC CHA	RACTERI	STICS	-	•	40°C ≤ T/	4≤ +85°	C for Industrial C for Extended
Param No.	Symbol	Characteristic	c ⁽¹⁾	Min.	Max.	Units	Conditions
TQ50	TqIL	Filter Time to Recognize with Digital Filter	Low,	3 * N * Tcy	_	ns	N = 1, 2, 4, 16, 32, 64, 128 and 256 (Note 2)
TQ51	TqiH	Filter Time to Recognize with Digital Filter	High,	3 * N * Tcy	_	ns	N = 1, 2, 4, 16, 32, 64, 128 and 256 (Note 2)
TQ55	Tqidxr	Index Pulse Recognized Counter Reset (ungated		3 Tcy	_	ns	_

- Note 1: These parameters are characterized but not tested in manufacturing.
 - 2: Alignment of index pulses to QEA and QEB is shown for position counter Reset timing only. Shown for forward direction only (QEA leads QEB). Same timing applies for reverse direction (QEA lags QEB) but index pulse recognition occurs on falling edge.

TABLE 30-35: SPI2 MAXIMUM DATA/CLOCK RATE SUMMARY

AC CHARAG	CTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +125^{\circ}\text{C}$ for Extended						
Maximum Data Rate	Master Transmit Only (Half-Duplex)	Master Transmit/Receive (Full-Duplex)	Slave Transmit/Receive (Full-Duplex)	CKE	СКР	SMP			
15 MHz	Table 30-35	_	_	0,1	0,1	0,1			
9 MHz	_	Table 30-36		1	0,1	1			
9 MHz	_	Table 30-37		0	0,1	1			
15 MHz	_	_	Table 30-38	1	0	0			
11 MHz	_	_	Table 30-39	1	1	0			
15 MHz	_	_	Table 30-40	0	1	0			
11 MHz	<u> </u>	_	Table 30-41	0	0	0			

FIGURE 30-14: SPI2 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY CKE = 0) TIMING CHARACTERISTICS

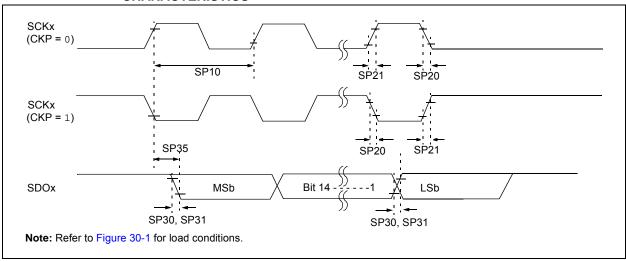
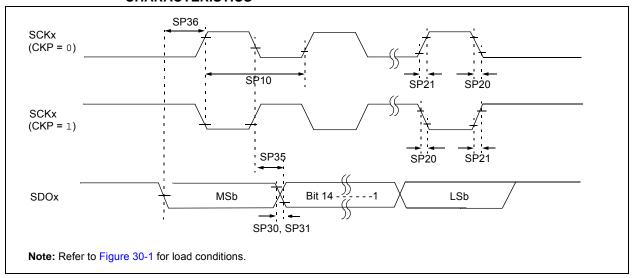


FIGURE 30-15: SPI2 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY CKE = 1) TIMING CHARACTERISTICS



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TABLE 30-36: SPI2 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +125^{\circ}\text{C}$ for Extended				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP10	TscP	Maximum SCK Frequency	_	_	15	MHz	See Note 3
SP20	TscF	SCKx Output Fall Time	_	_	_	ns	See parameter DO32 and Note 4
SP21	TscR	SCKx Output Rise Time	_		_	ns	See parameter DO31 and Note 4
SP30	TdoF	SDOx Data Output Fall Time	_		_	ns	See parameter DO32 and Note 4
SP31	TdoR	SDOx Data Output Rise Time	_	_	_	ns	See parameter DO31 and Note 4
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	_	6	20	ns	_
SP36	TdiV2scH, TdiV2scL	SDOx Data Output Setup to First SCKx Edge	30	_		ns	_

Note 1: These parameters are characterized, but are not tested in manufacturing.

- 2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.
- **3:** The minimum clock period for SCKx is 66.7 ns. Therefore, the clock generated in Master mode must not violate this specification.
- 4: Assumes 50 pF load on all SPIx pins.

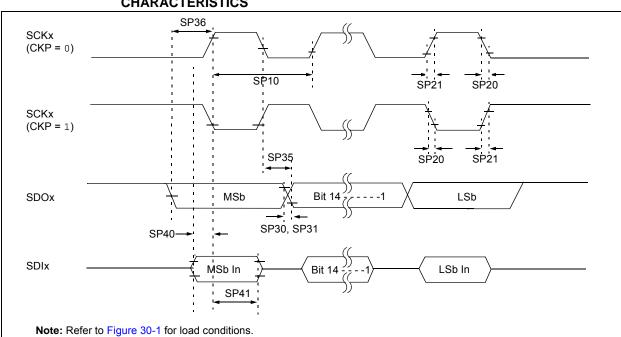


FIGURE 30-16: SPI2 MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1) TIMING CHARACTERISTICS

TABLE 30-37: SPI2 MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1) TIMING REQUIREMENTS

AC CHA	RACTERIST	Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +125^{\circ}\text{C}$ for Extended					
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP10	TscP	Maximum SCK Frequency		_	9	MHz	See Note 3
SP20	TscF	SCKx Output Fall Time		_	_	ns	See parameter DO32 and Note 4
SP21	TscR	SCKx Output Rise Time	_	_	_	ns	See parameter DO31 and Note 4
SP30	TdoF	SDOx Data Output Fall Time	1	_	_	ns	See parameter DO32 and Note 4
SP31	TdoR	SDOx Data Output Rise Time		_	_	ns	See parameter DO31 and Note 4
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	_	6	20	ns	_
SP36	TdoV2sc, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	_	_	ns	_
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	_		ns	_
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	_	_	ns	_

- **Note 1:** These parameters are characterized, but are not tested in manufacturing.
 - 2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.
 - **3:** The minimum clock period for SCKx is 111 ns. The clock generated in Master mode must not violate this specification.
 - 4: Assumes 50 pF load on all SPIx pins.

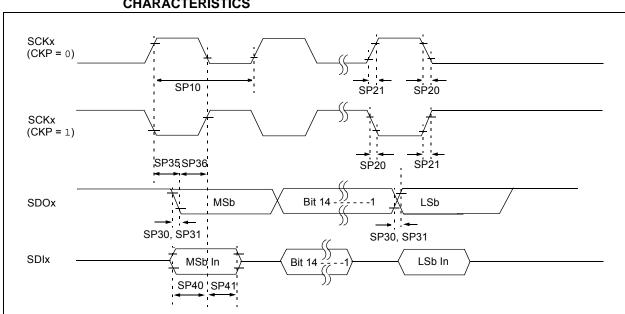


FIGURE 30-17: SPI2 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING CHARACTERISTICS

TABLE 30-38: SPI2 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING REQUIREMENTS

	11/11/	ZUINLIVILIVIS						
			Standard (unless o		g Condition	ons: 3.0V	to 3.6V	
AC CHA	RACTERIST	ICS	Operating temperature $-40^{\circ}\text{C} \le \text{Ta} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{Ta} \le +125^{\circ}\text{C}$ for Extended					
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions	
SP10	TscP	Maximum SCK Frequency	_	_	9	MHz	-40°C to +125°C and see Note 3	
SP20	TscF	SCKx Output Fall Time	_	_	_	ns	See parameter DO32 and Note 4	
SP21	TscR	SCKx Output Rise Time	_	_	-	ns	See parameter DO31 and Note 4	
SP30	TdoF	SDOx Data Output Fall Time	_	_	_	ns	See parameter DO32 and Note 4	
SP31	TdoR	SDOx Data Output Rise Time	_	_	_	ns	See parameter DO31 and Note 4	
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	_	6	20	ns	_	
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	_	_	ns	_	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	_	_	ns	_	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	_	_	ns	_	

- Note 1: These parameters are characterized, but are not tested in manufacturing.
 - 2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.
 - 3: The minimum clock period for SCKx is 111 ns. The clock generated in Master mode must not violate this specification.
 - 4: Assumes 50 pF load on all SPIx pins.

Note: Refer to Figure 30-1 for load conditions.

FIGURE 30-18: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0) TIMING CHARACTERISTICS

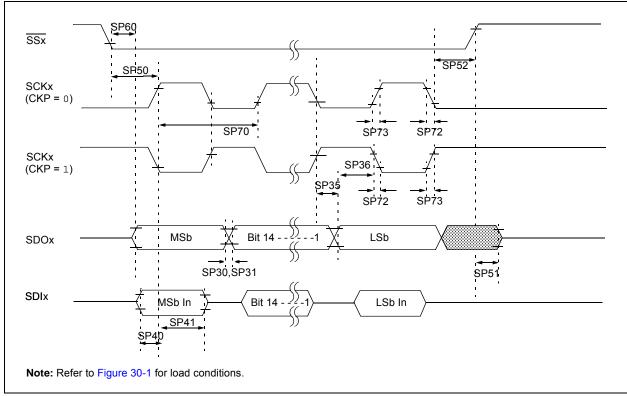


TABLE 30-39: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)					
			Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +125^{\circ}\text{C}$ for Extended					
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions	
SP70	TscP	Maximum SCK Input Frequency	_	_	15	MHz	See Note 3	
SP72	TscF	SCKx Input Fall Time	_	_	_	ns	See parameter DO32 and Note 4	
SP73	TscR	SCKx Input Rise Time	_	_	_	ns	See parameter DO31 and Note 4	
SP30	TdoF	SDOx Data Output Fall Time	_	_	_	ns	See parameter DO32 and Note 4	
SP31	TdoR	SDOx Data Output Rise Time	_		_	ns	See parameter DO31 and Note 4	
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	_	6	20	ns	_	
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	_	_	ns	_	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	_	_	ns	_	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	_	_	ns	_	
SP50	TssL2scH, TssL2scL	SSx ↓ to SCKx ↑ or SCKx ↓ Input	120	_	_	ns	_	
SP51	TssH2doZ	SSx ↑ to SDOx Output High-Impedance ⁽⁴⁾	10	_	50	ns	_	
SP52	TscH2ssH TscL2ssH	SSx ↑ after SCKx Edge	1.5 Tcy + 40	_	_	ns	See Note 4	
SP60	TssL2doV	SDOx Data Output Valid after SSx Edge	_	_	50	ns	_	

- Note 1: These parameters are characterized, but are not tested in manufacturing.
 - 2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.
 - **3:** The minimum clock period for SCKx is 66.7 ns. Therefore, the SCK clock generated by the Master must not violate this specification.
 - 4: Assumes 50 pF load on all SPIx pins.

FIGURE 30-19: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0) TIMING CHARACTERISTICS

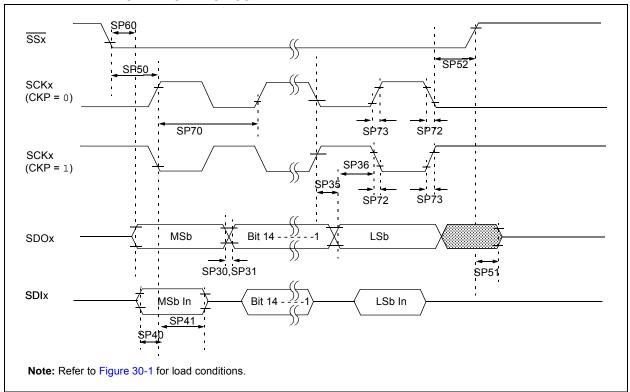


TABLE 30-40: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended					
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions	
SP70	TscP	Maximum SCK Input Frequency	_	_	11	MHz	See Note 3	
SP72	TscF	SCKx Input Fall Time	_	_	_	ns	See parameter DO32 and Note 4	
SP73	TscR	SCKx Input Rise Time	_	_	_	ns	See parameter DO31 and Note 4	
SP30	TdoF	SDOx Data Output Fall Time	_	_	_	ns	See parameter DO32 and Note 4	
SP31	TdoR	SDOx Data Output Rise Time	_		_	ns	See parameter DO31 and Note 4	
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	_	6	20	ns	_	
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	_	_	ns	_	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	_	_	ns	_	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	_	_	ns	_	
SP50	TssL2scH, TssL2scL	SSx ↓ to SCKx ↑ or SCKx ↓ Input	120	_	_	ns	_	
SP51	TssH2doZ	SSx ↑ to SDOx Output High-Impedance ⁽⁴⁾	10	_	50	ns	_	
SP52	TscH2ssH TscL2ssH	SSx ↑ after SCKx Edge	1.5 Tcy + 40	_	_	ns	See Note 4	
SP60	TssL2doV	SDOx Data Output Valid after SSx Edge	_		50	ns	_	

- **Note 1:** These parameters are characterized, but are not tested in manufacturing.
 - **2:** Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.
 - **3:** The minimum clock period for SCKx is 91 ns. Therefore, the SCK clock generated by the Master must not violate this specification.
 - 4: Assumes 50 pF load on all SPIx pins.

FIGURE 30-20: SPI2 SLAVE MODE (FULL-DUPLEX CKE = 0, CKP = 1, SMP = 0) TIMING CHARACTERISTICS

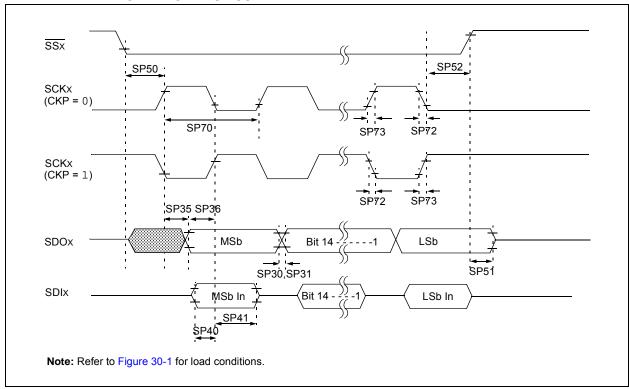


TABLE 30-41: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended					
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions	
SP70	TscP	Maximum SCK Input Frequency	_	_	15	MHz	See Note 3	
SP72	TscF	SCKx Input Fall Time	_	_	_	ns	See parameter DO32 and Note 4	
SP73	TscR	SCKx Input Rise Time	_	_	_	ns	See parameter DO31 and Note 4	
SP30	TdoF	SDOx Data Output Fall Time	_	_	_	ns	See parameter DO32 and Note 4	
SP31	TdoR	SDOx Data Output Rise Time	_	_	_	ns	See parameter DO31 and Note 4	
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	_	6	20	ns	_	
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	_	_	ns	_	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	_	_	ns	_	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	_	_	ns	_	
SP50	TssL2scH, TssL2scL	SSx ↓ to SCKx ↑ or SCKx ↓ Input	120	_	_	ns	_	
SP51	TssH2doZ	SSx ↑ to SDOx Output High-Impedance ⁽⁴⁾	10	_	50	ns	_	
SP52	TscH2ssH TscL2ssH	SSx ↑ after SCKx Edge	1.5 Tcy + 40	_	_	ns	See Note 4	

Note 1: These parameters are characterized, but are not tested in manufacturing.

- **2:** Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.
- **3:** The minimum clock period for SCKx is 66.7 ns. Therefore, the SCK clock generated by the Master must not violate this specification.
- 4: Assumes 50 pF load on all SPIx pins.

FIGURE 30-21: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING CHARACTERISTICS

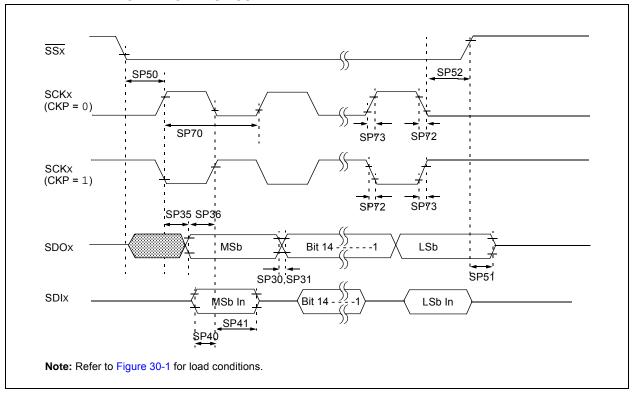


TABLE 30-42: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +125^{\circ}\text{C}$ for Extende					
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions	
SP70	TscP	Maximum SCK Input Frequency	_	_	11	MHz	See Note 3	
SP72	TscF	SCKx Input Fall Time	_	_	_	ns	See parameter DO32 and Note 4	
SP73	TscR	SCKx Input Rise Time	_	_	_	ns	See parameter DO31 and Note 4	
SP30	TdoF	SDOx Data Output Fall Time	_	_	_	ns	See parameter DO32 and Note 4	
SP31	TdoR	SDOx Data Output Rise Time	_	_	_	ns	See parameter DO31 and Note 4	
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	_	6	20	ns	_	
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	_	_	ns	_	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	_	_	ns	_	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	_	_	ns	_	
SP50	TssL2scH, TssL2scL	SSx ↓ to SCKx ↑ or SCKx ↓ Input	120	_	_	ns	_	
SP51	TssH2doZ	SSx ↑ to SDOx Output High-Impedance ⁽⁴⁾	10	_	50	ns	_	
SP52	TscH2ssH TscL2ssH	SSx ↑ after SCKx Edge	1.5 Tcy + 40	_	_	ns	See Note 4	

- **2:** Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.
- **3:** The minimum clock period for SCKx is 91 ns. Therefore, the SCK clock generated by the Master must not violate this specification.
- 4: Assumes 50 pF load on all SPIx pins.

TABLE 30-43: SPI1 MAXIMUM DATA/CLOCK RATE SUMMARY

AC CHARAC	CTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{Ta} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{Ta} \le +125^{\circ}\text{C}$ for Extended					
Maximum Data Rate	Master Transmit Only (Half-Duplex)	Master Transmit/Receive (Full-Duplex)	Slave Transmit/Receive (Full-Duplex)	CKE	СКР	SMP		
15 MHz	Table 30-44		_	0,1	0,1	0,1		
10 MHz	_	Table 30-45	_	1	0,1	1		
10 MHz	_	Table 30-46	_	0	0,1	1		
15 MHz	_		Table 30-47	1	0	0		
11 MHz	_		Table 30-48	1	1	0		
15 MHz	_	_	Table 30-49	0	1	0		
11 MHz	_		Table 30-50	0	0	0		

FIGURE 30-22: SPI1 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY CKE = 0) TIMING CHARACTERISTICS

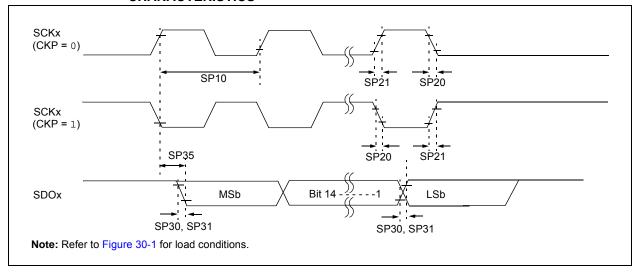


FIGURE 30-23: SPI1 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY CKE = 1) TIMING CHARACTERISTICS

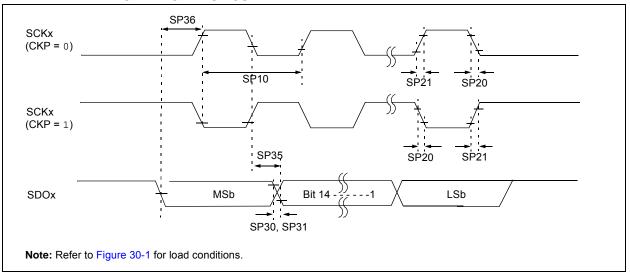


TABLE 30-44: SPI1 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY) TIMING REQUIREMENTS

AC CHARACTERISTICS			(unless	Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +125^{\circ}\text{C}$ for Extended					
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions		
SP10	TscP	Maximum SCK Frequency	_	_	15	MHz	See Note 3		
SP20	TscF	SCKx Output Fall Time	_	_	_	ns	See parameter DO32 and Note 4		
SP21	TscR	SCKx Output Rise Time	_	_	_	ns	See parameter DO31 and Note 4		
SP30	TdoF	SDOx Data Output Fall Time	_	_	_	ns	See parameter DO32 and Note 4		
SP31	TdoR	SDOx Data Output Rise Time	_	_	_	ns	See parameter DO31 and Note 4		
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	_	6	20	ns	_		
SP36	TdiV2scH, TdiV2scL	SDOx Data Output Setup to First SCKx Edge	30	_	_	ns	_		

- 2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.
- **3:** The minimum clock period for SCKx is 66.7 ns. Therefore, the clock generated in Master mode must not violate this specification.
- 4: Assumes 50 pF load on all SPIx pins.

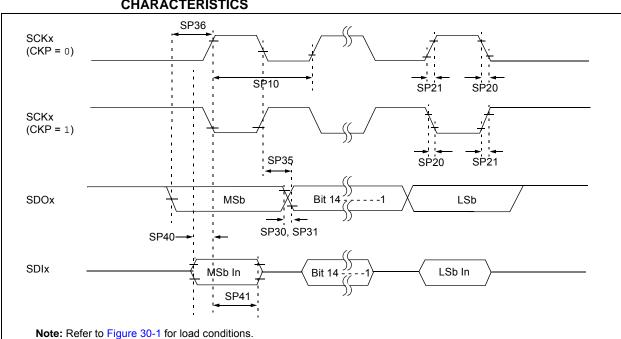


FIGURE 30-24: SPI1 MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1) TIMING CHARACTERISTICS

TABLE 30-45: SPI1 MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1) TIMING REQUIREMENTS

AC CHA	RACTERIST	ics	Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +125^{\circ}\text{C}$ for Extended					
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions	
SP10	TscP	Maximum SCK Frequency	_	_	10	MHz	See Note 3	
SP20	TscF	SCKx Output Fall Time	_	_	_	ns	See parameter DO32 and Note 4	
SP21	TscR	SCKx Output Rise Time	_	_	_	ns	See parameter DO31 and Note 4	
SP30	TdoF	SDOx Data Output Fall Time		_	_	ns	See parameter DO32 and Note 4	
SP31	TdoR	SDOx Data Output Rise Time	_	_	_	ns	See parameter DO31 and Note 4	
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	_	6	20	ns	_	
SP36	TdoV2sc, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	_	_	ns	_	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	_	_	ns	_	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	_	_	ns	_	

Note 1: These parameters are characterized, but are not tested in manufacturing.

- 2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.
- 3: The minimum clock period for SCKx is 100 ns. The clock generated in Master mode must not violate this specification.
- 4: Assumes 50 pF load on all SPIx pins.

FIGURE 30-25: SPI1 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING CHARACTERISTICS

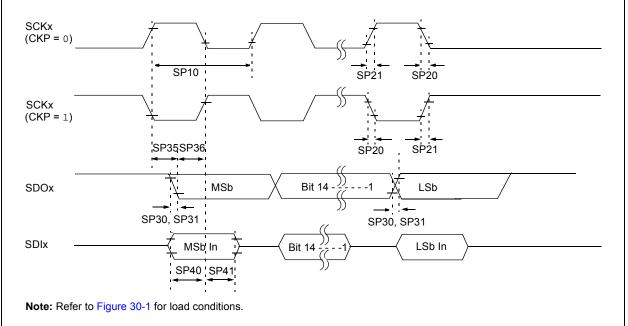


TABLE 30-46: SPI1 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING REQUIREMENTS

	11/11/	ZUINLIVILIVIS						
	Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)							
AC CHA	RACTERIST	ICS	Operating		ture -40°		+85°C for Industrial +125°C for Extended	
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Conditions			
SP10	TscP	Maximum SCK Frequency	_	_	10	MHz	-40°C to +125°C and see Note 3	
SP20	TscF	SCKx Output Fall Time	_	_	_	ns	See parameter DO32 and Note 4	
SP21	TscR	SCKx Output Rise Time	_	_	-	ns	See parameter DO31 and Note 4	
SP30	TdoF	SDOx Data Output Fall Time	_	_	_	ns	See parameter DO32 and Note 4	
SP31	TdoR	SDOx Data Output Rise Time	_	_	_	ns	See parameter DO31 and Note 4	
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	_	6	20	ns	_	
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	_	-	ns	_	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	_	_	ns	_	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	_	_	ns	_	

- Note 1: These parameters are characterized, but are not tested in manufacturing.
 - 2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.
 - 3: The minimum clock period for SCKx is 100 ns. The clock generated in Master mode must not violate this specification.
 - 4: Assumes 50 pF load on all SPIx pins.

FIGURE 30-26: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0) TIMING CHARACTERISTICS

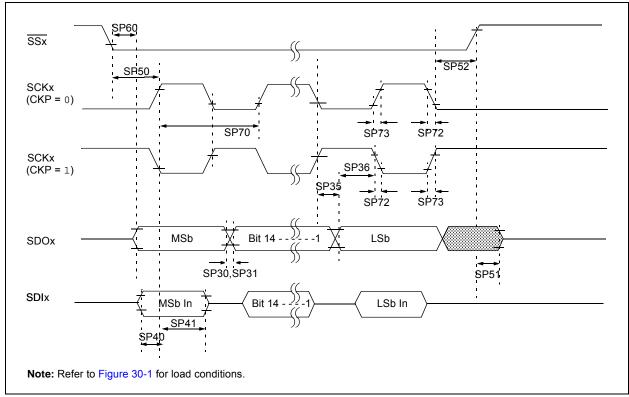


TABLE 30-47: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0) TIMING REQUIREMENTS

AC CHA	ARACTERIST	rics	Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{Ta} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{Ta} \le +125^{\circ}\text{C}$ for Extende					
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Min. Typ. ⁽²⁾ Max. Units				
SP70	TscP	Maximum SCK Input Frequency	_	_	15	MHz	See Note 3	
SP72	TscF	SCKx Input Fall Time	_		_	ns	See parameter DO32 and Note 4	
SP73	TscR	SCKx Input Rise Time	_	_	_	ns	See parameter DO31 and Note 4	
SP30	TdoF	SDOx Data Output Fall Time	_	_	_	ns	See parameter DO32 and Note 4	
SP31	TdoR	SDOx Data Output Rise Time	_		_	ns	See parameter DO31 and Note 4	
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	_	6	20	ns	_	
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	_	-	ns	_	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	_	_	ns	_	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	_	_	ns	_	
SP50	TssL2scH, TssL2scL	SSx ↓ to SCKx ↑ or SCKx ↓ Input	120	_	_	ns	_	
SP51	TssH2doZ	SSx ↑ to SDOx Output High-Impedance ⁽⁴⁾	10	_	50	ns	_	
SP52	TscH2ssH TscL2ssH	SSx ↑ after SCKx Edge	1.5 Tcy + 40	_		ns	See Note 4	
SP60	TssL2doV	SDOx Data Output Valid after SSx Edge	_	_	50	ns	_	

4: Assumes 50 pF load on all SPIx pins.

^{2:} Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

^{3:} The minimum clock period for SCKx is 66.7 ns. Therefore, the SCK clock generated by the Master must not violate this specification.

FIGURE 30-27: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0) TIMING CHARACTERISTICS

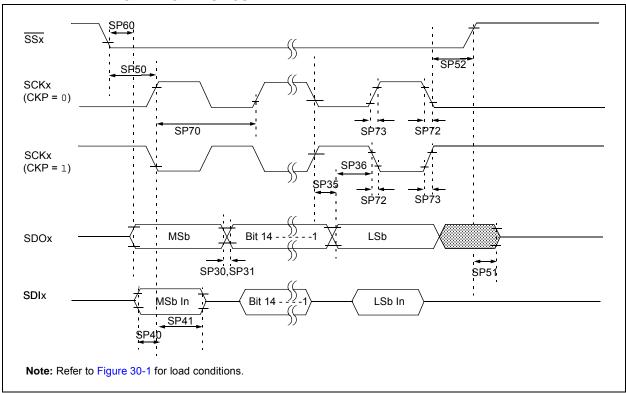


TABLE 30-48: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0) TIMING REQUIREMENTS

AC CHA	AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +125^{\circ}\text{C}$ for Extended					
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Min. Typ. ⁽²⁾ Max.			Conditions		
SP70	TscP	Maximum SCK Input Frequency	_	_	11	MHz	See Note 3		
SP72	TscF	SCKx Input Fall Time	_	_	_	ns	See parameter DO32 and Note 4		
SP73	TscR	SCKx Input Rise Time	_	_	_	ns	See parameter DO31 and Note 4		
SP30	TdoF	SDOx Data Output Fall Time	_	_	_	ns	See parameter DO32 and Note 4		
SP31	TdoR	SDOx Data Output Rise Time	_		_	ns	See parameter DO31 and Note 4		
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	_	6	20	ns	_		
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	_	_	ns	_		
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	_	_	ns	_		
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	_	_	ns	_		
SP50	TssL2scH, TssL2scL	SSx ↓ to SCKx ↑ or SCKx ↓ Input	120	_	_	ns	_		
SP51	TssH2doZ	SSx ↑ to SDOx Output High-Impedance ⁽⁴⁾	10	_	50	ns	_		
SP52	TscH2ssH, TscL2ssH	SSx ↑ after SCKx Edge	1.5 Tcy + 40	_	_	ns	See Note 4		
SP60	TssL2doV	SDOx Data Output Valid after SSx Edge	_		50	ns	_		

- **Note 1:** These parameters are characterized, but are not tested in manufacturing.
 - **2:** Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.
 - **3:** The minimum clock period for SCKx is 91 ns. Therefore, the SCK clock generated by the Master must not violate this specification.
 - 4: Assumes 50 pF load on all SPIx pins.

FIGURE 30-28: SPI1 SLAVE MODE (FULL-DUPLEX CKE = 0, CKP = 1, SMP = 0) TIMING CHARACTERISTICS

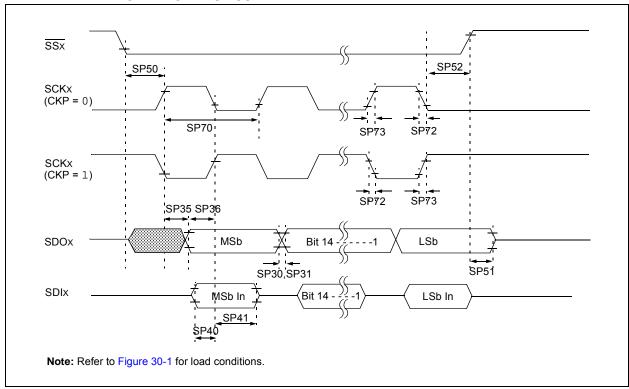


TABLE 30-49: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +125^{\circ}\text{C}$ for Extende					
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions	
SP70	TscP	Maximum SCK Input Frequency	_	_	15	MHz	See Note 3	
SP72	TscF	SCKx Input Fall Time	_	_	_	ns	See parameter DO32 and Note 4	
SP73	TscR	SCKx Input Rise Time	_	_	_	ns	See parameter DO31 and Note 4	
SP30	TdoF	SDOx Data Output Fall Time	_	_	_	ns	See parameter DO32 and Note 4	
SP31	TdoR	SDOx Data Output Rise Time	_	_	_	ns	See parameter DO31 and Note 4	
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	_	6	20	ns	_	
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	_	_	ns	_	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	_	_	ns	_	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	_	_	ns	_	
SP50	TssL2scH, TssL2scL	SSx ↓ to SCKx ↑ or SCKx ↓ Input	120	_	_	ns	_	
SP51	TssH2doZ	SSx ↑ to SDOx Output High-Impedance ⁽⁴⁾	10	_	50	ns	_	
SP52	TscH2ssH, TscL2ssH	SSx ↑ after SCKx Edge	1.5 Tcy + 40	_	_	ns	See Note 4	

- **2:** Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.
- **3:** The minimum clock period for SCKx is 66.7 ns. Therefore, the SCK clock generated by the Master must not violate this specification.
- 4: Assumes 50 pF load on all SPIx pins.

FIGURE 30-29: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING CHARACTERISTICS

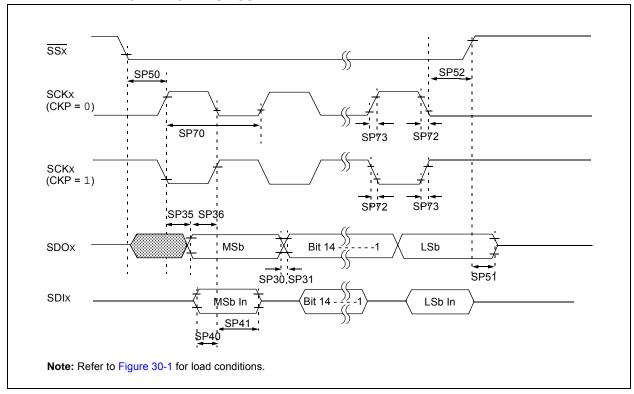


TABLE 30-50: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industria $-40^{\circ}\text{C} \le \text{TA} \le +125^{\circ}\text{C}$ for Extended				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP70	TscP	Maximum SCK Input Frequency	_	_	11	MHz	See Note 3
SP72	TscF	SCKx Input Fall Time	_	_	_	ns	See parameter DO32 and Note 4
SP73	TscR	SCKx Input Rise Time	_	_	_	ns	See parameter DO31 and Note 4
SP30	TdoF	SDOx Data Output Fall Time	_	_	_	ns	See parameter DO32 and Note 4
SP31	TdoR	SDOx Data Output Rise Time	_	_	_	ns	See parameter DO31 and Note 4
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	_	6	20	ns	_
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	_	_	ns	_
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	_	_	ns	_
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	_	_	ns	_
SP50	TssL2scH, TssL2scL	SSx ↓ to SCKx ↑ or SCKx ↓ Input	120	_	_	ns	_
SP51	TssH2doZ	SSx ↑ to SDOx Output High-Impedance ⁽⁴⁾	10	_	50	ns	_
SP52	TscH2ssH, TscL2ssH	SSx ↑ after SCKx Edge	1.5 Tcy + 40	_	_	ns	See Note 4

- **2:** Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.
- **3:** The minimum clock period for SCKx is 91 ns. Therefore, the SCK clock generated by the Master must not violate this specification.
- 4: Assumes 50 pF load on all SPIx pins.

FIGURE 30-30: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (MASTER MODE)

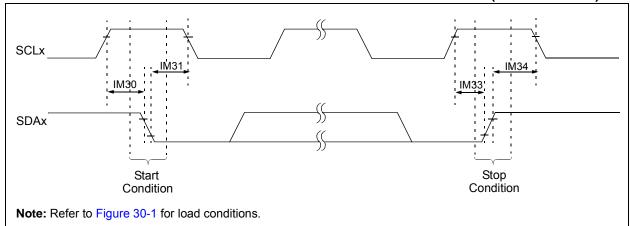


FIGURE 30-31: I2Cx BUS DATA TIMING CHARACTERISTICS (MASTER MODE)

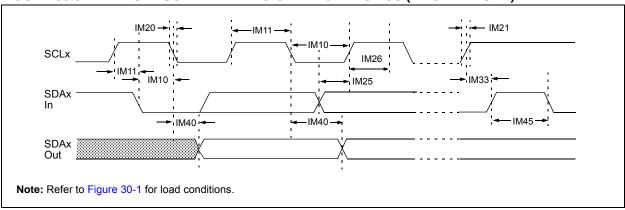


TABLE 30-51: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE)

AC CHA	ARACTER	ISTICS		Standard Operatir (unless otherwise Operating tempera	stated) ture -40)°C≤ Ta≤	v to 3.6v +85°C for Industrial +125°C for Extended
Param No.	Symbol	Charac	teristic	Min. ⁽¹⁾	Max.	Units	Conditions
IM10	TLO:SCL	Clock Low Time	100 kHz mode	Tcy/2 (BRG + 2)	_	μS	_
			400 kHz mode	Tcy/2 (BRG + 2)	_	μS	_
			1 MHz mode ⁽²⁾	Tcy/2 (BRG + 2)	_	μS	_
IM11	THI:SCL	Clock High Time	100 kHz mode	Tcy/2 (BRG + 2)	_	μS	_
			400 kHz mode	Tcy/2 (BRG + 2)	_	μS	_
			1 MHz mode ⁽²⁾	Tcy/2 (BRG + 2)	_	μS	_
IM20	TF:SCL	SDAx and SCLx	100 kHz mode	_	300	ns	CB is specified to be
		Fall Time	400 kHz mode	20 + 0.1 CB	300	ns	from 10 to 400 pF
			1 MHz mode ⁽²⁾	_	100	ns	
IM21	TR:SCL	SDAx and SCLx	100 kHz mode	_	1000	ns	CB is specified to be
		Rise Time	400 kHz mode	20 + 0.1 CB	300	ns	from 10 to 400 pF
			1 MHz mode ⁽²⁾	_	300	ns	
IM25	TSU:DAT	Data Input	100 kHz mode	250	_	ns	_
		Setup Time	400 kHz mode	100	_	ns	
			1 MHz mode ⁽²⁾	40	_	ns	
IM26	THD:DAT	Data Input	100 kHz mode	0	_	μS	_
		Hold Time	400 kHz mode	0	0.9	μS	
			1 MHz mode ⁽²⁾	0.2	_	μS	
IM30	Tsu:sta	Start Condition	100 kHz mode	Tcy/2 (BRG + 2)	_	μS	Only relevant for
		Setup Time	400 kHz mode	Tcy/2 (BRG + 2)	_	μS	Repeated Start
			1 MHz mode ⁽²⁾	Tcy/2 (BRG + 2)	_	μS	condition
IM31	THD:STA	Start Condition	100 kHz mode	Tcy/2 (BRG + 2)	_	μS	After this period the
		Hold Time	400 kHz mode	Tcy/2 (BRG +2)	_	μS	first clock pulse is
			1 MHz mode ⁽²⁾	Tcy/2 (BRG + 2)	_	μS	generated
IM33	Tsu:sto	Stop Condition	100 kHz mode	Tcy/2 (BRG + 2)		μS	_
		Setup Time	400 kHz mode	Tcy/2 (BRG + 2)	_	μS	
			1 MHz mode ⁽²⁾	Tcy/2 (BRG + 2)	_	μS	
IM34	THD:STO	Stop Condition	100 kHz mode	Tcy/2 (BRG + 2)		μS	_
		Hold Time	400 kHz mode	Tcy/2 (BRG + 2)	_	μS	
			1 MHz mode ⁽²⁾	Tcy/2 (BRG + 2)	_	μS	
IM40	TAA:SCL	Output Valid	100 kHz mode	_	3500	ns	_
		From Clock	400 kHz mode	_	1000	ns	_
			1 MHz mode ⁽²⁾	_	400	ns	_
IM45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	_	μS	Time the bus must be
			400 kHz mode	1.3		μS	free before a new
			1 MHz mode ⁽²⁾	0.5	_	μS	transmission can start
IM50	Св	Bus Capacitive L	oading	_	400	pF	_
IM51	TPGD	Pulse Gobbler De	elay	65	390	ns	See Note 3
Note 1	DDC io	the value of the 12	C David Data Car	oveten Defente Con	4! a.a. 40 %	lutan luta	grated Circuit (I ² C™)"

Note 1: BRG is the value of the I²C Baud Rate Generator. Refer to **Section 19. "Inter-Integrated Circuit (I²C™)"** (DS70330) in the "dsPIC33E/PIC24E Family Reference Manual". Please see the Microchip web site for the latest family reference manual sections.

^{2:} Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

^{3:} Typical value for this parameter is 130 ns.

^{4:} These parameters are characterized, but not tested in manufacturing.

FIGURE 30-32: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (SLAVE MODE)

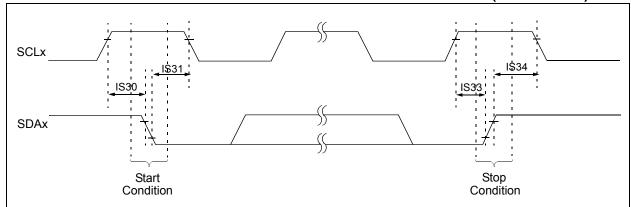


FIGURE 30-33: I2Cx BUS DATA TIMING CHARACTERISTICS (SLAVE MODE)

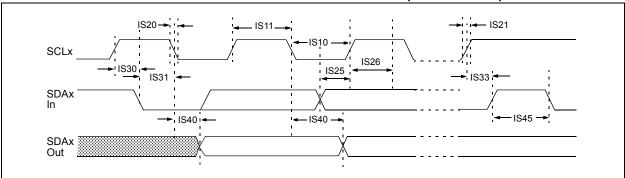


TABLE 30-52: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE)

IS10	Symbol TLO:SCL THI:SCL	Charac Clock Low Time	teristic	Extended Min.	Mov		
		Clock Low Time	100 kHz mode	1	Max.	Units	Conditions
1911	THI:SCL			4.7	1	μS	_
1011	THI:SCL		400 kHz mode	1.3		μS	_
1011	THI:SCL		1 MHz mode ⁽¹⁾	0.5		μS	_
		Clock High Time	100 kHz mode	4.0		μS	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	0.6		μS	Device must operate at a minimum of 10 MHz
			1 MHz mode ⁽¹⁾	0.5		μS	_
IS20 1	TF:SCL	SDAx and SCLx	100 kHz mode	_	300	ns	CB is specified to be from
		Fall Time	400 kHz mode	20 + 0.1 CB	300	ns	10 to 400 pF
			1 MHz mode ⁽¹⁾	_	100	ns	
IS21 T	Tr:scl	SDAx and SCLx	100 kHz mode	_	1000	ns	CB is specified to be from
		Rise Time	400 kHz mode	20 + 0.1 CB	300	ns	10 to 400 pF
			1 MHz mode ⁽¹⁾	_	300	ns	
IS25 7	Tsu:dat	Data Input	100 kHz mode	250	_	ns	_
		Setup Time	400 kHz mode	100	_	ns	
			1 MHz mode ⁽¹⁾	100		ns	
IS26 7	THD:DAT	Data Input	100 kHz mode	0	_	μS	_
		Hold Time	400 kHz mode	0	0.9	μS	
			1 MHz mode ⁽¹⁾	0	0.3	μS	
IS30 1	Tsu:sta	Start Condition	100 kHz mode	4.7	_	μS	Only relevant for Repeated
		Setup Time	400 kHz mode	0.6	_	μS	Start condition
			1 MHz mode ⁽¹⁾	0.25	_	μS	
IS31 7	THD:STA	Start Condition	100 kHz mode	4.0	_	μS	After this period, the first
		Hold Time	400 kHz mode	0.6	_	μS	clock pulse is generated
			1 MHz mode ⁽¹⁾	0.25	_	μS	
IS33	Tsu:sto	Stop Condition	100 kHz mode	4.7	_	μS	_
		Setup Time	400 kHz mode	0.6	_	μS	
			1 MHz mode ⁽¹⁾	0.6	_	μS	
IS34 7	THD:STO	Stop Condition	100 kHz mode	4	_	μS	_
		Hold Time	400 kHz mode	0.6		μS	
			1 MHz mode ⁽¹⁾	0.25		μS	
IS40 7	TAA:SCL	Output Valid	100 kHz mode	0	3500	ns	_
		From Clock	400 kHz mode	0	1000	ns	
			1 MHz mode ⁽¹⁾	0	350	ns	
IS45 7	TBF:SDA	Bus Free Time	100 kHz mode	4.7	_	μS	Time the bus must be free
			400 kHz mode	1.3	_	μ S	before a new transmission
			1 MHz mode ⁽¹⁾	0.5	_	 μS	can start
IS50 (Св	Bus Capacitive Lo		_	400	pF	_
	TPGD	Pulse Gobbler De		65	390	ns	See Note 2

Note 1: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

^{2:} The Typical value for this parameter is 130 ns.

^{3:} These parameters are characterized, but not tested in manufacturing.

FIGURE 30-34: ECAN MODULE I/O TIMING CHARACTERISTICS

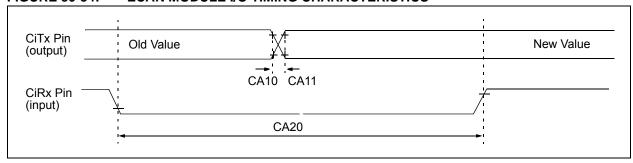


TABLE 30-53: ECAN MODULE I/O TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +125^{\circ}\text{C}$ for Extended				
Param No.	Symbol	Characteristic ⁽¹⁾	Min. Typ. ⁽²⁾ Max. Units Conditions					
CA10	TioF	Port Output Fall Time	_	_		ns	See parameter DO32	
CA11	TioR	Port Output Rise Time	— — ns See parameter DO					
CA20 Tcwf Pulse Width to Trigger CAN Wake-up Filter			120	_	_	ns	_	

- Note 1: These parameters are characterized but not tested in manufacturing.
 - 2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 30-35: UART MODULE I/O TIMING CHARACTERISTICS

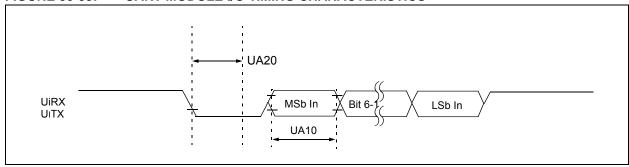


TABLE 30-54: UART MODULE I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40 $^{\circ}$ C \leq TA \leq +125 $^{\circ}$ C					
Param No. Symbol Characteristic ⁽¹⁾			Min. Typ. ⁽²⁾ Max. Units Condition					
UA10	Tuabaud	UART Baud Time	66.67	_	_	ns	_	
UA11	Fbaud	UART Baud Frequency	_	_	15	Mbps	_	
UA20	UA20 Tcwf Start Bit Pulse Width to Trigger UART Wake-up				_	ns	_	

- **Note 1:** These parameters are characterized but not tested in manufacturing.
 - **2:** Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

TABLE 30-55: CTMU CURRENT SOURCE SPECIFICATIONS

DC CHARACTERISTICS				Standard Operating Conditions:3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +125^{\circ}\text{C}$ for Extended						
Param No.	Symbol	Characteristic	Min.	Тур.	Max.	Units	Conditions			
CTMU CUR	RENT SOUR	CE								
CTMUI1	IOUT1	Base Range ⁽¹⁾	_	0.65	_	μA	CTMUICON<9:8> = 01			
CTMUI2	IOUT2	10x Range ⁽¹⁾	_	6.5	_	μΑ	CTMUICON<9:8> = 10			
CTMUI3	Іоит3	100x Range ⁽¹⁾	_	65	_	μA	CTMUICON<9:8> = 11			
CTMUI4	Iout4	1000x Range ⁽¹⁾	_	580	_	μA	CTMUICON<9:8> = 00			
CTMUFV1	VF	Temperature Diode Forward Voltage ^(1,2)	_	0.598	_	V	TA = +25°C, CTMUICON<9:8> = 01			
			_	0.658	_	V	TA = +25°C, CTMUICON<9:8> = 10			
			_	0.721	_	TA = +25°C, CTMUICON<9:8> = 11				
CTMUFV2	VFVR	Temperature Diode Rate of Change ^(1,2)	_	-1.92	_	mV/°C	CTMUICON<9:8> = 01			
		Change ^(1,2)	_	-1.74	_	mV/°C	CTMUICON<9:8> = 10			
			_	-1.56	_	mV/°C	CTMUICON<9:8> = 11			

Note 1: Nominal value at center point of current trim range (CTMUICON<15:10> = 000000).

- **2:** Parameters are characterized but not tested in manufacturing. Measurements taken with the following conditions:
 - VREF+ = AVDD = 3.3V
 - · ADC configured for 10-bit mode
 - ADC module configured for conversion speed of 500 ksps
 - All PMD bits are cleared (PMDx = 0)
 - Executing a while(1) statement
 - Device operating from the FRC with no PLL

TABLE 30-56: ADC MODULE SPECIFICATIONS

AC CHA	Standard Operating Conditions (see Note 1): 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq \text{TA} \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq \text{TA} \leq +125^{\circ}\text{C}$ for Extended						+85°C for Industrial				
Param No.	Symbol	Characteristic	Min.	Тур.	Max.	Units	Conditions				
Device Supply											
AD01	AVDD	Module VDD Supply	Greater of VDD – 0.3 or 3.0	_	Lesser of VDD + 0.3 or 3.6	V	_				
AD02	AVss	Module Vss Supply	Vss - 0.3	_	Vss + 0.3	V	_				
		,	Reference	ce Inpu	ts		,				
AD05	VREFH	Reference Voltage High	AVss + 2.5		AVDD	V	See Note 1 VREFH = VREF+ VREFL = VREF-				
AD05a			3.0	_	3.6	V	VREFH = AVDD VREFL = AVSS = 0				
AD06	VREFL	Reference Voltage Low	AVss	_	AVDD - 2.5	V	See Note 1				
AD06a			0	_	0	V	VREFH = AVDD VREFL = AVSS = 0				
AD07	VREF	Absolute Reference Voltage	2.5	_	3.6	V	VREF = VREFH - VREFL				
AD08	IREF	Current Drain	_	_	10 600	μ Α μ Α	ADC off ADC on				
AD09	IAD	Operating Current		5 2	_ _	mA mA	ADC operating in 10-bit mode, see Note 1 ADC operating in 12-bit mode, see Note 1				
	•		Analog	g Input		I					
AD12	VINH	Input Voltage Range VINH	VINL	_	VREFH	V	This voltage reflects Sample and Hold Channels 0, 1, 2, and 3 (CH0-CH3), positive input				
AD13	VINL	Input Voltage Range VINL	VREFL	_	AVss + 1V	V	This voltage reflects Sample and Hold Channels 0, 1, 2, and 3 (CH0-CH3), negative input				
AD17	Rin	Recommended Impedance of Analog Voltage Source	_	_	200	Ω	Impedance to achieve maximum performance of ADC				

Note 1: Device is functional at VBOR < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized.

TABLE 30-57: ADC MODULE SPECIFICATIONS (12-BIT MODE)

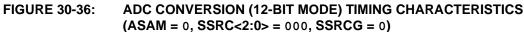
AC CHARACTERISTICS				Standard Operating Conditions (see Note 1): 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +125^{\circ}\text{C}$ for Extended							
Param No.	Symbol	Characteristic	Min.	Тур.	Max.	Conditions					
ADC Accuracy (12-bit Mode) – Measurements with external VREF+/VREF-											
AD20a	Nr	Resolution	1:	2 data bi	s	bits	_				
AD21a	INL	Integral Nonlinearity	-2	_	+2	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V				
AD22a	DNL	Differential Nonlinearity	>-1	_	<1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V				
AD23a	GERR	Gain Error	1.25	1.5	3	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V				
AD24a	EOFF	Offset Error	1.25	1.52	2	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V				
AD25a	_	Monotonicity	_	_		_	Guaranteed				
		ADC Accuracy (12-bit Mo	de) – Me	asureme	nts with	interna	I VREF+/VREF-				
AD20a	Nr	Resolution	1:	2 data bit	ts	bits	_				
AD21a	INL	Integral Nonlinearity	-2		+2	LSb	VINL = AVSS = 0V, AVDD = 3.6V				
AD22a	DNL	Differential Nonlinearity	>-1	_	<1	LSb	VINL = AVSS = 0V, AVDD = 3.6V				
AD23a	GERR	Gain Error	2	3	7	LSb	VINL = AVSS = 0V, AVDD = 3.6V				
AD24a	Eoff	Offset Error	2	3	5	LSb	VINL = AVSS = 0V, AVDD = 3.6V				
AD25a	_	Monotonicity	_		_	_	Guaranteed				
		Dynami	c Perforn	nance (1	2-bit Mo	de)					
AD30a	THD	Total Harmonic Distortion	_		-75	dB					
AD31a	SINAD	Signal to Noise and Distortion	68.5	69.5	1	dB	_				
AD32a	SFDR	Spurious Free Dynamic Range	80	_	_	dB	_				
AD33a	FNYQ	Input Signal Bandwidth	_		250	kHz	_				
AD34a	ENOB	Effective Number of Bits	11.09	11.3	_	bits	_				

Note 1: Device is functional at VBOR < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized.

TABLE 30-58: ADC MODULE SPECIFICATIONS (10-BIT MODE)

AC CHARACTERISTICS				Standard Operating Conditions (see Note 1): 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{Ta} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{Ta} \le +125^{\circ}\text{C}$ for Extended					
Param No.	Symbol	Characteristic	Min.	Тур.	Max.	Units	Conditions		
		ADC Accuracy (10-bit Mode) – Meas	urement	ts with e	xternal	VREF+/VREF-		
AD20b	Nr	Resolution	10) data bi	ts	bits	_		
AD21b	INL	Integral Nonlinearity	-1.5	_	+1.5	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V		
AD22b	DNL	Differential Nonlinearity	>-1		<1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V		
AD23b	GERR	Gain Error	1	3	6	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V		
AD24b	EOFF	Offset Error	1	2	3	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V		
AD25b	_	Monotonicity	_	_	_	_	Guaranteed		
		ADC Accuracy (10-bit Mode	e) – Meas	uremen	ts with in	nternal \	VREF+/VREF-		
AD20b	Nr	Resolution	10) data bi	ts	bits	_		
AD21b	INL	Integral Nonlinearity	-1.5		+1.5	LSb	VINL = AVSS = 0V, AVDD = 3.6V		
AD22b	DNL	Differential Nonlinearity	>-1	_	<1	LSb	VINL = AVSS = 0V, AVDD = 3.6V		
AD23b	GERR	Gain Error	1	5	6	LSb	VINL = AVSS = 0V, AVDD = 3.6V		
AD24b	Eoff	Offset Error	1	2	5	LSb	VINL = AVSS = 0V, AVDD = 3.6V		
AD25b		Monotonicity		_		_	Guaranteed		
		Dynamic	Performa	nce (10-	bit Mod	e)			
AD30b	THD	Total Harmonic Distortion	_	_	-64	dB	_		
AD31b	SINAD	Signal to Noise and Distortion	57	58.5	1	dB	_		
AD32b	SFDR	Spurious Free Dynamic Range	72	_	_	dB	_		
AD33b	FNYQ	Input Signal Bandwidth	_	_	550	kHz	_		
AD34b	ENOB	Effective Number of Bits	9.16	9.4	_	bits	_		

Note 1: Device is functional at VBOR < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized.



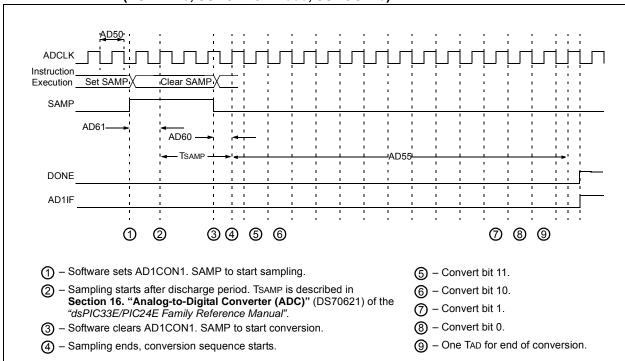
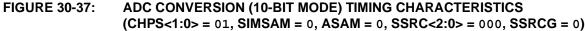


TABLE 30-59: ADC CONVERSION (12-BIT MODE) TIMING REQUIREMENTS

AC CHA	ARACTE	Standard Operating Conditions (see Note 2): 3.0V to 3.6V (unless otherwise stated) $ \begin{array}{ll} \text{Operating temperature} & -40^{\circ}\text{C} \leq \text{TA} \leq +85^{\circ}\text{C for Industrial} \\ -40^{\circ}\text{C} \leq \text{TA} \leq +125^{\circ}\text{C for Extended} \end{array} $					
Param No.	Symbol	Characteristic	Min.	Тур.	Max.	Units	Conditions
		Clock	k Paramet	ters			
AD50	TAD	ADC Clock Period	117.6	_	_	ns	_
AD51	trc	ADC Internal RC Oscillator Period	_	250	_	ns	_
		Conv	version R	ate			
AD55	tconv	Conversion Time	_	14 TAD		ns	_
AD56	FCNV	Throughput Rate	_	_	500	Ksps	_
AD57a	TSAMP	Sample Time when Sampling any ANx Input	3 TAD	_	_	_	_
AD57b	Тѕамр	Sample Time when Sampling the Op amp Outputs (Configuration A ⁽⁴⁾ and Configuration B ⁽⁵⁾)	3 TAD	_	_	_	_
		Timin	g Parame	ters			
AD60	tPCS	Conversion Start from Sample Trigger ⁽⁶⁾	2 TAD	_	3 TAD	_	Auto convert trigger not selected
AD61	tPSS	Sample Start from Setting Sample (SAMP) bit ⁽⁶⁾	2 TAD	_	3 TAD	_	_
AD62	tcss	Conversion Completion to Sample Start (ASAM = 1) ⁽⁶⁾	_	0.5 TAD	_	_	_
AD63	tDPU	Time to Stabilize Analog Stage from ADC Off to ADC On ⁽⁶⁾	1	_	20	μS	See Note 3

- Note 1: Because the sample caps will eventually lose charge, clock rates below 10 kHz may affect linearity performance, especially at elevated temperatures.
 - 2: Device is functional at VBOR < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized.
 - 3: The parameter tDPU is the time required for the ADC module to stabilize at the appropriate level when the module is turned on (ADON (AD1CON1<15>) = '1'). During this time, the ADC result is indeterminate.
 - **4:** See Figure 25-5 for configuration information.
 - **5:** See Figure 25-6 for configuration information.
 - **6:** These parameters are characterized, but not tested in manufacturing.



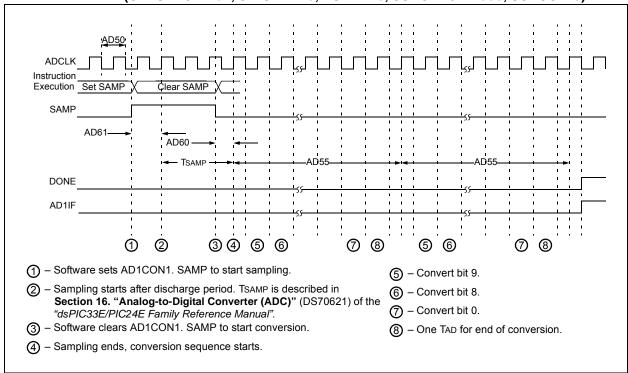


FIGURE 30-38: ADC CONVERSION (10-BIT MODE) TIMING CHARACTERISTICS (CHPS<1:0> = 01, SIMSAM = 0, ASAM = 1, SSRC<2:0> = 111, SSRCG = 0, SAMC<4:0> = 00010)

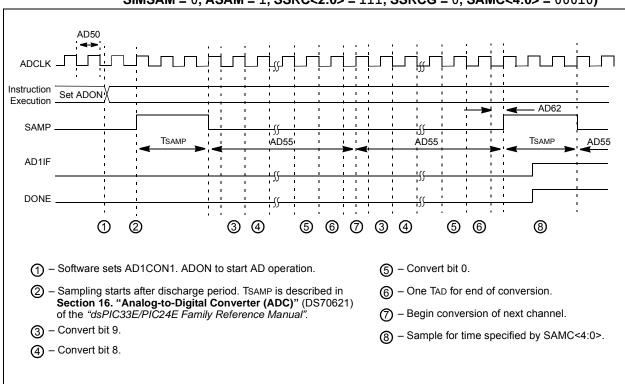


TABLE 30-60: ADC CONVERSION (10-BIT MODE) TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions (see Note 1): 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +125^{\circ}\text{C}$ for Extended					
Param No.	Symbol	Characteristic	Min.	Typ. ⁽¹⁾	Max.	Units	Conditions		
		Cloc	k Parame	ters					
AD50	TAD	ADC Clock Period	76	_	_	ns	_		
AD51	trc	ADC Internal RC Oscillator Period	_	250	_	ns	_		
		Con	version F	Rate					
AD55	tconv	Conversion Time	_	12 TAD		_	_		
AD56	FCNV	Throughput Rate	_		1.1	Msps	Using Simultaneous Sampling		
AD57a	Тѕамр	Sample Time when Sampling any ANx Input	2 TAD	_	_	_	_		
AD57b	Тѕамр	Sample Time when Sampling the Op amp Outputs (Configuration A ⁽⁴⁾ and Configuration B ⁽⁵⁾)	4 TAD	_	_	_	_		
		Timin	g Param	eters					
AD60	tPCS	Conversion Start from Sample Trigger ⁽⁶⁾	2 TAD	_	3 TAD	_	Auto-Convert Trigger not selected		
AD61	tpss	Sample Start from Setting Sample (SAMP) bit ⁽⁶⁾	2 TAD	_	3 TAD	_	_		
AD62	tcss	Conversion Completion to Sample Start (ASAM = 1) ⁽⁶⁾	_	0.5 TAD	_	_	_		
AD63	tDPU	Time to Stabilize Analog Stage from ADC Off to ADC On ⁽⁶⁾	_	_	20	μS	See Note 3		

- **Note 1:** Device is functional at VBOR < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized.
 - **2:** Because the sample caps will eventually lose charge, clock rates below 10 kHz may affect linearity performance, especially at elevated temperatures.
 - 3: The parameter tDPU is the time required for the ADC module to stabilize at the appropriate level when the module is turned on (AD1CON1<ADON> = 1). During this time, the ADC result is indeterminate.
 - 4: See Figure 25-5 for configuration information.
 - **5:** See Figure 25-6 for configuration information.
 - **6:** These parameters are characterized, but not tested in manufacturing.

TABLE 30-61: DMA MODULE TIMING REQUIREMENTS

AC CHA	AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industriance $-40^{\circ}\text{C} \le \text{TA} \le +125^{\circ}\text{C}$ for Extenditions (in the condition of the co					
Param No.	Characteristic	Min.	Тур.	Max.	Units	Conditions		
DM1	DMA Byte/Word Transfer Latency	1 Tcy ⁽²⁾	_	_	ns	_		

- **Note 1:** These parameters are characterized, but not tested in manufacturing.
 - 2: Because DMA transfers use the CPU data bus, this time is dependent on other functions on the bus.

31.0 DC AND AC DEVICE CHARACTERISTICS GRAPHS

Note: The graphs provided following this note are a statistical summary based on a limited number of samples and are provided for design guidance purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

FIGURE 31-1: VOH – 4x DRIVER PINS

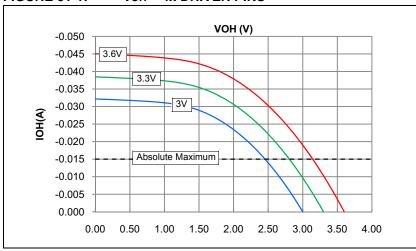


FIGURE 31-3: Vol – 4x DRIVER PINS

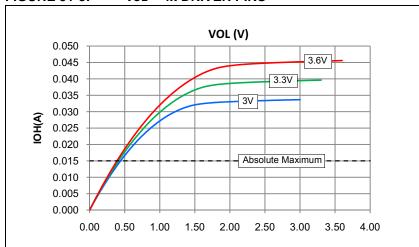


FIGURE 31-2: VOH – 8x DRIVER PINS

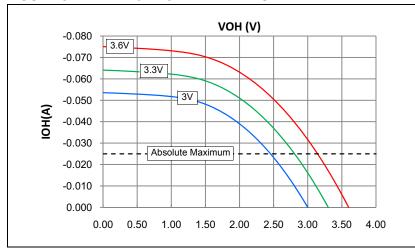
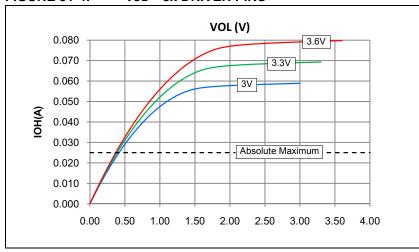
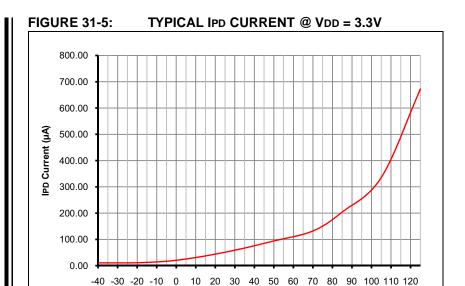
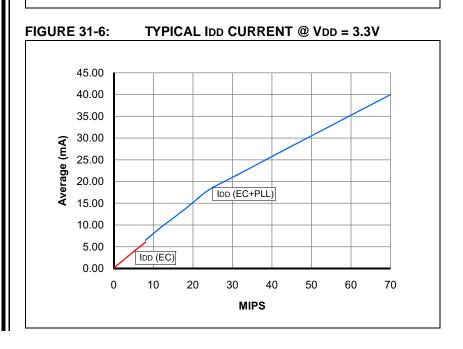


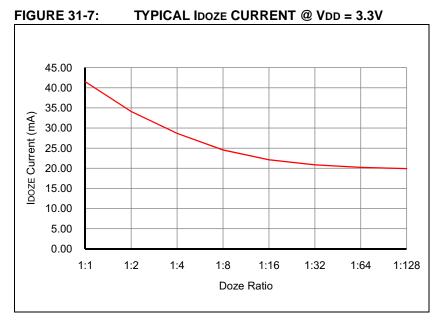
FIGURE 31-4: Vol – 8x DRIVER PINS

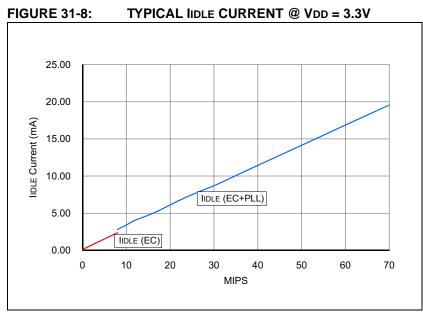




Temperature (Celsius)









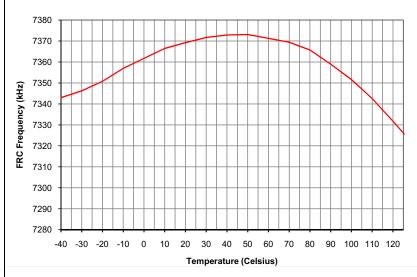


FIGURE 31-10: TYPICAL LPRC FREQUENCY @ VDD = 3.3V

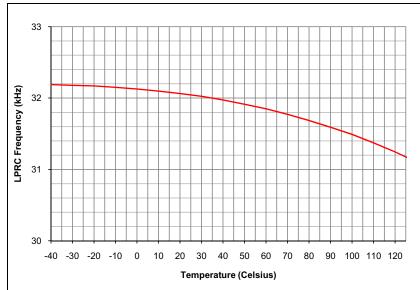
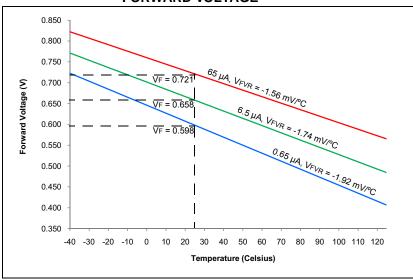


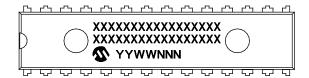
FIGURE 31-11: TYPICAL CTMU TEMPERATURE DIODE FORWARD VOLTAGE



32.0 PACKAGING INFORMATION

32.1 Package Marking Information

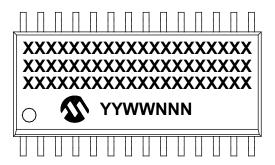
28-Lead SPDIP (.300")







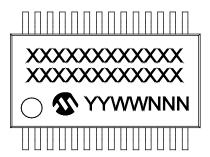
28-Lead SOIC (7.50 mm)



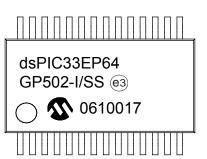
Example



28-Lead SSOP (5.30 mm)



Example



Legend: XX...X Customer-specific information

Y Year code (last digit of calendar year)
YY Year code (last 2 digits of calendar year)
WW Week code (week of January 1 is week '01')
NNN Alphanumeric traceability code

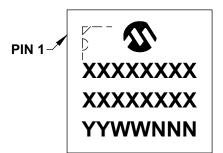
(Sn) Pb-free JEDEC designator for Matte Tin (Sn)

This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

32.1 Package Marking Information (Continued)

28-Lead QFN-S (6x6x0.9 mm)



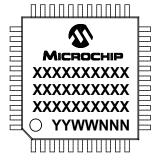
36-Lead VTLA (TLA)



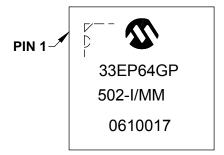
44-Lead VTLA (TLA)



44-Lead TQFP (10x10x1 mm)



Example



Example



Example



Example

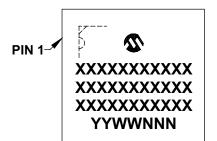


Legend:	XXX	Customer-specific information
	Υ	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	MNN	Alphanumeric traceability code
	NNN e3	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3)
		can be found on the outer packaging for this package.

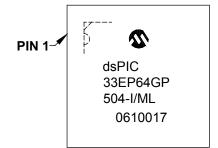
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

32.1 Package Marking Information (Continued)

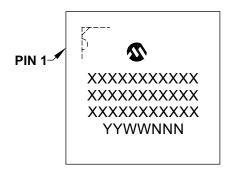
44-Lead QFN (8x8x0.9 mm)



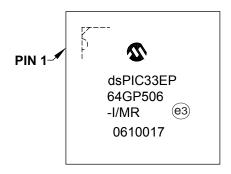
Example



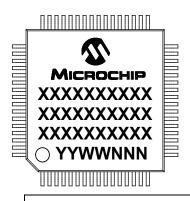
64-Lead QFN (9x9x0.9 mm)



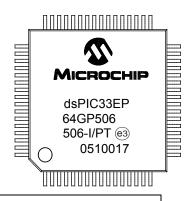
Example



64-Lead TQFP (10x10x1 mm)



Example



Legend: XX...X Customer-specific information

Y Year code (last digit of calendar year)
YY Year code (last 2 digits of calendar year)
WW Week code (week of January 1 is week '01')

NNN Alphanumeric traceability code

e3 Pb-free JEDEC designator for Matte Tin (Sn)

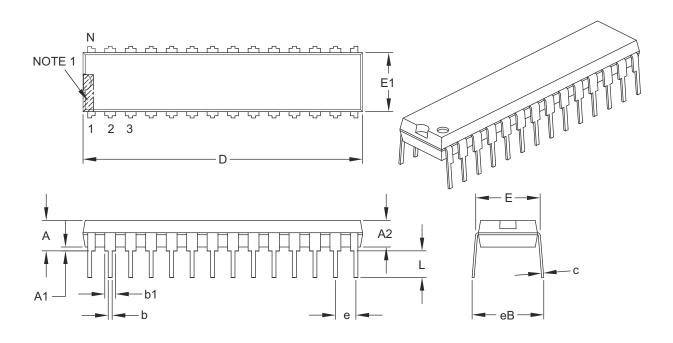
This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

32.2 Package Details

28-Lead Skinny Plastic Dual In-Line (SP) - 300 mil Body [SPDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units			INCHES			
Dimension	n Limits	MIN	NOM	MAX			
Number of Pins	N		28				
Pitch	е		.100 BSC				
Top to Seating Plane	Α	_	_	.200			
Molded Package Thickness	A2	.120	.135	.150			
Base to Seating Plane	A1	.015	_	_			
Shoulder to Shoulder Width	Е	.290	.310	.335			
Molded Package Width	E1	.240	.285	.295			
Overall Length	D	1.345	1.365	1.400			
Tip to Seating Plane	L	.110	.130	.150			
Lead Thickness	С	.008	.010	.015			
Upper Lead Width	b1	.040	.050	.070			
Lower Lead Width	b	.014	.018	.022			
Overall Row Spacing §	eB	_	_	.430			

Notes:

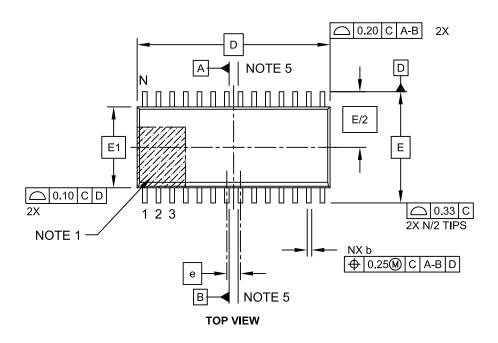
- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. § Significant Characteristic.
- 3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- 4. Dimensioning and tolerancing per ASME Y14.5M.

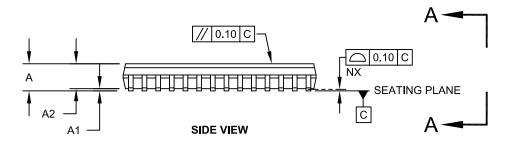
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

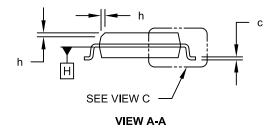
Microchip Technology Drawing C04-070B

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

te: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



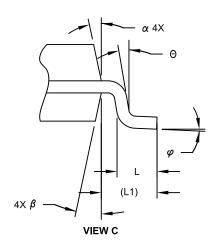


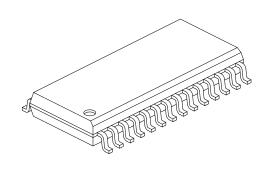


Microchip Technology Drawing C04-052C Sheet 1 of 2

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





	N	MILLIMETERS				
Dimension	Limits	MIN	NOM	MAX		
Number of Pins	N		28			
Pitch	е		1.27 BSC			
Overall Height	Α	ı	-	2.65		
Molded Package Thickness	A2	2.05	-	-		
Standoff §	A1	0.10	-	0.30		
Overall Width	Е		10.30 BSC			
Molded Package Width	E1	7.50 BSC				
Overall Length	D		17.90 BSC			
Chamfer (Optional)	h	0.25	-	0.75		
Foot Length	L	0.40	-	1.27		
Footprint	L1		1.40 REF			
Lead Angle	Θ	0°	-	-		
Foot Angle	φ	0°	-	8°		
Lead Thickness	С	0.18	-	0.33		
Lead Width	b	0.31	-	0.51		
Mold Draft Angle Top	α	5°	-	15°		
Mold Draft Angle Bottom	β	5°	-	15°		

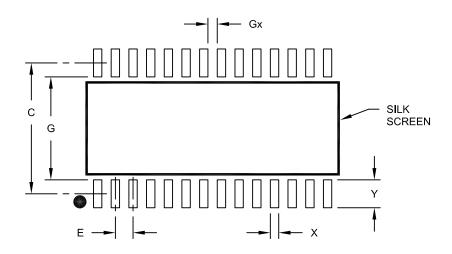
Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. § Significant Characteristic
- Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
- 4. Dimensioning and tolerancing per ASME Y14.5M
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- REF: Reference Dimension, usually without tolerance, for information purposes only.
- 5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing C04-052C Sheet 2 of 2

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	N	II LLIMETER	S	
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	E 1.27 BSC		
Contact Pad Spacing	С		9.40	
Contact Pad Width (X28)	Х			0.60
Contact Pad Length (X28)	Υ			2.00
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.40		

Notes:

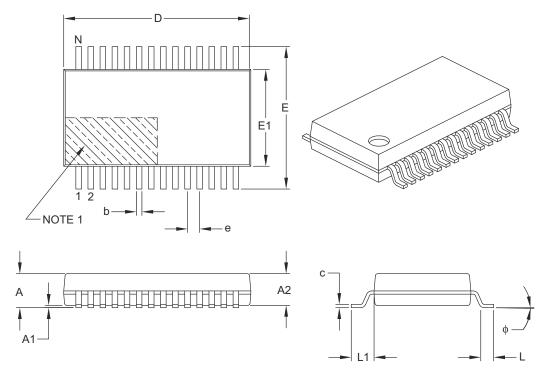
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2052A

28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	
Number of Pins	N		28		
Pitch	е		0.65 BSC		
Overall Height	Α	-	_	2.00	
Molded Package Thickness	A2	1.65	1.75	1.85	
Standoff	A1	0.05	_	-	
Overall Width	E	7.40	7.80	8.20	
Molded Package Width	E1	5.00	5.30	5.60	
Overall Length	D	9.90	10.20	10.50	
Foot Length	L	0.55	0.75	0.95	
Footprint	L1		1.25 REF		
Lead Thickness	С	0.09	_	0.25	
Foot Angle	ф	0°	4°	8°	
Lead Width	b	0.22	_	0.38	

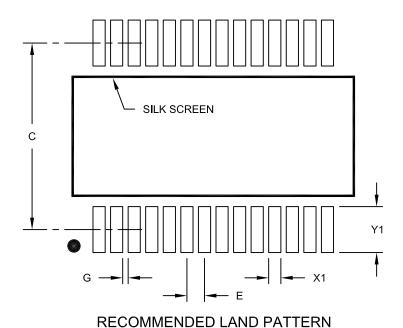
Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
- 3. Dimensioning and tolerancing per ASME Y14.5M.
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-073B

28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



MILLIMETERS Units **Dimension Limits** MIN MON MAX Contact Pitch Ε 0.65 BSC Contact Pad Spacing С 7.20 Contact Pad Width (X28) X1 0.45 Contact Pad Length (X28) Υ1 1.75 0.20 Distance Between Pads G

Notes:

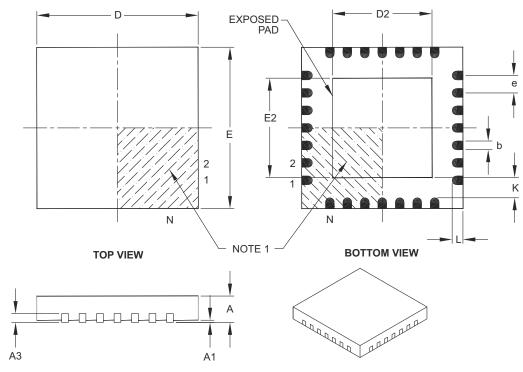
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2073A

28-Lead Plastic Quad Flat, No Lead Package (MM) – 6x6x0.9 mm Body [QFN-S] with 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		MILLIMETERS		
Dimen	sion Limits	MIN	NOM	MAX	
Number of Pins	N		28		
Pitch	е		0.65 BSC		
Overall Height	Α	0.80	0.90	1.00	
Standoff	A1	0.00	0.02	0.05	
Contact Thickness	A3		0.20 REF		
Overall Width	Е		6.00 BSC		
Exposed Pad Width	E2	3.65	3.70	4.70	
Overall Length	D		6.00 BSC		
Exposed Pad Length	D2	3.65	3.70	4.70	
Contact Width	b	0.23	0.38	0.43	
Contact Length	L	0.30	0.40	0.50	
Contact-to-Exposed Pad	K	0.20	_	-	

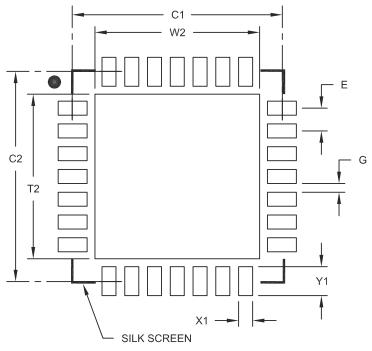
Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. Package is saw singulated.
- 3. Dimensioning and tolerancing per ASME Y14.5M.
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-124B

28-Lead Plastic Quad Flat, No Lead Package (MM) -6x6x0.9 mm Body [QFN-S] with 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	Е		0.65 BSC	
Optional Center Pad Width	W2			4.70
Optional Center Pad Length	T2			4.70
Contact Pad Spacing	C1		6.00	
Contact Pad Spacing	C2		6.00	
Contact Pad Width (X28)	X1			0.40
Contact Pad Length (X28)	Y1			0.85
Distance Between Pads	G	0.25		

Notes:

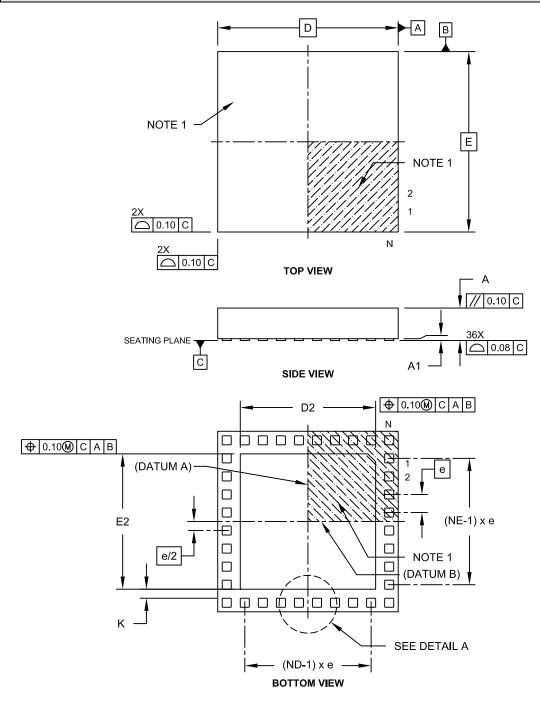
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2124A

36-Lead Thermal Leadless Array Package (TL) – 5x5x0.9 mm Body with Exposed Pad [TLA]

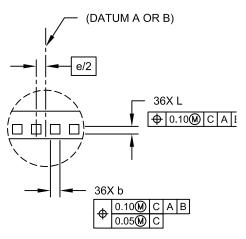
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

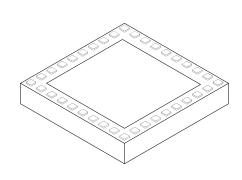


Microchip Technology Drawing C04-187B Sheet 1 of 2

36-Lead Thermal Leadless Array Package (TL) – 5x5x0.9 mm Body with Exposed Pad [TLA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





DETAIL A

	Units	Units MILLIMETERS		
Dimensior	Limits	s MIN NOM MAX		
Number of Pins	N		36	
Number of Pins per Side	ND		10	
Number of Pins per Side	NE		8	
Pitch	е	0.50 BSC		
Overall Height	Α	0.80	0.90	1.00
Standoff	A1	0.025	ı	0.075
Overall Width	E		5.00 BSC	
Exposed Pad Width	E2	3.60	3.75	3.90
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.60	3.75	3.90
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.20	0.25	0.30
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. Package is saw singulated.
- 3. Dimensioning and tolerancing per ASME Y14.5M.

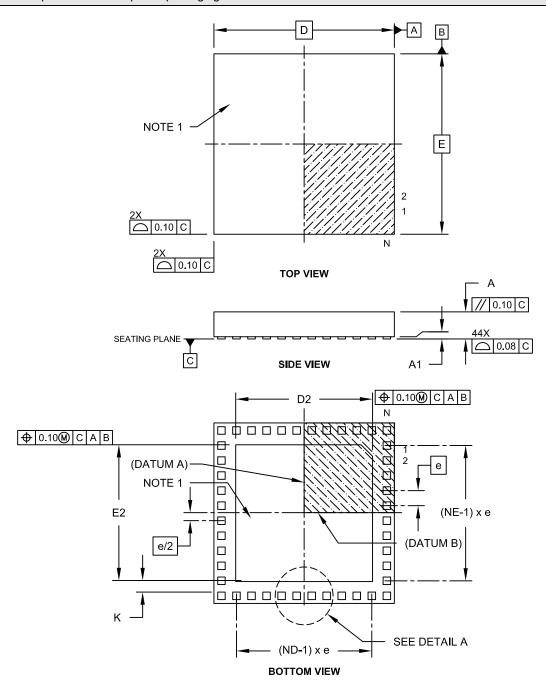
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-187B Sheet 2 of 2

44-Lead Thermal Leadless Array Package (TL) – 6x6x0.9 mm Body with Exposed Pad [TLA]

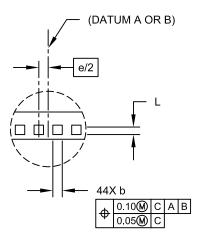
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

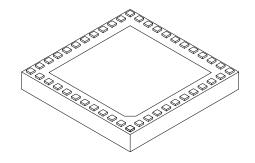


Microchip Technology Drawing C04-157B Sheet 1 of 2

44-Lead Thermal Leadless Array Package (TL) – 6x6x0.9 mm Body with Exposed Pad [TLA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





DETAIL A

	Units MILLIMETERS			S
Dimension	Limits	MIN NOM MAX		
Number of Pins	N		44	
Number of Pins per Side	DN		12	
Number of Pins per Side	NE		10	
Pitch	е	0.50 BSC		
Overall Height	Α	0.80	0.90	1.00
Standoff	A1	0.025	-	0.075
Overall Width	Е	6.00 BSC		
Exposed Pad Width	E2	4.40	4.55	4.70
Overall Length	D	6.00 BSC		
Exposed Pad Length	D2	4.40	4.55	4.70
Contact Width	b	0.20	0.25	0.30
Contact Length	Г	0.20	0.25	0.30
Contact-to-Exposed Pad	K	0.20	-	_

Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. Package is saw singulated.
- 3. Dimensioning and tolerancing per ASME Y14.5M.

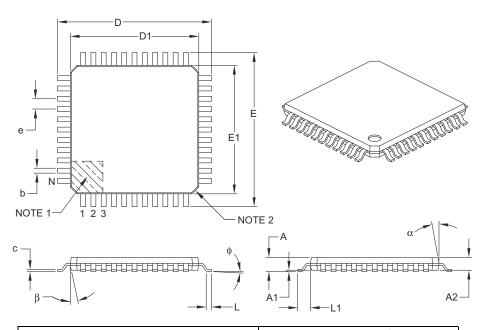
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-157B Sheet 2 of 2

44-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		MILLIMETERS		
Dimension	n Limits	MIN	NOM	MAX	
Number of Leads	Ν		44		
Lead Pitch	е		0.80 BSC		
Overall Height	Α	-	_	1.20	
Molded Package Thickness	A2	0.95	1.00	1.05	
Standoff	A1	0.05	_	0.15	
Foot Length	L	0.45	0.60	0.75	
Footprint	L1		1.00 REF		
Foot Angle	ф	0°	3.5°	7°	
Overall Width	Е		12.00 BSC		
Overall Length	D		12.00 BSC		
Molded Package Width	E1		10.00 BSC		
Molded Package Length	D1		10.00 BSC		
Lead Thickness	С	0.09	_	0.20	
Lead Width	b	0.30	0.37	0.45	
Mold Draft Angle Top	α	11°	12°	13°	
Mold Draft Angle Bottom	β	11°	12°	13°	

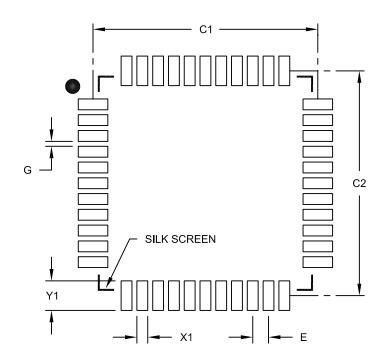
Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. Chamfers at corners are optional; size may vary.
- 3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
- 4. Dimensioning and tolerancing per ASME Y14.5M.
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-076B

44-Lead Plastic Thin Quad Flatpack (PT) 10X10X1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	N	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	
Contact Pitch	E	0.80 BSC			
Contact Pad Spacing	C1		11.40		
Contact Pad Spacing	C2		11.40		
Contact Pad Width (X44)	X1			0.55	
Contact Pad Length (X44)	Y1			1.50	
Distance Between Pads	G	0.25			

Notes:

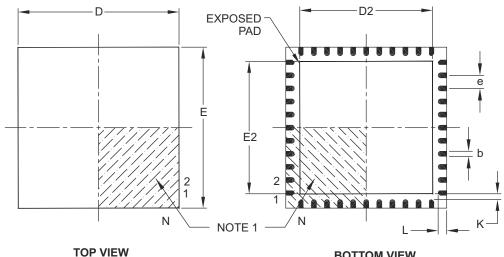
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2076B

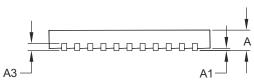
44-Lead Plastic Quad Flat, No Lead Package (ML) – 8x8 mm Body [QFN]

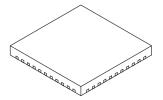
For the most current package drawings, please see the Microchip Packaging Specification located at Note: http://www.microchip.com/packaging











	Units		MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX	
Number of Pins	N		44		
Pitch	е		0.65 BSC		
Overall Height	A	0.80	0.90	1.00	
Standoff	A1	0.00	0.02	0.05	
Contact Thickness	A3		0.20 REF		
Overall Width	E		8.00 BSC		
Exposed Pad Width	E2	6.30	6.45	6.80	
Overall Length	D		8.00 BSC		
Exposed Pad Length	D2	6.30	6.45	6.80	
Contact Width	b	0.25	0.30	0.38	
Contact Length	L	0.30	0.40	0.50	
Contact-to-Exposed Pad	K	0.20	_	_	

Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. Package is saw singulated.
- 3. Dimensioning and tolerancing per ASME Y14.5M.

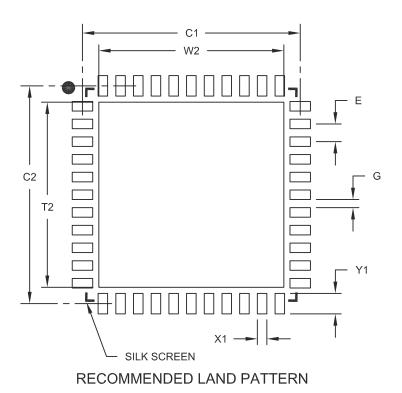
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-103B

44-Lead Plastic Quad Flat, No Lead Package (ML) – 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units MILLIMETERS Dimension Limits MIN NOM MAX Contact Pitch 0.65 BSC Е Optional Center Pad Width 6.80 W2 Optional Center Pad Length T2 6.80 Contact Pad Spacing C1 8.00 Contact Pad Spacing C2 8.00 Contact Pad Width (X44) X1 0.35 Contact Pad Length (X44) Υ1 0.80 Distance Between Pads G 0.25

Notes:

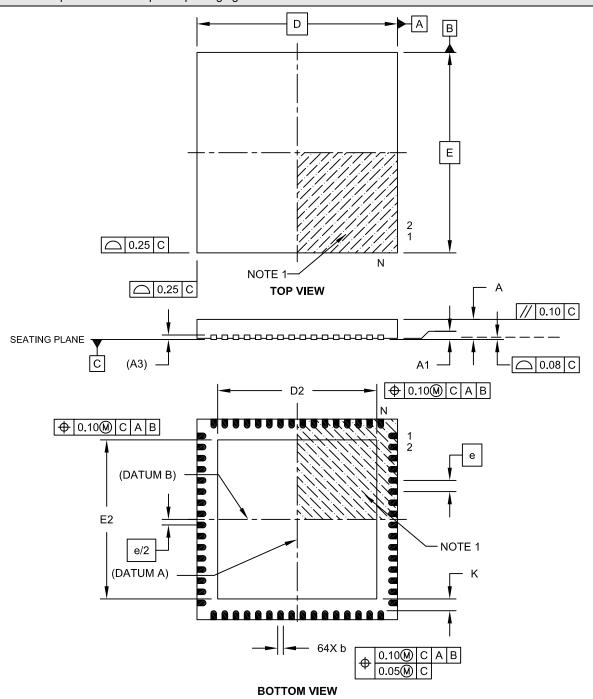
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2103A

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN] With 7.15 x 7.15 Exposed Pad [QFN]

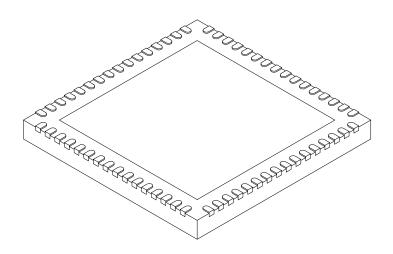
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-149C Sheet 1 of 2

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN] With 7.15 x 7.15 Exposed Pad [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX
Number of Pins	Z		64	
Pitch	е		0.50 BSC	
Overall Height	Α	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Width	Е		9.00 BSC	
Exposed Pad Width	E2	7.05	7.15	7.50
Overall Length	D		9.00 BSC	
Exposed Pad Length	D2	7.05	7.15	7.50
Contact Width	b	0.18 0.25 0.30		
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. Package is saw singulated.
- 3. Dimensioning and tolerancing per ASME Y14.5M.

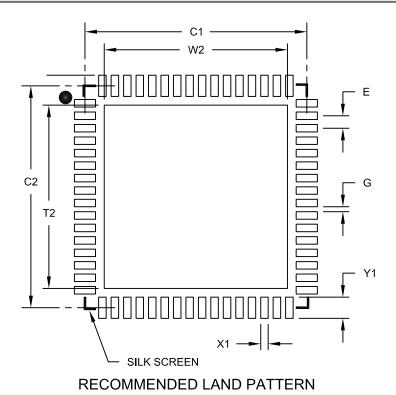
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-149C Sheet 2 of 2

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN] With 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units **MILLIMETERS Dimension Limits** MIN MOM MAX Contact Pitch 0.50 BSC Ε Optional Center Pad Width W2 7.35 7.35 Optional Center Pad Length T2 Contact Pad Spacing C1 8.90 Contact Pad Spacing C2 8.90 0.30 Contact Pad Width (X64) X1 Contact Pad Length (X64) Y1 0.85 Distance Between Pads 0.20

Notes:

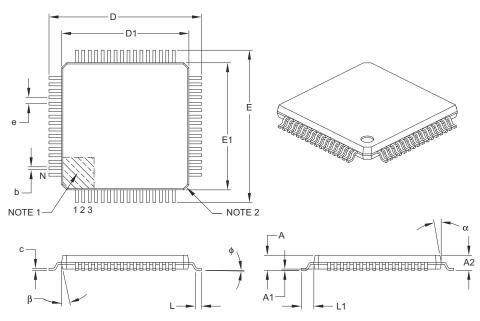
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2149A

64-Lead Plastic Thin Quad Flatpack (PT) - 10x10x1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension	Dimension Limits		NOM	MAX
Number of Leads	N		64	
Lead Pitch	е		0.50 BSC	
Overall Height	Α	_	_	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	-	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ф	0°	3.5°	7°
Overall Width	Е		12.00 BSC	
Overall Length	D		12.00 BSC	
Molded Package Width	E1		10.00 BSC	
Molded Package Length	D1		10.00 BSC	
Lead Thickness	С	0.09	_	0.20
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

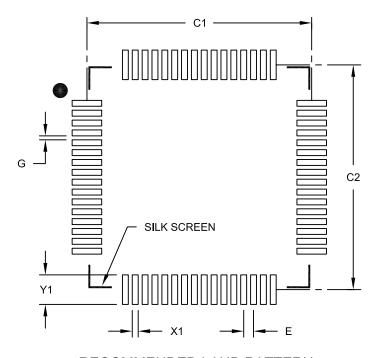
Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. Chamfers at corners are optional; size may vary.
- 3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
- 4. Dimensioning and tolerancing per ASME Y14.5M.
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-085B

64-Lead Plastic Thin Quad Flatpack (PT) 10x10x1 mm Body, 2.00 mm Footprint [TQFP]

For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	s MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	Е	0.50 BSC		
Contact Pad Spacing	C1	11.40		
Contact Pad Spacing	C2		11.40	
Contact Pad Width (X64)	X1			0.30
Contact Pad Length (X64)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2085B

APPENDIX A: REVISION HISTORY

Revision A (April 2011)

This is the initial released version of this document.

Revision B (July 2011)

This revision includes minor typographical and formatting changes throughout the data sheet text.

All other major changes are referenced by their respective section in Table A-1.

TABLE A-1: MAJOR SECTION UPDATES

Section Name	Update Description
"High-Performance, 16-bit Digital Signal Controllers and Microcontrollers"	Changed all pin diagrams references of VLAP to TLA.
Section 4.0 "Memory Organization"	Updated the All Resets values for CLKDIV and PLLFBD in the System Control Register Map (see Table 4-35).
Section 5.0 "Flash Program Memory"	Updated "one word" to "two words" in the first paragraph of Section 5.2 "RTSP Operation".
Section 9.0 "Oscillator Configuration"	Updated the PLL Block Diagram (see Figure 9-2). Updated the Oscillator Mode, Fast RC Oscillator (FRC) with divide-by-N and PLL (FRCPLL), by changing (FRCDIVN + PLL) to (FRCPLL).
	Changed (FRCDIVN + PLL) to (FRCPLL) for COSC<2:0> = 001 and NOSC<2:0> = 001 in the Oscillator Control Register (see Register 9-1).
	Changed the POR value from 0 to 1 for the DOZE<1:0> bits, from 1 to 0 for the FRCDIV<0> bit, and from 0 to 1 for the PLLPOST<0> bit; Updated the default definitions for the DOZE<2:0> and FRCDIV<2:0> bits and updated all bit definitions for the PLLPOST<1:0> bits in the Clock Divisor Register (see Register 9-2).
	Changed the POR value from 0 to 1 for the PLLDIV<5:4> bits and updated the default definitions for all PLLDIV<8:0> bits in the PLL Feedback Division Register (see Register 9-2).
Section 22.0 "Charge Time Measurement Unit (CTMU)"	Updated the bit definitions for the IRNG<1:0> bits in the CTMU Current Control Register (see Register 22-3).
Section 25.0 "Op amp/ Comparator Module"	Updated the voltage reference block diagrams (see Figure 25-1 and Figure 25-2).

TABLE A-1: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description	
Section 30.0 "Electrical Characteristics"	Removed Voltage on VCAP with respect to Vss and added Note 5 in Absolute Maximum Ratings ⁽¹⁾ .	
	Removed parameter DC18 (Vcore) and Note 3 from the DC Temperature and Voltage Specifications (see Table 30-4).	
	Updated Note 1 in the DC Characteristics: Operating Current (IDD) (see Table 30-6).	
	Updated Note 1 in the DC Characteristics: Idle Current (IDLE) (see Table 30-7).	
	Changed the Typical values for parameters DC60a-DC60d and updated Note 1 in the DC Characteristics: Power-down Current (IPD) (see Table 30-8).	
	Updated Note 1 in the DC Characteristics: Doze Current (IDOZE) (see Table 30-9).	
	Updated Note 2 in the Electrical Characteristics: BOR (see Table 30-12).	
	Updated parameters CM20 and CM31, and added parameters CM44 and CM45 in the AC/DC Characteristics: Op amp/Comparator (see Table 30-14).	
	Added the Op amp/Comparator Reference Voltage Settling Time Specifications (see Table 30-15).	
	Added Op amp/Comparator Voltage Reference DC Specifications (see Table 30-16).	
	Updated Internal FRC Accuracy parameter F20a (see Table 30-21).	
	Updated the Typical value and Units for parameter CTMUI1, and added parameters CTMUI4, CTMUFV1, and CTMUFV2 to the CTMU Current Source Specifications (see Table 30-55).	
Section 31.0 "Packaging Information"	Updated packages by replacing references of VLAP with TLA.	
"Product Identification System"	Changed VLAP to TLA.	

Revision C (November 2011)

This revision includes typographical and formatting changes throughout the data sheet text.

In addition, where applicable, new sections were added to each peripheral chapter that provide information and links to related resources, as well as helpful tips. For examples, see Section 20.1 "UART Helpful Tips" and Section 3.6 "CPU Resources".

All occurrences of TLA were updated to VTLA throughout the document, with the exception of the pin diagrams (updated diagrams were not available at time of publication).

A new chapter, Section 31.0 "DC and AC Device Characteristics Graphs", was added.

All other major changes are referenced by their respective section in Table A-2.

TABLE A-2: MAJOR SECTION UPDATES

Section Name	Update Description
"16-bit Microcontrollers and Digital Signal Controllers (up to 256 KB Flash and 32 KB SRAM) with High-Speed PWM, Op amps, and Advanced Analog"	The content on the first page of this section was extensively reworked to provide the reader with the key features and functionality of this device family in an "at-a-glance" format.
Section 1.0 "Device Overview"	Updated the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X Block Diagram (see Figure 1-1), which now contains a CPU block and a reference to the CPU diagram. Updated the description and Note references in the Pinout I/O Descriptions for these
	pins: C1IN2-, C2IN2-, C3IN2-, OA1OUT, OA2OUT, and OA3OUT (see Table 1-1).
Section 2.0 "Guidelines for Getting Started with 16-bit Digital Signal Controllers and Microcontrollers"	Updated the Recommended Minimum Connection diagram (see Figure 2-1).
Section 3.0 "CPU"	Updated the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X CPU Block Diagram (see Figure 3-1).
	Updated the Status register definition in the Programmer's Model (see Figure 3-2).
Section 4.0 "Memory	Updated the Data Memory Maps (see Figure 4-6 and Figure 4-11).
Organization"	Removed the DCB<1:0> bits from the OC1CON2, OC2CON2, OC3CON2, and OC4CON2 registers in the Output Compare 1 Through Output Compare 4 Register Map (see Table 4-10).
	Added the TRIG1 and TRGCON1 registers to the PWM1 Generator 1 Register Map (see Table 4-13).
	Added the TRIG2 and TRGCON2 registers to the PWM1 Generator 1 Register Map (see Table 4-14).
	Added the TRIG3 and TRGCON3 registers to the PWM1 Generator 1 Register Map (see Table 4-15).
	Updated the second note in Section 4.7.1 "Bit-Reversed Addressing Implementation".
Section 8.0 "Direct Memory Access (DMA)"	Updated the DMA Controller diagram (see Figure 8-1).
Section 14.0 "Input Capture"	Updated the bit values for the ICx clock source of the ICTSEL<12:10> bits in the ICxCON1 register (see Register 14-1).
Section 15.0 "Output Compare"	Updated the bit values for the OCx clock source of the OCTSEL<2:0> bits in the OCxCON1 register (see Register 15-1).
	Removed the DCB<1:0> bits from the Output Compare x Control Register 2 (see Register 15-2).

TABLE A-2: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
Section 16.0 "High-Speed PWM Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)"	Updated the High-Speed PWM Module Register Interconnection Diagram (see Figure 16-2). Added the TRGCONx and TRIGx registers (see Register 16-12 and Register 16-14, respectively).
Section 21.0 "Enhanced CAN (ECAN™) Module (dsPIC33EPXXXGP/MC50X Devices Only)"	Updated the CANCKS bit value definitions in CiCTRL1: ECAN Control Register 1 (see Register 21-1).
Section 22.0 "Charge Time Measurement Unit (CTMU)"	Updated the IRNG<1:0> bit value definitions and added Note 2 in the CTMU Current Control Register (see Register 22-3).
Section 25.0 "Op amp/ Comparator Module"	Updated the Op amp/Comparator I/O Operating Modes Diagram (see Figure 25-1). Updated the User-programmable Blanking Function Block Diagram (see Figure 25-3). Updated the Digital Filter Interconnect Block Diagram (see Figure 25-4). Added Section 25.1 "Op amp Application Considerations". Added Note 2 to the Comparator Control Register (see Register 25-2). Updated the bit definitions in the Comparator Mask Gating Control Register (see Register 25-5).
Section 27.0 "Special Features"	Updated the FICD Configuration Register, updated Note 1, and added Note 3 in the Configuration Byte Register Map (see Table 27-1). Added Section 27.2 "User ID Words".
Section 30.0 "Electrical Characteristics"	Updated the following Absolute Maximum Ratings: • Maximum current out of Vss pin • Maximum current into VDD pin Added Note 1 to the Operating MIPS vs. Voltage (see Table 30-1). Updated all Idle Current (IIDLE) Typical and Maximum DC Characteristics values (see
	Table 30-7). Updated all Doze Current (IDOZE) Typical and Maximum DC Characteristics values (see Table 30-9). Added Note 2, removed parameter CM24, updated the Typical values parameters
	CM10, CM20, CM21, CM32, CM41, CM44, and CM45, and updated the Minimum values for CM40 and CM41, and the Maximum value for CM40 in the AC/DC Characteristics: Op amp/Comparator (see Table 30-14).
	Updated Note 2 and the Typical value for parameter VR310 in the Op amp/ Comparator Reference Voltage Settling Time Specifications (see Table 30-15).
	Added Note 1, removed parameter VRD312, and added parameter VRD314 to the Op amp/Comparator Voltage Reference DC Specifications (see Table 30-16).
	Updated the Minimum, Typical, and Maximum values for Internal LPRC Accuracy (see Table 30-22).
	Updated the Minimum, Typical, and Maximum values for parameter SY37 in the Reset, Watchdog Timer, Oscillator Start-up Timer, Power-up Timer Timing Requirements (see Table 30-24).
	The Maximum Data Rate values were updated for the SPI2 Maximum Data/Clock Rate Summary (see Table 30-35)

TABLE A-2: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
Section 30.0 "Electrical	These SPI2 Timing Requirements were updated:
Characteristics" (Continued)	 Maximum value for parameter SP10 and the minimum clock period value for SCKx in Note 3 (see Table 30-36, Table 30-37, and Table 30-38)
	 Maximum value for parameter SP70 and the minimum clock period value for SCKx in Note 3 (see Table 30-40 and Table 30-42)
	The Maximum Data Rate values were updated for the SPI2 Maximum Data/Clock Rate Summary (see Table 30-43)
	These SPI1 Timing Requirements were updated:
	 Maximum value for parameters SP10 and the minimum clock period value for SCKx in Note 3 (see Table 30-44, Table 30-45, and Table 30-46)
	 Maximum value for parameters SP70 and the minimum clock period value for SCKx in Note 3 (see Table 30-47 through Table 30-50)
	 Minimum value for parameters SP40 and SP41 see Table 30-44 through Table 30-50)
	Updated all Typical values for the CTMU Current Source Specifications (see Table 30-55).
	Updated Note1, the Maximum value for parameter AD06, the Minimum value for AD07, and the Typical values for AD09 in the ADC Module Specifications (see Table 30-56).
	Added Note 1 to the ADC Module Specifications (12-bit Mode) (see Table 30-57).
	Added Note 1 to the ADC Module Specifications (10-bit Mode) (see Table 30-58).
	Updated the Minimum and Maximum values for parameter AD21b in the 10-bit Mode ADC Module Specifications (see Table 30-58).
	Updated Note 2 in the ADC Conversion (12-bit Mode) Timing Requirements (see Table 30-59).
	Updated Note 1 in the ADC Conversion (10-bit Mode) Timing Requirements (see Table 30-60).

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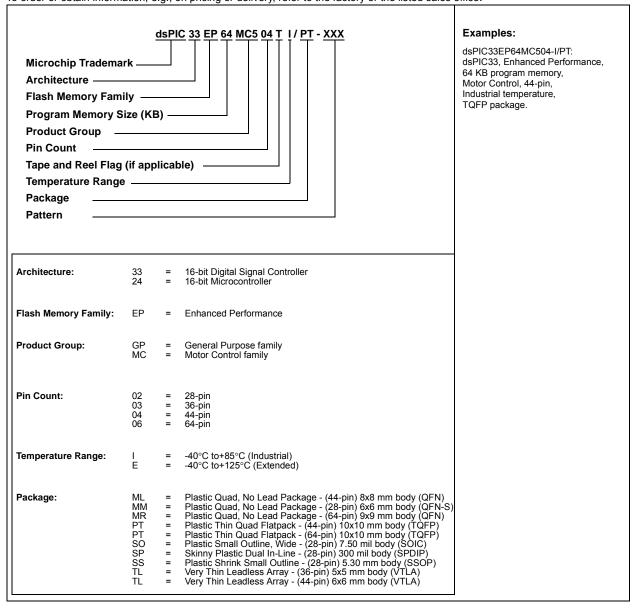
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