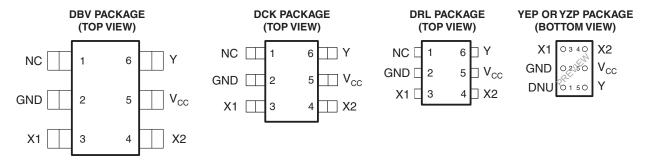


FEATURES

- Available in Texas Instruments NanoStar[™] and NanoFree[™] Packages
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- One Unbuffered Inverter (SN74LVC1GU04) and One Buffered Inverter (SN74LVC1G04)
- Suitable for Commonly Used Clock Frequencies:
 - 15 kHz, 3.58 MHz, 4.43 MHz, 13 MHz,
 25 MHz, 26 MHz, 27 MHz, 28 MHz
- Max t_{pd} of 2.4 ns at 3.3 V
- Low Power Consumption, 10-μA Max I_{CC}

- ±24-mA Output Drive at 3.3 V
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



See mechanical drawings for dimensions.

NC - No internal connection

DNU - Do not use

DESCRIPTION/ORDERING INFORMATION

The SN74LVC1GX04 is designed for 1.65-V to 5.5-V V_{CC} operation. This device incorporates the SN74LVC1GU04 (inverter with unbuffered output) and the SN74LVC1G04 (inverter) functions into a single device. The LVC1GX04 is optimized for use in crystal oscillator applications.

ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING(2)
	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YEP		SN74LVC1GX04YEPR ⁽³⁾	PREVIEW
	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	SN74LVC1GX04YZPR ⁽³⁾	PREVIEW
-40°C to 85°C	SOT (SOT-23) – DBV	Reel of 3000	SN74LVC1GX04DBVR	CX4
	SOT (SOT-23) – DBV	Reel of 250	SN74LVC1GX04DBVT	UA4_
	SOT (SC 70) DCK	Reel of 3000	SN74LVC1GX04DCKR	5
	SOT (SC-70) – DCK	Reel of 250	SN74LVC1GX04DCKT	D2_
	SOT (SOT-553) – DRL	Reel of 4000	SN74LVC1GX04DRLR	UC_

⁽¹⁾ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

⁽³⁾ Package preview



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoStar, NanoFree are trademarks of Texas Instruments.

⁽²⁾ DBV/DCK/DRL: The actual top-side marking has one additional character that designates the assembly/test site. YEP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, ● = Pb-free).



DESCRIPTION/ORDERING INFORMATION (CONTINUED)

X1 and X2 can be connected to a crystal or resonator in oscillator applications. The device provides an additional buffered inverter (Y) for signal conditioning (see Figure 3). The additional buffered inverter improves the signal quality of the crystal oscillator output by making it rail to rail.

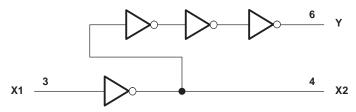
NanoStar[™] and NanoFree[™] package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off} (Y output only). The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

FUNCTION TABLE

INPUT	OUTPUTS				
X1	X2	Υ			
Н	L	Н			
L	Н	L			

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	6.5	V
V _I	Input voltage range (2)		-0.5	6.5	V
Vo	Voltage range applied to Y output in the high-impedance or power-off state (2)			6.5	V
Vo	Voltage range applied to any output in the high or low state (2)(3)			V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
Io	Continuous output current			±50	mA
	Continuous current through V _{CC} or GND			±100	mA
		DBV package		165	
0	Dealers thereal impades (4)	DCK package		259	°C/W
θ_{JA}	Package thermal impedance (4)	DRL package		142	
		YEP/YZP package		123	
T _{stg}	Storage temperature range		-65	150	°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

⁽²⁾ The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

⁽³⁾ The value of V_{CC} is provided in the recommended operating conditions table.

⁽⁴⁾ The package thermal impedance is calculated in accordance with JESD 51-7.



Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT		
		Operating	1.65	5.5			
V_{CC}	Supply voltage	Data retention only	1.5		V		
		Crystal oscillator use	2				
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 5.5 V	$0.75 \times V_{CC}$		V		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 5.5 V		$0.25 \times V_{CC}$	V		
VI	Input voltage		0	5.5	V		
.,	Output wells as	X2, Y	0	V _{CC}	V		
Vo	Output voltage	Y output only, Power-down mode, $V_{CC} = 0 \text{ V}$	0	5.5	V		
		V _{CC} = 1.65 V		-4			
	OH High-level output current	V _{CC} = 2.3 V		-8			
I _{OH}				-16	mA		
		V _{CC} = 3 V		-24			
		V _{CC} = 4.5 V		-32			
		V _{CC} = 1.65 V		4			
		V _{CC} = 2.3 V		8			
I _{OL}	Low-level output current			16	mA		
		V _{CC} = 3 V		24			
		V _{CC} = 4.5 V		32			
		V_{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20			
Δt/Δν	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		10	ns/V		
		V _{CC} = 5 V ±0.5 V		10	0		
T _A	Operating free-air temperature	,	-40	85	°C		

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PAF	RAMETER	TEST C	CONDITIONS	V _{cc}	MIN TY	P ⁽¹⁾ MAX	UNIT		
		$I_{OH} = -100 \mu A$		1.65 V to 5.5 V	V _{CC} - 0.1				
	V	$I_{OH} = -4 \text{ mA}$		1.65 V	1.2				
V		$I_{OH} = -8 \text{ mA}$	V _I = 5.5 V or GND	2.3 V	1.9] _V		
V _{OH}	$I_{OH} = -16 \text{ mA}$	V ₁ = 5.5 V OI GIND	3 V	2.4		V			
		$I_{OH} = -24 \text{ mA}$		3 V	2.3				
		$I_{OH} = -32 \text{ mA}$		4.5 V	3.8				
		I _{OL} = 100 μA		1.65 V to 5.5 V	0.1		V		
		$I_{OL} = 4 \text{ mA}$		1.65 V	0.45				
V		$I_{OL} = 8 \text{ mA}$	V _I = 5.5 V or GND	2.3 V	0.3				
V _{OL}		$I_{OL} = 16 \text{ mA}$	V ₁ = 5.5 V OI GIND	3 V					
		$I_{OL} = 24 \text{ mA}$		3 V					
		I _{OL} = 32 mA		4.5 V	0.55				
I _I	X1	V _I = 5.5 V or GND		0 to 5.5 V		±5	μΑ		
I _{off}	X1, Y	V _I or V _O = 5.5 V		0		±10	μΑ		
I _{CC}		$V_I = 5.5 \text{ V or GND},$	I _O = 0	1.65 V to 5.5 V		10	μΑ		
C _i		$V_I = V_{CC}$ or GND		3.3 V		7	pF		

⁽¹⁾ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 15 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = ± 0.	1.8 V 15 V	V _{CC} = ± 0.	2.5 V 2 V	V _{CC} = ± 0.	3.3 V 3 V	V _{CC} = ± 0.		UNIT
	(INFOT)	(OUTFUT)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
	X1	X2	1	4	0.8	2.6	0.6	2.4	0.5	2	20
^L pd	A1	Υ(1)	3.5	10	2.2	6	2	5	1.5	3.5	ns

⁽¹⁾ X2 - no external load

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 30 \text{ pF}$ or 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM	FROM TO (INPUT) (OUTPUT)		V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		= 5 V 5 V	UNIT
	(INFOT)	(OUTFUT)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
,	VA	X2	1.1	7	0.8	4	8.0	3.7	0.8	3	
T _{pd}	X1	Υ(1)	3.8	18	2	7.4	2	7.8	2	5	ns

⁽¹⁾ X2 - no external load

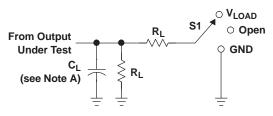
Operating Characteristics

 $T_A = 25^{\circ}C$

PARAMETER		TEST	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	V _{CC} = 5 V	UNIT	
	FARAMETER	CONDITIONS	TYP	TYP	TYP	TYP	UNII	
C_{pd}	Power dissipation capacitance	f = 10 MHz	22	22	24	35	pF	



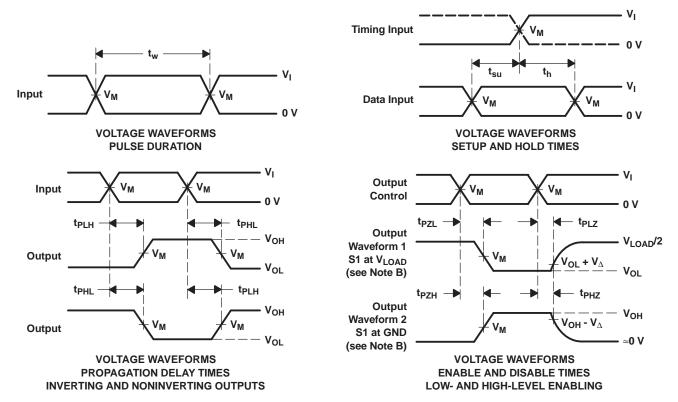
PARAMETER MEASUREMENT INFORMATION



TEST	S1
t _{PLH} /t _{PHL}	Open
t _{PLZ} /t _{PZL}	V_{LOAD}
t _{PHZ} /t _{PZH}	GND

LOAD CIRCUIT

.,	INF	PUTS	.,	.,		_	V
V _{CC}	VI	t _r /t _f	_r /t _f V _M V _{LOAD}		CL	R _L	$oldsymbol{V}_{\Delta}$
1.8 V \pm 0.15 V	V _{CC}	≤2 ns	V _{CC} /2	2×V _{CC}	15 pF	1 M Ω	0.15 V
2.5 V \pm 0.2 V	V _{CC}	≤2 ns	V _{CC} /2	2×V _{CC}	15 pF	1 M Ω	0.15 V
3.3 V \pm 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	15 pF	1 Μ Ω	0.3 V
5 V \pm 0.5 V	V _{CC}	≤2.5 ns	V _{CC} /2	2×V _{CC}	15 pF	1 Μ Ω	0.3 V



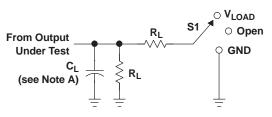
NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50~\Omega$.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



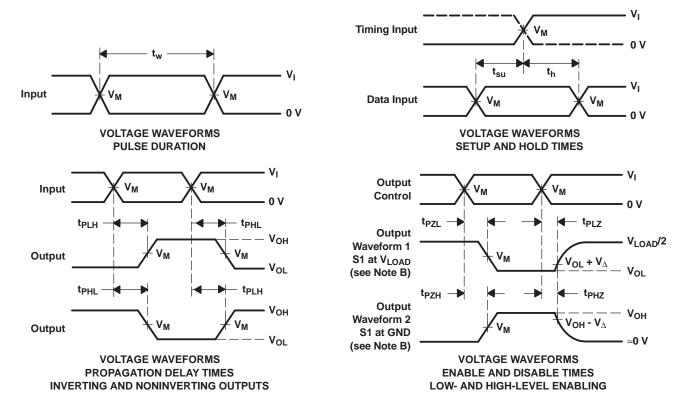
PARAMETER MEASUREMENT INFORMATION



TEST	S1
t _{PLH} /t _{PHL}	Open
t _{PLZ} /t _{PZL}	V _{LOAD}
t _{PHZ} /t _{PZH}	GND

LOAD CIRCUIT

V	INF	PUTS	· ·	V		1	
V _{CC}	VI	t _r /t _f	V _M	V _{LOAD}	CL	R_L	$oldsymbol{V}_{\Delta}$
1.8 V \pm 0.15 V	v _{cc}	≤2 ns	V _{CC} /2	2×V _{CC}	30 pF	1 k Ω	0.15 V
2.5 V \pm 0.2 V	V_{CC}	≤2 ns	V _{CC} /2	2×V _{CC}	30 pF	500 Ω	0.15 V
3.3 V \pm 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V \pm 0.5 V	v_{cc}	≤2.5 ns	V _{CC} /2	2×V _{CC}	50 pF	500 Ω	0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \ \Omega$.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. All parameters and waveforms are not applicable to all devices.

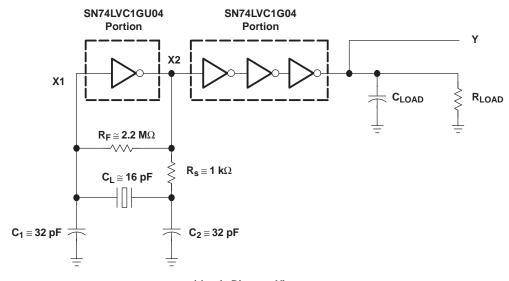
Figure 2. Load Circuit and Voltage Waveforms



APPLICATION INFORMATION

Figure 3 shows a typical application of the SN74LVC1GX04 in a Pierce oscillator circuit. The buffered inverter (SN74LVC1G04 portion) produces a rail-to-rail voltage waveform. The recommended load for the crystal shown in this example is 16 pF. The value of the recommended load (C_L) can be found in the crystal manufacturer's data sheet.

Values of C_1 and C_2 are chosen so that $C_1 = \frac{C_1 C_2}{C_1 + C_2}$ and $C_1 = C_2$. R_s is the current-limiting resistor, and the value depends on the maximum power dissipation of the crystal. Generally, the recommended value of R_s is specified in the crystal manufacturer's data sheet and, usually, this value is approximately equal to the reactance of C_2 at resonance frequency, i.e., $C_2 = \frac{R_s - C_2}{C_2}$. $C_3 = \frac{R_s}{C_3} = \frac{R_s}{C_3}$ is the feedback resistor that is used to bias the inverter in the linear region of operation. Usually, the value is chosen to be within 1 M Ω to 10 M Ω .

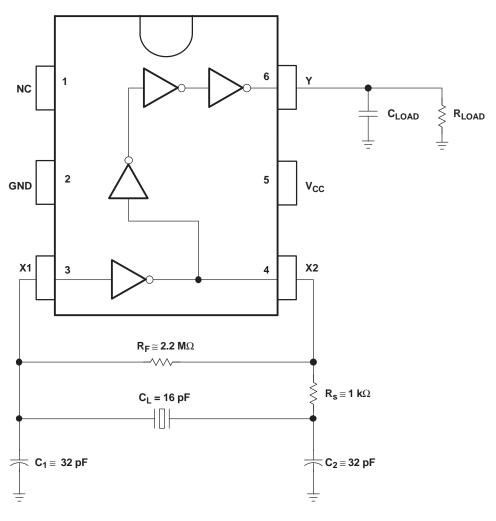


a) Logic Diagram View

Figure 3. Oscillator Circuit



APPLICATION INFORMATION



b) Oscillator Circuit in DBV or DCK Pinout

Figure 3. Oscillator Circuit (continued)

Practical Design Tips

- The open-loop gain of the unbuffered inverter decreases as power-supply voltage decreases. This decreases
 the closed-loop gain of the oscillator circuit. The value of R_s can be decreased to increase the closed-loop
 gain, while maintaining the power dissipation of the crystal within the maximum limit.
- R_s and C₂ form a low-pass filter and reduce spurious oscillations. Component values can be adjusted, based on the desired cutoff frequency.
- ullet C₂ can be increased over C₁ to increase the phase shift and help in start-up of the oscillator. Increasing C₂ may affect the duty cycle of the output voltage.
- At high frequency, phase shift due to R_s becomes significant. In this case, R_s can be replaced by a capacitor to reduce the phase shift.



APPLICATION INFORMATION

Testing

After the selection of proper component values, the oscillator circuit should be tested using these components. To ensure that the oscillator circuit performs within the recommended operating conditions, follow these steps:

- 1. Without a crystal, the oscillator circuit should not oscillate. To check this, the crystal can be replaced by its equivalent parallel-resonant resistance.
- 2. When the power-supply voltage drops, the closed-loop gain of the oscillator circuit reduces. Ensure that the circuit oscillates at the appropriate frequency at the lowest V_{CC} and highest V_{CC} .
- 3. Ensure that the duty cycle, start-up time, and frequency drift over time is within the system requirements.







PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74LVC1GX04DBVRE4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVC1GX04DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVC1GX04DBVTE4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVC1GX04DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVC1GX04DCKRE4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVC1GX04DCKRG4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVC1GX04DCKTE4	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVC1GX04DCKTG4	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVC1GX04DRLRG4	ACTIVE	SOT	DRL	6	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1GX04DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1GX04DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1GX04DCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1GX04DCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1GX04DRLR	ACTIVE	SOT	DRL	6	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is



PACKAGE OPTION ADDENDUM

18-Sep-2008

provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC1GX04:

Enhanced Product: SN74LVC1GX04-EP

NOTE: Qualified Version Definitions:

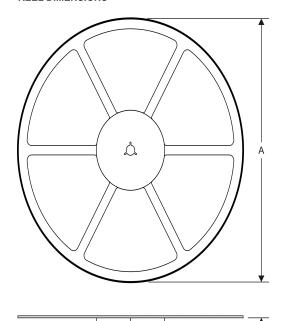
• Enhanced Product - Supports Defense, Aerospace and Medical Applications

PACKAGE MATERIALS INFORMATION

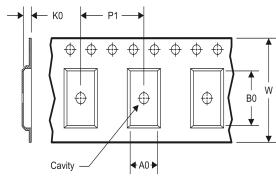
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TAPE AND REEL INFORMATION

REEL DIMENSIONS







A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter	Reel Width	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
	,,	Ū			(mm)	W1 (mm)	` ,	` ,	` ,	` ,	` ,	
SN74LVC1GX04DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1GX04DBVR	SOT-23	DBV	6	3000	178.0	9.2	3.3	3.2	1.55	4.0	8.0	Q3
SN74LVC1GX04DBVT	SOT-23	DBV	6	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1GX04DCKR	SC70	DCK	6	3000	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
SN74LVC1GX04DCKR	SC70	DCK	6	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1GX04DCKR	SC70	DCK	6	3000	180.0	8.4	2.25	2.4	1.22	4.0	8.0	Q3
SN74LVC1GX04DCKT	SC70	DCK	6	250	180.0	8.4	2.25	2.4	1.22	4.0	8.0	Q3
SN74LVC1GX04DRLR	SOT	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1GX04DBVR	SOT-23	DBV	6	3000	202.0	201.0	28.0
SN74LVC1GX04DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
SN74LVC1GX04DBVT	SOT-23	DBV	6	250	202.0	201.0	28.0
SN74LVC1GX04DCKR	SC70	DCK	6	3000	205.0	200.0	33.0
SN74LVC1GX04DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
SN74LVC1GX04DCKR	SC70	DCK	6	3000	202.0	201.0	28.0
SN74LVC1GX04DCKT	SC70	DCK	6	250	202.0	201.0	28.0
SN74LVC1GX04DRLR	SOT	DRL	6	4000	202.0	201.0	28.0

DBV (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- Falls within JEDEC MO-178 Variation AB, except minimum lead width.



DBV (R-PDSO-G6)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



DCK (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-203 variation AB.



DCK (R-PDSO-G6)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



DRL (R-PDSO-N6)

PLASTIC SMALL OUTLINE



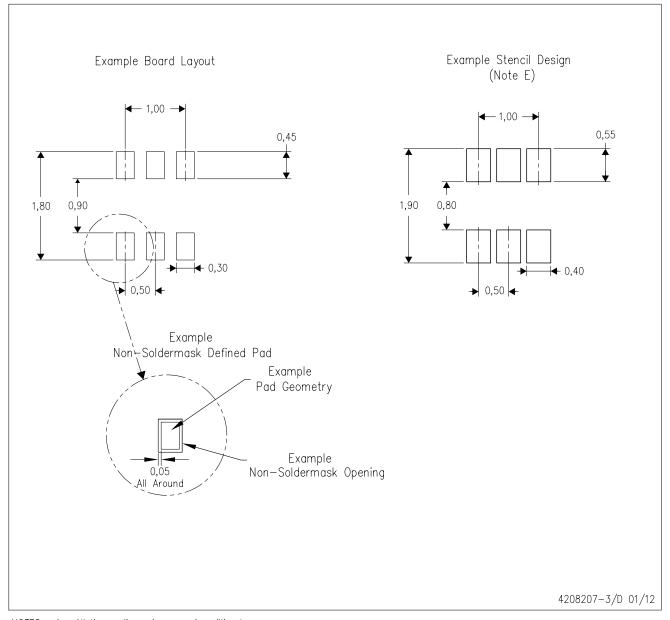
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs.

 Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
- D. JEDEC package registration is pending.



DRL (R-PDSO-N6)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
- E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
- F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- G. Side aperture dimensions over—print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.



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