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2.5-V PHASE-LOCKED-LOOP CLOCK DRIVER

FEATURES

- Spread-Spectrum Clock Compatible
- Operating Frequency: 60 MHz to 220 MHz
- Low Jitter (Cycle-Cycle): ±35 ps
- Low Static Phase Offset: ±50 ps
- Low Jitter (Period): ±30 ps
- 1-to-10 Differential Clock Distribution (SSTL2)
- Best in Class for V_{OX} = V_{DD}/2 ±0.1 V
- Operates From Dual 2.6-V or 2.5-V Supplies
- Available in a 40-Pin MLF Package, 48-Pin TSSOP Package, 56-Ball MicroStar Junior™ BGA Package
- Consumes < 100-μA Quiescent Current
- External Feedback Pins (FBIN, FBIN) Are Used to Synchronize the Outputs to the Input Clocks
- Meets/Exceeds JEDEC Standard (JESD82-1)
 For DDRI-200/266/333 Specification
- Meets/Exceeds Proposed DDRI-400 Specification (JESD82-1A)
- Enters Low-Power Mode When No CLK Input Signal Is Applied or PWRDWN Is Low

APPLICATIONS

- DDR Memory Modules (DDR400/333/266/200)
- Zero-Delay Fan-Out Buffer

DESCRIPTION

The CDCVF857 is a high-performance, low-skew, low-jitter, zero-delay buffer that distributes a differential clock input pair (CLK, CLK) to 10 differential pairs of clock outputs (Y[0:9], Y[0:9]) and one differential pair of feedback clock outputs (FBOUT, FBOUT). The clock outputs are controlled by the clock inputs (CLK, CLK), the feedback clocks (FBIN, FBIN), and the analog power input (AVDD). When PWRDWN is high, the outputs switch in phase and frequency with CLK. When PWRDWN is low, all outputs are disabled to a high-impedance state (3-state) and the PLL is shut down (low-power mode). The device also enters this low-power mode when the input frequency falls below a suggested detection frequency that is below 20 MHz (typical 10 MHz). An input frequency detection circuit detects the low frequency condition and, after applying a >20-MHz input signal, this detection circuit turns the PLL on and enables the outputs.

When AV_{DD} is strapped low, the PLL is turned off and bypassed for test purposes. The CDCVF857 is also able to track spread spectrum clocking for reduced EMI.

Because the CDCVF857 is based on PLL circuitry, it requires a stabilization time to achieve phase-lock of the PLL. This stabilization time is required following power up. The CDCVF857 is characterized for both commercial and industrial temperature ranges.

AVAILABLE OPTIONS

T _A	TSSOP (DGG)	40-Pin MLF	56-Ball BGA ⁽¹⁾
–40°C to 85°C	CDCVF857DGG	CDCVF857RTB	CDCVF857GQL
−40°C to 85°C		CDCVF857RHA	CDCVF857ZQL

(1) Maximum load recommended is 12 pf for 200 MHz. At 12-pf load, maximum T_A allowed is 70°C.



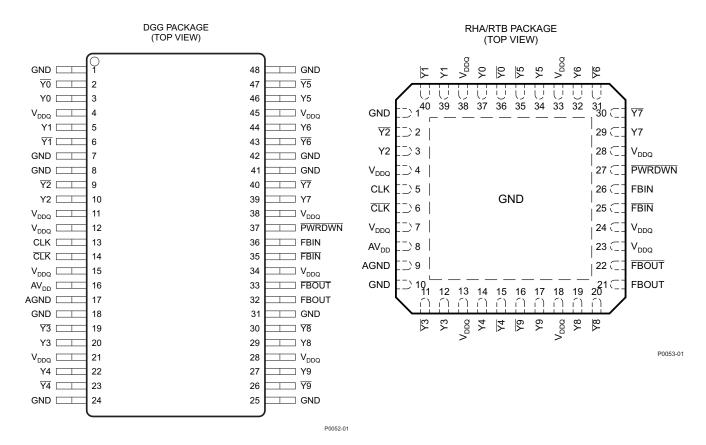
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MicroStar Junior is a trademark of Texas Instruments.



FUNCTION TABLE (Select Functions)

	INPUTS				OUTPUTS				
AVDD	PWRDWN	CLK	CLK	Y[0:9]	<u>Y[0:9]</u>	FBOUT	FBOUT		
GND	Н	L	Н	L	Н	L	Н	Bypassed/off	
GND	Н	Н	L	Н	L	Н	L	Bypassed/off	
Х	L	L	Н	Z	Z	Z	Z	Off	
Х	L	Н	L	Z	Z	Z	Z	Off	
2.5 V (nom)	Н	L	Н	L	Н	L	Н	On	
2.5 V (nom)	Н	Н	L	Н	L	Н	L	On	
2.5 V (nom)	X	<20 MHz	<20 MHz	Z	Z	Z	Z	Off	





MicroStar Junior™ BGA (GQL/ZQL) PACKAGE (TOP VIEW) GND 2 Υ2 2 3 5 6 В <u>Y6</u> <u>Y1</u> -Υ1 Y6 NC NC GND GND GND GND (NC) NC Y7 $\frac{Y2}{Y2}$ 77 NB Ε **PWRDWN** $V_{DDQ} \ V_{DDQ}$ V_{DDQ} NB NB **FBIN** CLK CLK FBIN NC NC G $V_{\rm DDQ}$ $\begin{matrix} V_{DDQ} \\ A_{VDD} \end{matrix}$ FBOUT NC NC FBOUT AGND GND GND <u>78</u> Y3 Y3 Y8 Κ V_{DDQ} GND 7 74 V_{DDQ} 79 γ3

NB = No Ball NC = No Connection

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FUNCTIONAL BLOCK DIAGRAM

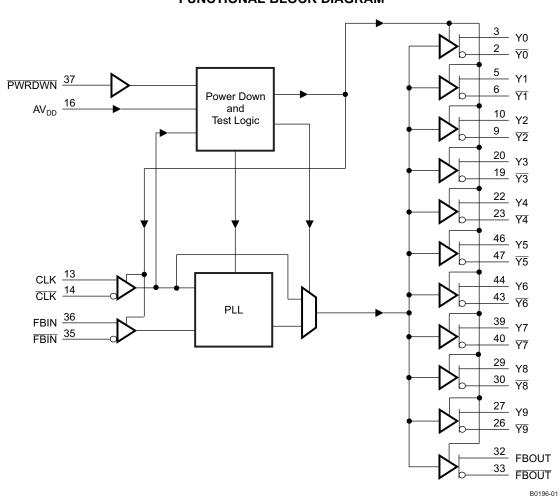




Table 1. TERMINAL FUNCTIONS

	TE	ERMINAL		1/0	DESCRIPTION
NAME	DGG	RHA/RTB	GQL/ZQL	1/0	DESCRIPTION
AGND	17	9	H1	-	Ground for 2.5-V analog supply
AV_{DD}	16	8	G2	_	2.5-V analog supply
CLK, CLK	13, 14	5, 6	F1, F2	ı	Differential clock input
FBIN, FBIN	35, 36	25, 26	F5, F6	- 1	Feedback differential clock input
FBOUT, FBOUT	32, 33	21, 22	H6, G5	0	Feedback differential clock output
GND	1, 7, 8, 18, 24, 25, 31, 41, 42, 48	1, 10	A3, A4, C1, C2, C5, C6, H2, H5, K3, K4	-	Ground
PWRDWN	37	27	E6	I	Output enable for Y and \overline{Y}
V_{DDQ}	4, 11, 12, 15, 21, 28, 34, 38, 45	4, 7, 13, 18, 23, 24, 28, 33, 38	B3, B4, E1, E2, E5, G1, G6, J3, J4	_	2.5-V supply
Y0, ₹0	3, 2	37, 36	A1, A2	0	
Y1, Y 1	5, 6	39, 40	B2, B1	0	
Y2, ₹ 2	10, 9	3, 2	D1, D2	0	
Y3, ₹3	20, 19	12,11	J2, J1	0	
Y4, ₹4	22, 23	14, 15	K1, K2	0	Buffered output copies of input clock, CLK, CLK
Y5, ₹5	46, 47	34, 35	A6, A5	0	Burrered output copies of imput clock, CER, CER
Y6, ₹6	44, 43	32, 31	B5, B6	0	
Y7, ₹ 7	39, 40	29, 30	D6, D5	0	
Y8, ₹8	29, 30	19, 20	J5, J6	0	
Y9, ▼ 9	27, 26	17, 16	K6, K5	0	

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

V_{DDQ} , AV_{DD}	Supply voltage range		0.5 V to 3.6 V
VI	Input voltage range (2)(3)		–0.5 V to V _{DDQ} + 0.5 V
Vo	Output voltage range (2)(3)		-0.5 V to V _{DDQ} + 0.5 V
I _{IK}	Input clamp current	$V_I < 0$ or $V_I > V_{DDQ}$	±50 mA
I _{OK}	Output clamp current	$V_O < 0$ or $V_O > V_{DDQ}$	±50 mA
Io	Continuous output current	$V_O = 0$ to V_{DDQ}	±50 mA
I _{DDC}	Continuous current to GND or V _{DDQ}		±100 mA
T _{stg}	Storage temperature range		−65°C to 150°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

R _{0JA} for	R _{θJA} for TSSOP (DGG) Package ⁽¹⁾			F (RHA/RTB) Package	R _{θJA} for BGA (GQL/ZQL) Package ⁽²⁾		
Airflow	Low K	High K	Airflow	With 4 Thermal Vias	Airflow	High K	
0 ft/min	89.1°C/W	70°C/W	0 ft/min	44.7°C/W	0 ft/min	132.2°C/W	
150 ft/min	78.5°C/W	65.3°C/W	150 ft/min		150 ft/min	126.4°C/W	

⁽¹⁾ The package thermal impedance is calculated in accordance with JESD 51.

⁽²⁾ The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

⁽³⁾ This value is limited to 3.6 V maximum.

⁽²⁾ Connecting the NC-balls (C3, C4, D3, D4, G3, G4, H3, H4) to a ground plane improves the θ_{JA} to 114.8°C/W (0 airflow).



RECOMMENDED OPERATING CONDITIONS

				MIN	NOM MAX	UNIT
	Cupply voltage	V _{DDQ} PC1600 – PC3200		2.3	2.7	V
	Supply voltage	AVDD		V _{DDQ} - 0.12	2.7	V
\/	Low-level input voltage	CLK, CLK, I	FBIN, <u>FBIN</u>		$V_{DDQ}/2 - 0.18$	V
V_{IL}	Low-level input voltage	PWRDWN		-0.3	0.7	V
\/	Lligh lovel input veltage	CLK, CLK, I	FBIN, <u>FBIN</u>	VDDQ/2 + 0.18		V
V _{IH}	High-level input voltage	PWRDWN		1.7	V _{DDQ} + 0.3	V
	DC input signal voltage (1)			-0.3	$V_{DDQ} + 0.3$	V
\/	Differential input signal voltage (2)	DC	CLK, FBIN	0.36	$V_{DDQ} + 0.6$	V
V_{ID}	Differential input signal voltage (-)	AC	CLK, FBIN	0.7	$V_{DDQ} + 0.6$	V
V_{IX}	Input differential pair cross voltage (3)(4)			$V_{DDQ}/2 - 0.2$	$V_{DDQ}/2 + 0.2$	V
I _{OH}	High-level output current				-12	mA
I_{OL}	Low-level output current				12	mA
SR	Input slew rate			1	4	V/ns
T _A	Operating free-air temperature			-40	85	°C

- (1) The unused inputs must be held high or low to prevent them from floating.
- The dc input signal voltage specifies the allowable dc execution of the differential input.
- The differential input signal voltage specifies the differential voltage |VTR VCP| required for switching, where VTR is the true input level and VCP is the complementary input level.

 The differential cross-point voltage tracks variations of V_{CC} and is the voltage at which the differential signals must cross.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP (1)	MAX	UNIT
V_{IK}	Input voltage, all inputs	$V_{DDQ} = 2.3 \text{ V}, I_{I} = -18 \text{ mA}$				-1.2	V
V	Lligh lovel output voltage	V_{DDQ} = min to max, I_{OH} = -	$V_{DDQ} = min to max, I_{OH} = -1 mA$				V
V _{OH}	High-level output voltage	$V_{DDQ} = 2.3 \text{ V}, I_{OH} = -12 \text{ mA}$		1.7			V
V	Low-level output voltage	$V_{DDQ} = min to max, I_{OL} = 1$	mA			0.1	V
V _{OL}	Low-level output voltage	$V_{DDQ} = 2.3 \text{ V}, I_{OL} = 12 \text{ mA}$				0.6	V
V_{OD}	Output voltage swing (2)	Differential outputs are tern	ainated with	1.1		$V_{DDQ} - 0.4$	V
V _{OX}	Output differential cross-voltage (3)	120 Ω , $C_L = 14 \text{ pF}$ (see Fig		$V_{DDQ}/2 - 0.1$	$V_{\rm DDQ}/2$	$V_{DDQ}/2 + 0.1$	V
I	Input current	$V_{DDQ} = 2.7 \text{ V}, V_{I} = 0 \text{ V to } 2$.7 V			±10	μΑ
I _{OZ}	High-impedance-state output current	$V_{DDQ} = 2.7 \text{ V}, V_{O} = V_{DDQ} \text{ or GND}$				±10	μΑ
I _{DDPD}	Power-down current on V _{DDQ} + AV _{DD}	CLK and $\overline{\text{CLK}} = 0 \text{ MHz}$; $\overline{\text{PV}}$ Low; Σ of I_{DD} and AI_{DD}	CLK and $\overline{\text{CLK}} = 0 \text{ MHz}$; $\overline{\text{PWRDWN}} = \text{Low}$; Σ of I_{DD} and AI_{DD}		20	100	μΑ
Λ1	Cumply ourrant on AV	f _O = 170 MHz			6	8	A
Al _{DD}	Supply current on AV _{DD}	f _O = 200 MHz			8	10	mA
C _I	Input capacitance	$V_{DDQ} = 2.5 \text{ V}, V_{I} = V_{DDQ} \text{ or}$	GND	2	2.5	3.5	pF
		Without load	f _O = 170 MHz		120	140	
		Williout loau	f _O = 200 MHz		125	150	
		Differential outputs	f _O = 170 MHz		220	270	
I _{DD}	Dynamic current on V _{DDQ}	terminated with 120 Ω , C _L = 0 pF	f _O = 200 MHz		230	280	mA
		Differential outputs	f _O = 170 MHz		280	330	
		terminated with 120 Ω , C _L = 14 pF	f _O = 200 MHz		300	350	

 ⁽¹⁾ All typical values are at nominal V_{DDQ}.
 (2) The differential output signal voltage specifies the differential voltage |VTR - VCP|, where VTR is the true output level and VCP is the complementary output level.

The differential cross-point voltage tracks variations of V_{DDQ} and is the voltage at which the differential signals must cross. (3)



ELECTRICAL CHARACTERISTICS (continued)

over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾ MA)	UNIT
ΔC	Part-to-part input capacitance variation	$V_{DDQ} = 2.5 \text{ V}, V_{I} = V_{DDQ} \text{ or GND}$			pF
$C_{I(\Delta)}$	Input capacitance difference between CLK and CLK, FBIN, and FBIN	$V_{DDQ} = 2.5 \text{ V}, V_I = V_{DDQ} \text{ or GND}$		0.29	pF

TIMING REQUIREMENTS

over recommended ranges of supply voltage and operating free-air temperature

	PARAMETER	MIN	MAX	UNIT
4	Operating clock frequency	60	220	MHz
† _{CLK}	Application clock frequency	90	220	IVITZ
	Input clock duty cycle	40%	60%	
	Stabilization time (PLL mode) (1)		10	μs
	Stabilization time (bypass mode) (2)		30	ns

⁽¹⁾ The time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLK and V_{DD} must be applied. Until phase lock is obtained, the specifications for propagation delay, skew, and jitter parameters given in the switching characteristics table are not applicable. This parameter does not apply for input modulation under SSC application.

SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH} ⁽¹⁾	Low-to-high level propagation delay time	Test mode/CLK to any output		3.5		ns
t _{PHL} ⁽¹⁾	High-to-low level propagation delay time	Test mode/CLK to any output		3.5		ns
		100 MHz (PC1600)	-65		65	
		133/167/200 MHz (PC2100/2700/3200)	-30		30	ps
(2)	Europe (mode to mode) and Europe (100 MHz (PC1600)	-50		50	
t _{jit(cc)} (2)	Jitter (cycle-to-cycle), see Figure 4	133/167/200 MHz (PC2100/2700/3200)	-35		35	ps
(2)	Half and addition and Figure 0	100 MHz (PC1600)	-100		100	
t _{jit(hper)} (2)	Half-period jitter, see Figure 8	133/167/200 MHz (PC2100/2700/3200)	-75		75	ps
t _{slr(o)}	Output clock slew rate, see Figure 9	Load: 120 Ω, 14 pF	1		2	V/ns
t _(ф)	Static phase offset, see Figure 5	100/133/167/200 MHz	-50		50	ps
t _{sk(o)}	Output skew, see Figure 6	Load: 120 Ω, 14 pF; 100/133/167/200 MHz			40	ps

⁽¹⁾ Refers to the transition of the noninverting output.

⁽²⁾ A recovery time is required when the device goes from power-down mode into bypass mode (AV_{DD} at GND).

⁽²⁾ This parameter is assured by design but cannot be 100% production tested.



PARAMETER MEASUREMENT INFORMATION

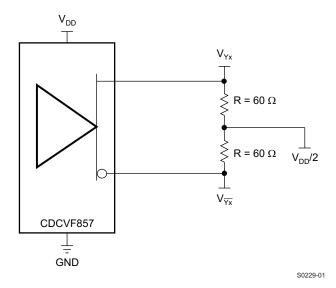


Figure 1. IBIS Model Output Load

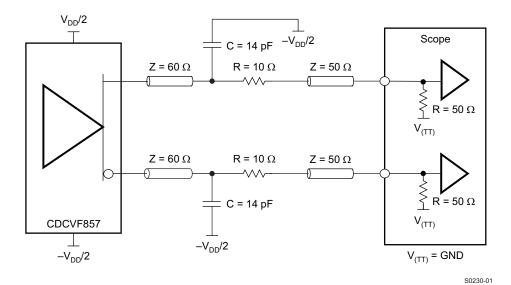


Figure 2. Output Load Test Circuit



PARAMETER MEASUREMENT INFORMATION (continued)

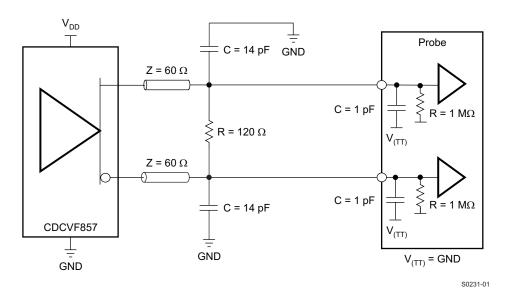


Figure 3. Output Load Test Circuit for Crossing Point

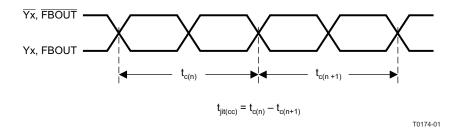


Figure 4. Cycle-to-Cycle Jitter

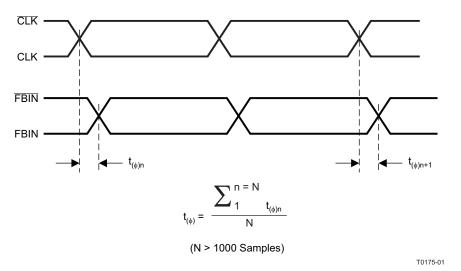


Figure 5. Phase Offset



PARAMETER MEASUREMENT INFORMATION (continued)

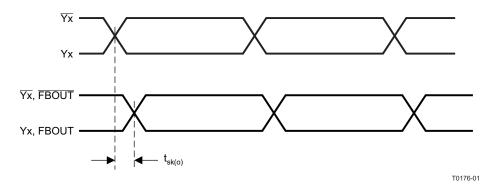
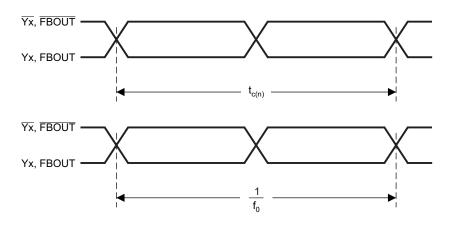


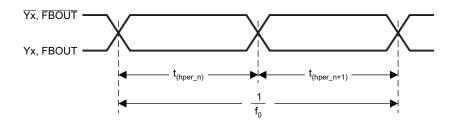
Figure 6. Output Skew



 $t_{\text{jit(per)}} = t_{\text{c(n)}} - \frac{1}{f_0}$ f_0 = Average Input Frequency Measured at CLK/ $\overline{\text{CLK}}$

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Figure 7. Period Jitter



n = Any Half Cycle $t_{\text{jit(hper)}} = t_{\text{(hper_n)}} - \frac{1}{2 \times f_0}$ n = Any Half Cycle $f_0 = \text{Average Input Frequency Measured at CLK/CLK}$

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Figure 8. Half-Period Jitter



PARAMETER MEASUREMENT INFORMATION (continued)

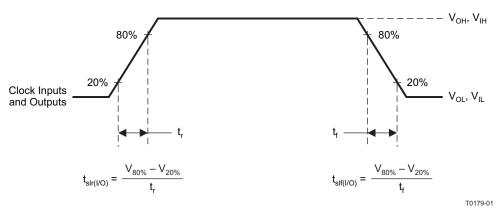
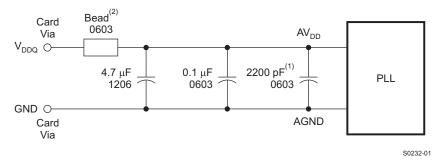


Figure 9. Input and Output Slew Rates



- (1) Place the 2200-pF capacitor close to the PLL.
- (2) Recommended bead: Fair-Rite P/N 2506036017Y0 or equilvalent (0.8 Ω dc maximum, 600 Ω at 100 MHz).

NOTE: Use a wide trace for the PLL analog power and ground. Connect PLL and capacitors to AGND trace and connect trace to one GND via (farthest from the PLL).

Figure 10. Recommended AV_{DD} Filtering



14-Jun-2010

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
CDCVF857DGG	ACTIVE	TSSOP	DGG	48	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Request Free Samples
CDCVF857DGGG4	ACTIVE	TSSOP	DGG	48	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Request Free Samples
CDCVF857DGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples
CDCVF857DGGRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples
CDCVF857GQLR	ACTIVE	BGA MICROSTAR JUNIOR	GQL	56	1000	TBD	SNPB	Level-2A-220C-4 WKS	Request Free Samples
CDCVF857RHAR	ACTIVE	VQFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Purchase Samples
CDCVF857RHARG4	ACTIVE	VQFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Purchase Samples
CDCVF857RHAT	ACTIVE	VQFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Request Free Samples
CDCVF857RHATG4	ACTIVE	VQFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Request Free Samples
CDCVF857RTBR	OBSOLETE	VQFN	RTB	40		TBD	Call TI	Call TI	Replaced by CDCVF857RHAR
CDCVF857RTBT	OBSOLETE	VQFN	RTB	40		TBD	Call TI	Call TI	Replaced by CDCVF857RHAT
CDCVF857ZQLR	ACTIVE	BGA MICROSTAR JUNIOR	ZQL	56	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-2-260C-1 YEAR	Request Free Samples

⁽¹⁾ The marketing status values are defined as follows: **ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.



PACKAGE OPTION ADDENDUM

14-Jun-2010

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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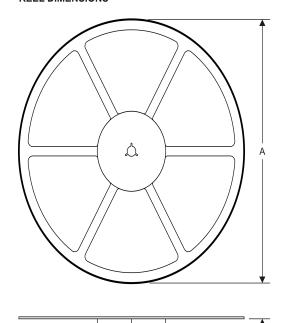
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PACKAGE MATERIALS INFORMATION

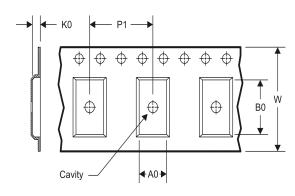
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TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCVF857DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1
CDCVF857GQLR	BGA MI CROSTA R JUNI OR	GQL	56	1000	330.0	16.4	4.8	7.3	1.45	8.0	16.0	Q1
CDCVF857RHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
CDCVF857RHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
CDCVF857ZQLR	BGA MI CROSTA R JUNI OR	ZQL	56	1000	330.0	16.4	4.8	7.3	1.45	8.0	16.0	Q1

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*All dimensions are nominal

All difficusions are norminal							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCVF857DGGR	TSSOP	DGG	48	2000	346.0	346.0	41.0
CDCVF857GQLR	BGA MICROSTAR JUNIOR	GQL	56	1000	333.2	345.9	28.6
CDCVF857RHAR	VQFN	RHA	40	2500	346.0	346.0	33.0
CDCVF857RHAT	VQFN	RHA	40	250	210.0	185.0	35.0
CDCVF857ZQLR	BGA MICROSTAR JUNIOR	ZQL	56	1000	333.2	345.9	28.6

ZQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-285 variation BA-2.
- D. This package is Pb-free. Refer to the 56 GQL package (drawing 4200583) for tin-lead (SnPb).

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GQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-285 variation BA-2.
- D. This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.





- NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) Package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - F. Package complies to JEDEC MO-220 variation VJJD-2.



RHA (S-PVQFN-N40)

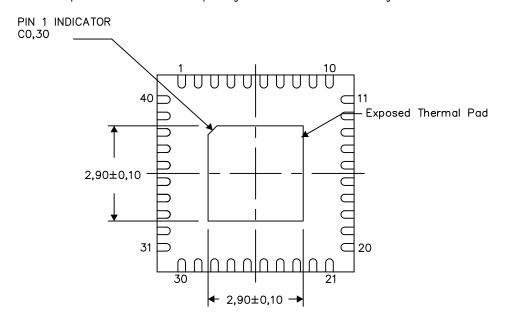
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No—Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

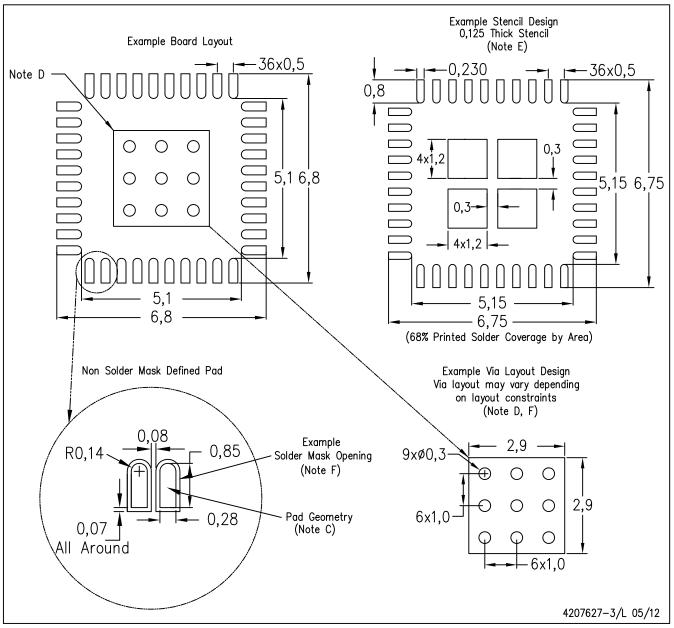
4206355-3/Q 05/12

NOTES: A. All linear dimensions are in millimeters



RHA (S-PVQFN-N40)

PLASTIC QUAD FLATPACK NO-LEAD



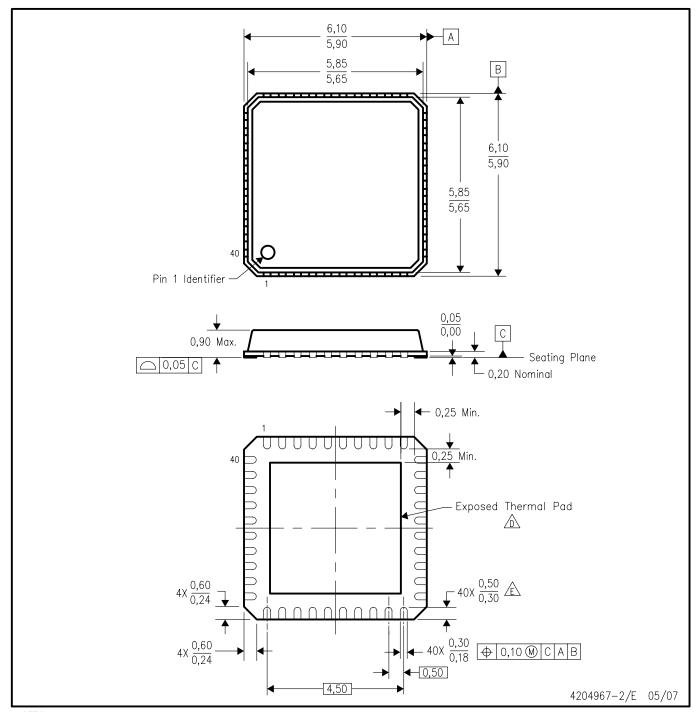
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat—Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.



RTB (S-PQFP-N40)

PLASTIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters.

Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) Package configuration.

The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions. Some products have selected lands extended past 0,50 length. See Product Data Sheet for details regarding specific land length exceptions.



DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

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