PW PACKAGE (TOP VIEW)

AGND

V_{CC} 🛭 2

1Y0 🛮 3

1Y1 1Y2

GND

24

23

15

CLK

AV_{CC}

2Y3

□ v_{cc} 2G 14 13 **∏** FBIN

- Use CDCVF2509A as a Replacement for this Device
- **Designed to Meet PC SDRAM Registered DIMM Specification**
- **Spread Spectrum Clock Compatible**
- Operating Frequency 25 MHz to 125 MHz
- Phase Error Time Minus Jitter at 66 MHz to 100 MHz Is ±150 ps
- Jitter (peak peak) at 66 MHz to 100 MHz Is ±80 ps
- Jitter (cycle cycle) at 66 MHz to 100 MHz

- FBOU

 FBOU

description

The CDC2509B is a high-performance, low-skew, low-jitter, phase-lock loop (PLL) clock drivers. They use a PLL to precisely a gr, in both frequency and phase, the feedback (FBOUT) output to the clock (CLK) input signal. They are so incall Cosigned for use with synchronous DRAMs. The CDC2509B operates at 3.3-V V_{CC}. They also provide integrated series-damping resistors that make it ideal for driving point-to-point loads.

One bank of five outputs and one bank of four outputs provide nine low-skew, low-jitter copies of CLK. Output signal duty cycles are adjusted to 50%, independent of the duty cycle at CLK. Each bank of outputs is enabled or disabled separately via the control (1G and 2G) inputs. When the G inputs are high, the outputs switch in phase and frequency with CLK; when the G inputs are low, the outputs are disabled to the logic-low state.

Unlike many products containing PLLs, the CDC2509B does not require external RC networks. The loop filter for the PLL is included on-chip, minimizing component count, board space, and cost.

Because it is based on PLL circuitry, the CDC2509B requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization time is required, following power up and application of a fixed-frequency, fixed-phase signal at CLK, and following any changes to the PLL reference or feedback signals. The PLL can be bypassed for test purposes by strapping AV_{CC} to ground.



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STRUMENTS

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description (continued)

The CDC2509B is characterized for operation from 0°C to 70°C.

For application information refer to application reports High Speed Distribution Design Techniques for CDC509/516/2509/2510/2516 (literature number SLMA003) and Using CDC2509A/2510A PLL with Spread Spectrum Clocking (SSC) (literature number SCAA039).

AND SELECTION OF A SECONDARY OF A SE functional block diagram 2G ________ 21 2Y0 20 2Y1 CLK ______ 17 2Y2 PLL 16 2Y3 FBIN -12 FBOUT AVCC **AVAILABLE OPTIONS**



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	PACKAGE
TA	SMALL OUTLINE (PW)
0°C to 70°C	CDC2509BPWR

Terminal Functions

TEF	RMINAL		
NAME	NO.	I/O	DESCRIPTION
CLK	24	-	Clock input. CLK provides the clock signal to be distributed, with CDCs 19B and the CDC2510B clock drivers. CLK is used to provide the reference signal to the interacted PLL that generates the clock output signals. CLK must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and a valid CLK signal is applied, a stability don time is required for the PLL to phase lock the feedback signal to its reference signal.
FBIN	13	I	Feedback input. FBIN provides the feedback small to the internal PLL. FBIN must be hard-wired to FBOUT to complete the PLL. The integrated PLL synch onizes CLK and FBIN so that there is nominally zero phase error between CLK and FBIN.
1G	11	Ι	Output bank enable. 1G is the output enable by putputs 1Y(0:4). When 1G is low, outputs 1Y(0:4) are disabled to a logic-low state. When 4G is high, all outputs 1Y(0:4) are enabled and switch at the same frequency as CLK.
2G	14	1	Output bank enable. 20 is 10 output enable for outputs 2Y(0:3). When 2G is low, outputs 2Y(0:3) are disabled to a logic lows, at2. When 2G is high, all outputs 2Y(0:3) are enabled and switch at the same frequency as CLK.
FBOUT	12	0	Feedback output a DOUT is indicated for external feedback. It switches at the same frequency as CLK. When extendity wire (t) LBIN, FBOUT completes the feedback loop of the PLL. FBOUT has an integrated 1.3 22 ser as damping resistor.
1Y (0:4)	3, 4, 5, 8, 9	0	Clock cutruts. These outputs provide low-skew copies of CLK. Output bank 1Y(0:4) is enabled via the 1C in u. These patputs can be disabled to a logic-low state by deasserting the 1G control input. Each output has an integrated 25- Ω series-damping resistor.
2Y (0:3)	16, 17, 20, 21		clock outputs. These outputs provide low-skew copies of CLK. Output bank 2Y(0:3) is enabled via the 2C in Ω . These outputs can be disabled to a logic-low state by deasserting the 2G control input. Each of the third part of the control input input. Each of the control input is an integrated 25- Ω series-damping resistor.
AVCC	23	Pewer	Malog power supply. AV _{CC} provides the power reference for the analog circuitry. In addition, AV _{CC} can be used to bypass the PLL for test purposes. When AV _{CC} is strapped to ground, PLL is bypassed and CLK is buffered directly to the device outputs.
AGND	1	Ground	Analog ground. AGND provides the ground reference for the analog circuitry.
Vcc	2, 10, 15, 22	Power	Power supply
GND	6, 7, 18, 19	Ground	Ground



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range:	AV _{CC} (see Note 1)		
Input voltage range, VI	(see Note 2)		
Voltage range applied t	o any output in the high or low state	· ,	C
VO (see Notes 2 and	13)		5 V to V _{CC} + 0.5 V
Input clamp current, IIK	$(V_I < 0)$		–50 mA
Output clamp current, I	$OK (VO < 0 \text{ or } VO > VCC) \dots$		±50 mA
Continuous output curre	ent, I_{Ω} ($V_{\Omega} = 0$ to V_{CC})		±50 mA
Continuous current thro	ough each V _{CC} or GND		1. ±100 mA
Maximum power dissip	ation at $I_A = 55^{\circ}C$ (in still air) (see N	Note 4)	O./ VV
Storage temperature ra	inge, T _{sta}		–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent dam to to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicate to der "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device relicoility.

- NOTES: 1. AV_{CC} must not exceed V_{CC}.
 - put clamp-current ratings are observed. 2. The input and output negative-voltage ratings may be exceeded in
 - 3. This value is limited to 4.6 V maximum.
 - This value is limited to 4.0 V maximum.
 The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Consideration note in the ABT Advanced BiCMOS Technology Data Book, literature number SCBD002.

recommended operating conditions (see

	MIN	MAX	UNIT
Supply voltage, V _{CC} , AV _{CC}	3	3.6	V
High-level input voltage, VIH	2		V
Low-level input voltage, V _{IL}		8.0	V
Input voltage, V _I	0	VCC	V
High-level output current, IOH		-12	mA
Low-level output current, IOL		12	mA
Operating free-air temperature TA	0	70	°C

or low to prevent them from floating. NOTE 5: Unused inputs m



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST C	ONDITIONS	V _{CC} , AV _{CC}	MIN	TYP†	MAX	UNIT
VIK	I _I = -18 mA		3 V			-1.2	V
	I _{OH} = -100 μA		MIN to MAX	V _{CC} -0.2	•		
VOH	$I_{OH} = -12 \text{ mA}$		3 V	2.1	9		V
	$I_{OH} = -6 \text{ mA}$		3 V	2.4	~		
	I _{OL} = 100 μA		MIN to MAX		7,	0.2	
V _{OL}	I _{OL} = 12 mA		3 V	0 4		0.8	V
	I _{OL} = 6 mA		34	1		0.55	
lj	$V_I = V_{CC}$ or GND		3.6			±5	μΑ
I _{CC} ‡	$V_I = V_{CC}$ or GND,	$I_O = 0$, Outputs: low or high	3.6 V			10	μΑ
ΔlCC	One input at V _{CC} – 0.6 V,	Other inputs at V _{CC} or GND	33 V to 36 v			500	μΑ
C _i	$V_I = V_{CC}$ or GND	7	3.4		4		pF
Co	$V_O = V_{CC}$ or GND		3.3 V		6		pF

[†] For conditions shown as MIN or MAX, use the appropriate value specified under roomended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		MIN	MAX	UNIT
fclk	Clock frequency	25	125	MHz
	Input clock duty cycle	40%	60%	
	Stabilization time§		1	ms

[§] Time required for the integrated PLL circuit to obtain these lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLK. Until phase lock is obtained, the specifications for propagation delay, skew, and jitter parameters given in the which no characteristics table are not applicable. This parameter does not apply for input modulation under SSC application.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L 30 pF (see Note 6 and Figures 1 and 2) $^{\parallel}$

PARAMETER	FROM	-		V _{CC} , AV _{CC} = 3.3 V ± 0.165 V			V _{CC} , AV _{CC} = 3.3 V ± 0.3 V			
	(INPUT)/CONDITION	(OUTPUT)	MIN	TYP	MAX	MIN	TYP	MAX		
tphase error, – jitter (see Notes 7 and 8, Figures 3, 4, and 5)	CLKIN↑ = 66 MHz to100 MHz	FBIN↑	-150		150	-200		200	ps	
t _{sk(o)} #	Any Y or FBOUT	Any Y or FBOUT						200	ps	
Jitter _(pk-pk) (see Figure 6)		Any Y or FBOUT				-80		80		
Jitter(cycle-cycle) (see Figure 6)	CLKIN = 66 MHz to 100 MHz	Any Y or FBOUT						100	ps	
Duty cycle	F(CLKIN > 60 MHz)	Any Y or FBOUT				45%		55%		
t _r		Any Y or FBOUT		1.3	1.9	0.8		2.1	ns	
tf		Any Y or FBOUT		1.7	2.5	1.2		2.7	ns	

[¶] These parameters are not production tested.

- 7. This is considered as static phase error.
- 8. Phase error does not include jitter. The total phase error is -230 ps to 230 ps for the 5% V_{CC} range.

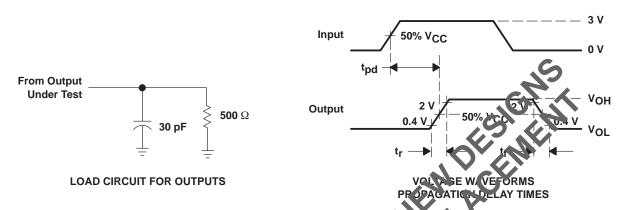


[‡] For ICC of AVCC, and ICC vs Frequency (see Figures 7 and 8).

[#]The t_{sk(O)} specification is only valid for equal loading of all outputs.

NOTES: 6. The specifications for parameters in this table are applicable only after any appropriate stabilization time has elapsed.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characters 00 MHz, $Z_O = 50 \Omega$, $t_r \le 1.2$ ns, $t_f \le 1.2$ ns.
- C. The outputs are measured one at a time with one transition per n

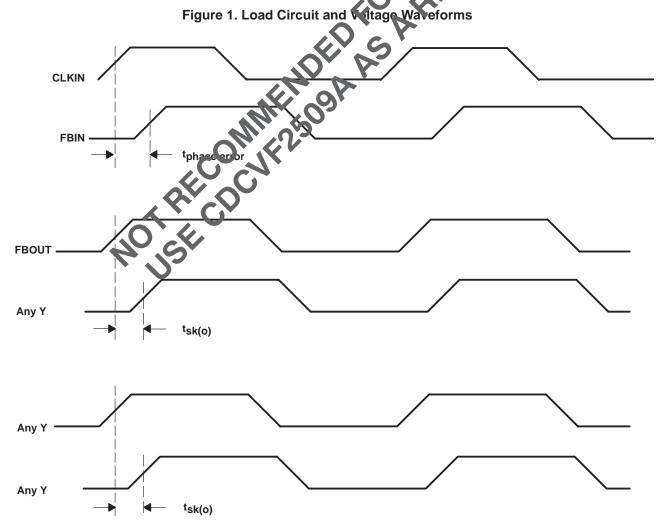


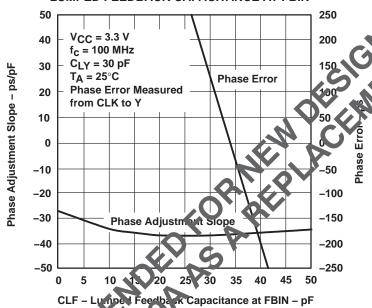
Figure 2. Phase Error and Skew Calculations



TYPICAL CHARACTERISTICS

PHASE ADJUSTMENT SLOPE AND PHASE ERROR

LUMPED FEEDBACK CAPACITANCE AT FBIN



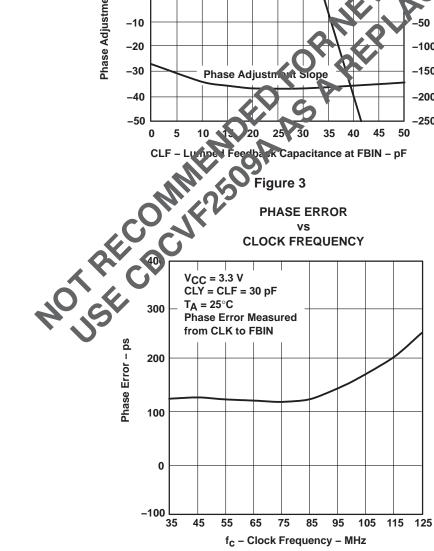


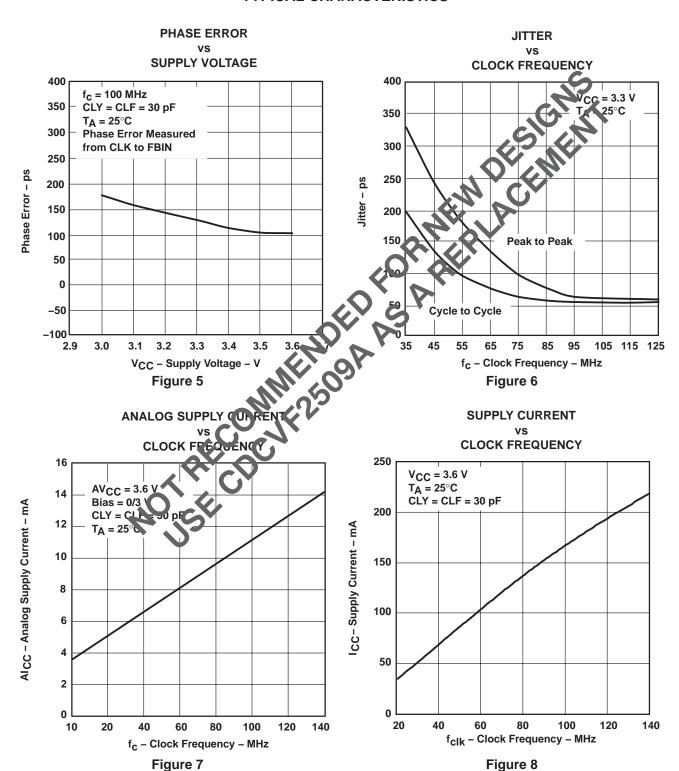
Figure 4

NOTES: A. CLY = Lumped capacitive load at Y

B. CLF = Lumped feedback capacitance at FBIN



TYPICAL CHARACTERISTICS



NOTES: A. CLY = Lumped capacitive load at Y

B. CLF = Lumped feedback capacitance at FBIN



PACKAGE OPTION ADDENDUM

www.ti.com 3-Jul-2009

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CDC2509BPW	NRND	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDC2509BPWG4	NRND	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDC2509BPWR	NRND	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDC2509BPWRG4	NRND	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION





Α	0	Dimension designed to accommodate the component width
В	0	Dimension designed to accommodate the component length
		Dimension designed to accommodate the component thickness
٧	٧	Overall width of the carrier tape
ГР	1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device		Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDC2509BPWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1





*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDC2509BPWR	TSSOP	PW	24	2000	346.0	346.0	33.0

PW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



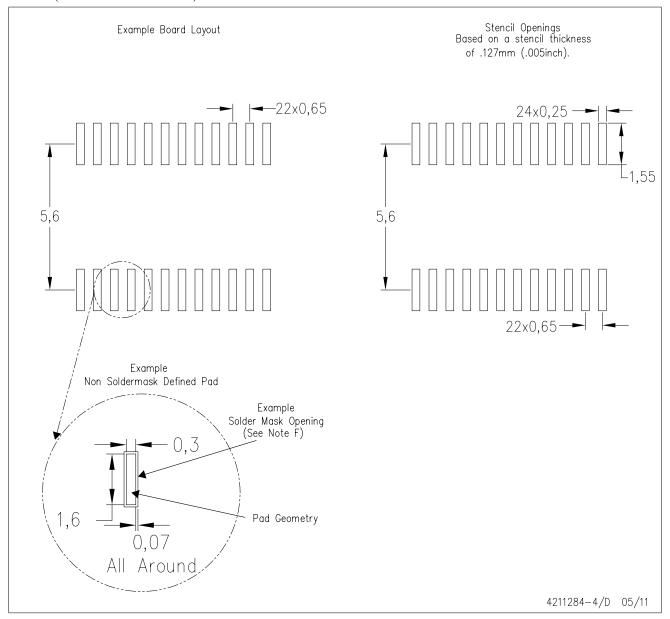
NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



PW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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