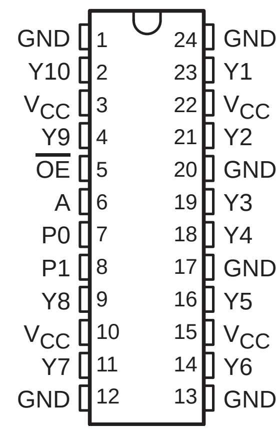
- **Controlled Baseline**
  - **One Assembly/Test Site, One Fabrication Site**
- **Extended Temperature Performance of −55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree†**
- **Low Output Skew, Low Pulse Skew for Clock-Distribution and Clock-Generation Applications**
- **Operates at 3.3-V V_{CC}**
- **LVTTL-Compatible Inputs and Outputs**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Distributes One Clock Input to 10 Outputs**

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

- **Outputs Have Internal Series Damping Resistor to Reduce Transmission Line Effects**
- **Distributed V_{CC} and Ground Pins Reduce Switching Noise**
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Shrink Small-Outline (DB) Package**

DB PACKAGE
(TOP VIEW)



description

The CDC2351 is a high-performance clock-driver circuit that distributes one input (A) to 10 outputs (Y) with minimum skew for clock distribution. The output-enable ($\overline{OE}$) input disables the outputs to a high-impedance state. Each output has an internal series damping resistor to improve signal integrity at the load. The CDC2351 operates at nominal 3.3-V V_{CC}.

The propagation delays are adjusted at the factory using the P0 and P1 pins. The factory adjustments ensure that the part-to-part skew is minimized and is kept within a specified window. Pins P0 and P1 are not intended for customer use and should be connected to GND.

The CDC2351M is characterized for operation over the full military temperature range of −55°C to 125°C.

ORDERING INFORMATION

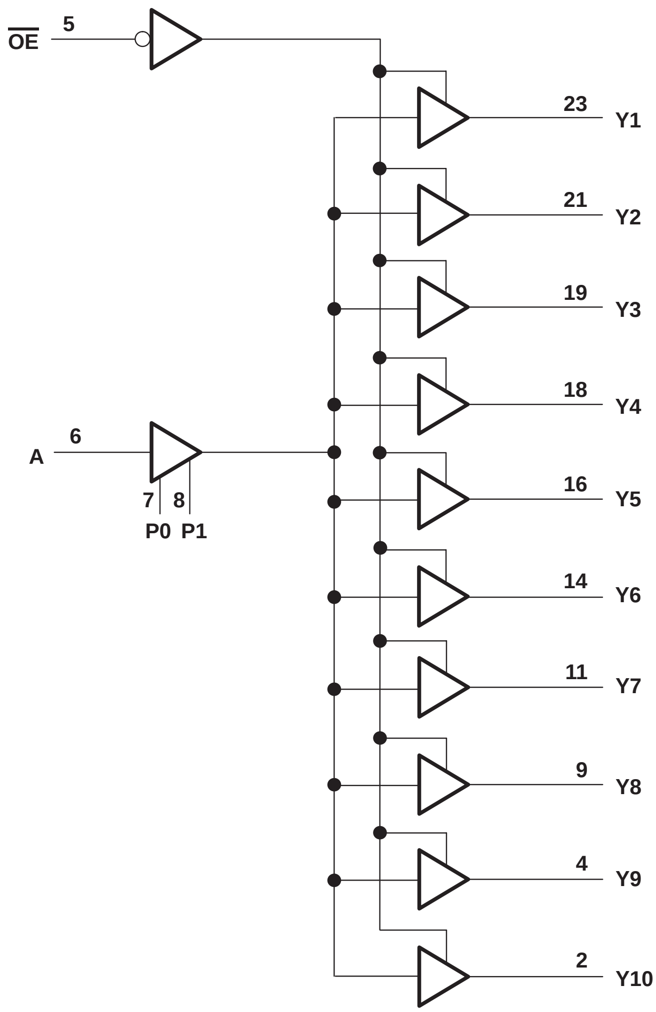
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−55°C to 125°C	SSOP − DB	Tape and Reel	CDC2351MDBREP	CK2351MEP

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS		OUTPUTS
A	$\overline{OE}$	In
L	H	Z
H	H	Z
L	L	L
H	L	H

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) . . . . −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state,
V_O (see Note 1) . . . . −0.5 V to 3.6 V
Current into any output in the low state, I_O . . . . 24 mA
Input clamp current, I_{IK} (V_I < 0) . . . . −18 mA
Output clamp current, I_{OK} (V_I < 0) . . . . −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DB package . . . . 0.65 W
Storage temperature range, T_{stg} . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, see the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		3	3.6	V
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage		0	5.5	V
I_{OH}	High-level output current			−12	mA
I_{OL}	Low-level output current			12	mA
f_{clock}	Input clock frequency			100	MHz
T_A	Operating free-air temperature	CDC2351M	−55	125	°C

NOTE 3: Unused pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS				MIN	TYP	MAX	UNIT
V_{IK}	V_{CC} = 3 V,	I_I = −18 mA					−1.2	V
V_{OH}	V_{CC} = 3 V,	I_{OH} = − 12 mA			2			V
V_{OL}	V_{CC} = 3 V,	I_{OL} = 12 mA					0.8	V
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND					±1	μA
I_O‡	V_{CC} = 3.6 V,	V_O = 2.5 V			−7		−70	mA
I_{OZ}	V_{CC} = 3.6 V,	V_{CC} = 3 V or 0					±10	μA
I_{CC}	V_{CC} = 3.6 V,	I_O = 0,	V_I = V_{CC} or GND	Outputs high			0.3	mA
				Outputs low			15	
				Outputs disabled			0.3	
C_i	V_I = V_{CC} or GND,	V_{CC} = 3.3 V,		f = 10 MHz		4		pF
C_o	V_O = V_{CC} or GND,	V_{CC} = 3.3 V,		f = 10 MHz		6		pF

‡ Not more than one output should be tested at a time and the duration of the test should not exceed one second.

switching characteristics, C_L = 50 pF (see Figure 1 and Figure 2)

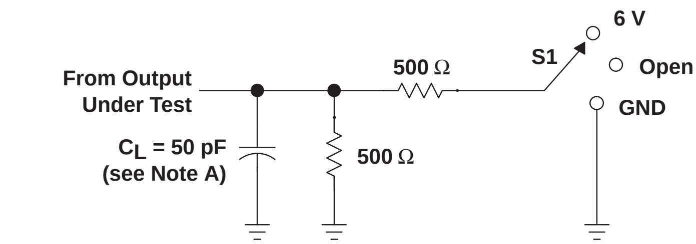
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V, T_A = 25°C			V_{CC} = 3 V to 3.6 V, T_A = −55°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A	Y	3.8	4.3	4.8	1.1	11	ns
t_{PHL}			3.6	4.1	4.6	1	9.7	
t_{PZH}	$\overline{OE}$	Y	2.4	4.9	6	1	12	ns
t_{PZL}			2.4	4.3	6	1	11.1	
t_{PHZ}	$\overline{OE}$	Y	2.2	4.4	6.3	1	11.1	ns
t_{PLZ}			2.2	4.6	6.3	1	11.5	
$t_{sk(o)}$	A	Y		0.3	0.5		2.5	ns
$t_{sk(p)}$	A	Y		0.2	0.8		3	ns
$t_{sk(pr)}$	A	Y			1			ns
t_r	A	Y					2.5	ns
t_f	A	Y					2.5	ns

switching characteristics temperature and V_{CC} coefficients over recommended operating free-air temperature and V_{CC} range (see Note 4)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
$\propto t_{PLH}(T)$	Average temperature coefficient of low-to-high propagation delay	A	Y		85†	ps/10°C
$\propto t_{PHL}(T)$	Average temperature coefficient of high-to-low propagation delay	A	Y		50†	ps/10°C
$\propto t_{PLH}(V_{CC})$	Average V_{CC} coefficient of low-to-high propagation delay	A	Y		−145‡	ps/ 100 mV
$\propto t_{PHL}(V_{CC})$	Average V_{CC} coefficient of high-to-low propagation delay	A	Y		−100‡	ps/ 100 mV

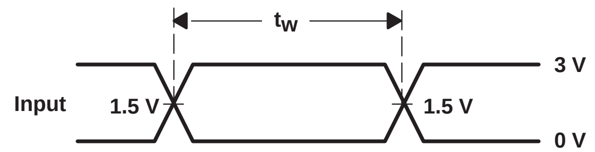
† $\propto t_{PLH}(T)$ and $\propto t_{PHL}(T)$ are virtually independent of V_{CC}.
‡ $\propto t_{PLH}(V_{CC})$ and $\propto t_{PHL}(V_{CC})$ are virtually independent of temperature.
NOTE 4: This data was extracted from characterization material and has not been tested at the factory.

PARAMETER MEASUREMENT INFORMATION

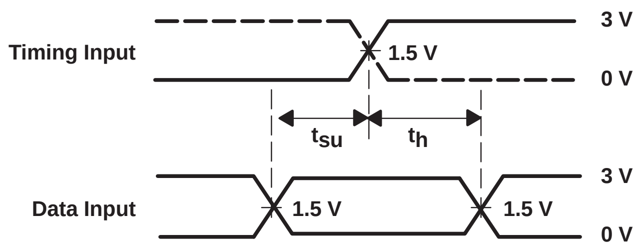


LOAD CIRCUIT

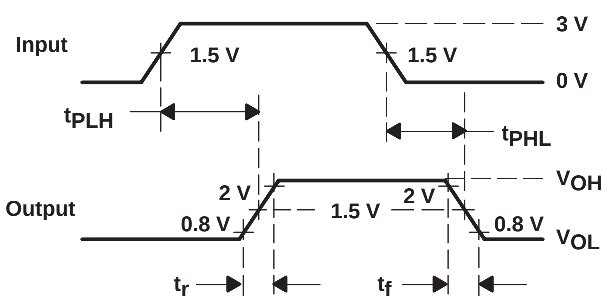
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



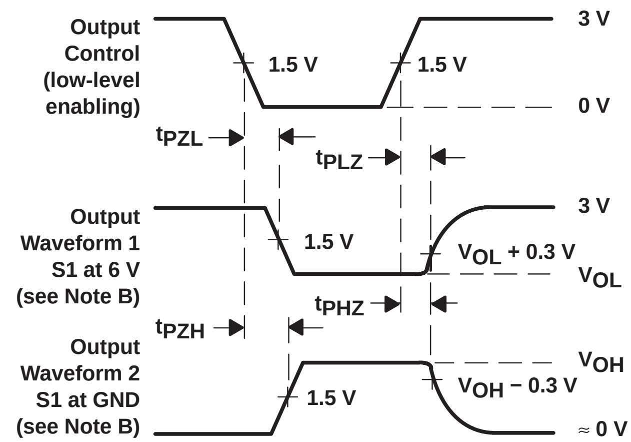
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

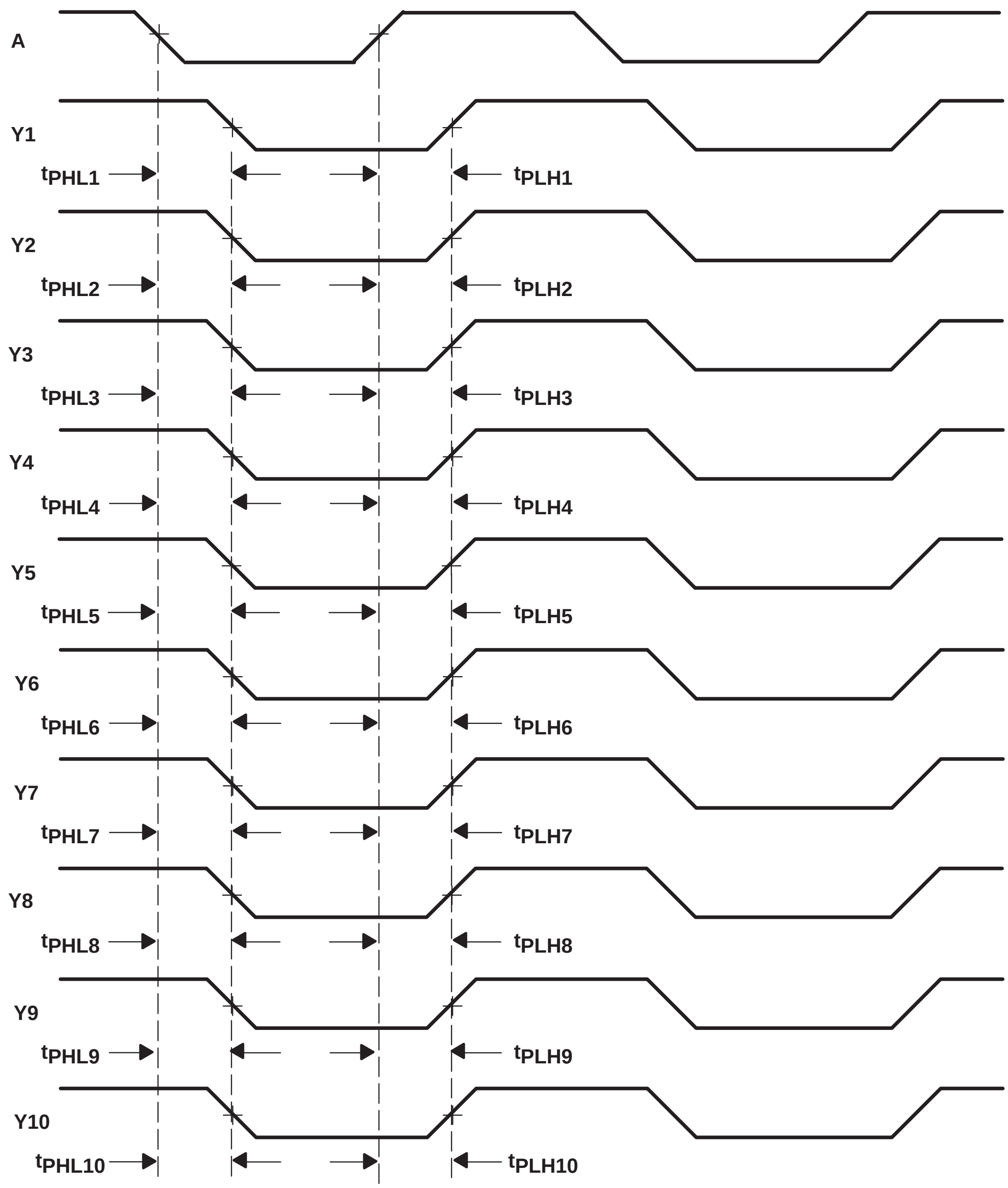


VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output skew, $t_{sk(o)}$, is calculated as the greater of:
- The difference between the fastest and slowest of t_{PLHn} (n = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10)
- The difference between the fastest and slowest of t_{PHLn} (n = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10)

B. Pulse skew, $t_{sk(p)}$, is calculated as the greater of | $t_{PLHn} - t_{PHLn}$ | (n = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10).

C. Process skew, $t_{sk(pr)}$, is calculated as the greater of:
- The difference between the fastest and slowest of t_{PLHn} (n = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10) across multiple devices under identical operating conditions.
- The difference between the fastest and slowest of t_{PHLn} (n = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10) across multiple devices under identical operating conditions.

Figure 2. Waveforms for Calculation of $t_{sk(o)}$, $t_{sk(p)}$, $t_{sk(pr)}$

IMPORTANT NOTICE