Integrated Low Profile Transceiver Module for Telekom Applications 9.6 kbit/s to 1.152 Mbit/s Data Transmission Rate

Description

The miniaturized TFBS5607 is an ideal transceiver for applications in telecommunications like mobile phones, pagers, and PDAs of all kinds. The devices are both designed for optimum performance and minimum package size.

These devices cover the latest IrDA® physical layer for Low Power SIR and MIR 1.152 Mbit/s IrDA® mode.

The transceivers is in a very low profile package, allowing to replace and upgrade a variety of common SIR devices to MIR functionality with the additional feature of variable logic voltage swing. The TFBS5607 is using the Vishay Semiconductors, IBM® and Infineon® order of the pinning.

The new features

The devices are modifications of the TFDU5107 devices. An additional new feature as in TFDU5107 is the adjustable logic voltage $V_{ddlogic}$ swing. It can be set externally between 1.5 V and 5.5 V.

The device covers the supply voltage range **from 5.5 V down to 2.7 V** and with its **low current consumption** it is optimum suited for battery powered applications. Double eye safety protection by pulse duration and current limitation is integrated. The device is defined to operate over an extended low power IrDA range close to 1 m. A custom modification of current control for MIR low power standard is available on request.

Features

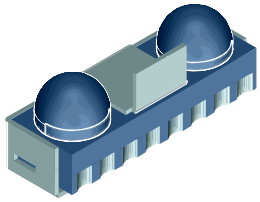
- Package:
  TFBS5607 Vishay Legacy Pinning Order
- Compatible to IrDA Low Power Standard (MIR and SIR with Lowest Current Consumption)
- Wide Supply Voltage Range (2.7 V to 5.5 V)
- Logic Input and Output Voltage 1.5 V to 5.5 V
- Tri – State – Receiver Output with weak pull-up efficient in shut down mode
- Lowest Power Consumption, typically 500 µA (900 µA max.) in Receive Mode, <1 µA in Shutdown Mode
- Fewest External Components
- Vishay's well known High EMI Immunity
- Eye Safety Protection Integrated

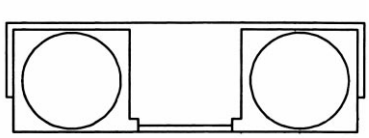
Applications

- Mobile Phones, Pagers, Hand–held Battery Operated Equipment
- Computers (WinCE, PalmPC, PDAs)
- Digital Still and Video Cameras
- Extended IR Adapters
- Medical and Industrial Data Collection

Packages

TFBS5607





Ordering Information

Part Number	Qty / Reel	Description
TFBS5607–TR3	2500 pcs	

Functional Block Diagram

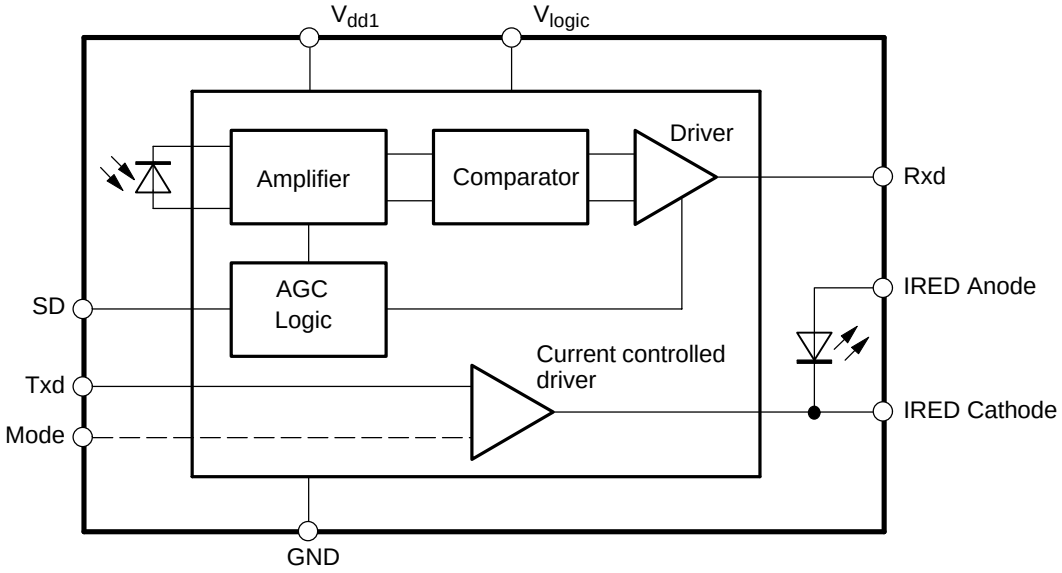


Figure 1. Functional Block Diagram
(mode input is for internal current selection of customized version for low power or full IrDA range)

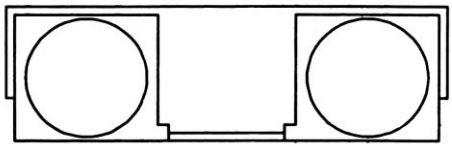
Definitions:

In the Vishay transceiver data sheets the following nomenclature is used for defining the IrDA operating modes:
SIR: 2.4 kbit/s to 115.2 kbit/s, equivalent to the basic serial infrared standard with the physical layer version IrPhy 1.0
MIR 576 kbit/s to 1152 kbit/s
FIR 4 Mbit/s
VFIR 16 Mbit/s
MIR and FIR were implemented with IrPhy 1.1, followed by IrPhy 1.2, adding the SIR Low Power Standard. IrPhy 1.3 extended the Low Power Option to MIR and FIR and VFIR was added with IrPhy 1.4. A new version of the standard in any obsoletes the former version.

Pin Description

Pin TFBS5607	Function	Description	I/O	Active
1	IRED Anode	IRED Anode to be externally connected to V_{CC} through a current control resistor. This pin is allowed to be supplied from an uncontrolled power supply separated from the controlled V_{CC} supply.		
2	IRED Cathode	IRED Cathode, internally connected to driver transistor		
3	Txd	Transmit Data Input	I	HIGH
4	Rxd	Received Data Output, push–pull CMOS driver output capable of driving a standard CMOS or TTL load. No external pull–up or pull–down resistor is required. Pin is connected to V_{logic} with a weak pull-up (500 kΩ) when device is in shutdown mode. Rxd output is quiet during transmission.	O	LOW
5	SD	Shutdown, **will switch the device into shutdown after a delay of 1 ms**	I	HIGH
6	Vdd	Supply Voltage		
7	V_{logic}	Defines the input and output logic swing voltage	I	
8	GND	Ground		

TFBS5607



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Pin order:
IREDA IRED C Txd Rxd SD Vdd Vlogic GND

Figure 2. Pinning

Absolute Maximum Ratings

Reference Point Ground, Pin 8, unless otherwise noted

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage Range	0 V < V_{dd2} < 6 V	V_{dd1}	–0.5		6	V
	0 V < V_{dd1} < 6 V	V_{dd2}	–0.5		6	V
	0 V < V_{dd1} < 6 V 0 V < V_{dd2} < 6 V	V_{logic}	–0.5		6	V
Input Current	all pins (IRED Anode excluded)				10	mA
Output Sink Current, Rxd	Rxd				25	mA
Rep. Pulsed IRED Current	IRED Anode, t_{on}< 20%, < 20 µs	I_{IRED}(RP)			500	mA
Average IRED Current		I_{IRED}(DC)			125	mA
Power Dissipation		P_{tot}			450	mW
Junction Temperature		T_J			125	°C
Ambient Temperature Range (Operating)		T_{amb}	–25		85	°C
Storage Temperature Range		T_{stg}	–25		85	°C
Soldering Temperature	t = 20 s @215°C			215	240	°C
Transmitter Data and Shutdown Input Voltage	2.7 V < V_{dd1} < 5.5 V	V_{Txd}, V_{SD}	–0.5		6	V
Receiver Data Output Voltage		V_{Rxd}	–0.5		V_{logic}+0.5	V
Virtual source size	Method: (1–1/e) encircled energy	d	2.5	2.8		mm
Max. Intensity for Class 1 operation of IEC 60825 or EN60825	EN60825, 1.1.2001 Worst case IrDA pulse pattern, lab. conditions.	I_e			500*) save in all modes	mW/sr

*) The Jan. 2001 edition of the IEC825–1 or EN60825–1 gives no limitation below the IrDA standard maximum. IrDA max. limit is 500 mW/sr.
The device is protected against Txd short by an internal shut–off when the pulse duration is exceeding maximum IrDA specification value of pulse duration. In addition the max. current is limited.

Optoelectronic Characteristics

T_{amb} = 25°C, V_{dd1} = 2.4 V to 5.5 V unless otherwise noted.
Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Transceiver						
Supported Data Rates Rxd pulse duration 400 ns	Base band SIR mode		9.6		1152	kbit/s
	Base band 1.152 Mbit/s		9.6		152	kbit/s
Supply Voltage Range	specified operation	V_{dd1}	2.4		5.5	V
Supply Voltage	V_{dd2} = 2.4 V to 5.5 V	V_{dd2}	2.4		5.5	V
Supply Current receive mode	V_{dd1} = 2.4 V to 5.5 V	I_S		500	900	µA
Supply Current shutdown mode	V_{dd1} = 2.4 V to 5.5 V	I_{SSD}		0.1	1	µA
Average Supply Current *)	V_{dd1} = 2.4 V to 5.5 V	I_S		60	110	mA
Standard MIR transmit mode I_e > 100 mW/sr	above V_{dd1} = 3.3 V a serial resistor for reducing the internal power dissipation should be implemented, e.g. R_L = 2.7 Ω					
Logic Voltage Range	V_{dd2} = 2.4 V to 5.5 V	V_{logic}	1.5		5.5	V
Shutdown/ Mode clock pulse duration		t_{prog}	0.2		20	µs
Shutdown delay ”Receive off”		t_{prog}	1		1.5	ms
Shutdown delay ”Receive on”		t_{prog}	40		100	µs
Transceiver “Power on“ Settling Time	Time from switching on V_{dd1} to established specified operation			50		µs

*) Max. data is for 20% (25%) duty cycle for SIr (MIR) 1.152 Mbit/s low power mode. The typical value is given for the case of normal operation with statistical equal distribution of “0” and “1” states.

Optoelectronic Characteristics

T_{amb} = 25°C, V_{dd1} = 2.4 V to 5.5 V unless otherwise noted.
Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Receiver						
Min. Detection Threshold Irradiance SIR 9.6 kbit/s to 1.152 Mbit/s *)	$\|\alpha\| \le 15°$ V_{dd1} = 2.4 V to 5.5 V	$E_{e,\,min}$		40	80	mW/m^2
Min. Detection Threshold Irradiance SIR 576 kbit/s to 1.152 Mbit/s *)	$\|\alpha\| \le 15°$ V_{dd1} = 2.4 V to 5.5 V	$E_{e,\,min}$		70	150	mW/m^2
Maximum Detection Threshold Irradiance	$\|\alpha\| \le 90°$ V_{dd1} = 3 V	$E_{e,\,max}$	8000	15000		W/m^2
	$\|\alpha\| \le 90°$ V_{dd1} = 5 V	$E_{e,\,max}$		5000		W/m^2
Logic Low Receiver Input Irradiance		$E_{e,max,low}$	4			mW/m^2
Output Voltage Rxd	active C = 15 pF, R = 2.2 kΩ	V_{OL}		0.5	0.8	V
	non active C = 15 pF, R = 2.2 kΩ	V_{OH}	V_{dd1}–0.5			V
Output Current Rxd V_{OL} < 0.8 V					4	mA
Rise Time @Load C = 15 pF	1.5 V ≤ V_{logic} < 1.8 V	t_r		30		ns
Fall Time @Load C = 15 pF	1.5 V ≤ V_{logic} < 1.8 V	t_f		30		ns
Rise Time @Load: C = 15 pF, R = 2.2 kΩ	1.8 V ≤ V_{logic} < 5.5 V	t_r	20	25	70	ns
Fall Time @Load: C = 15 pF, R = 2.2 kΩ	1.8 V ≤ V_{logic} < 5.5 V	t_f	20	25	70	ns
Rxd Signal Electrical Output Pulse Width	1.5 V ≤ V_{logic} < 5.5 V	t_p	250	400	550	ns
Latency	MIR mode	t_L		50	200	µs

*) Rxd output pulse duration 400 ns

Optoelectronic Characteristics

T_{amb} = 25 °C, V_{dd1} = 2.4 V to 5.5 V unless otherwise noted.
Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Transmitter						
Logic CMOS High/Low Decision Threshold		V_{IL}(Txd)		1/2 x V_{logic}		V
Logic Low Transmitter Input Voltage		V_{IL}(Txd)	0		0.2 x V_{logic}	V
Logic High Transmitter Input Voltage	1.5 V < V_{logic} < 5.5 V	V_{IH}(Txd)	0.8 x V_{logic}		V_{logic} + 0.5	V
Output Radiant Intensity, $\|\alpha\| \leq 15°$	V_{dd2} = 3 V	I_e	40	90		mW/sr
Controlled IRED drive peak current *)	V_{dd1} = 2.7 V to 5.5 V	I_{IRED}		450		mA
Maximum Output Pulse width (eye safety protection)	P_{WI} > 23 µs	P_{WOmin}	23		80	µs
Optical Pulse width	P_{WI} > 1.6 µs	P_{WO}	1.45		1.75	µs
	P_{WI} > 217 ns	P_{WO}	210		226	ns
Optical Rise/Falltime		t_r, t_f			40	ns
Peak Wavelength of Emission		λ_p	850		900	nm
Spectral Optical Radiation Bandwidth		$\Delta\lambda$		40		nm
Output Radiant Intensity	Txd logic low level	I_e			0.04	µW/sr
Overshoot, Optical					25	%
Rising Edge Peak to Peak Jitter		t_j			0.2	µs

*) The current through the IRED can be reduced and defined by an external resistor, the internal current limitation is set to 450 mA peak, nominal. For operating above V_{IRED} = 4 V an external resistor is to be used for internal power dissipation reduction

Identification

The identification of the device can be recalled by setting the SD active followed by activating Txd for a short period. With the low going edge of Txd a single pulse is generated at Rxd.
The SD is indendet to activate the shutdown function after a delay of 1 ms. Therefore the full sequence should be run with that 1 ms time limitation,
see drawing.

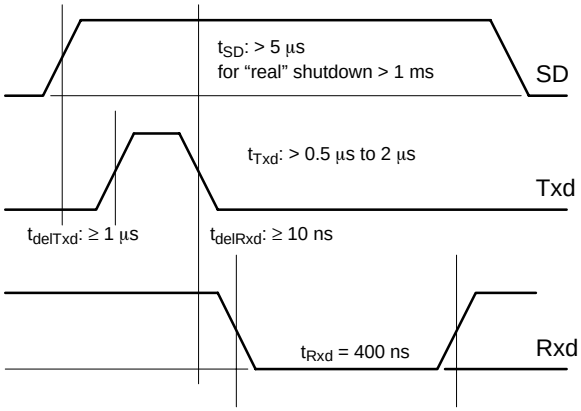


Figure 3. Timing for self identification

Current Derating Diagram

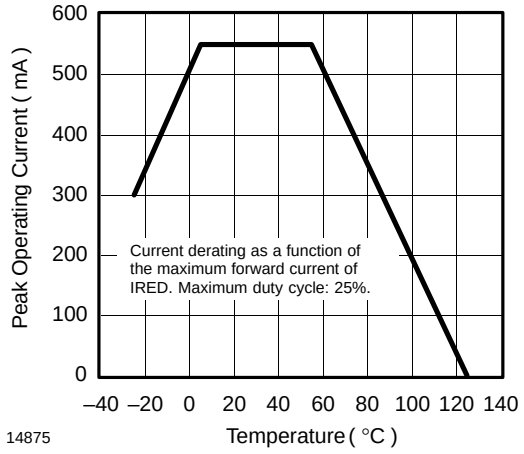


Figure 4. Current Derating as a Function of Ambient Temperature and Duty Cycle, see Absolute Maximum Ratings

Recommended Solder Profile

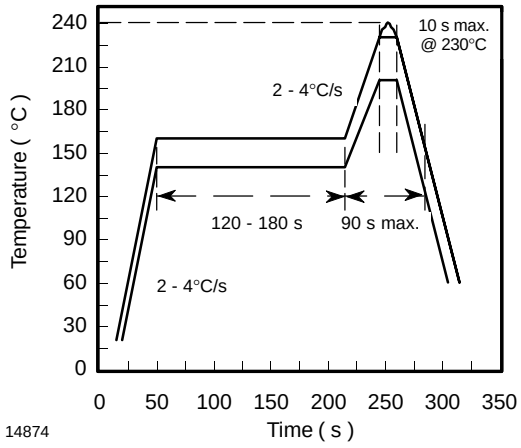


Figure 5. Recommended Solder Profile

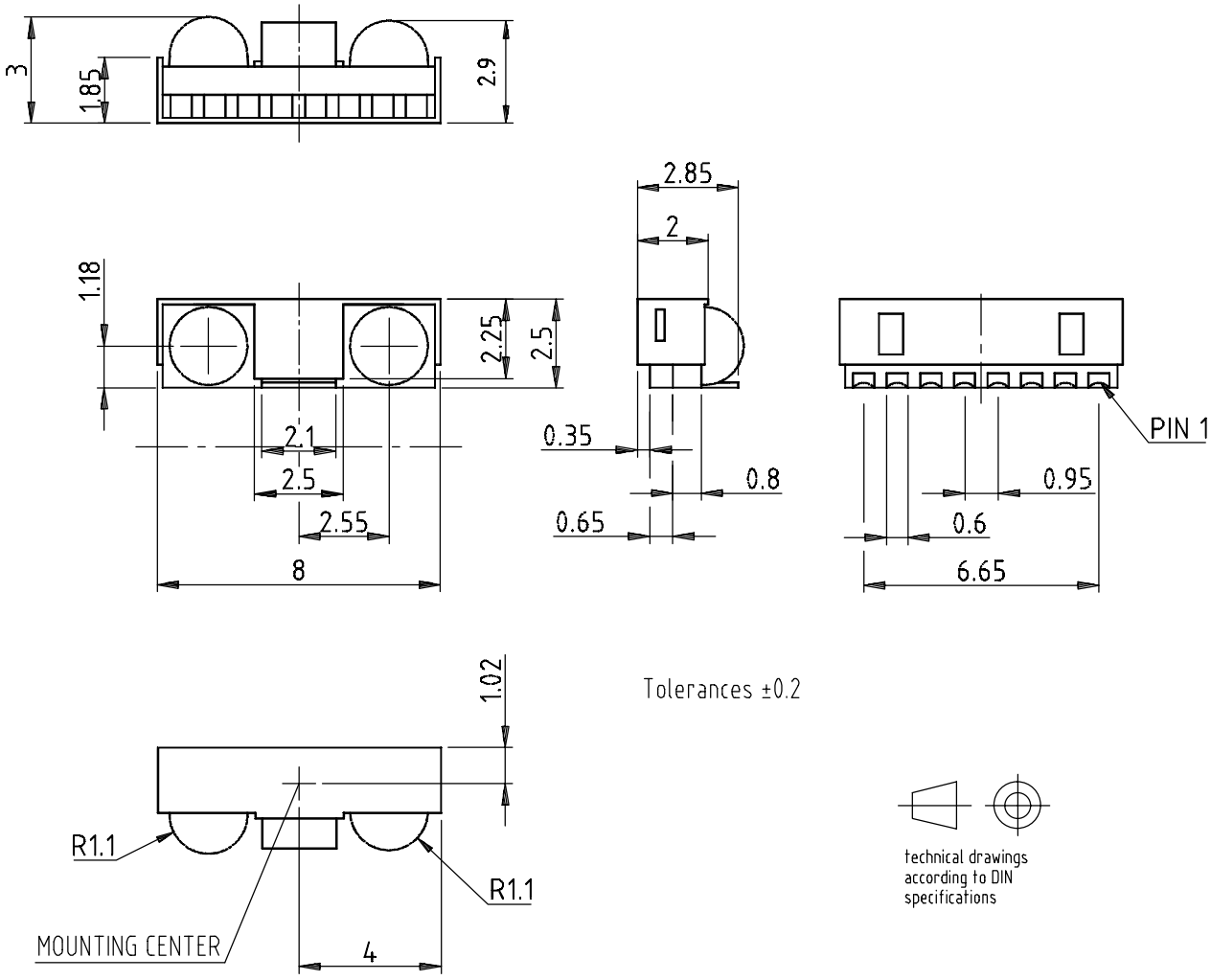
V_{logic} Setting

The logic voltage swing is set by applying an external voltage to the V_{logic} pin.

Table 1. Truth table

Inputs			Outputs	
SD	Txd	Optical input Irradiance mW/ m^2	Rxd	LED drive current resulting intensity I_e in mW/ sr
high < 1 ms	pulse	x	low going Txd triggers monostable to edit a 400 ns (nominal) low pulse	0
high > 1 ms	x	x	floating (500 kΩ to V_{dd})	0
low	high	x	high	> 40
low	high > 80 µs	x	high	0
low	low	< 4	high	0
low	low	≥ 40	low, edge triggered pulse of 400 ns durating	0

TFBS5607 (Mechanical Dimensions)



Drawing-No.: 6.550-5226.01-4
Issue: 1; 29.09.00

Dimensions in mm

16503

Pad Layout

The leads of the device should be soldered in the center position of the pads.

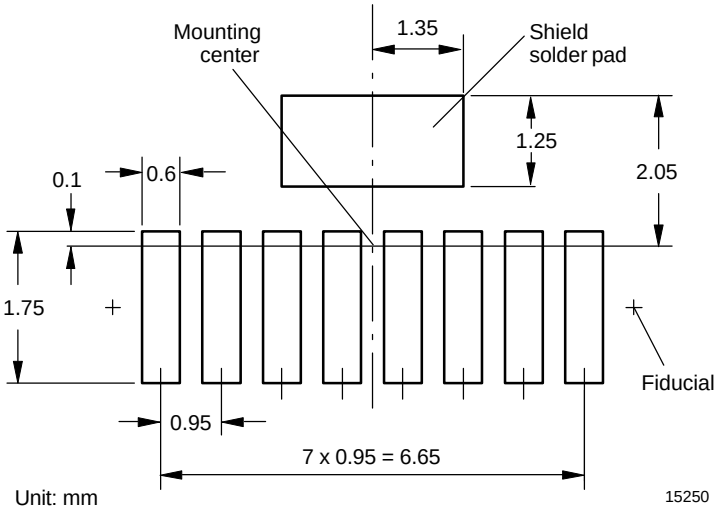


Figure 6. Recommended Land Pattern

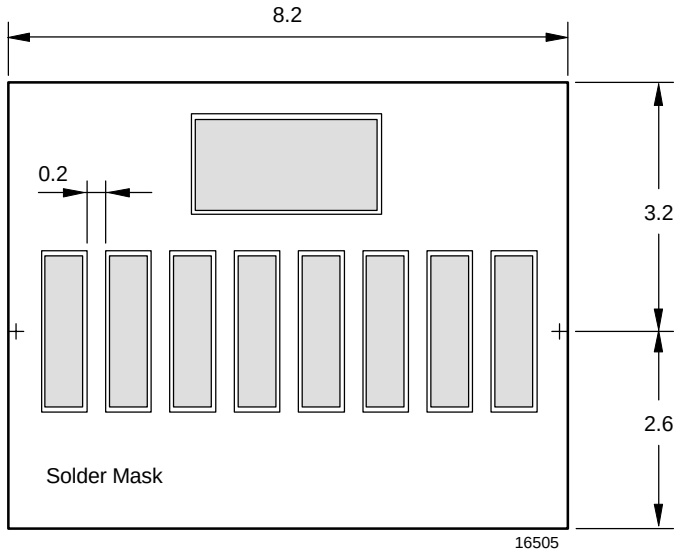
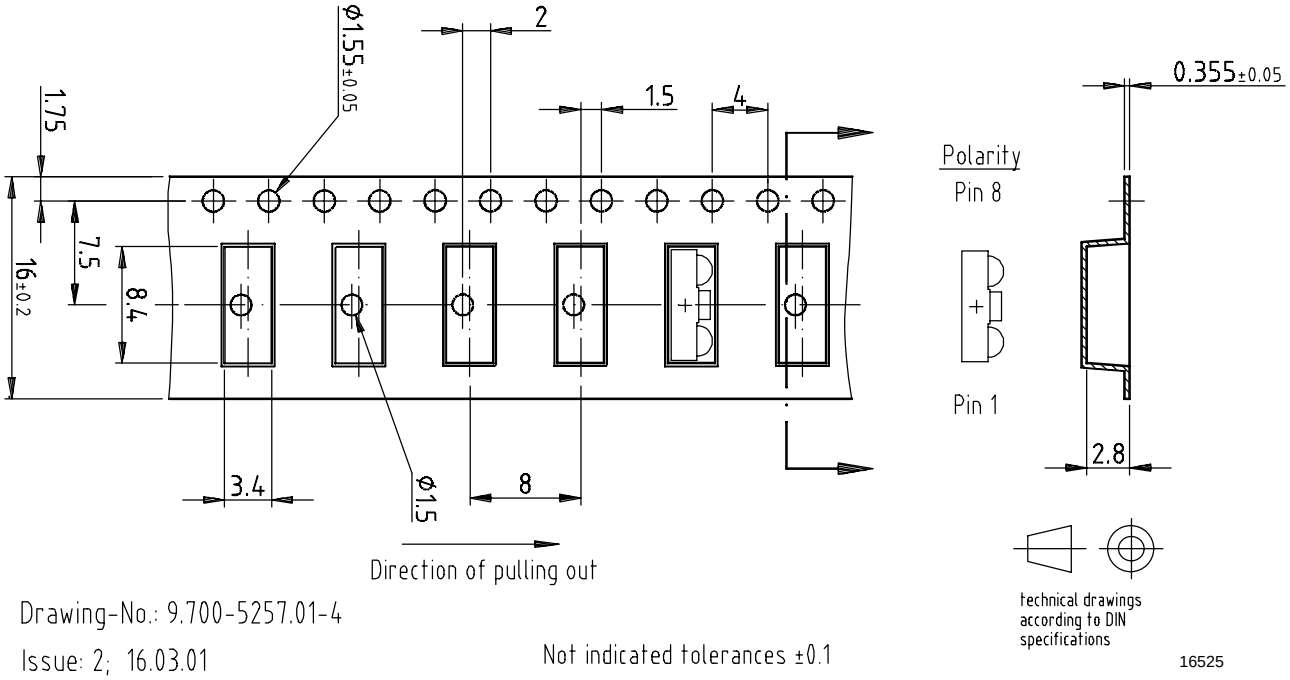


Figure 7. Adjacent Land Keep–out and Solder Mask Areas

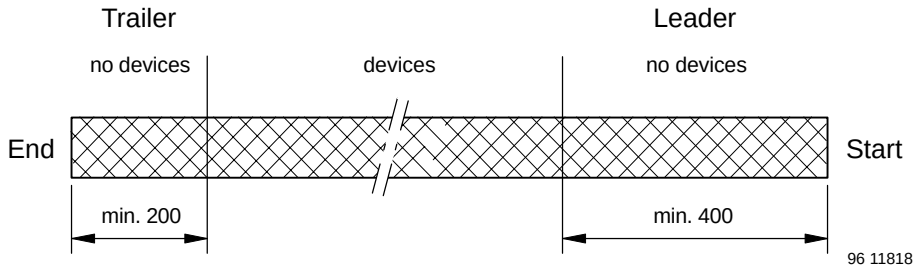
Tape and Reel Dimensions



Drawing-No.: 9.700-5257.01-4
Issue: 2; 16.03.01

Not indicated tolerances ±0.1

16525



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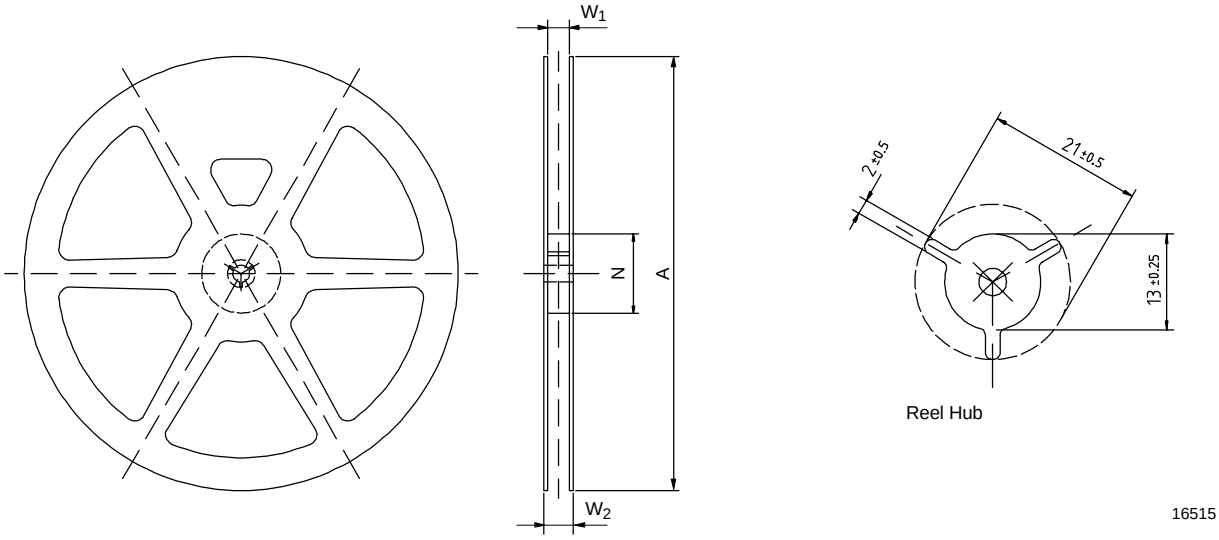

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Version	Tape Width	A	N	W_1	$W_{2\ max}$
B	16	330 ± 1	60 + 2.5	16.4 + 2	22.4

Appendix

Application Hints

Recommended Circuit Diagram TFBS5607

The TFBS5607 doesn't need any external components when operated at a "clean" power supply. In a more noisy ambient it is recommended to add a combination of a resistor and capacitor (R1, C1, C2) for noise suppression as shown in the figure below. A combination of a electrolytic for the low frequency range and a ceramic capacitor for suppressing the high frequency disturbance will be most effective. The capacitor C3 is only necessary when inductive wiring is used or the power supply cannot deliver the operating peak pulse current. However, a low impedance layout is the better and more cost efficient solution.

The inputs TXD and SD are high impedance CMOS inputs. Therefore, the lines from the I/O to those inputs should be carefully designed not to pick up ambient noise. If long lines are used, loads at the Txd input of the TFBS5607 and at the Rxd input of the controller (!) are recommended. At the IRED Anode voltage supply line an additional capacitor might be necessary when inductive wiring is used. For adjusting the intensity depending on the application, a serial resistor in the Vcc2 supply to the IRED Anode pin can be used.

Shut Down

To shut down the TFBS5600 into a standby mode the SD pin has to be set active. After a delay of < 1 ms it will switch to the standby mode.

Latency

The receiver is in specified conditions after the defined latency. In a UART related application after that time (typically 50 µs) the receiver buffer of the UART must be cleared. Therefore, the transceiver has to wait at least the specified latency after receiving the last bit before starting the transmission to be sure that the corresponding receiver is in a defined state.

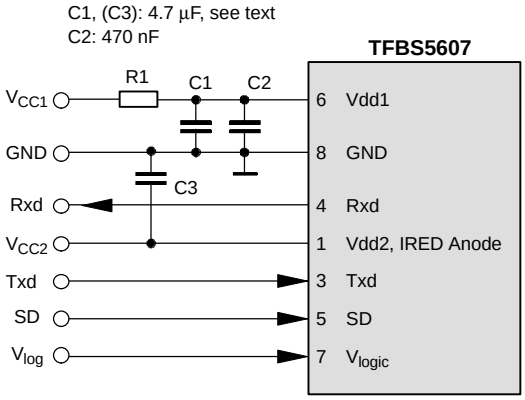

Figure 8. Recommended Application Circuit

Table 2. Recommended Application Circuit Components

Component	Recommended Value	Vishay Part Number
C1, C3	4.7 µF, 16 V	293D 475X9 016B 2T
C2	0.47 µF, Ceramic	VJ 1206 Y 104 J XXMT
R1	47 Ω, 0.125 W	CRCW–1206–47R0–F–RT1

Revision History:

A1.2, 18/02/2002: Final new revision

A1.3, 17/07/2002: Typos corrected, operating voltage range adjusted to 2.7 V to 5.5 V, wavelength range of transmitter adapted to full IrDA® range.

Ozone Depleting Substances Policy Statement

It is the policy of **Vishay Semiconductor GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

Vishay Semiconductor GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

Vishay Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

Vishay Semiconductor GmbH, P.O.B. 3535, D-74025 Heilbronn, Germany
Telephone: 49 (0)7131 67 2831, Fax number: 49 (0)7131 67 2423

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