USB332x

Industry's Smallest Hi-Speed USB Transceiver with 1.8V ULPI Interface

PRODUCT FEATURES

Data Brief

- Integrated ESD protection circuits
  - Up to ±15kV IEC Air Discharge without external devices
- Over-Voltage Protection circuit (OVP) protects the VBUS pin from continuous DC voltages up to 30V
- Integrated USB Switch
  - No degradation of Hi-Speed electrical characteristics
  - Allows single USB port of connection by providing switching function for:
    - Battery charging
    - Stereo and mono/mic audio
    - USB Full-Speed/Low-Speed data
- flexPWR™ Technology
  - Low current design ideal for battery powered applications
  - "Sleep" mode tri-states all ULPI pins and places the part in a low current state
  - 1.8V IO Voltage (±10%)
- Integrated battery to 3.3V LDO regulator
  - 2.2uF bypass capacitor
  - 100mV dropout voltage
- "Wrapper-less" design for optimal timing performance and design ease
  - Low Latency Hi-Speed Receiver (43 Hi-Speed clocks Max) allows use of legacy UTMI Links with a ULPI bridge
- External Reference Clock operation
  - 0 to 3.6V input drive tolerant
  - Able to accept "noisy" clock sources as reference to internal, low-jitter PLL
  - Frequencies: 12, 13, 19.2, 24, 26, 27, 38.4, 52 or 60MHz
- Smart detection circuits allow identification of USB charger, headset, or data cable insertion
- Includes full support for the optional On-The-Go (OTG) protocol detailed in the On-The-Go Supplement Revision 1.3 specification
- Supports the OTG Host Negotiation Protocol (HNP) and Session Request Protocol (SRP)
- UART mode for non-USB serial data transfers
- Internal 5V cable short-circuit protection of ID, DP and DM lines to VBUS or ground
- Industrial Operating Temperature -40°C to +85°C
- 25 ball WLCSP lead-free RoHS compliant package; (1.95 x 1.95 x 0.53mm height)

Applications

The USB332x is targeted for any application where a Hi-Speed USB connection is desired and when board space, power, and interface pins must be minimized.

The USB332x is well suited for:

- Cell Phones
- PDAs
- MP3 Players
- GPS Personal Navigation Devices
- Datacards
- Scanners
- External Hard Drives
- Digital Still and Video Cameras
- Portable Media Players
- Entertainment Devices
- Printers
- HDTVs
- Set Top Boxes/DVR/PVR
- Video Record/Playback Systems
- IP and Video Phones
- Gaming Consoles
- POS Terminals

ORDER NUMBER(S):

ORDER NUMBER	REFCLK FREQUENCY (Note 1)	PACKAGE TYPE	REEL SIZE
USB3321C-GL-TR	26MHz	25 Ball, WLCSP Lead-Free RoHS Compliant Package (tape and reel)	3000 pieces
USB3322C-GL-TR	12MHz		
USB3324C-GL-TR	52MHz		
USB3325C-GL-TR	24MHz		
USB3326C-GL-TR	19.2MHz		
USB3327C-GL-TR	27MHz		
USB3328C-GL-TR	38.4MHz		
USB3329C-GL-TR	13MHz		

Note 1 All versions support ULPI Clock In Mode (60MHz input at REFCLK).

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General Description

SMSC's USB332x is a family of Hi-Speed USB 2.0 Transceivers that provides a physical layer (PHY) solution well-suited for portable electronic devices. Both commercial and industrial temperature applications are supported.

Each model in the USB332x family may use a 60MHz reference clock, or the model-number specific reference clock shown in ORDER NUMBER(S): on page 2.

Several advanced features make the USB332x the transceiver of choice by reducing both electrical bill of material (eBOM) part count and printed circuit board (PCB) area. Outstanding ESD robustness eliminates the need for external ESD protection devices in typical applications. The internal Over-Voltage Protection circuit (OVP) protects the USB332x from voltages up to 30V. By using a reference clock from the Link, the USB332x removes the cost of a dedicated crystal reference from the design. And the integrated USB switch enables unique product features with a single USB port of connection.

The USB332x meets all of the electrical requirements to be used as a Hi-Speed USB Host, Device, or an On-the-Go (OTG) transceiver. In addition to the supporting USB signaling, the USB332x also provides USB UART mode and USB Audio mode.

USB332x uses the industry standard UTMI+ Low Pin Interface (ULPI) to connect the USB PHY to the Link. ULPI uses a method of in-band signaling and status byte transfers between the Link and PHY to facilitate a USB session with only 12 pins.

The USB332x uses SMSC's "wrapper-less" technology to implement the ULPI interface. This "wrapper-less" technology allows the PHY to achieve a low latency transmit and receive time. SMSC's low latency transceiver allows an existing UTMI Link to be reused by adding a UTMI to ULPI bridge. By adding a bridge to the ASIC the existing and proven UTMI Link IP can be reused.

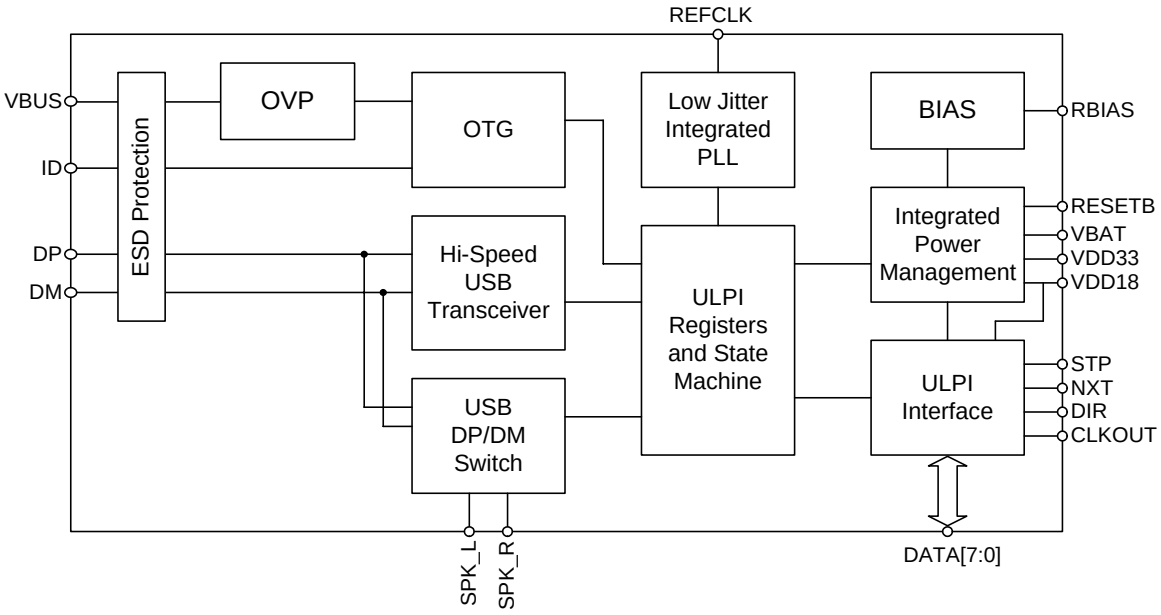


Figure 1 USB332x Block Diagram

The USB332x includes an integrated 3.3V LDO regulator that may optionally be used to generate 3.3V from power applied at the **VBAT** pin. The voltage on the **VBAT** pin can range from 3.1 to 5.5V. The regulator dropout voltage is less than 100mV which allows the PHY to continue USB signaling when the voltage on **VBAT** drops to 3.1V. The USB transceiver will continue to operate at lower voltages, although some parameters may be outside the limits of the USB specifications. If the user would like to provide a 3.3V supply to the USB332x, the **VBAT** and **VDD33** pins should be connected together.

The USB332x also includes integrated pull-up resistors that can be used for detecting the attachment of a USB Charger. By sensing the attachment to a USB Charger, a product using the USB332x can charge its battery at more than the 500mA allowed when charging from a USB Host.

In USB UART mode, the USB332x **DP** and **DM** pins are redefined to enable pass-through of asynchronous serial data. The USB332x can only enter UART mode when the user programs the part into this mode.

In USB audio mode, a switch connects the **DP** pin to the **SPK_R** pin, and another switch connects he **DM** pin to the **SPK_L** pin. The USB332x can be configured to enter USB audio mode. In addition, these switches are on when the **RESETB** pin of the USB332x is asserted. The USB audio mode enables audio signalling from a single USB port of connection, and the switches may also be used to connect Full Speed USB from another PHY onto the USB cable.

USB332x Pin Locations and Descriptions

Package Diagram with Ball Locations

The illustration below is viewed from the top of the package.

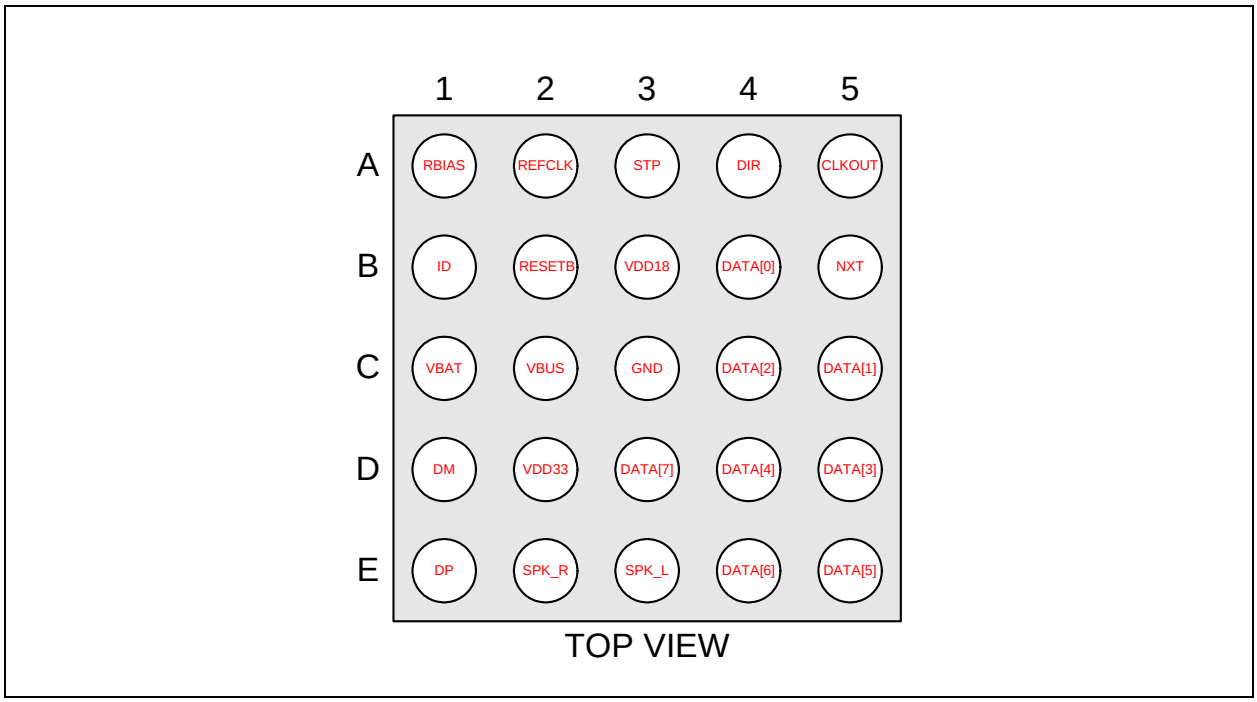


Figure 2 USB332x Ball Locations - Top View

Ball Definitions

The following table details the ball definitions for the figure above.

Table 1 USB332x Pin Description

BALL	NAME	DIRECTION/ TYPE	ACTIVE LEVEL	DESCRIPTION
B1	**ID**	Input, Analog	N/A	**ID** pin of the USB cable. For applications not using ID this pin can be connected to **VDD33**. For an A-Device **ID** is grounded. For a B-Device **ID** is floated.
C2	**VBUS**	I/O, Analog	N/A	This pin connects to an external resistor (R_{VBUS}) connected to the VBUS pin of the USB cable. This pin is used for the VBUS comparator inputs and for VBUS pulsing during session request protocol.
C1	**VBAT**	Power	N/A	Regulator input. The regulator supply can be from 5.5V to 3.1V.

Table 1 USB332x Pin Description (continued)

BALL	NAME	DIRECTION/ TYPE	ACTIVE LEVEL	DESCRIPTION
D2	**VDD33**	Power	N/A	3.3V Regulator Output. A 2.2uF (<1 ohm ESR) bypass capacitor to ground is required for regulator stability. The bypass capacitor should be placed as close as possible to the USB332x.
D1	**DM**	I/O, Analog	N/A	D- pin of the USB cable.
E1	**DP**	I/O, Analog	N/A	D+ pin of the USB cable.
E2	**SPK_R**	I/O, Analog	N/A	USB switch in/out for DP signals
E3	**SPK_L**	I/O, Analog	N/A	USB switch in/out for DM signals
D3	**DATA[7]**	I/O, CMOS	N/A	ULPI bi-directional data bus. **DATA[7]** is the MSB.
E4	**DATA[6]**	I/O, CMOS	N/A	ULPI bi-directional data bus.
E5	**DATA[5]**	I/O, CMOS	N/A	ULPI bi-directional data bus.
D4	**DATA[4]**	I/O, CMOS	N/A	ULPI bi-directional data bus.
A5	**CLKOUT**	Output, CMOS	N/A	**ULPI Clock Out Mode:** 60MHz ULPI clock output. All ULPI signals are driven synchronous to the rising edge of this clock. **ULPI Clock In Mode:** This pin is connected to VDD18 to configure 60MHz ULPI Clock IN mode.
D5	**DATA[3]**	I/O, CMOS	N/A	ULPI bi-directional data bus.
C4	**DATA[2]**	I/O, CMOS	N/A	ULPI bi-directional data bus.
C5	**DATA[1]**	I/O, CMOS	N/A	ULPI bi-directional data bus.
B4	**DATA[0]**	I/O, CMOS	N/A	ULPI bi-directional data bus. **DATA[0]** is the LSB.
B5	**NXT**	Output, CMOS	High	The PHY asserts **NXT** to throttle the data. When the Link is sending data to the PHY, **NXT** indicates when the current byte has been accepted by the PHY. The Link places the next byte on the data bus in the following clock cycle.
A4	**DIR**	Output, CMOS	N/A	Controls the direction of the data bus. When the PHY has data to transfer to the Link, it drives **DIR** high to take ownership of the bus. When the PHY has no data to transfer it drives **DIR** low and monitors the bus for commands from the Link.

Table 1 USB332x Pin Description (continued)

BALL	NAME	DIRECTION/ TYPE	ACTIVE LEVEL	DESCRIPTION
A3	**STP**	Input, CMOS	High	The Link asserts **STP** for one clock cycle to stop the data stream currently on the bus. If the Link is sending data to the PHY, **STP** indicates the last byte of data was on the bus in the previous cycle.
B3	**VDD18**	Power	N/A	External 1.8V Supply input pin. This pad needs to be bypassed with a 0.1uF capacitor to ground, placed as close as possible to the USB332x.
B2	**RESETB**	Input, CMOS,	Low	When low, the part is suspended with all ULPI outputs tri-stated. When high, the USB332x will operate as a normal ULPI device. The state of this pin may be changed asynchronously to the clock signals. When asserted for a minimum of 1 microsecond and then de-asserted, the ULPI registers are reset to their default state and all internal state machines are reset.
A2	**REFCLK**	Input, CMOS	N/A	**ULPI Clock Out Mode:** Model-specific reference clock. See ORDER NUMBER(S): on page 2. **ULPI Clock In Mode:** 60MHz ULPI clock input.
A1	**RBIAS**	Analog, CMOS	N/A	Bias Resistor pin. This pin requires an 8.06kΩ (±1%) resistor to ground, placed as close as possible to the USB332x. Nominal voltage during ULPI operation is 0.8V.
C3	**GND**	Ground	N/A	Ground.

Application Diagrams

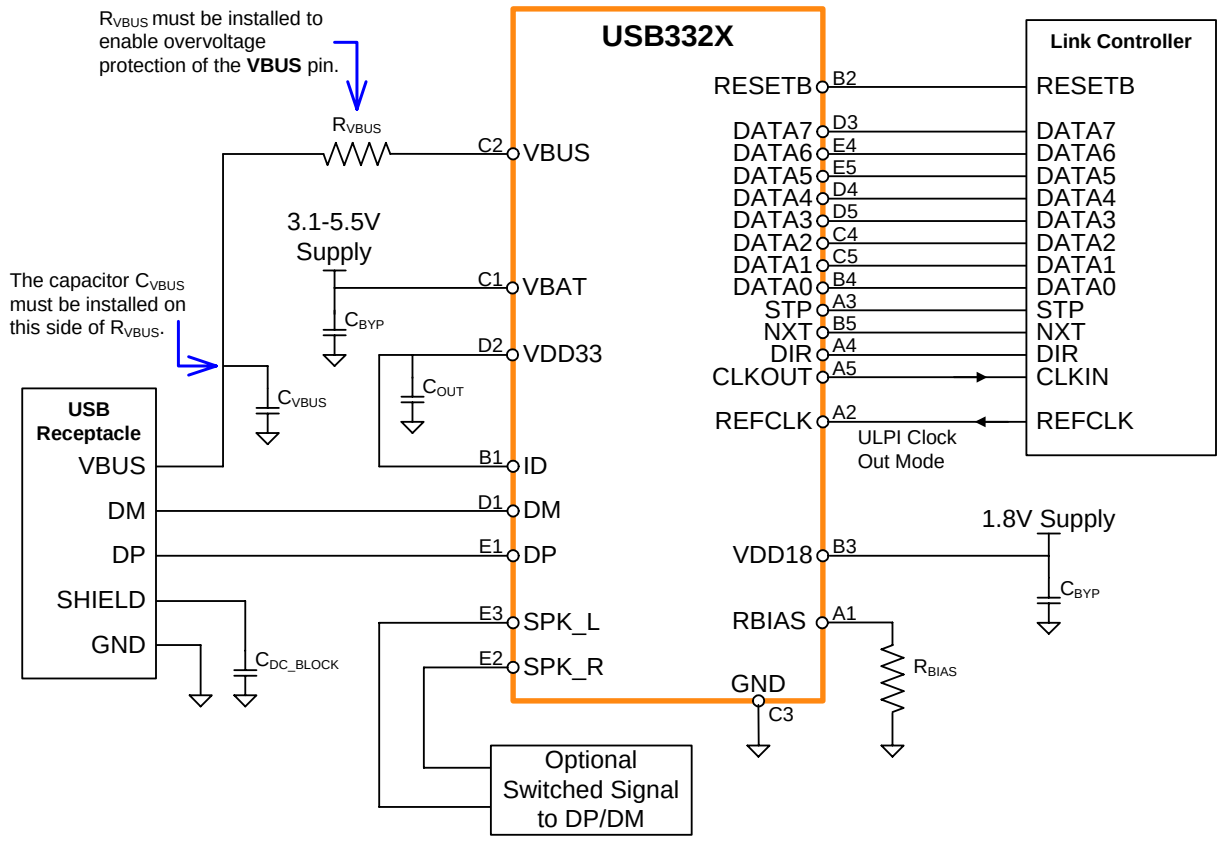


Figure 3 USB332x WLCSP Application Diagram (Device configured for ULPI Clock Out mode)

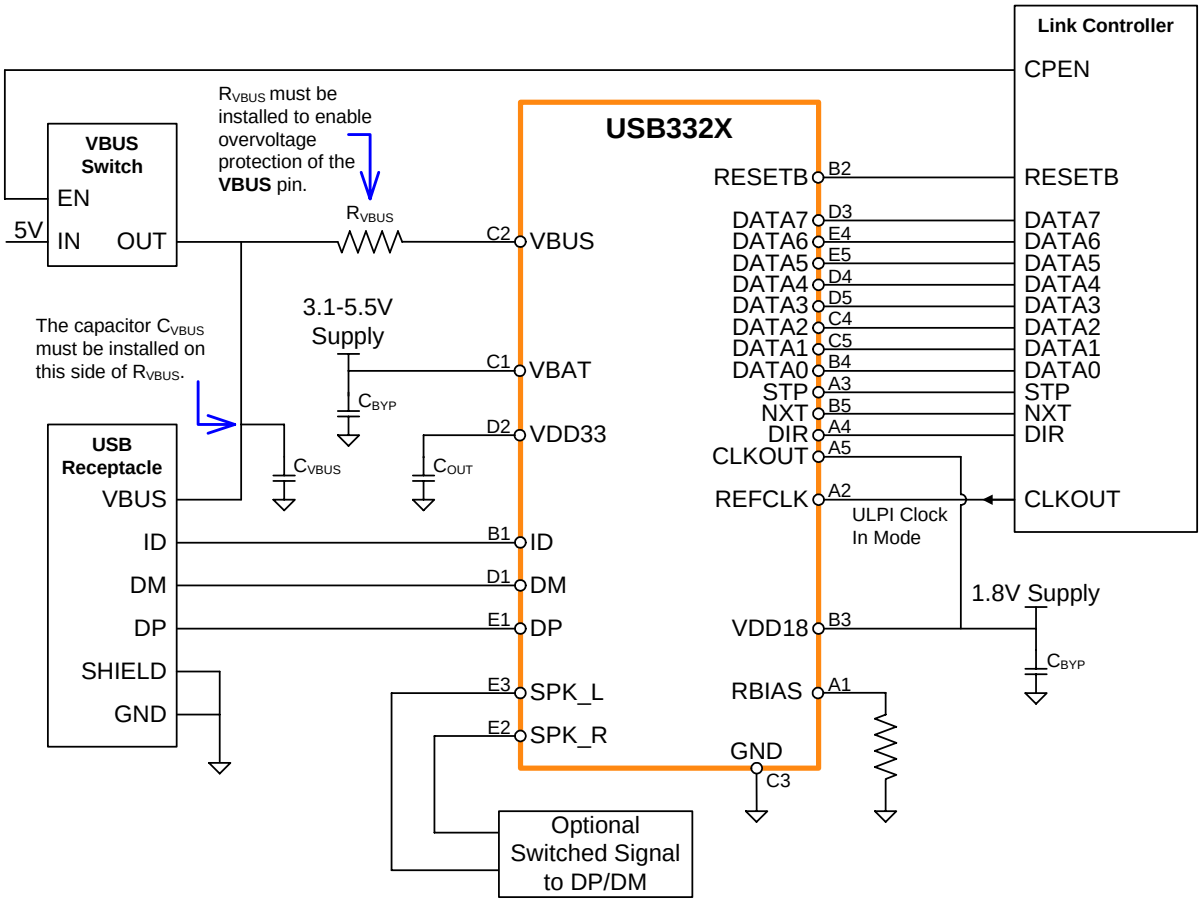
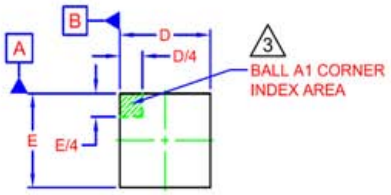
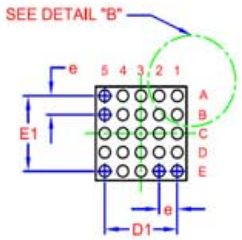


Figure 4 USB332x WLCSP Application Diagram (Host or OTG configured for ULPI Clock In mode)

Package Outline

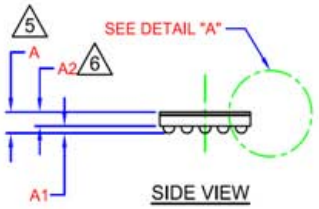


TOP VIEW

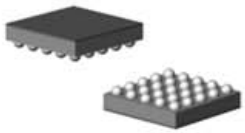


BOTTOM VIEW

COMMON DIMENSIONS					
SYMBOL	MIN	NOM	MAX	NOTE	REMARK
A	-	0.53	0.62	5	OVERALL PACKAGE HEIGHT
A1	0.16	-	0.24	-	STANDOFF
A2	-	-	0.38	6	PACKAGE THICKNESS
D/E	1.93	-	1.97	-	X/Y DIE SIZE
D1/E1	1.60 BSC			-	X/Y END BALLS DISTANCE
b	0.20	0.25	0.30	2	BALL DIAMETER
e	0.40 BSC			-	BALL PITCH
ccc	0	-	0.05	4	COPLANARITY



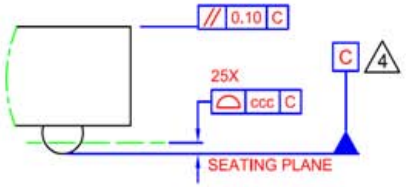
SIDE VIEW



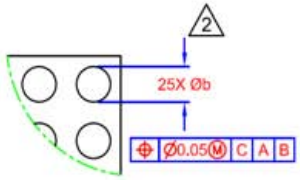
3-D VIEWS

NOTES:

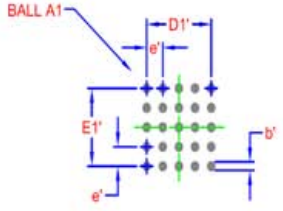
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER, PARALLEL TO PRIMARY DATUM "C".
3. THE BALL "A1" CORNER MUST BE IDENTIFIED IN THE INDICATED AREA OF THE TOP PACKAGE SURFACE.
4. PRIMARY DATUM "C" AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE CONTACT SOLDER BALLS.
5. DIMENSION "A" DOES NOT INCLUDE ATTACHED EXTERNAL FEATURES, SUCH AS HEAT SINK OR CHIP CAPACITORS.
   DIMENSION "A(MAX)" IS GIVEN FOR THE EXTREMELY THIN VARIATION OF THE PACKAGE PROFILE HEIGHT.
6. DIMENSION "A2" INCLUDES A DIE COATING THICKNESS.



DETAIL A



DETAIL B



LAND PATTERN DIMENSIONS			
SYMBOL	MIN	NOM	MAX
D1'/E1'	-	1.60	-
b'	0.15	-	0.20
e'	-	0.40	-

THE USER MAY MODIFY THE PCB LAND PATTERN DIMENSIONS, BASED ON THEIR EXPERIENCE AND/OR PROCESS CAPABILITY

RECOMMENDED PCB LAND PATTERN

Figure 5 25WLCSP, 1.95x1.95mm Body, 0.4mm Pitch