

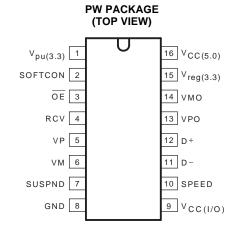
ADVANCED UNIVERSAL SERIAL BUS TRANSCEIVERS

Check for Samples: TUSB1106-Q1

FEATURES

- Qualified for Automotive Applications
- Compatible With Universal Serial Bus Specification Rev. 2.0
- Transmit and Receive Serial Data at Both Full-Speed (12-Mbit/s) and Low-Speed (1.5-Mbit/s) Data Rates
- Integrated Bypassable 5-V to 3.3-V Voltage Regulator for Powering Via USB V_{BUS}
- V_{BUS} Disconnection Indication Through V_P and V_M
- Used as USB Device Transceiver or USB Host Transceiver
- · Stable RCV Output During SE0 Condition
- Two Single-Ended Receivers With Hysteresis
- Low-Power Operation, Ideal for Portable Equipment
- Support I/O Voltage Range From 1.65 V to 3.6 V

 Available in a Thin Shrink Small-Outline Package [TSSOP (PW)]



DESCRIPTION

The TUSB1106-Q1 universal serial bus (USB) transceiver is compliant with the Universal Serial Bus Specification Rev. 2.0. This device can transmit and receive serial data at both full-speed (12-Mbit/s) and low-speed (1.5-Mbit/s) data rates. The TUSB1106-Q1 can be used as USB device transceiver or USB host transceiver.

The device allows USB application-specific ICs (ASICs) and programmable logic devices (PLDs), with power-supply voltages from 1.65 V to 3.6 V, to interface with the physical layer (PHY) of the universal serial bus. It has an integrated 5-V to 3.3-V voltage regulator for direct powering via the USB supply VBUS.

The TUSB1106-Q1 allows only differential input mode and is available in a PW package.

The TUSB1106-Q1 is ideal for portable electronic devices such as mobile phones, personal digital assistants, information appliances, and digital still cameras.

ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾ (2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING	
-40°C to 85°C	TSSOP - PW	Reel of 2000	TUSB1106IPWRQ1	TU1106I	

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

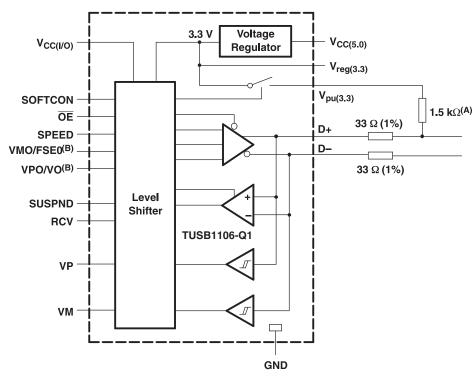
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



FUNCTIONAL BLOCK DIAGRAM



- A. Connect to D– for low-speed operation and to D+ for high-speed operation.
- B. Pin function depends on device type.

TERMINAL FUNCTIONS

TERMII	NAL		TERMINAL FUNCTIONS
NAME	NO.	I/O	DESCRIPTION
ŌĒ	3	I	Output enable (CMOS level with respect to $V_{\text{CC(I/O)}}$, active LOW). Enables the transceiver to transmit data on the USB bus input pad. Push pull, CMOS.
RCV	4	0	Differential data receiver (CMOS level with respect to $V_{CC(I/O)}$). Driven LOW when input SUSPND is HIGH. The output state of RCV is preserved and stable during an SE0 condition output pad. Push pull, 4-mA output drive, CMOS.
VP	5	0	Single-ended D+ receiver (CMOS level with respect to V). For external detection of single-ended zero (SE0), error conditions, speed of connected device. Driven HIGH when no supply voltage is connected to $V_{CC(5.0)}$ and $V_{reg(3.3)}$ output pad. Push pull, 4-mA output drive, CMOS.
VM	6	0	Single-ended D– receiver (CMOS level with respect to $V_{CC(I/O)}$). For external detection of single-ended zero (SE0), error conditions, speed of connected device. Driven HIGH when no supply voltage is connected to $V_{CC(5.0)}$ and $V_{reg(3.3)}$ output pad. Push pull, 4-mA output drive, CMOS.
SUSPND	7	1	Suspend (CMOS level with respect to $V_{CC(I/O)}$). A HIGH level enables low-power state while the USB bus is inactive and drives output RCV to a LOW-level input pad. Push pull, CMOS.
MODE		I	Mode (CMOS level with respect to $V_{\text{CC(I/O)}}$). A HIGH level enables the differential input mode (VPO, VMO), whereas a LOW level enables a single-ended input mode (VO, FSE0). See Table 5 and Table 6 input pad. Push pull, CMOS.
GND	8		Ground supply
V _{CC(I/O)}	9		Supply voltage for digital I/O pins (1.65 to 3.6 V). When $V_{CC(I/O)}$ is not connected, the D+ and D- pins are in 3-state. This supply pin is independent of $V_{CC(5.0)}$ and $V_{reg(3.3)}$ and must never exceed the $V_{reg(3.3)}$ voltage.
SPEED	10	I	Speed selection (CMOS level with respect to $V_{CC(I/O)}$). Adjusts the slew rate of differential data outputs D+ and D- according to the transmission speed. Input pad, push pull, CMOS. LOW – low speed (1.5 Mbit/s) HIGH – full speed (12 Mbit/s)
D-	11	AI/O	Negative USB data bus connection (analog, differential). For low-speed mode, connect to pin $V_{pu(3.3)}$ via a 1.5-k Ω resistor.
D+	12	AI/O	Positive USB data bus connection (analog, differential). For full-speed mode, connect to pin $V_{pu(3.3)}$ via a 1.5-k Ω resistor.
VPO/VO		I	Driver data (CMOS level with respect to V _{CC(I/O)} , Schmitt trigger). See Driving Function table.
VPO	13		Push pull, CMOS.
VMO/FSE0		I	Driver data (CMOS level with respect to V _{CC(I/O)} , Schmitt trigger). See Driving Function table.
VMO	14		Push pull, CMOS.
V _{reg(3.3)}	15		Internal regulator option. Regulated supply-voltage output (3 V to 3.6 V) during 5-V operation. A decoupling capacitor of at least 0.1 mF is required for the regulator bypass option. Used as a supply-voltage input for 3.3 V \pm 10% operation.
V _{CC(5.0)}	16		Internal regulator option. Supply-voltage input (4 V to 5.5 V). Can be connected directly to USB supply VBUS regulator bypass option. Connect to $V_{reg(3.3)}$.
V _{pu(3.3)}	1		Pullup supply voltage (3.3 V \pm 10%). Connect an external 1.5-k Ω resistor on D+ (full speed) or D– (low speed). Pin function is controlled by input SOFTCON. SOFTCON = LOW – $V_{pu(3.3)}$ floating (high impedance), ensures zero pullup current SOFTCON = HIGH – $V_{pu(3.3)}$ = 3.3 V, internally connected to $V_{reg(3.3)}$
SOFTCON	2	I	Software-controlled USB connection. A HIGH level applies 3.3 V to pin $V_{pu(3.3)}$, which is connected to an external 1.5-k Ω pullup resistor. This allows USB connect/disconnect signaling to be controlled by software input pad. Push pull, CMOS.



FUNCTIONAL DESCRIPTION

Function Selection

FUNCTION TABLE

SUSPND	OE	D+, D-	RCV	VP, VM	FUNCTION
L	L	Driving and receiving	Active	Active	Normal driving (differential receiver active)
L	Н	Receiving ⁽¹⁾	Active	Active	Receiving
Н	L	Driving	Inactive ⁽²⁾	Active	Driving during suspend (3) (differential receiver inactive)
Н	Н	High-Z ⁽¹⁾	Inactive (2)	Active	Low-power state

- 1) Signal levels on D+ and D- are determined by other USB devices and external pullup/pulldown resistors.
- (2) In suspend mode (SUSPND = HIGH) the differential receiver is inactive and output RCV is always LOW. Out of suspend (K), signaling is detected via the single-ended receivers VP and VM.
- (3) During suspend, the slew-rate control circuit of low-speed operation is disabled. The D+ and D- lines are still driven to their intended states, without slew-rate control. This is permitted because driving during suspend is used to signal remote wakeup by driving a K signal (one transition from idle to K state) for a period of 1 ms to 15 ms.

Operating Functions

Driving Function (Pin \overline{OE} = L) Using Differential Input Data Interface

\/MO	\/D0	DATA	DATA STATE		
VMO	VPO	DATA	LOW SPEED FULL SPEE	FULL SPEED	
L	L	SE0	X	Х	
Н	L	Differential logic 0	J	К	
L	Н	Differential logic 1	K	J	
Н	Н	Illegal state	Х	Х	

Table 1. Receiving Function (Pin $\overline{OE} = H$)

				DATA	STATE
D+, D-	RCV	VP ⁽¹⁾	VM ⁽¹⁾	LOW SPEED	FULL SPEED
Differential logic 0	L	L	Н	J	К
Differential logic 1	Н	Н	L	К	J
SE0	RCV*(2)	L	L	Х	Х

- VP = VM = H indicates the sharing mode (V_{CC(5.0)} and V_{reg(3.3)} are disconnected).
- (2) RCV* denotes the signal level on output RCV just before SE0 state occurs. This level is stable during the SE0 period.

Power-Supply Configurations

The TUSB1106-Q1 can be used with different power-supply configurations, which can be dynamically changed. An overview is given in Table 3.

- Normal mode Both V_{CC(I/O)} and V_{CC(5.0)} or (V_{CC(5.0)} and V_{reg(3.3)}) are connected. For 5-V operation, V_{CC(5.0)} is connected to a 5-V source (4 V to 5.5 V). The internal voltage regulator then produces 3.3 V for the USB connections. For 3.3-V operation, both V_{CC(5.0)} and V_{reg(3.3)} are connected to a 3.3-V source (3 V to 3.6 V). V_{CC(I/O)} is independently connected to a voltage source (1.65 V to 3.6 V), depending on the supply voltage of the external circuit.
- Disable mode $V_{CC(I/O)}$ is not connected, $V_{CC(5.0)}$ or $(V_{CC(5.0)}$ and $V_{reg(3.3)})$ are connected. In this mode, the internal circuits of the TUSB1106-Q1 ensure that the D+ and D- pins are in 3-state and the power consumption drops to the low-power (suspended) state level. Some hysteresis is built into the detection of $V_{CC(I/O)}$ lost.
- Sharing mode $V_{CC(I/O)}$ is connected, ($V_{CC(5.0)}$ and $V_{reg(3.3)}$) are not connected. In this mode, the D+ and D- pins are made 3-state and the TUSB1106-Q1 allows external signals of up to 3.6 V to share the D+ and D-

Submit Documentation Feedback

lines. The internal circuits of the TUSB1106-Q1 ensure that virtually no current (maximum 10 μ A) is drawn via the D+ and D– lines. The power consumption through $V_{CC(I/O)}$ drops to the low-power (suspended) state level. Both the VP and VM pins are driven HIGH to indicate this mode. Pin RCV is made LOW. Some hysteresis is built into the detection of $V_{reg(3.3)}$ lost.

Table 2. Pin States in Disable or Sharing Mode

PINS	DISABLE-MODE STATE	SHARING-MODE STATE
V _{CC(5.0)} /V _{reg(3.3)}	5-V input/3.3-V output, 3.3-V input/3.3-V input	Not present
V _{CC(I/O)}	Not present	1.65-V to 3.6-V input
V _{pu(3.3)}	High impedance (off)	High impedance (off)
D+, D-	High impedance	High impedance
VP, VM	Invalid ⁽¹⁾	Н
RCV	Invalid ⁽²⁾	L
Inputs (VO/VPO, FSE0/VMO, SPEED, SUSPND, OE, SOFTCON)	High impedance	High impedance

⁽¹⁾ High impedance or driven LOW

Table 3. Power-Supply Configuration Overview

V _{CC(5.0)} or V _{reg(3.3)}	V _{CC(I/O)}	CONFIGURATION	SPECIAL CHARACTERISTICS
Connected	Connected	Normal mode	
Connected	Not connected	Disable mode	D+, D–, and V _{pu(3.3)} are in high impedance. VP, VM, and RCV are invalid. (1)
Not connected	Connected	Sharing mode	D+, D–, and V _{pu(3.3)} are in high impedance. VP and VM are driven HIGH. RCV is driven LOW.

⁽¹⁾ High impedance or driven LOW

Power-Supply Input Options

The TUSB1106-Q1 has two power-supply input options.

- Internal regulator V_{CC(5.0)} is connected to 4 V to 5.5 V. The internal regulator is used to supply the internal circuitry with 3.3 V (nominal). V_{req(3.3)} becomes a 3.3-V output reference.
- Regulator bypass V_{CC(5.0)} and V_{reg(3.3)} are connected to the same supply. The internal regulator is bypassed and the internal circuitry is supplied directly from the V_{reg(3.3)} power supply. The voltage range is 3 V to 3.6 V to comply with the USB specification.

The supply-voltage range for each input option is specified in Table 4.

Table 4. Power-Supply Input Options

INPUT OPTION	V _{CC(5.0)}	V _{REG(3.3)}	V _{CC(I/O)}		
Internal regulator	Supply input for internal regulator (4 V to 5.5 V)	Voltage-reference output (3.3 V, 300 μA)	Supply input for digital I/O pins (1.65 V to 3.6 V)		
Regulator bypass	Connected to V _{reg(3.3)} with maximum voltage drop of 0.3 V (2.7 V to 3.6 V)	Supply input (3 V to 3.6 V)	Supply input for digital I/O pins (1.65 V to 3.6 V)		

Copyright © 2011, Texas Instruments Incorporated

⁽²⁾ High impedance or driven LOW



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC(5.0)}	Supply voltage range		-0.5	6	V
V _{I(I/O)}	Supply voltage range		-0.5	4.6	V
V _{CCreg(3.3)}	Regulated voltage range		-0.5	4.6	V
VI	DC input voltage		-0.5	V _{CC(I/O)} + 0.5	V
I _{IK}	Input clamp current	$V_I = -1.8 \text{ V to } 5.4 \text{ V}$		100	mA
T _{stq}	Storage temperature range		-40	125	°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V _{CC(5.0)}	Supply voltage, internal regulator option	5-V operation	4	5	5.5	V
V _{CCreg(3.3)}	Supply voltage, regulator bypass option	3.3-V operation	3	3.3	3.6	V
V _{CC(I/O)}	I/O supply voltage		1.65		3.6	V
V_{I}	I/O supply voltage		0		$V_{CC(I/O)}$	V
$V_{I/O}$	Input voltage on analog I/O pins (D+, D-)		0		3.6	V
T _c	Junction temperature		-40		85	°C

STATIC ELECTRICAL CHARACTERISTICS - SUPPLY PINS

over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

	PARAMETER	TEST CON	IDITIONS	MIN	TYP	MAX	UNIT
V _{reg(3.3)}	Regulated supply-voltage output	Internal regulator option, I _{load}	≤ 300 µA ⁽¹⁾ (2)	3	3.3	3.6	V
I _{CC}	Operating supply current	Full-speed transmitting and re $C_L = 50 \text{ pF}$ on D+ and D- $^{(3)}$	eceiving at 12 Mbit/s,		6	8	mA
I _{CC(I/O)}	Operating I/O supply current	Full-speed transmitting and re	eceiving at 12 Mbit/s ⁽³⁾		2.3	2.5	mA
I _{CC(idle)}	Supply current during full-speed idle and SE0	Full-speed idle: $V_{D+} > 2.7 \text{ V}, V_{D-} < 0.3 \text{ V}$ SE0: $V_{D+} < 0.3 \text{ V}, V_{D-} < 0.3 \text{ V}^{(4)}$				500	μΑ
I _{CC(I/O)(static)}	Static I/O supply current	Full-speed idle, SE0 or suspe	end		10	22	μA
I _{CC(susp)}	Suspend supply current	SUSPND = HIGH ⁽⁴⁾			10	22	μΑ
I _{CC(dis)}	Disable-mode supply current	V _{CC(I/O)} not connected ⁽⁴⁾			10	22	μΑ
I _{CC(I/O)(sharing)}	Sharing-mode I/O supply current	V _{CC(5.0)} or V _{reg(3.3)} not connect	cted		10	22	μΑ
I _{Dx(sharing)}	Sharing-mode load current on D+ and D-	V _{CC(5.0)} or V _{reg(3.3)} not connec SOFTCON = LOW, V _{Dx} = 3.6	cted, V			10	μΑ
W	Regulated supply-voltage	$1.65 \text{ V} \le V_{CC(I/O)} \le V_{reg(3.3)},$	Supply lost during power down		6 8 2.3 2.5 500 10 22 10 22 10 22 10 0.8	0.8	V
V _{reg(3.3)th}	detection threshold	$2.7 \text{ V} \le V_{\text{reg}(3.3)} \le 3.6 \text{ V}$	Supply detect during power up (5)	2.4			V
V _{reg(3.3)hys}	Regulated supply-voltage detection hysteresis	V _{CC(I/O)} = 1.8 V			0.45		٧
V	I/O supply-voltage	V 27V+026V	Supply lost during power down			0.5	V
$V_{CC(I/O)th}$	detection threshold	V _{reg(3.3)} = 2.7 V to 3.6 V Supply detect during power up		1.4			V
V _{CC(I/O)hys}	I/O supply-voltage detection hysteresis	V _{reg(3.3)} = 3.3 V			0.45		V

 I_{load} includes the pullup resistor current via $V_{pu(3.3)}$. In suspend mode, the typical voltage is 2.8 V. Maximum value is characterized only, not tested in production. (3)

Excluding any load current and $V_{pu(3.3)}V_{sw}$ source current to the 1.5-k Ω and 15-k Ω pullup and pulldown resistors (200 μ A typ) When $V_{CC(I/O)}$ < 2.7 V, the minimum value for $V_{reg(3.3)th}$ (present) is 2 V.

STATIC ELECTRICAL CHARACTERISTICS - DIGITAL PINS

over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	V _{CC(I/O)}	MIN	MAX	UNIT
V_{IL}	LOW-level input voltage		1.65 V to 3.6 V		0.3 V _{CC(I/O)}	V
V _{IH}	HIGH-level input voltage		1.65 V to 3.6 V	0.6 V _{CC(I/O)}		V
		I _{OL} = 100 μA	4.05.7/+= 2.0.7/		0.3 V _{CC(I/O)} 0.15 0.4 0.15 0.4 0.15 0.4 0.15 0.4 0.15	
	HIGH-level input voltage	0.4				
		I _{OL} = 100 μA	4.0.1/ + 0.45.1/		0.3 V _{CC(I/O)} 0.15 0.4 0.15 0.4 0.15 0.4 0.15	
.,	LOW level autout valtage	I _{OL} = 2 mA	1.8 V ± 0.15 V		0.4	V
V_{OL}	LOW-level output voltage	I _{OL} = 100 μA	251/ + 221/		0.15	V
		I _{OL} = 2 mA	2.5 V ± 0.2 V		0.4	
		I _{OL} = 100 μA	2271.027		0.15	
		I _{OL} = 2 mA	3.3 V ± 0.3 V			
		I _{OH} = 100 μA	4.05.1/10.0.1/	V _{CC(I/O)} - 0.15		
		$I_{OH} = 2 \text{ mA}$	1.00 V 10 3.0 V	V _{CC(I/O)} - 0.4		
		I _{OH} = 100 μA	4.0.1/ + 0.45.1/	1.5	0.3 V _{CC(I/O)} 0.15 0.4 0.15 0.4 0.15 0.4 0.15 0.4 1	
.,	LUCI Llaval avitavit valta sa	I _{OH} = 2 mA	1.8 V ± 0.15 V	1.25		V
V_{OH}	HIGH-level output voltage	I _{OH} = 100 μA	251/ + 221/	2.15		V
		I _{OH} = 2 mA	2.5 V ± 0.2 V	1.9	0.4 0.15 0.4 0.15 0.4 0.15 0.4	
		$I_{OH} = 100 \mu A$	3.3 V ± 0.3 V	2.85		
		I _{OH} = 2 mA	3.3 V ± 0.3 V	2.6		
I _{LI}	Input leakage current			-1	1	μΑ
C _{IN}	Input capacitance	Pin to GND			3.5	pF



STATIC ELECTRICAL CHARACTERISTICS - ANALOG I/O PINS

over recommended ranges of operating free-air temperature and supply voltage, V_{CC} = 4 V to 5.5 V or $V_{reg(3.3)}$ = 3 V to 3.6 V, V_{GND} = 0 V, T_A = -40°C to 85°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DI}	Differential input sensitivity	$ V_{I(D+)} - V_{I(D-)} $	0.2			V
V_{CM}	Differential common-mode voltage	Includes V _{DI} range	0.8		2.5	V
V_{IL}	LOW-level input voltage, single-ended receiver		2		8.0	V
V _{IH}	HIGH-level input voltage, single-ended receiver		0.4			V
V _{hys}	Hysteresis voltage, single-ended receiver				0.7	V
V _{OL}	LOW-level output voltage	$R_L = 1.5 \text{ k}\Omega \text{ to } 3.6 \text{ V}$			0.3	V
V_{OH}	HIGH-level output voltage	$R_L = 1.5 \text{ k}\Omega \text{ to GND}$	2.8(1)		3.6	V
I _{LZ}	OFF-state leakage current				1	μΑ
C _{IN}	Transceiver capacitance	Pin to GND			25	pF
Z_{DRV}	Driver output impedance	Steady-state drive	34 ⁽²⁾	39	44	Ω
Z _{INP}	Input impedance		10			МΩ
R _{SW}	Internal switch resistance at V _{pu(3.3)}				13	Ω
V_{TERM}	Termination voltage for upstream port pullup (RPU)		3(3) (4)		3.6	V

 $V_{OH(min)}$ = $V_{reg(3.3)}$ – 0.2 V Includes external resistors of 33 Ω ±1% on both D+ and D– (2) (3) (4)

This voltage is available at $V_{reg(3.3)}$ and $V_{pu(3.3)}$. In suspend mode, the minimum voltage is 2.7 V.



DYNAMIC ELECTRICAL CHARACTERISTICS – ANALOG I/O PINS (D+, D-)⁽¹⁾ (2) Driver Characteristics, Full-Speed Mode

over recommended ranges of operating free-air temperature and supply voltage, $V_{CC} = 4 \text{ V}$ to 5.5 V or $V_{\text{reg}(3.3)} = 3 \text{ V}$ to 3.6 V, $V_{CC(I/O)} = 1.65 \text{ V}$ to 3.6 V, $V_{GND} = 0 \text{ V}$, see Table 10 for valid voltage level combinations, $T_A = -40^{\circ}\text{C}$ to 85°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t _{FR}	Rise time	$C_L = 50 \text{ pF to } 125 \text{ pF},$ 10% to 90% of $ V_{OH} - V_{OL} $ (see Figure 1)	4	20	ns
t _{FF}	Fall time	$C_L = 50 \text{ pF to } 125 \text{ pF},$ 90% to 10% of $ V_{OH} - V_{OL} $ (see Figure 1)	4	20	ns
FRFM	Differential rise/fall time matching (t _{FR} /t _{FF})	Excluding the first transition from idle state	90	111.1	%
V_{CRS}	Output signal crossover voltage	Excluding the first transition from idle state (see Figure 10)	1.3	2	V

- (1) Test circuit, see Figure 13
- (2) Driver timing in low-speed mode is not specified. Low-speed delay timings are dominated by the slow rise/fall times t_{LR} and t_{LF}.

DYNAMIC ELECTRICAL CHARACTERISTICS – ANALOG I/O PINS (D+, D-)⁽¹⁾ (2) Driver Characteristics, Low-Speed Mode

over recommended ranges of operating free-air temperature and supply voltage, $V_{CC} = 4 \text{ V}$ to 5.5 V or $V_{\text{reg}(3.3)} = 3 \text{ V}$ to 3.6 V, $V_{CC(I/O)} = 1.65 \text{ V}$ to 3.6 V, $V_{GND} = 0 \text{ V}$, see Table 10 for valid voltage level combinations, $T_A = -40^{\circ}\text{C}$ to 85°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t _{LR}	Rise time	$C_L = 200 \text{ pF to } 600 \text{ pF},$ 10% to 90% of $ V_{OH} - V_{OL} $ (see Figure 1)	75	300	ns
t _{LF}	Fall time	$C_L = 200 \text{ pF to } 600 \text{ pF},$ 90% to 10% of $ V_{OH} - V_{OL} $ (see Figure 1)	75	300	ns
LRFM	Differential rise/fall time matching (t _{LR} /t _{LF})	Excluding the first transition from idle state	80	125	%
V_{CRS}	Output signal crossover voltage	Excluding the first transition from idle state (see Figure 10)	1.3	2	V

- (1) Test circuit, see Figure 13
- (2) Driver timing in low-speed mode is not specified. Low-speed delay timings are dominated by the slow rise/fall times t_{LR} and t_{LF}.

DYNAMIC ELECTRICAL CHARACTERISTICS – ANALOG I/O PINS (D+, D-)⁽¹⁾ (2) Driver Timing, Full-Speed Mode

over recommended ranges of operating free-air temperature and supply voltage, $V_{CC} = 4 \text{ V}$ to 5.5 V or $V_{\text{reg}(3.3)} = 3 \text{ V}$ to 3.6 V, $V_{CC(I/O)} = 1.65 \text{ V}$ to 3.6 V, $V_{GND} = 0 \text{ V}$, see Table 10 for valid voltage level combinations, $T_A = -40^{\circ}\text{C}$ to 85°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT	
t _{PLH(drv)}	Driver propagation delay	LOW to HIGH (see Figure 4)		18	ns	
t _{PHL(drv)}	(VO/VPO, FSE0/VMO to D+, D-)	PO, FŠE0/VMO to D+, D-) HIGH to LOW (see Figure 4)				
t _{PHZ}	Disconsiderable dates (OF to D. D.)	HIGH to OFF (see Figure 2)		15		
t _{PLZ}	Driver disable delay (OE to D+, D-)	LOW to OFF (see Figure 2)		15	ns	
t _{PZH}	Driver enable dalay (OF to D. D.)	OFF to HIGH (see Figure 2)		15		
t _{PZL}	Driver enable delay (OE to D+, D-)	OFF to LOW (see Figure 2)		15	ns	

- (1) Test circuit, see Figure?
- (2) Driver timing in low-speed mode is not specified. Low-speed delay timings are dominated by the slow rise/fall times t_{LR} and t_{LF}.

10



DYNAMIC ELECTRICAL CHARACTERISTICS FOR ANALOG I/O PINS (D+, D-)⁽¹⁾ Receiver Timing, Full-Speed and Low-Speed Mode, Differential Receiver

over recommended ranges of operating free-air temperature and supply voltage, $V_{CC} = 4 \text{ V}$ to 5.5 V or $V_{\text{reg}(3.3)} = 3 \text{ V}$ to 3.6 V, $V_{CC(I/O)} = 1.65 \text{ V}$ to 3.6 V, $V_{GND} = 0 \text{ V}$, see Table 10 for valid voltage level combinations, $T_A = -40^{\circ}\text{C}$ to 85°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN MAX	UNIT
t _{PLH(rcv)}	Propagation delay (D. D. to PC)()	LOW to HIGH (see Figure 3)	15	20
t _{PHL(rcv)}	Propagation delay (D+, D- to RCV)	HIGH to LOW (see Figure 3)	15	ns

⁽¹⁾ Test circuit, see Figure?

DYNAMIC ELECTRICAL CHARACTERISTICS FOR ANALOG I/O PINS (D+, D-)⁽¹⁾ Receiver Timing, Full-Speed and Low-Speed Mode, Single-Ended Receiver

over recommended ranges of operating free-air temperature and supply voltage, $V_{CC} = 4 \text{ V}$ to 5.5 V or $V_{\text{reg}(3.3)} = 3 \text{ V}$ to 3.6 V, $V_{CC(I/O)} = 1.65 \text{ V}$ to 3.6 V, $V_{GND} = 0 \text{ V}$, see Table 10 for valid voltage level combinations, $T_A = -40^{\circ}\text{C}$ to 85°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t _{PLH(se)}	Propagation delay (D. D. to V.D. \/M)	LOW to HIGH (see Figure 3)		18	20
t _{PHL(se)}	Propagation delay (D+, D– to VP, VM)	HIGH to LOW (see Figure 3)		18	ns

(1) Test circuit, see Figure 13

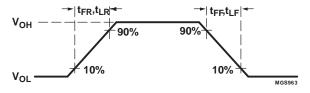


Figure 1. Rise and Fall Times

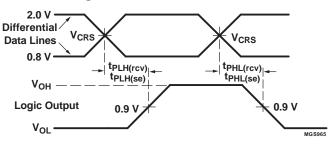


Figure 3. D+, D- to RCV, VP, VM

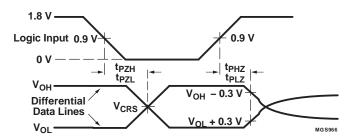


Figure 2. OE to D+, D-

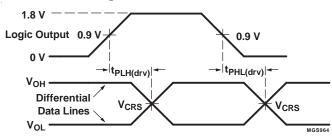


Figure 4. VO/VPO, FSE0/VMO to D+, D-

APPLICATION INFORMATION

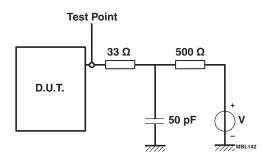


Figure 5. Load for Enable and Disable Times

- A. $V = 0 V \text{ for } t_{PZH}, t_{PHZ}$
- B. $V = V_{reg(3.3)}$ for t_{PZL} , t_{PLZ}

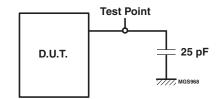


Figure 6. Load for VM, VP, and RCV

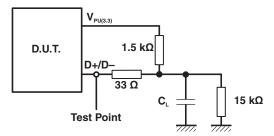


Figure 7. Load for D+, D-

- A. Full-speed mode: connected to D+
- B. Low-speed mode: Connected to D-
- C. Load capacitance:
 - $C_L = 50 \text{ pF}$ or 125 pF (full-speed mode, minimum or maximum timing)
 - $C_L = 200 \text{ pF} \text{ or } 600 \text{ pF} \text{ (low-speed mode, minimum or maximum timing)}$

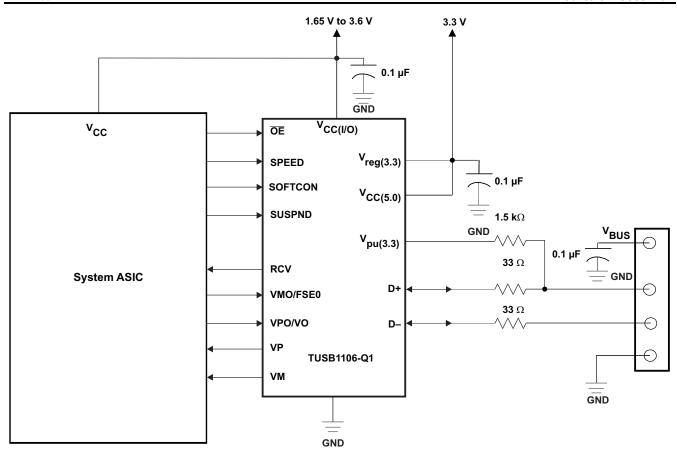


Figure 8. Peripheral-Side (Full-Speed) Regulator Bypass Mode

Peripheral-Side (Full-Speed) Regulator Bypass Mode

This mode is applicable when there is a 3.3-V supply already available on the board. The V_{BUS} pin of the USB connector, if left unused at the peripheral side, should be terminated with a 0.1- μ F capacitor. While operating at full speed, the 1.5-k Ω resistor must be connected between the D+ line and $V_{PU(3.3)}$ or an external 3.3-V supply. When the $V_{CC(5.0)}$ and the $V_{reg(3.3)}$ are connected together, the device operates at regulator bypass mode. This enables power savings since the regulator is turned off.



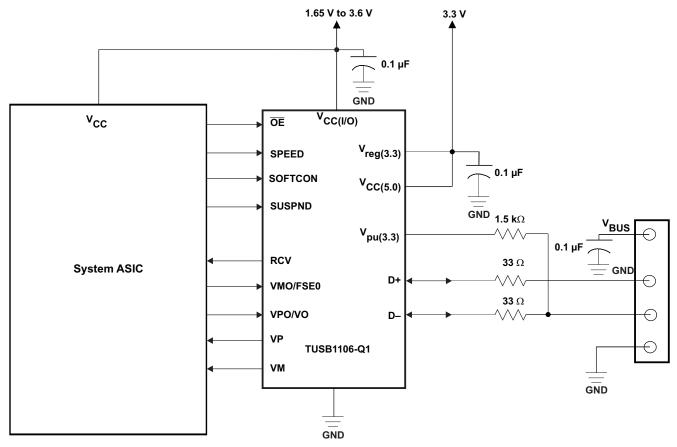


Figure 9. Peripheral-Side (Low-Speed) Regulator Bypass Mode

Peripheral-Side (Low-Speed) Regulator Bypass Mode

This mode is applicable when there is a 3.3-V supply already available on the board. The V_{BUS} pin of the USB connector, if left unused at the peripheral side, should be terminated with a 0.1- μ F capacitor. While operating at low speed, the 1.5- $k\Omega$ resistor must to be connected between the D– line and $V_{PU(3.3)}$ or an external 3.3-V supply. When the $V_{CC(5.0)}$ and the $V_{reg(3.3)}$ are connected together, the device operates at regulator bypass mode. This enables power savings since the regulator is turned off.

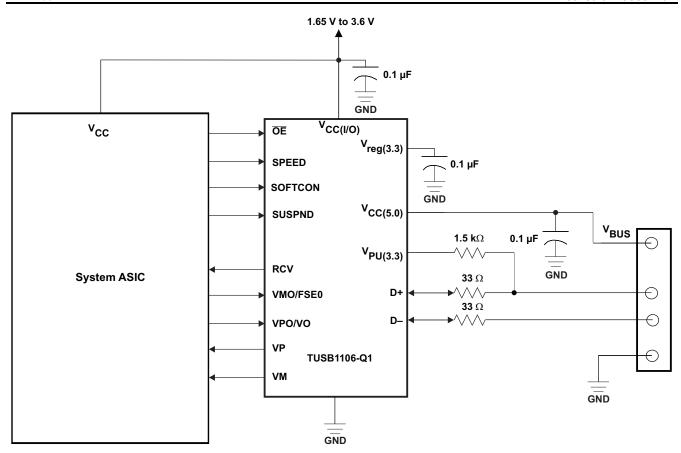


Figure 10. Peripheral-Side (Full-Speed) Internal Regulator Mode

Peripheral-Side (Full-Speed) Internal Regulator Mode

The USB side of the TUSB1106-Q1 can be powered from the V_{BUS} line directly if a 3.3-V supply is not present on board. In this case, the internal regulator can be used to provide the 3.3-V supply for USB signaling. The $V_{CC(5.0)}$ is connected to the V_{BUS} , which receives 5-V supply from the host, and generates the 3.3-V output at the $V_{reg(3.3)}$ pin. In this mode, it is important that both $V_{CC(5.0)}$ and $V_{reg(3.3)}$ pins have individual bypass capacitors in the range of 0.1 μ F. Powering $V_{CC(5.0)}$ through the V_{BUS} port of the USB connector realizes significant power saving for portable applications, such as cell phones, PDAs, etc. In this operating mode, the $I_{CC(5.0)}$ current is fed from the host. The USB-side power consumption, $I_{CC(5.0)}$ is 4 mA (with the regulator active), as opposed to logic-side $I_{CC(IO)}$ of 1 mA under full-speed operation. While operating at full speed, the 1.5-k Ω resistor must be connected between the D+ line and the $V_{PU(3.3)}$ or an external 3.3-V supply.



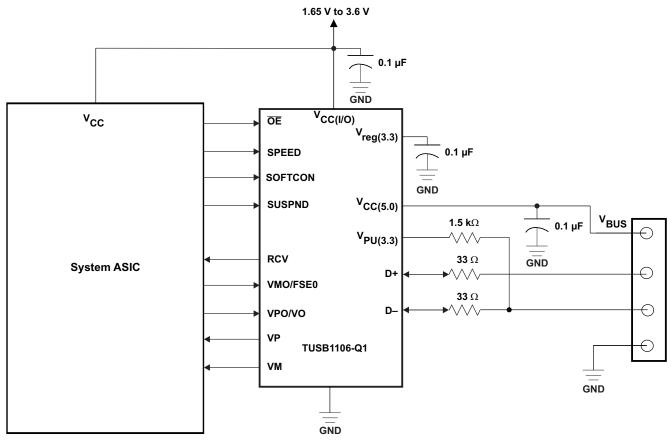


Figure 11. Peripheral-Side (Low-Speed) Internal Regulator Mode

Peripheral-Side (Low-Speed) Internal Regulator Mode

The USB side of the TUSB1106-Q1 can be powered from the V_{BUS} line directly if a 3.3-V supply is not present on board. In this case, the internal regulator can be used to provide the 3.3-V supply for the USB signaling. The $V_{CC(5.0)}$ is connected to the V_{BUS} , which receives 5-V supply from the host, and generates the 3.3-V output at the $V_{reg(3.3)}$ pin. In this mode, it is important that both $V_{CC(5.0)}$ and $V_{reg(3.3)}$ pins have individual bypass capacitors in the range of 0.1 µF. Powering $V_{CC(5.0)}$ through the V_{BUS} port of the USB connector realizes significant power saving for portable applications, such as cell phones, PDAs, etc. In this operating mode, the $I_{CC(5.0)}$ current is fed from the host side. The USB-side power consumption, $I_{CC(5.0)}$ is 4 mA (with the regulator active), as opposed to logic-side $I_{CC(IO)}$ of 1 mA under full-speed operation. While operating at low speed, the 1.5-k Ω resistor must be connected between the D– line and the $V_{PU(3.3)}$ or an external 3.3-V supply.

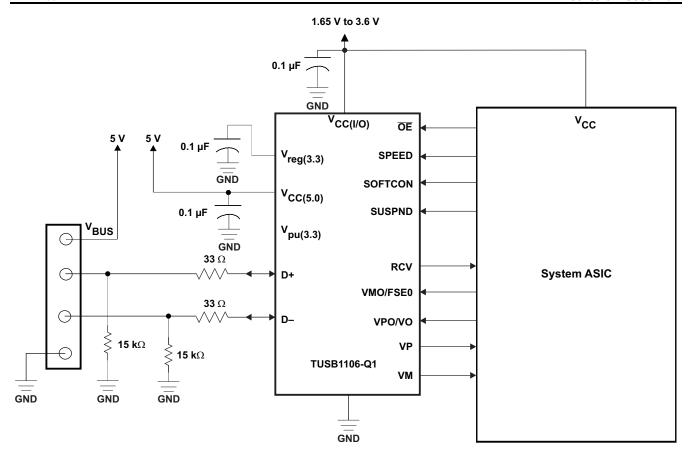


Figure 12. Host Side (V_{CC(5.0)} Supplied From V_{BUS} Pin)

Host Side (V_{CC(5.0)} Supplied From V_{BUS} Pin)

If there is no 3.3-V supply on board, an external 5-V supply can support the USB-side power needs. When the $V_{\text{CC}(5.0)}$ is connected to an external 5-V supply, the on-chip regulator generates the 3.3-V internal supply rail, which is used to drive the USB signaling levels at the USB side of the TUSB1106-Q1. The logic-side I/Os can operate at any voltage range from 1.65 V to 3.6 V.



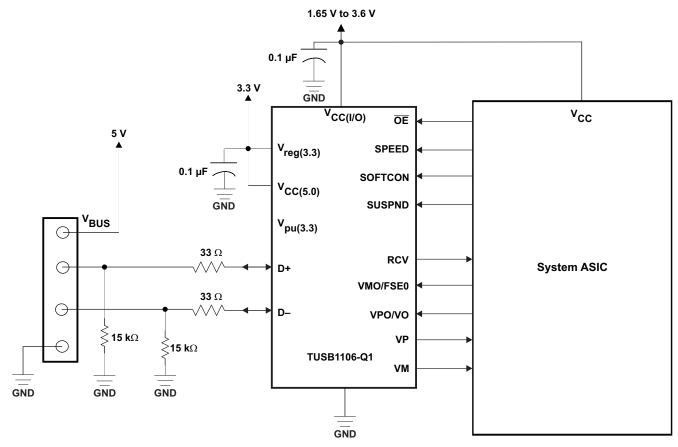


Figure 13. Host-Side (3.3-V Supply Present) Internal Regulator Bypass Mode

Host-Side (3.3-V Supply Present) Internal Regulator Bypass Mode

If a 3.3-V supply supports the USB-side power, $V_{CC(5.0)}$ and $V_{reg(3.3)}$ must to be tied together and connected to a 3.3-V supply. It also makes the regulator inactive.



16-Sep-2011

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
TUSB1106IPWRQ1	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TUSB1106-Q1:

Catalog: TUSB1106

NOTE: Qualified Version Definitions:

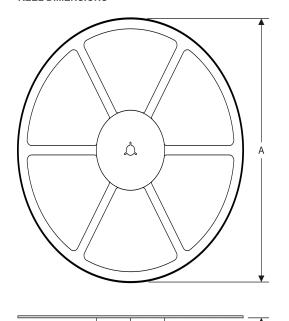
Catalog - TI's standard catalog product

PACKAGE MATERIALS INFORMATION

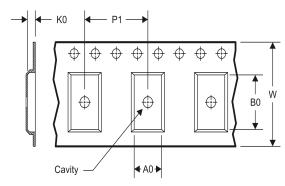
www.ti.com 16-Sep-2011

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device		~ .	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TUSB1106IPW	RQ1 T	SSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

www.ti.com 16-Sep-2011



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TUSB1106IPWRQ1	TSSOP	PW	16	2000	346.0	346.0	29.0

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Applications

interface.ti.com

Audio www.ti.com/audio Communications and Telecom www.ti.com/communications **Amplifiers** amplifier.ti.com Computers and Peripherals www.ti.com/computers dataconverter.ti.com Consumer Electronics www.ti.com/consumer-apps **Data Converters DLP® Products** www.dlp.com **Energy and Lighting** www.ti.com/energy DSP dsp.ti.com Industrial www.ti.com/industrial Clocks and Timers www.ti.com/clocks Medical www.ti.com/medical

Logic logic.ti.com Space, Avionics and Defense www.ti.com/space-avionics-defense

Security

Power Mgmt power.ti.com Transportation and Automotive www.ti.com/automotive

Microcontrollers microcontroller.ti.com Video and Imaging www.ti.com/video

RFID <u>www.ti-rfid.com</u>

OMAP Mobile Processors www.ti.com/omap

Interface

Wireless Connctivity www.ti.com/wirelessconnectivity

TI E2E Community Home Page <u>e2e.ti.com</u>

www.ti.com/security