PW PACKAGE (TOP VIEW)

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- 400-MHz Differential Clock Source for Direct Rambus Memory Systems for an 800-MHz Data Transfer Rate
- Operates From Two (3.3-V and 1.80-V) Power Supplies With 180 mW (Typ) at 400 MHz Total
- Packaged in a Thin Shrink Small-Outline Package (PW)
- External Crystal Required for Input

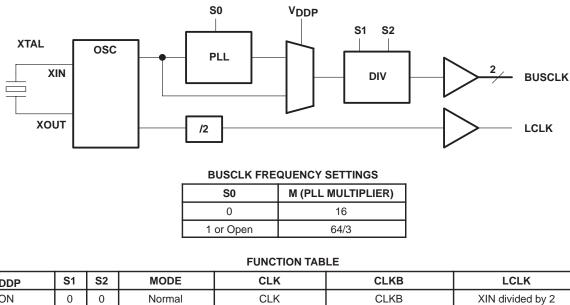
V_{DDP} 16 10 1 S0 GNDP 🗖 2 15 XOUT 🗖 3 14 ⊐ GND 13 4 🗖 CLK V_{DDL} 🗖 5 12 🗖 CLKB 6 11 🖵 GND II V_{DD} 10 7 GNDL 🗖 8 9 S1 □ 🗖 S2

description

The Direct Rambus clock generator – lite (DRCG-Lite) is an independent crystal clock generator. It performs clock multiplication using PLL, sourced by an internal crystal oscillator. It provides one differential, high-speed Rambus channel compatible output pair. Also, one single-ended output is available to deliver 1/2 of the crystal frequency. The Rambus channel operates at up to 400 MHz with an option to select 300 MHz as well. The desired crystal is a 18.75-MHz crystal in a series resonance fundamental application.

The CDCR61A is characterized for operation over free-air temperatures of 0°C to 85°C.

functional block diagram



V _{DDP}	S1	S2	MODE	CLK	CLKB	LCLK
ON	0	0	Normal	CLK	CLKB	XIN divided by 2
ON	1	1	Normal	CLK	CLKB	XIN divided by 2
ON	0	1	Test	Divided by 2	Divided by 2	XIN divided by 2
ON	1	0	Test	Divided by 4	Divided by 4	XIN divided by 2
0 V	0	0	Test	XIN	XIN (invert)	XIN divided by 2
0 V	1	1	Test	XIN	XIN (invert)	XIN divided by 2
0 V	0	1	Test	XIN divided by 2	XIN (invert) divided by 2	XIN divided by 2
0 V	1	0	Test	XIN divided by 4	XIN (invert) divided by 4	XIN divided by 2



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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TERMIN	TERMINAL I/O		DESCRIPTION
NAME	NO.	1/0	DESCRIPTION
CLK	13	0	Output clock, connect to Rambus channel
CLKB	12	0	Output clock (complement), connect to Rambus channel
GNDP, GNDL, GND	2, 7, 11, 14		Ground
LCLK	6	0	LVCMOS output, 1/2 of crystal frequency
S0, S1, S2	16, 8, 9	I	LVTTL level logic select terminal for function selection
V _{DD}	10, 15		Power supply, 3.3 V
VDDP	1		Power supply for PLL, 3.3 V (0 V for Test mode)
VDDL	5		Power supply for LCLK, 1.8 V
XIN	4	I	Reference crystal input
XOUT	3	0	Reference crystal feedback

Terminal Functions

absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

Supply voltage range, V _{DD} or V _{DDP} (see Note 1)	–0.5 V to 4 V
Supply voltage range, V _{DDL} (see Note 1)	–0.5 V to 4 V
Input voltage range,V _I , at any input terminal	–0.5 V to V _{DD} + 0.5 V
Output voltage range, V _O , at any output terminal (CLK, CLKB) .	–0.5 V to V _{DD} + 0.5 V
Output voltage range, V _O , at any output terminal (LCLK)	–0.5 V to V _{DDL} + 0.5 V
ESD rating (MIL-STD 883C, Method 3015)	> 2 kV, Machine Model >200 V
Continuous total power dissipation	see Dissipation Rating Table
Operating free-air temperature range, T _A	0°C to 85°C
Storage temperature range, T _{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the GND terminals.

DISSIPATION RATING TABLE

PACKAGE	T _A ≤ 25°C	DERATING FACTOR	T _A = 85°C
	POWER RATING	ABOVE T _A = 25°C‡	POWER RATING
PW	1400 mW	11 mW/°C	740 mW

[‡] This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.



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recommended operating conditions

		MIN	NOM	MAX	UNIT	
Supply voltage, V _{DD}	3	3.3	3.6	V		
LCLK supply voltage, VDDL		1.7	1.8	2.1	V	
	SO			0.35×V _{DD}	V	
Low-level input voltage, VIL	S1, S2		0.35×V _{DD}		v	
	SO	0.65×V _{DD}			V	
High-level input voltage, VIH	S1, S2	0.65×V _{DD}				
	SO	10	55	100	L-O	
Internal pullup resistance	S1, S2	90	145	250	kΩ	
	CLK, CLKB			16	A	
Low-level output current, IOL	LCLK			10	mA	
	CLK, CLKB			-16		
High-level output current, IOH	LCLK			-10	mA	
Input frequency at crystal input	·	14.0625	18.75		MHz	
· · · · · · · · · · · · · · · · · · ·	S0, S1, S2			2.5		
Input capacitance (CMOS), CI [†]	XIN, XOUT	1	-	20	pF	
Operating free-air temperature, TA	•	0		85	°C	

 † Capacitance measured at f = 1 MHz, dc bias = 0.9 V, and V_{AC} < 100 mV

timing requirements

	MIN	MAX	UNIT
Clock cycle time, t _(cycle)	2.5	3.7	ns
Input slew rate, SR	0.5	4	V/ns
State transition latency (V _{DDX} or S0 to CLKs – normal mode), t _(STL)		3	ms

crystal specifications

	MIN	MAX	UNIT
Frequency	14.0625	18.75	MHz
Frequency tolerance (at 25°C ±3°C)	-15	15	ppm
Equivalent resistance (C _L = 10 pF)		100	Ω
Temperature drift (-10°C to 75°C)		10	ppm
Drive level	0.01	1500	μW
Motional inductance	20.7	25.3	mH
Insulation resistance	500		MΩ
Spurious attenuation ratio (at frequency \pm 500 kHz)	3		dB
Overtone spurious	8		dB



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CON	MIN	typ‡	MAX	UNIT		
V _{O(X)}	Differential crossing-point c	utput voltage	See Figures 1 and 7		1.25		1.85	V
VO(PP)	Peak-to-peak output voltag single ended	V _{OH} – V _{OL} ,	See Figure 1	0.4		0.7	V	
VIK	Input clamp voltage		V _{DD} = 3 V,	lj = -18 mA			-1.2	V
RI	Input resistance	XIN, XOUT	V _{DD} = 3.3 V,	$V_{I} = V_{O}$		>50		kΩ
		XOUT	V _{DD} = 3.3 V,	V _O = 2 V			27	mA
ΙΗ	High-level input current	S0	V _{DD} = 3.6 V,	$V_{I} = V_{DD}$			10	A
		S1, S2	V _{DD} = 3.6 V,	$V_{I} = V_{DD}$			10	μA
		XOUT	V _{DD} = 3.3 V,	VO = 0 V			-5.7	mA
IIL	Low-level input current	S0	V _{DD} = 3.6 V,	$V_{I} = 0 V$	-30		-100	A
		S1, S2	V _{DD} = 3.6 V,	$V_{I} = 0 V$	-10		-50	μA
			See Figure 1				2.1	
VOH		CLK, CLKB	V _{DD} = min to max,	I _{OH} = -1 mA	V _{DD} - 0.1 V			v
	High-level output voltage		V _{DD} = 3 V,	I _{OH} = -16 mA	2.2			
		LCLK	V _{DDL} = min to max,	I _{OH} = - 10 mA	V _{DDL} - 0.45 V		V _{DDL}	
		CLK, CLKB	See Figure 1	See Figure 1				
	Low-level output voltage		V _{DD} = min to max,	I _{OL} = 1 mA			0.1	v
VOL			V _{DD} = 3 V,	I _{OL} = 16 mA			0.5	
		LCLK	V _{DDL} = min to max,	I _{OL} = 10 mA	0		0.45	
		CLK, CLKB	V _{DD} = 3.135 V,	V _O = 1 V	-32	-52		
			V _{DD} = 3.3 V,	V _O = 1.65 V		-51		
lau	High-level output current		V _{DD} = 3.465 V,	V _O = 3.135 V		-14.5	-21	
ЮН	Figh-level output current		V _{DDL} = 1.7 V,	$V_{O} = 0.5 V$	-11	-26		mA
		LCLK	V _{DDL} = 1.8 V,	$V_{O} = 0.9 V$		-28		
			V _{DDL} = 2.1 V,	V _O = 1.6 V		-24.5	-35	
			V _{DD} = 3.135 V,	V _O = 1.95 V	43	61.5		
		CLK, CLKB	V _{DD} = 3.3 V,	V _O = 1.65 V		65		
	Low-level output current		V _{DD} = 3.465 V,	$V_{O} = 0.4 V$		25.5	36	mA
IOL	Low-level output current		V _{DDL} = 1.7 V,	V _O = 1.2 V	11	27		
		LCLK	V _{DDL} = 1.8 V,	V _O = 0.9 V		30		
			V _{DDL} = 2.1 V,	$V_{O} = 0.5 V$		28	38	
rон	High-level dynamic output i	esistance§	ΔI_{O} – 14.5 mA to ΔI_{O}) – 16.5 mA	12	25	40	Ω
rol	Low-level dynamic output r	esistance§	ΔI_{O} + 14.5 mA to ΔI_{C}) + 16.5 mA	12	17	40	Ω
CO	Output capacitance	CLK, CLKB					3	pF
0	Culpul capacitance	LCLK					3	p P

[†] V_{DD} refers to any of the following; V_{DD}, V_{DDL}, and V_{DDP} [‡] All typical values are at V_{DD} = 3.3 V, V_{DDL} = 1.8 V, T_A = 25°C. § $r_O = \Delta V_O / \Delta I_O$. This is defined at the output terminals, not at the measurement point of Figure 1.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

	PARAMETER	TEST CONDITIONS [†]	MIN	TYP [‡]	MAX	UNIT
IDD	Static supply current	Outputs high or low ($V_{DDP} = 0 V$)			6.5	mA
IDDL	Static supply current (LVCMOS)	Outputs high or low ($V_{DDP} = 0 V$)			50	μA
IDD(NORMAL)	Supply surrent in normal state	300 MHz			39	mA
	Supply current in normal state	400 MHz			50	mA
IDDL(NORMAL)	Supply current in normal state (LVCMOS)	400 MHz			8	mA

 † V_{DD} refers to any of the following; V_{DD}, V_{DDL}, and V_{DDP}

[‡] All typical values are at $V_{DD} = 3.3 \text{ V}$, $V_{DDL} = 1.8 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER		TEST CONDITIONS	MIN	τυρ† ΜΑΧ	UNIT
t(cycle)	Clock cycle time (CLK, CLKB)		2.5	3.7	ns	
. .	Total jitter over 1, 2, 3, 4, 5, or 6	300 MHz	See Figure 2		140	
^t cj	clock cycles‡	400 MHz	See Figure 3		100	ps
÷	Long-term jitter	300 MHz	See Figure 4		400	ps
tj∟	Long-term jitter	400 MHz	See Figure 4		300	μs
^t DC	Output duty cycle over 10,000 cycles	_	See Figure 5	45%	55%	
^t DC,ERR	Output cycle-to-cycle duty cycle error	300 MHz	See Figure 6		70	
		400 MHz	See Figure 6		55	ps
t _r , t _f	Output rise and fall times (measured at 20%-80% of output voltage) [#]			160	400	ps
Δt	Difference between rise and fall times device (20%–80%) $ t_f-t_f ^{\#}$	See Figure 9,		100	ps	
^t c(LCLK)	Clock cycle time (LCLK)			106.6	142.2	ns
^t (cj)	LCLK cycle jitter§		See Figure 11	-0.2	0.2	ns
^t (cj10)	LCLK 10-cycle jitter ^{§¶}		See Figure 11	-1.3 t _(cj)	1.3 t _(cj)	ns
tDC	Output duty cycle	LCLK		40%	60%	
t _r , t _f	Output rise and fall times (measured at 20%-80% of output voltage)	LCLK	See Figure 9		1	ns
	PLL loop bandwidth		f _{mod} = 50 kHz		-3	dB
	FLL loop bandwidth		f _{mod} = 8 MHz	-20		uв

[†] All typical values are at $V_{DD} = 3.3$ V, $T_A = 25^{\circ}$ C.

[‡]Output short-term jitter specification is peak-to-peak (see Figure 9).

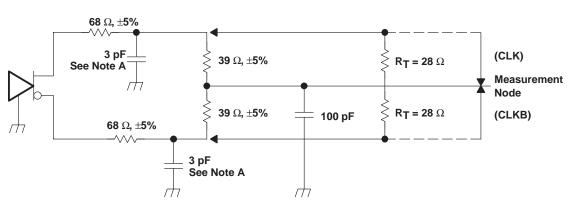
§ LCLK cycle jitter and 10-cycle jitter are defined as the difference between the measured period and the nominal period.

ILCLK 10-cycle jitter specification is based on the measured value of LCLK cycle jitter.

[#]V_{DD}= 3.3 V



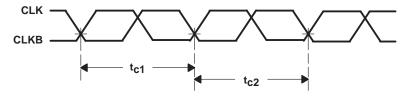
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PARAMETER MEASUREMENT INFORMATION

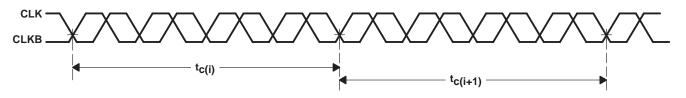
NOTE A: These capacitors represent parasitic capacitance. No discrete capacitors are used on the test board during device characterization.





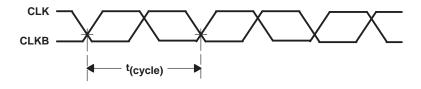
Cycle-to-cycle jitter = $|t_{C1} - t_{C2}|$ over 10000 consecutive cycles

Figure 2. Cycle-to-Cycle Jitter



 $t_{C(i)}$ = nominal expected time Cycle-to-cycle jitter = | $t_{C(i)} - t_{C(i+1)}$ | over 10000 consecutive cycles

Figure 3. Short-Term Cycle-to-Cycle Jitter over 2, 3, 4, or 6 Cycles



t_{jL} = | t_(cycle), max⁻ t_(cycle), min| over 10000 consecutive cycles

Figure 4. Long-Term Jitter



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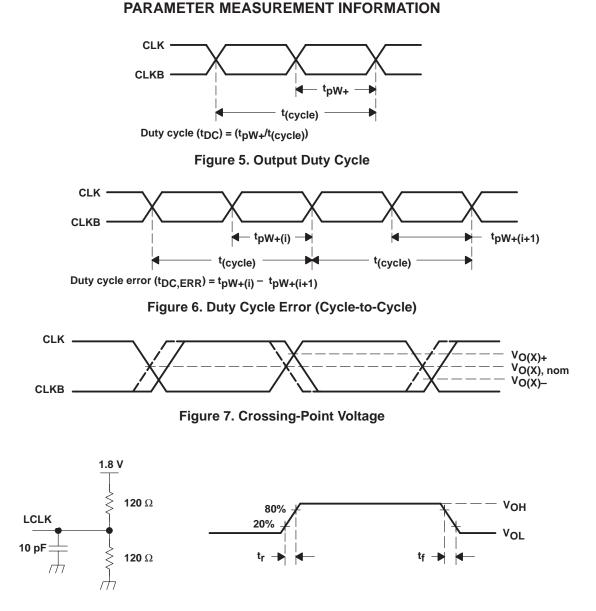
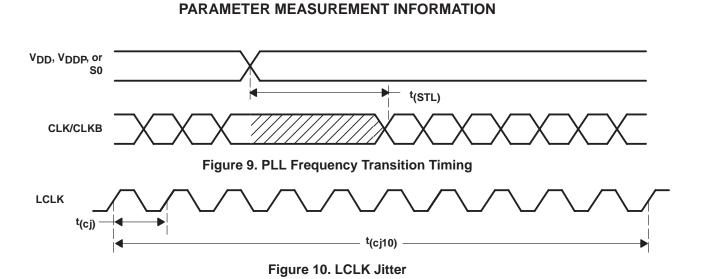


Figure 8. LCLK Test Load Circuit and Voltage Waveform for CLK/CLKB and LCLK



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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
CDCR61APW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
CDCR61APWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
CDCR61APWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
CDCR61APWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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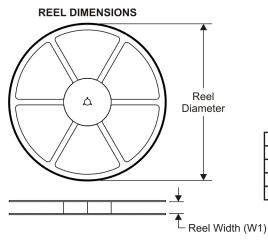
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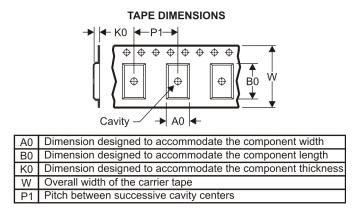
PACKAGE MATERIALS INFORMATION

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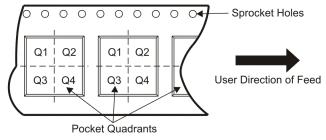
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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal	

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCR61APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TEXAS INSTRUMENTS

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PACKAGE MATERIALS INFORMATION

30-Jul-2010



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCR61APWR	TSSOP	PW	16	2000	346.0	346.0	29.0

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994. β . This drawing is subject to change without notice.

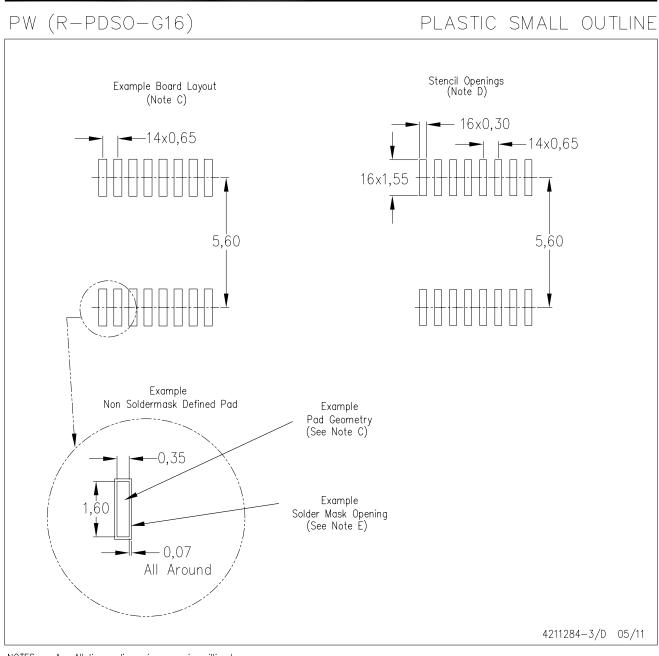
Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153



LAND PATTERN DATA



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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