CDC950 133-MHz DIFFERENTIAL CLOCK SYNTHESIZER/DRIVER FOR

PC MOTHERBOARDS/SERVERS SCAS646B – FEBRUARY 2001 – REVISED OCTOBER 2003

48 SEL100/133

DGG PACKAGE (TOP VIEW)

٠	Generates Clocks for Next Generation
	Microprocessors

- Uses a 14.318-MHz Crystal Input to Generate Multiple Output Frequencies
- Includes Spread Spectrum Clocking (SSC), 0.6% Downspread for Reduced EMI With Theoretical EMI of 7 dB
- Power Management Control Terminals
- Low Output Skew and Jitter for Clock Distribution
- Operates From a Single 3.3-V Supply
- Generates the Following Clocks:
  - 8 Host (Diff Pairs, 100/133 MHz)
  - 1 CLK33 (3.3 V, 33.3 MHz)
  - 1 REFCLK (3.3 V, 14.318 MHz)
  - 2 3V48 (3.3 V, 180° Shifted Pairs, 48 MHz)
- Packaged in a 48-Pin TSSOP Package

#### description

The CDC950 is a differential clock synthesizer/ driver that generates HCLK/HCLK, CLK33, 3V48, and REFCLK system clock signals to support a computer system with next generation processors and double data rate (DDR) memory subsystems.

All output frequencies are generated from a 14.318-MHz crystal input. A reference clock input

can be provided at the XIN input instead of a crystal. Two phase-locked loops (PLLs) are used to generate the host frequencies and the 48-MHz clock frequencies. On-chip loop filters and internal feedback eliminate the need for external components.

The HCLK, CLK33 clock, and 48-MHz clock outputs provide low-skew/low-jitter clock signals for reliable clock operation. All outputs have 3-state capability, which can be selected through control inputs SEL100/133, 3V48/SelA, and 3V48/SelB.

The outputs are either differential host clock or 3.3-V single-ended CMOS buffers. With a logic high-level on the  $\overline{PWRDWN}$  terminal, the device operates normally. When a logical low-level input is applied, the device powers down completely with the HOST clock at 2 × I<sub>REF</sub>, HOSTB is undriven, CLK33, 3V48, and REFCLK outputs are in a low-level output state and 3V48B is in a high-level output state.

The host bus can operate at 100 MHz or 133 MHz. Output frequency selection is done with the corresponding setting for SEL100/133 control input. The CLK33 (PCI) frequency is fixed to 33 MHz.

Since the CDC950 is based on PLL circuitry, it requires a stabilization time to achieve phase-lock of the PLL. This stabilization time is required following power up, as well as following changes to the SEL inputs. With the use of an external reference clock, this signal must be fixed-frequency and fixed-phase prior to stabilization time starts. The CDC950 is characterized for operation from 0°C to 85°C.



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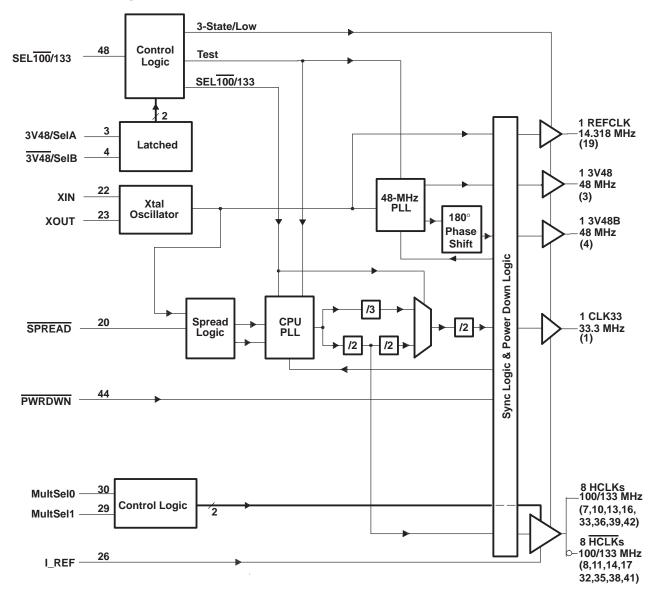


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0 =	<b>4</b> '	Ψυμυ	
V <sub>DD</sub> 3.3V	2	47 🛛 🤆	SND
3V48/SelA	3	46 🛛 A	V <sub>DD</sub> 3.3V
3V48/SelB	4	45 🛛 A	GND
GND	5	44 🛛 P	WRDWN
V <sub>DD</sub> 3.3V	6	43 🛛 V	<sub>DD</sub> 3.3V
HCLK(0)	7	42 ] ⊢	ICLK(4)
HCLK(0)	8	41 🛛 F	ICLK(4)
GND	9	40 🛛 🤆	SND
HCLK(1)	10	39 🛛 ⊢	ICLK(5)
HCLK(1)	11	38 🛛 F	ICLK(5)
V <sub>DD</sub> 3.3V	12	37 🛛 V	′ <sub>DD</sub> 3.3V
HCLK(2)	13	36 🛛 ⊢	ICLK(6)
HCLK(2)	14	35 🛛 F	ICLK(6)
GND	15	34 🛛 🤆	SND
HCLK(3)	16	33]⊦	ICLK(7)
HCLK(3)	17	32 🛛 F	ICLK(7)
V <sub>DD</sub> 3.3V	18	31 🛛 V	<sub>DD</sub> 3.3V
REFCLK	19	30 🛛 N	lultSel0
SPREAD	20	29 🛛 N	lultSel1
GND	21	28 ] 🤆	SND
XIN	22	27 🛛 A	GND
XOUT	23	26 🛛 I_	REF
V <sub>DD</sub> 3.3V	24	25 A	V <sub>DD</sub> 3.3V

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#### functional block diagram





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#### **Terminal Functions**

TERM	IINAL		
NAME	NO.	1/0	DESCRIPTION
3V48/SelA, 3V48/SelB	3, 4	I/O	48-MHz 180° shifted pair clocks for USB use Logic select pins. Selects the mode of operation, see Table 1 for details.
AGND	27, 45	Р	Analog ground
AV <sub>DD</sub> 3.3V	25, 46	Р	Power. Analog power supply
CLK33	1	0	33-MHz reference clock for PCI use, host clock divided by 3 or by 4
GND	5, 9, 15, 21, 28, 34, 40, 47	Ρ	Ground
HCLK	7, 10, 13, 16, 33, 36, 39, 42	0	CPU and host clock outputs [7:0]. These eight differential CPU clock pairs run at 100/133 MHz. The $V_{OH}$ swing amplitude is configured by MultSel0, MultSel1 pins. See Table 5 and Intel's CK00 document for details.
HCLK	8, 11, 14, 17, 32, 35, 38, 41	0	CPU and host clock outputs [7:0]. These eight differential CPU clock pairs run at 100/133 MHz. The $V_{OH}$ swing amplitude is configured by MultSel0, MultSel1 pins. See Table 5 and Intel's CK00 document for details.
I_REF	26	I	Current reference. This pin establishes the reference current for host clock parts. See Table 5 and Intel's CK00 document for details.
MultSel0	30	Ι	See Table 5 and Intel's CK00 document for details.
MultSel1	29	Ι	See Table 5 and Intel's CK00 document for details.
PWRDWN	44	I	Power-down input. 3.3-V LVTTL compatible, asynchronous input that requests the device to enter the power-down mode. See Table 2 for details.
REFCLK	19	0	14.138-MHz reference clock output: 3.3 V copy of the 14.318-MHz reference clock.
SEL100/133	48	I	Active low LVTTL level logic select. SEL100/133 is used for enabling 100/133 MHz. Low = 100 MHz, high = 133 MHz
SPREAD	20	U	Spread spectrum enable. 3.3-V LVTTL compatible, input that enables the spread spectrum mode when held low. See Table 4 for details.
V <sub>DD</sub> 3.3V	2, 6, 12, 18, 24, 31, 37, 43	Ρ	Power. Power supply
XIN	22	I	Crystal connection or an external reference frequency input. Connect to either a 14.138-MHz crystal or an external reference signal.
XOUT	23	0	Crystal connection. An output connection for an external 14.318-MHz crystal. If using an external reference, this pin must be left unconnected.



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## **Function Tables**

### **Table 1. Select Functions**

INPUTS				οι	FUNCTION		
SEL100/133	SelA	SelB	HCLK, HCLK	CLK33	3V48, <del>3V48</del>	REFCLK	FUNCTION
0	0	0	100 MHz	33 MHz	48 MHz	14.318 MHz	Active 100 MHz
0	0	1	100 MHz	33 MHz	L, H	14.318 MHz	100 MHz mode; PLL48 powerdown
0	1	0	105 MHz	35 MHz	48 MHz	14.318 MHz	100 MHz mode 5% overclocking
0	1	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z	All 3-state outputs
1	0	0	133 MHz	33 MHz	48 MHz	14.318 MHz	Active 133 MHz
1	0	1	127 MHz	31.7 MHz	48 MHz	14.318 MHz	133 MHz mode –5% underclocking
1	1	0	133 MHz	33 MHz	48 MHz	14.318 MHz	Test mode
1	1	1	TCLK/2	TCLK/8	TCLK/2	TCLK	Test mode (PLL bypass)

#### **Table 2. Enable Functions**

INPUT		OUTPUTS						
PWRDWN	HCLK	HCLK	CLK33	3V48	3V48	REFCLK		
0	$2 \times I_{REF}$	Hi-Z	L	L	Н	L		
1	On	On	On	On	On	On		

#### **Table 3. Output Buffer Specifications**

BUFFER NAME	V <sub>DD</sub> RANGE (V)	IMPEDANCE (Ω)	BUFFER TYPE
3V48, REFCLK	3.135 – 3.465	20–60	TYPE 3
CLK33	3.135 – 3.465	12–55	TYPE 5
HCLK/HCLK	3.135 – 3.465		TYPE X1

#### **Table 4. Spread Spectrum Functions**

INPUT	
SPREAD	OUTPUTS
0	Spread spectrum clocking active, -0.6% at HCLK/HCLK, CLK33
1	Spread spectrum clocking inactive



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#### **Function Tables (Continued)**

INF	TU	BOARD TARGET	REI	FERENCE R,	OUTPUT CURRENT	
MultSel0	MultSel1	TRACE/TERM Z	IREF	= = VDD/(3 Rr)	юн	V <sub>OH</sub> at Z
0	0	<b>60</b> Ω	Rr = 475 1%,	I_REF = 2.32 mA	5×I <sub>REF</sub>	0.71 V at 60 $\Omega$
0	0	50 Ω	Rr = 475 1%,	I_REF = 2.32 mA	5×I <sub>REF</sub>	0.59 V at 50 $\Omega$
0	1	60 Ω	Rr = 475 1%,	I_REF = 2.32 mA	6×I <sub>REF</sub>	0.85 V at 60 $\Omega$
0	1	<b>50</b> Ω	Rr = 475 1%,	I_REF = 2.32 mA	6×I <sub>REF</sub>	0.71 V at 50 $\Omega$
1	0	60 Ω	Rr = 475 1%,	I_REF = 2.32 mA	$4 \times I_{REF}$	0.56 V at 60 $\Omega$
1	0	50 Ω	Rr = 475 1%,	I_REF = 2.32 mA	$4 \times I_{REF}$	0.47 V at 50 $\Omega$
1	1	60 Ω	Rr = 475 1%,	I_REF = 2.32 mA	$7 \times I_{REF}$	0.99 V at 60 $\Omega$
1	1	50 Ω	Rr = 475 1%,	I_REF = 2.32 mA	$7 \times I_{REF}$	0.82 V at 50 $\Omega$
0	0	30 (dc equivalent)	Rr = 221 1%,	I_REF = 5 mA	$5 \times I_{REF}$	0.75 V at 30 $\Omega$
0	0	25 (dc equivalent)	Rr = 221 1%,	I_REF = 5 mA	5×I <sub>REF</sub>	0.62 V at 25 $\Omega$
0	1	30 (dc equivalent)	Rr = 221 1%,	I_REF = 5 mA	6×I <sub>REF</sub>	0.90 V at 30 $\Omega$
0	1	25 (dc equivalent)	Rr = 221 1%,	I_REF = 5 mA	6×I <sub>REF</sub>	0.75 V at 25 $\Omega$
1	0	30 (dc equivalent)	Rr = 221 1%,	I_REF = 5 mA	$4 \times I_{REF}$	0.60 V at 30 $\Omega$
1	0	25 (dc equivalent)	Rr = 221 1%,	I_REF = 5 mA	$4 \times I_{REF}$	0.5 V at 25 $\Omega$
1	1	30 (dc equivalent)	Rr = 221 1%,	I_REF = 5 mA	7×I <sub>REF</sub>	1.05 V at 30 $\Omega$
1	1	25 (dc equivalent)	Rr = 221 1%,	I_REF = 5 mA	7×IREF	0.84 V at 25 $\Omega$

#### Table 5. Host/HOST Output Buffer Specifications

NOTE: The entries in **boldface** are the primary system configurations of interest. The outputs should be optimized for these configurations.

#### absolute maximum ratings over operating free-air temperature (unless otherwise noted)<sup>†</sup>

Supply voltage range, V <sub>DD</sub> Input voltage range, V <sub>I</sub> (see Note 1)–0	
Voltage range applied to any output in the high-impedance or power-off state, $V_O$	
(see Note 1)(	0.5 V to V <sub>DD</sub> + 0.5 V
Current into any output in the low state, IO	$\dots 2 \times rated I_{OL}$
Input clamp current, I <sub>IK</sub> : (V <sub>I</sub> < 0)	
(V <sub>I</sub> > V <sub>DD</sub> )	50 mA
Output clamp current, I <sub>OK</sub> : (V <sub>O</sub> < 0)	
$V_{O} > V_{DD}$ )	
Package thermal impedance, $\theta_{JA}$ (see Note 2)	
Maximum power dissipation at $T_A = 55^{\circ}C$ (in still air) (see Note 3)	1070 mW
Operating free-air temperature range, T <sub>A</sub>	
Storage temperature range, T <sub>stg</sub>	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	

<sup>+</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for the through-hole packages, which use a trace length of zero.

3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.



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	DISSIPATION RATING TABLE							
DGG 1400 mW 11.2 mW/°C 900 mW 730 mW	PACKAGE				T <sub>A</sub> = 85°C POWER RATING			
	DGG	1400 mW	11.2 mW/°C	900 mW	730 mW			

<sup>†</sup>This is the inverse of the traditional junction-to-case thermal resistance (R<sub> $\theta$ JA</sub>) and uses a board-mounted device at 89°C/W

## recommended operating conditions (see Note 4)

		MIN	NOM‡	MAX	UNIT	
Supply voltages, V <sub>DD</sub> , AV <sub>DD</sub>		3.135	3.3	3.465		
High-level input voltage, VIH		2				
Low-level input voltage, VIL				0.8	V	
Input voltage, VI		-0.3		V <sub>DD</sub> + 0.3		
	HCLK/HCLK			-40		
	CLK33		-18			
High-level output current, IOH	3V48/SelA and 3V48/SelB			-14		
	REFCLK					
	HCLK/HCLK	2 0.8 -0.3 V <sub>DD</sub> +0.3 -40 -18 B/SelB -14 -14 0 0 12	mA			
	CLK33			12		
Low-level output current, IOL	3V48/SelA and 3V48/SelB			9		
REFCLK				9		
Reference frequency, f(XIN)§	Test mode		14			
Crystal, f <sub>(XTAL)</sub> ¶	Normal mode	13.8	14.318	14.8	MHz	
Operating free-air temperature, $T_A$		0		85	°C	

<sup>‡</sup> All nominal values are measured at their respective nominal V<sub>DD</sub> values.

\$ Reference frequency is a test clock driven on the XIN input during the device test mode or normal mode. In test mode, XIN can be driven externally up to  $f_{(XIN)} = 16$  MHz. If XIN is driven externally, XOUT is floating.

This is a series fundamental crystal with fo = 14.31818 MHz

NOTE 4: Unused inputs must be held high or low to prevent them from floating.



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#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMET	ER	TES	ST CONDITIONS		MIN	TYP†	MAX	UNIT
VIK	Input clamp voltag	je	V <sub>DD</sub> = 3.135 V,	lj = -18 mA				-1.2	V
Ίн	High-level input current	All inputs except SelA, SelB	V <sub>DD</sub> = 3.465 V,	$V_I = V_{DD}$				5	μΑ
۱ <sub>IL</sub>	Low-level input current	All inputs except SelA, SelB	V <sub>DD</sub> = 3.465 V,	VI = GND				-5	μΑ
IOZ	High-impedance -state output current	All outputs including SelA, SelB	V <sub>DD</sub> = 3.465 V	$3V48/SelA, \overline{3V48}/SelA, \overline{3V48}/SelL100/133 = L,      V_O = V_{DD} or GNE      PWRDWN = H$				±10	μA
IDD(Z)	High-impedance-state supply current <sup>‡</sup>		V <sub>DD</sub> = 3.465 V	3V48/SelA, 3V48/SelB = H, SEL100/133 = L, PWRDWN = H			19	25	mA
IDD(PD)		SelA, SelB = L	VDD Supply			43	47	mA	
AIDD(PD)	PWRDWN state supply current <sup>‡</sup>		<u>R<sub>(ref)</sub> = 47</u> 5 Ω PWRDWN = L	AVDD Supply			3.4	4.2	mA
		.+	V <sub>DD</sub> = 3.465 V,	PWRDWN = H	100 MHz		173	190	
IDD(D)	Dynamic supply c	urrent+	$R_{ref} = 475 \Omega,$ $I_O = 6 \times I_{ref}$	SSC = ON/OFF C <sub>L</sub> = MAX	133 MHz		183	200	mA
				100 MHz and SSC off 133 MHz and SSC off		19		24	
• •						26		33	
AIDD	Analog power supply current		V <sub>DD</sub> = 3.465 V	100 MHz and SSC on		26		33	mA
				133 MHz and SSC on		35		45	
Cl	Input capacitance	§	V <sub>DD</sub> = 3.3 V,	$V_I = V_{DD}$ or GND		2		5	- F
C <sub>(XTAL)</sub>	Crystal load capa	citance¶	Effective capacity	between CIN and C	OUT	13.5		22.5	pF

<sup>†</sup> All typical values are measured at their respective nominal V<sub>DD</sub> values.

This is the corresponding capacitive load for the XTAL in this oscillator application (Pierce oscillator)



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# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

## HCLK/HCLK (Type X1)

	PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
r <sub>o</sub>	Output resistance			3000			Ω
VO	Output voltage					1.2	V
		V <sub>DD</sub> = 3.30 V nom		-7% I(NOM)	I	7% (NOM)	
10	Output current	V <sub>DD</sub> = 3.30 V, ±5%	All combinations of Table 5, See Note 5	-12% I(NOM)	I	12% (NOM)	mA
CO	Output capacitance	$V_{DD} = 3.30 \text{ V nom}$	$V_{O} = V_{DD} GND$		3.5		pF

NOTE 5: I(NOM) is output current (IOH) of table 5.

# 3V48, 3V48REFCLK (Type 3)

	PARAME	TER	TEST CC	NDITIONS	MIN	түр†	MAX	UNIT
			$V_{DD}$ = min to max,	$I_{OH} = -1 \text{ mA}$	V <sub>DD</sub> – 0.1			
Vон	High-level output volta	age	V <sub>DD</sub> = 3.135 V,	I <sub>OH</sub> = -14 mA	2.4			
	Level and a dama to all		$V_{DD}$ = min to max,	I <sub>OL</sub> = 1 mA			0.1	V
VOL	Low-level output volta	ige	V <sub>DD</sub> = 3.135 V,	I <sub>OL</sub> = 9 mA		0.18	0.4	
		V <sub>DD</sub> = 3.135 V,	$V_{O} = 1 V$	-29				
ЮН	IOH High-level output current		V <sub>DD</sub> = 3.3 V,	V <sub>O</sub> = 1.65 V		-37		
			V <sub>DD</sub> = 3.465 V,	V <sub>O</sub> = 3.135 V		-11	-23	
			V <sub>DD</sub> = 3.135 V,	V <sub>O</sub> = 1.95 V	29			mA
IOL	Low-level output curre	ent	V <sub>DD</sub> = 3.3 V,	V <sub>O</sub> = 1.65 V		39		
				$V_{O} = 0.4 V$		16	27	
СО	Output capacitance		V <sub>DD</sub> = 3.3 V,	$V_{O} = V_{DD}$ or GND	4.5		7	pF
_		High state	$V_{O} = 0.5 V_{DD},$	V <sub>O</sub> /I <sub>OH</sub>	20	40	60	0
Zo	Output impedance	Low state	$V_{O} = 0.5 V_{DD},$	V <sub>O</sub> /I <sub>OL</sub>	20	40	60	Ω

<sup>†</sup> All typical values are measured at their respective nominal  $V_{DD}$  values.



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#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

#### CLK33 (Type 5)

	PARAMETER		TEST C	ONDITIONS	MIN	TYP†	MAX	UNIT
Maria	Link laval autout valt		V <sub>DD</sub> = min to max,	I <sub>OH</sub> = -1 mA	V <sub>DD</sub> – 0.1			
VOH	High-level output volt	age	V <sub>DD</sub> = 3.135 V,	I <sub>OH</sub> = -18 mA	2.4			
	Level and a damate of the		$V_{DD}$ = min to max,	I <sub>OL</sub> = 1 mA			0.1	V
V <sub>OL</sub> Low-level output volta		age	V <sub>DD</sub> = 3.135 V,	I <sub>OL</sub> = 12 mA		0.15	0.4	
			V <sub>DD</sub> = 3.135 V,	$V_{O} = 1 V$	-33			
IOH	High-level output curr	h-level output current		V <sub>O</sub> = 1.65 V		-53		
-			V <sub>DD</sub> = 3.465 V,	V <sub>O</sub> = 3.135 V		-16	-33	
			V <sub>DD</sub> = 3.135 V,	V <sub>O</sub> = 1.95 V	30			mA
loL	Low-level output curre	ent	V <sub>DD</sub> = 3.3 V,	V <sub>O</sub> = 1.65 V		51		
-			V <sub>DD</sub> = 3.465 V,	V <sub>O</sub> = 0.4 V		21	38	
CO	Output capacitance		V <sub>DD</sub> = 3.3 V,	$V_{O} = V_{DD}$ or GND	4.5		7.5	pF
7		High state	V <sub>O</sub> = 0.5 V <sub>DD</sub> ,	V <sub>O</sub> /I <sub>OH</sub>	12	35	55	0
Zo	Output impedance	Low state	$V_{O} = 0.5 V_{DD},$	V <sub>O</sub> /I <sub>OL</sub>	12	35	55	Ω

<sup>†</sup> All typical values are measured at their respective nominal V<sub>DD</sub> values.

## switching characteristics, V\_DD = 3.135 V to 3.465 V, T\_A = 0°C to 85°C

I	PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	ТҮР	MAX	UNIT
V <sub>(over)</sub>	Overshoot <sup>†</sup>			HCLK/HCLK 0.7-V		١	/ <sub>OH</sub> + 200	
V <sub>(under)</sub>	Undershoot <sup>†</sup>			amplitude		,	V <sub>OL</sub> – 200	mV
V <sub>(over)</sub>	Overshoot <sup>†</sup>			Other clocks,	GND – 0.7			V
V <sub>(under)</sub>	Undershoot <sup>†</sup>			C <sub>L</sub> = worst case			V <sub>DD</sub> + 0.7	V
t <sub>PZL</sub>	Output enable time from low level	SEL100/133	All outputs	SEL <u>100</u> /133 ↑ R <sub>ref</sub> = 475 Ω			10	
<sup>t</sup> PZH	Output enable time to high level	SEL100/133	All outputs	SEL <u>100</u> /133 ↑ R <sub>ref</sub> = 475 Ω			10	
<sup>t</sup> PHZ	Output disable time from high level	SEL100/133	All outputs	SEL <u>100</u> /133 ↓ R <sub>ref</sub> = 475 Ω			10	ns
<sup>t</sup> PLZ	Output disable time from low level	SEL100/133	All outputs	$\begin{array}{l} SEL\overline{100}/133 \downarrow \\ R_{ref} = 475 \ \Omega \end{array}$		10		
	Stabilization time <sup>‡</sup>	V <sub>DD</sub>	All outputs	After power up			0.1	ms
t <sub>S</sub>	Stabilization time+	PWRDWN	All outputs	From PWRDWN 1			0.25	ms

<sup>†</sup> These parameters are assured by design and lab characterization, not 100% production tested.

<sup>‡</sup> Stabilization time is the time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. In order for phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at XIN. Until phase lock is obtained, the specifications for propagation delay and skew parameters given in the switching characteristics tables are not applicable. Stabilization time is defined as the time since V<sub>DD</sub> achieves its nominal operating level (3.3 V) or PWRDWN transition from a low to a high level (2 V) until the output frequency is stable and operating within specification.



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## switching characteristics, $V_{DD}$ = 3.135 V to 3.465 V, $T_A$ = 0°C to 85°C (continued)

# HCLK/HCLK (Type X1), CL = 2 pF, R<sub>ref</sub> = 475 $\Omega$ , 6 x R<sub>ref</sub>

	PARAMETE	R	TEST CONDITIONS	TEST CONDITIONS			MAX	UNIT	
			f(HCLK) = 100 MHz	f(HCLK) = 100 MHz			10.2		
			f(HCLK) = 133 MHz		7.5		7.65	ns	
-			(	SSC off	-80		80		
Tjit(cc)	Cycle-to-cycle jitter		f(HCLK) = 100 or 133 MHz	SSC on	-110		110	ps	
<sup>t</sup> dc	Duty cycle		f(HCLK) = 100 or 133 MHz, Crossing point	45%		55%			
<sup>t</sup> sk(o)	HCLK bus skew		f(HCLK) = 100 or 133 MHz, Crossing point			70		ps	
t <sub>r</sub>	Rise time <sup>†</sup>	0.7.1/	V <sub>O</sub> = 0.14 V to 0.56 V		175		700		
tf	Fall time <sup>†</sup>	0.7-V amplitude	V <sub>O</sub> = 0.14 V to 0.56 V	V <sub>O</sub> = 0.14 V to 0.56 V			700	ps	
v(cross)	Cross point voltages†	0.7-V amplitude	f(HCLK) = 100  or  133-MHz HCLK and HCLK		45% VOH		55% Voh	V	

<sup>†</sup> These parameters are assured by design and lab characterization, not 100% production tested.

<sup>‡</sup>The average over any 1-µs period of time is greater than the minimum specified period.

## CLK33 (Type 5), CL = 30 pF, RL = 500 $\Omega$

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	PCI clock period <sup>†</sup>	f <sub>(HCLK)</sub> = 100 or 133 MHz	30	30.06	30.6	ns
T <sub>jit(cc)</sub>	Cycle-to-cycle jitter	f(HCLK) = 100 or 133 MHz	-150		150	ps
t(dc)	Duty cycle	f <sub>(CLK33)</sub> = 33.3 MHz	45%		55%	
t <sub>r</sub>	Rise time	$V_{O} = 0.4 V \text{ to } 2.4 V$	0.5		2	
t <sub>f</sub>	Fall time	$V_{O} = 0.4 \text{ V to } 2.4 \text{ V}$	0.5		2	ns

<sup>†</sup>The average over any 1-µs period of time is greater than the minimum specified period.

## 3V48 (Type 3), C<sub>L</sub> = 20 pF, R<sub>L</sub> = 500 $\Omega$

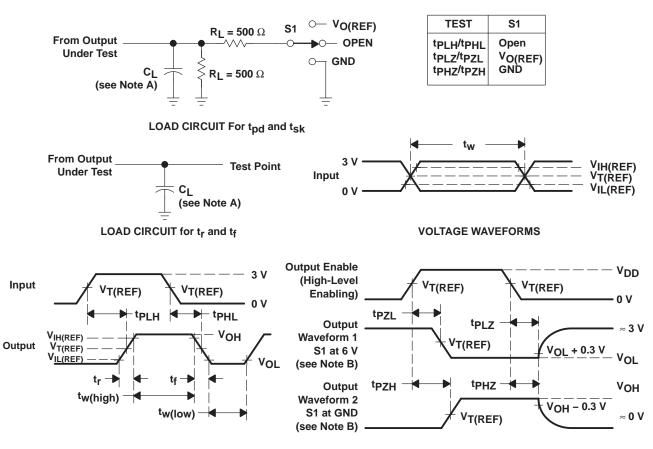
	PARAMETER	TEST CONDITIONS	MIN	TYP MAX	UNIT
	3V48 clock period	f(HCLK) = 100 or 133 MHz		20.83	ns
T <sub>jit(cc)</sub>	Cycle-to-cycle jitter	f(HCLK) = 100 or 133 MHz	-300	300	ps
t <sub>dc</sub>	Duty cycle	f <sub>(3V48)</sub> = 48 MHz	45%	55%	
t <sub>r</sub>	Rise time	$V_{O} = 0.4 \text{ V} \text{ to } 2.4 \text{ V}$	1	4	
t <sub>f</sub>	Fall time	$V_{O} = 0.4 \text{ V} \text{ to } 2.4 \text{ V}$	1	4	ns

## REF (Type 3), CL = 20 pF, RL = 500 $\Omega$

	PARAMETER	TEST CONDITIONS	MIN	TYP M	٩X	UNIT
	REF clock period	f(REF) = 14.318 MHz		69.84		~~
Tjit(cc)	Cycle-to-cycle jitter	f(HCLK) = 100 or 133 MHz	-0.5	(	0.5	ns
t(dc)	Duty cycle	f(REF) = 14.318 MHz	45%	55	5%	
t <sub>r</sub>	Rise time	$V_{O} = 0.4 \text{ V} \text{ to } 2.4 \text{ V}$	1		4	
tf	Fall time	$V_{O} = 0.4 V \text{ to } 2.4 V$	1		4	ns



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#### PARAMETER MEASUREMENT INFORMATION

#### **VOLTAGE WAVEFORMS**

- NOTES: A. C<sub>L</sub> includes probe and jig capacitance. C<sub>L</sub> = 2 pF (HCLK, HCLK), C<sub>L</sub> = 20 pF (48 MHz, REF), C<sub>L</sub> = 30 pF (CLK33).
  B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  14.318 MHz, Z<sub>O</sub> = 50  $\Omega$ , t<sub>f</sub>  $\leq$  2.5 ns, t<sub>f</sub>  $\leq$  2.5 ns.
  - D. The outputs are measured one at a time with one transition per measurement.

	PARAMETER	3.3-V INTERFACE	UNIT
VIH(REF)	High-level reference voltage	2.4	
VIL(REF)	Low-level reference voltage	0.4	V
V <sub>T(REF)</sub>	Input threshold reference voltage	1.5	v
VO(REF)	Off-state reference voltage	6	



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#### VDD R(S1) = 33 Ω TLA HCLK HCLK MultSel0 **CDC950** R(T1) = 49.9 Ω MultSel1 R(S1) = 33 Ω HCLK TLB HCLK R(T1) = 49.9 Ω RI(REF) = 475 Ω $C_L = 2 pF$ $C_L = 2 pF$

## APPLICATION INFORMATION

C<sub>L</sub> Represents C<sub>BOARD</sub> and C<sub>jig</sub>  $Z_{TLA} = Z_{TLB} = 50 \Omega$ 

Figure 2. Load Circuit for HCLK Bus

## spread spectrum clock (SSC) implementation for CDC950

Simultaneously switching at a fixed frequency generates a significant power peak at the selected frequency, which in turn causes EMI disturbance to the environment. The purpose of the internal frequency modulation of the CPU-PLL allows energy to be distributed to many different frequencies which reduces the power peak.

A typical characteristic for a single frequency spectrum and a frequency modulated spectrum is shown in Figure 3.

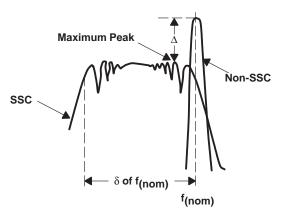


Figure 3. Frequency Power Spectrum With and Without the Use of SSC

The modulated spectrum has its distribution (left side) associated with the single-frequency spectrum which indicates a down-spread modulation.

The peak reduction depends on the modulation scheme and modulation profile. System performance and timing requirements are the limiting factors for actual design implementations. The implementation was driven to keep the average clock frequency close to its upper specification limit. The modulation amount was set to approximately -0.6%.

To allow a downstream PLL to follow the frequency modulated signal, the bandwidth of the modulation signal is limited in order to minimize SSC induced tracking skew jitter. The modulation frequency is approximately 31 kHz.



## PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
CDC950DGG	ACTIVE	TSSOP	DGG	48	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CDC950DGGG4	ACTIVE	TSSOP	DGG	48	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CDC950DGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CDC950DGGRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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## TAPE AND REEL INFORMATION





# QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



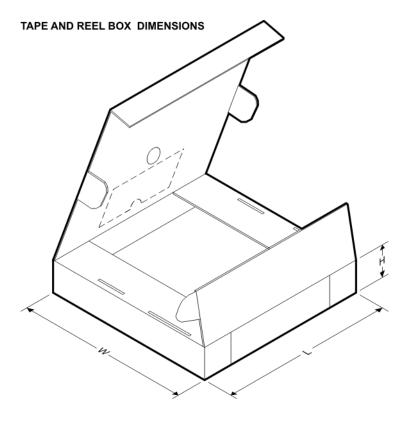
*All dimensions a	are nominal
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Device		Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDC950DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1



# PACKAGE MATERIALS INFORMATION

6-Aug-2008



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDC950DGGR	TSSOP	DGG	48	2000	333.2	345.9	31.8

# **MECHANICAL DATA**

MTSS003D - JANUARY 1995 - REVISED JANUARY 1998

#### DGG (R-PDSO-G\*\*)

#### PLASTIC SMALL-OUTLINE PACKAGE

**48 PINS SHOWN** 



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153



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