SN54BCT29825, SN74BCT29825 8-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

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- State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Package Options Include Plastic Small-Outline Packages (DW), Ceramic Chip Carriers (FK) and Flatpacks (W), and Standard Plastic and Ceramic 300-mil DIPs (JT, NT)

description

These 8-bit bus-interface flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

The eight flip-flops are edge-triggered D-type flip-flops. With the clock-enable (\overline{CLKEN}) input low, the device enters data on the low-to-high transition of the clock. Taking \overline{CLKEN} high disables the clock buffer, thus latching the outputs. Taking the clear (\overline{CLR}) input low causes the eight Q outputs to go low independently of the clock.

Buffered output-enable ($\overline{OE1}$, $\overline{OE2}$, or $\overline{OE3}$) inputs can be used to place the eight outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

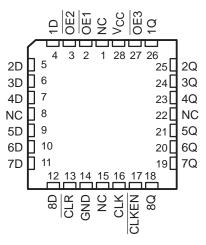
The output-enable inputs do not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54BCT29825 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74BCT29825 is characterized for operation from 0°C to 70°C.

SN74BCT29825DW OR NT PACKAGE (TOP VIEW)								
OE1	1 U	24	V _{CC}					
OE2	2	23	OE3					
1D[3	22	1Q					
2D 🛛	4	21	2Q					
3D 🛛	5	20	3Q					
4D[6	19	4Q					
5D[7	18	5Q					
6D 🛛	8	17	6Q					
7D[9	16	7Q					
8D[10	15	8Q					
CLR[11	14	CLKEN					
GND[12	13	CLK					

SN54BCT29825 ... JT OR W PACKAGE

SN54BCT29825 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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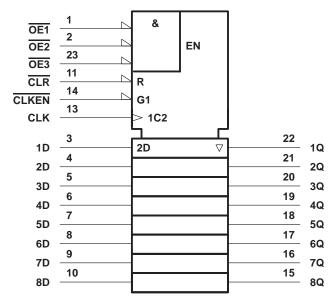
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FUNCTION TABLE								
	INPUTS							
<u>OE</u> †	CLR	CLKEN	CLK	D	Q			
L	L	Х	Х	Х	L			
L	Н	L	\uparrow	Н	Н			
L	Н	L	\uparrow	L	L			
L	Н	Н	H or L	Х	Q ₀			
н	Х	Х	Х	Х	Z			

 $+ \overline{OE} = H$ if any of the output-enable inputs is high.

 $\overline{OE} = L$ if all of the output-enable inputs are low.

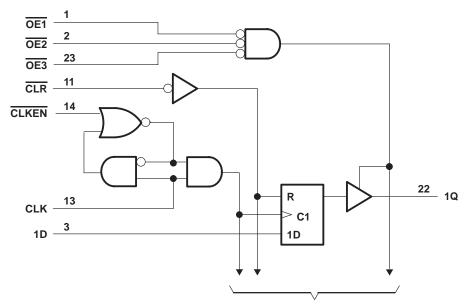
logic symbol[‡]



[‡] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DW, JT, NT, and W packages.



logic diagram (positive logic)



To Seven Other Channels

Pin numbers shown are for the DW, JT, NT, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}	–0.5 V to 7 V
Input voltage range, V _I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, VO	–0.5 V to 5.5 V
Voltage range applied to any output in the high state, VO	$\dots -0.5$ V to V _{CC}
Input clamp current, I _{IK} (V _I < 0)	
Current into any output in the low state, IO: SN54BCT29825	48 mA
SN74BCT29825	96 mA
Operating free-air temperature range: SN54BCT29825	–55°C to 125°C
SN74BCT29825	0°C to 70°C
Storage temperature range	−65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

		SN54BCT29825			SN7			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			0.8	V
Iк	Input clamp current			-18			-18	mA
ЮН	High-level output current	-15		-24	mA			
IOL	Low-level output current			24			48	mA
ТА	Operating free-air temperature	-55		125	0		70	°C



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

			SN5	4BCT29	825	SN7			
PARAMETER	TES	ST CONDITIONS	MIN	TYP†	MAX	MIN	TYP†	MAX	UNIT
VIK	$V_{CC} = 4.5 V,$	lj = -18 mA			-1.2			-1.2	V
		I _{OH} = -15 mA	2	3.2		2.4	3.3		
VOH	$V_{CC} = 4.5 V$	I _{OH} = – 24 mA				2	3.1		V
	V _{CC} = 4.75 V,	$I_{OH} = -3 \text{ mA}$				2.7			
Max		I _{OL} = 24 mA		0.38	0.55				V
VOL	$V_{CC} = 4.5 V$	I _{OL} = 48 mA					0.42	0.55	V
lį	V _{CC} = 5.5 V,	$V_{I} = 7 V$			0.1			0.1	mA
IIН	$V_{CC} = 5.5 V,$	V _I = 2.7 V	-10		-75	-10		-75	μA
١ _{١L}	V _{CC} = 5.5 V,	V _I = 0.5 V			-0.2			-0.2	mA
los‡	$V_{CC} = 5.5 V,$	$V_{O} = 0$	-75		-250	-75		-250	mA
IOZH	V _{CC} = 5.5 V,	V _O = 2.7 V			20			20	μΑ
IOZL	$V_{CC} = 5.5 V,$	V _O = 0.5 V			-20			-20	μΑ
ICCL	$V_{CC} = 5.5 V,$	Outputs open		26	40		26	40	mA
Іссн	V _{CC} = 5.5 V,	Outputs open		10	16		10	16	mA
ICCZ	V _{CC} = 5.5 V,	Outputs open		6	10		6	10	mA
Ci	V _{CC} = 5 V,	VI = 2.5 V or 0.5 V		5			5		pF
Co	V _{CC} = 5 V,	V _O = 2.5 V or 0.5 V		7			7		pF

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[‡]Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V _{CC} = 5 V, T _A = 25°C		SN54BCT29825		SN74BCT29825		UNIT	
			MIN	MAX	MIN	MAX	MIN	MAX		
fclock	Clock frequency		0	125	0	125	0	125	MHz	
		CLR low	4		4		4			
tw	t _w Pulse duration	CLK high or low	4		4		4		ns	
	t _{SU} Setup time before CLK [↑]	Data high	6		6		6			
		Data low	3.5		3.5		3.5			
tsu		CLR	1		1		1		ns	
		CLKEN high or low	8		8		8			
		Data high	1.5		1.5		1.5			
th	th Hold time after CLK↑	Data low	0		0		0		ns	
		CLKEN high or low	0.5		0.5		0.5			



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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Note 2)

PARAMETER FROM		TO	V ₍ T	V _{CC} = 5 V, T _A = 25°C		SN54BCT29825		SN74BCT29825		UNIT
	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}			125			125		125		MHz
^t PLH	<u>our</u>	0	2.2	5.4	7.8	2.2	9.9	2.2	9	
^t PHL	CLK	Q	3.1	5.9	7.7	3.1	9.1	3.1	8.4	ns
^t PHL	CLR	Q	3	6.4	8.3	3	9.6	3	9.5	ns
^t PZH	OE	0	2.1	6.2	8.4	2.1	10.8	2.1	10.3	
^t PZL	ÛE	Q	5.1	9.1	11.4	5.1	13.6	5.1	13.2	ns
^t PHZ	OE	Q	2.4	5.9	7.8	2.4	9.8	2.4	9	
^t PLZ		Q	1.8	5.2	7.2	1.8	9.2	1.8	8.2	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.



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