SCLS400G - APRIL 1998 - REVISED APRIL 2005

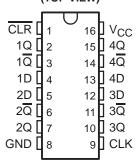
- 2-V to 5.5-V V<sub>CC</sub> Operation
- Max t<sub>pd</sub> of 7.5 ns at 5 V
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   <0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- Typical V<sub>OHV</sub> (Output V<sub>OH</sub> Undershoot)
   >2.3 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- Support Mixed-Mode Voltage Operation on All Ports
- Contain Four Flip-Flops With Double-Rail Outputs
- Applications Include:
  - Buffer/Storage Registers
  - Shift Registers
  - Pattern Generators
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

#### description/ordering information

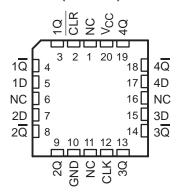
The 'LV175A devices are quadruple D-type flip-flops designed for 2-V to 5.5-V  $V_{CC}$  operation.

These devices have a direct clear (CLR) input and feature complementary outputs from each flip-flop.

#### SN54LV175A . . . J OR W PACKAGE SN74LV175A . . . D, DB, DGV, NS, OR PW PACKAGE (TOP VIEW)



# SN54LV175A . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

#### ORDERING INFORMATION

TA	PACK	AGE <sup>†</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	0010 B	Tube of 40	SN74LV175AD	11/4754
	SOIC - D	Reel of 2500	SN74LV175ADR	LV175A
	SOP - NS	Reel of 2000	SN74LV175ANSR	74LV175A
4000 1- 0500	SSOP – DB	Reel of 2000	SN74LV175ADBR	LV175A
–40°C to 85°C		Tube of 90	SN74LV175APW	
	TSSOP - PW	Reel of 2000	SN74LV175APWR	LV175A
		Reel of 250	SN74LV175APWT	
	TVSOP - DGV	Reel of 2000	SN74LV175ADGVR	LV175A
	CDIP – J	Tube of 25	SNJ54LV175AJ	SNJ54LV175AJ
–55°C to 125°C	CFP – W	Tube of 150	SNJ54LV175AW	SNJ54LV175AW
	LCCC - FK	Tube of 55	SNJ54LV175AFK	SNJ54LV175AFK

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design quidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



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#### description/ordering information (continued)

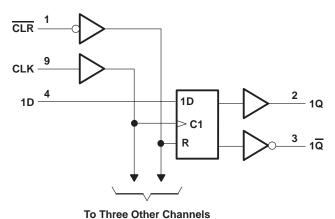
Information at the data (D) inputs meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock (CLK) pulse.

Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going edge of CLK. When CLK is at either the high or low level, the D input has no effect at the output.

FUNCTION TABLE (each flip-flop)

	INPUTS		OUTI	PUTS
CLR	CLK	Q	Q	
L	Х	Χ	L	Н
Н	$\uparrow$	Н	Н	L
Н	$\uparrow$	L	L	Н
Н	L	Χ	$Q_0$	$\overline{Q}_0$

#### logic diagram (positive logic)



Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.



### SN54LV175A, SN74LV175A QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>		
Input voltage range, V <sub>I</sub> (see Note 1)		–0.5 V to 7 V
Voltage range applied to any output in the high	n-impedance	
or power-off state, V <sub>O</sub> (see Note 1)		0.5 V to 7 V
Output voltage range, VO (see Notes 1 and 2)		
Input clamp current, $I_{IK}$ ( $V_I < 0$ )		–20 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)		
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )		±25 mA
Continuous current through V <sub>CC</sub> or GND		
Package thermal impedance, θ <sub>JA</sub> (see Note 3)		
,	DB package	
	DGV package	
	NS package	
	PW package	
Storage temperature range, T <sub>stg</sub>	. •	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. This value is limited to 5.5 V maximum.
- 3. The package thermal impedance is calculated in accordance with JESD 51-7.



### SN54LV175A, SN74LV175A QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

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#### recommended operating conditions (see Note 4)

			SN54L	.V175A	SN74L	.V175A	
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		2	5.5	2	5.5	V
		V <sub>CC</sub> = 2 V	1.5		1.5		
Maria	High lavelingut vallage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	V <sub>CC</sub> × 0.7		$V_{CC} \times 0.7$		V
VIH	High-level input voltage	$V_{CC} = 3 V \text{ to } 3.6 V$	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		$V_{CC} = 2 V$		0.5		0.5	
Mari	Low lovel input valtage	$V_{CC}$ = 2.3 V to 2.7 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	V
V <sub>IL</sub>	Low-level input voltage	$V_{CC} = 3 V \text{ to } 3.6 V$		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		V <sub>C</sub> C×0.3		$V_{CC} \times 0.3$	
٧ı	Input voltage		0	5.5	0	5.5	V
٧o	Output voltage		0 ,	Vcc	0	VCC	V
		$V_{CC} = 2 V$	S	-50		-50	μΑ
	I liab lavel autout aumant	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	90	-2		-2	
ЮН	High-level output current	$V_{CC} = 3 V \text{ to } 3.6 V$	d'a	-6		-6	mA
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		-12		-12	
		$V_{CC} = 2 V$		50		50	μΑ
	Lauria and autout aumant	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		2		2	
lOL	Low-level output current	$V_{CC} = 3 V \text{ to } 3.6 V$		6		6	mA
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		12		12	
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		200		200	
Δt/Δν	Input transition rise or fall rate	$V_{CC} = 3 V \text{ to } 3.6 V$		100		100	ns/V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		20		20	
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

242445	TEGT CONDITIONS		SN54	LV175A		SN74	LV175A	١	
PARAMETER	TEST CONDITIONS	VCC	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
	I <sub>OH</sub> = -50 μA	2 V to 5.5 V	V <sub>CC</sub> -0.1			V <sub>CC</sub> -0.1			
.,	$I_{OH} = -2 \text{ mA}$	2.3 V	2			2			.,,
Voн	$I_{OH} = -6 \text{ mA}$	3 V	2.48	_		2.48			V
	I <sub>OH</sub> = −12 mA	4.5 V	3.8	14		3.8			
	I <sub>OL</sub> = 50 μA	2 V to 5.5 V		JE [	0.1			0.1	
V	$I_{OL} = 2 \text{ mA}$	2.3 V		2	0.4			0.4	V
VOL	I <sub>OL</sub> = 6 mA	3 V		5	0.44			0.44	V
	I <sub>OL</sub> = 12 mA	4.5 V	200		0.55			0.55	
lį	$V_I = 5.5 \text{ V or GND}$	0 to 5.5 V	Q'		±1			±1	μΑ
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			20			20	μΑ
l <sub>off</sub>	$V_I$ or $V_O = 0$ to 5.5 $V$	0			5			5	μΑ
Ci	$V_I = V_{CC}$ or GND	3.3 V		1.4			1.4		pF

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# timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 2.5 V $\pm$ 0.2 V (unless otherwise noted) (see Figure 1)

			T <sub>A</sub> = 2	25°C	SN54L	/175A	SN74L	/175A	
			MIN	MAX	MIN	MAX	MIN	MAX	UNIT
	Dulan dura Can	CLR low	6		6		6		
t <sub>W</sub>	Pulse duration	CLK high or low	6.5		7	10,01	7		ns
	Outure these beginning OLIKA	Data	7		7.5	M	7.5		
t <sub>su</sub>	Setup time before CLK↑	CLR inactive	7		7.5		7.5		ns
th	Hold time, data after CLK↑		0.5		1		1		ns

# timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V $\pm$ 0.3 V (unless otherwise noted) (see Figure 1)

			$T_A = 1$	25°C	SN54L	/175A	SN74L	/175A	
			MIN	MAX	MIN	MAX	MIN	MAX	UNIT
	Poles desettes	CLR low	5		5		5		
t <sub>W</sub>	Pulse duration	CLK high or low	5		5	N.C.	5		ns
	Outure the before OUK	Data	5		5	MIL	5		
t <sub>su</sub>	Setup time before CLK↑	CLR inactive	5		5		5		ns
t <sub>h</sub>	Hold time, data after CLK↑		1		1		1		ns

# timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

			T <sub>A</sub> = 2	25°C	SN54L	√175A	SN74LV	/175A	LINUT
			MIN	MAX	MIN	MAX	MIN	MAX	UNIT
	Dulas dimetias	CLR low	5		5		5		
t <sub>W</sub>	Pulse duration	CLK high or low	5		5	10,01	5		ns
Ţ.	Outure the before OUK	Data	4		4	M	4		
t <sub>su</sub>	Setup time before CLK↑	CLR inactive	5		5		5		ns
t <sub>h</sub>	Hold time, data after CLK↑		1		1		1		ns

# switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 2.5 V $\pm$ 0.2 V (unless otherwise noted) (see Figure 1)

	FROM	то	LOAD	T,	<sub>Δ</sub> = 25°C	;	SN54L\	/175A	SN74L\	/175A	
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
4			C <sub>L</sub> = 15 pF	50*	105*		45*	3	45		NAL I-
<sup>T</sup> max			C <sub>L</sub> = 50 pF	40	80		35	1/4	35		MHz
	CLR	Any	0. 45.5		7.9*	16.6*	1*	20*	1	20	
<sup>t</sup> pd	CLK	Any	$C_L = 15 pF$		9.3*	18.8*	1*/	22*	1	22	ns
	CLR	Any	0 50 5		10.4	21.6	<del>4</del> )	25.5	1	25.5	
<sup>t</sup> pd	CLK	Any	$C_L = 50 pF$		12	23.3	01	27	1	27	ns
tsk(o)			C <sub>L</sub> = 50 pF			2	6			2	ns

<sup>\*</sup> On products compliant to MIL-PRF-38535, this parameter is not production tested.



### SN54LV175A, SN74LV175A QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

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# switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V $\pm$ 0.3 V (unless otherwise noted) (see Figure 1)

DADAMETER	FROM	то	LOAD	T,	4 = 25°C	;	SN54L\	/175A	SN74L\	/175A	LINUT
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
4			C <sub>L</sub> = 15 pF	90*	155*		75*	4	75		N 41 1-
f <sub>max</sub>			C <sub>L</sub> = 50 pF	50	120		45	1/4	45		MHz
	CLR	Any	0 45 5		5.5*	10.1*	1*	12*	1	12	
<sup>t</sup> pd	CLK	Any	$C_L = 15 pF$		6.5*	11.5*	1*	13.5*	1	13.5	ns
,	CLR	Any	0 50 5		7.4	13.6	3	15.5	1	15.5	
<sup>t</sup> pd	CLK	Any	$C_L = 50 pF$		8.4	15	01	17	1	17	ns
tsk(o)			C <sub>L</sub> = 50 pF			1.5	Q			1.5	ns

<sup>\*</sup> On products compliant to MIL-PRF-38535, this parameter is not production tested.

# switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

	FROM	то	LOAD	T,	<sub>Δ</sub> = 25°C	;	SN54L\	/175A	SN74L	/175A	
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
			C <sub>L</sub> = 15 pF	150*	215*		125*	4	125		MI I-
f <sub>max</sub>			C <sub>L</sub> = 50 pF	85	165		75	1/4	75		MHz
4 .	CLR	Any	0. 45 = 5		3.7*	6.4*	1*	7.5*	1	7.5	
t <sub>pd</sub>	CLK	Any	$C_L = 15 pF$		4.6*	7.3*	1*	8.5*	1	8.5	ns
	CLR	Any	0 50 5		5.3	8.4	<del>4</del> 9	9.5	1	9.5	
<sup>t</sup> pd	CLK	Any	$C_L = 50 pF$	·	6	9.3	01	10.5	1	10.5	ns
tsk(o)			C <sub>L</sub> = 50 pF			1	Ya			1	ns

<sup>\*</sup> On products compliant to MIL-PRF-38535, this parameter is not production tested.

### noise characteristics, $V_{CC} = 3.3 \text{ V}$ , $C_L = 50 \text{ pF}$ , $T_A = 25^{\circ}\text{C}$ (see Note 5)

	DADAMETED	SN	74LV175	iΑ	
	PARAMETER	MIN	TYP	MAX	UNIT
V <sub>OL(P)</sub>	Quiet output, maximum dynamic V <sub>OL</sub>		0.3	8.0	V
V <sub>OL(V)</sub>	Quiet output, minimum dynamic V <sub>OL</sub>		-0.3	-0.8	V
V <sub>OH(V)</sub>	Quiet output, minimum dynamic VOH		3		V
V <sub>IH(D)</sub>	High-level dynamic input voltage	2.31			V
V <sub>IL(D)</sub>	Low-level dynamic input voltage			0.99	V

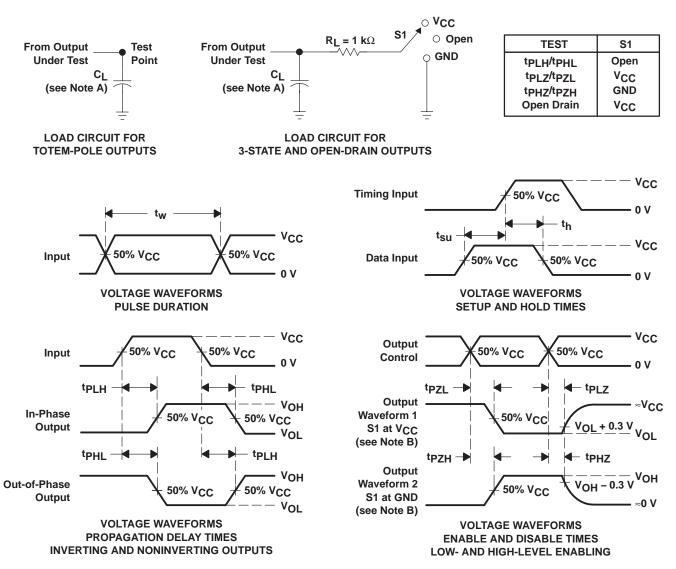
NOTE 5: Characteristics are for surface-mount packages only.

### operating characteristics, T<sub>A</sub> = 25°C

	PARAMETER			TEST CONDITIONS			UNIT
ſ	<u> </u>	Down dissination conseitance	C:	f 40 MH-	3.3 V	13.6	, F
	Cpd	Power dissipation capacitance	$C_L = 50 pF$ ,	f = 10 MHz	5 V	14.5	pF



#### PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_Q = 50 \Omega$ ,  $t_f \leq 3$  ns,  $t_f \leq 3$  ns.
  - D. The outputs are measured one at a time, with one input transition per measurement.
  - E. tpLZ and tpHZ are the same as tdis.
  - F. tpzi and tpzH are the same as ten.
  - G. tpHL and tpLH are the same as tpd.
  - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms





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#### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74LV175AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV175ADE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV175ADG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV175ADGVR	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV175ADGVRE4	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV175ADGVRG4	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV175ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV175ADRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV175ADRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV175ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV175ANSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV175ANSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV175APW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV175APWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV175APWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV175APWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV175APWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV175APWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV175APWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV175APWTE4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV175APWTG4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.



#### PACKAGE OPTION ADDENDUM

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(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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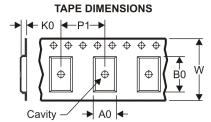
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

### PACKAGE MATERIALS INFORMATION

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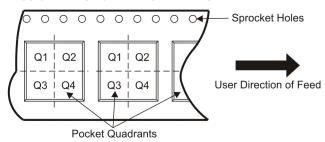
#### TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device		Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV175ADGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV175ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LV175ANSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LV175APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV175APWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

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\*All dimensions are nominal

All differences are frominal									
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)		
SN74LV175ADGVR	TVSOP	DGV	16	2000	346.0	346.0	29.0		
SN74LV175ADR	SOIC	D	16	2500	333.2	345.9	28.6		
SN74LV175ANSR	SO	NS	16	2000	346.0	346.0	33.0		
SN74LV175APWR	TSSOP	PW	16	2000	346.0	346.0	29.0		
SN74LV175APWT	TSSOP	PW	16	250	346.0	346.0	29.0		

#### DGV (R-PDSO-G\*\*)

#### **24 PINS SHOWN**

#### **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. Falls within JEDEC: 24/48 Pins – MO-153 14/16/20/56 Pins – MO-194



## D (R-PDS0-G16)

#### PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



PW (R-PDSO-G16)

#### PLASTIC SMALL OUTLINE

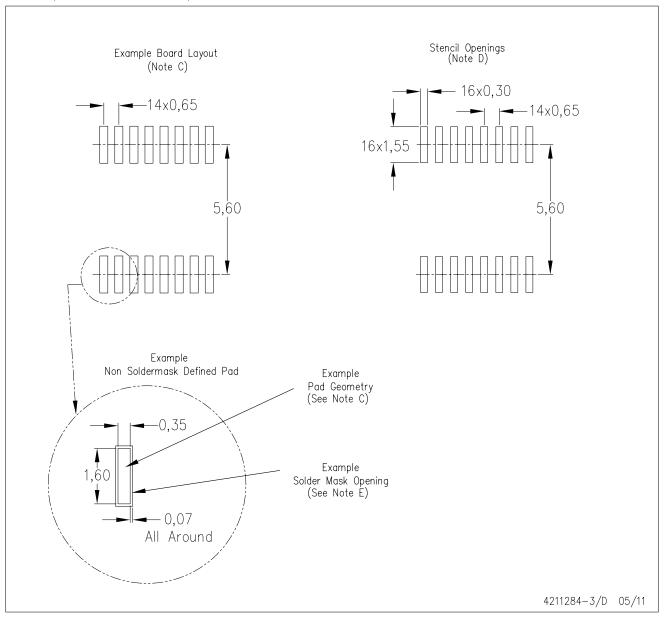


- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



# PW (R-PDSO-G16)

## PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



#### **MECHANICAL DATA**

### NS (R-PDSO-G\*\*)

## 14-PINS SHOWN

#### PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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